AMC0100R Precision, ±250mV Input, Functionally Isolated Amplifier With Single-Ended, Ratiometric Output

1 Features

- Linear input voltage range: ±250mV
- Supply voltage range:
  - High-side (VDD1): 3.0V to 5.5V
  - Low-side (VDD2): 3.0V to 5.5V
- Single-ended, ratiometric output
  - Reference Input: 2.7V to 5.5V
- Low DC errors:
  - Offset error: ±0.25mV (maximum)
  - Offset drift: ±1µV/°C (maximum)
  - Gain error: ±0.25% (maximum)
  - Gain drift: ±35ppm/°C (maximum)
  - Nonlinearity: 0.04% (maximum)
- High CMTI: 150V/ns (minimum)
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Functional Isolation:
  - $200V_{RMS}$, $280V_{DC}$ working voltage
  - $570V_{RMS}$, $800V_{DC}$ transient overvoltage (60s)
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- 48V motor drives
- 48V frequency inverters
- Analog input modules
- Power supplies

3 Description

The AMC0100R is a precision, galvanically isolated amplifier with a ±250mV differential input, and single-ended, ratiometric output. The input is optimized for direct connection to a shunt resistor or other low-impedance signal source.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels or noise sensitive circuitry from power stages. The isolation barrier supports a working voltage up to $200V_{RMS}$ / $280V_{DC}$ and transient over voltages up to $570V_{RMS}$ / $800V_{DC}$ (60s).

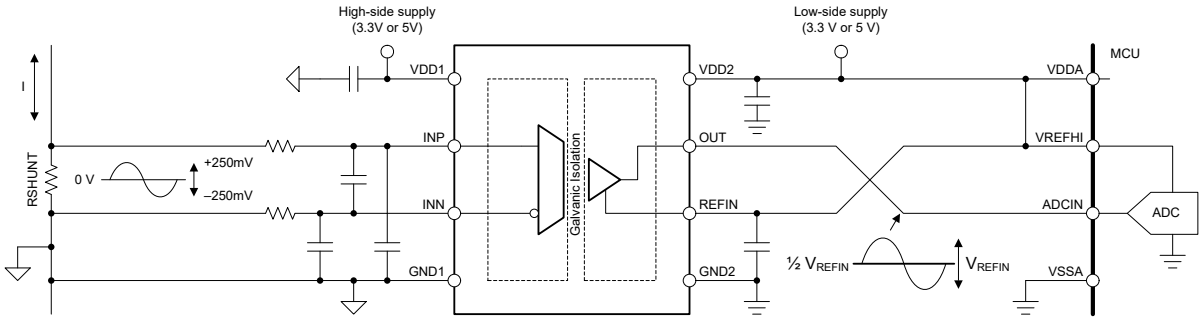
The AMC0100R outputs a single-ended signal proportional to the input voltage. The full-scale output is set by the voltage applied to the REFIN pin. The output of the AMC0100R is designed to connect directly to the input of an ADC. Connect REFIN to the same reference voltage as the ADC to match the dynamic input voltage range of the ADC.

The AMC0100R is available in a 8-pin, 0.65mm pitch VSON package and is fully specified over the temperature range from –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC0100R	DEN (VSON 8)	3.5mm × 2.7mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information (DEN Package)....6
5.5 Package Characteristics....6
5.6 Electrical Characteristics....7
5.7 Switching Characteristics....8
5.8 Timing Diagram....8
5.9 Typical Characteristics....9
6 Detailed Description....16
6.1 Overview....16
6.2 Functional Block Diagram....16
6.3 Feature Description....16
6.4 Device Functional Modes....18
7 Application and Implementation....20
7.1 Application Information....20
7.2 Typical Application....20
7.3 Best Design Practices....24
7.4 Power Supply Recommendations....25
7.5 Layout....25
8 Device and Documentation Support....26
8.1 Documentation Support....26
8.2 Receiving Notification of Documentation Updates....26
8.3 Support Resources....26
8.4 Trademarks....26
8.5 Electrostatic Discharge Caution....26
8.6 Glossary....26
9 Revision History....26
10 Mechanical, Packaging, and Orderable Information....26

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4 Pin Configuration and Functions

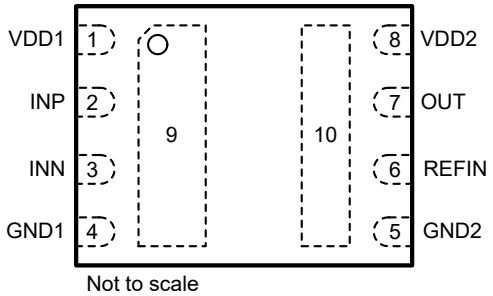

Figure 4-1. DEN Package, 8-pin VSON (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply[(1)]
2	INP	Analog input	Noninverting analog input[(2)]
3	INN	Analog Input	Inverting analog input[(2)]
4,9[(3)]	GND1	High-side ground	High-side analog ground
5,10[(3)]	GND2	Low-side ground	Low-side analog ground
6	REFIN	Analog input	The voltage applied to this pin sets the full-scale output of the device. Connect REFIN to a low-impedance source as described in the *Connecting the REFIN Pin* section.
7	OUT	Analog output	Analog output
8	VDD2	Low-side power	Low-side power supply[(1)]

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Input Filter Design* section for input filter design recommendations.
(3) Both pins are connected internally with a low-impedance path.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, INN to GND1	GND1 – 4	VDD1 + 0.5	V
Reference input voltage	REFIN to GND2	GND2 – 0.5	VDD2 + 0.5	V
Analog output voltage	OUT to GND2	GND2 – 0.5	VDD2 + 0.5	V
Transient isolation voltage[2]	AC voltage, t = 60s[3]		570	V_{RMS}
	DC voltage, t = 60s		800	V_{DC}
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Common-mode from left-side (pins1-4) to right-side (pins5-8) of the package.
(3) Cumulative.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD1	High-side power supply	VDD1 to GND1	3	5.0	5.5	V
VDD2	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Nominal differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$	–320		320	mV
V_{FSR}	Specified linear differential input voltage	$V_{IN} = V_{INP} – V_{INN}$	–250		250	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to GND1	–0.16		1	V
$C_{IN, EXT}$	Minimum external capacitance connected to the input	from INP to INN		10		nF
REFERENCE INPUT						
V_{REFIN}	Reference input voltage	REFIN to GND2	2.7		VDD2	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	OUT to GND2			500	pF
R_{LOAD}	Resistive load	OUT to GND2		10	1	kΩ
ISOLATION BARRIER						

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5.3 Recommended Operating Conditions (continued)

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IOWM}	Functional isolation working voltage[1]	AC voltage (sine wave)			200	V_{RMS}
		DC voltage			280	V_{DC}
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

(1) Common-mode from left-side (pins1-4) to right-side (pins5-8) of the package.

5.4 Thermal Information (DEN Package)

THERMAL METRIC[1]		DEN (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	23.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Package Characteristics

PARAMETER		TEST CONDITIONS	VALUE	UNIT
DEN PACKAGE				
CLR	External clearance	Shortest pin-to-pin distance through air	≥ 1	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	≥ 1	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
C_{IO}	Capacitance, input to output[1]	V_{IO} = 0.5 V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Resistance, input to output[1]	T_A = 25°C	> 10^{12}	Ω

(1) All pins on each side of the barrier are tied together, creating a two-pin device.

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5.6 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, V_{REFIN} = 3.3V, V_{INP} = –250mV to +250mV, and V_{INN} = 0V; typical specifications are at T_A = 25°C, VDD1 = 5V, VDD2 = 3.3V, and V_{REFIN} = 1.65V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
C_{IN}	Effective input sampling capacitance			1.8		pF
R_{IN}	Input impedance		25	27.5	30	kΩ
I_{INP}	Input current	$V_{IN} = (V_{INP} – V_{INN}) = V_{FSR, MAX}$		9		µA
I_{INN}	Input current	$V_{IN} = (V_{INP} – V_{INN}) = V_{FSR, MAX}$		–9		µA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1kV	150			V/ns
REFERENCE INPUT						
R_{REFIN}	Input Impedance	REFIN to GND2, V_{REFIN} = 3.3V, T_A = 25°C	65.3	76.8	88.3	kΩ
		REFIN to GND2, V_{REFIN} = 5V, T_A = 25°C	62	72.9	83.9	
TCR_{REFIN}	Input Impedance thermal drift			–235		ppm/°C
ANALOG OUTPUT						
	Nominal Gain			V_{REFIN} / 2 / |$V_{Clipping}$|		V/V
R_{OUT}	Output resistance			<0.2		Ω
	Output short-circuit current	OUT pin, sourcing or sinking, INN = INP = GND1 or VDD1, output shorted to either GND2 or VDD2		11		mA
DC ACCURACY						
V_{OS}	Offset voltage(1) (2)	T_A = 25°C, INP = INN = GND1	–0.25	±0.01	0.25	mV
TCV_{OS}	Offset drift(1) (2) (4)		–3.5	–1.8	1	µV/°C
E_G	Gain error(1)	T_A = 25°C	–0.25%	±0.04	0.25%	
TCE_G	Gain drift(1) (5)		–35	±5	35	ppm/°C
	Nonlinearity(1)		–0.04%		0.04%	
	Output noise	INP = INN = GND1, f_{IN} = 0Hz, BW = 100kHz brickwall filter		260		$µV_{RMS}$
CMRR	Common-mode rejection ratio	f_{IN} = 0Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–100		dB
		f_{IN} = 10kHz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–82		
PSRR	Power-supply rejection ratio(2)	VDD1 DC PSRR, INP = INN = GND1, VDD1 from 3V to 5.5V		–89		dB
		VDD1 AC PSRR, INP = INN = GND1, VDD1 with 10kHz / 100mV ripple		–81		
		VDD2 DC PSRR, INP = INN = GND1, VDD2 from 3.3V to 5.5V		–110		
		VDD2 AC PSRR, INP = INN = GND1, VDD2 with 10kHz / 100mV ripple		–82		
AC ACCURACY						
BW	Output bandwidth		250	280		kHz
THD	Total harmonic distortion(3)	f_{IN} = 10kHz		–80		dB
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10kHz		84		dB
	Signal-to-noise ratio	f_{IN} = 10kHz, BW = 100kHz		77		
POWER SUPPLY						
IDD1	High-side supply current			5.4	6.7	mA

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5.6 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, V_{REFIN} = 3.3V, V_{INP} = –250mV to +250mV, and V_{INN} = 0V; typical specifications are at T_A = 25°C, VDD1 = 5V, VDD2 = 3.3V, and V_{REFIN} = 1.65V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD2	Low-side supply current			5.0	7.6	mA
$VDD1_{UV}$	High-side undervoltage detection threshold	VDD1 rising	2.5	2.6	2.7	V
		VDD1 falling	1.9	2.0	2.1	
$VDD2_{UV}$	Low-side undervoltage detection threshold	VDD2 rising	2.3	2.5	2.7	V
		VDD2 falling	1.9	2.05	2.2	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (–40 to 125°C).
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125°C).

5.7 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.7		µs
t_f	Output signal fall time			1.7		µs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output		0.8	1.3	µs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output		2.5	3	µs
t_{AS}	Analog settling time	VDD1 step to 3.0V with VDD2 ≥ 3.0V, V_{REFIN} = 3.3V, to V_{OUT} valid, 0.1% settling		30	100	µs

5.8 Timing Diagram

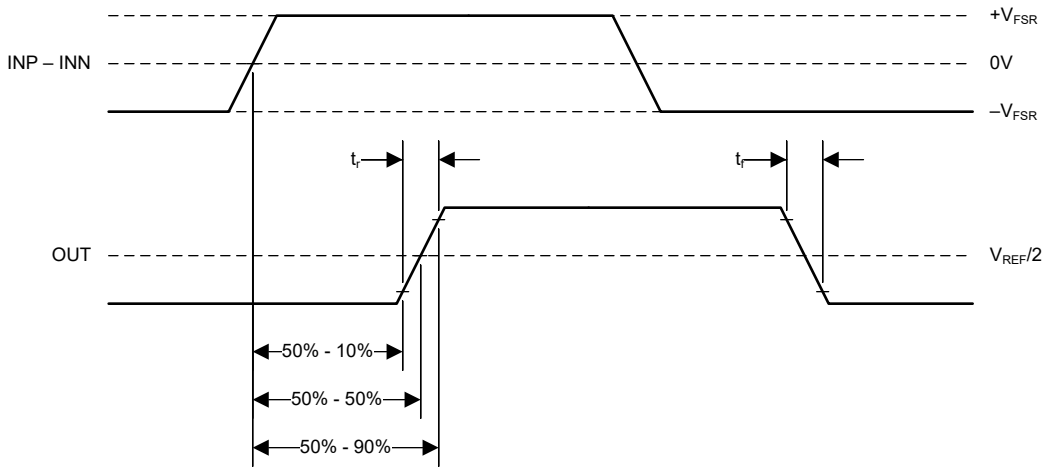

Figure 5-1. Rise, Fall, and Delay Time Waveforms

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5.9 Typical Characteristics

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

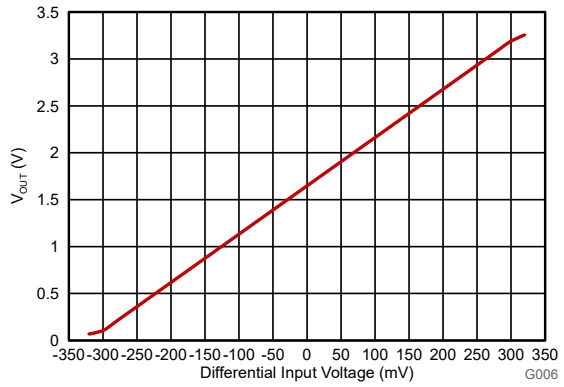
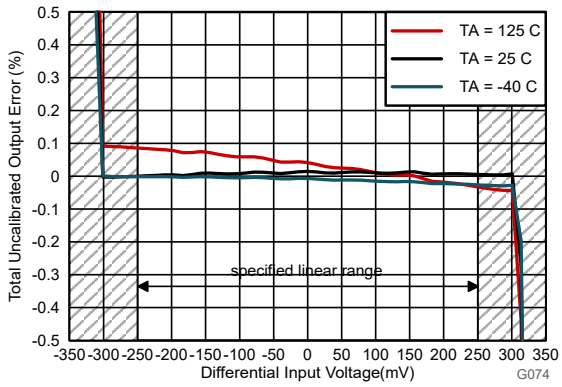


Figure 5-2. Output Voltage vs Input Voltage



Total uncalibrated output error is defined as:(($V_{OUT_Measured}$ – $V_{OUT_Expected}$) / V_{REFIN}) x 100 , where $V_{OUT_Expected}$ = V_{IN} / $V_{Clipping}$ x V_{REFIN} / 2 + V_{REFIN} / 2, V_{REFIN} = 3.3V and $V_{Clipping}$ = 0.32V

Figure 5-3. Unadjusted Error vs Input Voltage

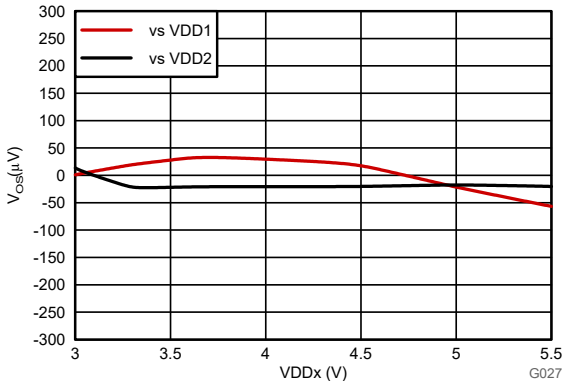


Figure 5-4. Input Offset Voltage vs Supply Voltage

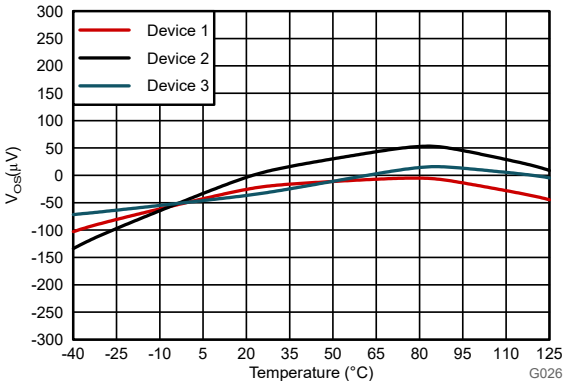
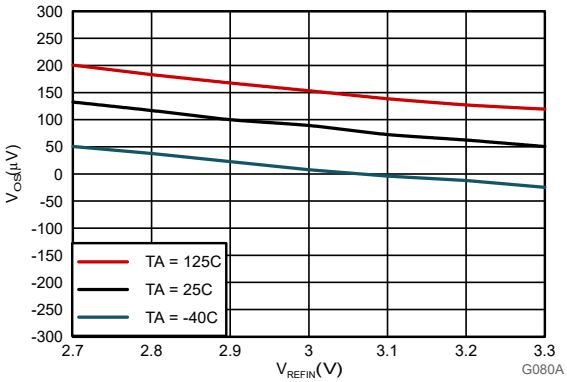
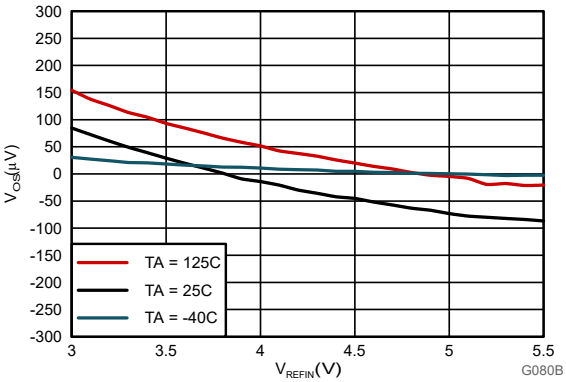


Figure 5-5. Input Offset Voltage vs Temperature



VDD2 = 3.3V

Figure 5-6. Input Offset Voltage vs VREFIN

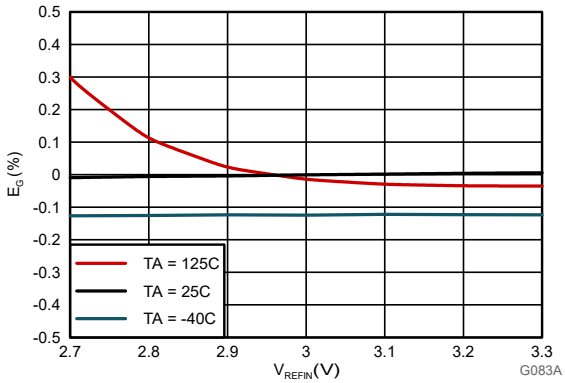


VDD2 = 5.5V

Figure 5-7. Input Offset Voltage vs VREFIN

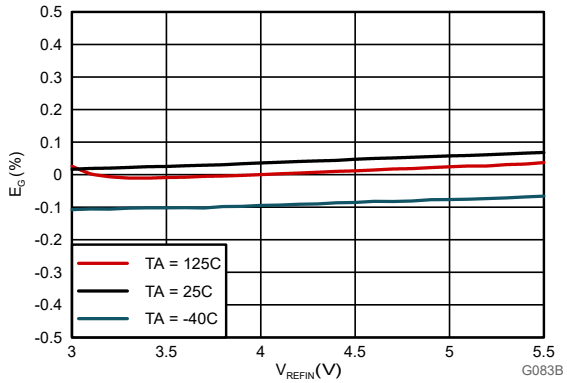
5.9 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)



VDD2 = 3.3V

Figure 5-8. Gain Error vs VREFIN



VDD2 = 5.5V

Figure 5-9. Gain Error vs VREFIN

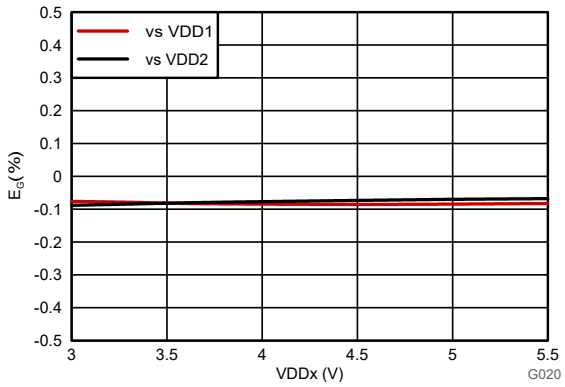


Figure 5-10. Gain Error vs Supply Voltage

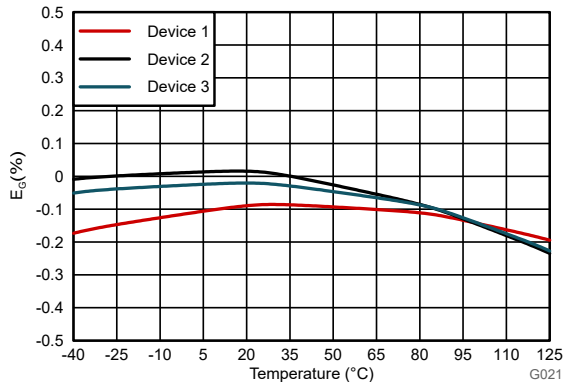


Figure 5-11. Gain Error vs Temperature

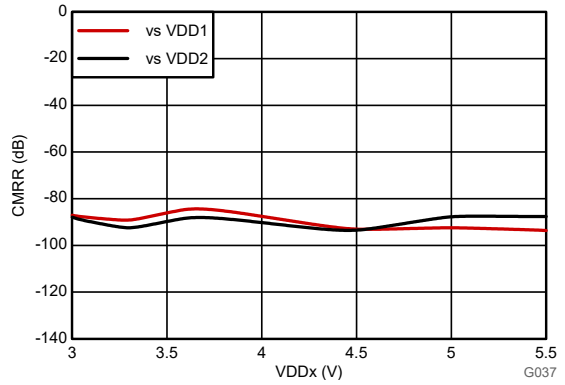


Figure 5-12. Common-Mode Rejection Ratio vs Supply Voltage

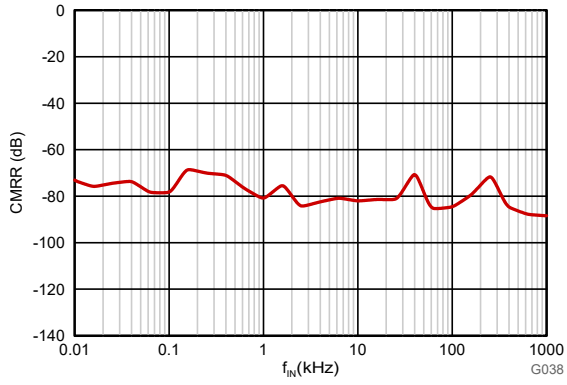


Figure 5-13. Common-Mode Rejection Ratio vs Input Frequency

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5.9 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

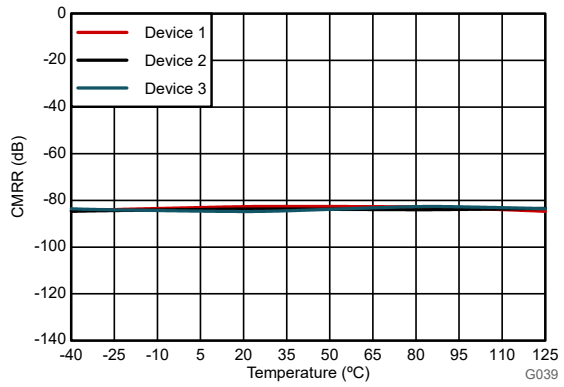

Figure 5-14. Common-Mode Rejection Ratio vs Temperature

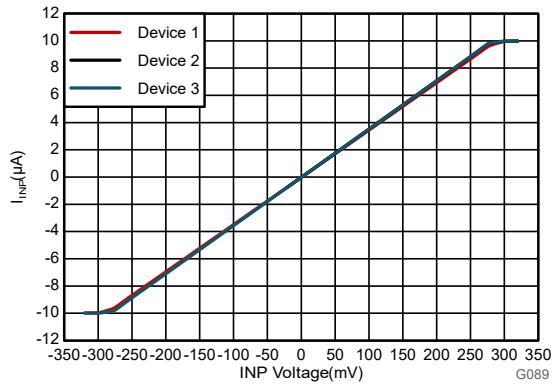

Figure 5-15. Input Current vs Input Voltage

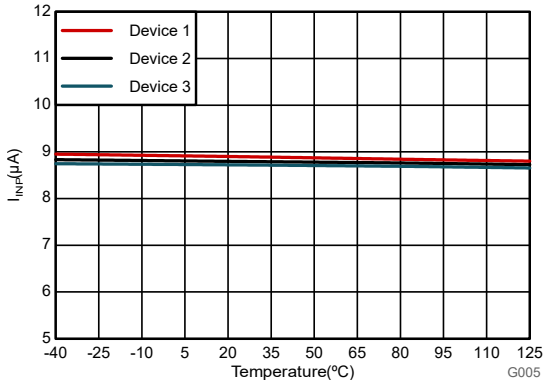

Figure 5-16. Input Current vs Temperature

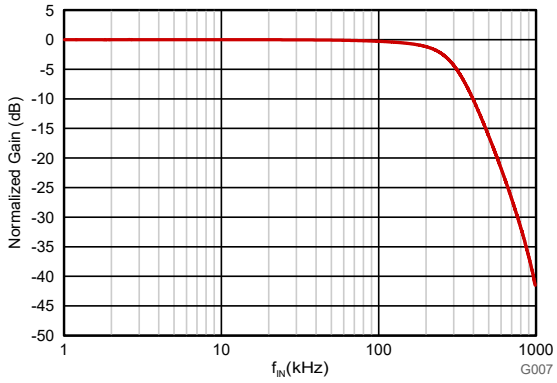

Figure 5-17. Normalized Gain vs Input Frequency

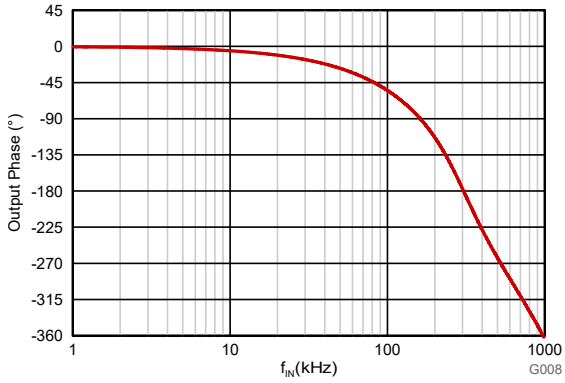

Figure 5-18. Output Phase vs Input Frequency

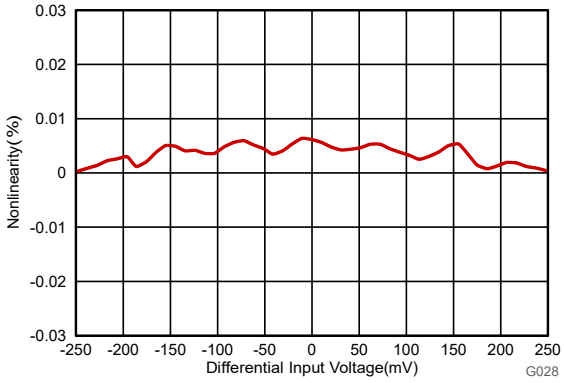

Figure 5-19. Nonlinearity vs Input Voltage

5.9 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

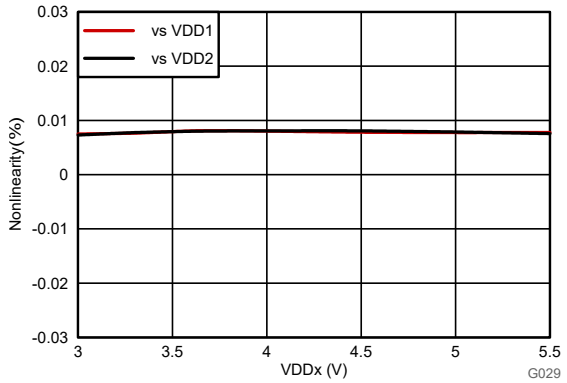

Figure 5-20. Nonlinearity vs Supply Voltage

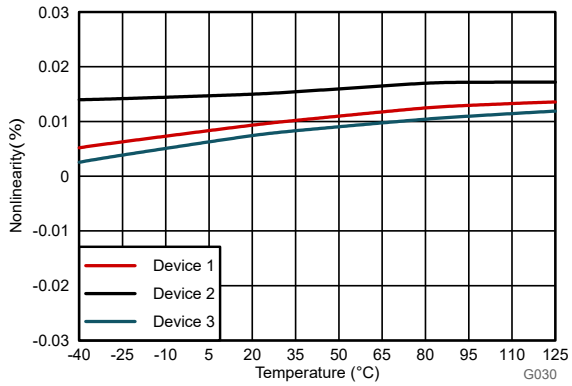

Figure 5-21. Nonlinearity vs Temperature

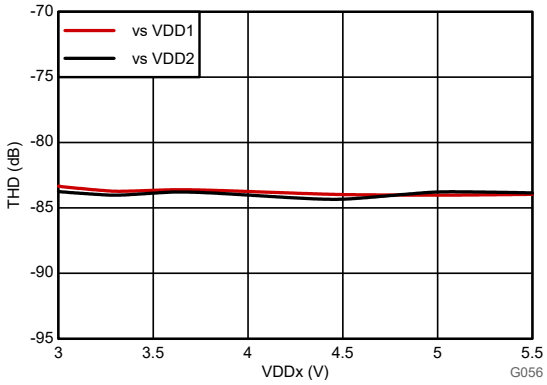

Figure 5-22. Total Harmonic Distortion vs Supply Voltage

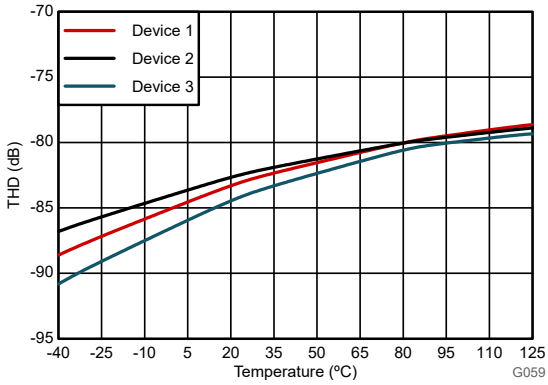

Figure 5-23. Total Harmonic Distortion vs Temperature

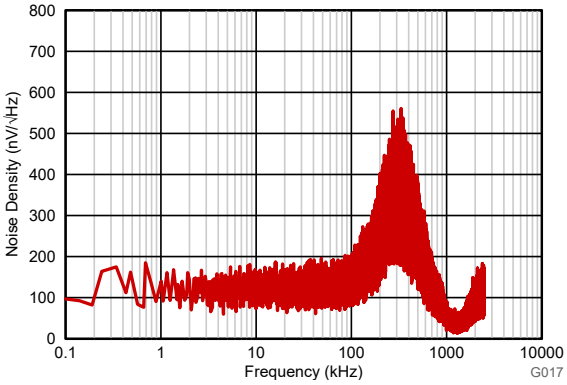

Figure 5-24. Input-Referred Noise Density vs Frequency

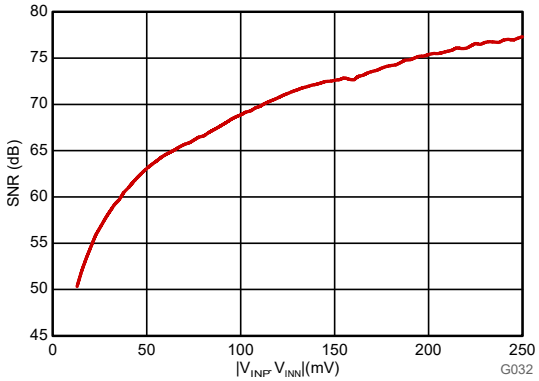

Figure 5-25. Signal-to-Noise Ratio vs Input Voltage

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5.9 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

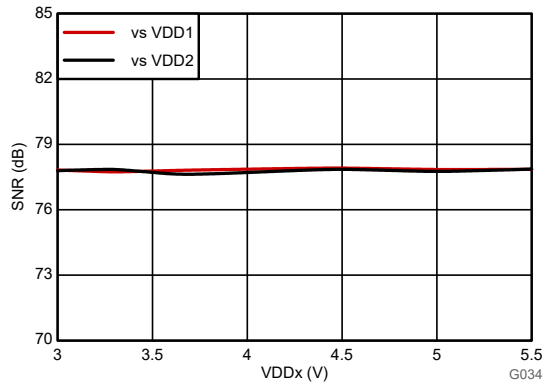

Figure 5-26. Signal-to-Noise Ratio vs Supply Voltage

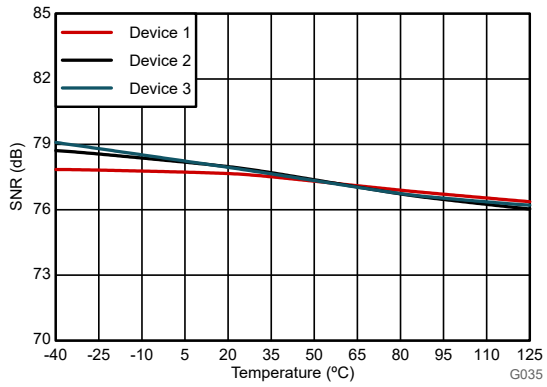

Figure 5-27. Signal-to-Noise Ratio vs Temperature

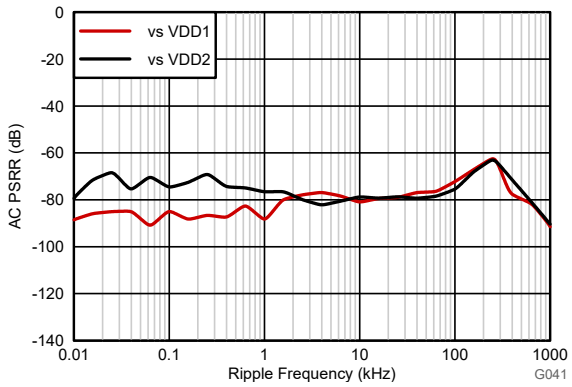

Figure 5-28. Power-Supply Rejection Ratio vs Ripple Frequency

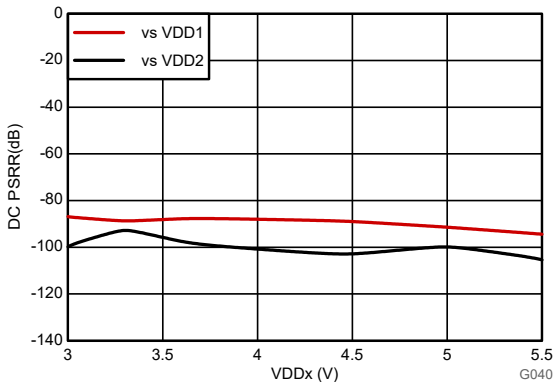

Figure 5-29. Power-Supply Rejection Ratio vs Supply Voltage

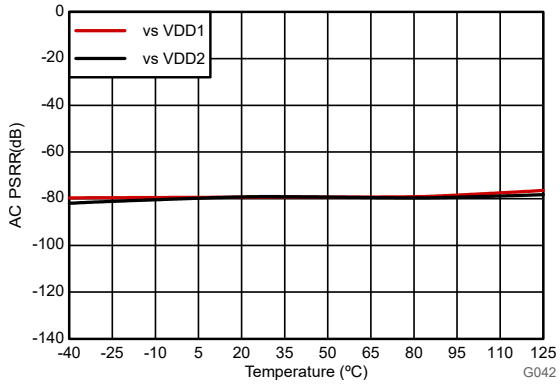

Figure 5-30. Power-Supply Rejection Ratio vs Temperature

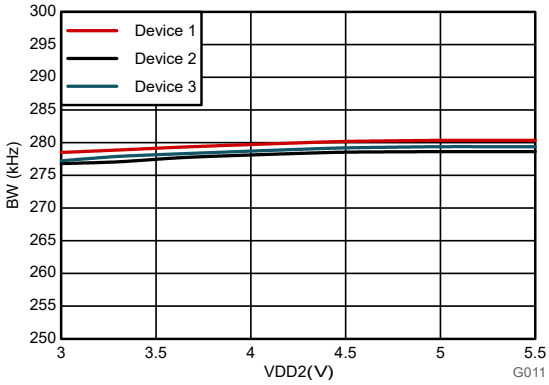

Figure 5-31. Output Bandwidth vs Low-Side Supply Voltage

5.9 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

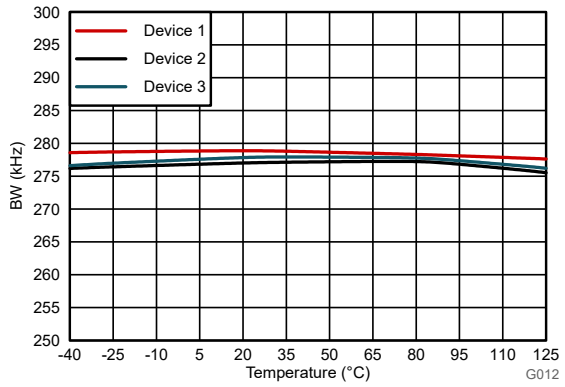

Figure 5-32. Output Bandwidth vs Temperature

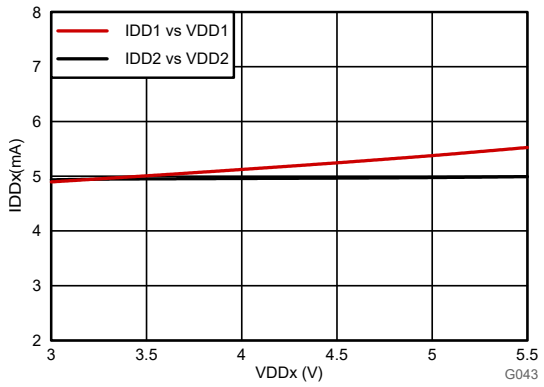

Figure 5-33. Supply Current vs Supply Voltage

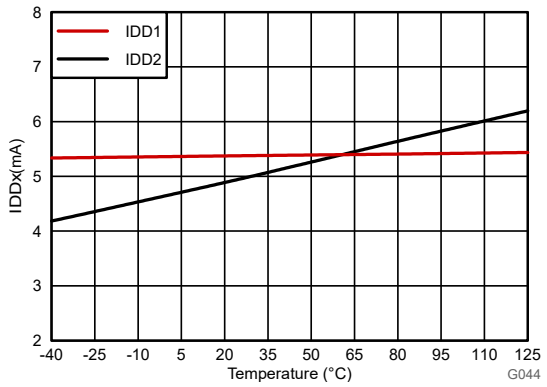

Figure 5-34. Supply Current vs Temperature

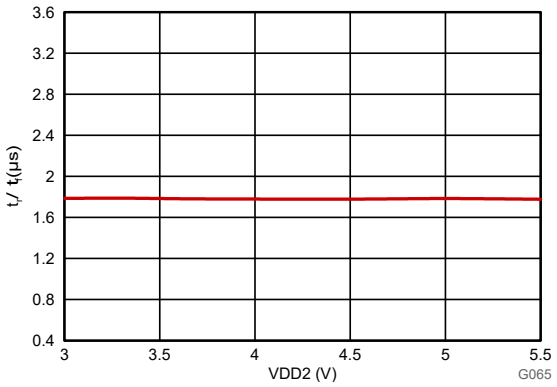

Figure 5-35. Output Rise and Fall Time vs Low-Side Supply

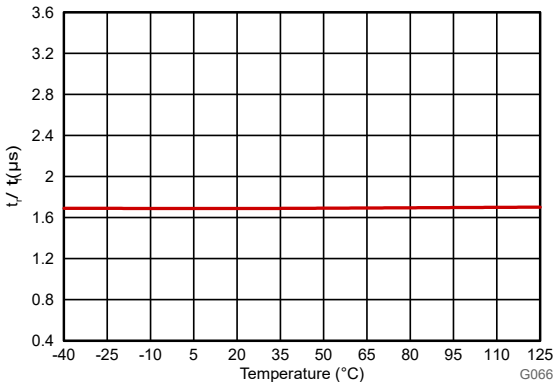

Figure 5-36. Output Rise and Fall Time vs Temperature

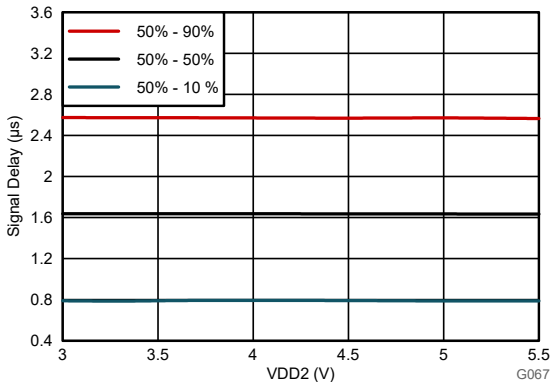

Figure 5-37. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

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5.9 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –250mV to 250mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

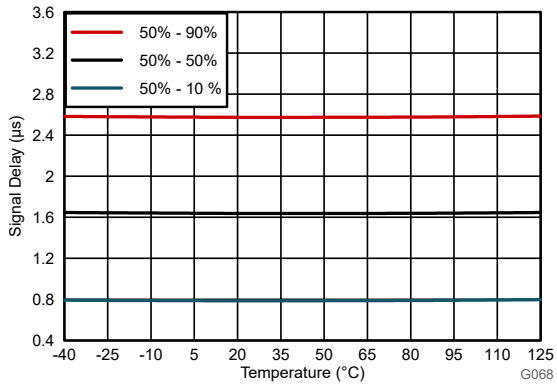


Figure 5-38. V_{IN} to V_{OUT} Signal Delay vs Temperature

6 Detailed Description

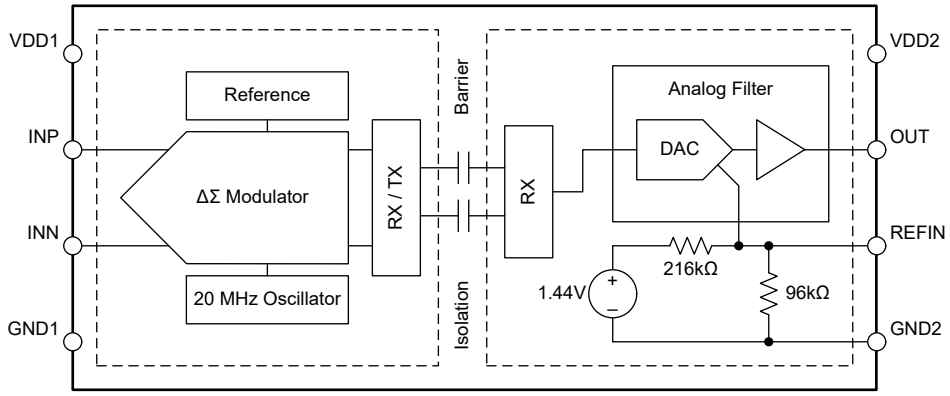
6.1 Overview

The AMC0100R is a precision, galvanically isolated amplifier with a ±250mV differential input, and single-ended, ratiometric output. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side.

On the low-side, the received bitstream is processed by an analog filter that outputs a GND2-referenced, single-ended signal at the OUT pin. This single-ended output signal is proportional to the input signal. The full-scale output voltage of the isolated amplifier is equal to the voltage applied to the REFIN pin.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation used in the AMC0100R transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Input

The high-impedance input buffer on the INP pin feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal. First, if the input voltage exceeds the value specified in the *Section 5.1* table, the input current must be limited to 10mA. This limitation is caused by the device input electrostatic discharge (ESD) diodes turning on. Second, linearity and noise performance are specified only when the input voltage is within the linear full-scale range (V_{FSR}). V_{FSR} is specified in the *Section 5.3* table.

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6.3.2 Isolation Channel Signal Transmission

As shown in Figure 6-1, the AMC0100R uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) is illustrated in the *Section 6.2* . TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0100R is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the analog filter. The AMC0100R transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

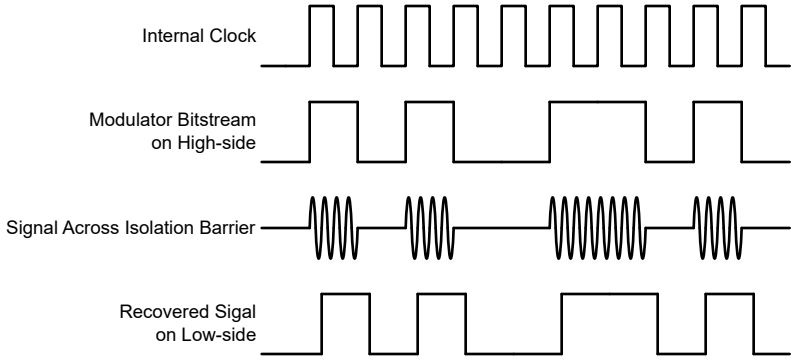

Figure 6-1. OOK-Based Modulation Scheme

6.3.3 Analog Output

The AMC0100R provides a single-ended analog output voltage proportional to the input voltage. The output is referred to GND2 and is galvanically isolated from the input of the device. The output is designed to connect directly to the input of an ADC.

The full-scale output voltage is set by the REFIN pin. For any input voltage within the specified linear input range, the device outputs a voltage equal to:

$$V_{OUT} = V_{IN} / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2 = (V_{INP} - V_{INN}) / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2 \quad (1)$$

Connect REFIN to the same reference voltage as a downstream ADC to match the ADC dynamic input voltage range. With a shared reference voltage, the ADC outputs a negative full-scale code when the negative clipping voltage is applied to the input of the AMC0100R. The ADC outputs the mid-range code when 0V is applied to the input of the AMC0100R. The ADC outputs a positive full-scale code when the positive clipping voltage is applied to the input of the AMC0100R.

The device is linear within the specified linear full-scale range. Beyond the linear full-scale range, the output continues to follow the input, but with reduced linearity performance. The output clips when the input voltage reaches the clipping voltage. Figure 6-2 shows the input-to-output transfer characteristic.

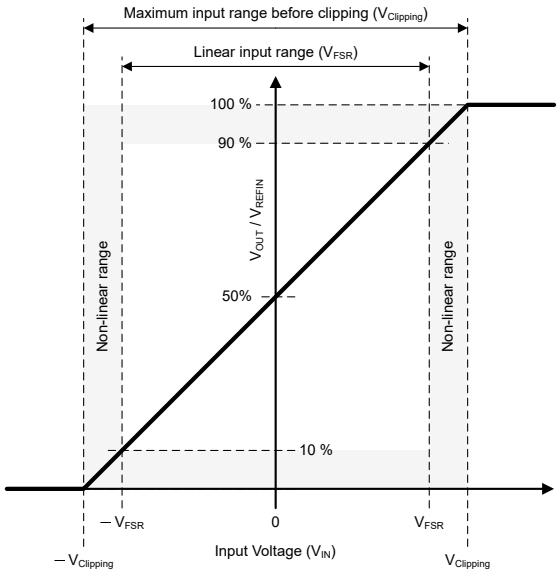

Figure 6-2. Input-to-Output Transfer Curve of the AMC0100R

6.4 Device Functional Modes

The AMC0100R operates in one of the following states:

- Off-state: The low-side supply (VDD2) is below the $VDD2_{UV}$ threshold. The device is not responsive. OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes.
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within recommended operating conditions. The high-side supply (VDD1) is below the $VDD1_{UV}$ threshold. The OUT pin is driven to V_{REFIN} / 2.
- Analog input overrange (positive full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is above the maximum clipping voltage $V_{Clipping, MAX}$. The device outputs V_{REFIN} at the OUT pin.
- Analog input underrange (negative full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is below the minimum clipping voltage $V_{Clipping, MIN}$. The OUT pin is driven to GND2.
- Normal operation: VDD1, VDD2, and V_{IN} are within the recommended operating conditions. The device outputs a voltage that is proportional to the input voltage.

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Table 6-1 lists the operating modes.

Table 6-1. Device Operational Modes

OPERATING CONDITION	VDD1	VDD2	V_{IN}	DEVICE RESPONSE
Off	Don't care	VDD2 < $VDD2_{UV}$	Don't care	OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes.
Missing high-side supply	VDD1 < $VDD1_{UV}$	Valid(1)	Don't care	The OUT pin is driven to V_{REFIN} / 2.
Input overrange	Valid(1)	Valid(1)	V_{IN} > $V_{Clipping, MAX}$	The device outputs V_{REFIN} at the OUT pin.
Input underrange	Valid(1)	Valid(1)	V_{IN} < $V_{Clipping, MIN}$	The OUT pin is driven to GND2.
Normal operation	Valid(1)	Valid(1)	Valid(1)	The device outputs a voltage that is proportional to the input voltage.

(1) *Valid* denotes operation within the recommended operating conditions.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC0100R a high-performance solution for industrial applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

7.2 Typical Application

Figure 7-1 shows the AMC0100R in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC0100R. The AMC0100R digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents that signal as a single ended voltage on the output pin.

The differential input, single ended output, and the high common-mode transient immunity (CMTI) of the AMC0100R provide reliable and accurate operation even in high-noise environments.

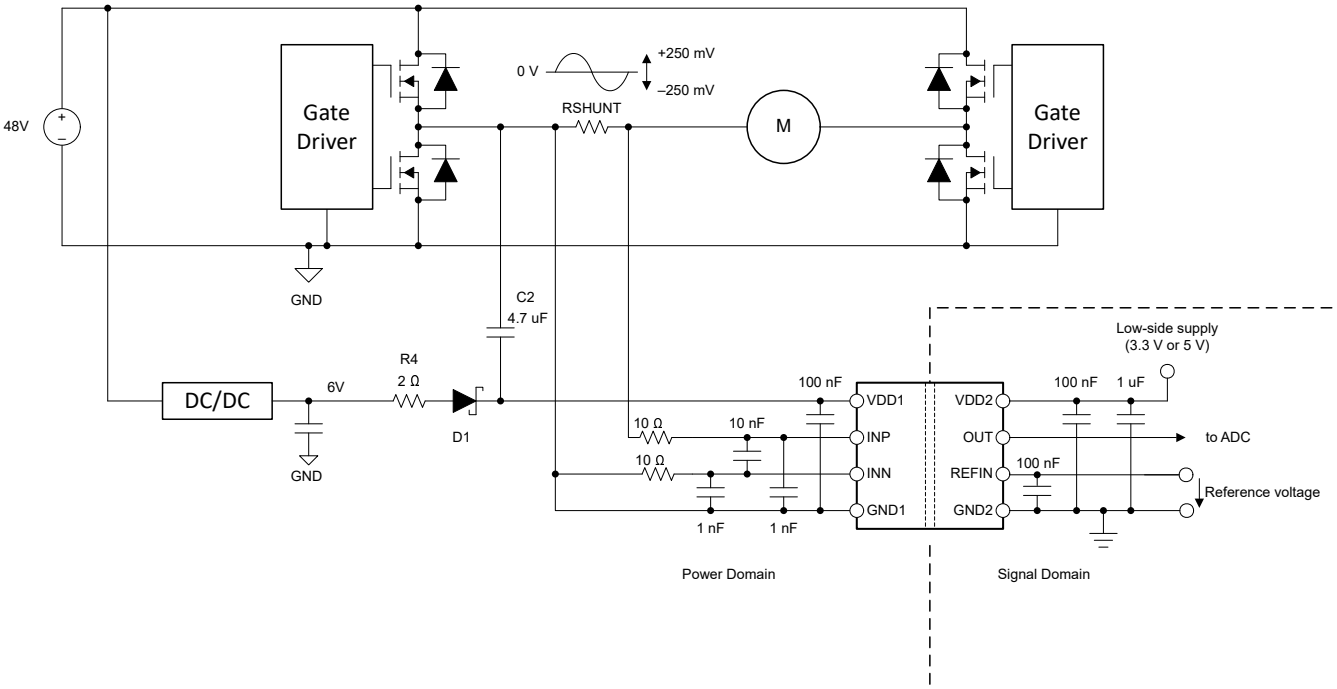

Figure 7-1. Using the AMC0100R for Current Sensing in a Typical Application

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7.2.1 Design Requirements

Table 7-1 lists the parameters for this typical application.

Table 7-1. Design Requirements

PARAMETER	VALUE
System voltage, power-stage	48V
Bootstrap supply voltage (V_{BS})	6V
Maximum ripple voltage on AVDD supply (V_{RIPPLE})	200mV
PWM frequency	16kHz
PWM duty cycle range	5% to 95%
Linear current sensing range	±5A

7.2.2 Detailed Design Procedure

In Figure 7-1, the high-side power supply (AVDD) is generated from a bootstrap circuit (R4, D1, C2).

The high-side ground reference (GND1) is derived from the end of the shunt resistor connected to the negative input of the AMC0100R (INN). For a four-terminal shunt, connect the device inputs to the inner leads of the shunt and connect GND1 to the outer leads. To minimize offset and improve accuracy, route the ground connection as a separate trace. Connect GND1 directly to the shunt resistor rather than shorting GND1 to INN at the input to the device. See the *Layout* section for more details.

7.2.2.1 Shunt Resistor Sizing

The shunt resistor (RSHUNT) value is determined by the device linear input voltage range (±250mV) and the desired linear current sensing range of ±5A. RSHUNT is calculated as 250mV / 5A = 50mΩ. The peak power dissipated in the shunt resistor is RSHUNT × $I_{PEAK}{}^2$ = 50mΩ × $(5A)^2$ = 1.25W. For a linear response, operate the shunt resistor at no more than 2/3 of the rated power. Therefore, a shunt resistor with a nominal power rating of approximately 1.8W is selected.

Select a lower shunt resistor value if transient overcurrents are expected in the system that exceed the linear input voltage range of the AMC0100R. However, if reduced linearity and lower resolution is acceptable for the overcurrent range, allow the voltage drop across the shunt to exceed the linear input voltage range up to the clipping voltage of the AMC0100R. In any case, make sure the voltage drop caused by the maximum overcurrent does not exceed the input voltage that causes a clipping output. That is, make sure $|V_{SHUNT}| \leq |V_{Clipping}|$.

7.2.2.2 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

Place capacitors C6 and C7 to improve common-mode rejection at high frequencies (>1MHz) and to improve offset voltage performance. For best performance, verify C6 matches the value of C7 and that both capacitors are 10 to 20 times lower in value than C5. NP0-type capacitors offer low temperature drift and low voltage coefficients, and are preferred for common-mode filtering.

For most applications, the structure shown in Figure 7-2 achieves excellent performance.

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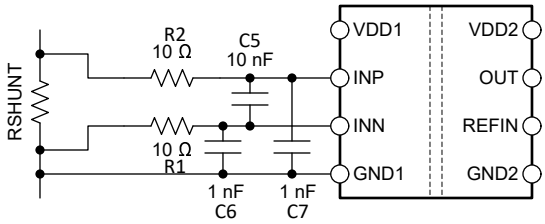

Figure 7-2. Input Filter

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7.2.2.3 Designing the Bootstrap Supply

The bootstrap capacitor (C2, Figure 7-1) is charged during the PWM on-time of the low-side FET of the left-hand-side half bridge. During the PWM off-time, C2 rises with the switch pin voltage and serves as the AMC0100R power supply. R4 serves as a current-limiting resistor during the charging phase, and D1 prevents reverse current from flowing back to the bootstrap supply during the discharge phase.

The voltage C2 charges up to during the PWM on-time depends on the values of the bootstrap supply and the current limiting resistor R2. Additionally, this voltage depends on the PWM duty cycle and the forward voltage of the diode D1 ($V_{F, D1}$).

The voltage C2 discharges to during the PWM off-time depends on the reverse recovery time of D1. Additionally, this voltage depends on the PWM duty cycle and the current draw of the AMC0100R (I_{VDD1}) . To minimize switching losses, select a fast switching diode with high forward current capability.

Make sure C2 is sized to support the maximum IDD1 current for the duration of the maximum PWM off-time. During this time, make sure C2 does not discharge below the minimum recommended VDD1 voltage of 3V. Lower capacitance values allow faster charging and therefore support lower PWM duty cycles. However, lower values also generate more voltage ripple and limit the maximum PWM off time. In this example, a ripple voltage (V_{RIPPLE}) of less than 200mV is targeted. The maximum PWM off-time is 95% × (1 / f_{PWM}) = 0.95 × 62.5µs, which is approximately 60µs. $IDD1_{MAX}$ is specified as 6.7mA. The minimum capacitance value is calculated as $C_{2, MIN}$ = $IDD1_{MAX}$ × $t_{PWM-OFF, MAX}$ / V_{RIPPLE} = 6.7mA × 60µs / 200mV = 2.0µF. A 4.7µF capacitor is selected to allow for component tolerances and adds margin to the design.

Make sure the bootstrap circuit supports recharging C2 within the minimum PWM on-time of 5% × (1 / f_{PWM}) = 0.05 × 62.5µs, or approximately 3.1µs. The average charging current during this time is C2 × V_{RIPPLE} / $t_{PWM-ON, MIN}$ = 4.7µF × 200mV / 3.1µs, which is approximately 300mA. This current is the minimum forward current that diode D1 has to support. The maximum allowable voltage drop across diode D1 and current limiting resistor R4 is determined by the minimum capacitor voltage and the V_{BS} value. The minimum capacitor voltage is 3V and equivalent to $VDD1_{MIN}$. V_{BS} is the bootstrap supply voltage and is equal to 6V. Assume a diode forward voltage of 1V is used. Make sure R4 is < (V_{BS} – $V_{F, D1}$ – $V_{C2, MIN}$) / I_{CHARGE} = (6V – 1V – 3V) / 300mA = 6Ω. A 2Ω resistor is selected to provide margin to the design.

7.2.2.4 Connecting the REFIN Pin

The reference input has a finite input impedance as shown in the *Section 6.2* . Consider this impedance when driving the REFIN pin from a high-impedance source. Connect a 100nF capacitor from REFIN to GND2 to filter out high-frequency noise at the reference input. Figure 7-3 shows different options for connecting the REFIN pin.

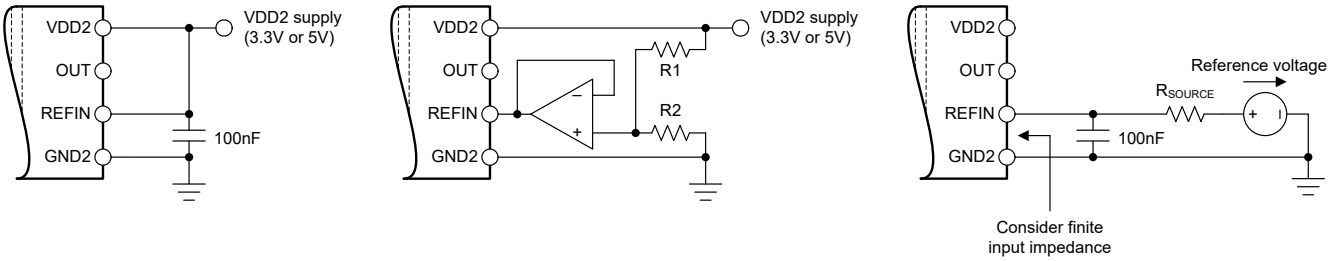

Figure 7-3. Connecting the REFIN Pin

In the first example, REFIN is shorted to VDD2. In the second example, V_{REFIN} is derived from VDD2 through a buffered resistive divider. In the third example, an external voltage source drives the reference input pin.

7.2.3 Application Curves

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. Figure 7-4 shows the typical full-scale step response of the AMC0100R.

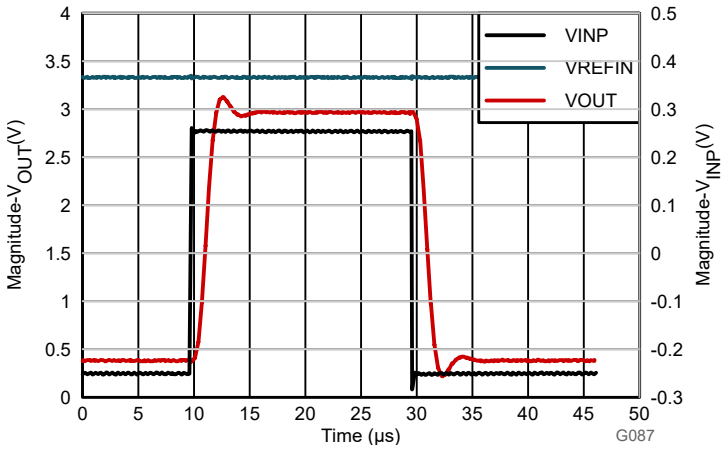

Figure 7-4. Output Step Response of the AMC0100R

Figure 7-5 shows the typical step response of the AMC0100R when a transient step is applied on its reference input pin with INP and INN connected to GND1.

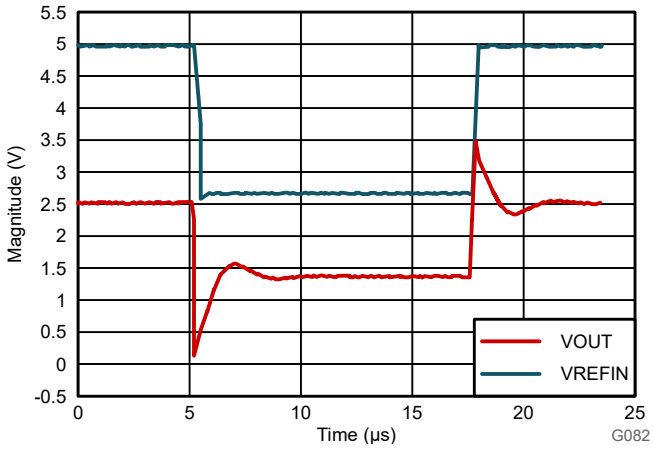

Figure 7-5. Reference Input Step Response of the AMC0100R

7.3 Best Design Practices

Place a minimum 10nF capacitor at the device input (from INP to INN). This capacitor helps avoid voltage droop at the input during the sampling period of the switched-capacitor input stage.

Do not short GND1 to INN directly at the device input. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. See the *Section 7.5.2* section for more details.

Do not leave the inputs of the AMC0100R unconnected (floating) when the device is powered up. If the device inputs are left floating, the device output is not valid.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the *Section 5.3* table.

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7.4 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0100R is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC0100R does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 7-6 shows a decoupling diagram for the AMC0100R.

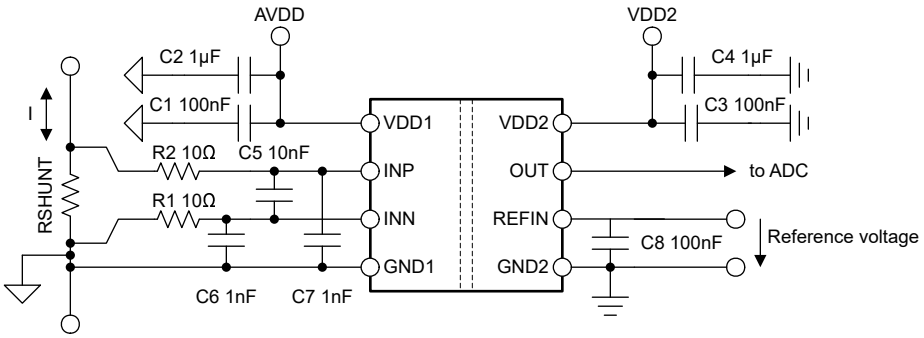


Figure 7-6. Decoupling of the AMC0100R

Verify capacitors provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

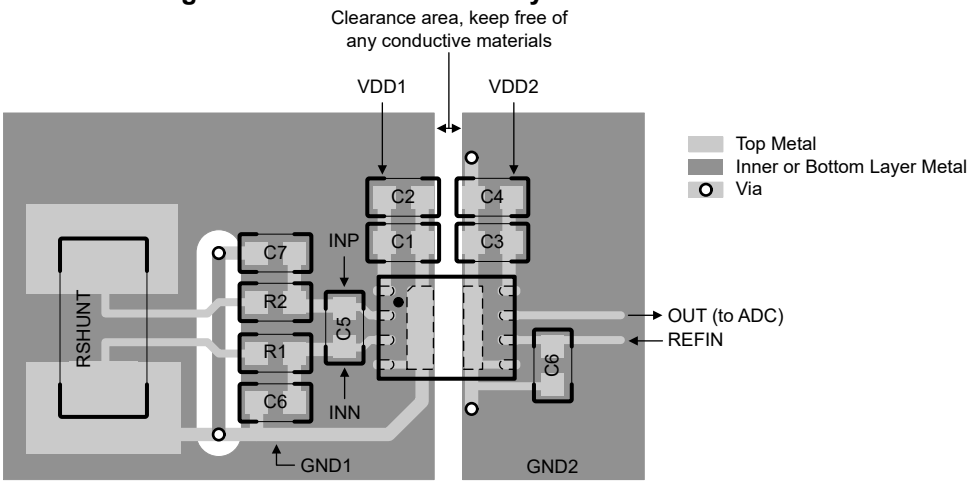
7.5 Layout

7.5.1 Layout Guidelines

The *Section 7.5.2* section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0100R supply pins). This example also depicts the placement of other components required by the device.

7.5.2 Layout Example

Figure 7-7. Recommended Layout of the AMC0100R



8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instrument, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC0100RDENR	Active	Production	VSON (DEN) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C0100R

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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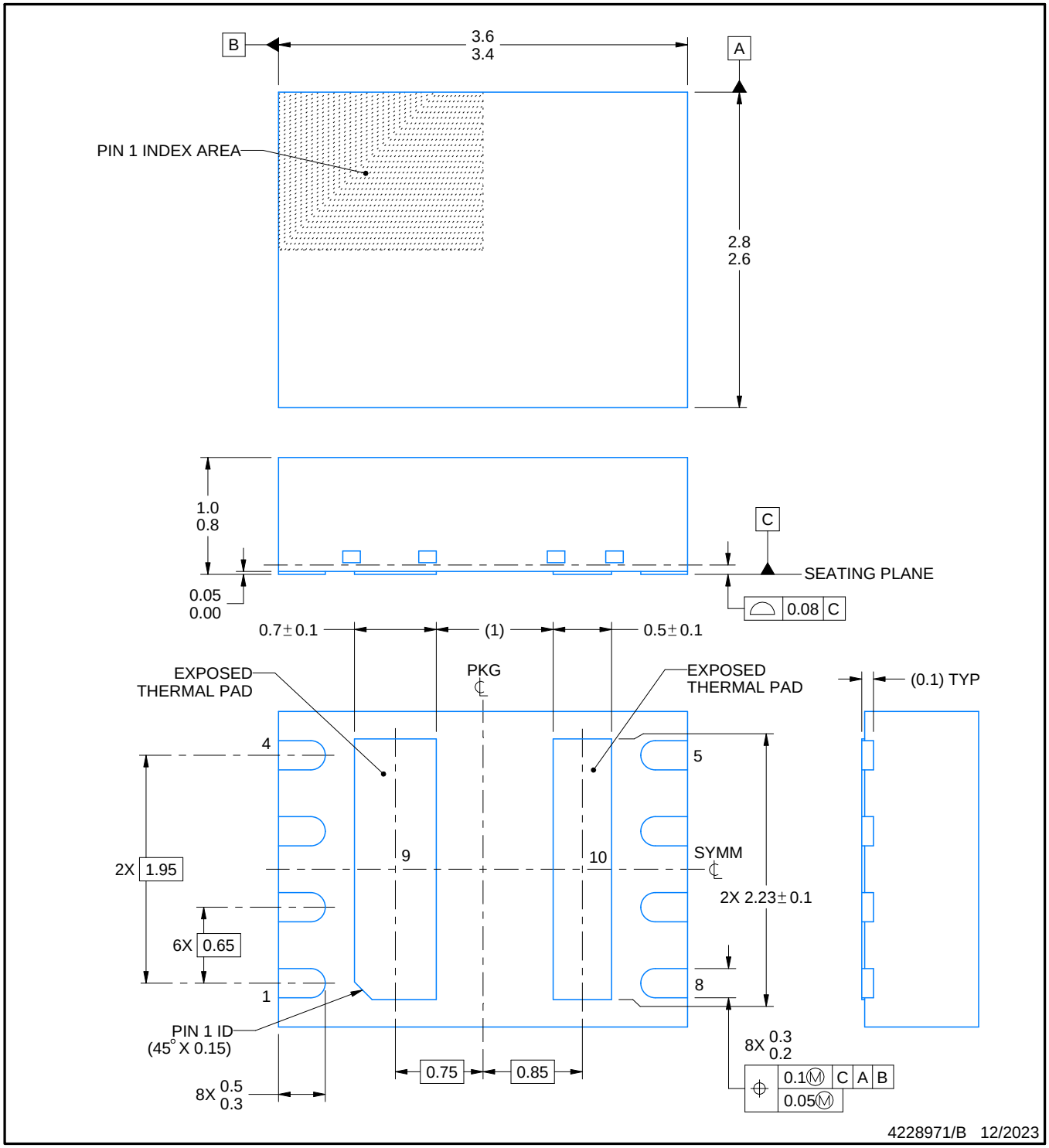
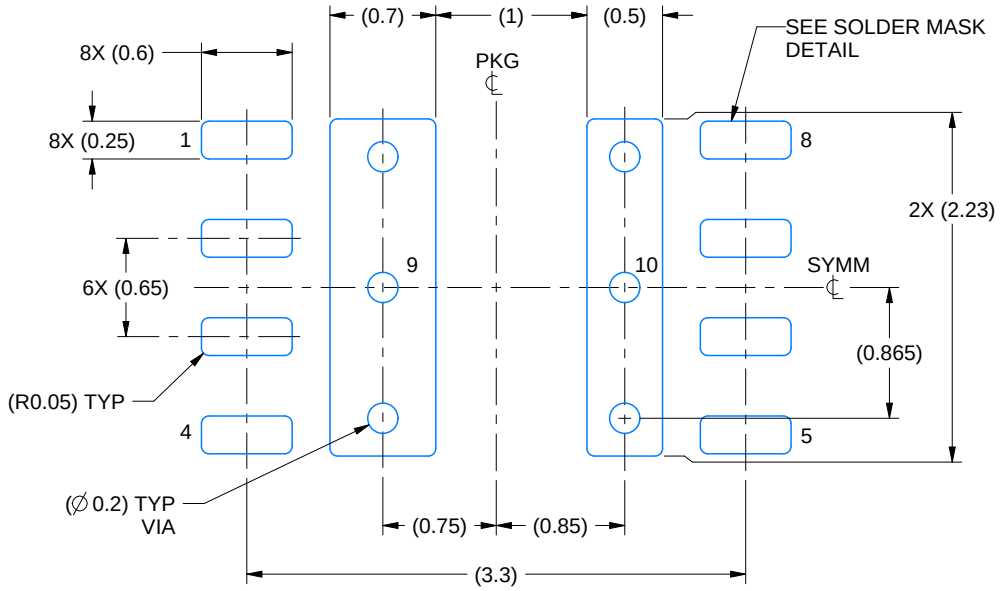
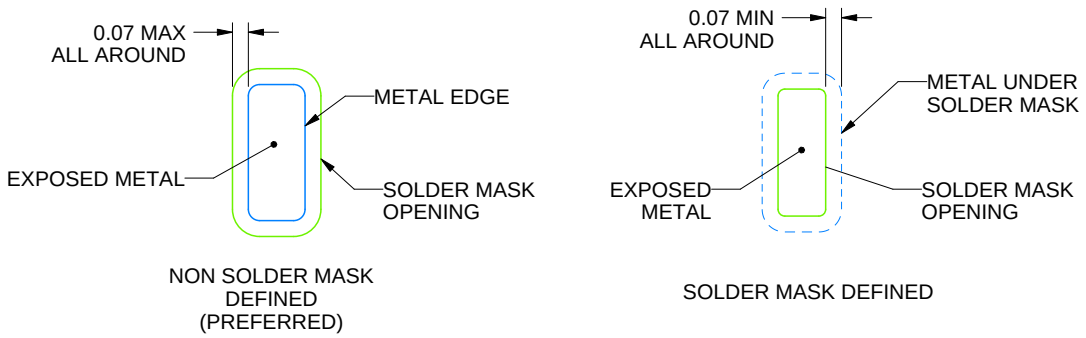


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

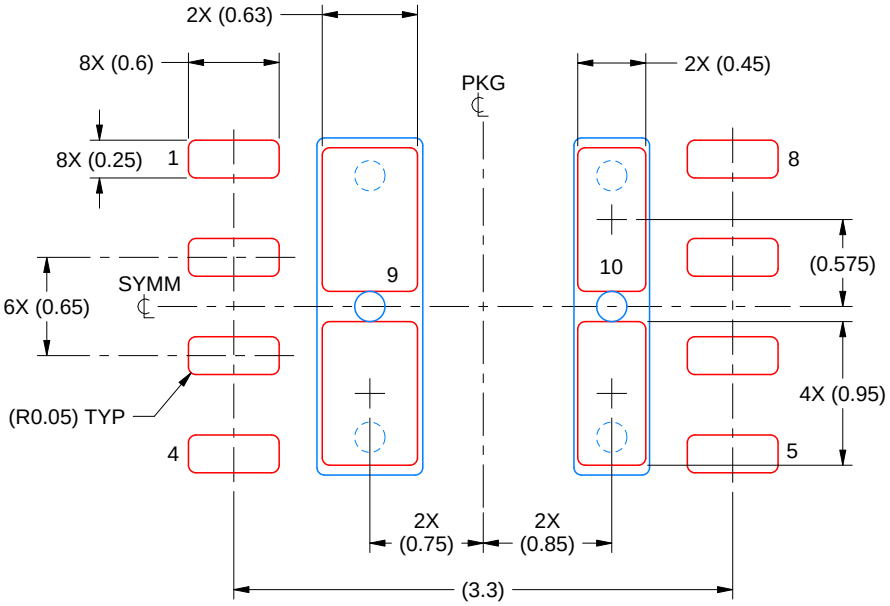


SOLDER MASK DETAILS

4228971/B 12/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 9 & 10: 77%

4228971/B 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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