

TPS537x2 Dual-Channel DDCAP+™, Step-Down, Multiphase Controller with Intel® VR14.Cloud, AMD® SVI3 2.0 and 3.12, AVSBus® 1.4, and PMBus® Interfaces

1 Features

- Input voltage range: 4.5V to 17V
- Output voltage range: 0.25V to 5.5V
- Dual output with 8 phase, 12 phase, and 16 phase package options, flexible phase order assignment and up to 4x native phase stacking
- Native trans-inductor voltage regulator (TLVR) topology support including open detect
- Intel® VR14.Cloud, VR14/VR13.HC/VR13 SVID, AMD® SVI3 2.0/3.12, AVSBus® 1.4, and PMBus® Interfaces
- Enhanced Dual-edge D-CAP+ (DDCAP+) control loop to provide best-in-class transient performance with excellent dynamic current sharing
- Telemetry options with peak detection, time above programmable thresholds, and NVM storage (VR14.Cloud telemetry level 2)
- Available PMBus Secure Device Security Level 2 support from supply-chain to end-of-life protection
- Field programmable firmware updates available in both prototyping and production
- Pin-selectable NVM configurations and PMBus address for reduced programming spins
- Individual phase current calibrations and reports
- Fast phase-adding for undershoot reduction
- Fully compatible with TI power stages and power modules for high-density power delivery
- Patented AutoBalance™ phase current balancing
- Accurate, adjustable voltage positioning
- Selectable per-phase current limit with peak & valley options.
- Selectable current limit on total average current.
- Analog IMON voltage output with programmable gain and offset options.
- Operating temperature from -40°C to 125°C

2 Applications

- [Rack server](#)
- [Microserver and tower server](#)
- [High performance computing](#)
- [Baseband unit \(BBU\)](#)
- [Data center switch](#)
- [Campus and branch switches](#)
- [Core routers and Edge routers](#)
- [Hardware accelerator cards](#)
- [High performance computing](#)

3 Description

The TPS537x2 family of step-down controllers are high-performance, dual output multiphase controllers available in 8-phase, 12-phase, and 16-phase package options. The controller has a high degree of programmability with support for up to eight separate pin-selectable configurations. Advanced control features such as Dual-edge D-CAP+™ (DDCAP+) architecture with native TLVR support and full PID loop provide fast transient response and good current sharing minimizes output capacitance requirements and saves system cost. Controllers are fully compatible with relevant TI smart power stages. The device also provides a novel phase interleaving strategy and optional phase shedding for efficiency improvements at different loads and long term reliability improvements. All programmable parameters can be reported and configured by the PMBus interface and can be stored in NVM as the new default values to minimize the external component count.

Packaging Information

PART NUMBER	PIN COUNT ⁽¹⁾	BODY SIZE (NOM)
TPS53782ZLAR (8ph)	40	5.00 × 5.00mm
TPS537C2ZLCR (12ph)	48	6.00 × 6.00mm
TPS537G2ZLFR (16ph)	56	7.00 × 7.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

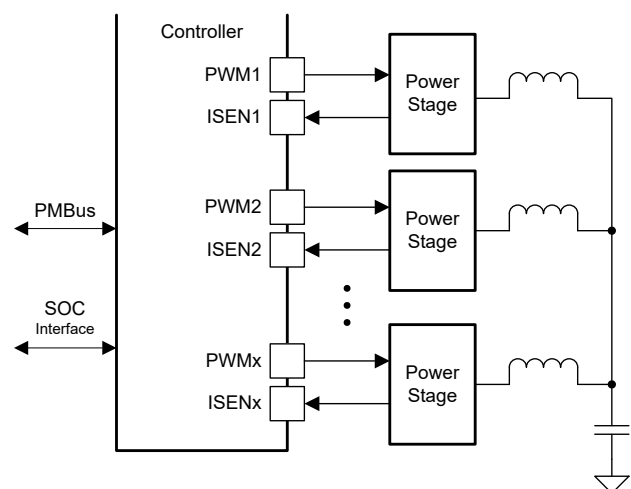


Figure 3-1. Simplified Example Application



4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.3 Trademarks

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4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

5.1 Packaging Information

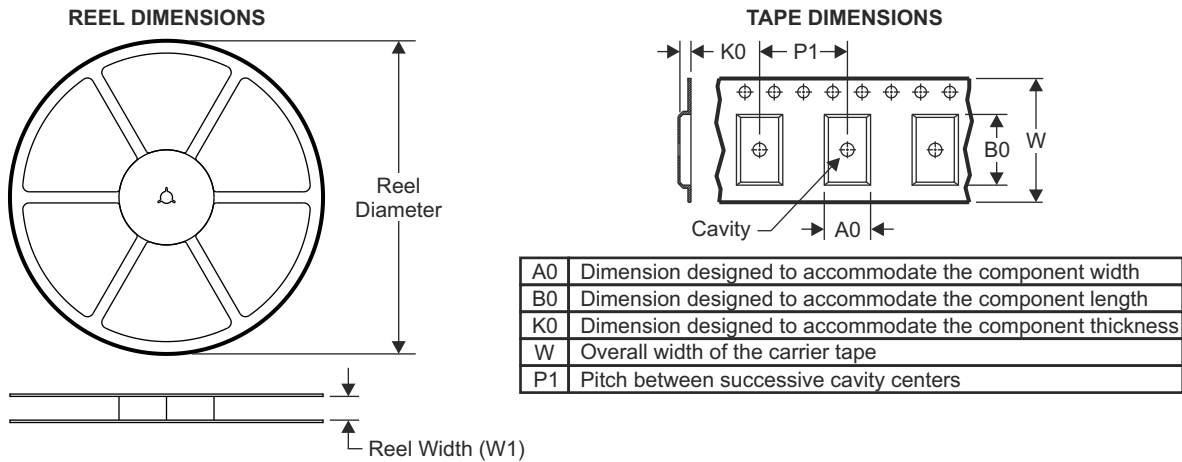
Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽³⁾	MSL Peak Temp ⁽⁴⁾	Op Temp (°C)	Device Marking ⁽⁵⁾ ⁽⁶⁾
TPS53782ZLAR	Preview	FCLGA	ZLA	40	3000	Green (RoHS & no Sb/Br)	ENEPIG	LEVEL3- 260C-168 HR	–40 to 125	TPS 53782
TPS537C2ZLCR	Preview	FCLGA	ZLC	48	3000	Green (RoHS & no Sb/Br)	ENEPIG	LEVEL3- 260C-168 HR	–40 to 125	TPS 537C2
TPS537G2ZLFR	Preview	FCLGA	ZLF	56	3000	Green (RoHS & no Sb/Br)	ENEPIG	LEVEL3- 260C-168 HR	–40 to 125	TPS 537G2

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

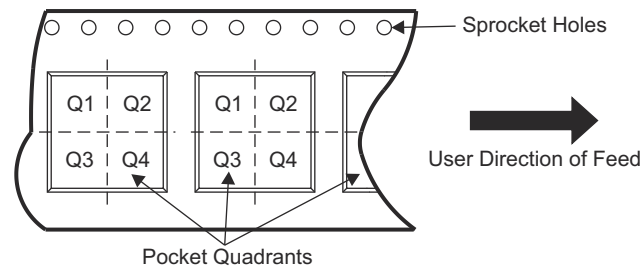
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5.2 Tape and Reel Information

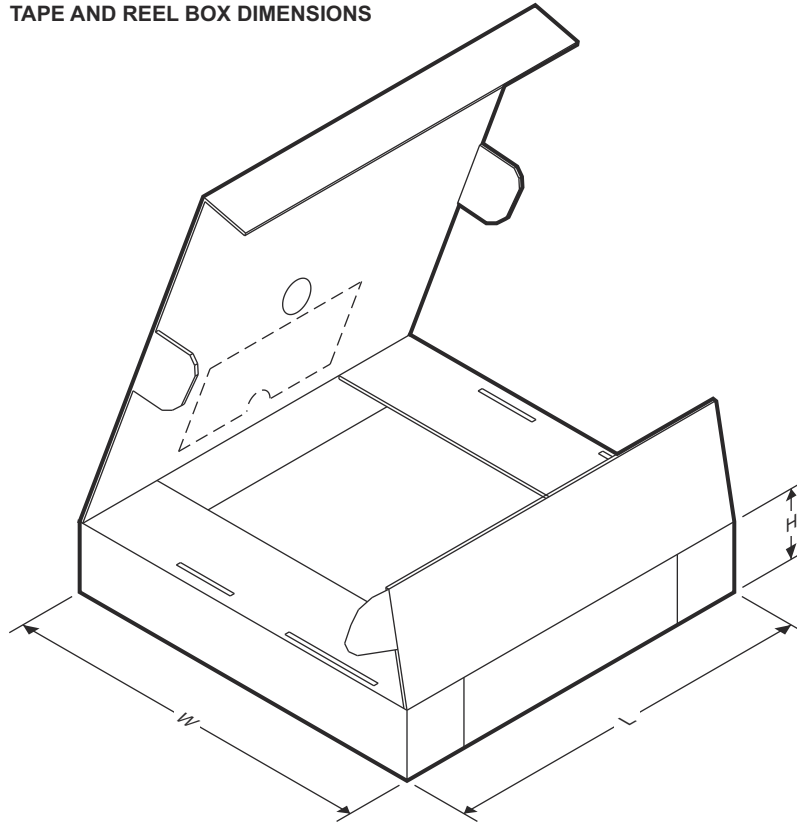


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53782ZLAR	FCLGA	ZLA	40	3000	330	12.4	5.3	5.3	1.5	8	12	Q1
TPS537C2ZLCR	FCLGA	ZLC	48	3000	330	16.4	6.25	6.25	1.05	12	16	Q1
TPS537G2ZLFR	FCLGA	ZLF	56	3000	330	16.4	7.3	7.3	1.1	12	16	Q1

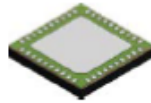
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53782ZLAR	FCLGA	ZLA	40	3000	336.6	336.6	31.8
TPS537C2ZLCR	FCLGA	ZLC	48	3000	336.6	336.6	31.8
TPS537G2ZLFR	FCLGA	ZLF	56	3000	336.6	336.6	31.8

PRODUCT PREVIEW

5.3 Mechanical Data

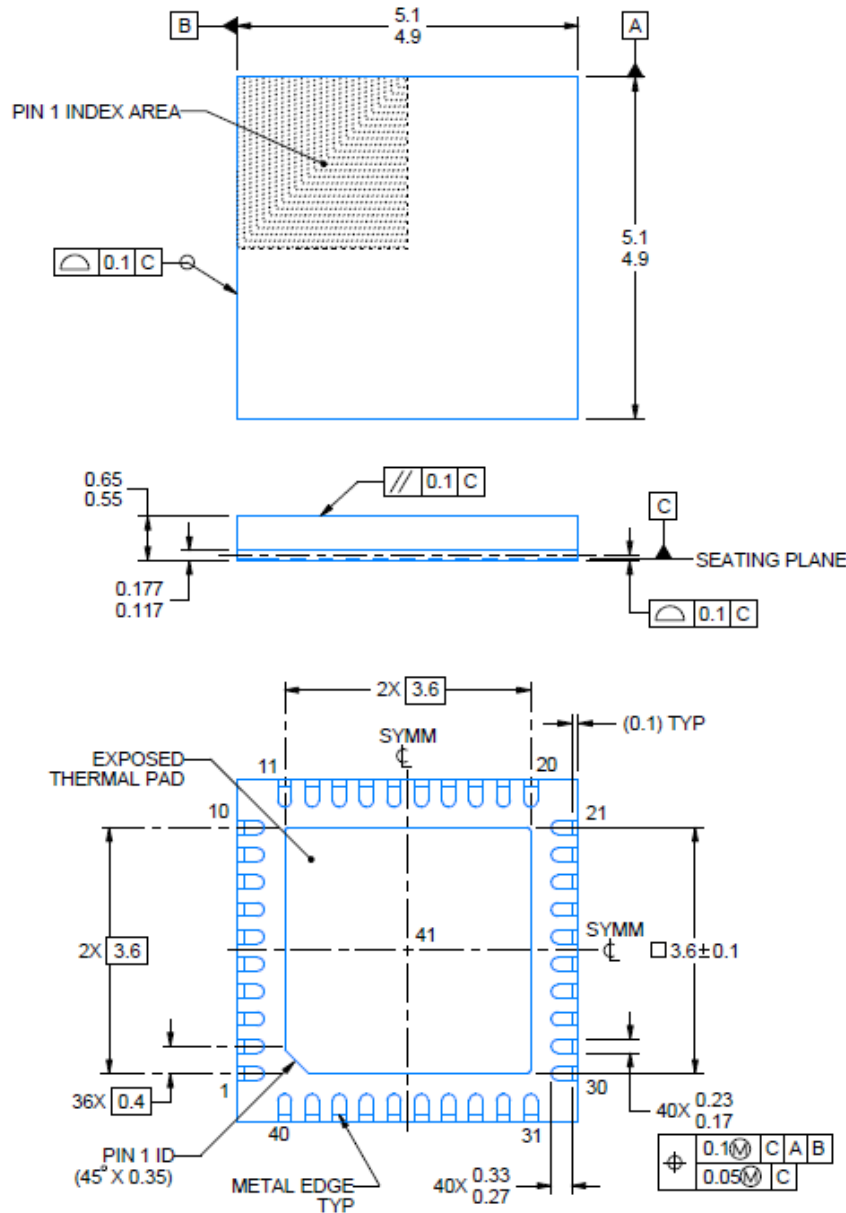


PACKAGE OUTLINE

ZLA0040A

FCLGA - 0.65 mm max height

LAND GRID ARRAY



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NOTES:

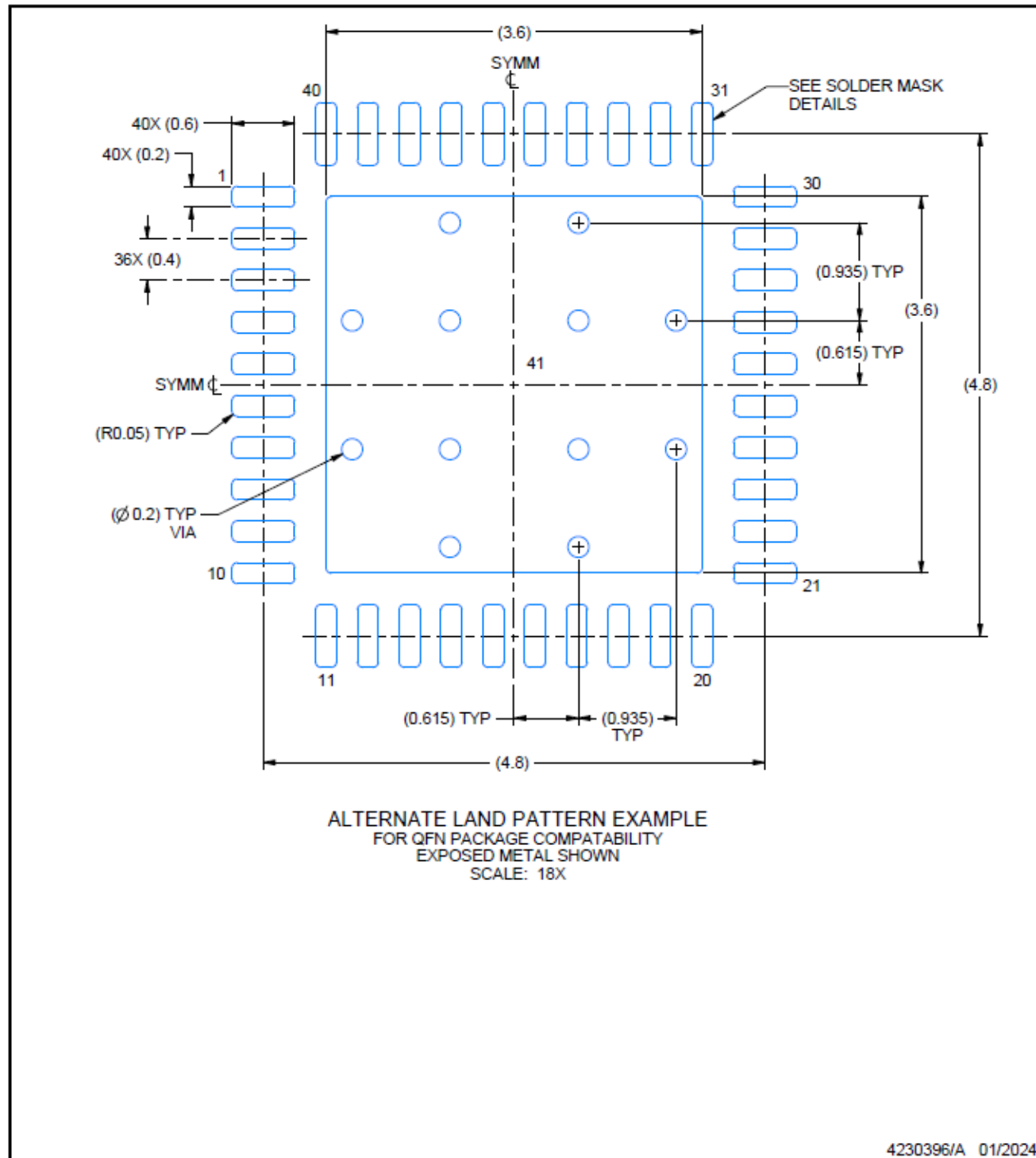
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

ZLA0040A

FCLGA - 0.65 mm max height

LAND GRID ARRAY



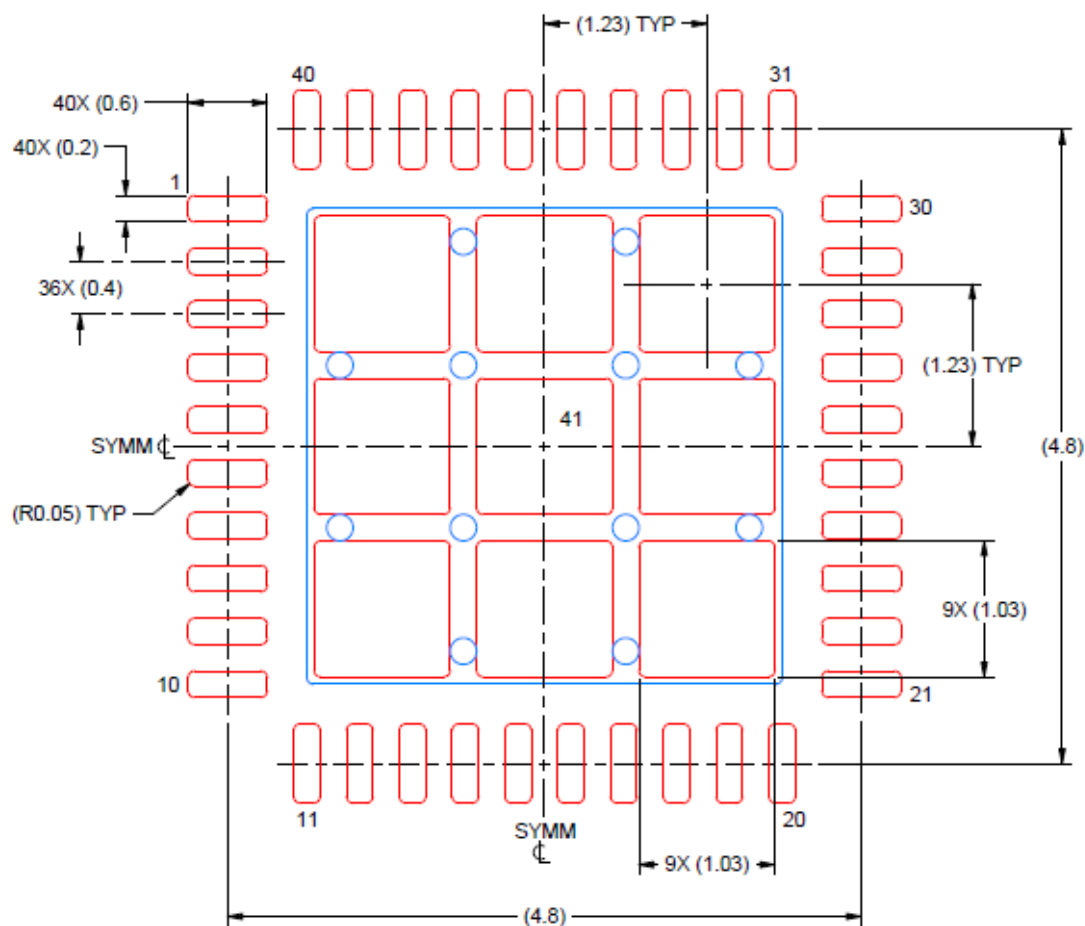
PRODUCT PREVIEW

EXAMPLE STENCIL DESIGN

ZLA0040A

FCLGA - 0.65 mm max height

LAND GRID ARRAY

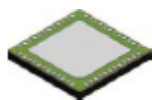


ALTERNATE SOLDER PASTE EXAMPLE
FOR QFN PACKAGE COMPATABILITY
BASED ON 0.125 MM THICK STENCIL
SCALE: 18X

EXPOSED PAD 57
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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PRODUCT PREVIEW

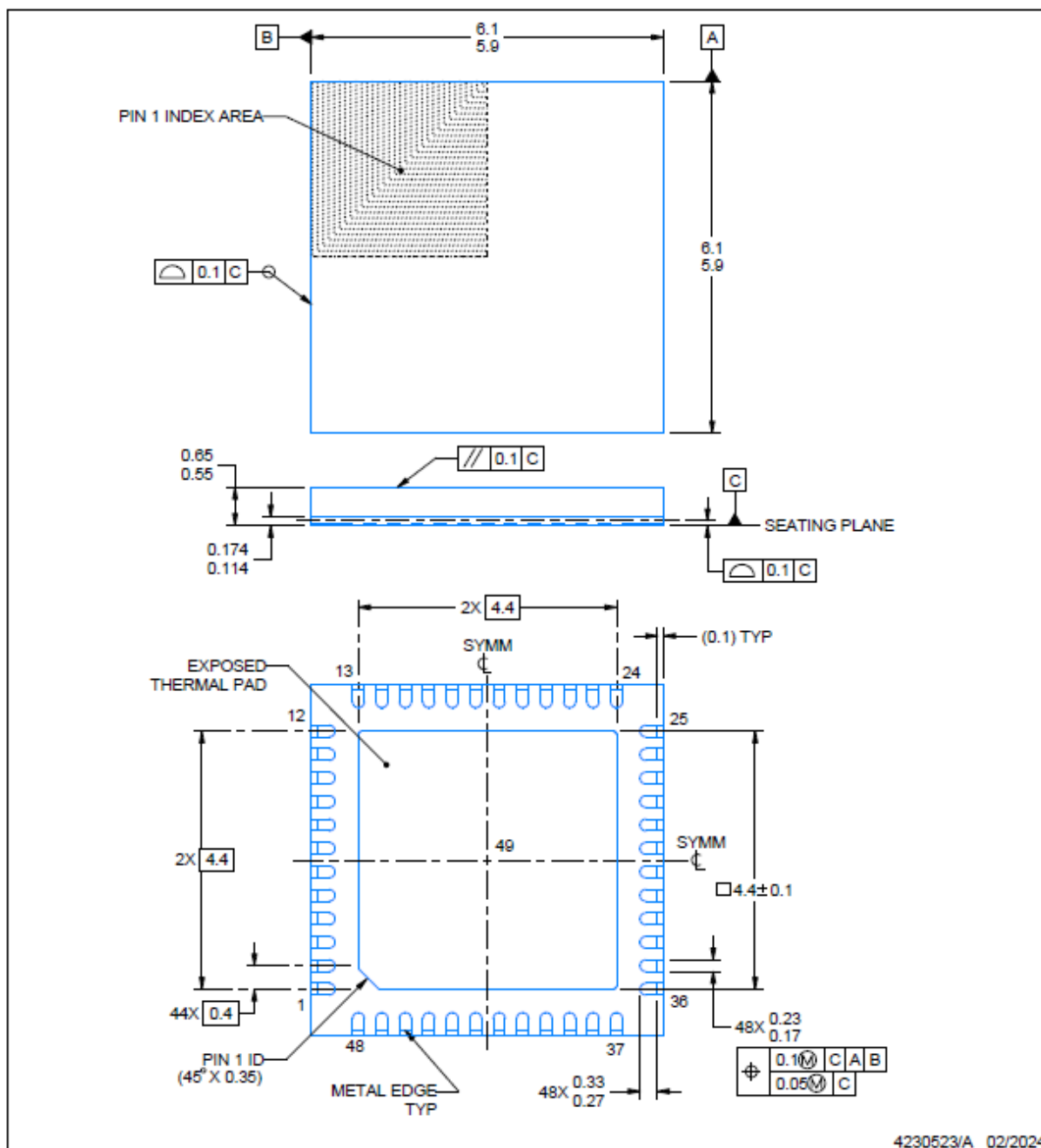


ZLC0048A

PACKAGE OUTLINE

FCLGA - 0.65 mm max height

LAND GRID ARRAY



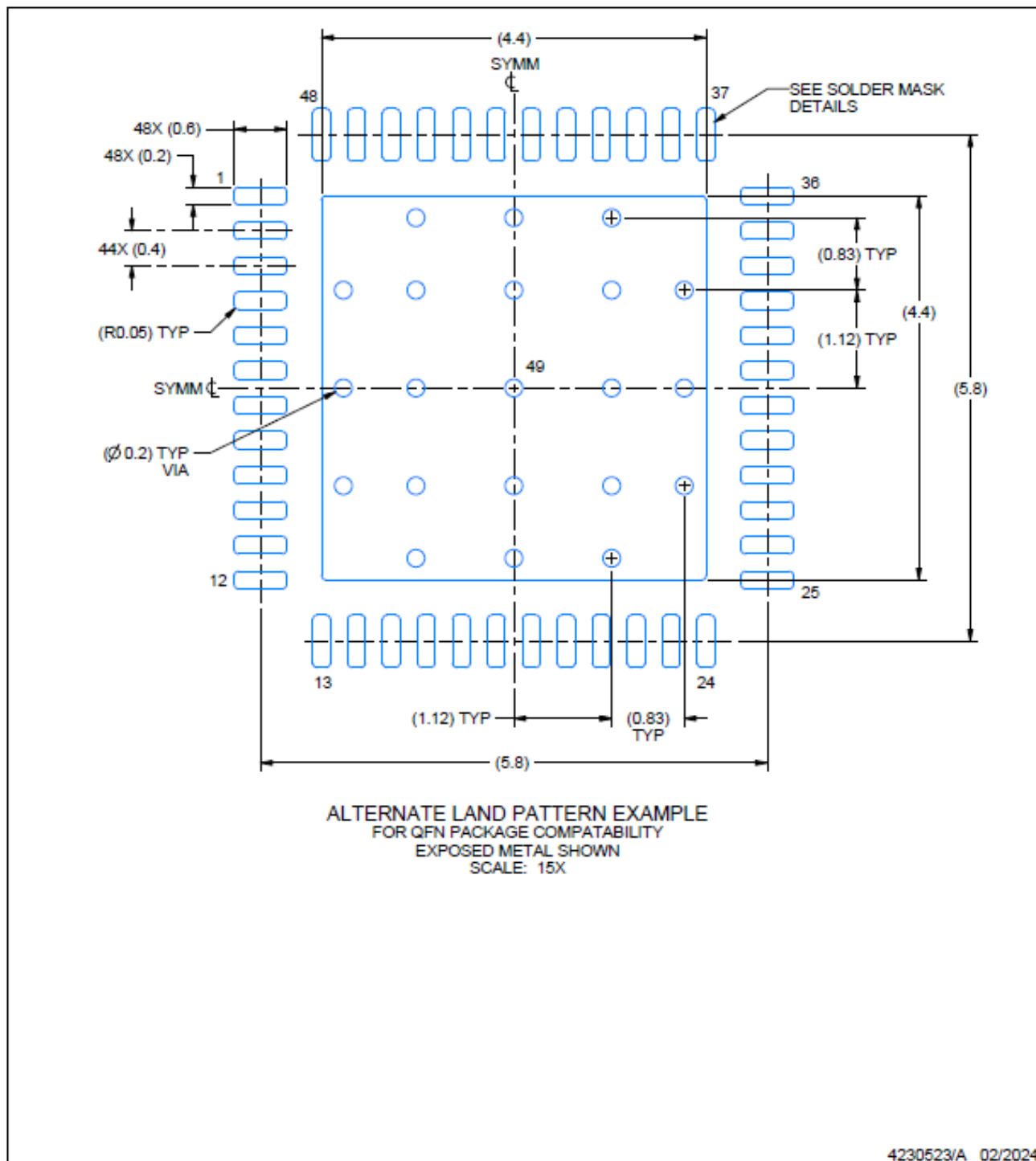
PRODUCT PREVIEW

EXAMPLE BOARD LAYOUT

ZLC0048A

FCLGA - 0.65 mm max height

LAND GRID ARRAY

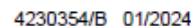


PRODUCT PREVIEW

4230523/A 02/2024

FCLGA - 0.65 mm max height

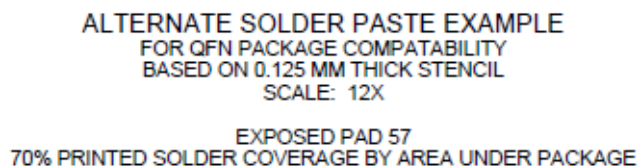
PRODUCT PREVIEW



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

FCLGA - 0.65 mm max height

PRODUCT PREVIEW



Product Folder Links: [TPS53782](#) [TPS537C2](#) [TPS537G2](#)

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