SN74AC126-Q1 Automotive Quadruple Non-Inverting Buffers with 3-State Outputs

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in wettable flank QFN package
- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Maximum t_{pd} of 10.1ns at 5V, 50pF load

2 Applications

- Drive an indicator LED
- Redrive a digital signal
- Drive a transmission line
- Hold a signal during controller reset

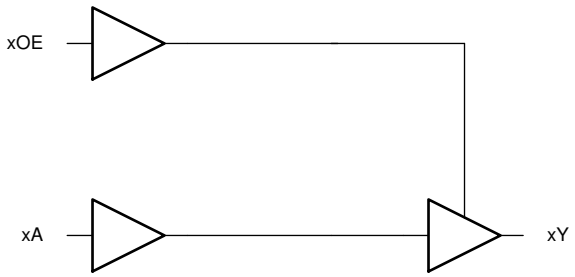
3 Description

The SN74AC126-Q1 contains four independent buffers with 3-state outputs.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AC126-Q1	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	BQA (WQFN, 14)	3mm x 2.5mm	3mm x 2.5mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

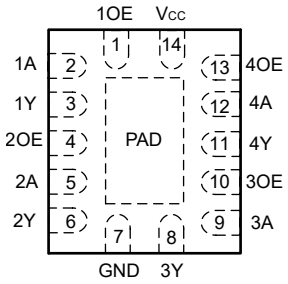


Figure 4-1. SN74AC126-Q1 BQA Package (Top View)

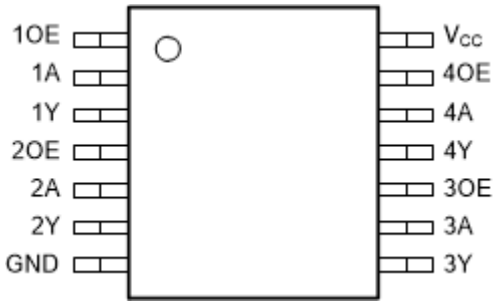


Figure 4-2. SN74AC126-Q1 , PW Package (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$1\overline{OE}$	1	I	Channel 1, output enable
1A	2	I	Channel 1, input A
1Y	3	O	Channel 1, output Y
$2\overline{OE}$	4	I	Channel 2, output enable
2A	5	I	Channel 2, input B
2Y	6	O	Channel 2, output Y
GND	7	G	Ground
3Y	8	O	Channel 3, output Y
3A	9	I	Channel 3, input A
$3\overline{OE}$	10	I	Channel 3, output enable
4Y	11	O	Channel 4, output Y
4A	12	I	Channel 4, input A
$4\overline{OE}$	13	I	Channel 4, output enable
V_{CC}	14	P	Positive supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.
(2) WBQA package only.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range(2)		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous output current through V_{CC} or GND			±200	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.5	6	V
V_{IH}	High-level input voltage	V_{CC} = 1.5V	1.2		V
		V_{CC} = 1.8V	1.26		
		V_{CC} = 2.5V	1.75		
		V_{CC} = 3V	2.1		
		V_{CC} = 4.5V	3.15		
		V_{CC} = 6V	4.2		
V_{IL}	Low-Level input voltage	V_{CC} = 1.5V		0.3	V
		V_{CC} = 1.8V		0.54	
		V_{CC} = 2.5V		0.75	
		V_{CC} = 3V		0.9	
		V_{CC} = 4.5V		1.35	
		V_{CC} = 6V		1.8	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8V		–1	mA
		V_{CC} = 2.5V		–2	
		V_{CC} = 3V		–12	
		V_{CC} = 4.5V to 6V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.8V		1	mA
		V_{CC} = 2.5V		2	
		V_{CC} = 3V		12	
		V_{CC} = 4.5V to 6V		24	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.5V to 3V		50	ns/V
		V_{CC} = 3.6V to 6V		20	
T_A	Operating free-air temperature		–40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	14	149.8	81.6	106.0	23.5	104.7	N/A	°C/W
BQA (WQFN)	14	95.2	106.6	64.8	19.8	64.6	40.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = -50µA	1.5V	1.4	1.49		V
		1.8V	1.7	1.79		
		2.5V	2.4	2.49		
		3V	2.9	2.99		
		4.5V	4.4	4.49		
		6V	5.4	5.99		
	I_{OH} = -1mA	1.8V	1.44			
	I_{OH} = -2mA	2.5V	2			
	I_{OH} = -12mA	3V	2.4			
	I_{OH} = -24mA	4.5V	3.7			
	I_{OH} = -24mA	6V	4.7			
	I_{OH} = -75mA	6V	3.85			
V_{OL}	I_{OL} = 50µA	1.5V		0.01	0.1	V
		1.8V		0.01	0.1	
		2.5V		0.01	0.1	
		3V		0.01	0.1	
		4.5V		0.01	0.1	
		6V		0.01	0.1	
	I_{OL} = 1mA	1.8V			0.36	
	I_{OL} = 2mA	2.5V			0.5	
	I_{OL} = 12mA	3V			0.5	
	I_{OL} = 24mA	4.5V			0.5	
	I_{OL} = 24mA	6V			0.5	
	I_{OL} = 75mA	6V			1.65	
I_I	V_I = 6V or GND	0V to 6V			±1	µA
I_{OZ}	V_O = V_{CC} or GND	6V			±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	6V			20	µA
C_I	V_I = V_{CC} or GND	5V		2		pF
C_O	Output disabled, V_O = V_{CC} or GND	5V		4		pF

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5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
C_L = 15 pF							
t_{PLH}	A	Y	1.5V		13.4	20.8	ns
t_{PHL}			1.5V		12.7	19.5	
t_{PLZ}	OE	Y	1.5V		9.4	13.5	ns
t_{PHZ}			1.5V		15.2	21.6	
t_{PZL}	OE	Y	1.5V		12.5	19.7	ns
t_{PZH}			1.5V		14.9	23.1	
t_r		Y	1.5V		3.7	5.8	ns
t_f			1.5V		4.1	6.5	
$t_{sk(o)}$		Y	1.5V		0.5	1.1	ns
t_{PLH}	A	Y	1.8V		9.5	14.5	ns
t_{PHL}			1.8V		9.3	14	
t_{PLZ}	OE	Y	1.8V		6.9	9.8	ns
t_{PHZ}			1.8V		11.6	15.8	
t_{PZL}	OE	Y	1.8V		9.1	13.9	ns
t_{PZH}			1.8V		10.7	16.2	
t_r		Y	1.8V		2.9	4.4	ns
t_f			1.8V		3.1	4.7	
$t_{sk(o)}$		Y	1.8V		0.3	0.7	ns
t_{PLH}	A	Y	2.5V		6.1	9	ns
t_{PHL}			2.5V		5.9	8.6	
t_{PLZ}	OE	Y	2.5V		3.9	5.5	ns
t_{PHZ}			2.5V		6.3	8.9	
t_{PZL}	OE	Y	2.5V		6	9	ns
t_{PZH}			2.5V		6.9	10.2	
t_r		Y	2.5V		2.2	3.5	ns
t_f			2.5V		2.1	3.2	
$t_{sk(o)}$		Y	2.5V		0.2	0.4	ns
t_{PLH}	A	Y	3.3V		5.1	7.4	ns
t_{PHL}			3.3V		5	7.1	
t_{PLZ}	OE	Y	3.3V		3.3	4.5	ns
t_{PHZ}			3.3V		5.2	7.2	
t_{PZL}	OE	Y	3.3V		5	7.3	ns
t_{PZH}			3.3V		5.7	8.3	
t_r		Y	3.3V		1.8	2.9	ns
t_f			3.3V		1.8	2.7	
$t_{sk(o)}$		Y	3.3V		0.1	0.4	ns
t_{PLH}	A	Y	5V		3.7	5.2	ns
t_{PHL}			5V		3.8	5.1	
t_{PLZ}	OE	Y	5V		2.4	3.1	ns
t_{PHZ}			5V		3.9	5.1	
t_{PZL}	OE	Y	5V		3.7	5.1	ns
t_{PZH}			5V		4.2	5.8	

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over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t_r		Y	5V		1.4	2.2	ns
t_f			5V		1.4	2	
$t_{sk(o)}$		Y	5V		0.1	0.3	ns
t_{PLH}	A	Y	6V		3.2	4.3	ns
t_{PHL}			6V		3.3	4.3	
t_{PLZ}	OE	Y	6V		2.1	2.6	ns
t_{PHZ}			6V		3.3	4.3	
t_{PZL}	OE	Y	6V		3.1	4.3	ns
t_{PZH}			6V		3.5	4.8	
t_r		Y	6V		1.1	1.7	ns
t_f			6V		1.1	1.6	
$t_{sk(o)}$		Y	6V		0.1	0.3	ns
C_L = 50 pF							
t_{PLH}	A	Y	1.5V		15.6	24.1	ns
t_{PHL}			1.5V		14.9	22.9	
t_{PLZ}	OE	Y	1.5V		13.3	17.7	ns
t_{PHZ}			1.5V		23.1	29.7	
t_{PZL}	OE	Y	1.5V		15.1	23.7	ns
t_{PZH}			1.5V		17.3	26.5	
t_r		Y	1.5V		7.5	12	ns
t_f			1.5V		7.2	11.9	
$t_{sk(o)}$		Y	1.5V		0.5	1.1	ns
t_{PLH}	A	Y	1.8V		11.4	17.1	ns
t_{PHL}			1.8V		11.1	16.6	
t_{PLZ}	OE	Y	1.8V		10.1	13.1	ns
t_{PHZ}			1.8V		17.8	22.4	
t_{PZL}	OE	Y	1.8V		11	16.8	ns
t_{PZH}			1.8V		12.6	18.8	
t_r		Y	1.8V		5.7	8.9	ns
t_f			1.8V		5.5	8.6	
$t_{sk(o)}$		Y	1.8V		0.3	0.7	ns
t_{PLH}	A	Y	2.5V		7.5	11	ns
t_{PHL}			2.5V		7.2	10.4	
t_{PLZ}	OE	Y	2.5V		5	6.8	ns
t_{PHZ}			2.5V		8.5	11.2	
t_{PZL}	OE	Y	2.5V		7.6	11.1	ns
t_{PZH}			2.5V		8.4	12.2	
t_r		Y	2.5V		4.3	6.8	ns
t_f			2.5V		3.8	5.8	
$t_{sk(o)}$		Y	2.5V		0.2	0.4	ns
t_{PLH}	A	Y	3.3V		6.3	9	ns
t_{PHL}			3.3V		6.1	8.7	
t_{PLZ}	OE	Y	3.3V		4	5.4	ns
t_{PHZ}			3.3V		7	9	

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over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t_{PZL}	OE	Y	3.3V		6.4	9.2	ns
t_{PZH}			3.3V		7	10	
t_r		Y	3.3V		3.6	5.7	ns
t_f			3.3V		3.2	4.9	
$t_{sk(o)}$		Y	3.3V		0.2	0.3	ns
t_{PLH}	A	Y	5V		4.7	6.5	ns
t_{PHL}			5V		4.7	6.2	
t_{PLZ}	OE	Y	5V		3.2	3.6	ns
t_{PHZ}			5V		5.6	6.1	
t_{PZL}	OE	Y	5V		5.7	6.5	ns
t_{PZH}			5V		6.4	7.3	
t_r		Y	5V		2.7	4.1	ns
t_f			5V		2.5	3.6	
$t_{sk(o)}$		Y	5V		0.1	0.3	ns
t_{PLH}	A	Y	6V		4	5.5	ns
t_{PHL}			6V		4	5.2	
t_{PLZ}	OE	Y	6V		2.4	3	ns
t_{PHZ}			6V		3.8	4.8	
t_{PZL}	OE	Y	6V		4.1	5.5	ns
t_{PZH}			6V		4.5	6.2	
t_r		Y	6V		2.3	3.5	ns
t_f			6V		2.2	3	
$t_{sk(o)}$		Y	6V		0.1	0.3	ns
C_L = 150 pF							
t_{PLH}	A	Y	1.5V		20.8	32	ns
t_{PHL}			1.5V		19.4	30.1	
t_{PLZ}	OE	Y	1.5V		25	30	ns
t_{PHZ}			1.5V		45.7	52.6	
t_{PZL}	OE	Y	1.5V		20.5	32.8	ns
t_{PZH}			1.5V		22.6	34.4	
t_r		Y	1.5V		18	29.6	ns
t_f			1.5V		15	25.8	
$t_{sk(o)}$		Y	1.5V		0.5	1.1	ns
t_{PLH}	A	Y	1.8V		15.1	22.8	ns
t_{PHL}			1.8V		14.5	21.8	
t_{PLZ}	OE	Y	1.8V		19.7	22.8	ns
t_{PHZ}			1.8V		35.9	40.8	
t_{PZL}	OE	Y	1.8V		15.1	23.1	ns
t_{PZH}			1.8V		16.6	24.6	
t_r		Y	1.8V		13.3	21.7	ns
t_f			1.8V		11.1	18.5	
$t_{sk(o)}$		Y	1.8V		0.3	0.6	ns
t_{PLH}	A	Y	2.5V		10.2	15	ns
t_{PHL}			2.5V		9.5	13.7	

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over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t_{PLZ}	OE	Y	2.5V		8.3	10.1	ns
t_{PHZ}			2.5V		14.8	17.6	
t_{PZL}	OE	Y	2.5V		10.4	15.1	ns
t_{PZH}			2.5V		11.4	16.2	
t_r		Y	2.5V		9.9	16.6	ns
t_f			2.5V		7.6	12	
$t_{sk(o)}$		Y	2.5V		0.2	0.4	ns
t_{PLH}	A	Y	3.3V		8.7	12.5	ns
t_{PHL}			3.3V		8.2	11.5	
t_{PLZ}	OE	Y	3.3V		7	8.3	ns
t_{PHZ}			3.3V		12.1	14.2	
t_{PZL}	OE	Y	3.3V		8.9	12.6	ns
t_{PZH}			3.3V		9.7	13.6	
t_r		Y	3.3V		8.4	13.7	ns
t_f			3.3V		6.5	9.9	
$t_{sk(o)}$		Y	3.3V		0.2	0.3	ns
t_{PLH}	A	Y	5V		6.6	9.2	ns
t_{PHL}			5V		6.4	8.4	
t_{PLZ}	OE	Y	5V		4.7	5.4	ns
t_{PHZ}			5V		7.8	9	
t_{PZL}	OE	Y	5V		6.8	9.2	ns
t_{PZH}			5V		7.5	10.2	
t_r		Y	5V		6.2	9.8	ns
t_f			5V		5	7.2	
$t_{sk(o)}$		Y	5V		0.1	0.4	ns
t_{PLH}	A	Y	6V		5.7	7.9	ns
t_{PHL}			6V		5.4	7.1	
t_{PLZ}	OE	Y	6V		3.8	4.4	ns
t_{PHZ}			6V		5.7	6.8	
t_{PZL}	OE	Y	6V		5.8	7.7	ns
t_{PZH}			6V		6.5	8.7	
t_r		Y	6V		5.1	7.9	ns
t_f			6V		4.4	6.1	
$t_{sk(o)}$		Y	6V		0.1	0.3	ns
C_{PD} (1)	Any		5V		17		pF

(1) Power dissipation capacitance is calculated using the method described in CMOS Power Consumption and Cpd Calculation.

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5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

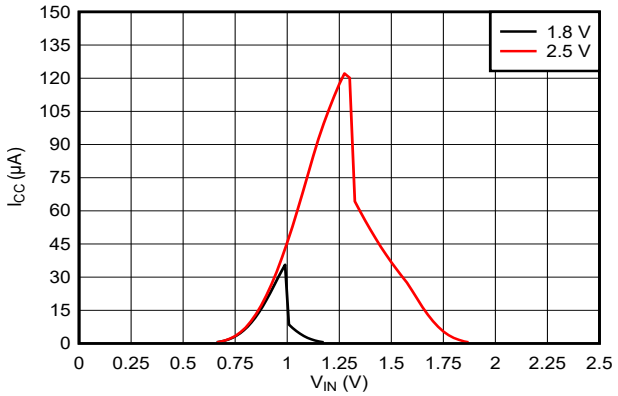


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

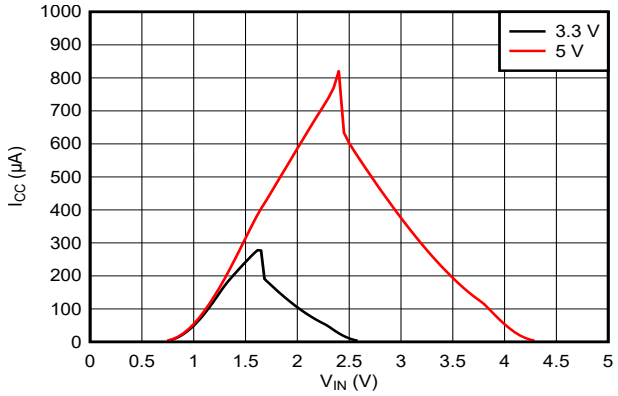


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

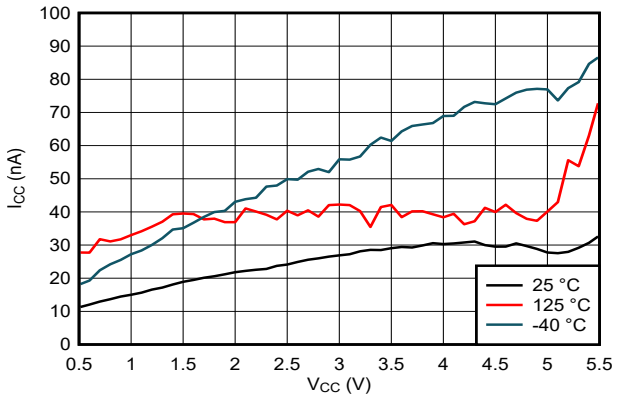


Figure 5-3. Supply Current Across Supply Voltage

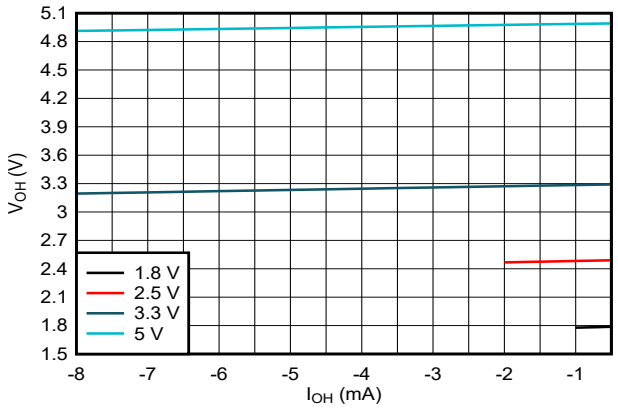


Figure 5-4. Output Voltage vs Current in HIGH State

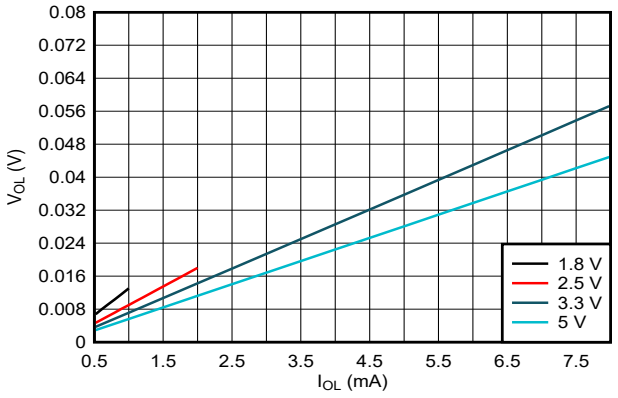


Figure 5-5. Output Voltage vs Current in LOW State

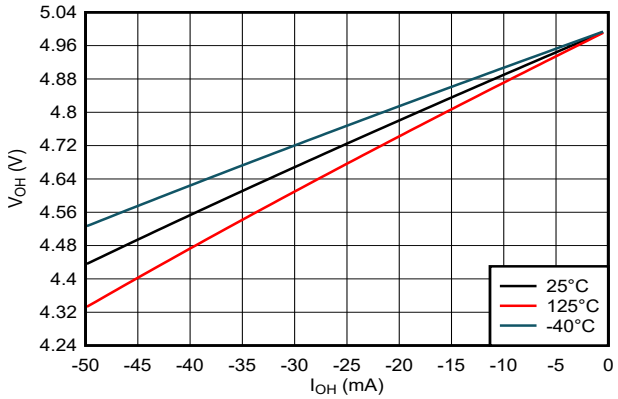


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

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5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

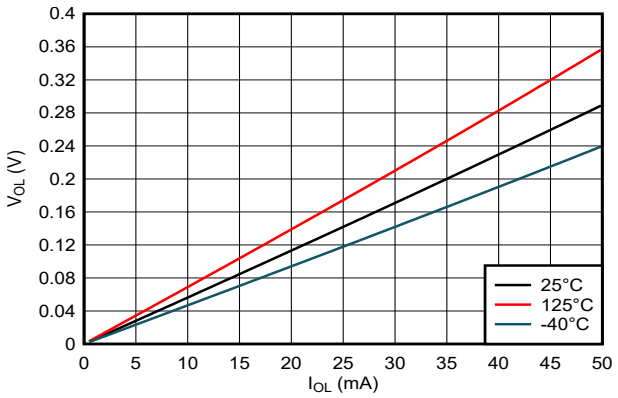


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

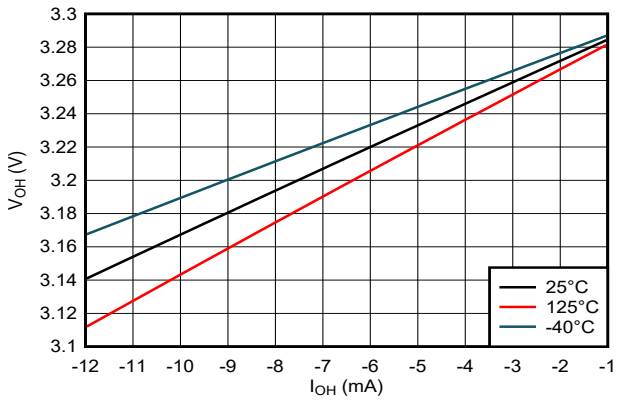


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

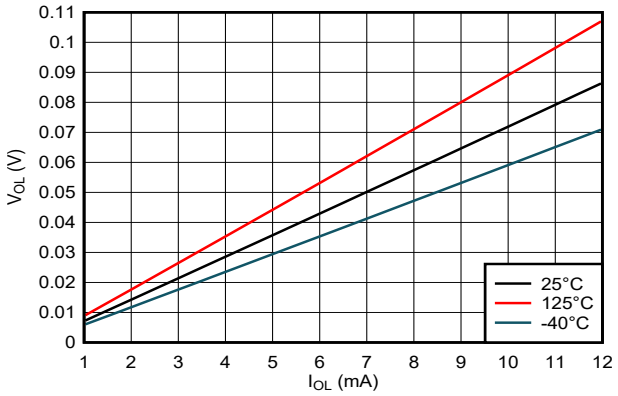


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

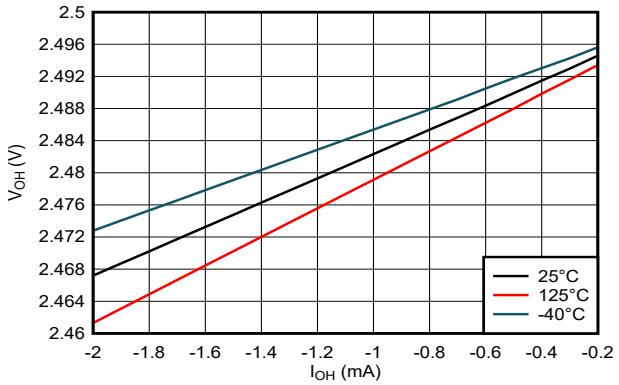


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

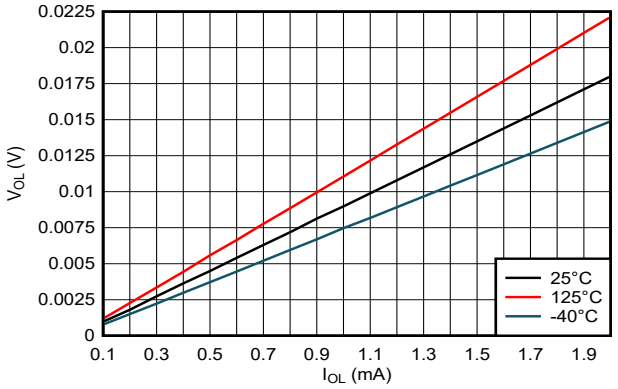


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

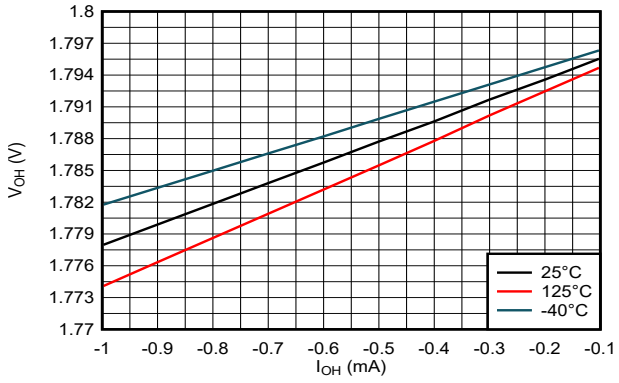


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

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5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

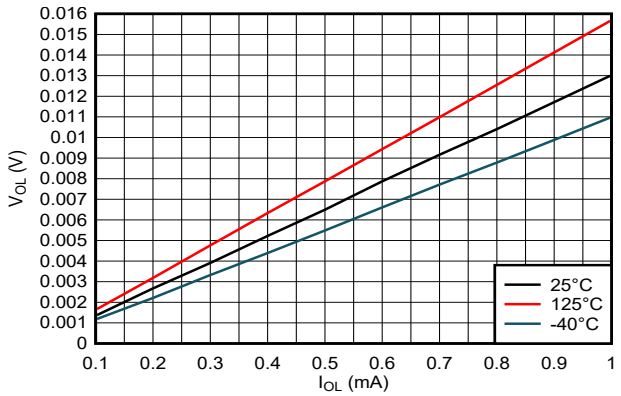


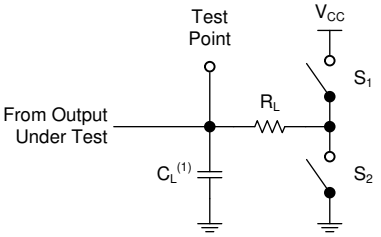
Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

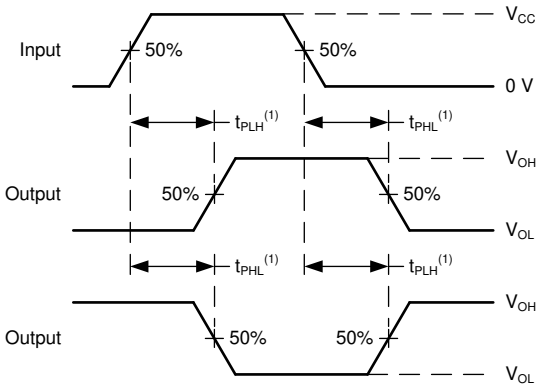
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH}, t_{PHL}	OPEN	OPEN	—	50pF	—	ALL
t_{PLZ}, t_{PZL}	CLOSED	OPEN	500Ω	50pF	0.15V	≤ 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	500Ω	50pF	0.15V	≤ 2.5V
t_{PLZ}, t_{PZL}	CLOSED	OPEN	500Ω	50pF	0.3V	> 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	500Ω	50pF	0.3V	> 2.5V



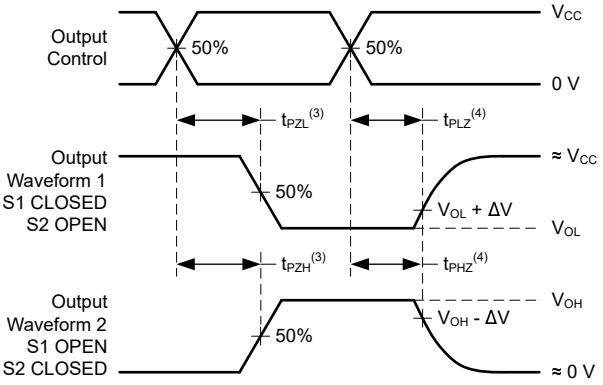
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

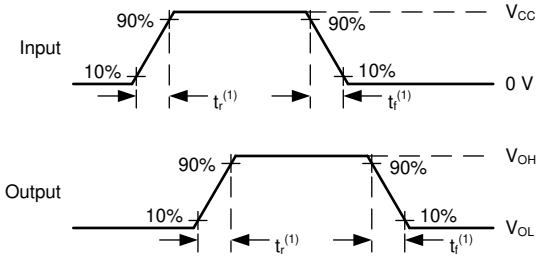
Figure 6-2. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

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7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function Y = A in positive logic.

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7.2 Feature Description

7.2.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.2.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

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7.2.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.

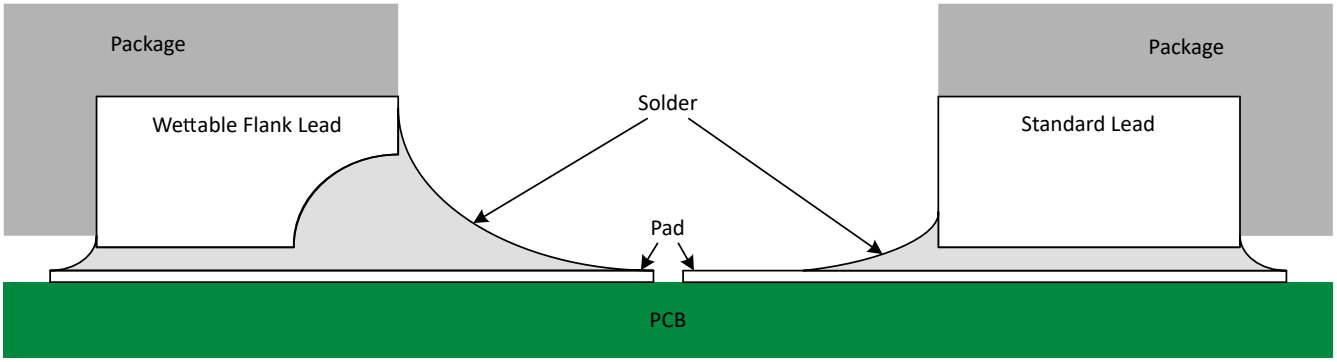


Figure 7-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-1, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

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7.2.4 Clamp Diode Structure

As shown in Figure 7-2, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

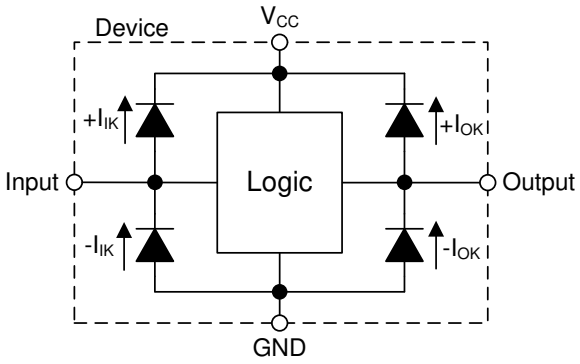


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

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7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
OE	A	Y
L	X	Z
H	L	L
H	H	H

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AC126-Q1 can be used to drive signals over relatively long traces or transmission lines. A series damping resistor placed in series with the transmitter's output can be used to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

8.2 Typical Application

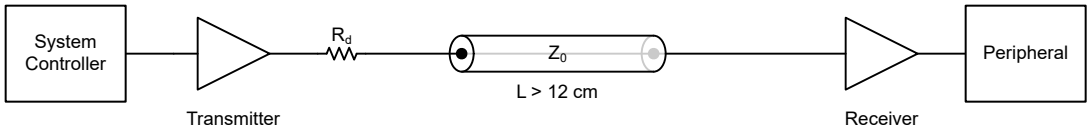


Figure 8-1. Typical Application Block Diagram

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8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC126-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC126-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC126-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AC126-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

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8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC126-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74AC126-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Electrical Characteristics* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AC126-Q1 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Application Curve

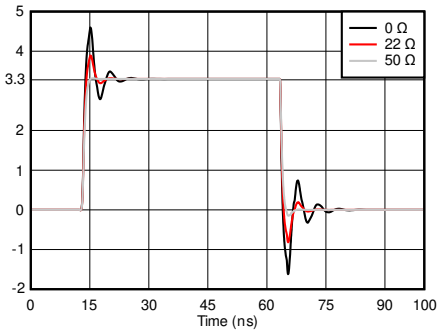


Figure 8-2. Simulated Signal Integrity at the Receiver with Different Damping Resistor (R_d) Values

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8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

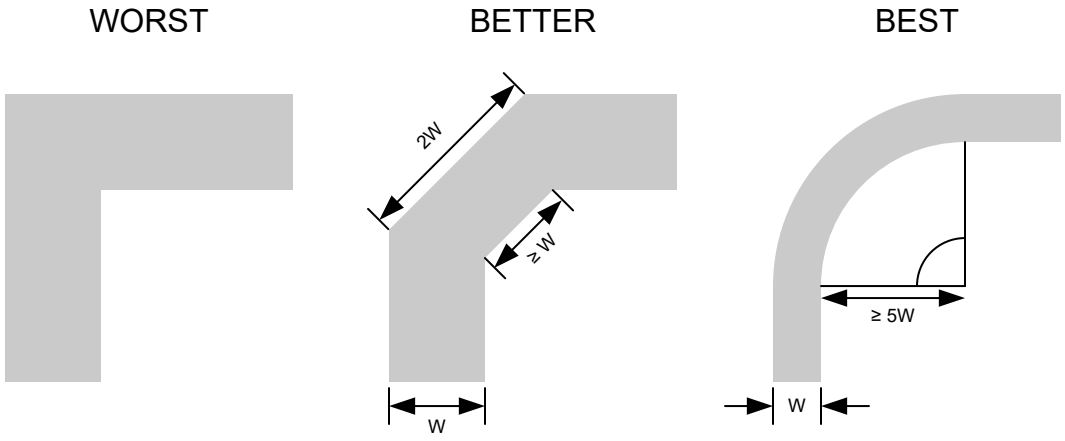


Figure 8-3. Example Trace Corners for Improved Signal Integrity

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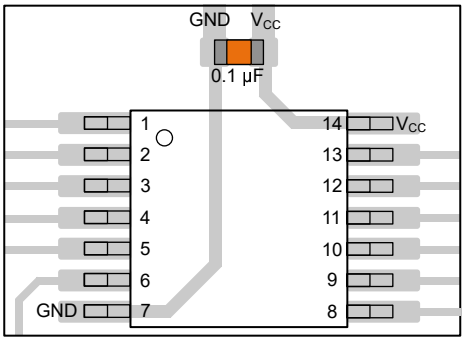


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

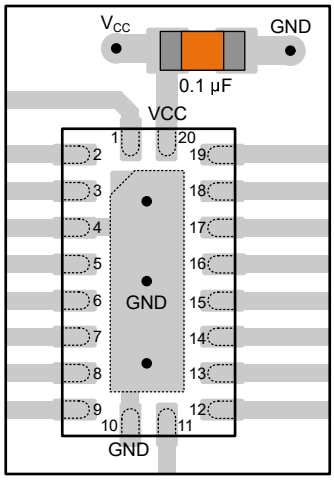


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

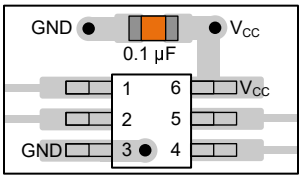


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

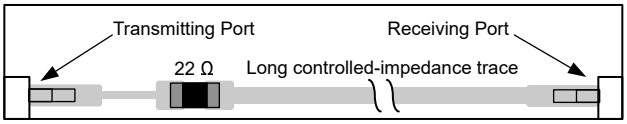


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AC126PWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	AC126Q
SN74AC126WBQARQ1	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	AC126Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AC126-Q1 :

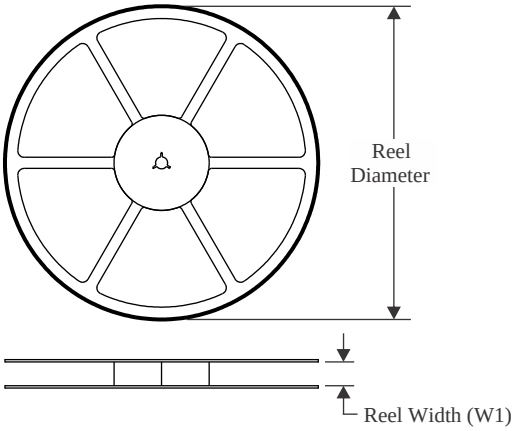
- Catalog : SN74AC126

NOTE: Qualified Version Definitions:

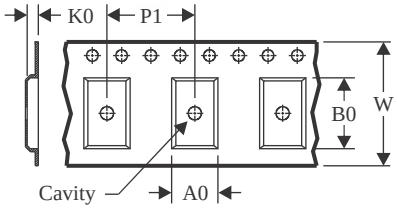
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

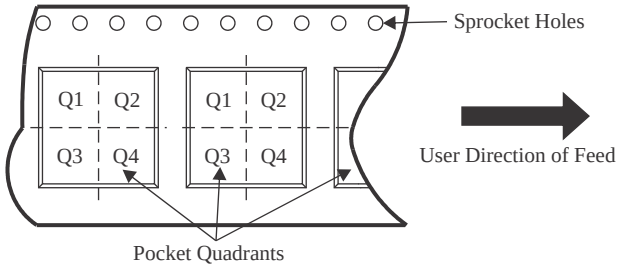


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

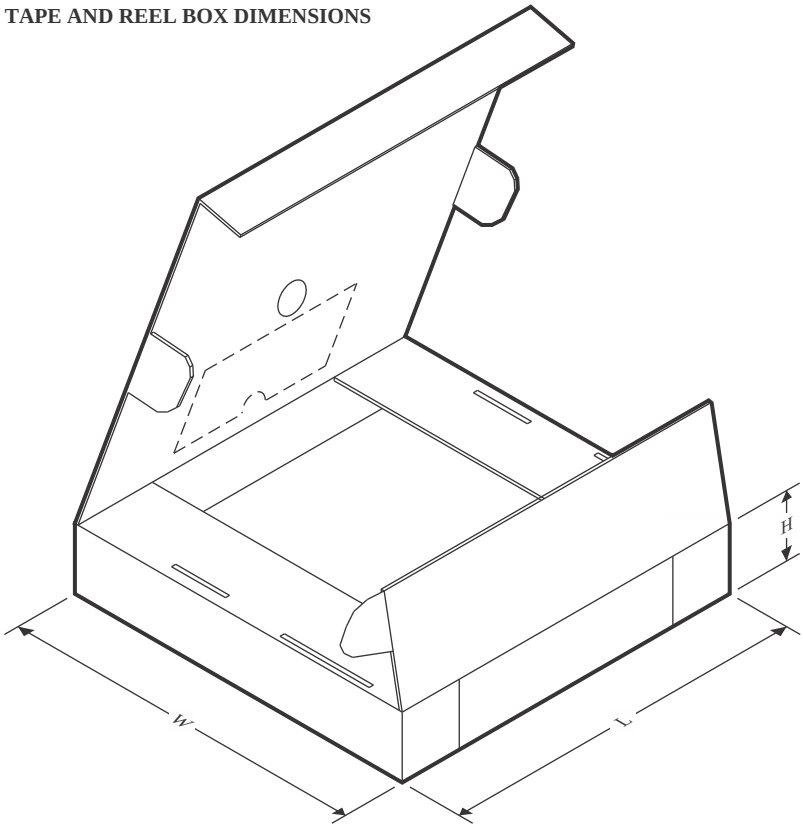
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC126PWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC126WBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC126PWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74AC126WBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

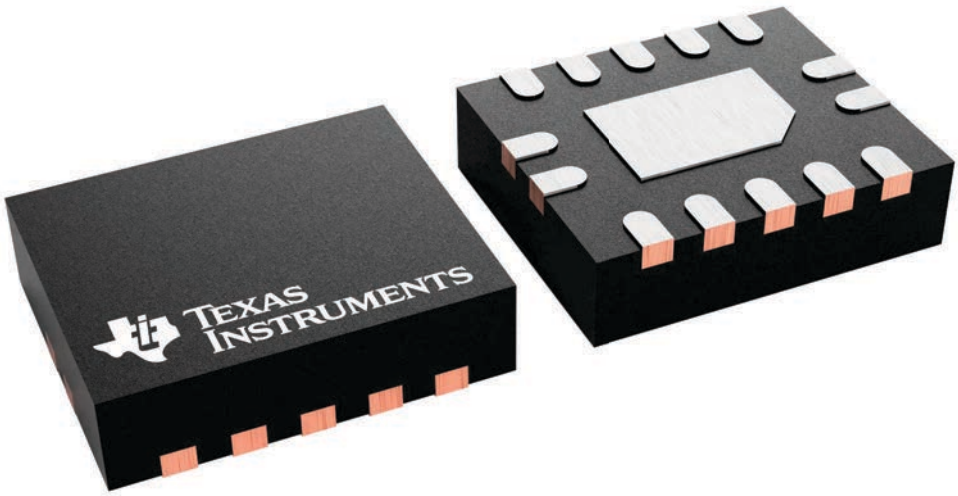
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

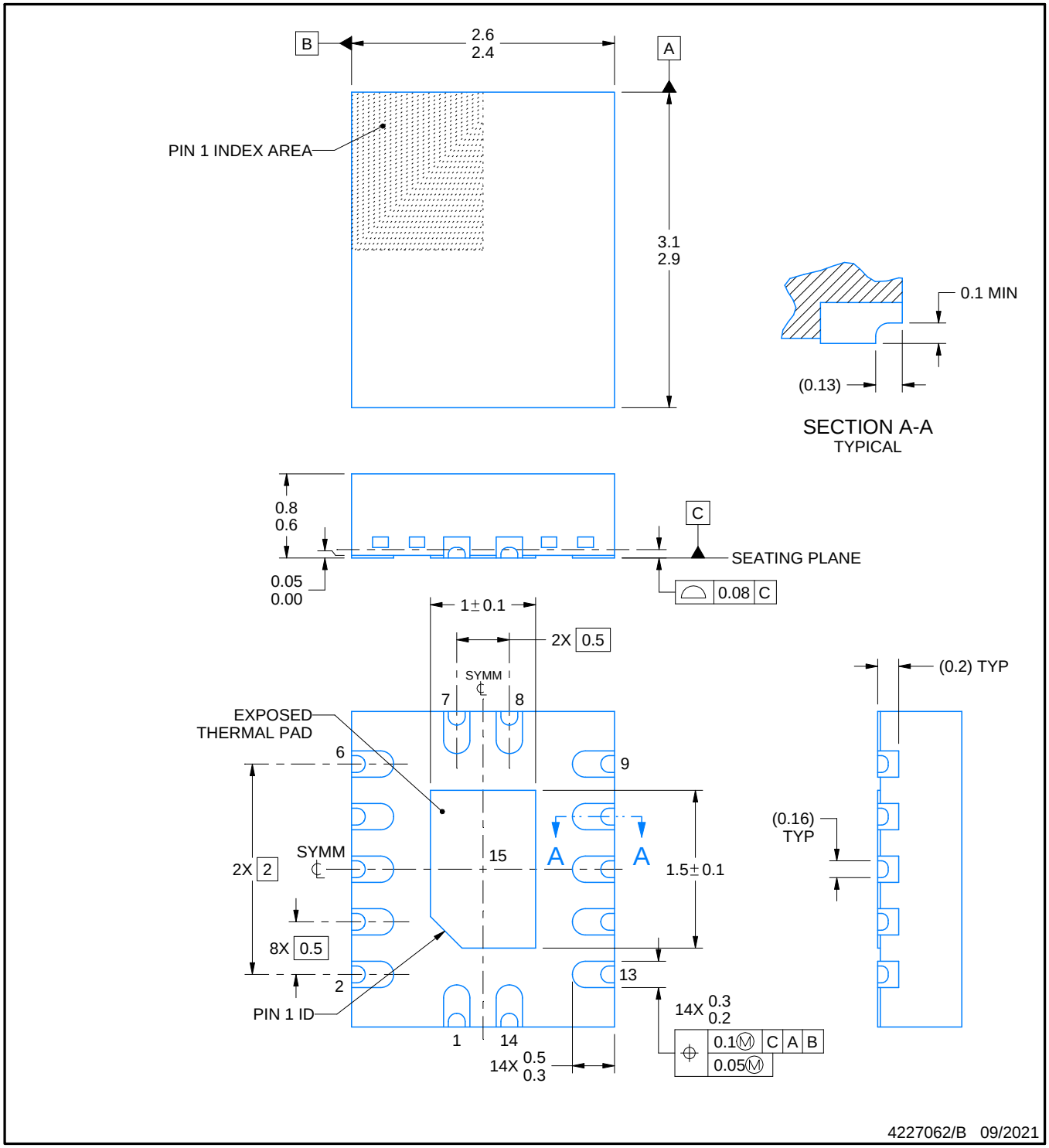


BQA0014B

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

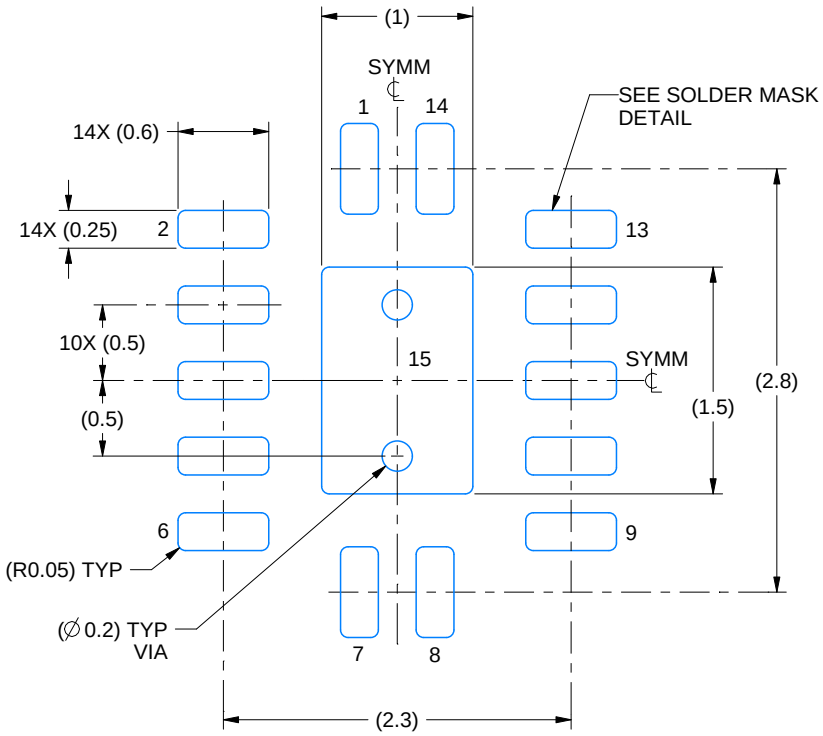
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

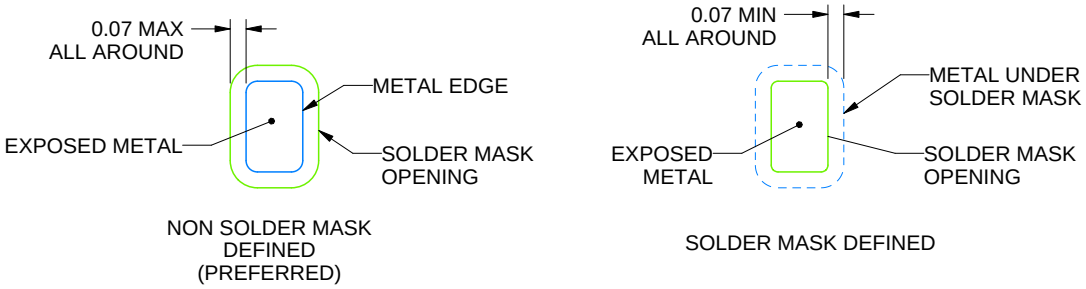
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

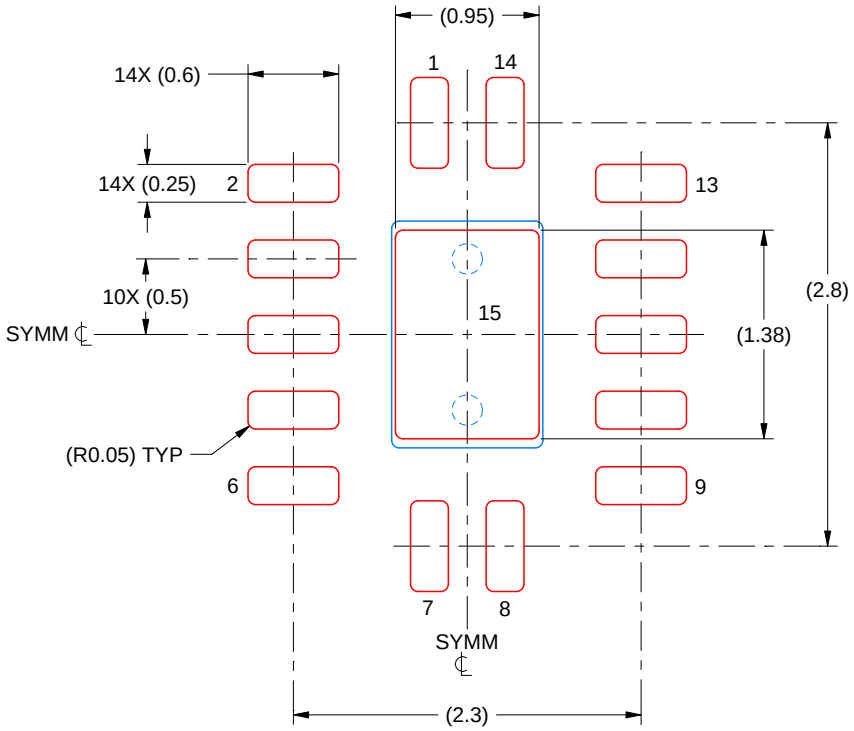


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

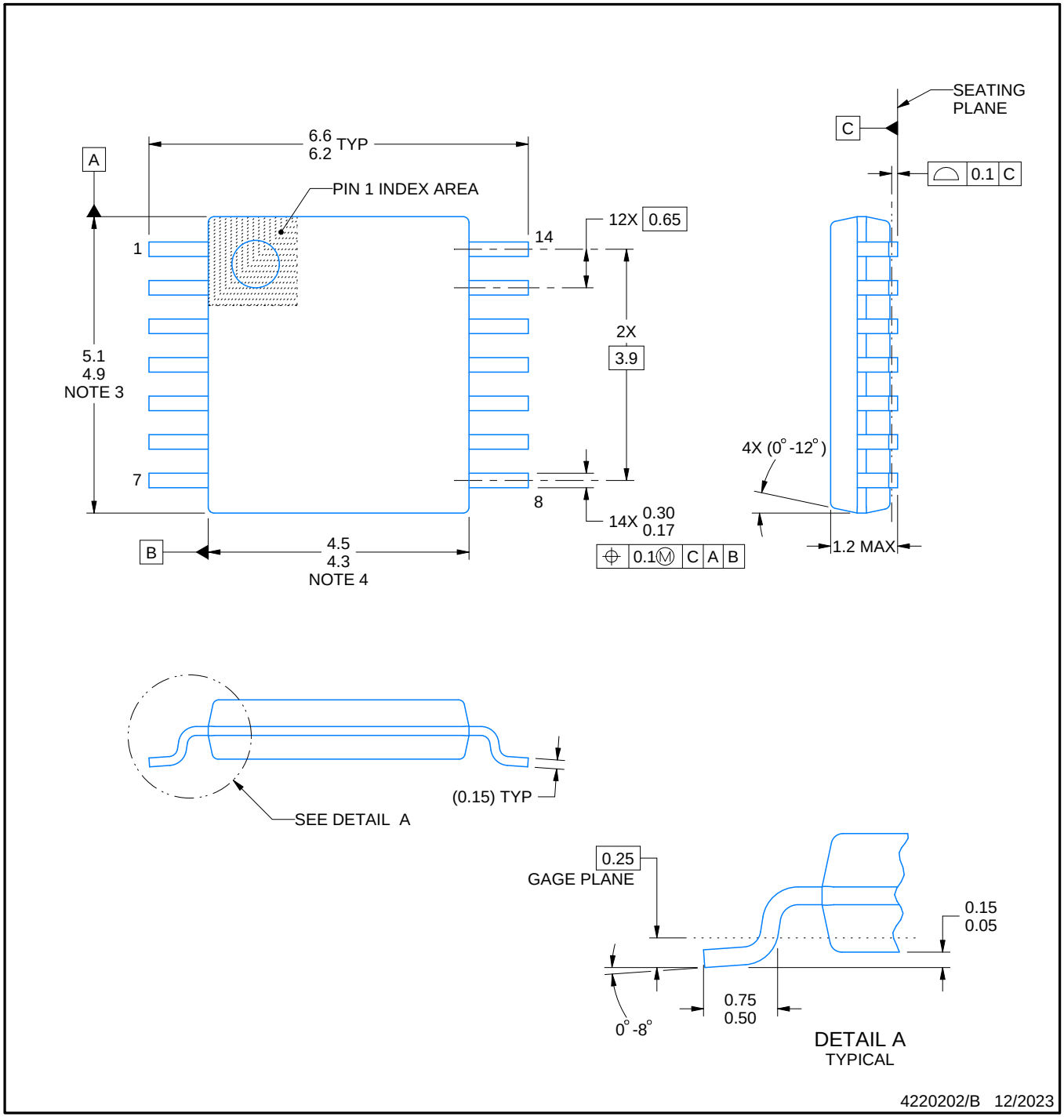
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

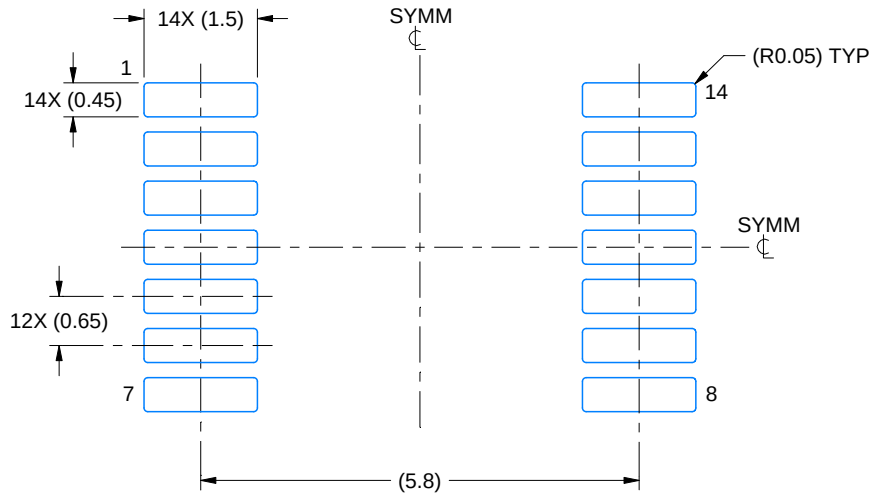
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

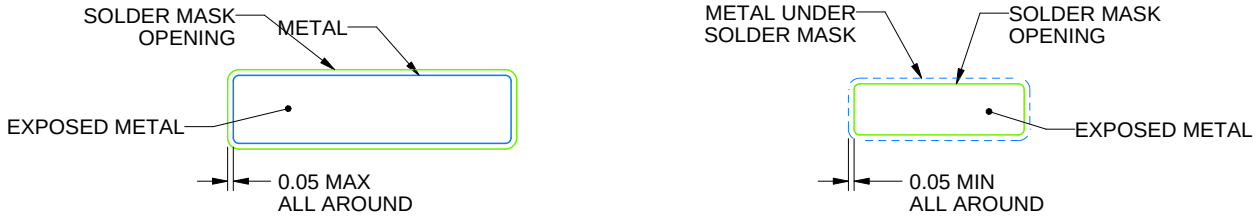


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

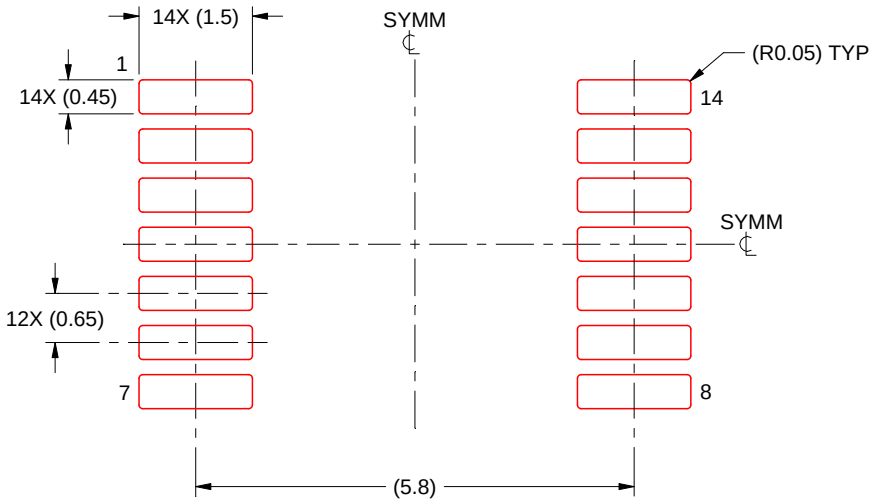


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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