DLPC8424, DLPC8444, and DLPC8454 High-Resolution Controllers

1 Features

- DLPC84x4 controllers support the following 1080p DMDs:
  - DLPC8424 supports the DLP230NP DMD up to 1080p at 60Hz and 540p at 120Hz (3D)
  - DLPC8444 supports the DLP472NPDMD up to 1080p at 240Hz (2D) and 120Hz (3D)
  - DLPC8454 supports the DLP473NE DMD up to 1080p at 240Hz (2D) and 120Hz (3D)
- Single V-by-One® HS video input port with 1, 2, 4, or 8 lanes
  - Up to 600MHz pixel clock and 2160p at 60Hz
  - Up to 3.0Gbps per input transmission rate
- Two FPD-Link video input ports, 6 lanes per port
  - Up to 300MHz pixel clock and 1080p at 120Hz
- Input formats supported
  - RGB and YCbCr
  - 4:4:4 and 4:2:2
- Internal Arm® processor
  - 52 configurable GPIOs
  - PWM generator
  - Capture and delay timers
  - USB 2.0 high-speed controller
  - SPI and I^2C controllers
  - UART and interrupt controllers
- Warping engine
  - 1D and 2D keystone correction
  - Embedded partial frame memory for video processing
- Additional image processing
  - Overlap color support
  - Variable refresh rate (VRR) support
  - Rolling buffer for reduced frame latency
  - DynamicBlack
  - Frame rate multiplication
  - Color coordinate adjustment
  - Color temperature adjustment
  - Programmable degamma
  - Read-side spatial-temporal multiplexing
  - Integrated support for 3-D display
- Splash screen display
- Serial flash for µP and PWM sequences
- System control
  - DMD power and reset driver control
  - DMD horizontal and vertical image flip
- JTAG boundary scan test support
- Supports LED, RGB laser, and laser-phosphor illumination-based systems

2 Applications

- Mobile smart TV
- Mobile projector
- Digital signage
- Lifestyle projector
- Education and Enterprise projector (DLP473NE)

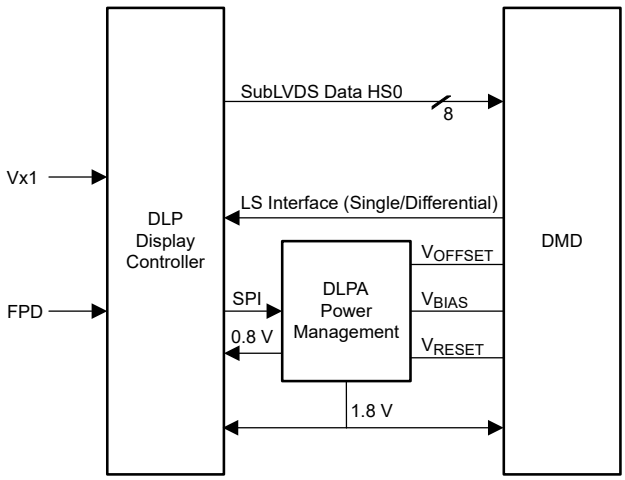
3 Description

The DLPC8424, DLPC8444, and DLPC8454 are 1080p FHD digital display controllers for TI DLP® Products. The DLP chipset comprises one display controller, one matched DMD, the DLPA3085 or DLPA3082 power management IC, and the DLPA100 motor driver IC (for laser-phosphor illumination systems only). This chipset fits display systems that require high resolution and high brightness in a small form factor. For reliable operation, the DLPC8424 or DLPC8444 or DLPC8454 display controller must always be used with the correct DMD and the DLPA3085 or DLPA3082 PMIC. Note: DLPA3085 is not supported by the DLPC8454.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
DLPC8424AMD	FCCSP (484)	9.00mm × 9.00mm
DLPC8444AMD	FCCSP (484)	9.00mm × 9.00mm
DLPC8454AMD	FCCSP (484)	9.00mm × 9.00mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



1080p FHD Display Chipset

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Compatability Table....3
5 Pin Configuration and Functions....4
5.1 Initialization, Board Level Test, and Debug....4
5.2 V-by-One Interface Input Data and Control....6
5.3 FPD-Link Port(s) Input Data and Control....7
5.4 DSI Input Data and Clock (Not Supported in DLPC8424, DLPC8444, and DLPC8454)....8
5.5 DMD SubLVDS Interface....9
5.6 DMD Reset and Low-Speed Interfaces....11
5.7 Flash Interface....11
5.8 Peripheral Interfaces....12
5.9 GPIO Peripheral Interface....13
5.10 Clock and PLL Support....17
5.11 Power and Ground....18
5.12 I/O Type Subscript Definition....20
5.13 Internal Pullup and Pulldown Characteristics....20
6 Specifications....21
6.1 Absolute Maximum Ratings....21
6.2 ESD Ratings....22
6.3 Recommended Operating Conditions....22
6.4 Thermal Information....23
6.5 Power Electrical Characteristics....23
6.6 Pin Electrical Characteristics....24
6.7 DMD SubLVDS Interface Electrical Characteristics....25
6.8 DMD Low-Speed Interface Electrical Characteristics....26
6.9 V-by-One Interface Electrical Characteristics....26
6.10 FPD Link LVDS Electrical Characteristics....27
6.11 USB Electrical Characteristics....27
6.12 System Oscillator Timing Requirements....28
6.13 Power Supply and Reset Timing Requirements....29
6.14 V-by-One Interface General Timing Requirements....30
6.15 FPD Link Interface General Timing Requirements....31
6.16 Flash Interface Timing Requirements....31
6.17 Source Frame Timing Requirements....32
6.18 Synchronous Serial Port Interface Timing Requirements....33
6.19 I^2C Interface Timing Requirements....35
6.20 Programmable Output Clock Timing Requirements....35
6.21 JTAG Boundary Scan Interface Timing Requirements (Debug Only)....35
6.22 DMD Low-Speed Interface Timing Requirements....37
6.23 DMD SubLVDS Interface Timing Requirements....37
7 Detailed Description....38
7.1 Overview....38
7.2 Functional Block Diagrams....38
7.3 Feature Description....40
8 Power Supply Recommendations....62
8.1 System Power-Up and Power-Down Sequence....62
8.2 DMD Fast Park Control (PARKZ)....64
8.3 Power Supply Management....65
8.4 Hotplug Usage....65
8.5 Power Supplies for Unused Input Source Interfaces....65
8.6 Power Supplies....65
9 Layout....66
9.1 Layout Guidelines....66
9.2 Thermal Considerations....72
10 Device and Documentation Support....73
10.1 Third-Party Products Disclaimer....73
10.2 Documentation Support....73
10.3 Receiving Notification of Documentation Updates....73
10.4 Support Resources....73
10.5 Device Nomenclature....74
10.6 Trademarks....74
10.7 Electrostatic Discharge Caution....74
10.8 Glossary....74
11 Revision History....75
12 Mechanical, Packaging, and Orderable Information....75

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4 Compatability Table

The DLP controller, DMD, and PMIC must be matched according to the Device Compatability Table to comprise a valid chispet.

Table 4-1. Device Compatability Table

DLP Controller	DMD	DLPA PMIC
DLPC8424	DLP230NP	DLPA3085 (no overlap) or DLPA3082 (with overlap)
DLPC8444	DLP472NP	DLPA3085 (no overlap) or DLPA3082 (with overlap)
DLPC8454	DLP473NE	DLPA3082 (with overlap)

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5 Pin Configuration and Functions

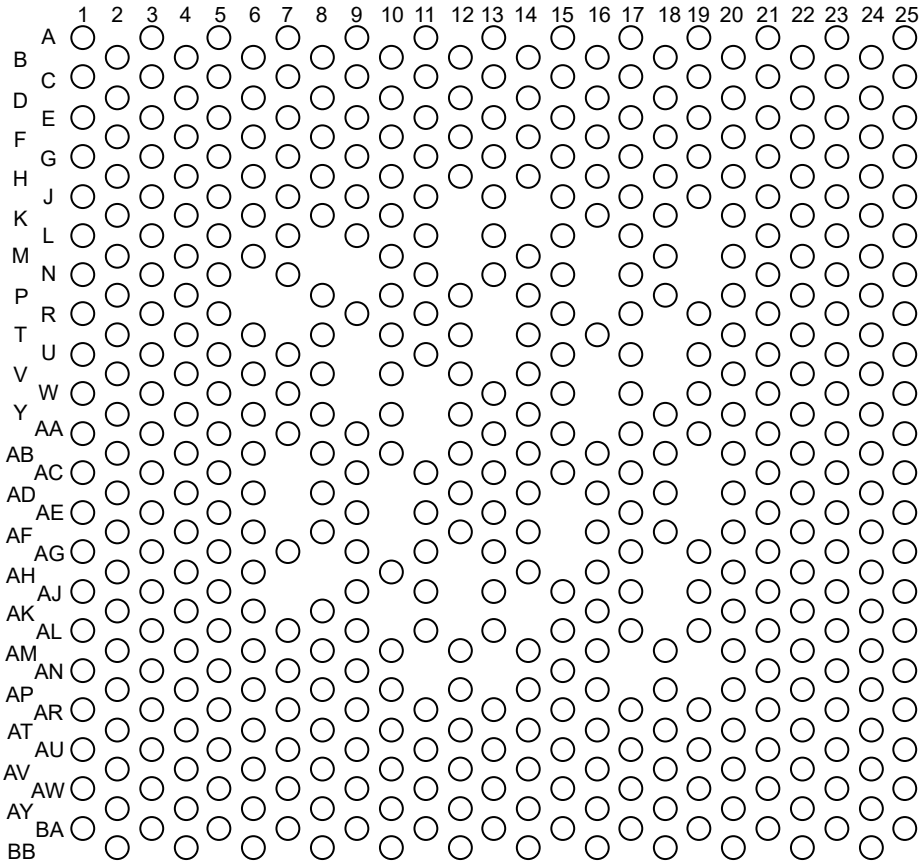

Figure 5-1. AMD Package 484-Pin FCCSP Top View

5.1 Initialization, Board Level Test, and Debug

Table 5-1. Initialization, Board Level Test, and Debug

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
PROJ_ON	AP2	I1	Normal mirror parking request (active low): To be driven by the PROJ_ON output of the host. A logic low on this signal causes the Controller to PARK the DMD, but it does not power down the DMD (the DLPA does that instead). The minimum high time is 200ms. The minimum low time is 200ms.
RESETZ	P2	I1	Power-on reset (active low input with a hysteresis buffer). Self-configuration starts when a low-to-high transition is detected on RESETZ. All controller power and clocks must be stable before this reset is deasserted. No signals are in their active state while RESETZ is asserted. This pin is typically connected to the RESETZ pin of the DLPA PMIC.
PARKZ	AR1	I1	DMD fast park control (active low Input with a hysteresis buffer). This signal is used to quickly park the DMD when a loss of power is imminent. The longest lifetime of the DMD may not be achieved with the fast park operation; therefore, this signal is intended to only be asserted when a normal park operation is unable to be completed. The PARKZ signal is typically provided from the DLPA interrupt output signal.
JTAGTCK	V24	I2	JTAG and ARM-ICE Serial Data Clock. This signal is shared between JTAG and ARM-ICE (TI test only), operation. Includes a weak internal pulldown
JTAGTMS1	U23	I2	JTAG Test Mode Select. Includes a weak internal pullup
JTAGTMS2	W25	I2	ARM-ICE Test Mode Select For normal operation, this pin must be left open or unconnected. Includes a weak internal pullup

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Table 5-1. Initialization, Board Level Test, and Debug (continued)

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
JTAGTRSTZ	AA25	I2	JTAG, ARM-ICE Reset. *For normal operation, this pin must be pulled to ground through an external resistor with a value 8kΩ or less. Failure to pull this pin low during normal operation causes start-up and initialization problems.* For JTAG Boundary Scan and ARM-ICE Debug operation, this pin must be pulled up or left disconnected. Includes a weak internal pullup and hysteresis
JTAGTDI	Y24	I2	JTAG, ARM-ICE, and CPU MBIST: Serial Data In. Includes a weak internal pullup
JTAGTDO1	V22	B14	JTAG Serial Data Out
JTAGTDO2	W23	B14	ARM-ICE Serial Data Out. For normal operation, this pin requires an external pullup resistor with a value of ≤ 9.15kΩ.
ETM_TRACECLK	U25	O14	Reserved Pin, must be left unconnected.
ETM_TRACECTL	T24	O14	Reserved Pin, must be left unconnected.
TSTPT_0	T22	B14	Test pin 0 This pin has an internal pulldown and may require an external pullup resistor (no pullup: Normal Boot, pullup: Wait for Host commands) with a value of ≤ 9.15kΩ.
TSTPT_1	R25	B14	Test pin 1 This pin has an internal pulldown for Normal Boot operation.
TSTPT_2	R23	B14	Test pin 2 This pin has an internal pulldown and may require an external pullup resistor (no pullup: I^2C address = 0x36, pullup: I^2C address = 0x34) with a value of ≤ 9.15kΩ.
TSTPT_3	P24	B14	Test pin 3 This pin has an internal pulldown and may require an external pullup resistor (no pullup: Host interface is USB or I^2C, pullup: Host interface is I^2C only) with a value of ≤ 9.15kΩ.
TSTPT_4	N25	B14	Test pin 4 This pin has an internal pulldown resistor.
TSTPT_5	P22	B14	Test pin 5 This pin has an internal pulldown resistor.
TSTPT_6	N23	B14	Test pin 6 This pin has an internal pulldown resistor.
TSTPT_7	M24	B14	Test pin 7 This pin has an internal pulldown resistor.
GPTP0	AA23	B13	General Purpose Test pin 0 This pin has an internal pulldown and may require an external pullup resistor (no pullup: external crystal, pullup: external clock) with a value of ≤ 9.15kΩ.
GPTP1	AB22	B13	General Purpose Test pin 1 This pin has an internal pulldown resistor.
GPTP2	AC25	B13	General Purpose Test pin 2 This pin has an internal pulldown resistor.
ATB_0_H	AH4	PWR	Reserved Pin, must be left unconnected.
ATB_1_H	AJ5	PWR	Reserved Pin, must be left unconnected.
ATEST	G13	PWR	Reserved Pin, must be left unconnected.
CAP_VDDS_FLSH	AD22	PWR	External bias capacitance
CAP_VDDS_INTF	AJ21	PWR	External bias capacitance
IFORCE	L3	PWR	Manufacturing use only. Must be tied to ground.
VSENSE	K2	PWR	Reserved Pin, must be left unconnected.
HWTEST_EN	Y22	I2	Reserved Pin. This signal must be connected directly to ground on the PCB for normal operation. Includes weak internal pulldown and hysteresis.

(1) See Section 5.12 for more information on I/O definitions

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5.2 V-by-One Interface Input Data and Control

PIN		I/O [1]	DESCRIPTION [2] [3] [4]
NAME	NO.		
P1_VX1_D0_P	AV8	I5	V-by-One interface data lanes
P1_VX1_D0_N	AU9		
P1_VX1_D1_P	BB8		
P1_VX1_D1_N	AY8		
P1_VX1_D2_P	BA9		
P1_VX1_D2_N	AW9		
P1_VX1_D3_P	BB10		
P1_VX1_D3_N	AY10		
P1_VX1_D4_P	BA11		
P1_VX1_D4_N	AW11		
P1_VX1_D5_P	AV12		
P1_VX1_D5_N	AU13		
P1_VX1_D6_P	BB12		
P1_VX1_D6_N	AY12		
P1_VX1_D7_P	BA13		
P1_VX1_D7_N	AW13		
P1_HTPDN	AN3	O10	V-by-One interface hot plug detect (controller receiver pulls this signal low to indicate its presence to the transmitter). This signal is open-drain at the controller output. A pullup resistor is required at the transmitter.
P1_LOCKN	AM4	O10	V-by-One interface clock detect lock (controller receiver pulls this signal low to indicate clock extraction lock to the transmitter). This signal is open-drain at the controller output. A pullup resistor is required at the transmitter.
P1_RREF	AU11	PWR	V-by-One bias resistor input

(1) See I/O Type Subscript Definition for more information on I/O definitions.
(2) The system supports 1-lane, 2-lane, 4-lane, or 8-lane operation, based on the bandwidth requirement of the input source. The inputs for any unused data lanes must be left open; not all lanes are used. If the V-by-One video interface is not used at all, the pins should be connected to ground.
(3) The V-by-One port supports limited lane remapping to help optimize board layout. The details are described in V-by-One Interface.
(4) In this document, the terms V-by-One and Vx1 are used interchangeably.

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5.3 FPD-Link Port(s) Input Data and Control

PIN		I/O [1]	DESCRIPTION [2] [3] [4]
NAME	NO.		
P2A_LVDS_C_P	BA17	I4	FPD-Link Port A Clock Lane
P2A_LVDS_C_N	AW17	I4	
P2A_LVDS_D0_P	BA15	I4	FPD-Link Port A Data Lanes
P2A_LVDS_D0_N	AW15	I4	
P2A_LVDS_D1_P	BB16	I4	
P2A_LVDS_D1_N	AY16	I4	
P2A_LVDS_D2_P	AV16	I4	
P2A_LVDS_D2_N	AU15	I4	
P2A_LVDS_D3_P	BB18	I4	
P2A_LVDS_D3_N	AY18	I4	
P2A_LVDS_D4_P	AV18	I4	
P2A_LVDS_D4_N	AU17	I4	
P2A_LVDS_RPI	AT16	PWR	FPD-Link Port A Bias Resistor Pin
P2B_LVDS_C_P	BA21	I4	FPD-Link Port B Clock Lane
P2B_LVDS_C_N	AW21	I4	
P2B_LVDS_D0_P	BB20	I4	FPD-Link Port B Data Lanes
P2B_LVDS_D0_N	AY20	I4	
P2B_LVDS_D1_P	AV20	I4	
P2B_LVDS_D1_N	AU19	I4	
P2B_LVDS_D2_P	AV22	I4	
P2B_LVDS_D2_N	AU21	I4	
P2B_LVDS_D3_P	BB22	I4	
P2B_LVDS_D3_N	AY22	I4	
P2B_LVDS_D4_P	BA23	I4	
P2B_LVDS_D4_N	AW23	I4	
P2B_LVDS_RPI	AT20	PWR	FPD-Link Port B Bias Resistor Pin

(1) See Section 5.12 for more information on I/O definitions.
(2) Throughout this document, the terms FPD and FPD-Link refer to FPD-Link I.
(3) Tie the inputs for any unused port(s) to ground, or pull to ground through an external resistor.
(4) If only one of these two ports is needed, either port can be used, with the other port to be treated as an unused port.

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5.4 DSI Input Data and Clock (Not Supported in DLPC8424, DLPC8444, and DLPC8454)

PIN		I/O [1]	DESCRIPTION[2]
NAME	NO.		
P3_DSI_C_P	BB6	I6	Reserved
P3_DSI_C_N	AY6	I6	
P3_DSI_D0_P	BA5	I6	Reserved
P3_DSI_D0_N	AW5	I6	
P3_DSI_D1_P	BB4	I6	
P3_DSI_D1_N	AY4	I6	
P3_DSI_D2_P	AV4	I6	
P3_DSI_D2_N	AU5	I6	
P3_DSI_D3_P	BA3	I6	
P3_DSI_D3_N	AW3	I6	
P3_DSI_RCALIB	AV6	PWR	Reserved

(1) See Section 5.12 for more information on I/O definitions.
(2) Tie the inputs for any unused port(s) to ground, or pull to ground through an external resistor.

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5.5 DMD SubLVDS Interface

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
DMD_HS0_CLK_P	B6	O15	Channel 0 DMD SubLVDS clock lane
DMD_HS0_CLK_N	D6	O15	
DMD_HS0_WDATA0_P	A3	O15	Channel 0 DMD SubLVDS data lane
DMD_HS0_WDATA0_N	C3	O15	
DMD_HS0_WDATA1_P	F4	O15	
DMD_HS0_WDATA1_N	E5	O15	
DMD_HS0_WDATA2_P	B4	O15	
DMD_HS0_WDATA2_N	D4	O15	
DMD_HS0_WDATA3_P	A5	O15	
DMD_HS0_WDATA3_N	C5	O15	
DMD_HS0_WDATA4_P	F6	O15	
DMD_HS0_WDATA4_N	E7	O15	
DMD_HS0_WDATA5_P	A7	O15	
DMD_HS0_WDATA5_N	C7	O15	
DMD_HS0_WDATA6_P	F8	O15	
DMD_HS0_WDATA6_N	E9	O15	
DMD_HS0_WDATA7_P	B8	O15	
DMD_HS0_WDATA7_N	D8	O15	
DMD_HS1_CLK_P	A13	O15	Channel 1 DMD SubLVDS clock lane
DMD_HS1_CLK_N	C13	O15	
DMD_HS1_WDATA0_P	B10	O15	Channel 1 DMD SubLVDS data lane
DMD_HS1_WDATA0_N	D10	O15	
DMD_HS1_WDATA1_P	A11	O15	
DMD_HS1_WDATA1_N	C11	O15	
DMD_HS1_WDATA2_P	F10	O15	
DMD_HS1_WDATA2_N	E11	O15	
DMD_HS1_WDATA3_P	B12	O15	
DMD_HS1_WDATA3_N	D12	O15	
DMD_HS1_WDATA4_P	B14	O15	
DMD_HS1_WDATA4_N	D14	O15	
DMD_HS1_WDATA5_P	F12	O15	
DMD_HS1_WDATA5_N	E13	O15	
DMD_HS1_WDATA6_P	A15	O15	
DMD_HS1_WDATA6_N	C15	O15	
DMD_HS1_WDATA7_P	F14	O15	
DMD_HS1_WDATA7_N	E15	O15	
DMD_HS2_CLK_P	A19	O15	Channel 2 DMD SubLVDS clock lane
DMD_HS2_CLK_N	C19	O15	

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5.5 DMD SubLVDS Interface (continued)

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
DMD_HS2_WDATA0_P	A17	O15	Channel 2 DMD SubLVDS data lane
DMD_HS2_WDATA0_N	C17	O15	
DMD_HS2_WDATA1_P	F16	O15	
DMD_HS2_WDATA1_N	E17	O15	
DMD_HS2_WDATA2_P	B18	O15	
DMD_HS2_WDATA2_N	D18	O15	
DMD_HS2_WDATA3_P	F18	O15	
DMD_HS2_WDATA3_N	E19	O15	
DMD_HS2_WDATA4_P	B20	O15	
DMD_HS2_WDATA4_N	D20	O15	
DMD_HS2_WDATA5_P	A21	O15	
DMD_HS2_WDATA5_N	C21	O15	
DMD_HS2_WDATA6_P	F20	O15	
DMD_HS2_WDATA6_N	E21	O15	
DMD_HS2_WDATA7_P	B22	O15	
DMD_HS2_WDATA7_N	D22	O15	
DMD_HS3_CLK_P	H24	O15	Channel 3 DMD SubLVDS clock lane
DMD_HS3_CLK_N	J25	O15	
DMD_HS3_WDATA0_P	B24	O15	Channel 3 DMD SubLVDS data lane
DMD_HS3_WDATA0_N	C25	O15	
DMD_HS3_WDATA1_P	D24	O15	
DMD_HS3_WDATA1_N	E25	O15	
DMD_HS3_WDATA2_P	F22	O15	
DMD_HS3_WDATA2_N	E23	O15	
DMD_HS3_WDATA3_P	F24	O15	
DMD_HS3_WDATA3_N	G25	O15	
DMD_HS3_WDATA4_P	H22	O15	
DMD_HS3_WDATA4_N	G23	O15	
DMD_HS3_WDATA5_P	K24	O15	
DMD_HS3_WDATA5_N	L25	O15	
DMD_HS3_WDATA6_P	K22	O15	
DMD_HS3_WDATA6_N	J23	O15	
DMD_HS3_WDATA7_P	M22	O15	
DMD_HS3_WDATA7_N	L23	O15	

(1) See Section 5.12 for more information on I/O definitions.

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5.6 DMD Reset and Low-Speed Interfaces

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
DMD_LS0_CLK_P	F2	O15	DMD low-speed differential interface, Port 0 Clock
DMD_LS0_CLK_N	E1	O15	
DMD_LS0_WDATA_P	B2	O15	DMD low-speed differential interface, Port 0 Write Data
DMD_LS0_WDATA_N	C1	O15	
DMD_LS1_CLK	G1	O12	DMD low-speed single-ended interface, Port 1 Clock
DMD_LS1_WDATA	E3	O12	DMD low-speed single-ended interface, Port 1 Write Data
DMD_LS2_CLK	H2	O12	DMD low-speed single-ended interface, Port 2 Clock
DMD_LS2_WDATA	G3	O12	DMD low-speed single-ended interface, Port 2 Write Data
DMD_LS0_RDATA	H4	I1	DMD, low-speed single-ended serial interface, Port 0 Read Data [2]
DMD_LS1_RDATA	J3	I1	DMD, low-speed single-ended serial interface, Port 1 Read Data [2]. If this port is not used, this signal requires an external pullup or pulldown to keep this input from floating.
DMD_LS2_RDATA	M4	I1	DMD, low-speed single-ended serial interface, Port 2 Read Data [2]. If this port is not used, this signal requires an external pullup or pulldown to keep this input from floating.
DMD_LS3_RDATA	K4	I1	DMD, low-speed single-ended serial interface, Port 3 Read Data [2]. If this port is not used, this signal requires an external pullup or pulldown to keep this input from floating.
DMD_DEN_ARSTZ	J1	O10	DMD driver enable signal / Active Low Asynchronous Reset ('1' = Enabled, '0' = Reset) This signal is driven low after the DMD is parked and before power is removed from the DMD. *If the 1.8V power to the controller is independent of the 1.8V power to the DMD, then an external pulldown resistor must be used to hold the signal low in the event the controller power is inactive while DMD power is applied.*

(1) See Section 5.12 for more information on I/O definitions.
(2) All control interface reads make use of the single ended low-speed signals. The read data is clocked by the low-speed differential write clock.

5.7 Flash Interface

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
FLSH_CSZ	AG23	B16	Chip select: Boot FLASH Only (Boot FLASH must use this chip select)
FLSH_CLK	AG25	B16	Flash Clock
FLSH_DATA0	AH22	B16	Address bit 0 (LSB)
FLSH_DATA1	AH24	B16	Address bit 1
FLSH_DATA2	AJ25	B16	Address bit 2
FLSH_DATA3	AJ23	B16	Address bit 3

(1) See Section 5.12 for more information on I/O definitions.

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5.8 Peripheral Interfaces

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
IIC0_SCL	AL25	B18	I2C Port 0 (Primary-Secondary), Typically Secondary for Host Command and Control to Controller, SCL (bidirectional, open-drain): An external pullup is required. The minimum acceptable value for this pullup is 470Ω.
IIC0_SDA	AK24	B18	
SSP0_DO	AP24	O17	SSP/SPI Port 0 Data Out (Primary): Transmit data pin
SSP0_DI	AN23	I3	SSP/SPI Port 0 Data In (Primary): Receive data pin
SSP0_CLK	AN25	O17	SSP/SPI Port 0 Clock (Primary): Clock pin
SSP0_CSZ_0	AM22	O17	SPI Port 0 chip select 0 (Primary): Chip select (Active Low). An external pullup resistor (≤ 10kΩ) is suggested to avoid a floating chip select input to the external device.
USB_DAT_P	AU1	B7	USB OTG Data Lane
USB_DAT_N	AW1	B7	
USB_VBUS	AP4	B7	USB OTG 5V Power Supply Detection
USB_ID	AT2	I7	USB OTG Mini Receptacle Identification
USB_TXRTUNE	AR3	PWR	RTTRIM USB OTG Reference Resistor: An external reference resistor, for calibrating the on-chip resistors, must be connected with a value of 499Ω.
HOST_IRQ	AK22	O17	Host interrupt (output): HOST_IRQ indicates when the DLPC auto-initialization is in progress and, most importantly, when it completes. The HOST_IRQ also toggles during command handling to indicate when the execution is in progress. This pin is tri-stated during reset. An external pullup must be included on this signal.

(1) See Section 5.12 for more information on I/O definitions.

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5.9 GPIO Peripheral Interface

PIN		I/O [1]	DESCRIPTION [2] [3] [4]
NAME	NO.		
GPIO_00	AR25	B17	General purpose I/O 00: Options: 1. Alt 0: SSP1_SCLK (O-P/I-S) 2. Alt 1: XY_IF_SCLK (I) 3. SW GPIO (B)
GPIO_01	AU25	B17	General purpose I/O 01: Options: 1. Alt 0: SSP1_DI (I) 2. Alt 1: XY_IF_DI(I) 3. SW GPIO (B)
GPIO_02	AW25	B17	General purpose I/O 02: Options: 1. Alt 0: SSP1_DO (O) 2. Alt 1: XY_IF_DO (O) 3. SW GPIO (B)
GPIO_03	AT24	B17	General purpose I/O 03: Options: 1. Alt 0: SSP1_CSZ_0 (O-P/I-S) 2. Alt 1: XY_IF_CSZ (I) 3. SW GPIO (B)
GPIO_04	AV24	B17	General purpose I/O 04: Options: 1. Alt 0: SSP1_CSZ_1 (O-P/I-S) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_05	AR23	B17	General purpose I/O 05: Options: 1. Alt 0: SSP1_CSZ_2 (O-P/I-S) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_06	AP22	B17	General purpose I/O 06: Options: 1. Alt 0: SSP0_BCSZ (O-P/I-S) 2. Alt 1: SSP1_BCSZ (O-P/I-S) 3. SW GPIO (B)
GPIO_07	AL23	B17	General purpose I/O 07: Options: 1. Alt 0: IIC1_SCL (B) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_08	AM24	B17	General purpose I/O 08: Options: 1. Alt 0: IIC1_SDA (B) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_09	N3	B10	General purpose I/O 09: Options: 1. Alt 0: WPC_COLOR_SENSOR_VSYNC(O) 2. Alt 1: MEMAUX_1(O) 3. SW GPIO (B)
GPIO_10	P4	B9	General purpose I/O 10: Options: 1. Alt 0: UART1_RSTZ (O) 2. Alt 1: N/A 3. SW GPIO (B)

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5.9 GPIO Peripheral Interface (continued)

PIN		I/O [1]	DESCRIPTION [2] [3] [4]
NAME	NO.		
GPIO_11	T4	B10	General purpose I/O 11: Options: 1. Alt 0: UART1_CTSZ(I) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_12	V4	B10	General purpose I/O 12: Options: 1. Alt 0: DMD_PWR_EN (O) 2. Alt 1: RC_CHARGE (O) 3. SW GPIO (B)
GPIO_13	AD24	B14	General purpose I/O 13: Options: 1. Alt 0: PAUX0 (O) 2. Alt 1: LED_SEL0 (O) 3. SW GPIO (B)
GPIO_14	AC23	B14	General purpose I/O 14: Options: 1. Alt 0: PAUX1 (O) 2. Alt 1: LED_SEL1 (O) 3. SW GPIO (B)
GPIO_15	AE25	B14	General purpose I/O 15: Options: 1. Alt 0: PAUX2 (O) 2. Alt 1: LED_SEL2 (O) 3. SW GPIO (B)
GPIO_16	AE23	B14	General purpose I/O 16: Options: 1. Alt 0: PAUX3 (O) 2. Alt 1: LED_SEL3 (O) 3. SW GPIO (B)
GPIO_17	AF24	B13	General purpose I/O 17: Options: 1. Alt 0: PAUX4 (O) 2. Alt 1: LED_SEL4 (O) 3. SW GPIO (B)
GPIO_18	AF22	B13	General purpose I/O 18: Options: 1. Alt 0: PAUX5 (O) 2. Alt 1: LED_SEL5 (O) 3. SW GPIO (B)
GPIO_19	R1	B10	General purpose I/O 19: Options: 1. Alt 0: PAUX6 (O) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_20	R3	B10	General purpose I/O 20: Options: 1. Alt 0: PAUX7 (O) 2. Alt 1: SL_Trigger (I) 3. SW GPIO (B)
GPIO_21	U1	B10	General purpose I/O 21: Options: 1. Alt 0: PAUX8 (O) 2. Alt 1: N/A 3. SW GPIO (B)

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5.9 GPIO Peripheral Interface (continued)

PIN		I/O [1]	DESCRIPTION [2] [3] [4]
NAME	NO.		
GPIO_22	T2	B9	General purpose I/O 22: Options: 1. Alt 0: PAUX9 (O) 2. Alt 1: CW_INDEX0 (I) 3. SW GPIO (B)
GPIO_23	U3	B10	General purpose I/O 23: Options: 1. Alt 0: PAUX10 (O) 2. Alt 1: PWM_OUT_CW0 (O) 3. SW GPIO (B)
GPIO_24	W1	B10	General purpose I/O 24: Options: 1. Alt 0: PAUX11 (O) 2. Alt 1: PWM_OUT_CW1 (O) 3. SW GPIO (B)
GPIO_25	V2	B10	General purpose I/O 25: Options: 1. Alt 0: PWM_OUT_RLED (O) 2. Alt 1: CMP_MSEL_0 (O) 3. SW GPIO (B)
GPIO_26	W3	B10	General purpose I/O 26: Options: 1. Alt 0: PWM_OUT_GLED (O) 2. Alt 1: CMP_PWM (O) 3. SW GPIO (B)
GPIO_27	AA1	B10	General purpose I/O 27: Options: 1. Alt 0: PWM_OUT_BLED (O) 2. Alt 1: CMP_OUT (I) 3. SW GPIO (B)
GPIO_28	Y4	B10	General purpose I/O 28: Options: 1. Alt 0: PWM_OUT_IRLED (O) 2. Alt 1: LS_PWR (O) 3. SW GPIO (B)
GPIO_29	Y2	B10	General purpose I/O 29: Options: 1. Alt 0: PWM_OUT_UVLED (O) 2. Alt 1: CW_INDEX_1 (I) 3. SW GPIO (B)
GPIO_30	AA3	B11	General purpose I/O 30: Options: 1. Alt 0: HBT_CLKOUT (O) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_31	AB4	B10	General purpose I/O 31: Options: 1. Alt 0: HBT_DO (O) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_32	AC1	B10	General purpose I/O 32: Options: 1. Alt 0: HBT_CLKIN_0 (I) 2. Alt 1: N/A 3. SW GPIO (B)

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5.9 GPIO Peripheral Interface (continued)

PIN		I/O [1]	DESCRIPTION [2] [3] [4]
NAME	NO.		
GPIO_33	AB2	B10	General purpose I/O 33: Options: 1. Alt 0: HBT_DI_0 (I) 2. Alt 1:N/A 3. SW GPIO (B)
GPIO_34	AC3	B9	General purpose I/O 34: Options: 1. Alt 0: HBT_CLKIN_1 (I) 2. Alt 1: GP_CLK2 (O) 3. SW GPIO (B)
GPIO_35	AD4	B10	General purpose I/O 35: Options: 1. Alt 0: HBT_DI_1 (I) 2. Alt 1: CAL_PWR(O) 3. SW GPIO (B)
GPIO_36	AE1	B10	General purpose I/O 36: Options: 1. Alt 0: HBT_CLKIN_2 (I) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_37	AD2	B10	General purpose I/O 37: Options: 1. Alt 0: HBT_DI_2 (I) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_38	AE3	B10	General purpose I/O 38: Options: 1. Alt 0: EFSYNC (O)/DASYNC(I) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_39	AG1	B10	General purpose I/O 39: Options: 1. Alt 0: SEQ_SYNC (B - Open Drain) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_40	AF4	B10	General purpose I/O 40: Options: 1. Alt 0: AWC0_DACCLK_0_1 (O) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_41	AF2	B11	General purpose I/O 41: Options: 1. Alt 0: AWC0_DACCLK_0_1 (O) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_42	AJ1	B10	General purpose I/O 42: Options: 1. Alt 0: AWC0_DACS_PWMA_0 (O) 2. Alt 1: N/A 3. SW GPIO (B)
GPIO_43	AG3	B10	General purpose I/O 43: Options: 1. Alt 0: AWC0_DACD_PWMB_0 (O) 2. Alt 1: PWM_OUT_BLED_2 (O) 3. SW GPIO (B)

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5.9 GPIO Peripheral Interface (continued)

PIN		I/O [1]	DESCRIPTION [2] [3] [4]
NAME	NO.		
GPIO_44	AH2	B10	General purpose I/O 44: Options: 1. Alt 0: AWC0_DACS_PWMA_1 (O) 2. Alt 1: PAUX_INT0 (O) 3. SW GPIO (B)
GPIO_45	AJ3	B10	General purpose I/O 45: Options: 1. Alt 0: AWC0_DACD_PWMB_1 (O) 2. Alt 1: PAUX_INT1 (O) 3. SW GPIO (B)
GPIO_46	AL1	B10	General purpose I/O 46: Options: 1. Alt 0: N/A 2. Alt 1: PAUX_INT2 (O) 3. SW GPIO (B)
GPIO_47	AK4	B11	General purpose I/O 47: Options: 1. Alt 0: AWC1_DACCLK_0_1 (O) 2. Alt 1: PAUX_INT3 (O) 3. SW GPIO (B)
GPIO_48	AK2	B10	General purpose I/O 48: Options: 1. Alt 0: AWC1_DACS_PWMA_0 (O) 2. Alt 1: SF_SEL_0 (O) 3. SW GPIO (B)
GPIO_49	AN1	B10	General purpose I/O 49: Options: 1. Alt 0: AWC1_DACD_PWMB_0 (O) 2. Alt 1: SF_SEL_1 (O) 3. SW GPIO (B)
GPIO_50	AL3	B10	General purpose I/O 50: Options: 1. Alt 0: AWC1_DACS_PWMA_1 (O) 2. Alt 1: SF_SEL_2 (O) 3. SW GPIO (B)
GPIO_51	AM2	B10	General purpose I/O 51: Options: 1. Alt 0: AWC1_DACD_PWMB_1 (O) 2. Alt 1: SF_SEL_3 (O) 3. SW GPIO (B)

(1) See Section 5.12 for more information on I/O definitions.
(2) This table defines the GPIO capabilities of the controller. Please see *GPIO functionality* for specific product configuration allocations of these GPIOs.
(3) Most GPIO has at least one alternate hardware functional use in addition to being available as a general purpose I/O. Depending on the product configuration, GPIO may be reserved specifically for use as an alternate hardware function (and would therefore not be available as a general purpose I/O). More information on GPIO allocations for specific product configurations can be found in *GPIO functionality*.
(4) All GPIOs that are available as a general purpose I/O must be configured as an input, a standard output, or an open-drain output. This is set in the flash configuration. Configure unused GPIO as a logic zero output and leave unconnected; otherwise, an external pullup or pulldown resistor is required to avoid a floating input. The reset default for all GPIO is as an input signal. An external pullup resistor (≤ 10kΩ) is required for each signal configured as open-drain output.

5.10 Clock and PLL Support

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
REFCLK_I	N1	I8	Crystal Input: Reference clock crystal input[2] [3]

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5.10 Clock and PLL Support (continued)

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
REFCLK_O	L1	O8	Crystal Output: Reference clock crystal output[2] [5]
OCLKA	AB24	O14	General Purpose Output Clock A [4] Targeted for driving the Color Wheel motor controller. Frequency is software programmable, with a power-up default frequency of 0.99 MHz. Note: the output frequency is not affected by non-power-up reset operations (that is, the system holds the last programmed value until the system is power cycled).

(1) See I/O Table for more information on I/O definitions.
(2) For more information on this signal, see System Oscillator Timing.
(3) For applications where an external oscillator is used in place of a crystal, use an oscillator to drive this pin.
(4) For more information on this signal, see Programmable Output Clock Timing.
(5) For applications where an external oscillator is used in place of a crystal, this pin should be grounded.

5.11 Power and Ground

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
VDDA18_PLLM	AL11	PWR	1.8V (Nominal) for the Main I/F PLL
VDDA18_PLLD	J13	PWR	1.8V (Nominal) for the DMD I/F PLL
VDD_CORE	AA13, AA15, AA21, AB16, AC13, AD6, AD8, AD18, AD20, AE9, AE11, AF14, AF16, AF20, AG7, AH6, AJ11, AL9, AL13, AL17, AL19, K8, K18, L9, L13, M6, M20, N15, N17, T6, T12, T14, T20, U19, V8, V10, Y6, Y20	PWR	
VDDAR_CORE	AB10, AB12, AJ9, AJ13, AJ15, AJ17, AJ19, AK8, N11, N13, P8, P18, R9, R19, W15, W17	PWR	
VDDA_CORE_DSI	AR7	PWR	
VDDA_CORE_FPD	AM16, AM18, AM20	PWR	0.8V (Nominal) Fixed Power for FPD core
VDDA_CORE_USB	AM6	PWR	0.8V (Nominal) for USB Controller
VDDA_CORE_Vx1	AM10, AM14	PWR	0.8V (Nominal) Fixed Power for Vx1 core
VDDA18_DDI	J7, J9, J11, J15, J17, J19	PWR	1.8V (Nominal) Fixed IO Power for SubLVDS DMD Interface
VDDA18_DSI	AP8	PWR	1.8V (Nominal) for DSI
VDDA18_FPD	AN15, AP16, AP18, AR19	PWR	1.8V (Nominal) Fixed Power for FPD I/O
VDDA18_USB	AN7	PWR	1.8V (Nominal) for USB Phy
VDDA18_Vx1	AM12, AP10, AP14	PWR	1.8V (Nominal) Fixed Power for Vx1 I/O
VDDA33_USB	AP6	PWR	3.3V (Nominal) for USB Phy
VDDS18_LVCMOS1	AA5, AE5, AG5, AL5, W5		
VDDS18_LVCMOS2	N21, R21, U21, W21		
VDDS18_OSC	U5	PWR	1.8V (Nominal) Fixed Power for Reference Oscillator I/O
VDDSHV_FLSH	AC21, AE21	PWR	1.8V or 3.3V (Nominal) Multi-Voltage IO Power for the Quad-Serial Flash Interface

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5.11 Power and Ground (continued)

PIN		I/O [1]	DESCRIPTION
NAME	NO.		
VDDSHV_INTF	AG21, AL21	PWR	1.8V or 3.3V (Nominal) Multi-Voltage IO Power for SPI and I^2C I/O (including GPIO[8:0]) to support the PAD1000 in place of a PMIC I/O. Also HOST_IRQ
VSS	A1, A9, A23, A25, AA7, AA9, AA17, AA19, AB6, AB8, AB14, AB18, AB20, AC5, AC9, AC11, AC15, AC17, AD12, AD14, AD16, AE13, AE17, AF6, AF8, AF12, AF18, AG9, AG11, AG13, AG17, AG19, AH10, AH14, AH16, AH20, AK6, AK16, AK20, AL7, AL15, AM8, AN5, AN9, AN21, AP12, AP20, AR5, AR9, AR11, AR13, AR15, AR17, AR21, AT4, AT6, AT8, AT10, AT12, AT14, AT18, AT22, AU3, AU7, AU23, AV2, AV10, AV14, AW7, AW19, AY2, AY14, AY24, B16, BA1, BA7, BA19, BA25, BB2, BB14, BB24, C9, C23, D2, D16, G5, G7, G9, G11, G15, G17, G19, G21, H6, H8, H10, H12, H14, H16, H18, H20, J5, J21, K6, K10, K16, K20, L5, L7, L11, L15, L17, M2, M10, M14, M18 , N5, N7, P10, P12, P14, P20, R5, R11, R15, R17, T8, T10, T16, U7, U11, U15, U17, V6, V12, V14, V20, W7, W13, W19, Y8, Y10, Y12, Y14, Y18	RTN	Ground, at package level all grounds tie to VSS
VPP	L21	RTN	Manufacturing use only (efuse). Must be tied to ground

(1) See Section 5.12 for more information on I/O definitions.

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5.12 I/O Type Subscript Definition

I/O			
SUBSCRIPT	**DESCRIPTION**	**SUPPLY REFERENCE**	**ESD STRUCTURE**
1	LVCMOS 1.8V Only	VDDS18_LVCMOS1	ESD diode to supply rail and GND
2	LVCMOS 1.8V Only	VDDS18_LVCMOS2	ESD diode to supply rail and GND
3	LVCMOS 1.8/3.3V	VDDSHV_INTF	ESD diode to supply rail and GND
4	Differential FPD LVDS	VDDA18_FPD	ESD diode to supply rail and GND
5	Differential V-by-One	VDDA18_VX1	ESD diode to supply rail and GND
6	Differential DSI	VDDA18_DSI	ESD diode to supply rail and GND
7	USB 2.0	VDDA18_USB, VDDA33_USB	ESD diode to supply rail and GND
8	Reference Oscillator Input	VDDS18_OSC	ESD diode to supply rail and GND
9	LVCMOS 1.8V Only 6.5mA	VDDS18_LVCMOS1	ESD diode to supply rail and GND
10	LVCMOS 1.8V Only 8mA	VDDS18_LVCMOS1	ESD diode to supply rail and GND
11	LVCMOS 1.8V Only 12mA	VDDS18_LVCMOS1	ESD diode to supply rail and GND
12	LVCMOS 1.8V Only 24mA	VDDS18_LVCMOS1	ESD diode to supply rail and GND
13	LVCMOS 1.8V Only 6.5mA	VDDS18_LVCMOS2	ESD diode to supply rail and GND
14	LVCMOS 1.8V Only 8mA	VDDS18_LVCMOS2	ESD diode to supply rail and GND
15	Differential SubLVDS 1.8V	VDDA18_DDI	ESD diode to supply rail and GND
16	LVCMOS 1.8/3.3V 8mA	VDDSHV_FLSH	ESD diode to supply rail and GND
17	LVCMOS 1.8/3.3V 7.5mA	VDDSHV_INTF	ESD diode to supply rail and GND
18	i^2c 1.8/3.3V3mA@3.3V	VDDSHV_INTF	ESD diode to supply rail and GND
TYPE			
I	Input	N/A	
O	Output		
B	Bidirectional		
PWR	Power		
RTN	Ground return		

5.13 Internal Pullup and Pulldown Characteristics

INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS(1)	CONDITIONS	MIN	MAX	UNIT
Weak pullup resistance - FLSH_CSZ	VDD_FLSH = 3.3V	42	59	kΩ
Weak pullup resistance - SSP0_CSZ_0	VDD_INTF = 3.3V	18	26	kΩ
Weak pullup resistance - JTAGTRSTZ, JTAGTDI, JTAGTMS1, JTAGTMS2,	VDD18 = 1.8V	31	84	kΩ
Weak pulldown resistance - JTAGTCK, HWTEST_EN, TSTPT_0, TSTPT_1, TSTPT_2, TSTPT_3, TSTPT_4, TSTPT_5, TSTPT_6, TSTPT_7, GPTP0, GPTP1, GPTP2	VDD18 = 1.8V	31	71	kΩ

(1) An external 5.7kΩ or less pullup or pulldown resistor (if needed) is sufficient for any voltage condition to correctly override any associated internal pullup or pulldown resistance.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

Parameter		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE(2)					
VDD_CORE	0.8V (Nominal) for core logic	–0.3		1.05	V
VDDAR_CORE	SRAM core (0.8V nominal)	–0.3		1.05	V
VDDS18_LVCMOS1	1.8V (Nominal) Fixed IO Power, left side	–0.3		2.2	V
VDDS18_LVCMOS2	1.8V (Nominal) Fixed IO Power, right side	–0.3		2.2	V
VDDA_CORE_DSI	0.8V (Nominal) for DSI	–0.3		1.05	V
VDDA18_DSI	1.8V (Nominal) for DSI	–0.3		2.2	V
VDDA_CORE_FPD	0.8V (Nominal) Fixed Power for FPD core	–0.3		1.05	V
VDDA18_FPD	1.8V (Nominal) Fixed Power for FPD I/O	–0.3		2.2	V
VDDA_CORE_Vx1	0.8V (Nominal) Fixed Power for Vx1 core	–0.3		1.05	V
VDDA18_Vx1	1.8V (Nominal) Fixed Power for Vx1 I/O	–0.3		2.2	V
VDDA_CORE_USB	0.8V (Nominal) for USB Controller	–0.3		1.05	V
VDDA18_USB	1.8V (Nominal) for USB Phy	–0.3		2.2	V
VDDA33_USB	3.3V (Nominal) for USB Phy	–0.3		3.6	V
VDDSHV_INTF	1.8V or 3.3V (Nominal) Multi-Voltage IO Power for SPI and I^2C I/O (including GPIO[8:0]) to support the PAD1000 in place of a PMIC I/O. Also HOST_IRQ.	–0.3		3.8	V
VDDSHV_FLSH	1.8V or 3.3V (Nominal) Multi-Voltage IO Power for the Quad-Serial Flash Interface	–0.3		3.8	V
VDDA18_DDI	1.8V (Nominal) Fixed IO Power for SubLVDS DMD Interface	–0.3		2.2	V
VDDS18_OSC	1.8V (Nominal) Fixed Power for Reference Oscillator I/O	–0.3		2.2	V
VDDA18_PLLM	1.8V (Nominal) for the Main I/F PLL	–0.3		2.2	V
VDDA18_PLLD	1.8V (Nominal) for the DMD I/F PLL	–0.3		2.2	V
LDO INTF					
CAP_VDDS_INTF	External Capacitor for 3.3V/1.8V Dual-voltage Interface I/O		1.8	1.98	V
CAP_VDDS_FLSH	External Capacitor for3.3V/1.8V Dual-voltage Flash I/O				
GENERAL					
T_J	Operating junction temperature	–30		115	°C
T_C	Operating case temperature	–30		105	°C
Transient Overshoot and Undershoot at IO pin	20% of IO supply voltage for up to 20% of the signal period (see Figure 6-1, IO Transient Voltage Ranges).			0.2×VDD	V
T_{stg}	Storage temperature range	–40		125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to GND.

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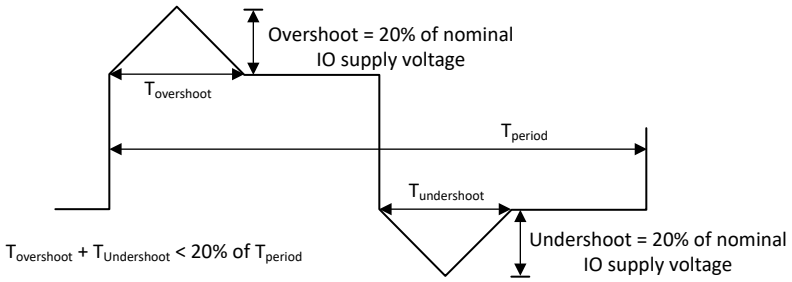

Figure 6-1. IO Transient Voltage Ranges

6.2 ESD Ratings

ANSI/ESDA/JEDEC JS-002

Parameter			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

PARAMETER		TOLERANCE	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VDD_CORE	0.8V (Nominal) for core logic		0.76	0.8	0.84	V
VDDAR_CORE	SRAM core (0.8V nominal)		0.76	0.8	0.84	V
VDDS18_LVCMOS1	1.8V (Nominal) Fixed IO Power, left side		1.647	1.8	1.953	V
VDDS18_LVCMOS2	1.8V (Nominal) Fixed IO Power, right side		1.647	1.8	1.953	V
VDDA_CORE_DSI	0.8V (Nominal) for DSI		0.76	0.8	0.84	V
VDDA18_DSI	1.8V (Nominal) for DSI		1.647	1.8	1.953	V
VDDA_CORE_FPD	0.8V (Nominal) Fixed Power for FPD core		0.76	0.8	0.84	V
VDDA18_FPD	1.8V (Nominal) Fixed Power for FPD I/O		1.647	1.8	1.953	V
VDDA_CORE_Vx1	0.8V (Nominal) Fixed Power for Vx1 core		0.76	0.8	0.84	V
VDDA18_Vx1	1.8V (Nominal) Fixed Power for Vx1 I/O		1.647	1.8	1.953	V
VDDA_CORE_USB	0.8V (Nominal) for USB Controller		0.76	0.8	0.84	V
VDDA18_USB	1.8V (Nominal) for USB Phy		1.647	1.8	1.953	V
VDDA33_USB	3.3V (Nominal) for USB Phy		3.02	3.3	3.52	V
VDDSHV_INTF	1.8V or 3.3V (Nominal) Multi-Voltage IO Power for SPI and I^2C I/O (including GPIO[8:0]) to support the PAD1000 in place of a PMIC I/O. Also HOST_IRQ.		1.647	1.8	1.953	V
VDDSHV_INTF	3.3V operation		3.02	3.3	3.52	V
VDDSHV_FLSH	1.8V or 3.3V (Nominal) Multi-Voltage IO Power for the Quad-Serial Flash Interface		1.647	1.8	1.953	V
VDDSHV_FLSH	3.3V operation		3.02	3.3	3.52	V
VDDA18_DDI	1.8V (Nominal) Fixed IO Power for SubLVDS DMD Interface		1.647	1.8	1.953	V
VDDS18_OSC	1.8V (Nominal) Fixed Power for Reference Oscillator I/O		1.647	1.8	1.953	V
VDDA18_PLLM	1.8V (Nominal) for the Main I/F PLL		1.647	1.8	1.953	V
VDDA18_PLLD	1.8V (Nominal) for the DMD I/F PLL		1.647	1.8	1.953	V

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6.3 Recommended Operating Conditions (continued)

PARAMETER		TOLERANCE	MIN	TYP	MAX	UNIT
GENERAL						
T_J	Operating junction temperature		–30		115	°C
T_C	Operating case temperature		–30		94	°C
T_A	Operating ambient temperature (1) (2)		–30		85	°C

(1) The operating ambient temperature range values were determined based on the board design parameters described in the General Layout Guidelines, rather than using a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage, and temperature. Ambient thermal conditions, which impact $R_{\theta JA}$, vary by application. Thus, maximum operating ambient temperature varies by application. $T_{a_min} = T_{j_min} – (P_{d_min} \times R_{\theta JA}) = 0°C – (host_min_valueW \times host_value°C/W) = – host_value°C/W) = -host_calculated_value°C$. $T_{a_max} = T_{j_max} – (P_{d_max} \times R_{\theta JA}) = +115°C – (host_max_valueW \times host_value°C/W) = +host_calculated_value°C$

(2) Operating ambient temperature is dependent on system thermal design. Operating case temperature may not exceed its specified range across ambient temperature conditions.

6.4 Thermal Information

THERMAL METRIC (1)		TEST CONDITIONS	FCCSP 484 PINS	UNIT
R_{JC}	Junction-to-case thermal resistance		3.3	°C/W
$R_{\theta JA}$	Junction-to-air thermal resistance	at 0m/s of forced airflow(2)	19.5	°C/W
		at 1m/s of forced airflow(2)	12.9	
		at 2m/s of forced airflow(2)	11.8	
ψ_{JT}	Temperature variance from junction to package top center temperature, per unit power dissipation		0.04	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC-defined standard test PCB. This JEDEC test PCB is not necessarily representative of the controller PCB, and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.

6.5 Power Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		Test Conditions	MIN	TYP	MAX	UNIT
DLPC8424						
$V_{(Supply08)}$	0.8V DVH Supply	Core Supply		524		mA
$V_{(Supply18)}$	1.8V DVH Supply	IO Supply, VbyOne, SubLVDS, GPIO		80		mA
$V_{(Supply33)}$	3.3V DVH Supply	USB Supply		1		mA
DLPC8444						
$V_{(Supply08)}$	0.8V DVH Supply	Core Supply		641		mA
$V_{(Supply18)}$	1.8V DVH Supply	IO Supply, VbyOne, SubLVDS, GPIO		212		mA
$V_{(Supply33)}$	3.3V DVH Supply	USB Supply		1		mA

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6.6 Pin Electrical Characteristics

PARAMETER		IO Type	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	9	LVCMOS 1.8V only / 6.5mA	1.26	1.8	1.98	V
		10	LVCMOS 1.8V only / 8mA	1.26	1.8	1.98	V
		11	LVCMOS 1.8V only / 12mA	1.26	1.8	1.98	V
		17	LVCMOS (1.8 or 3.3V) / 7.5mA	1.26	1.8	1.98	V
		16	LVCMOS (1.8 or 3.3V) / 8mA	1.26	1.8	1.98	V
V_{IL}	Low-level input threshold voltage	9	LVCMOS 1.8V only / 6.5mA	-0.3		0.58	V
		10	LVCMOS 1.8V only / 8mA	-0.3		0.58	V
		11	LVCMOS 1.8V only / 12mA	-0.3		0.58	V
		17	LVCMOS (1.8 or 3.3V) / 7.5mA	-0.3		0.49	V
		16	LVCMOS (1.8 or 3.3V) / 8mA	-0.3		0.49	V
V_{OH}	High-level output threshold voltage	9	LVCMOS 1.8V only / 6.5mA	1.35			V
		10	LVCMOS 1.8V only / 8mA	1.35			V
		11	LVCMOS 1.8V only / 12mA	1.35			V
		12	LVCMOS 1.8V only / 24mA	1.35			V
		17	LVCMOS (1.8 or 3.3V) / 7.5mA	1.35			V
		16	LVCMOS (1.8 or 3.3V) / 8mA	1.35			V
V_{OL}	Low-level output threshold voltage	9	LVCMOS 1.8V only / 6.5mA			0.45	V
		10	LVCMOS 1.8V only / 8mA			0.45	V
		11	LVCMOS 1.8V only / 12mA			0.45	V
		12	LVCMOS 1.8V only / 24mA			0.45	V
		17	LVCMOS (1.8 or 3.3V) / 7.5mA			0.45	V
		16	LVCMOS (1.8 or 3.3V) / 8mA			0.45	V
		18	I^2C Cell 1.8V/3.3V - 3mA @3.3V			0.4	V
I_{IH}	High-level input current	9	LVCMOS 1.8V only / 6.5mA			10	µA
		10	LVCMOS 1.8V only / 8mA			10	µA
		11	LVCMOS 1.8V only / 12mA			10	µA
		17	LVCMOS (1.8 or 3.3V) / 7.5mA			10	µA
		16	LVCMOS (1.8 or 3.3V) / 8mA			10	µA
		18	I^2C Cell 1.8V/3.3V - 3mA @3.3V			10	µA
I_{IL}	Low-level input current	9	LVCMOS 1.8V only / 6.5mA	-10			µA
		10	LVCMOS 1.8V only / 8mA	-10			µA
		11	LVCMOS 1.8V only / 12mA	-10			µA
		17	LVCMOS (1.8 or 3.3V) / 7.5mA	-10			µA
		16	LVCMOS (1.8 or 3.3V) / 8mA	-10			µA
		18	I^2C Cell 1.8V/3.3V - 3mA @3.3V	-10			µA
I_{OH}	High-level output current	9	LVCMOS 1.8V only / 6.5mA			6.5	mA
		10	LVCMOS 1.8V only / 8mA			8	mA
		11	LVCMOS 1.8V only / 12mA			12	mA
		17	LVCMOS (1.8 or 3.3V) / 7.5mA			6	mA
		16	LVCMOS (1.8 or 3.3V) / 8mA			8	mA
		18	I^2C Cell 1.8V/3.3V - 3mA @3.3V			3	mA

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6.6 Pin Electrical Characteristics (continued)

PARAMETER		IO Type	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current	9	LVCMOS 1.8V only / 6.5mA			6.5	mA
		10	LVCMOS 1.8V only / 8mA			8	mA
		11	LVCMOS 1.8V only / 12mA			12	mA
		17	LVCMOS (1.8 or 3.3V) / 7.5mA			6	mA
		16	LVCMOS (1.8 or 3.3V) / 8mA			8	mA
		18	I^2C Cell 1.8V/3.3V - 3mA @3.3V			3	mA

6.7 DMD SubLVDS Interface Electrical Characteristics

Operating over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CM}	Steady State Common mode voltage		0.8	0.9	1	V
V_{CM} (Δp.p)	V_{CM} Change peak-to-peak				75	mV
V_{CM} (Δss)	V_{CM} Change steady state		–10		10	mV
$\|V_{OD}\|$	Differential output voltage magnitude		170	250	350	mV
V_{OD} (Δ)	V_{OD} change (between logic states)		–10		10	mV
V_{OH}	Single-ended output voltage high		0.825	1.025	1.175	V
V_{OL}	Single-ended output voltage low		0.625	0.775	0.975	V
Tx_{term}	Internal differential termination		80	100	120	Ω
Tx_{load}	100Ω differential PCB trace (50Ω transmission lines)		0.25		10	inches

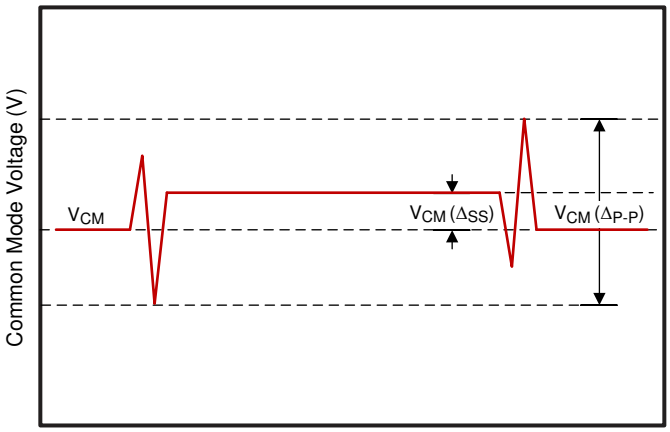

Figure 6-2. Common Mode Voltage

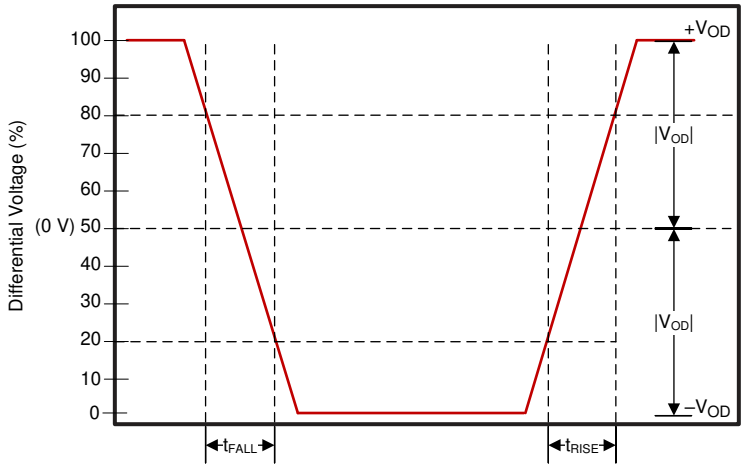

Figure 6-3. Differential Output Signal

6.8 DMD Low-Speed Interface Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tx_{load}	100Ω differential PCB trace (50Ω transmission lines)				10	inches
$V_{OH(DC)}$	DC Single-ended output voltage high	0.7 × VDDS18_LVCMOSX	1.35			V
$V_{OL(DC)}$	DC single-ended output voltage low	0.3 × VDDS18_LVCMOSX			0.45	V
$V_{OH(AC)}$ (1)	AC single-ended output voltage high		1.1			V
$V_{OL(AC)}$ (2)	AC single-ended output voltage low	–0.5, 0.2 × VDDS18_LVCMOSX			0.6	V

(1) $V_{OH(AC)}$ maximum applies to overshoot. When the DMD_LSX_WDATA and DMD_LSX_CLK lines include a proper 43Ω series termination resistor, the DMD operates within the LPSDR input AC specifications.
(2) $V_{OH(AC)}$ minimum applies to undershoot. When the DMD_LS_WDATA and DMD_LS_CLK lines include a proper 43Ω series termination resistor, the DMD operates within the LPSDR input AC specifications.

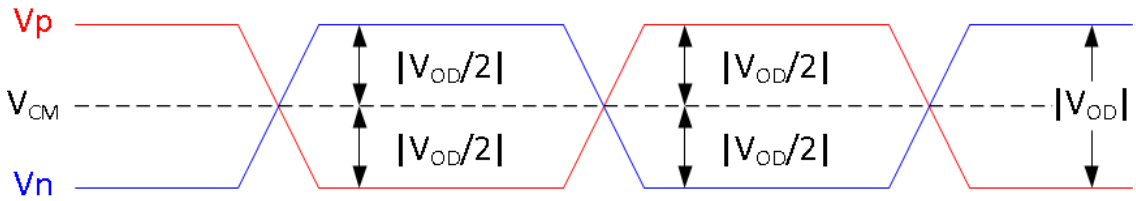

Figure 6-4. DMD Low-Speed Differential Voltage Parameters

6.9 V-by-One Interface Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)		MIN	NOM	MAX	UNIT
V_{DIFF}	Input peak-to-peak differential	2 × V_{ID}			mVppd
$\|V_{ID}\|$	Differential input voltage	50			mV
Rx_{term}	Internal differential termination	80	100	120	Ω

(1) See the V-by-One interface standard for more information.

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6.10 FPD Link LVDS Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)	PARAMETER(1)	MIN	NOM	MAX	UNIT
V_{DIFF}	Input peak-to-peak differential fail-safe (open circuit) mode disabled	200		1200	mVppd
	Input peak-to-peak differential fail-safe (open circuit) mode enabled	200		908	
$\|V_{ID}\|$	Differential input voltage fail-safe (open circuit) mode disabled	100		600	mV
	Differential input voltage fail-safe (open circuit) mode enabled	100		454	
V_{CM}	Steady-state common mode voltage(2) fail-safe (open circuit) mode disabled	0.3	1.25	1.45	V
	Steady-state common mode voltage(2) fail-safe (open circuit) mode enabled	0.3	1.25	1.45	
Rx_{term}	Internal differential termination	80	100	120	Ω

(1) See FPD-Link Interface.
(2) If V_{CM} falls below $V_{CM(min)}$ at the inputs to the receiver, an open input detection circuit is automatically enabled. This detection circuit disables the receiver until the input V_{CM} rises above $V_{CM(min)}$.

6.11 USB Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)			MIN	NOM	MAX	UNIT
Low-Speed and Full Speed (Input Level)						
V_{IH}	Single-ended input voltage high (driven)		2			V
V_{IL}	Single-ended input voltage low				0.8	V
V_{DI}	Differential input sensitivity	|(DP) - (DM)|	0.2			V
V_{CM}	Differential common mode voltage	Includes V_{DI} range	-50		500	mV
Low-Speed and Full Speed (Output Level)						
V_{OL}	Low-level output voltage	with 1.425kΩ pullup to 3.6V	0		0.3	V
V_{OH}	High-level output voltage	with 14.25kΩ pulldown	2.8		3.6	V
High-Speed (Input Level)						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)		100		150	mV
High-Speed (Output Level)						
Termination						
R_{PU}	Bus pullup resistor		1.425		1.575	KΩ
R_{PD}	Bus pulldown resistor		14.25		15.75	KΩ
Z_{HSDRV}	High-speed driver output impedance		40.5		49.5	Ω

(1) Referenced to VDDA33_USB.

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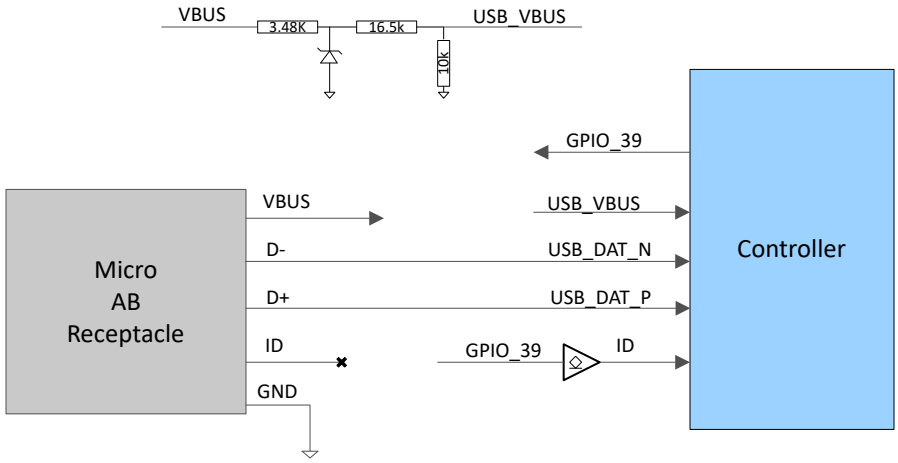

Figure 6-5. USB Example for the DLPC84x4 Controller

6.12 System Oscillator Timing Requirements

PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, REFCLK(1) (2)	PLL: 40MHz	39.992	40.000	40.008	MHz
t_c	Cycle time, REFCLK(1)	PLL: 40MHz	24.995	25.000	25.005	ns
$t_{w(H)}$	Pulse duration(3), REFCLK, high	PLL: 40MHz 50% to 50% reference points (signal)	11.25			ns
$t_{w(L)}$	Pulse duration(3), REFCLK, low	PLL: 40MHz 50% to 50% reference points (signal)	11.25			ns

(1) The REFCLK inputs do not support spread-spectrum clock spreading.
(2) Multi-controller systems require that a single oscillator be used to drive the REFCLK input for all controllers in the system.
(3) Applies only when driven through an external digital oscillator. This is a 1-sigma RMS value.

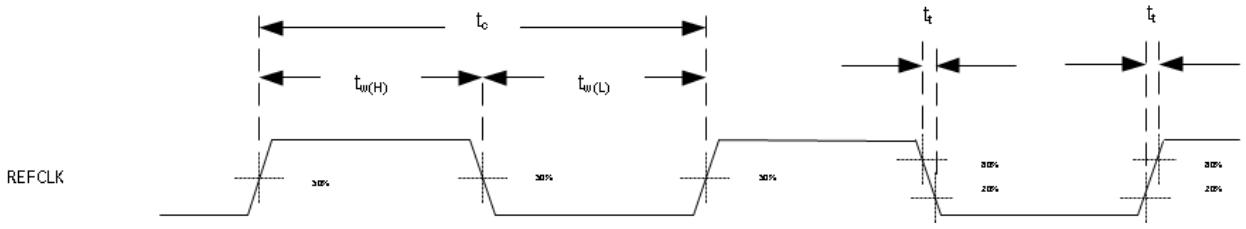

Figure 6-6. Common Mode Voltage

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6.13 Power Supply and Reset Timing Requirements

Over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{RAMP-UP}$	Power supply ramp-up time.(1)	Power supply ramp for each supply Ramp-up time: TOV × 10% to TOV × 90% TOV = Typical Operational Voltage		10	ms
			18		mv/µs
$t_{RAMP-UP-TOTAL}$	Total power supply ramp-up time.(1)	Total time within which the 0.8V, 1.8V, and 3.3V supplies must complete their ramp-up. Ramp-up time: TOV × 10% to TOV × 90% TOV = Typical Operational Voltage		100	ms
$t_{RAMP-DOWN}$	Power supply ramp-down time.(1)	Power supply ramp for each supply Ramp-down time: TOV × 90% to TOV × 10% TOV = Typical Operational Voltage	0		ms
t_{w1}	Pulse duration, in-active low, RESETZ	RESETZ inactive time 50% to 50% reference points (signal)	100		ms
t_{t1}	Transition time, RESETZ $t_{t1} = t_{f1}$ and t_{r1}	Rise and Fall time for RESETZ(2) 20% to 80% reference points (signal		25	µs
t_{PROJ_ON}	PROJ_ON fall time delay	PROJ_ON delay to fall time for any power supply ≤ 80%	10		ms
$t_{REFCLKA}$	Time to stable REFCLK(3)	Time to stable REFLCKA before POSENSE	1		ms

(1) It is assumed that all 0.8V supplies come from the same source, although some will have additional filtering before entering the Controller. As such, it is expected that these supplies will ramp together (aside from differences caused by filtering). This same expectation is true for the 1.8V and 3.3V supplies.
(2) As long as the noise on this signal is below the hysteresis threshold.
(3) This delay requirement parameter is defined by the design of the REFCLK oscillator and defines the minimum time required for the internal oscillator to lock after the power supplies have ramped up and a stable external reference is provided, and prior to the release of RESETZ.

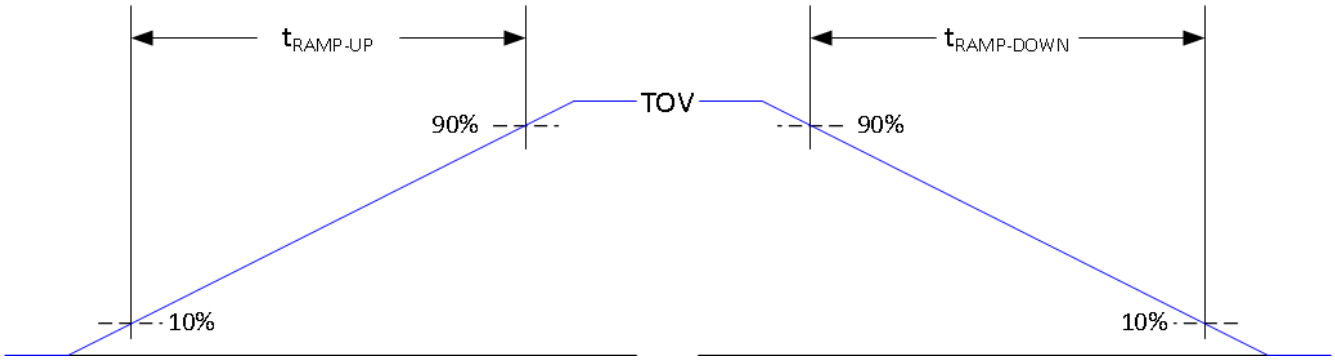

Figure 6-7. Power Supply Ramp Time

6.14 V-by-One Interface General Timing Requirements

PARAMETER[1]			MIN	MAX	UNIT
f_{clock}	Source clock frequency	1 lane to 8 lanes	20	600	MHz
$f_{link-clk}$	Link clock frequency per lane	8 lanes	43	75	MHz
		4 lanes	43	85	MHz
		2 lanes	43	85	MHz
		1 lane	43	85	MHz
f_{link}	Link transfer rate	3-Byte Mode	2	2.55	Gbps
		4 Byte Mode	2	3	Gbps
		5 Byte Mode	2	3	Gbps
tRBIT	Unit Interval	3-Byte Mode	392	500	ps
		4 Byte Mode	294	500	ps
		5 Byte Mode	294	500	ps
t_A	Jitter Margin[2]		0.25		UI
t_B	Rise / Fall Time[2]		0.05		UI
t_{EYE}	Differential Data Eye[2]	Differential Data Eye[2]	0.5		UI
t_{skew_intra}	Allowable Intrapair skew	Allowable Intrapair skew	0.3	5	UI
t_{skew_inter}	Allowable Interpair Skew	Allowable Interpair Skew		5	UI
T_j	Total jitter			0.5	UI
R_j	Random jitter	10^{12} UI		0.2	UI
D_j_ISI	Deterministic jitter (ISI)			0.2	UI
S_j	Sinusoidal jitter			0.1	UI

(1) V-by-One high-speed technology supports 1, 2, 4, or 8-lane operation, in addition to 3-byte, 4-byte, and 5-byte transfer modes
(2) See V-by-One Timing.

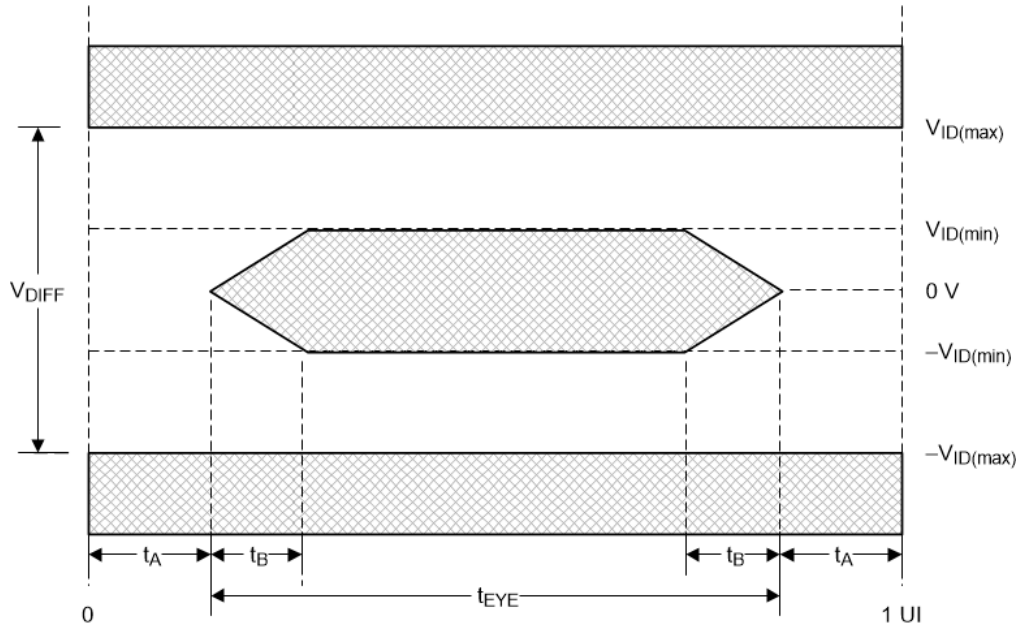

Figure 6-8. V-by-One Timing

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6.15 FPD Link Interface General Timing Requirements

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, FPDA_CLK_P/N, FPDB_CLK_P/N	1 port	10	160	MHz
t_{clock}	Clock period, FPDA_CLK_P/N, FPDB_CLK_P/N		6.25	100	ns
t_{RBIT}	Unit Interval	1 Port		7.143	ps
		Per Port	0.865		ps
t_{skew_ports}	Clock-to-clock skew margin between ports on same Controller, and between ports on different Controllers			1	clock
t_A	Jitter Margin and Skew Margin between clock and data (on the same port)	$f_{clock} \leq$ 100MHz		0.2	UI
		$f_{clock} >$ 100MHz		0.15	UI
t_B	Rise/Fall Time			0.1	UI
t_{EYE}	Differential Data Eye			0.7	UI

6.16 Flash Interface Timing Requirements

PARAMETER			MIN	MAX	UNIT
f_{CLOCK}	FLSH_CLK frequency		0.586	60.0	MHz
t_{CLKPER}	FLSH_CLK period	50% reference points	16.66	1707	ns
t_{WH}	FLSH_CLK high pulse width	50% reference points	7.5		ns
t_{WL}	FLSH_CLK low pulse width	50% reference points	7.5		ns
t_{P_SU}	FLSH_DATA[3:0] Input Setup Time	before FLSH_CLK↓	7.2		ns
t_{P_H}	FLSH_DATA[3:0] Input Hold Time	after FLSH_CLK↓	0.0		ns

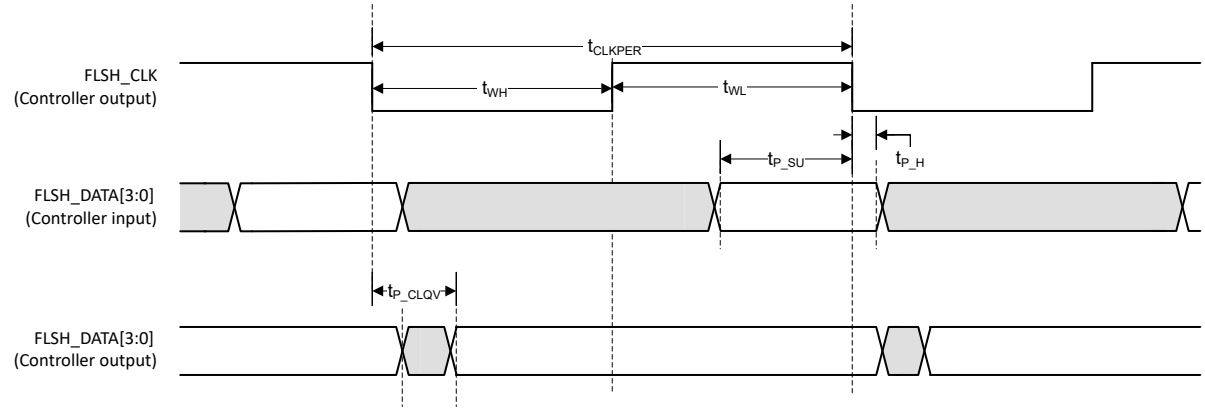

Figure 6-9. Flash Interface Timing

6.17 Source Frame Timing Requirements

PARAMETER (1) (7)			MIN	TYP	MAX	UNIT
t_{p_vsw}	VSYNC Active Pulse Width	50% reference points	1	10		lines
t_{p_vbp}	Vertical back porch (VBP)	50% reference points	2(2) (3)	72(2) (3)		lines
t_{p_vfp}	Vertical front porch (VFP)	50% reference points	1(2) (3)	8(2) (3)		lines
t_{p_tvb}	Total vertical blanking (TVB)	50% reference points	30(2) (3)	90(2) (3)		lines
t_{p_hsw}	HSYNC Active Pulse Width	50% reference points	3(4) (5)	88(4) (5)		PCLKs
t_{p_hbp}	Horizontal back porch (HBP)	50% reference points	4(4) (5)	296(4) (5)		PCLKs
t_{p_hfp}	Horizontal front porch (HFP)	50% reference points	7(4) (5)	176(4) (5)		PCLKs
t_{p_thb}	Total horizontal blanking (THB)(10)	50% reference points	80(4) (5)	560(4) (5)		PCLKs
APPL	Active Pixels per Line(8)		960(6) (9)	3840(6)	3840	Pixels
ALPF	Active Lines per Frame		540(6) (9)	2160(6)	2160	Lines

(1) The requirements in the table apply to all external sources of a 4K DLP display system.
(2) Total Vertical Blanking: The sum of VBP + VFP + VS.
(3) The vertical blanking required (per TVB) may be allocated as desired as long as the VFP and VBP minimum values are met.
(4) Total Horizontal Blanking: The sum of HBP + HFP + HS.
(5) The horizontal blanking required (per THB) may be allocated as desired as long as the HFP, HBP, and HS minimum values are met.
(6) To meet the min APPL and ALPF possible will require non-standard timing to keep the minimum pixel clock and blanking requirements. The defined minimum is based on a standard 720p input source as a reference for V-by-One. Other sources can support down to 540p.
(7) Video parameter limits set in compliance with the CVT 1.2 standard, including reduced blanking 4K 60Hz timing.
(8) The APPL must be a multiple of the incoming number of lanes (1, 2, 4, 8) when using V-by-One video input.
(9) V-by-One is only capable of supporting video sources down to 1280 × 720.
(10) The total horizontal blanking divided by the number of lanes used in the video source must be a whole number. If the blanking fluctuates by more than two pixels, the source will not lock.

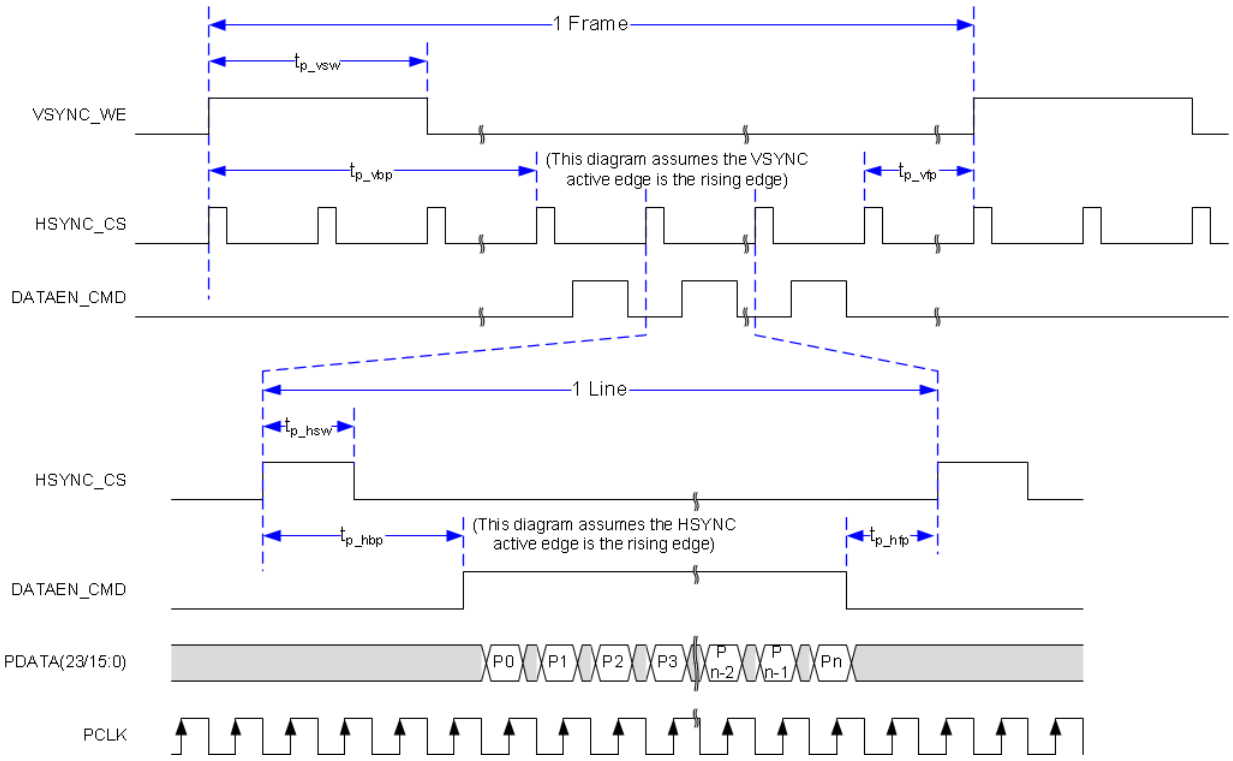

Figure 6-10. Source Frame Timing

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6.18 Synchronous Serial Port Interface Timing Requirements

PARAMETER			MIN	MAX	UNIT
SSP0 Host					
F_{CLK}	SSP*_CLK Frequency	Broadcast Write Transfers (1) (2)	0.457	75	MHz
		Full-Duplex SPI Transfers	0.457	50	MHz
T_{CLK}	SSP*_CLK Clock Period	Broadcast Write Transfers (1) (2)	13.33	2188	ns
		Full-Duplex SPI Transfers	20.00	2188	ns
t_{HPW}	SSP*_CLK high/low pulse width	Broadcast Write Transfers (1) (2)	6.0		ns
		Full-Duplex SPI Transfers	9.2		ns
t_{LPW}	SSP*_CLK high/low pulse width	Broadcast Write Transfers (1) (2)	6.0		ns
		Full-Duplex SPI Transfers	9.2		ns
t_S	SSP*_DI Input Setup Time	Before SSP*_CLK ↓ (Modes 0&3) (2)	9.4		ns
		Before SSP*_CLK ↑ (Modes 1&2)	9.4		ns
t_H	SSP*_DI Input Hold Time	Before SSP*_CLK ↓ (Modes 0&3) (2)	0		ns
		Before SSP*_CLK ↑ (Modes 1&2)	0		ns
t_{DOUT}	SSP*_DO Output Delay (2)	After SSP*_CLK ↓ (Modes 0&3)	–2.5	2.5	ns
		After SSP*_CLK ↑ (Modes 1&2)	–2.5	2.5	ns
		After SSP*_(B)CSZ ↓ (Modes 0&2)	–2.5	2.5	ns
		After SSP*_(B)CSZ ↑ (Modes 1&3)	–2.5	2.5	ns
SSP1 Target					
t_{CSZD}	SSP*_(B)CSZ* de-assertion (that is, high) time between SPI transfers (3)		13.33		ns
t_{CSS}	SSP*_(B)CSZ* Input Setup Time (4)	SSP*_(B)CSZ ↓ before SSP*_CLK ↑ (Modes 0&1)	6.0		ns
		SSP*_(B)CSZ ↓ before SSP*_CLK ↓ (Modes 2*3)	6.0		ns
t_{CSH}	SSP*_(B)CSZ* Input Setup Time (4)	SSP*_(B)CSZ ↑ after SSP*_CLK ↓ (Modes 0&1)	6.0		ns
		SSP*_(B)CSZ ↑ after SSP*_CLK ↑ (Modes 2*3)	6.0		ns
t_S	SSP*_DI Input Setup Time	Before SSP*_CLK↑ (Modes 0&3)	2.5		ns
		Before SSP*_CLK↓ (Modes 1&2)	2.5		
t_H	SSP*_DI Input Hold Time	Before SSP*_CLK↑ (Modes 0&3)	2.5		ns
		Before SSP*_CLK↓ (Modes 1&2)	2.5		ns
t_{DOUT}	SSP*_DO Output Delay	After SSP*_CLK↓ (Modes 0&3)	0	8.0	ns
		After SSP*_CLK↑ (Modes 1&2)	0	8.0	ns
		After SSP*_CSZ↓ (Modes 0&3)	0	8.0	ns
		After SSP*_CSZ↑ (Modes 1&2)	0	8.0	ns

(1) Broadcast Write transfers are half-duplex transfers in which the SSP host outputs SSP*_DO but does not receive any SSP*_DI input; hence, SSP*_DI input setup/hold timing checks are not applicable during Broadcast Write transfers.
(2) Applicable controller pins for SSP0 & SSP1 SPI interfaces are shown in Peripheral Interfaces.
(3) At least 1 SSP*_CLK period
(4) At least 0.5 SSP*_CLK period

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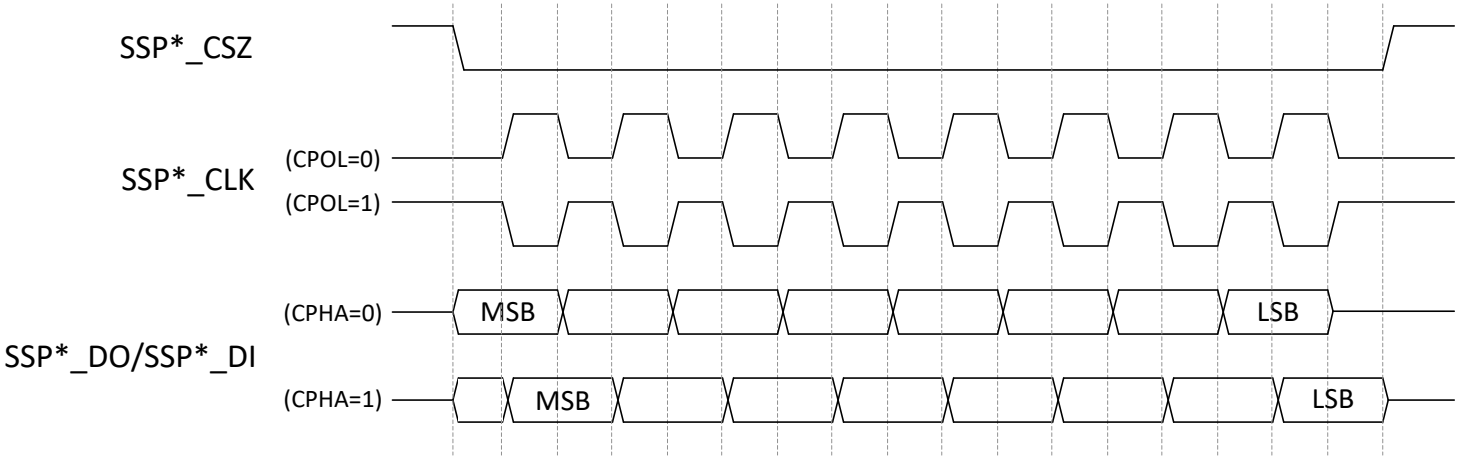

Figure 6-11. Timing Diagram for SPI Clocking Modes

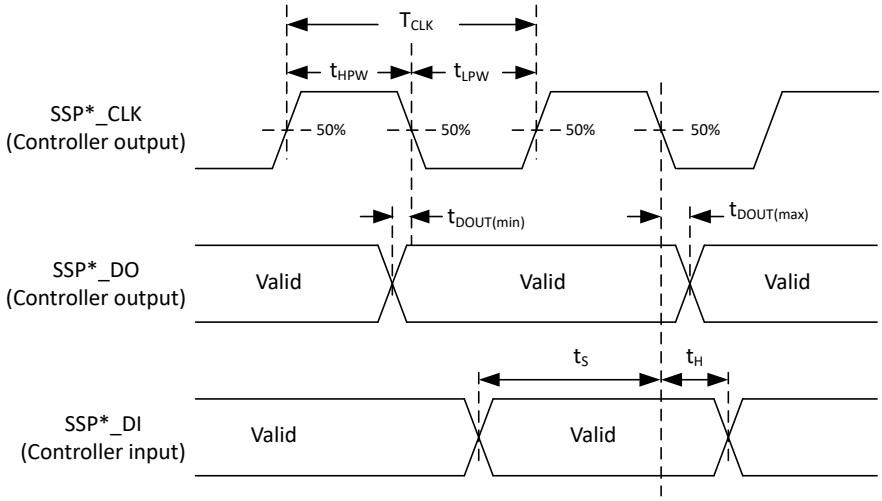

Figure 6-12. Timing Diagram for SSP Host Mode (Modes 0/3)

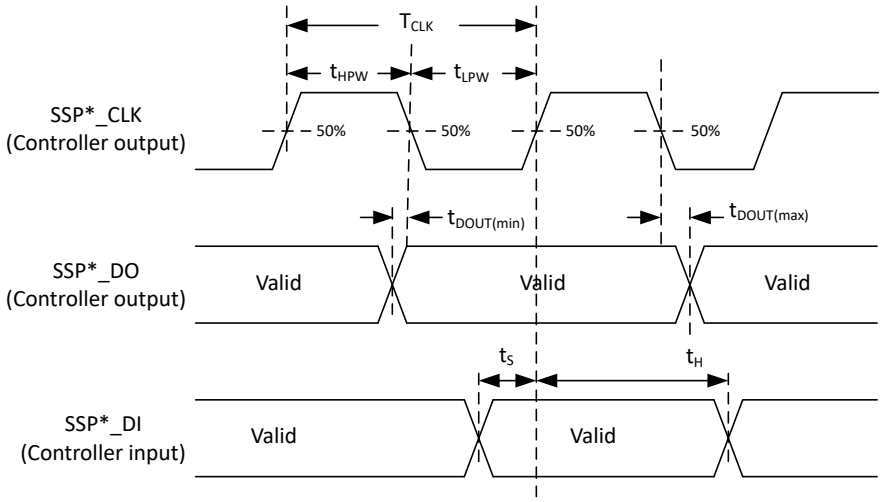

Figure 6-13. Timing Diagram for SSP Target Mode (Modes 0/3)

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6.19 I²C Interface Timing Requirements

PARAMETER (1)			MIN	MAX	UNIT
f_{clock}	Clock frequency, IICx_SCL (2) (50% reference points)	Full speed		400	kHz
		Standard mode		100	kHz
C_L	Capacitive Load (for each bus line)	Capacitive Load (for each bus line)		200	pF

(1) Meets all I²C timing per the I²C Bus Specification (except for capacitive loading as specified). For reference, see Version 2.1 of the Phillips-NXP specification.
(2) By definition, I²C transactions operate at the speed of the slowest device on the bus. Full Speed operation requires that all other I²C devices on the bus support Full Speed operation. The length of the line (due to its capacitance), as well as the value of the I²C pullup resistors, can reduce the obtainable clock rate.

6.20 Programmable Output Clock Timing Requirements

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, OCLKA (1)	0.987	42.86	MHz
t_{clock}	Clock period, OCLKA	23.33	1013.17	ns
$t_{w(H)}$	Pulse duration high, OCLKA (50% reference points)	$(t_{clock}/2) - 2$		ns
$t_{w(L)}$	Pulse duration low, OCLKA (50% reference points)	$(t_{clock}/2) - 2$		ns
$t_{cclkjit}$	Jitter, OCLKA		200	ps
f_{clock}	Clock frequency, OCLKB (2)	0.987	42.86	MHz
t_{clock}	Clock period, OCLKB	23.33	1013.17	ns
$t_{w(H)}$	Pulse duration high, OCLKB (50% reference points)	$(t_{clock}/2) - 2$		ns
$t_{w(L)}$	Pulse duration low, OCLKB (50% reference points)	$(t_{clock}/2) - 2$		ns
$t_{cclkjit}$	Jitter, OCLKB		200	ps

(1) OCLKA is on a dedicated output pin.
(2) OCLKB is an alternate function on GPIO_34.

6.21 JTAG Boundary Scan Interface Timing Requirements (Debug Only)

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK	Clock frequency, TCK		10	MHz
t_{clock}	Clock period, TCK		100		ns
$t_{w(H)}$	Pulse duration low, TCK	50% reference points	50		ns
$t_{w(L)}$	Pulse duration high, TCK	50% reference points	50		ns
t_s	Setup time – TDI, TMS1 valid before TCK↑	50% reference points	15		ns
t_h	Hold time – TDI, TMS1 valid after TCK↑	50% reference points	15		ns
tdelay	TDO2 Output delay after TCK↓	60pF load	0	15	ns

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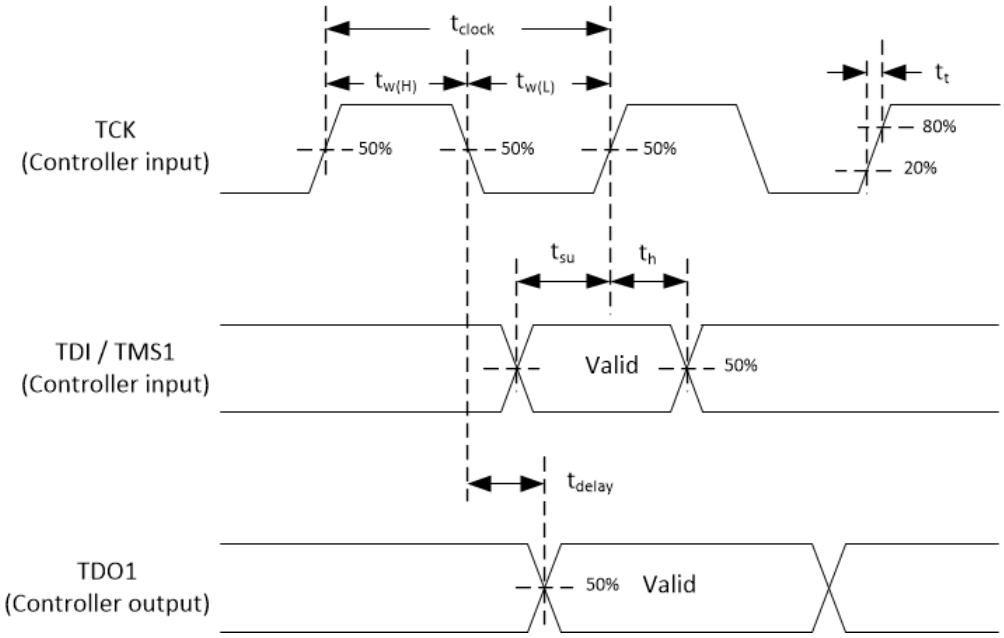

Figure 6-14. Timing Diagram for JTAG Boundary Scan

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6.22 DMD Low-Speed Interface Timing Requirements

PARAMETER			MIN	TYP	MAX	UNIT
DMD Low-Speed Interface (Single Ended)						
f_{clock}			119.966	120	120.034	MHz
Slew Rate	DMD_LS_WDATA and DMD_LS_CLK	VOL(DC) to VOH(AC) for rising edge and VOH(DC) to VOL(AC) for rising edge	1		3	V/ns
	DMD_DEN_ARSTZ	VOL(AC) to VOH(AC) for rising edge	0.25			
	DMD_LS_RDATAx		0.5			
DCD	Duty Cycle Distortion		45		55	%

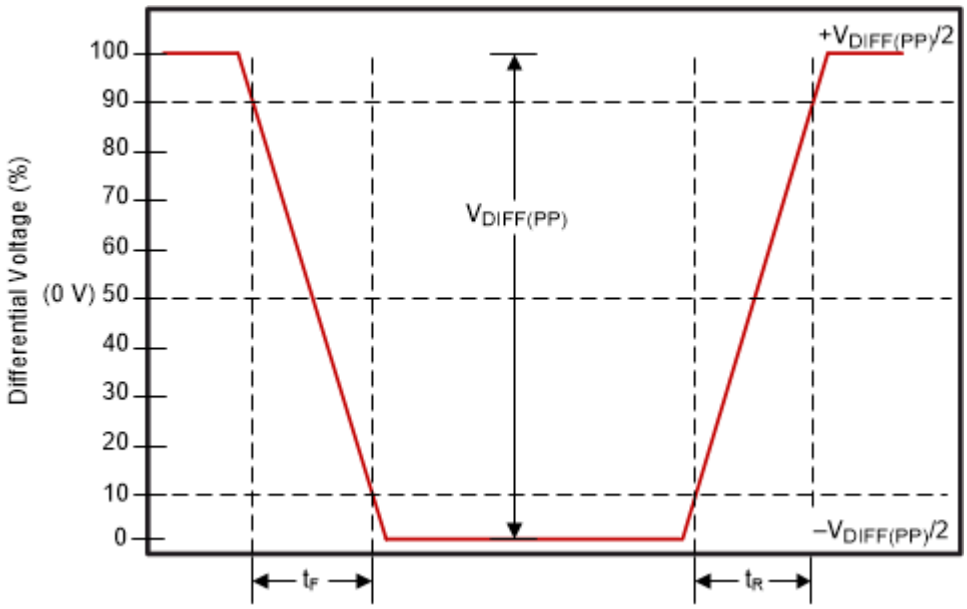

Figure 6-15. DMD Low-Speed Differential Timing Parameters

6.23 DMD SubLVDS Interface Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Differential output rise time (10%-90%)				400	ps
t_F	Differential output fall time (10%-90%)				400	ps
t_{switch}	DMD HS Clock switching rate		0	1200	1440	Mbps
f_{clock}	DMD HS Clock frequency		0	600	720	MHz
DCout	DMD HS Clock output duty cycle		45	50%	55	%

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7 Detailed Description

7.1 Overview

The DLP® Products chipset of this device consists of three components—the DLP230NP or DLP472NP or DLP473NE digital micromirror device (DMD), the DLPC8424 or DLPC8444 or DLPC8454 display controller, and the DLPA3085 or DLPA3082. The DLPC8424, DLPC8444, and DLPC8454 display controllers accept the DMD format incoming video and controls the timing of the DMD. They also control DLPA3085 or DLPA3082 or descrete light source signal timing to coordinate with DMD timing to synchronize light output with DMD mirror movement. The DLPC8424, DLPC8444, and DLPC8454 controllers provide interfaces, such as V-by-One and SubLVDS (DMD interface), to minimize power consumption and EMI. Applications include mobile smart TVs, digital signage, mobile home cinema, and enterprise and education (DLP473NE).

7.2 Functional Block Diagrams

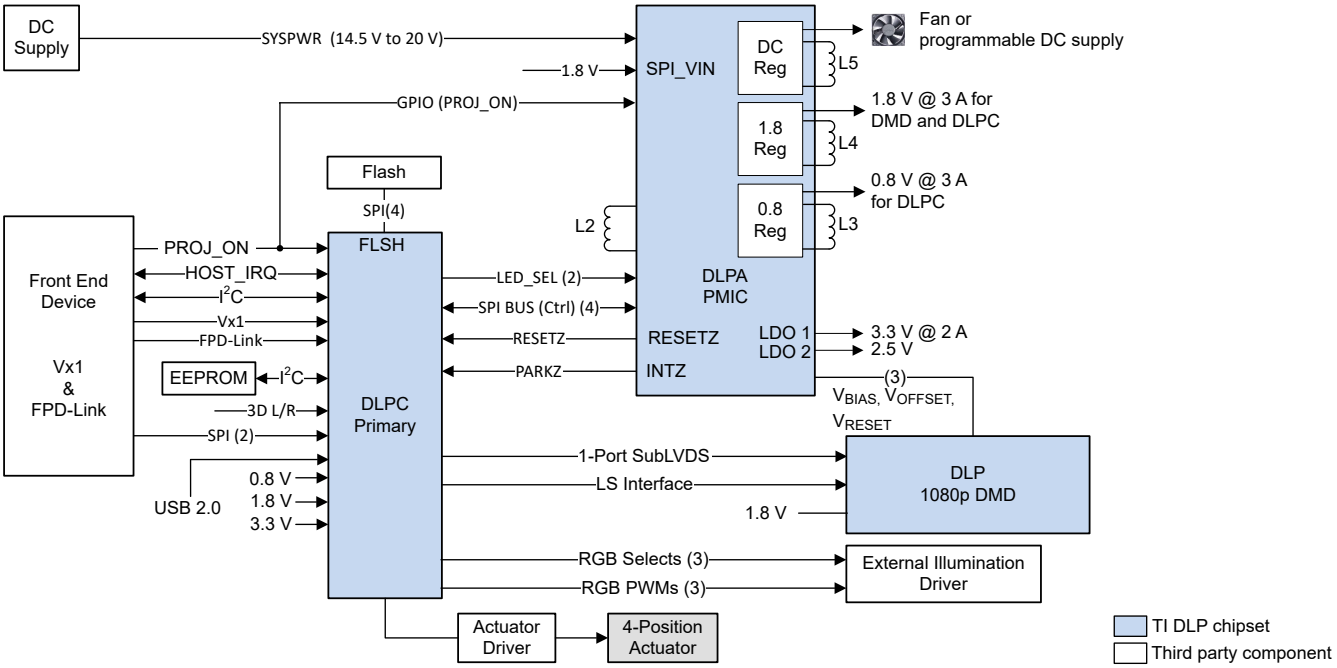

Figure 7-1. LED Functional Block Diagram

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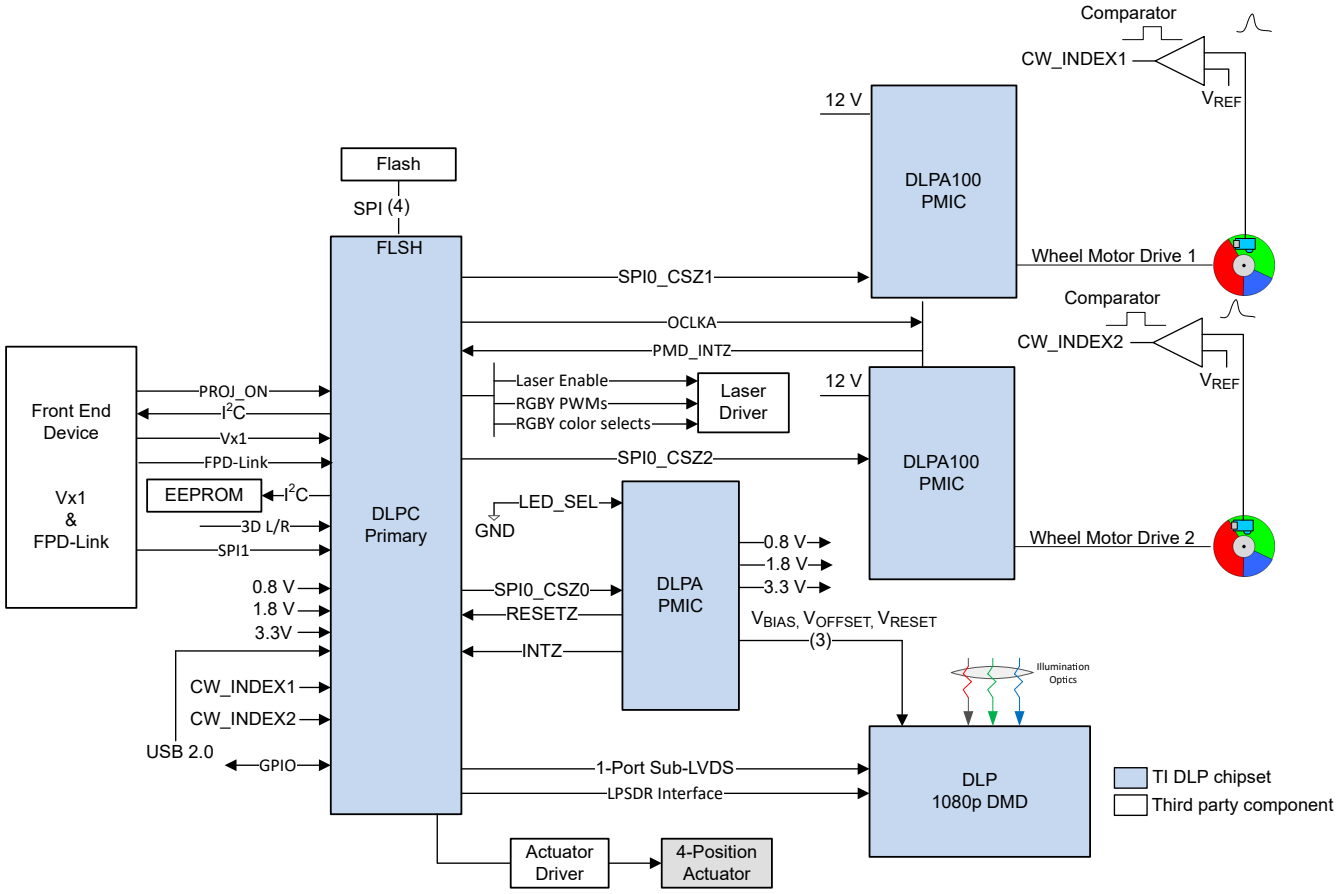

Figure 7-2. Laser-Phosphor Functional Block Diagram

7.3 Feature Description

7.3.1 Input Sources

Table 7-1. Supported Input Source Parameters

INTERFACE	Bits/Pixel Accepted (Max)	Bits/Pixel Processed (Max)	Source Resolution: 2D		Source Resolution: 3D (per Eye) (2)
			Min	Max (1)	Max
V-by-One	12	10	1280 × 720 (3)	3840 × 2160	1920 × 1080 (FS)
FPD Link	10	10	960 × 540	1920 × 1080	1920 × 1080 (FS)

(1) Despite a wider input range, the output resolution will be limited to the DMD and controller capabilities. The resolutions should be checked across devices, including with 3D sources.
(2) FS = Frame Sequential (Full Resolution)
(3) The minimum clock rate and link rate for the V-by-One interface, as well as Byte Mode, limits the smallest resolution that can be supported by this interface. This interface supports 3-Byte, 4-Byte, and 5-Byte Modes.

7.3.2 V-by-One Interface

The controller supports a single 8-lane V-by-One port, which can be configured for 1-, 2-, 4-, or 8-lane use. This interface supports limited lane remapping, which is shown in Table 7-2. Intralane remapping (that is, swapping P with N) is not supported.

Table 7-2. V-by-One Interface Lane Remapping Options

		V-BY-ONE PORT PHYSICAL LANES(1)							
CONFIGURATION(2)	# of LANES	LANE 7	LANE 6	LANE 5	LANE 4	LANE 3	LANE 2	LANE 1	LANE 0
1a	8	7	6	5	4	3	2	1	0
1b	4	—	—	—	—	3	2	1	0
1c	2	—	—	—	—	—	—	1	0
1d	1	—	—	—	—	—	—	—	0
2a	8	1	0	2	3	4	5	6	7
2b	4	1	0	2	3	—	—	—	—
2c	2	1	0	—	—	—	—	—	—
2d	1	—	0	—	—	—	—	—	—

(1) The lane numbers in the table header indicate the actual physical lanes defined in the controller interface. The lane numbers listed below the header are the lane bit numbers transmitted over that physical interface.
(2) There are two controller lane mapping options, with the option to use fewer than the full eight lanes for each.

Independent of the remapping of the physical V-by-One interface, the support a number of data mappings onto the actual physical interface as specified by the standard. V-by-One sources must match at least one of the mappings in Table 7-3, Table 7-4, Table 7-5, Table 7-6, Table 7-7, and Table 7-8.

Table 7-3. V-by-One Data Mapping for 36bpp/30bpp RGB/YCbCr 4:4:4

V-BY-ONE DATA MAP MODE 0			
V-BY-ONE INPUT DATA BIT	36bpp RGB/YCbCr 4:4:4(1)	30bpp RGB/YCbCr 4:4:4	MAPPER OUTPUT
D[0]	R/Cr[4]	R/Cr[2]	B(2)
D[1]	R/Cr[5]	R/Cr[3]	B(3)
D[2]	R/Cr[6]	R/Cr[4]	B(4)
D[3]	R/Cr[7]	R/Cr(5]	B(5)
D[4]	R/Cr[8]	R/Cr[6]	B(6)
D[5]	R/Cr[9]	R/Cr[7]	B(7)
D[6]	R/Cr[10]	R/Cr[8]	B(8)
D[7]	R/Cr[11]	R/Cr[9]	B(9)
D[8]	G/Y[4]	G/Y[2]	A(2)
D[9]	G/Y[5]	G/Y[3]	A(3)

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Table 7-3. V-by-One Data Mapping for 36bpp/30bpp RGB/YCbCr 4:4:4 (continued)

V-BY-ONE DATA MAP MODE 0			
V-BY-ONE INPUT DATA BIT	**36bpp RGB/YCbCr 4:4:4(1)**	**30bpp RGB/YCbCr 4:4:4**	**MAPPER OUTPUT**
D[10]	G/Y[6]	G/Y[4]	A(4)
D[11]	G/Y[7]	G/Y[5]	A(5)
D[12]	G/Y[8]	G/Y[6]	A(6)
D[13]	G/Y[9]	G/Y[7]	A(7)
D[14]	G/Y[10]	G/Y[8]	A(8)
D[15]	G/Y[11]	G/Y[9]	A(9)
D[16]	B/Cb[4]	B/Cb[2]	C(2)
D[17]	B/Cb[5]	B/Cb[3]	C(3)
D[18]	B/Cb[6]	B/Cb[4]	C(4)
D[19]	B/Cb[7]	B/Cb[5]	C(5)
D[20]	B/Cb[8]	B/Cb[6]	C(6)
D[21]	B/Cb[9]	B/Cb[7]	C(7)
D[22]	B/Cb[10]	B/Cb[8]	C(8)
D[23]	B/Cb[11]	B/Cb[9]	C(9)
D[24]	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref
D[25]	3DEN/Field	3DEN/Field	3DEN/Field
D[26]	B/Cb[2]	B/Cb[1]	C[0]
D[27]	B/Cb[3]	B/Cb[0]	C[1]
D[28]	G/Y[2]	G/Y[1]	A[0]
D[29]	G/Y[3]	G/Y[0]	A[1]
D[30]	R/Cr[2]	R/Cr[1]	B[0]
D[31]	R/Cr[3]	R/Cr[0]	B[1]

(1) For 36-bit inputs, the 12 bits per color truncates to 10 bits per color with the two least significant bits per color being discarded.

Table 7-4. V-by-One Data Mapping for 27bpp RGB/YCbCr 4:4:4

V-BY-ONE DATA MAP MODE 1		
V-BY-ONE INPUT DATA BIT	**27bpp RGB/YCbCr 4:4:4(1)**	**MAPPER OUTPUT**
D[0]	R/Cr[1]	B(2)
D[1]	R/Cr[2]	B(3)
D[2]	R/Cr[3]	B(4)
D[3]	R/Cr[4]	B(5)
D[4]	R/Cr[5]	B(6)
D[5]	R/Cr[6]	B(7)
D[6]	R/Cr[7]	B(8)
D[7]	R/Cr[8]	B(9)
D[8]	G/Y[1]	A(2)
D[9]	G/Y[2]	A(3)
D[10]	G/Y[3]	A(4)
D[11]	G/Y[4]	A(5)
D[12]	G/Y[5]	A(6)
D[13]	G/Y[6]	A(7)
D[14]	G/Y[7]	A(8)
D[15]	G/Y[8]	A(9)
D[16]	B/Cb[1]	C(2)
D[17]	B/Cb[2]	C(3)

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Table 7-4. V-by-One Data Mapping for 27bpp RGB/YCbCr 4:4:4 (continued)

V-BY-ONE DATA MAP MODE 1		
V-BY-ONE INPUT DATA BIT	**27bpp RGB/YCbCr 4:4:4(1)**	**MAPPER OUTPUT**
D[18]	B/Cb[3]	C(4)
D[19]	B/Cb[4]	C(5)
D[20]	B/Cb[5]	C(6)
D[21]	B/Cb[6]	C(7)
D[22]	B/Cb[7]	C(8)
D[23]	B/Cb[8]	C(9)
D[24]	3D_L/R_Ref	3D_L/R_Ref
D[25]	3DEN/Field	3DEN/Field
'0'	—	C[0]
D[27]	B/Cb[0]	C[1]
'0'	—	A[0]
D[29]	G/Y[0]	A[1]
'0'	—	B[0]
D[31]	R/Cr[0]	B[1]

(1) For 27-bit inputs, the 9 bits for each color shift up one bit, and the least significant bit of each color is set to '0'.

Table 7-5. V-by-One Data Mapping for 24bpp RGB/YCbCr 4:4:4

V-BY-ONE DATA MAP MODE 2		
V-BY-ONE INPUT DATA BIT	**24bpp RGB/YCbCr 4:4:4(1)**	**MAPPER OUTPUT**
D[0]	R/Cr[0]	B(2)
D[1]	R/Cr[1]	B(3)
D[2]	R/Cr[2]	B(4)
D[3]	R/Cr[3]	B(5)
D[4]	R/Cr[4]	B(6)
D[5]	R/Cr[5]	B(7)
D[6]	R/Cr[6]	B(8)
D[7]	R/Cr[7]	B(9)
D[8]	G/Y[0]	A(2)
D[9]	G/Y[1]	A(3)
D[10]	G/Y[2]	A(4)
D[11]	G/Y[3]	A(5)
D[12]	G/Y[4]	A(6)
D[13]	G/Y[5]	A(7)
D[14]	G/Y[6]	A(8)
D[15]	G/Y[7]	A(9)
D[16]	B/Cb[0]	C(2)
D[17]	B/Cb[1]	C(3)
D[18]	B/Cb[2]	C(4)
D[19]	B/Cb[3]	C(5)
D[20]	B/Cb[4]	C(6)
D[21]	B/Cb[5]	C(7)
D[22]	B/Cb[6]	C(8)
D[23]	B/Cb[7]	C(9)
D[24]	3D_L/R_Ref	3D_L/R_Ref
D[25]	3DEN/Field	3DEN/Field

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Table 7-5. V-by-One Data Mapping for 24bpp RGB/YCbCr 4:4:4 (continued)

V-BY-ONE DATA MAP MODE 2		
V-BY-ONE INPUT DATA BIT	**24bpp RGB/YCbCr 4:4:4(1)**	**MAPPER OUTPUT**
'0'	—	C[0]
'0'	—	C[1]
'0'	—	A[0]
'0'	—	A[1]
'0'	—	B[0]
'0'	—	B[1]

(1) For 24-bit inputs, the 8 bits for each color shift up two bits, and the two least significant bits of each color are set to '0'.

Table 7-6. V-by-One Data Mapping for 32bpp/24bpp/20bpp YCbCr 4:2:2

V-BY-ONE DATA MAP MODE 3(1)				
V-BY-ONE INPUT DATA BIT	**32bpp YCbCr 4:2:2(2)**	**24bpp YCbCr 4:2:2(3)**	**20bpp YCbCr 4:2:2**	**MAPPER OUTPUT**
D[0]	CbCr[8]	CbCr[4]	CbCr[2]	B(2)
D[1]	CbCr[9]	CbCr[5]	CbCr[3]	B(3)
D[2]	CbCr[10]	CbCr[6]	CbCr[4]	B(4)
D[3]	CbCr[11]	CbCr[7]	CbCr[5]	B(5)
D[4]	CbCr[12]	CbCr[8]	CbCr[6]	B(6)
D[5]	CbCr[13]	CbCr[8]	CbCr[7]	B(7)
D[6]	CbCr[14]	CbCr[10]	CbCr[8]	B(8)
D[7]	CbCr[15]	CbCr[11]	CbCr[9]	B(9)
D[8]	Y[8]	Y[4]	Y[2]	A(2)
D[9]	Y[9]	Y[5]	Y[3]	A(3)
D[10]	Y[10]	Y[6]	Y[4]	A(4)
D[11]	Y[11]	Y[7]	Y[5]	A(5)
D[12]	Y[12]	Y[8]	Y[6]	A(6)
D[13]	Y[13]	Y[9]	Y[7]	A(7)
D[14]	Y[14]	Y[10]	Y[8]	A(8)
D[15]	Y[15]	Y[11]	Y[9]	A(9)
'0'	—	—	—	C(2)
'0'	—	—	—	C(3)
'0'	—	—	—	C(4)
'0'	—	—	—	C(5)
'0'	—	—	—	C(6)
'0'	—	—	—	C(7)
'0'	—	—	—	C(8)
'0'	—	—	—	C(9)
D[24]	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref	3D_L/R_Ref
D[25]	3DEN/Field	3DEN/Field	3DEN/Field	3DEN/Field
'0'	—	—	—	C[0]
'0'	—	—	—	C[1]
D[28]	Y[6]	Y[2]	Y[2]	A[0]
D[29]	Y[7]	Y[3]	Y[3]	A[1]
D[30]	CbCr[6]	CbCr[2]	CbCr[2]	B[0]
D[31]	CbCr[7]	CbCr[3]	CbCr[3]	B[1]

(1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".

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(2) For 32-bit inputs, the 16 bits per color truncate to 10-bit per color, with the six least significant bits per color discarded.
(3) For 24-bit inputs, the 12 bits per color truncate to 10-bit per color, with the two least significant bits per color discarded.

Table 7-7. V-by-One Data Mapping for 18bpp YCbCr 4:2:2

V-BY-ONE DATA MAP MODE 4[1]		
V-BY-ONE INPUT DATA BIT	**18bpp YCbCr 4:2:2[2]**	**MAPPER OUTPUT**
D[0]	CbCr[1]	B(2)
D[1]	CbCr[2]	B(3)
D[2]	CbCr[3]	B(4)
D[3]	CbCr[4]	B(5)
D[4]	CbCr[5]	B(6)
D[5]	CbCr[6]	B(7)
D[6]	CbCr[7]	B(8)
D[7]	CbCr[8]	B(9)
D[8]	Y[1]	A(2)
D[9]	Y[2]	A(3)
D[10]	Y[3]	A(4)
D[11]	Y[4]	A(5)
D[12]	Y[5]	A(6)
D[13]	Y[6]	A(7)
D[14]	Y[7]	A(8)
D[15]	Y[8]	A(9)
'0'	—	C(2)
'0'	—	C(3)
'0'	—	C(4)
'0'	—	C(5)
'0'	—	C(6)
'0'	—	C(7)
'0'	—	C(8)
'0'	—	C(9)
D[24]	3D_L/R_Ref	3D_L/R_Ref
D[25]	3DEN/Field	3DEN/Field
'0'	—	C[0]
'0'	—	C[1]
'0'	—	A[0]
D[29]	Y[0]	A[1]
'0'	—	B[0]
D[31]	CbCr[0]	B[1]

(1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".
(2) For 18-bit inputs, the 9 bits for each color shift up one bit, and the least significant bits of each color are set to '0'.

Table 7-8. V-by-One Data Mapping for 16bpp YCbCr 4:2:2

V-BY-ONE DATA MAP MODE 5[1]		
V-BY-ONE INPUT DATA BIT	**16bpp YCbCr 4:2:2[2]**	**MAPPER OUTPUT**
D[0]	CbCr[0]	B(2)
D[1]	CbCr[1]	B(3)
D[2]	CbCr[2]	B(4)
D[3]	CbCr[3]	B(5)
D[4]	CbCr[4]	B(6)

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Table 7-8. V-by-One Data Mapping for 16bpp YCbCr 4:2:2 (continued)

V-BY-ONE DATA MAP MODE 5[1]		
V-BY-ONE INPUT DATA BIT	**16bpp YCbCr 4:2:2[2]**	**MAPPER OUTPUT**
D[5]	CbCr[5]	B(7)
D[6]	CbCr[6]	B(8)
D[7]	CbCr[7]	B(9)
D[8]	Y[0]	A(2)
D[9]	Y[1]	A(3)
D[10]	Y[2]	A(4)
D[11]	Y[3]	A(5)
D[12]	Y[4]	A(6)
D[13]	Y[5]	A(7)
D[14]	Y[6]	A(8)
D[15]	Y[7]	A(9)
'0'	—	C(2)
'0'	—	C(3)
'0'	—	C(4)
'0'	—	C(5)
'0'	—	C(6)
'0'	—	C(7)
'0'	—	C(8)
'0'	—	C(9)
D[24]	3D_L/R_Ref	3D_L/R_Ref
D[25]	3DEN/Field	3DEN/Field
'0'	—	C[0]
'0'	—	C[1]
'0'	—	A[0]
'0'	—	A[1]
'0'	—	B[0]
'0'	—	B[1]

(1) For all YCbCr 4:2:2 formats, data channel C is forced to "0".
(2) For 16-bit inputs, the 8 bits for each color shift up one bit, and the least significant bit of each color is set to '0'.

7.3.3 FPD-Link Interface

The DLPC84x4 supports two FPD-Link 5-lane ports, which can be configured for single-port use (Port A or Port B), or for dual-port use (Port A and Port B). The third FPD port (Port C) is reserved for parallel port use only. FPD ports A and B support a limited set of remapping options within each port, but there is no remapping between ports. When utilizing this feature, each unique lane pair can only be mapped to one unique destination lane pair, and intralane remapping (that is, swapping P with N) is not supported. In addition, the A and B ports can be swapped. Lane and port remapping (specified in Flash) can help with board layout as needed. The typical lane mapping is shown in Figure 7-3. An example of an alternate lane mapping is shown in Figure 7-4. The specific intraport remapping options available are shown in Table 7-9.

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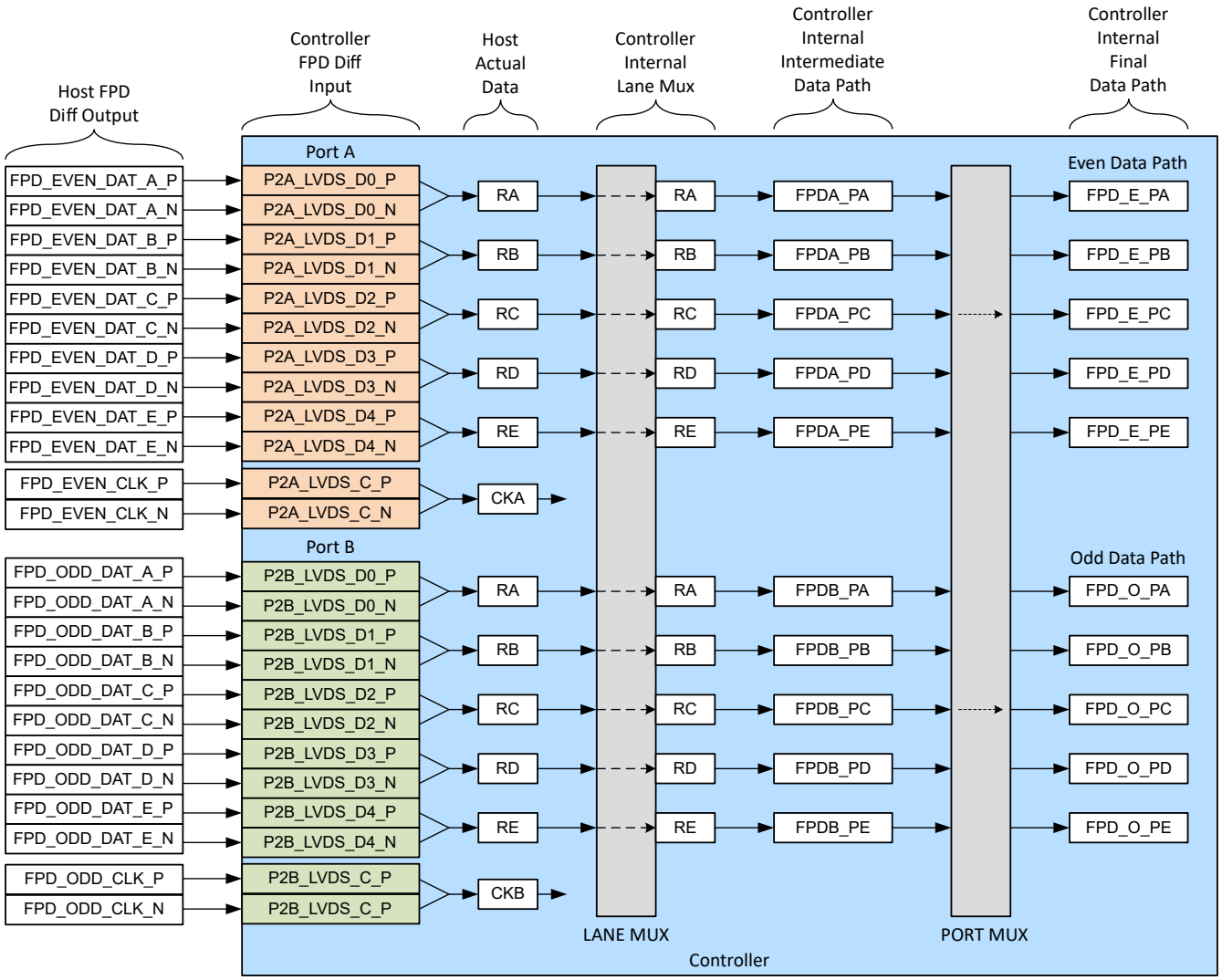

Figure 7-3. Example of Typical FPD-Link Port Lane Mapping

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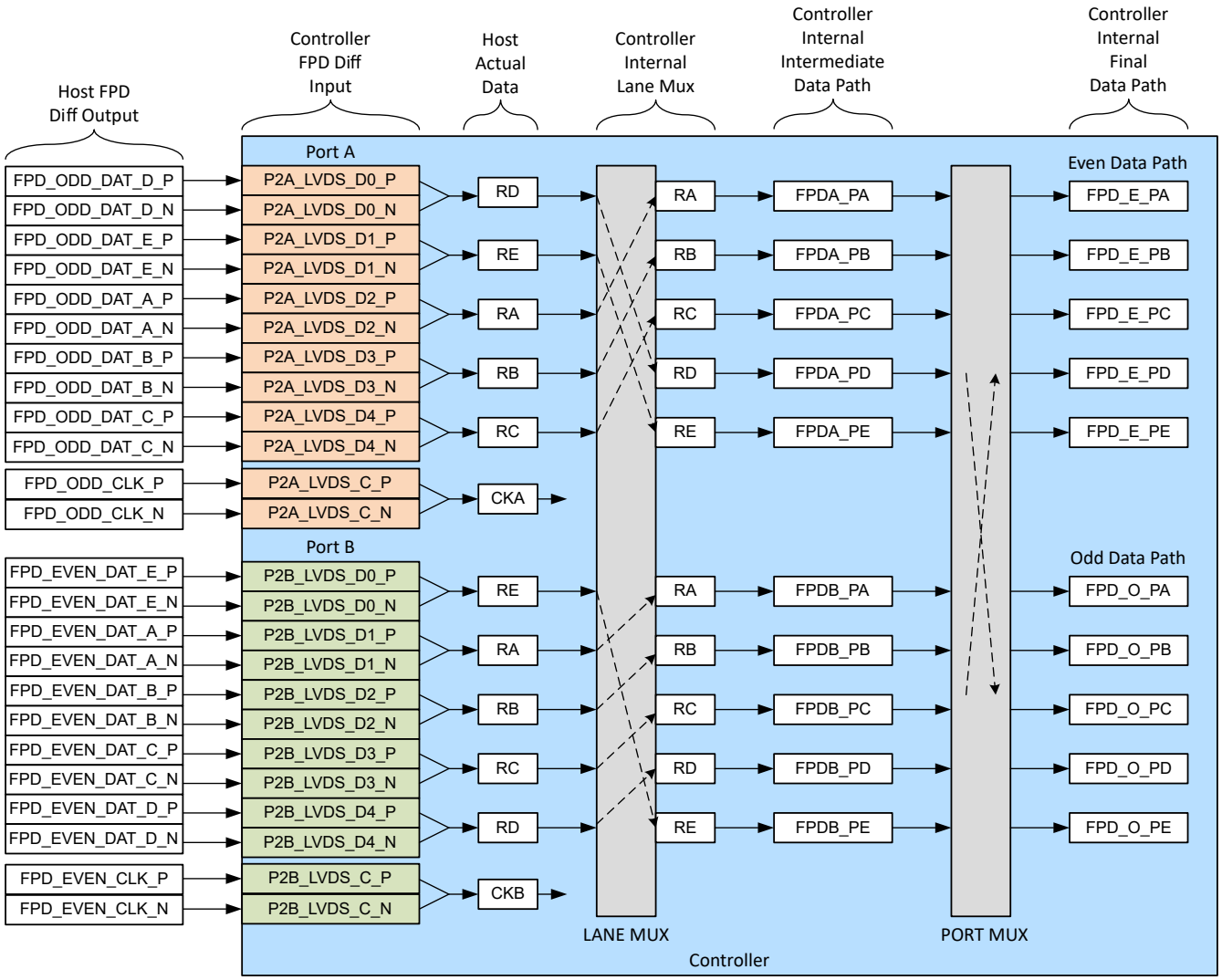

Figure 7-4. Example of Alternate FPD-Link Port Lane Mapping

Table 7-9. FPD-Link Intra Port Data Mapping Options

Mapping Options for Ports A and B	Input Data Port	Internal Final Data Path
0	P2x_LVDS_D0_P/N	FPD_x_PA
1	P2x_LVDS_D1_P/N	FPD_x_PA
2	P2x_LVDS_D2_P/N	FPD_x_PA
3	P2x_LVDS_D3_P/N	FPD_x_PA
4	P2x_LVDS_D4_P/N	FPD_x_PA
4	P2x_LVDS_D0_P/N	FPD_x_PB
0	P2x_LVDS_D1_P/N	FPD_x_PB
1	P2x_LVDS_D2_P/N	FPD_x_PB
2	P2x_LVDS_D3_P/N	FPD_x_PB
3	P2x_LVDS_D4_P/N	FPD_x_PB
3	P2x_LVDS_D0_P/N	FPD_x_PC
4	P2x_LVDS_D1_P/N	FPD_x_PC
0	P2x_LVDS_D2_P/N	FPD_x_PC
1	P2x_LVDS_D3_P/N	FPD_x_PC
2	P2x_LVDS_D4_P/N	FPD_x_PC
2	P2x_LVDS_D0_P/N	FPD_x_PD
3	P2x_LVDS_D1_P/N	FPD_x_PD
4	P2x_LVDS_D2_P/N	FPD_x_PD
0	P2x_LVDS_D3_P/N	FPD_x_PD
1	P2x_LVDS_D4_P/N	FPD_x_PD
1	P2x_LVDS_D0_P/N	FPD_x_PE
2	P2x_LVDS_D1_P/N	FPD_x_PE
3	P2x_LVDS_D2_P/N	FPD_x_PE
4	P2x_LVDS_D3_P/N	FPD_x_PE
0	P2x_LVDS_D4_P/N	FPD_x_PE

Independent of the remapping of the physical FPD interface, the DLPC84x4 supports a number of data mappings onto the actual physical interface. There are three different 30-bit data mappings and two different 24-bit data mappings supported. FPD sources must match at least one of these mappings. These are shown in Table 7-10, Table 7-11, Table 7-12, Table 7-13, and Table 7-14.

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Table 7-10. FPD-Link Data Mapping onto Physical Interface (30-Bit Mode 0)

Bit Mapping—30-Bit Mode 0[1] (30 bits per pixel)			
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**Mapper Output**
PA-6	G/Y[4]	Y[4]	A(4)
PA-5	R/Cr[9]	Cb/Cr[9]	B(9)
PA-4	R/Cr[8]	Cb/Cr[8]	B(8)
PA-3	R/Cr[7]	Cb/Cr[7]	B(7)
PA-2	R/Cr[6]	Cb/Cr[6]	B(6)
PA-1	R/Cr[5]	Cb/Cr[5]	B(5)
PA-0	R/Cr[4]	Cb/Cr[4]	B(4)
PB-6	B/Cb[5]	Unused	C(5)
PB-5	B/Cb[4]	Unused	C(4)
PB-4	G/Y[9]	Y[9]	A(9)
PB-3	G/Y[8]	Y[8]	A(8)
PB-2	G/Y[7]	Y[7]	A(7)
PB-1	G/Y[6]	Y[6]	A(6)
PB-0	G/Y[5]	Y[5]	A(5)
PC-6	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[9]	Unused	C(9)
PC-2	B/Cb[8]	Unused	C(8)
PC-1	B/Cb[7]	Unused	C(7)
PC-0	B/Cb[6]	Unused	C(6)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[3]	Unused	C(3)
PD-4	B/Cb[2]	Unused	C(2)
PD-3	G/Y[3]	Y[3]	A(3)
PD-2	G/Y[2]	Y[2]	A(2)
PD-1	R/Cr[3]	Cb/Cr[3]	B(3)
PD-0	R/Cr[2]	Cb/Cr[2]	B(2)
PE-6	Field	Field	Field
PE-5	B/Cb[1]	Unused	C(1)
PE-4	B/Cb[0]	Unused	C(0)
PE-3	G/Y[1]	Y[1]	A(1)
PE-2	G/Y[0]	Y[0]	A(0)
PE-1	R/Cr[1]	Cb/Cr[1]	B(1)
PE-0	R/Cr[0]	Cb/Cr[0]	B(0)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

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Table 7-11. FPD-Link Data Mapping onto Physical Interface (30-Bit Mode 1)

Bit Mapping—30-Bit Mode 1[1] (30 bits per pixel)			
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**Mapper Output**
PA-6	G/Y[2]	Y[2]	A(2)
PA-5	R/Cr[7]	Cb/Cr[7]	B(7)
PA-4	R/Cr[6]	Cb/Cr[6]	B(6)
PA-3	R/Cr(5]	Cb/Cr[5]	B(5)
PA-2	R/Cr[4]	Cb/Cr[4]	B(4)
PA-1	R/Cr[3]	Cb/Cr[3]	B(3)
PA-0	R/Cr[2]	Cb/Cr[2]	B(2)
PB-6	B/Cb[3]	Unused	C(3)
PB-5	B/Cb[2]	Unused	C(2)
PB-4	G/Y[7]	Y[7]	A(7)
PB-3	G/Y[6]	Y[6]	A(6)
PB-2	G/Y[5]	Y[5]	A(5)
PB-1	G/Y[4]	Y[4]	A(4)
PB-0	G/Y[3]	Y[3]	A(3)
PC-6	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[7]	Unused	C(7)
PC-2	B/Cb[6]	Unused	C(6)
PC-1	B/Cb[5]	Unused	C(5)
PC-0	B/Cb[4]	Unused	C(4)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[9]	Unused	C(9)
PD-4	B/Cb[8]	Unused	C(8)
PD-3	G/Y[9]	Y[9]	A(9)
PD-2	G/Y[8]	Y[8]	A(8)
PD-1	R/Cr[9]	Cb/Cr[9]	B(9)
PD-0	R/Cr[8]	Cb/Cr[8]	B(8)
PE-6	Field	Field	Field
PE-5	B/Cb[1]	Unused	C(1)
PE-4	B/Cb[0]	Unused	C(0)
PE-3	G/Y[1]	Y[1]	A(1)
PE-2	G/Y[0]	Y[0]	A(0)
PE-1	R/Cr[1]	Cb/Cr[1]	B(1)
PE-0	R/Cr[0]	Cb/Cr[0]	B(0)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

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Table 7-12. FPD-Link Data Mapping onto Physical Interface (30-Bit Mode 2)

Bit Mapping—30-Bit Mode 2[1] (30 bits per pixel)			
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**Mapper Output**
PA-6	G/Y[0]	Y[0]	A(0)
PA-5	R/Cr[5]	Cb/Cr[5]	B(5)
PA-4	R/Cr[4]	Cb/Cr[4]	B(4)
PA-3	R/Cr(3]	Cb/Cr[3]	B(3)
PA-2	R/Cr[2]	Cb/Cr[2]	B(2)
PA-1	R/Cr[1]	Cb/Cr[1]	B(1)
PA-0	R/Cr[0]	Cb/Cr[0]	B(0)
PB-6	B/Cb[1]	Unused	C(1)
PB-5	B/Cb[0]	Unused	C(0)
PB-4	G/Y[5]	Y[5]	A(5)
PB-3	G/Y[4]	Y[4]	A(4)
PB-2	G/Y[3]	Y[3]	A(3)
PB-1	G/Y[2]	Y[2]	A(2)
PB-0	G/Y[1]	Y[1]	A(1)
PC-6	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[5]	Unused	C(5)
PC-2	B/Cb[4]	Unused	C(4)
PC-1	B/Cb[3]	Unused	C(3)
PC-0	B/Cb[2]	Unused	C(2)
PD-6	3D_L/R_Ref	3D_L/R_Ref	3D_Ref
PD-5	B/Cb[7]	Unused	C(7)
PD-4	B/Cb[6]	Unused	C(6)
PD-3	G/Y[7]	Y[7]	A(7)
PD-2	G/Y[6]	Y[6]	A(6)
PD-1	R/Cr[7]	Cb/Cr[7]	B(7)
PD-0	R/Cr[6]	Cb/Cr[6]	B(6)
PE-6	Field	Field	Field
PE-5	B/Cb[9]	Unused	C(9)
PE-4	B/Cb[8]	Unused	C(8)
PE-3	G/Y[9]	Y[9]	A(9)
PE-2	G/Y[8]	Y[8]	A(8)
PE-1	R/Cr[9]	Cb/Cr[9]	B(9)
PE-0	R/Cr[8]	Cb/Cr[8]	B(8)

(1) Input data bits are defined with bit[9] as the most significant bit, and bit[0] as the least significant bit.

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Table 7-13. FPD-Link Data Mapping onto Physical Interface (24-Bit Mode 0) (1) (2)

Bit Mapping—24-Bit Mode 0(1) (24 bits per pixel)			
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**Mapper Output**
PA-6	G/Y[0]	Y[0]	A(2)
PA-5	R/Cr[5]	Cb/Cr[5]	B(7)
PA-4	R/Cr[4]	Cb/Cr[4]	B(6)
PA-3	R/Cr(3]	Cb/Cr[3]	B(5)
PA-2	R/Cr[2]	Cb/Cr[2]	B(4)
PA-1	R/Cr[1]	Cb/Cr[1]	B(3)
PA-0	R/Cr[0]	Cb/Cr[0]	B(2)
PB-6	B/Cb[1]	Unused	C(3)
PB-5	B/Cb[0]	Unused	C(2)
PB-4	G/Y[5]	Y[5]	A(7)
PB-3	G/Y[4]	Y[4]	A(6)
PB-2	G/Y[3]	Y[3]	A(5)
PB-1	G/Y[2]	Y[2]	A(4)
PB-0	G/Y[1]	Y[1]	A(3)
PC-6	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[5]	Unused	C(7)
PC-2	B/Cb[4]	Unused	C(6)
PC-1	B/Cb[3]	Unused	C(5)
PC-0	B/Cb[2]	Unused	C(4)
PD-6	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_Ref or Field
PD-5	B/Cb[7]	Unused	C(9)
PD-4	B/Cb[6]	Unused	C(8)
PD-3	G/Y[7]	Y[7]	A(9)
PD-2	G/Y[6]	Y[6]	A(8)
PD-1	R/Cr[7]	Cb/Cr[7]	B(9)
PD-0	R/Cr[6]	Cb/Cr[6]	B(8)
PE-6	Unused	Unused	Unused
PE-5	Unused	Unused	Unused
PE-4	Unused	Unused	Unused
PE-3	Unused	Unused	Unused
PE-2	Unused	Unused	Unused
PE-1	Unused	Unused	Unused
PE-0	Unused	Unused	Unused

(1) To support 24-bit data, the mapper shifts each 8-bit color up by 2 bits, and forces output bits A[1], A[0], B[1], B[0], C[1], and C[0] to value '0'.
(2) Input data bits are defined with bit[7] as the most significant bit, and bit[0] as the least significant bit.

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Table 7-14. FPD-Link Data Mapping onto Physical Interface (24-Bit Mode 1) (1)

Bit Mapping—24-Bit Mode 1(1) (2) (24 bits per pixel)			
Mapper Input	**RGB/YCbCr 4:4:4**	**YCbCr 4:2:2**	**Mapper Output**
PA-6	G/Y[2]	Y[2]	A(4)
PA-5	R/Cr[7]	Cb/Cr[7]	B(9)
PA-4	R/Cr[6]	Cb/Cr[6]	B(8)
PA-3	R/Cr(5]	Cb/Cr[5]	B(7)
PA-2	R/Cr[4]	Cb/Cr[4]	B(6)
PA-1	R/Cr[3]	Cb/Cr[3]	B(5)
PA-0	R/Cr[2]	Cb/Cr[2]	B(4)
PB-6	B/Cb[3]	Unused	C(5)
PB-5	B/Cb[2]	Unused	C(4)
PB-4	G/Y[7]	Y[7]	A(9)
PB-3	G/Y[6]	Y[6]	A(8)
PB-2	G/Y[5]	Y[5]	A(7)
PB-1	G/Y[4]	Y[4]	A(6)
PB-0	G/Y[3]	Y[3]	A(5)
PC-6	Data En	Data En	Data En
PC-5	VSYNC	VSYNC	VSYNC
PC-4	HSYNC	HSYNC	HSYNC
PC-3	B/Cb[7]	Unused	C(9)
PC-2	B/Cb[6]	Unused	C(8)
PC-1	B/Cb[5]	Unused	C(7)
PC-0	B/Cb[4]	Unused	C(6)
PD-6	3D_L/R_Ref or Field	3D_L/R_Ref or Field	3D_Ref or Field
PD-5	B/Cb[1]	Unused	C(3)
PD-4	B/Cb[0]	Unused	C(2)
PD-3	G/Y[1]	Y[1]	A(3)
PD-2	G/Y[0]	Y[0]	A(2)
PD-1	R/Cr[1]	Cb/Cr[1]	B(3)
PD-0	R/Cr[0]	Cb/Cr[0]	B(2)
PE-6	Unused	Unused	Unused
PE-5	Unused	Unused	Unused
PE-4	Unused	Unused	Unused
PE-3	Unused	Unused	Unused
PE-2	Unused	Unused	Unused
PE-1	Unused	Unused	Unused
PE-0	Unused	Unused	Unused

(1) To support 24-bit data, the mapper shifts each 8-bit color up by 2 bits, and forces output bits A[1], A[0], B[1], B[0], C[1], and C[0] to value '0'.
(2) Input data bits are defined with bit[7] as the most significant bit, and bit[0] as the least significant bit.

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7.3.4 DMD (SubLVDS) Interface

The controller DMD interface supports four high-speed SubLVDS output-only interfaces for data transmission, a single-ended, low-speed LVDS output-only interface for command write transactions, as well as four low-speed single-ended input interfaces used for command read transactions. Each SubLVDS port supports full data-only inter-lane remapping within the port, but not between ports. When utilizing this feature, each unique data lane pair can only be mapped to one unique destination data lane pair, and intralane remapping (that is, swapping P with N) is not supported. In addition, the four HS data ports can also be swapped. The HS CLK pins are not interchangeable between ports and must be grouped with the corresponding port data lanes. Lane and port remapping (specified in Flash) can help with board layout as needed. The number of HS ports and the number of HS lanes per HS port required are based on DMD type and DMD display resolution. Table 7-16 shows some remapping examples for a two HS ports configuration with the same rules applying up to four HS ports. When all ports are used, they do not need the same pin mapping.

Table 7-15. Controller to DLP230NP DMD Pin Mapping Examples

Controller PINS - REMAPPING EXAMPLES TO DMD PINS		
ASIC OUTPUT EXAMPLE 1	**ASIC OUTPUT EXAMPLE 2**	**DMD PINS**
DMD_HS0_CLK_P DMD_HS0_CLK_N	DMD_HS0_CLK_P DMD_HS0_CLK_N	DCLK_P DCLK_N
DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N	DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N	D_P(0) D_N(0)
DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N	DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N	D_P(1) D_N(1)
DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N	DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N	D_P(2) D_N(2)
DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N	DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	D_P(3) D_N(3)
DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N	D_P(4) D_N(4)
DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N	DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N	D_P(5) D_N(5)
DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N	DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N	D_P(6) D_N(6)
DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N	DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N	D_P(7) D_N(7)
DMD_LS1_CLK	DMD_LS1_CLK	LS_CLK
DMD_LS1_WDATA	DMD_LS1_WDATA	LS_WDATA
DMD_LS1_RDATA	DMD_LS1_RDATA	LS_RDATA
DMD_DEN_ARSTZ	DMD_DEN_ARSTZ	DEN_ARSTZ

Table 7-16. Controller to DLP472NP DMD Pin Mapping Examples

Controller PINS - REMAPPING EXAMPLES TO DMD PINS				DMD PINS
BASELINE	**FLIP HS0 180 No FLIP HS1**	**SWAP HS0 PORT WITH HS1 PORT**	**SWAP HS0 PORT WITH HS1 PORT AND MIXED REMAPPING**	
DMD_HS0_CLK_P DMD_HS0_CLK_N	DMD_HS0_CLK_P DMD_HS0_CLK_N	DMD_HS1_CLK_P DMD_HS1_CLK_N	DMD_HS1_CLK_P DMD_HS1_CLK_N	DCLK_AP DCLK_AN
DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N	DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N	DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N	D_AP(0) D_AN(0)
DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N	DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N	DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N	DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N	D_AP(1) D_AN(1)
DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N	DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N	DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N	DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N	D_AP(2) D_AN(2)
DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N	DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N	DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N	DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N	D_AP(3) D_AN(3)

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Table 7-16. Controller to DLP472NP DMD Pin Mapping Examples (continued)

Controller PINS - REMAPPING EXAMPLES TO DMD PINS				DMD PINS
BASELINE	FLIP HS0 180 No FLIP HS1	SWAP HS0 PORT WITH HS1 PORT	SWAP HS0 PORT WITH HS1 PORT AND MIXED REMAPPING	
DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N	DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N	DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N	DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N	D_AP(4) D_AN(4)
DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N	DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N	DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N	DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N	D_AP(5) D_AN(5)
DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N	DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N	DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N	DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N	D_AP(6) D_AN(6)
DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N	DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N	DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N	D_AP(7) D_AN(7)
DMD_HS1_CLK_P DMD_HS1_CLK_N	DMD_HS1_CLK_P DMD_HS1_CLK_N	DMD_HS0_CLK_P DMD_HS0_CLK_N	DMD_HS0_CLK_P DMD_HS0_CLK_N	DCLK_BP DCLK_BN
DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N	DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N	DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N	D_BP(0) D_BN(0)
DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N	DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N	DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N	DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N	D_BP(1) D_BN(1)
DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N	DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N	DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N	DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N	D_BP(2) D_BN(2)
DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N	DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N	DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N	DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N	D_BP(3) D_BN(3)
DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N	DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N	DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N	DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N	D_BP(4) D_BN(4)
DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N	DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N	DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N	DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N	D_BP(5) D_BN(5)
DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N	DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N	DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N	DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	D_BP(6) D_BN(6)
DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N	DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N	DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N	DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N	D_BP(7) D_BN(7)

7.3.5 Serial Flash Interface

The contoller interfaces to a single external standard/dual/quad SPI serial Flash memory device for configuration and operational data. The 6-pin interface consists of an active low chip select signal, a clock signal, and four bi-directional data signals that can be used to support Standard/Dual/Quad SPI data I/O configurations as necessary during serial flash command execution. Table 7-17 shows a list of supported serial Flash devices that have been validated with the controller.

Table 7-17. DLPC84x4 Supported Standard/Dual/Quad SPI Serial Flash Devices

DENSITY (Mbits)	VENDOR	PART NUMBER	PACKAGE SIZE
1.8V Compatible Devices			
8	Macronix	MX25R8035FBHIH2	WLCSP
16	Winbond	W25Q16JWBYIQ	WLCSP
32	Macronix	MX25U3232FBHI02	WLCSP
64	Winbond	W25Q64JWBYIQ	WLCSP
64	Winbond	W25Q64JWSSIQ	WLCSP
512	GigaDevice	GD25LB512MEYIG	WSON
3.3V Compatible Devices			
8	Macronix	MX25R8035FBHIH2	WLCSP

The controller can potentially support other standard/dual/quad SPI serial flash devices besides those shown in Table 7-17, provided that they have a similar feature set as shown in Table 7-18.

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Table 7-18. Feature Requirements for Serial Flash Device Compatibility with DLPC84x4

FEATURE	REQUIREMENT FOR COMPATIBILITY WITH DLPC84x4	COMMENTS
SPI data configuration (width)	Standard (SingleWire), Dual (Two Wire), Quad (Four Wire)	
SPI clocking mode	SPI mode 0	
SPI clock frequency	up to 60MHz	
Clock (↓) to Output Valid time	6ns (max)	for example, t_V or t_{CLQV}
Fast READ addressing	Auto-incrementing	
Programming mode	Page mode	
Page size	256 Bytes	
Sector (or Subsector) size	4KB	Requirederase granularity
Block structure	Uniform sector / Subsector	
Block protection (BP) bits	Disabled (that is, '0') by default	
Status register bit(0)	Write In Progress (WIP) / BUSY	
Status register bit(1)	Write enable latch (WEN)	
Status register bits(4:2)	Block Protection bits (BP[2:0])	
Status register bit(7)	Status register write protect (SRWP)	
Other Status Register bits	No specific status register bit assignment(s) required. "Other" status register bits often lack common/ standard implementation details across vendors/ devices. These "other" status register bits/signals can potentially be supported, although generally by the main application only (that is, particularly for devices not listed in Table 7-17).	for example, Quad Enable

For compatibility with the controller, serial flash devices must also support the following set of common commands.

Table 7-19. Common Command Set Supported by DLPC84x4 Compatible Serial Flash Devices

SPI FLASH COMMAND	FIRST BYTE (OP-CODE)	SECOND BYTE	THIRD BYTE	FOURTH BYTE	FIFTH BYTE	SIXTH BYTE	NO. OF DUMMY CLOCKS	COMMENTS
Fast READ (1-1-1)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)	8	Variable data payload
Dual READ (1-1-2)	0x3B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)	8	Variable data payload
2X READ (1-2-2)	0xBB	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)	4	Variable data payload
Quad READ (1-1-4)	0x6B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)	8	Variable data payload
4X READ (1-4-4)	0xEB	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0)	6	Variable data payload
Read status	0x05	STATUS(0)					0	STATUS(0) Reg: bit 1 = WEL bit 0 = WIP/BUSY
Write status	0x01	STATUS(0)					0	
Write Enable	0x06						0	
Write Disable	0x04						0	
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0)	DATA(1)	0	256 byte data payload
Sector/Subsector Erase (4KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)			0	
Block Erase (64KB)	0xD8	ADDRS(0)	ADDRS(1)	ADDRS(2)			0	
Full Chip Erase	0xC7						0	

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Table 7-19. Common Command Set Supported by DLPC84x4 Compatible Serial Flash Devices (continued)

SPI FLASH COMMAND	FIRST BYTE (OP-CODE)	SECOND BYTE	THIRD BYTE	FOURTH BYTE	FIFTH BYTE	SIXTH BYTE	NO. OF DUMMY CLOCKS	COMMENTS
Software Reset Enable	0x66						0	
Software Reset	0x99						0	
Read Id	0x9F	Data(0)	Data(1)	Data(2)			0	System only reads 1st three bytes.

SPI data configuration details associated with the various READ commands in the common command set are summarized in Table 7-20.

Table 7-20. Supported READ Command Protocol Implementation Details

READ COMMAND	SPI DATA I/O CONFIG FOR OPCODE (# Clocks)	SPI DATA I/O CONFIG FOR ADDRESS (# Clocks)	NUMBER OF DUMMY CLOCKS	SPI DATA I/O CONFIG FOR READ DATA (# Clocks)
Fast Read (1-1-1)	Standard (8)	Standard (8/byte)	8	Standard (8/byte)
Dual Read (1-1-2)	Standard (8)	Standard (8/byte)	8	Dual (4/byte)
2X Read (1-2-2)	Standard (8)	Dual (4/byte)	4	Dual (4/byte)
Quad Read (1-1-4)	Standard (8)	Standard (8/byte)	8	Quad (2/byte)
4X Read (1-4-4)	Standard (8)	Quad (2/byte)	6	Quad (2/byte)

Host commands issued over the applicable host command interface (that is, I^2C or SPI) can be used to program the serial flash device. The host can also specify target flash clock frequency and read command preferences in the flash table for the controller's embedded software to use based on the system's flash bandwidth requirements.

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7.3.6 GPIO Supported Functionality

The controller provides 52 general-purpose I/O that are available to support a variety of functions for many different product configurations. In general, most of these I/O pins support only one specific function based on a specific product configuration, although that function may be different for a different product configuration. A portion of the unused I/O can also be made available for TI test and debug use. Each of the following GPIO tables provides product-specific details on the allocated use of each of the GPIO for a specific supported product configuration.

Table 7-21. GPIO Supported Functionality—LED Illumination Systems

GPIO	SIGNAL NAME	DESCRIPTION
GPIO_00	SSP1_SCLK (I)	SSP Target
GPIO_01	SSP1_DI (I)	SSP Target
GPIO_02	SSP1_DO (O)	SSP Target
GPIO_03	SSP1_CSZ0 (I)	SSP Target
GPIO_04	SSP1_CSZ1 (I)	SSP Target
GPIO_05	SSP1_CSZ2 (I)	SSP Target
GPIO_06	SSP1_BCSZ (I)	SSP Target
GPIO_07	IIC1_SCL (B)	I2C Target
GPIO_08	IIC1_SDA (B)	I2C Target
GPIO_09	WPC_COLOR_SENSOR_VSYNC (O)	White Point Correction Sync
GPIO_10	UART1_TXD (O)	
GPIO_11	UART1_RXD (I)	
GPIO_12	RC_CHARGE (O)	
GPIO_13	LED_SEL0 (O)	
GPIO_14	LED_SEL1 (O)	
GPIO_15	General Purpose Input/Output	
GPIO_16	General Purpose Input/Output	
GPIO_17	General Purpose Input/Output	
GPIO_18	General Purpose Input/Output	
GPIO_19	General Purpose Input/Output	
GPIO_20	General Purpose Input/Output	
GPIO_21	3D LR (I)	For 3D applications: Left or right 3D reference (left = 1, right = 0). To be provided by the host when a 3D command is not provided. Must transition in the middle of each frame (no closer than 1ms to the active edge of VSYNC)
GPIO_22	General Purpose Input/Output	
GPIO_23	LL_FAULT (O)	Fault signal used for status on system faults where command handling may not be available
GPIO_24	General Purpose Input/Output	
GPIO_25	CMP_MSEL_0/THERM_PWR (O)	
GPIO_26	CMP_PWM (O)	
GPIO_27	CMP_OUT (I)	
GPIO_28	LS_PWR (O)	
GPIO_29	General Purpose Input/Output	
GPIO_30	General Purpose Input/Output	
GPIO_31	General Purpose Input/Output	
GPIO_32	General Purpose Input/Output	

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Table 7-21. GPIO Supported Functionality—LED Illumination Systems (continued)

GPIO	SIGNAL NAME	DESCRIPTION
GPIO_33	General Purpose Input/Output	
GPIO_34	General Purpose Input/Output	
GPIO_35	CAL_PWR (O)	
GPIO_36	General Purpose Input/Output	
GPIO_37	General Purpose Input/Output	
GPIO_38	General Purpose Input/Output	
GPIO_39	USB Select (O)	
GPIO_40	4 way XPR (O)	
GPIO_41	4 way XPR (O)	
GPIO_42	4 way XPR (O)	
GPIO_43	4 way XPR (O)	
GPIO_44	4 way XPR (O)	
GPIO_45	4 way XPR (O)	
GPIO_46	4 way XPR (O)	
GPIO_47	4 way XPR (O)	
GPIO_48	4 way XPR (O)	
GPIO_49	4 way XPR (O)	
GPIO_50	4 way XPR (O)	
GPIO_51	4 way XPR (O)	

Table 7-22. GPIO Supported Functionality—LED-PWM, RGB Laser, and Laser-Phosphor Illumination Systems

GPIO	SIGNAL NAME	DESCRIPTION
GPIO_00	SSP1_SCLK (I)	SSP Target
GPIO_01	SSP1_DI (I)	SSP Target
GPIO_02	SSP1_DO (O)	SSP Target
GPIO_03	SSP1_CSZ0 (I)	SSP Target
GPIO_04	SSP1_CSZ1 (I)	SSP Target
GPIO_05	SSP1_CSZ2 (I)	SSP Target
GPIO_06	SSP1_BCSZ (I)	SSP Target
GPIO_07	IIC1_SCL (B)	I2C Target
GPIO_08	IIC1_SDA (B)	I2C Target
GPIO_09	WPC_COLOR_SENSOR_VSYNC (O)	White Point Correction Sync
GPIO_10	UART1_TXD (O)	
GPIO_11	UART1_RXD (I)	
GPIO_12	General Purpose Input/Output	
GPIO_13	RED_ENABLE (O)	See Note (1)
GPIO_14	GREEN_ENABLE (O)	See Note (1)
GPIO_15	BLUE_ENABLE (O)	See Note (1)
GPIO_16	General Purpose Input/Output	
GPIO_17	General Purpose Input/Output	
GPIO_18	General Purpose Input/Output	
GPIO_19	General Purpose Input/Output	
GPIO_20	General Purpose Input/Output	

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Table 7-22. GPIO Supported Functionality—LED-PWM, RGB Laser, and Laser-Phosphor Illumination Systems (continued)

GPIO	SIGNAL NAME	DESCRIPTION
GPIO_21	3D LR (I)	For 3D applications: Left or right 3D reference (left = 1, right = 0). To be provided by the host when a 3D command is not provided. Must transition in the middle of each frame (no closer than 1ms to the active edge of VSYNC)
GPIO_22	CW_INDEX_0	See Note (2)
GPIO_23	LL_FAULT (O) / CW_PWM_0	Fault signal used to monitor system faults, software command available to provide further details. See Note (2) for CW_PWM_0
GPIO_24	CW_PWM_1	See Note (2)
GPIO_25	RED_PWM (O)	See Note (1)
GPIO_26	GREEN_PWM (O)	See Note (1)
GPIO_27	BLUE_PWM (O)	See Note (1)
GPIO_28	YELLOW_PWM (O)	See Note (2)
GPIO_29	CW_INDEX_1	See Note (2)
GPIO_30	General Purpose Input/Output	
GPIO_31	General Purpose Input/Output	
GPIO_32	General Purpose Input/Output	
GPIO_33	General Purpose Input/Output	
GPIO_34	General Purpose Input/Output	
GPIO_35	General Purpose Input/Output	
GPIO_36	General Purpose Input/Output	
GPIO_37	General Purpose Input/Output	
GPIO_38	General Purpose Input/Output	
GPIO_39	USB Select (O)	
GPIO_40	4 way XPR (O)	
GPIO_41	4 way XPR (O)	
GPIO_42	4 way XPR (O)	
GPIO_43	4 way XPR (O)	
GPIO_44	4 way XPR (O)	
GPIO_45	4 way XPR (O)	
GPIO_46	4 way XPR (O)	
GPIO_47	4 way XPR (O)	
GPIO_48	4 way XPR (O)	
GPIO_49	4 way XPR (O)	
GPIO_50	4 way XPR (O)	
GPIO_51	4 way XPR (O)	

Notes:

(1) Laser safety features, which may be used depending on customer application, are outside the scope of TI software and are the responsibility of the customer when these signals are used to drive LASER illumination sources.

(2) Applicable only to Laser-Phosphor illumination systems

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7.3.7 Debug Support

The controller contains a test point output port, TSTPT_(7:0), which enables the host to provide controller debug support. For the initial debug operation, the four signals (TSTPT(3:0)) are sampled as inputs approximately 1.5µs after PARKZ goes high (or after a system reset). Once their input state has been sampled and captured, this information is used to set up the initial test mode output state of the TSTPT_(7:0) bus. Table 7-23 defines the test mode selection for a few programmable output states for TSTPT_(7:0). Use the default state of 0000 (defined by the required external pulldown resistors) for normal operation (that is, no debug required).

To enable TI to use this debug capability, providing the option of a jumper to an external pullup is recommended for TSTPT(3:0), as well as providing access to allow observation of the TSTPT bus outputs.

Table 7-23. Examples of Test Mode Selection Outputs Defined by TSTPT(3:0)

TSTPT_(7:0) OUTPUT	TSTPT(3:0) CAPTURED VALUES[1]		
	0000 (DEFAULT) (NO SWITCHING ACTIVITY)	0101 CLOCK DEBUG	1000 SYSTEM CALIBRATION
TSTPT(0)	0	HIGH	Vertical Sync
TSTPT(1)	0	166.25MHz	Delayed CW Index
TSTPT(2)	0	83.13MHz	Sequence Index
TSTPT(3)	0	41.56MHz	CW Spoke Test Point
TSTPT(4)	0	10.39MHz	CW Revolution Test Point
TSTPT(5)	0	25.16MHz	Reset Sequence Aux Bit 0
TSTPT(6)	0	133.00MHz	Reset Sequence Aux Bit 1
TSTPT(7)	0	HIGH	Reset Sequence Aux Bit 2

(1) These are only the default output selections. The software can reprogram the selection at any time.

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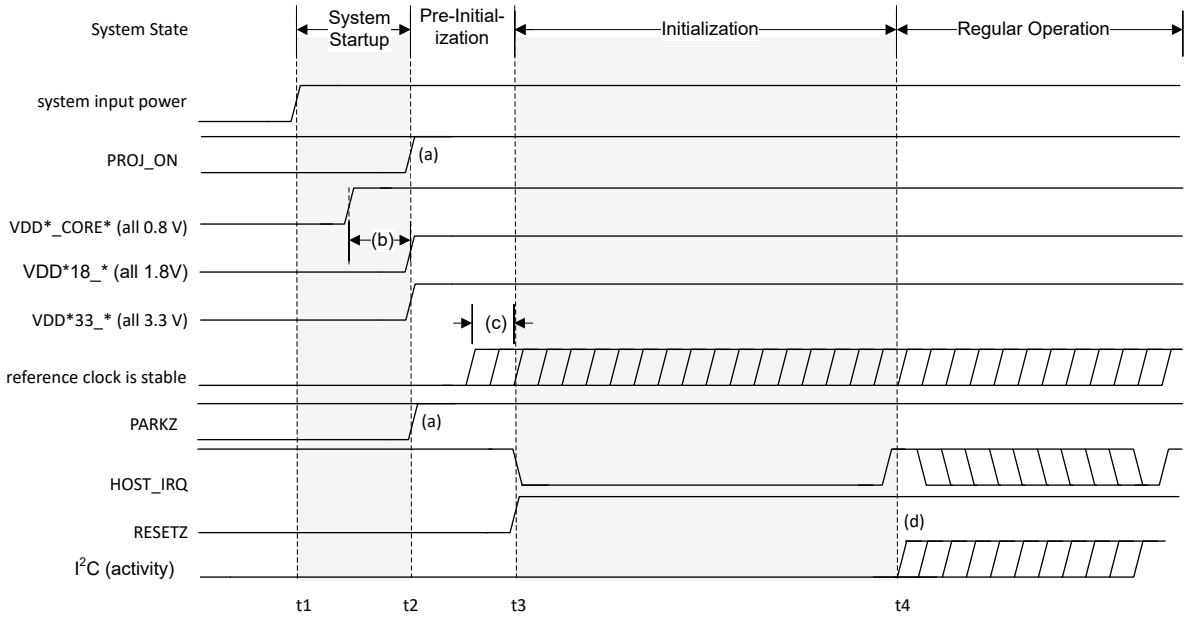
8 Power Supply Recommendations

8.1 System Power-Up and Power-Down Sequence

Although the controller requires an array of power supply voltage pins, there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the controller (this remains true for both power-up and power-down scenarios). The controllers require no minimum delay time between powering up and powering down the individual supplies. Additional power sequencing rules may exist for devices that share supplies with the controller (such as the PMIC and DMD). These devices may force additional system power sequencing requirements. The controller power-up sequence, the normal PARK power-down sequence, and the fast PARK power-down sequence of a typical DLPC system are shown in the following figures.



t1: Power applied to the system. All other voltage rails are derived from system input power.

t2: All supplies reach 95% of their specified nominal value. Note HOST_IRQ is an open-drain output.

t3: Point where RESETZ is deasserted (goes high). This marks the beginning of auto-initialization.

t4: HOST_IRQ goes high to indicate initialization is complete and host communication may begin.

(a): PARKZ and PROJ_ON should be high prior to RESETZ release to support auto-initialization.

(b): $t_{RAMP\text{-}UP\text{-}TOTAL}$, maximum time from 0.8V ramp start to all supplies stable.

(c): t_{REFCLK}, the minimum time reference clock must be stable before releasing RESETZ.

(d): I^2C activity cannot start until HOST_IRQ goes high to indicate auto-initialization is completed.

Figure 8-1. System Power-Up Waveforms (with DLPA3085 or DLPA3082)

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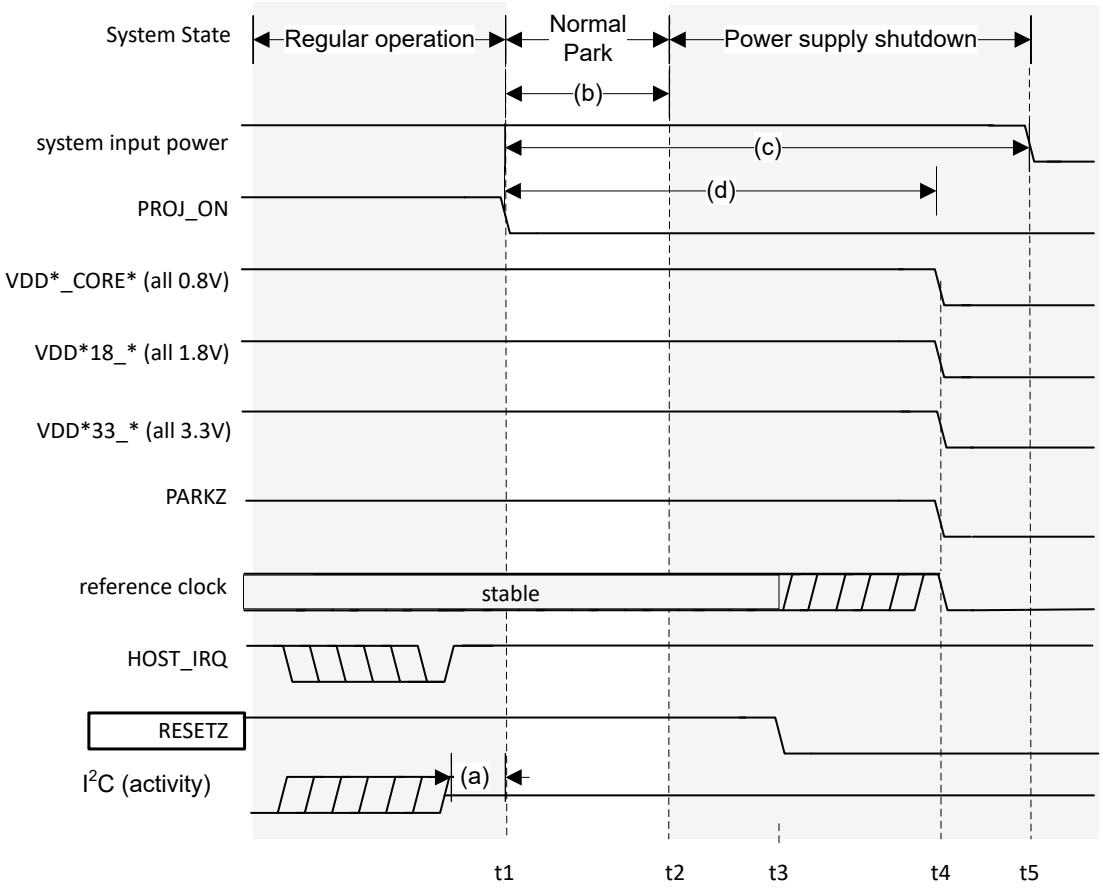

t1: PROJ_ON goes low to begin the power-down sequence.

t2: The controller completes the DMD mirror parking sequence.

t3: RESETZ is asserted, HOST_IRQ goes high.

t4: All controller power supplies are turned off and discharged.

t5: System power can safely be removed.

(a): I^2C activity after PROJ_ON is deasserted (goes low) is not supported.

(b): DMD mirror parking sequence begins when PROJ_ON is deasserted (going low).

(c): It is recommended that system input power be maintained within specifications well after PROJ_ON is deasserted (goes low) to allow time for DMD parking and supplies to fully power down.

(d): DLPA PMIC controls the controller's supply power-down timing.

Figure 8-2. Normal Park Power-Down Waveforms

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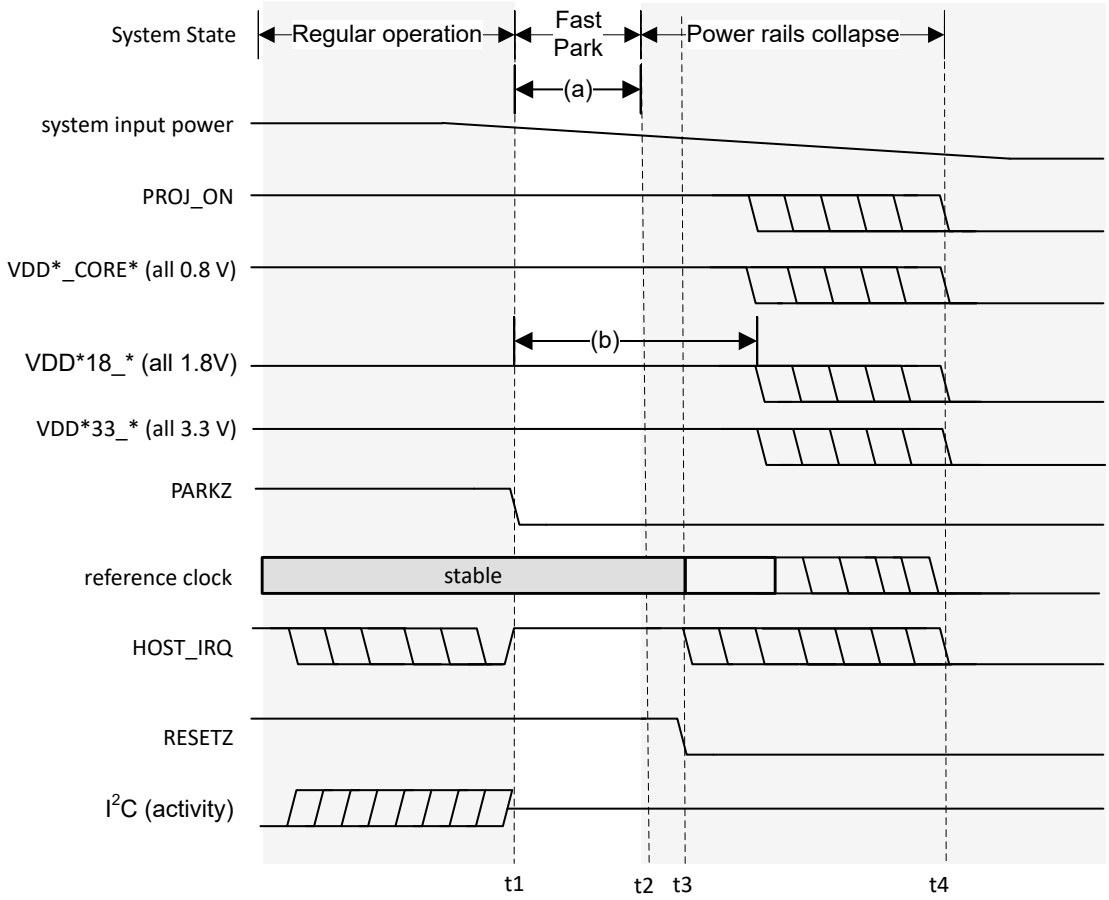

t1: A fault is detected (in this example, the PMIC detects a UVLO condition) and PARKZ is asserted (goes low) to tell the controller to initiate a fast park of the DMD.

t2: The controller finishes the fast park procedure.

t3: RESETZ is asserted, which puts the controller in a reset state that releases HOST_IRQ to a high.

t4: Eventually, all power supplies that were derived from SYSPWR collapse.

(a): All power supplies and the PLL_REFCLK must be held within specification for a minimum of 32µs after PARKZ is asserted (goes low) to protect DMD from possible damage.

(b): The DMD has power sequencing requirements that may impact the timing requirements of a 1.8V supply, refer to the DMD data sheet for more information.

Figure 8-3. Fast Park Power-Down Waveforms

8.2 DMD Fast Park Control (PARKZ)

PARKZ is an input early warning signal that must alert the controller at least 32µs before DC supply voltages drop below specifications. Typically, the PARKZ signal is provided by the DLPA3085 or DLPA3082 interrupt output signal. PARKZ must be deasserted (set high) prior to releasing RESETZ (that is, prior to the low-to-high transition on the RESETZ input) for normal operation. When PARKZ is asserted (set low), the controller performs a Fast Park operation on the DMD, which assists in maintaining the lifetime of the DMD. The reference clock must continue running, and RESETZ must remain deactivated for at least 32µs after PARKZ has been asserted (set low) to allow the park operation to complete.

Fast Park operation is only intended for use when loss of power is imminent and beyond the control of the host processor (for example, when the external power source has been disconnected or the battery has dropped

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below a minimum level). The longest lifetime of the DMD may not be achieved with Fast Park operation. The longest lifetime is achieved with a Normal Park operation. Hence, PARKZ is typically only used instead of a Normal Park request if there is not enough time for a Normal Park. A Normal Park operation takes much longer than 32µs to park the mirrors. During a Normal Park operation, the DLPA3085 or DLPA3082 keeps on all power supplies, and keeps RESETZ high, until the longer mirror parking has completed. Additionally, the DLPA3085 or DLPA3082 may hold the supplies on for a period of time after the parking has been completed. View the relevant DLPA3085 or DLPA3082 data sheet for more information. The longer mirror parking time ensures the longest DMD lifetime and reliability.

8.3 Power Supply Management

The DLPA3085 or DLPA3082 manages power for the controller and DMD. See Section 8.1 for all power sequencing and timing requirements.

8.4 Hotplug Usage

The hotplug expects the power to be stable to the controller; thus, no input source should be transmitted until the power rails are fully powered up. While the V-by-One, FPD-Link, DSI, and USB interfaces support hotplug usage (that is, these interfaces can be connected and disconnected while the controller is powered), and the controller itself (and any DMD connected to the system) do not support hotplug use. As such, power down the system prior to removing the controller or DMD from any system.

8.5 Power Supplies for Unused Input Source Interfaces

While certain product configurations may not offer or make use of all of the available input source interfaces (for example, V-by-One, FPD-Link, DSI), the power supplies that are associated with these unused input source interfaces must still be provided as if the interface is used.

8.6 Power Supplies

8.6.1 Power Supplies DLPA3085 or DLPA3082

The DLPA3085 or DLPA3082 power management IC controller power supplies 0.8V, 1.8V, and 3.3V. Additional filtering must be provided for each uniquely defined power pin (for example, VDD_CORE, VDDR_CORE). Filtering for the power pins is discussed further in Section 9.1 of this document.

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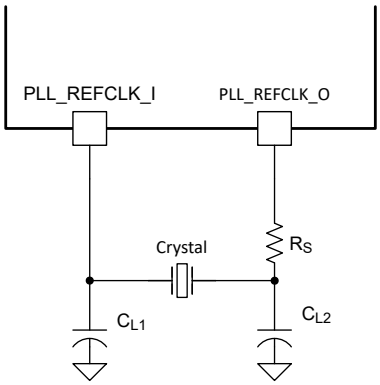
9 Layout

9.1 Layout Guidelines

9.1.1 Layout Guideline for DLPC8424 or DLPC8444 or DLPC8454 Reference Clock

The controller requires two external reference clocks to feed its internal PLLs. A crystal or oscillator can supply these references. The recommended crystal configurations and reference clock frequencies are listed in Discrete Components Required for Crystal, with additional required discrete components shown in Table 9-1.



C_L = Crystal load capacitance

Figure 9-1. Discrete Components Required for Crystal

9.1.1.1 Recommended Crystal Oscillator Configuration

Table 9-1. Recommended Crystal Configurations

PARAMETER	CRYSTAL	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	40	MHz
Crystal frequency tolerance (1)	±100 (200 p-p max)	PPM
Crystal equivalent series resistance (ESR)	60 (Max)	Ω
Crystal load capacitance	20 (Max)	pF
Crystal Shunt Load capacitance	7 (Max)	pF
Temperature range	–40°C to +85°C	°C
Drive level	100 (Nominal)	µW
C_{L1} external crystal load capacitor	See equation in (2)	pF
C_{L2} external crystal load capacitor	See equation in (3)	pF
PCB layout	A ground isolation ring around the crystal is recommended.	

(1) Crystal frequency tolerance to include accuracy, temperature, aging, and trim sensitivity. These are typically specified separately, and the sum of all required to meet this requirement.
(2) CL1 = 2 × (CL – Cstray_pll_refclk_i), where: Cstray_pll_refclk_i = Sum of the package and PCB stray capacitance at the crystal pin associated with the controller pin REFCLKx_I. See Table 9-2.
(3) CL2 = 2 × (CL – Cstray_pll_refclk_o), where: Cstray_pll_refclk_o = Sum of the package and PCB stray capacitance at the crystal pin associated with the controller pin REFCLKx_O. See Table 9-2.

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Table 9-2. Crystal Pin Capacitance

PARAMETER		MIN	NOM	MAX	UNIT
Cstray_pll_refclk_i	Sum of package and PCB stray capacitance at REFCLKA_I		0.4		pF
Cstray_pll_refclk_o	Sum of package and PCB stray capacitance at REFCLKA_O		0.4		pF

The crystal circuits in the DLPC8424 or DLPC8444 or DLPC8454 have dedicated power (VDDS18_OSC) pins, with the recommended filtering for each shown in Figure 9-2, and the recommended values shown in DLPC8424, DLPC8444, and DLPC8454 Recommended Crystal Parts.

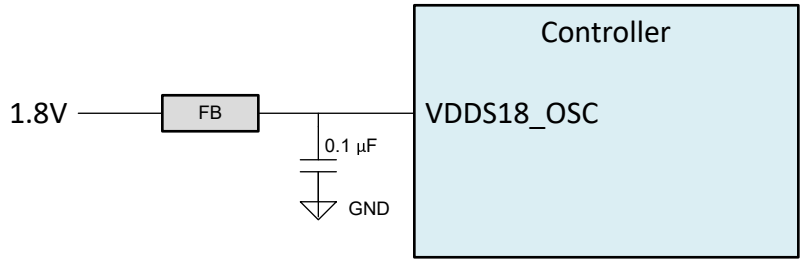

Figure 9-2. Crystal Power Supply Filtering

Table 9-3. DLPC8424, DLPC8444, and DLPC8454 Recommended Crystal Parts

MANUFACT-URER	PART NUMBER	NOMINAL FREQUENCY (MHz)	FREQUENCY TOLERANCE (ppm)	Maximum ESR (Ω)	LOAD CAPACITANCE (pF)	PACKAGE DIMENSIONS (mm)
KDS	DSX1612S	40	±50	50	8	1.6 x 1.2
KDS	DSK211G	40	±50	80	8	2.0 x 1.6
Murata	XRC GB40M00F0L 00R0	40	±200	100	6	2.0 x 1.6
NDK	NX1612SA	40	±25	80	8	1.6 x 1.2
NDK	NX2016SA	40	±35	50	8	2.0 x 1.6

9.1.2 V-by-One Interface Layout Considerations

The DLPC8424, DLPC8444, and DLPC8454 V-by-One SERDES differential interface waveform quality and timing are dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring a positive timing margin requires attention to many factors.

DLPC8424, DLPC8444, and DLPC8454 I/O timing parameters, V-by-One transmitter timing parameters, as well as Thine specific timing requirements, can be found in the corresponding transmitter data sheets. PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB-related requirements for V-by-One are provided in V-by-One Interface PBC Related Requirements as a starting point for the customer.

Table 9-4. V-by-One Interface PBC Related Requirements

PARAMETER(1)	MIN	TYP	MAX	UNIT
Intralane cross-talk (between VX1_DATAx_P and VX1_DATAx_N)			< 1.5	mVpp
Interlane cross-talk (between data lane pairs)			< 1.5	mVpp
Cross-talk between data lanes and other signals			< 1.5	mVpp
Intralane skew			< 40	ps
Inter-lane skew			< 800	ps

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Table 9-4. V-by-One Interface PBC Related Requirements (continued)

PARAMETER(1)	MIN	TYP	MAX	UNIT
Differential Impedance	90	100	110	Ω

(1) If using the minimum trace width and spacing to escape the controller ball field, widening these out after escape is desirable if practical to achieve the target 100Ω impedance (for example, to reduce transmission line losses).

Additional V-by-One layout guidelines:

- Route the differential signal pairs on the top layer of the PBC to minimize the number of vias. Limit the number of necessary vias to two.
- Route differential signal pairs over a single ground or power plane using a microstrip line configuration. Ground guard traces are also recommended.
- Do not route the differential signal pairs over the slit of power or ground planes.
- Minimize the trace length mismatch for each pair and between each pair to meet the skew requirements.
- Ensure that the bend angles associated with the differential signal pairs are between 135° and 225° (see Figure 9-3).

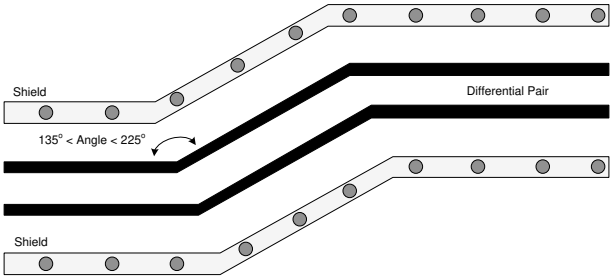

Figure 9-3. V-by-One Routing Example

9.1.3 DMD Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 9-5. Maximum Pin-to-Pin PCB Interconnect Recommendations

DMD BUS SIGNAL(1) (2)	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE-BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	10.0 (254)	See (3)	in (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	10.0 (254)	See (3)	in (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	10.0 (254)	See (3)	in (mm)
DMD_LS_WDATA	10.0 (254)	See (3)	in (mm)

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Table 9-5. Maximum Pin-to-Pin PCB Interconnect Recommendations (continued)

DMD BUS SIGNAL[1] [2]	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE-BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_LS_RDATA	10.0 (254)	See [3]	in (mm)
DMD_DEN_ARSTZ	10.0 (254)	See [3]	in (mm)

(1) The maximum signal routing length includes escape routing.
(2) Multiboard DMD routing length is more restricted due to the impact of the connector.
(3) Due to PCB variations, these recommendations cannot be defined. Any board design should SPICE simulate the controller IBIS model (found under the *Tools & Software* tab of the controller web page) so that routing lengths do not violate signal requirements.

Table 9-6. High-Speed PCB Signal Routing Matching Requirements

SIGNAL GROUP LENGTH MATCHING[1] [2] [3]				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH[4]	UNIT
DMD[5]	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	in (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	in (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	in (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	in (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	in (mm)

(1) The length-matching values apply to PCB routing lengths only. Internal package routing mismatch associated with the DLPC84x4 controller or the DMD requires no additional consideration.
(2) Training is applied to DMD HS data lines. This is why the defined matching requirements are slightly relaxed compared to the LS data lines.
(3) DMD LS signals are single-ended.
(4) Mismatch variance for a signal group is always with respect to the reference signal.
(5) DMD HS data lines are differential; thus, these specifications are pair-to-pair.

Table 9-7. Signal Requirements

PARAMETER	REFERENCE	REQUIREMENT
Source series termination	DMD_LS_WDATA	Required 33Ω ±10%
	DMD_LS_CLK	Required 33Ω ±10%
	DMD_DEN_ARSTZ	Acceptable
	DMD_LS_RDATA	Required 30.1Ω ±10%
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable

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Table 9-7. Signal Requirements (continued)

PARAMETER	REFERENCE	REQUIREMENT
Endpoint termination	DMD_LS_WDATA	Not acceptable
	DMD_LS_CLK	Not acceptable
	DMD_DEN_ARSTZ	Not acceptable
	DMD_LS_RDATA	Not acceptable
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
PCB impedance	DMD_LS_WDATA	50Ω ±10%
	DMD_LS_CLK	50Ω ±10%
	DMD_DEN_ARSTZ	50Ω ±10%
	DMD_LS_RDATA	50Ω ±10%
	DMD_HS_WDATA_x_y	100Ω ±10%
	DMD_HS_CLK_y	100Ω ±10%
Signal type	DMD_LS_WDATA	SDR (single data rate) referenced to DMD_LS_DCLK
	DMD_LS_CLK	SDR referenced to DMD_LS_DCLK
	DMD_DEN_ARSTZ	SDR
	DMD_LS_RDATA	SDR referenced to DMD_LS_DLCK
	DMD_HS_WDATA_x_y	SubLVDS
	DMD_HS_CLK_y	SubLVDS

9.1.4 Power Supply Layout Guidelines

The following filtering circuits are recommended for the power supply inputs listed below.

- VDDA18_Vx1
- VDDA18_FPD
- VDDA18_DSI
- VDDA33_USB
- VDDA18_USB
- VDD_CORE_Vx1
- VDD_CORE_FPD
- VDD_CORE_DSI
- VDD_CORE_USB

Because the PBC layout is critical to the performance of the interfaces associated with these power supplies, it is vital that these power supplies be treated like an analog signal. Specifically:

- Place high-frequency components (such as ferrites and capacitors) as close to the power ball(s) as possible.
- Choose high-frequency ceramic capacitors (such as those with a value of 0.1µF, 0.01µF, and 100nF) that have low ESR and ESL values. Design the leads as short as possible, and as such, it is recommended that these capacitors be placed under the package on the opposite side of the board.
- For each power pin, a single trace (as wide as possible) must be used from the controller to the capacitor and then through the series ferrite to the power source.
- For each power pin, add a 100nF decoupling capacitor placed near the escape via. Add this decoupling capacitance to the capacitance recommended for filters. These are minimum recommendations, so different layouts may require additional capacitance.

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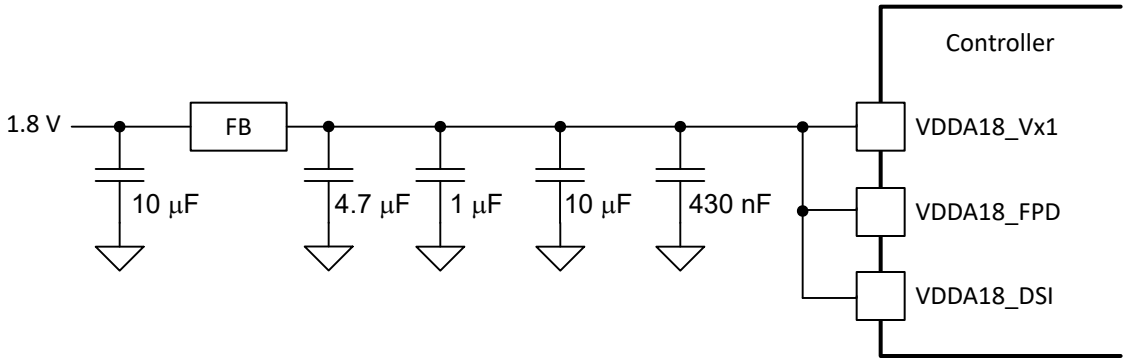

Figure 9-4. VDDA18_VX1 (V-by-One), VDDA18_FPD (FPD-Link), VDDA18_DSI (DSI) Recommended Filter

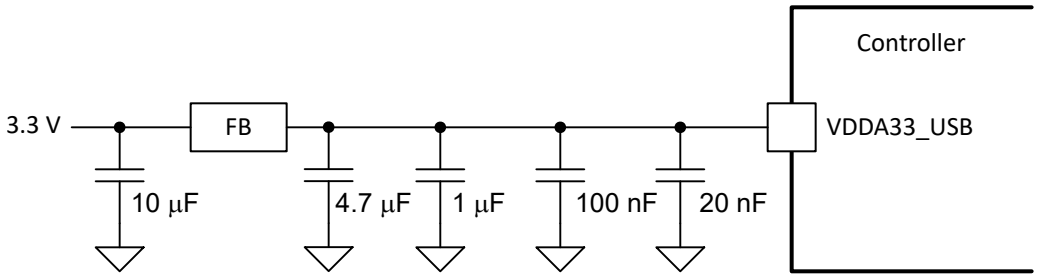

Figure 9-5. VDDA33_USB (USB) Recommended Filter

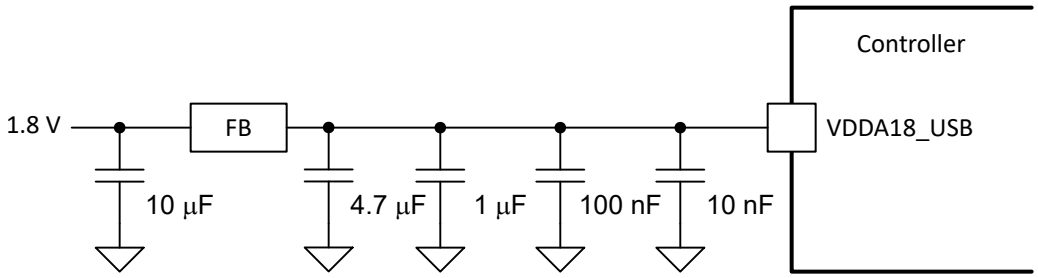

Figure 9-6. VDDA18_USB (USB) Recommended Filter

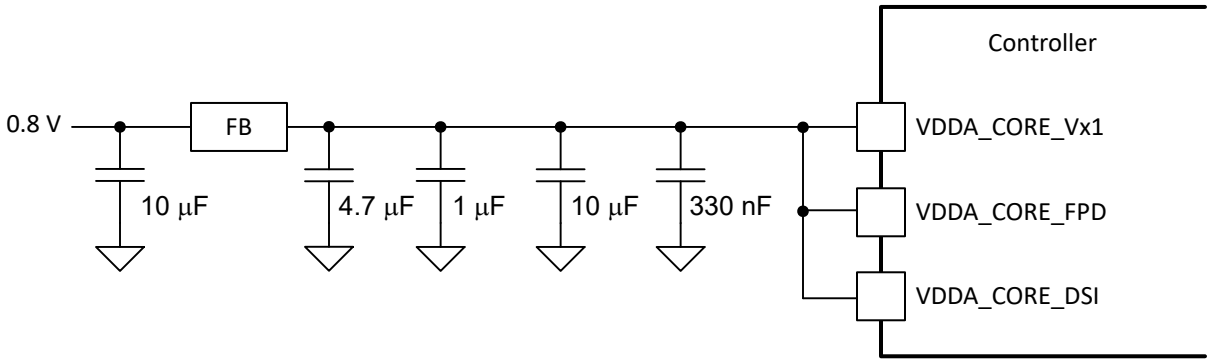

Figure 9-7. VDD_CORE_VX1 (V-by-One), VDD_CORE_FPD (FPD-Link), VDD_CORE_DSI (DSI) Recommended Filter

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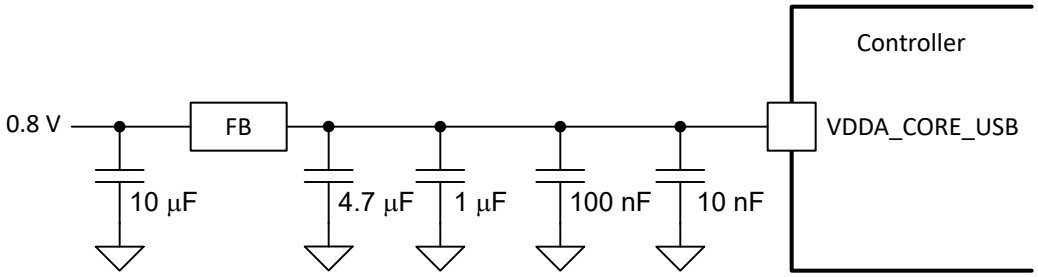

Figure 9-8. VDD_CORE_USB (USB) Recommended Filter

9.2 Thermal Considerations

The underlying thermal requirement for the DLPC8424 or DLPC8444 or DLPC8454 is that the maximum operating junction temperature (T_J) should not be exceeded (defined in the *Recommended Operating Conditions*). This temperature is dependent on the operating ambient temperature, heatsink, airflow, PCB design (including the component layout density and the amount of copper used), the power dissipation of the DLPC8424 or DLPC8444 or DLPC8454, and the power dissipation of surrounding components. The DLPC8424 or DLPC8444 or DLPC8454's package is designed to extract heat through the package heat slug to the heatsink, through the thermal balls, and through the power and ground planes of the PCB. Thus, heatsink, copper content, and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on the maximum DLPC8424 or DLPC8444 or DLPC8454 power dissipation and $R_{\theta JA}$ at 0m/s, 1m/s, and 2m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using the test board described in *Layout Guidelines*. This test PCB is not necessarily representative of the customer's PCB, and thus, the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. TI highly recommends that once the host PCB is designed and built, the thermal performance be measured and validated.

To do this, measure the top center case temperature under the worst-case product scenario (max power dissipation, max voltage, max ambient temperature) and validate that the maximum recommended case temperature (T_C) is not exceeded. This specification is based on the measured φ_{JT} for the DLPC8424 or DLPC8444 or DLPC8454 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40-gauge) thermocouple. Ensure that the bead and thermocouple wire contact the top of the package. Cover the bead and thermocouple wire with a minimal amount of thermally conductive epoxy. Route the wires closely along the package and the board surface to avoid cooling the bead through the wires.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- *DLPA3085 PMIC and High-Current LED Driver IC Data Sheet*
- *DLPA3082 PMIC IC Data Sheet*
- *DLP472NP 1080p Digital Micromirror Device Data Sheet*
- *DLP230NP 0.23 1080p Digital Micromirror Device Data Sheet*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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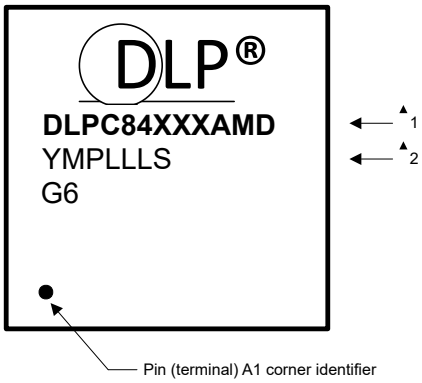
10.5 Device Nomenclature

10.5.1 Device Markings



Marking Definitions:

Line 1:	TI Part Number: Production	DLPC84XXX = Device ID blank or A, B, C ... = Part Revision AMD = Package designator
Line 2:	Vendor Year, Week and Lot code	YM = Year Month Date Code P = Secondary Site Code LLL = Assembly Site Code S = Primary Site
Line 3:	ECAT - Green Package Designator	G6

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Arm® is a registered trademark of Arm Ltd.
DLP® is a registered trademark of Texas Instruments.
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10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10.8.1 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF)	Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.
Active Pixels Per Line (APPL)	Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.
Horizontal Back Porch (HBP) Blanking	Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.
Horizontal Front Porch (HFP) Blanking	Number of blank pixel clocks after the last active pixel but before Horizontal Sync.

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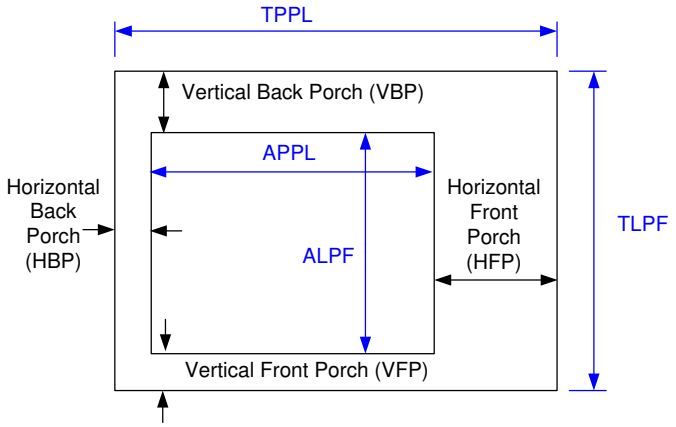
Horizontal Sync (HS)	Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.
Total Lines Per Frame (TLPF)	Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).
Total Pixel Per Line (TPPL)	Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).
Vertical Sync (VS)	Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.
Vertical Back Porch (VBP) Blanking	Number of blank lines after vertical sync but before the first active line.
Vertical Front Porch (VFP) Blanking	Number of blank lines after the last active line but before vertical sync.



11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLPC8424AMD	Active	Production	FCCSP (AMD) | 484	260 | JEDEC TRAY (10+1)	-	Call TI	Level-3-250C-168 HR	-	DLPC8424AMD
DLPC8444AMD	Active	Production	FCCSP (AMD) | 484	260 | JEDEC TRAY (10+1)	-	Call TI	Level-3-250C-168 HR	-	DLPC8444AMD
DLPC8454AMD	Active	Production	FCCSP (AMD) | 484	260 | JEDEC TRAY (10+1)	-	Call TI	Level-3-250C-168 HR	-	DLPC8454AMD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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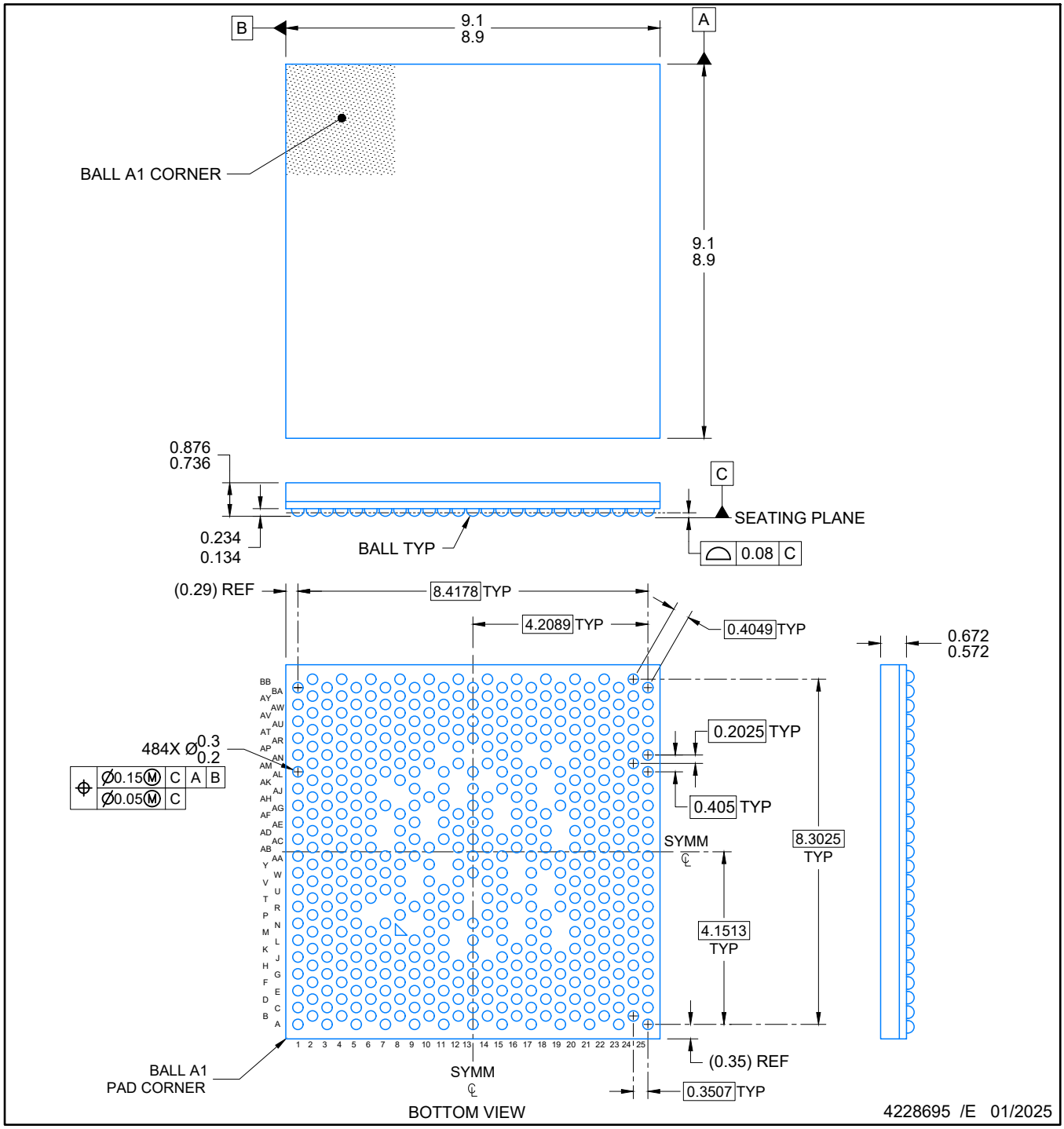
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

AMD0484A

FCCSP - 0.876 mm max height

Flip Chip-Chip Scale Package



NOTES:

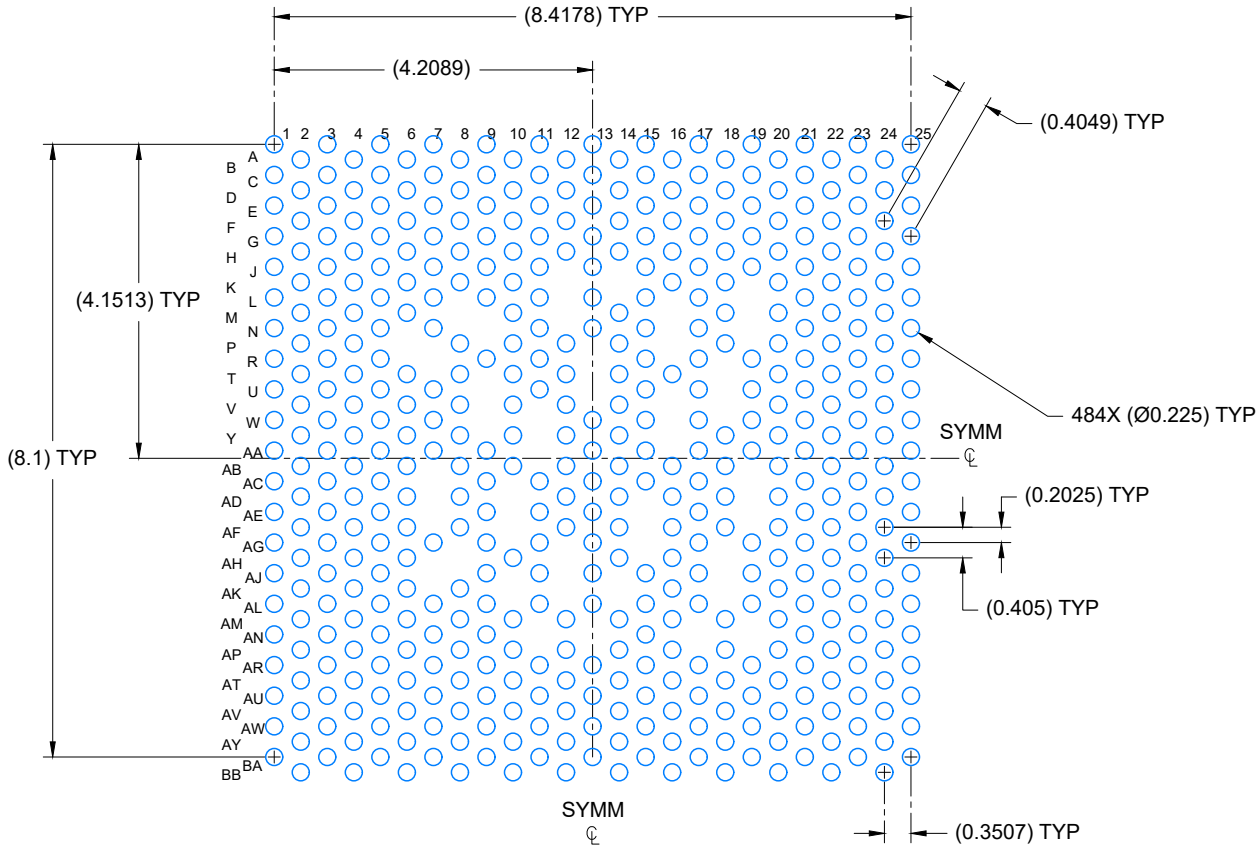
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

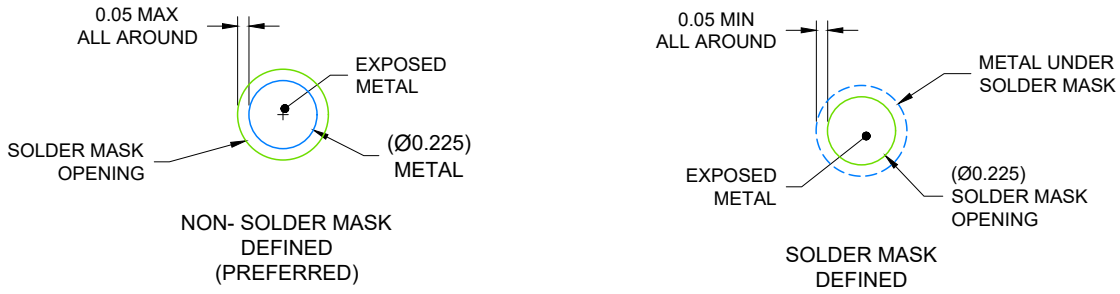
EXAMPLE BOARD LAYOUT

FCCSP - 0.876 mm max height

Flip Chip-Chip Scale Package



LAND PATTERN EXAMPLE
SCALE: 10X



SOLDER MASK DETAILS
NOT TO SCALE

4228695 /E 01/2025

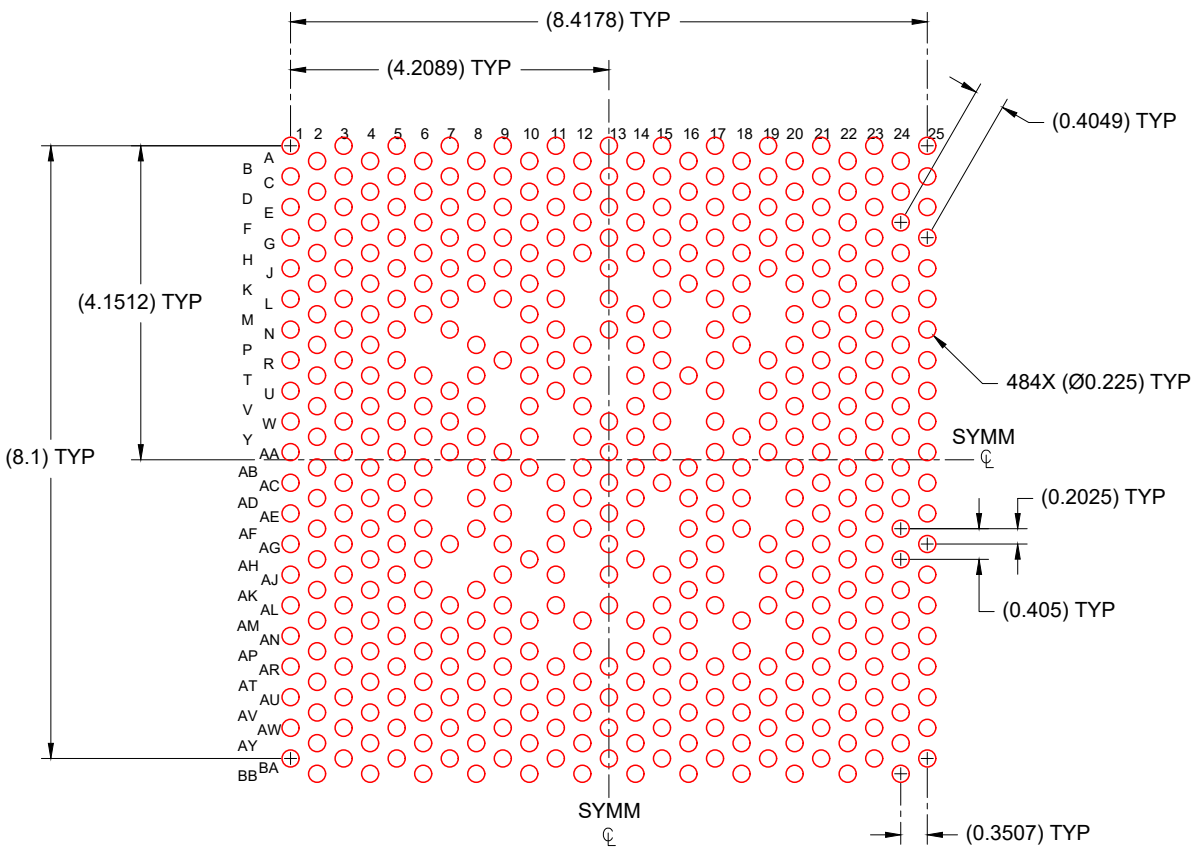
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

FCCSP - 0.876 mm max height

Flip Chip-Chip Scale Package



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4228695 /E 01/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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