# LM5176-Q1 55-V Wide $V_{IN}$ Synchronous 4-Switch Buck-Boost Controller

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: -40°C to 125°C $T_A$
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Single inductor buck-boost controller for step-up/ step-down DC/DC conversion
- Wide $V_{IN}$: 4.2 V (2.5 V with bias) to 55 V (60 V maximum)
- Flexible $V_{OUT}$: 0.8 V to 55 V
- $V_{OUT}$ short protection
- High efficiency buck-boost transition
- Adjustable switching frequency
- Optional frequency sync and dithering
- Integrated 2-A MOSFET gate drivers
- Cycle-by-cycle current limit and optional hiccup
- Optional input or output average current limiting
- Programmable input UVLO and soft-start
- Power good and output overvoltage protection
- Available in HTSSOP-28 package
- Create a custom design using the LM5176-Q1 with the WEBENCH Power Designer

## 2 Applications

- Automotive start-stop systems
- Backup battery and supercapacitor charging
- USB power delivery
- Battery-powered systems
- LED lighting

## 3 Description

The LM5176-Q1 is a synchronous four-switch buck-boost DC/DC controller capable of regulating the output voltage at, above, or below the input voltage. The LM5176-Q1 operates over a wide input voltage range of 4.2 V to 55 V (60 V absolute maximum) to support a variety of applications.

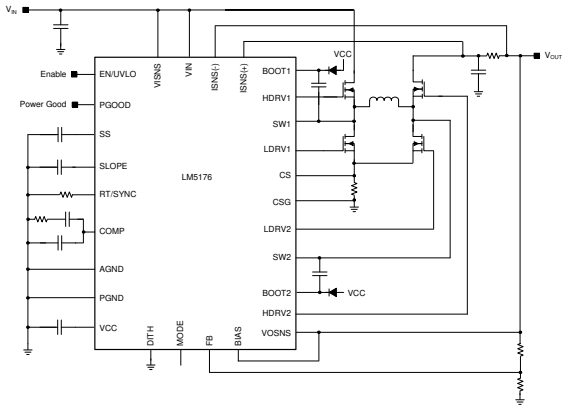
The LM5176-Q1 employs current-mode control both in buck and boost modes of operation for superior load and line regulation. The switching frequency is programmed by an external resistor and can be synchronized to an external clock signal.

The device also features a programmable soft-start function and offers protection features including cycle-by-cycle current limiting, input undervoltage lockout (UVLO), output overvoltage protection (OVP), and thermal shutdown. In addition, the LM5176-Q1 features optional average input or output current limiting, optional spread spectrum to reduce peak EMI, and optional hiccup mode protection in sustained overload conditions.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| LM5176QPWP | HTSSOP-28 | 9.7 mm x 4.4 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Simplified Schematic**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (June 2020) to Revision B (August 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 1 |

| Changes from Revision * (September 2018) to Revision A (June 2020) | Page |
|---|---|
| • Added functional safety bullet to the *Section 1* | 1 |
| • Restructured the *Section 11.1* to meet the current data sheet standards | 32 |


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# 5 Pin Configuration and Functions

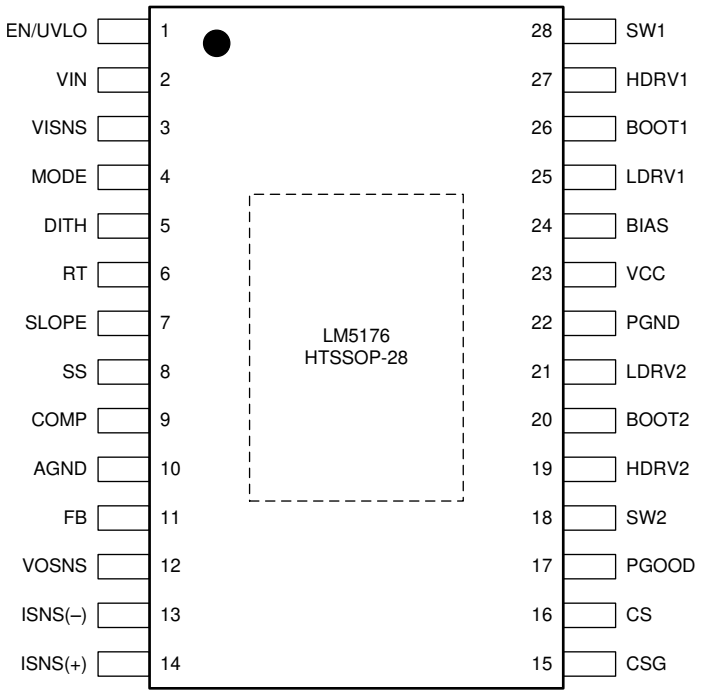


**Figure 5-1. HTSSOP-28 PWP Package Top View**

**Table 5-1. Pin Functions**

| PIN | | DESCRIPTION | |
|---|---|---|---|
| NAME | HTSSOP | | |
| EN/UVLO | 1 | Enable pin. For EN/UVLO < 0.4 V, the LM5176-Q1 is in a low current shutdown mode. For EN/UVLO > 1.22 V, the PWM function is enabled, provided VCC exceeds the VCC UV threshold. | |
| VIN | 2 | The input supply pin to the IC. Connect $V_{IN}$ to a supply voltage between 4.2 V and 55 V. | |
| VISNS | 3 | $V_{IN}$ sense input. Connect to power stage input rail. | |
| MODE | 4 | 1.38 V < MODE < 2.22 V : CCM, Hiccup Enabled | (Set $R_{MODE}$ resistor to AGND = 93.1 kΩ) |
| | | 2.6 V < MODE < VCC: CCM, Hiccup Disabled | (Set $R_{MODE}$ resistor to AGND = 200 kΩ or connect to VCC) |
| DITH | 5 | A capacitor connected between the DITH pin and AGND is charged and discharged with a current source. As the voltage on the DITH pin ramps up and down, the oscillator frequency is modulated by 10% of the nominal frequency set by the RT resistor. Grounding the DITH pin will disable the dithering feature. In the external Sync mode, the DITH pin voltage is ignored. | |
| RT/SYNC | 6 | Switching frequency programming pin. An external resistor is connected to the RT/SYNC pin and AGND to set the switching frequency. This pin can also be used to synchronize the PWM controller to an external clock. | |
| SLOPE | 7 | A capacitor connected between the SLOPE pin and AGND provides the slope compensation ramp for stable current mode operation in both buck and boost mode. | |
| SS | 8 | Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time. | |
| COMP | 9 | Output of the error amplifier. An external RC network connected between COMP and AGND compensates the regulator feedback loop. | |
| AGND | 10 | Analog ground of the IC | |
| FB | 11 | Feedback pin for output voltage regulation. Connect a resistor divider network from the output of the converter to the FB pin. | |
| VOSNS | 12 | $V_{OUT}$ sense input. Connect to the power stage output rail. | |

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**Table 5-1. Pin Functions (continued)**

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | HTSSOP | |
| ISNS(–)<br>ISNS(+) | 13<br>14 | Input or Output Current Sense Amplifier inputs. An optional current sense resistor connected between ISNS(+) and ISNS(–) can be located either on the input side or on the output side of the converter. If the sensed voltage across the ISNS(+) and ISNS(-) pins reaches 50 mV, a slow Constant Current (CC) control loop becomes active and starts discharging the soft-start capacitor to regulate the drop across ISNS(+) and ISNS(-) to 50 mV. Short ISNS(+) and ISNS(-) together to disable this feature. |
| CSG | 15 | The negative or ground input to the PWM current sense amplifier. Connect directly to the low-side (ground) of the current sense resistor. |
| CS | 16 | The positive input to the PWM current sense amplifier |
| PGOOD | 17 | Power-Good open-drain output. PGOOD is pulled low when FB is outside a -9%/+10% regulation window around the 0.8-V $V_{REF}$. |
| SW2<br>SW1 | 18<br>28 | The boost and the buck side switching nodes respectively. |
| HDRV2<br>HDRV1 | 19<br>27 | Output of the high-side gate drivers. Connect directly to the gates of the high-side MOSFETs. |
| BOOT2<br>BOOT1 | 20<br>26 | An external capacitor is required between the BOOT1, BOOT2 pins and the SW1, SW2 pins respectively to provide bias to the high-side MOSFET gate drivers. |
| LDRV2<br>LDRV1 | 21<br>25 | Output of the low-side gate drivers. Connect directly to the gates of the low-side MOSFETs. |
| PGND | 22 | Power ground of the IC. The high current ground connection to the low-side gate drivers. |
| VCC | 23 | Output of the VCC bias regulator. Connect capacitor to ground. |
| BIAS | 24 | Optional input to the VCC bias regulator. Powering VCC from an external supply instead of $V_{IN}$ can reduce power loss at high $V_{IN}$. For $V_{BIAS}$ > 8 V, the VCC regulator draws power from the BIAS pin. |
| PowerPAD™ | - | The PowerPAD should be soldered to the analog ground. If possible, use thermal vias to connect to a PCB ground plane for improved power dissipation. |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

| | MIN(1) | MAX | UNIT |
|---|---|---|---|
| VIN, EN/UVLO, VISNS, VOSNS, ISNS(+), ISNS(–) | –0.3 | 60 | V |
| BIAS | –0.3 | 40 | |
| FB, SS, DITH, RT/SYNC, SLOPE, COMP | –0.3 | 3.6 | |
| SW1, SW2 | –1 | 60 | |
| SW1, SW2 (20 ns transient) | –5.0 | 65 | |
| VCC, MODE, PGOOD | –0.3 | 8.5 | |
| LDRV1, LDRV2 | –0.3 | 8.5 | |
| BOOT1, HDRV1 with respect to SW1 | –0.3 | 8.5 | |
| BOOT2, HDRV2 with respect to SW2 | –0.3 | 8.5 | |
| BOOT1, BOOT2 | –0.3 | 68 | |
| ISNS(+) with respect to ISNS(-) | -0.3 | 0.3 | |
| CS, CSG | –0.3 | 0.3 | |
| Operating junction temperature | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | -65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1)<br>HBM ESD Classification Level 2 | | ±2000 | V |
| | Charged-device model (CDM), per AEC Q100-011<br>CDM ESD Classification Level C4B | All pins | ±500 | |
| | | Corner pins | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VIN | Input bias voltage | 4.2 | | 55 | V |
| VISNS | Input power stage voltage with external bias (BIAS ≥ 5 V or VIN ≥ 4.5 V) | 2.5 | | 55 | |
| BIAS | Bias supply voltage range (when VCC in regulation) | 8 | | 36 | |
| VOSNS | Output voltage range | 0.8 | | 55 | |
| EN/UVLO | Enable voltage range | 0 | | 55 | |
| ISNS(+), ISNS(-) | Average current sense common mode range | 0 | | 55 | |
| $T_J$ | Operating temperature range(2) | –40 | | 150 | °C |
| $F_{sw}$ | Operating frequency range | 100 | | 600 | kHz |

(1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see *Section 6.5* .
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

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## 6.4 Thermal Information

| THERMAL METRIC[1] | | LM5176-Q1 PWP (HTSSOP) 28 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 32.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 21.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 8.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 8.3 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.0 | |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

Typical values correspond to $T_J$ = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. $V_{IN}$ = 24 V unless otherwise stated.[1]

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE ($V_{IN}$)** | | | | | | |
| $I_Q$ | $V_{IN}$ shutdown current | $V_{EN/UVLO}$ = 0 V | | 2.6 | 10 | µA |
| | $V_{IN}$ operating current | $V_{EN/UVLO}$ = 2 V, $V_{FB}$ = 0.9 V | | 2 | 4 | mA |
| **VCC** | | | | | | |
| $V_{VCC(VIN)}$ | Regulation voltage | $V_{BIAS}$ = 0 V, VCC open | 6.95 | 7.35 | 7.88 | V |
| $V_{UV(VCC)}$ | VCC Undervoltage lockout | VCC increasing | 3.11 | 3.27 | 3.43 | |
| | Undervoltage hysteresis | | | 176 | | mV |
| $I_{VCC}$ | VCC current limit | $V_{VCC}$ = 0 V | 65 | | | mA |
| $R_{OUT(VCC)}$ | VCC regulator output impedance | $I_{VCC}$ = 30 mA, $V_{IN}$ = 4 V | | 8 | 16 | Ω |
| **BIAS** | | | | | | |
| $V_{BIAS(SW)}$ | BIAS switchover voltage | $V_{IN}$ = 24 V | 7.25 | 8 | 8.75 | V |
| **EN/UVLO** | | | | | | |
| $V_{EN(STBY)}$ | Standby threshold | EN/UVLO rising | 0.55 | 0.82 | 0.97 | V |
| $I_{EN(STBY)}$ | Standby source current | $V_{EN/UVLO}$ = 1.1 V | 1 | 2 | 3 | µA |
| $V_{EN(OP)}$ | Operating threshold | EN/UVLO rising | 1.17 | 1.22 | 1.29 | V |
| $\Delta I_{HYS(OP)}$ | Operating hysteresis current | $V_{EN/UVLO}$ = 1.5 V | 2.15 | 3.15 | 4.25 | µA |
| **SS** | | | | | | |
| $I_{SS}$ | Soft-start pull up current | $V_{SS}$ = 0 V | 3.75 | 5 | 6.35 | µA |
| $V_{SS(CL)}$ | SS clamp voltage | SS open | | 1.21 | | V |
| $V_{FB}$ - $V_{SS}$ | FB to SS offset | $V_{SS}$ = 0 V | | -18 | | mV |
| **EA (ERROR AMPLIFIER)** | | | | | | |
| $V_{REF}$ | Feedback reference voltage | FB = COMP | 0.788 | 0.800 | 0.812 | V |
| $gm_{EA}$ | Error amplifier gm | | | 1.31 | | mS |
| $I_{SINK}/I_{SOURCE}$ | COMP sink/source current | $V_{FB}$=$V_{REF}$ ± 300 mV | | 280 | | µA |
| $R_{OUT}$ | Amplifier output resistance | | | 20 | | MΩ |
| BW | Unity gain bandwidth | | | 2 | | MHz |
| $I_{BIAS(FB)}$ | Feedback pin input bias current | FB in regulation | | | 25 | nA |
| **FREQUENCY** | | | | | | |
| $f_{SW(1)}$ | Switching Frequency 1 | RT = 40 kΩ | 175 | 200 | 225 | kHz |
| $f_{SW(2)}$ | Switching Frequency 2 | RT = 20 kΩ | 350 | 390 | 430 | |


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Typical values correspond to $T_J$ = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. $V_{IN}$ = 24 V unless otherwise stated.(1)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DITHER** | | | | | | |
| $I_{DITHER}$ | Dither source/sink current | | | 11 | | µA |
| $V_{DITHER}$ | Dither high threshold | | | 1.27 | | V |
| | Dither low threshold | | | 1.16 | | |
| **SYNC** | | | | | | |
| $V_{SYNC}$ | Sync input high threshold | | 2.1 | | | V |
| | Sync input low threshold | | | | 1.2 | |
| $PW_{SYNC}$ | Minimum sync input pulse width | | 50 | | | ns |
| **CURRENT LIMIT** | | | | | | |
| $V_{CS(BUCK)}$ | Buck current limit threshold (Valley) | $V_{IN}$ = $V_{VISNS}$ = 24 V, $V_{VOSNS}$ = 12 V, $V_{SLOPE}$ = 0 V | 66 | 80 | 94 | mV |
| $V_{CS(BOOST)}$ | Boost current limit threshold (Peak) | $V_{IN}$ = $V_{VISNS}$ = 12 V, $V_{VOSNS}$ = 18 V, $V_{SLOPE}$ = 0 V | 100 | 120 | 140 | |
| $I_{BIAS(CS/CSG)}$ | CS/CSG pin bias current | $V_{CS}$ = $V_{CSG}$ = 0 V | | -80 | | µA |
| $I_{OFFSET(CS/CSG)}$ | CSG pin bias current | $V_{CS}$ = $V_{CSG}$ = 0 V | | | 19 | |
| **CONSTANT CURRENT LOOP** | | | | | | |
| $V_{SNS}$ | Average current loop regulation target | $V_{ISNS(-)}$ = 24 V, sweep ISNS(+), $V_{SS}$ = 0.8 V | 43 | 50 | 57 | mV |
| $I_{SNS}$ | ISNS(+)/ISNS(–) pin bias currents | $V_{ISNS(+)}$ = $V_{ISNS(–)}$ = $V_{IN}$ = 24 V | | 3 | | µA |
| Gm | gm of soft-start pull down amplifier | $V_{ISNS(+)}$–$V_{ISNS(–)}$ = 55 mV, $V_{SS}$ = 0.5 V | | 1 | | mS |
| **SLOPE** | | | | | | |
| $I_{SLOPE}$ | Buck adaptive slope current | $V_{IN}$ = $V_{VISNS}$ = 24 V, $V_{VOSNS}$ = 12 V, $V_{SLOPE}$ = 0 V | 24 | 30 | 35 | µA |
| | Boost adaptive slope current | $V_{IN}$ = $V_{VISNS}$ = 12 V, $V_{VOSNS}$ = 18 V, $V_{SLOPE}$ = 0 V | 13 | 17 | 21 | |
| $gm_{SLOPE}$ | Slope compensation amplifier gm | | | 2 | | µS |
| **MODE** | | | | | | |
| $I_{MODE}$ | Source current out of MODE pin | | 17 | 20 | 23 | µA |
| $V_{CCM_HIC}$ | CCM with hiccup threshold | | 1.18 | 1.28 | 1.38 | V |
| $V_{CCM}$ | CCM no hiccup threshold | | 2.22 | 2.4 | 2.6 | V |

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Typical values correspond to $T_J$ = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. $V_{IN}$ = 24 V unless otherwise stated.(1)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PGOOD** | | | | | | |
| $V_{PGD}$ | PGOOD trip threshold for falling FB | Measured with respect to $V_{REF}$ | | –9 | | % |
| | PGOOD trip threshold for rising FB | Measured with respect to $V_{REF}$ | | 10 | | % |
| | Hysteresis | | | 2.5 | | % |
| $I_{LEAK(PGD)}$ | PGOOD leakage current | | | | 100 | nA |
| $I_{SINK(PGD)}$ | PGOOD sink current | $V_{PGOOD}$ = 0.4 V | 2 | 4.2 | 6.5 | mA |
| **OUTPUT OVP** | | | | | | |
| $V_{OVP}$ | Output overvoltage threshold at FB pin | Measured with respect to $V_{REF}$ | | 10 | | % |
| | Hysteresis | | | 2.5 | | % |
| **NMOS DRIVERS** | | | | | | |
| $I_{HDRV1,2}$ | Driver peak source current | $V_{BOOT}$ - $V_{SW}$ = 7 V | | 1.8 | | A |
| | Driver peak sink current | $V_{BOOT}$ - $V_{SW}$ = 7 V | | 2.2 | | |
| $I_{LDRV1,2}$ | Driver peak source current | | | 1.8 | | |
| | Driver peak sink current | | | 2.2 | | |
| $R_{HDRV1,2}$ | Driver pull up resistance | $V_{BOOT}$ - $V_{SW}$ = 7 V | | 1.8 | | Ω |
| | Driver pull down resistance | $V_{BOOT}$ - $V_{SW}$ = 7 V | | 1.1 | | |
| $V_{UV(BOOT1,2)}$ | BOOT1,2 to SW1,2 UVLO threshold | HDRV1,2 shut off | | 3.4 | | V |
| | BOOT1,2 to SW1,2 UVLO hysteresis | HDRV1,2 start switching | | 150 | | mV |
| $R_{LDRV1,2}$ | Driver pull up resistance | | | 1.7 | | Ω |
| | Driver pull down resistance | | | 1.3 | | |
| $t_{DT1}$ | Dead time HDRV1,2 off to LDRV1,2 on | | | 45 | | ns |
| $t_{DT2}$ | Dead time LDRV1,2 off to HDRV1,2 on | | | 45 | | |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Thermal shutdown temperature | | | 165 | | °C |
| $T_{SD(HYS)}$ | Thermal shutdown hysteresis | | | 15 | | |

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.


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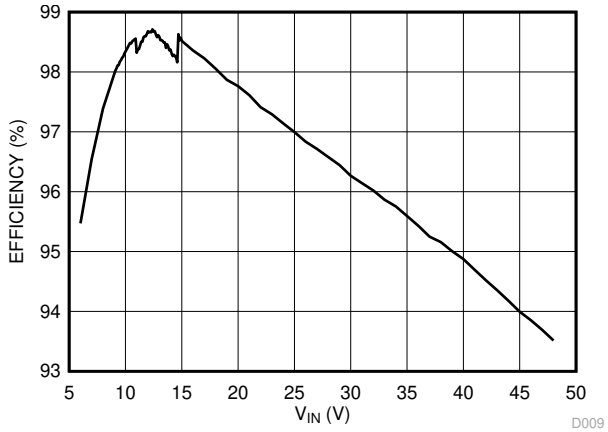
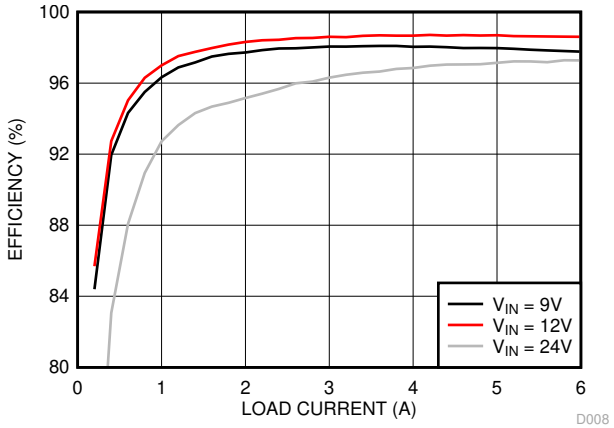
## 6.6 Typical Characteristics

At $T_A$ = 25°C, unless otherwise stated.




$V_{OUT}$ = 12 V  Fsw = 300 kHz  L1 = 4.7 µH
$I_{OUT}$ = 5 A

**Figure 6-1. Efficiency vs $V_{IN}$**




$V_{OUT}$ = 12 V  Fsw = 300 kHz  L1 = 4.7 µH

**Figure 6-2. Efficiency vs Load**

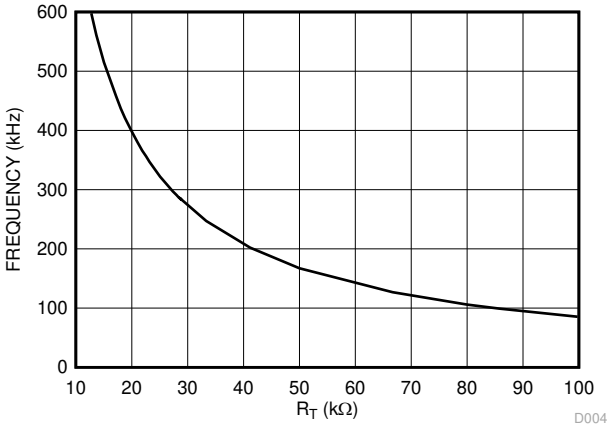



**Figure 6-3. Oscillator Frequency**

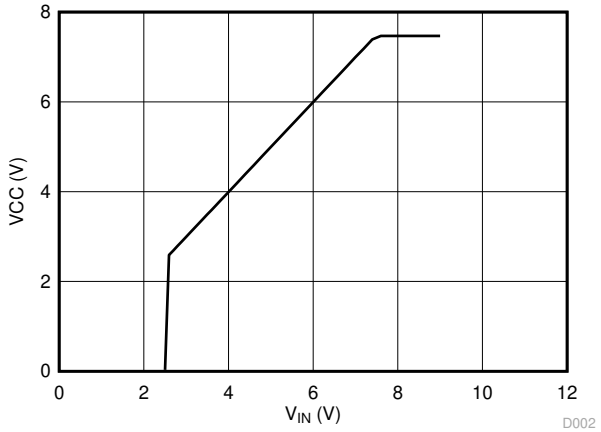



**Figure 6-4. VCC vs $V_{IN}$**

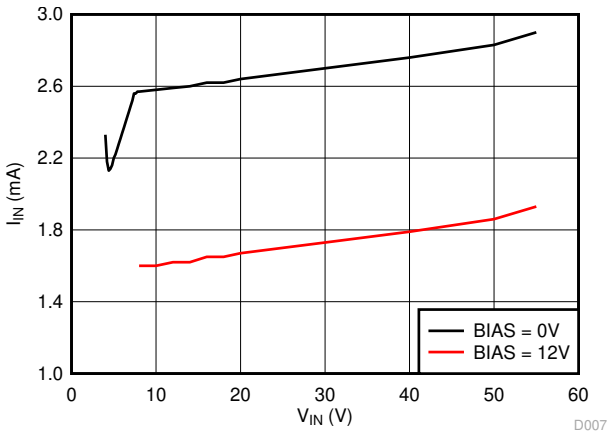



**Figure 6-5. $I_{IN}$ Operating vs $V_{IN}$**

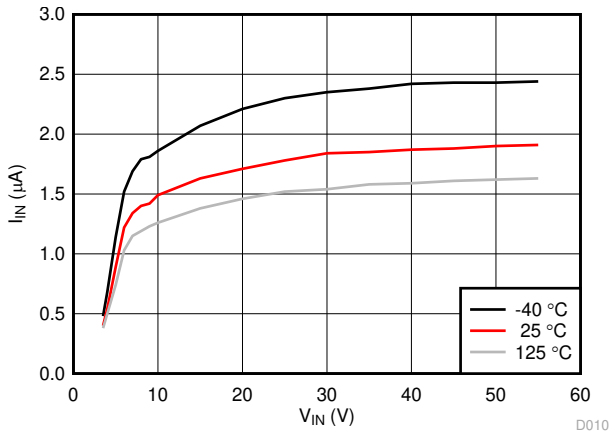



**Figure 6-6. $I_{IN}$ Shutdown vs $V_{IN}$**

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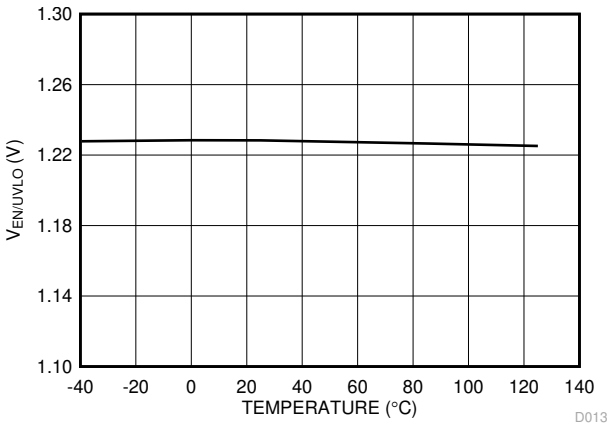



**Figure 6-7. ENABLE/UVLO Rising Threshold vs Temperature**

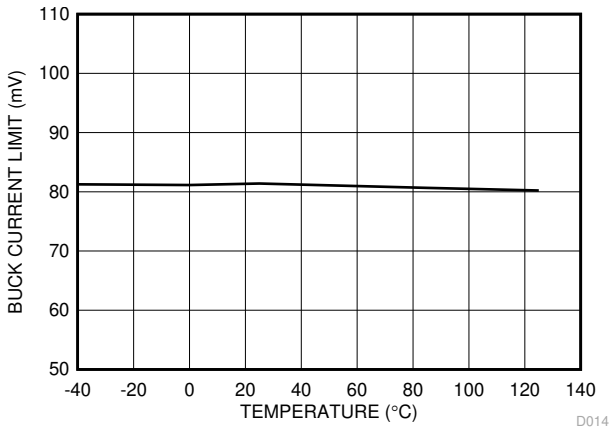



**Figure 6-8. Buck Current Limit vs Temperature**

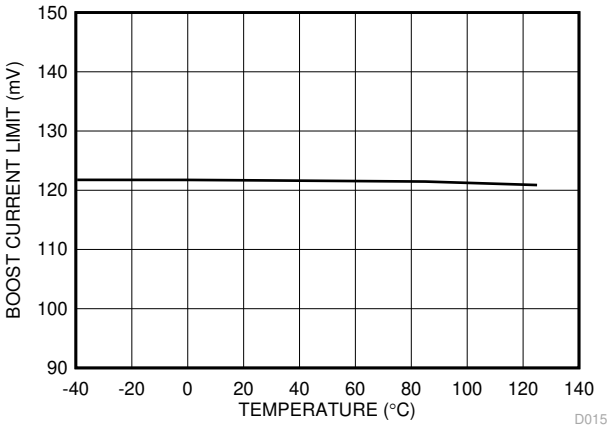
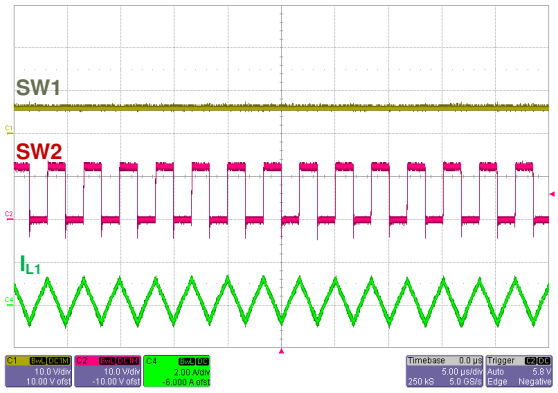
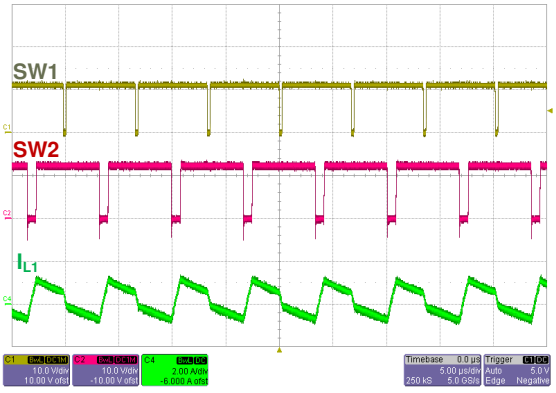



**Figure 6-9. Boost Current Limit vs Temperature**



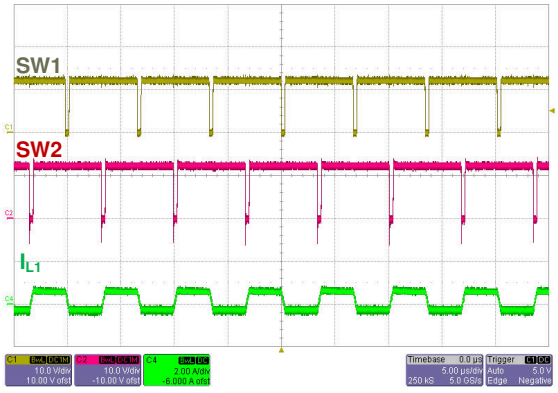

VOUT = 12 V VIN = 6 V

**Figure 6-10. Forced CCM Operation (Boost)**




VOUT = 12 V VIN = 11 V

**Figure 6-11. Forced CCM Operation (Buck-Boost)**




VOUT = 12 V VIN = 12 V

**Figure 6-12. Forced CCM Operation (Buck-Boost)**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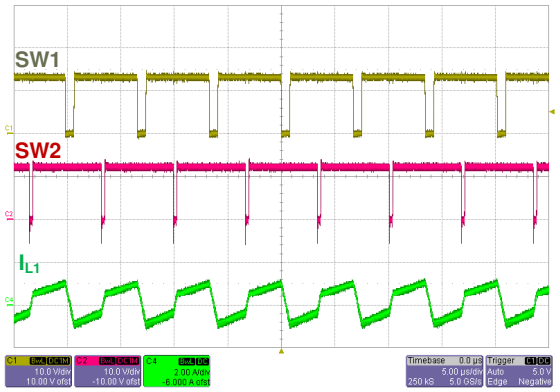
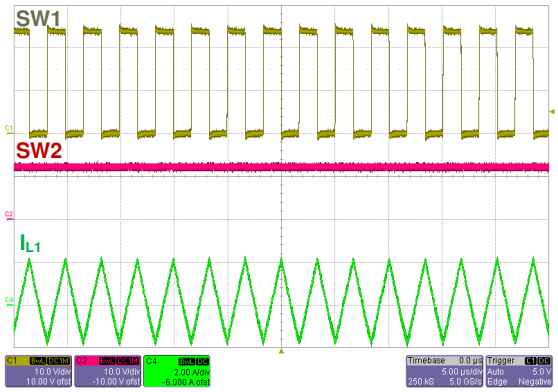


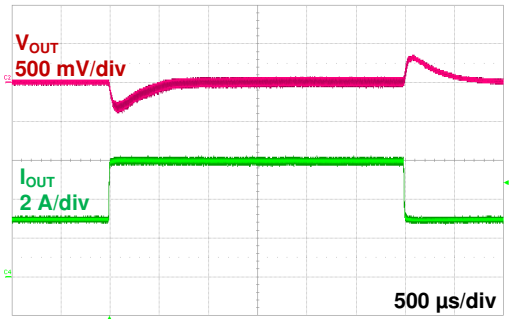

VOUT = 12 V VIN = 13 V

**Figure 6-13. Forced CCM Operation (Buck-Boost)**



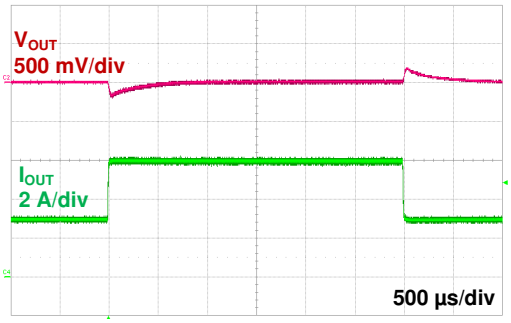

VOUT = 12 V VIN = 24 V

**Figure 6-14. Forced CCM Operation (Buck)**



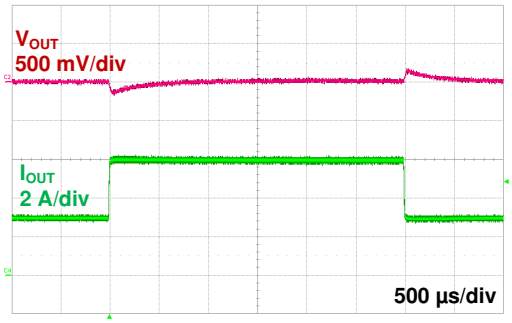

VIN = 6 V VOUT = 12 V Load 3 A to 6 A

**Figure 6-15. Load Step (Boost)**



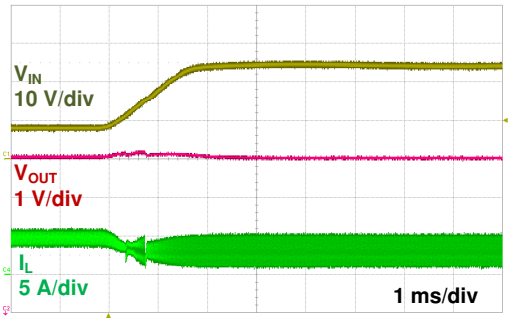

VIN = 12 V VOUT = 12 V Load 3 A to 6 A

**Figure 6-16. Load Step (Buck-Boost)**



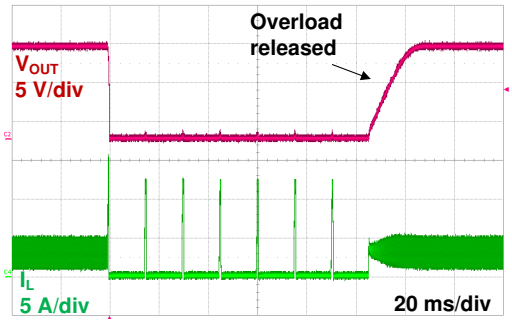

VIN = 24 V VOUT = 12 V Load 3 A to 6 A

**Figure 6-17. Load Step (Buck)**



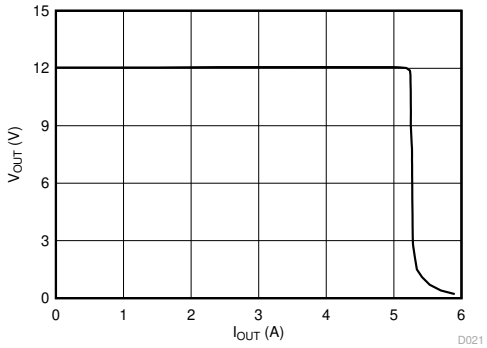

VIN = 8 V to 24 V VOUT = 12 V $I_{OUT}$ = 3 A

**Figure 6-18. Line Transient**




VIN = 24 V VOUT = 12 V Hiccup Enabled

**Figure 6-19. Hiccup Mode Current Limit**




VIN = 24 V RSNS = 10 mΩ

**Figure 6-20. Constant Current Constant Voltage (CCCV) Operation**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# 7 Detailed Description

## 7.1 Overview

The LM5176-Q1 is a wide input voltage four-switch buck-boost controller IC with integrated drivers for N-channel MOSFETs. It operates in buck mode when $V_{IN}$ is greater than $V_{OUT}$ and in boost mode when $V_{IN}$ is less than $V_{OUT}$. When $V_{IN}$ is close to $V_{OUT}$, the device operates in a proprietary transition buck or boost mode. The control scheme provides smooth operation for any input/output combination within the specified operating range. The buck or boost transition control scheme provides a low ripple output voltage when $V_{IN}$ equals $V_{OUT}$ without compromising the efficiency.

The LM5176-Q1 integrates four N-Channel MOSFET drivers including two low-side drivers and two high-side drivers, eliminating the need for external drivers or floating bias supplies. The internal VCC regulator supplies internal bias rails as well as the MOSFET gate drivers. The VCC regulator is powered either from the input voltage through the VIN pin or from the output or an external supply through the BIAS pin for improved efficiency.

The PWM control scheme is based on valley current mode control for buck operation and peak current mode control for boost operation. The inductor current is sensed through a single sense resistor in series with the low-side MOSFETs. The sensed current is also monitored for cycle-by-cycle current limit. The behavior of the LM5176-Q1 during an overload condition is dependent on the MODE pin programming (see the *Section 7.4.2* section). If hiccup mode fault protection is selected, the controller turns off after a fixed number of switching cycles in cycle-by-cycle current limit and restarts after another fixed number of clock cycles. The hiccup mode reduces the heating in the power components in a sustained overload condition. If hiccup mode is disabled through the MODE pin, the controller remains in a cycle-by-cycle current limit condition until the overload is removed.

In addition to the cycle-by-cycle current limiting, the LM5176-Q1 also provides an optional average current regulation loop that can be configured for either input or output current limiting. This is useful for battery charging or other applications where a constant current behavior may be required.

The soft-start time of LM5176-Q1 is programmed by a capacitor connected to the SS pin to minimize the inrush current and overshoot during start-up.

The precision EN/UVLO pin supports programmable input undervoltage lockout (UVLO) with hysteresis. The output overvoltage protection (OVP) feature turns off the high-side drivers when the voltage at the FB pin exceeds the output overvoltage threshold ($V_{OVP}$). The PGOOD output indicates when the FB voltage is inside the PGOOD regulation window centered at $V_{REF}$.

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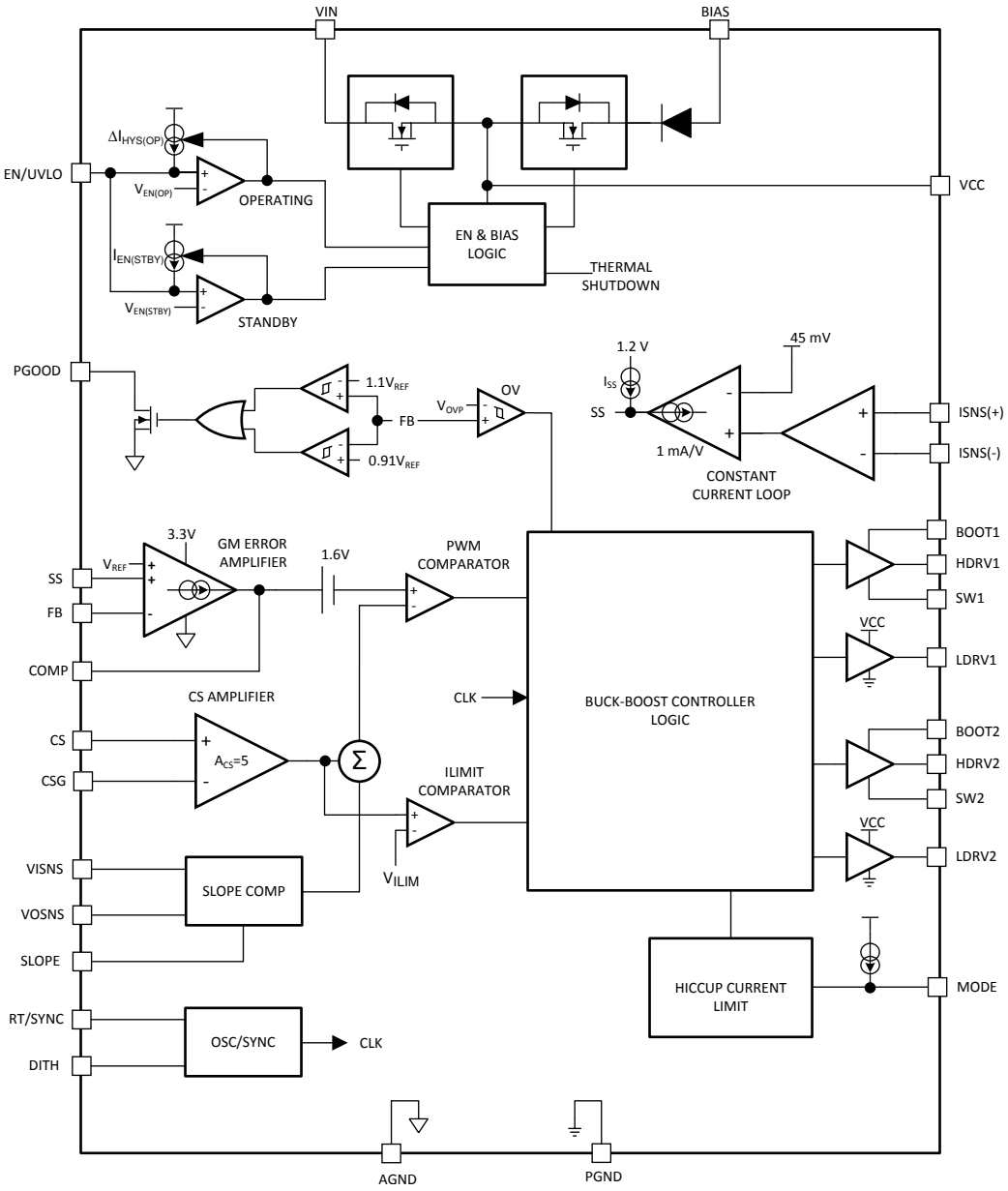
## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Fixed Frequency Valley/Peak Current Mode Control with Slope Compensation

The LM5176-Q1 implements a fixed frequency current mode control of both the buck and boost switches. The output voltage, scaled down by the feedback resistor divider, appears at the FB pin and is compared to the internal reference ($V_{REF}$) by an internal error amplifier. The error amplifier produces an error voltage by driving the COMP pin. An adaptive slope compensation signal based on $V_{IN}$, $V_{OUT}$, and the capacitor at the SLOPE pin is added to the current sense signal measured across the CS and CSG pins. The result is compared to the COMP error voltage by the PWM comparator.

The LM5176-Q1 regulates the output using valley current mode control in buck mode and peak current mode control in boost mode. For valley current mode control, the high-side buck MOSFET controlled by HDRV1 is turned on by the PWM comparator at the valley of the inductor ripple current and turned off by the oscillator clock signal. Valley current mode control is advantageous for buck converters where the PWM controller must resolve very short on-times. For peak current mode control in the boost mode, the low-side boost MOSFET controlled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by LDRV2 is turned on by the clock signal in each switching cycle and turned off by the PWM comparator at the peak of the inductor ripple current.

The low-side gate drive LDRV1, complementary to the HDRV1 drive signal, controls the synchronous rectification MOSFET of the buck stage. The high-side gate drive HDRV2, complementary to the low-side gate drive LDRV2, controls the high-side synchronous rectifier of the boost stage. For operation with $V_{IN}$ close to $V_{OUT}$, the LM5176-Q1 uses a proprietary buck or boost transition scheme to achieve smooth, low ripple transition zone behavior.

Peak and valley current mode controllers require slope compensation for stable current loop operation at duty cycle greater than 50% in peak current mode control and less than 50% in valley current mode control. The LM5176-Q1 provides a SLOPE pin to program optimum slope for any $V_{IN}$ and $V_{OUT}$ combination using an external capacitor.

### 7.3.2 VCC Regulator and Optional BIAS Input

The VCC regulator provides a regulated bias supply to the gate drivers. When EN/UVLO is above the standby threshold ($V_{EN(STBY)}$), the VCC regulator is turned on. For $V_{IN}$ less than the VCC regulation target, the VCC voltage tracks $V_{IN}$ with a small voltage drop as shown in Figure 6-4. If the EN/UVLO input is above the operating threshold ($V_{EN(OP)}$) and VCC exceeds the VCC UV threshold ($V_{UV(VCC)}$), the controller is enabled and switching begins.

The VCC regulator draws power from $V_{IN}$ when there is no supply voltage connected to the BIAS pin. If the BIAS pin is connected to an external voltage source that exceeds VCC by one diode drop, the VCC regulator draws power from the BIAS input instead of $V_{IN}$. Connecting the BIAS pin to $V_{OUT}$ in applications with $V_{OUT}$ greater than 8.5 V improves the efficiency of the regulator in the buck mode.

For low $V_{IN}$ operation, ensure that the VCC voltage is sufficient to fully enhance the MOSFETs. Use an external bias supply if $V_{IN}$ dips below the voltage required to sustain the VCC voltage. For these conditions, use a series blocking diode between the input supply and the VIN pin (Figure 7-1). This prevents VCC from back-feeding into $V_{IN}$ through the body diode of the VCC regulator.

A ceramic capacitor of 16 V or higher voltage rating and a value between 1 µF and 4.7 µF is required to supply the VCC regulator load transients. The VCC bypass capacitor should be connected between VCC and PGND pins.

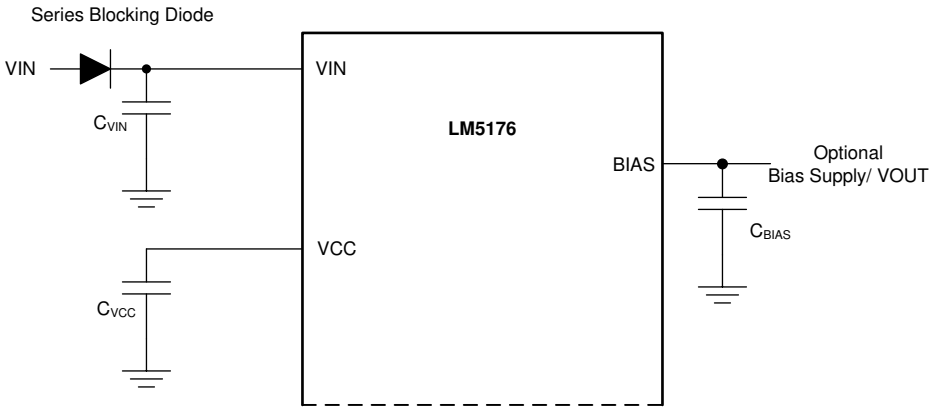


**Figure 7-1. VCC Regulator and Optional BIAS**

### 7.3.3 Enable/UVLO

The LM5176-Q1 has a dual function enable and undervoltage lockout (UVLO) circuit. The EN/UVLO pin has three distinct voltage ranges: shutdown, standby, and operating (see the *Section 7.4.1* section). When the EN/UVLO pin is below the standby threshold, $V_{EN(STBY)}$, the converter is held in a low power shutdown mode. When EN/UVLO voltage is greater than the standby threshold, $V_{EN(STBY)}$ but less than the operating threshold, $V_{EN(OP)}$, the internal bias rails and the VCC regulator are enabled but the soft-start (SS) pin is held low and the PWM controller is disabled. A pullup current $I_{EN(STBY)}$ is sourced out of the EN/UVLO pin in standby mode

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to provide hysteresis between the shutdown mode and the standby mode. When EN/UVLO is greater than the operating threshold $V_{EN(OP)}$ and VCC is above the undervoltage threshold $V_{UV(VCC)}$, the controller starts operation. A hysteresis current, $\Delta I_{HYS(OP)}$, is sourced out of the EN/UVLO pin when the EN/UVLO input exceeds the operating threshold to provide hysteresis that prevents on/off chattering in the presence of noise with a slowly changing input voltage.

The $V_{IN}$ UVLO threshold is typically set by a resistor divider from $V_{IN}$ to AGND (Figure 7-2). The turnon threshold $V_{IN(UV)}$ is calculated using Equation 1 where $R_{UV2}$ is the upper resistor and $R_{UV1}$ is the lower resistor in the EN/UVLO resistor divider:

$$V_{IN(UV)} = V_{EN(OP)} \times \left(1 + \frac{R_{UV2}}{R_{UV1}}\right) - R_{UV2} \times I_{EN(STBY)} \quad (1)$$

The hysteresis between the UVLO turnon threshold and turnoff threshold is set by the upper resistor in the EN/UVLO resistor divider and is given by:

$$\Delta V_{HYS(UV)} = \Delta I_{HYS(OP)} \times R_{UV2} \quad (2)$$

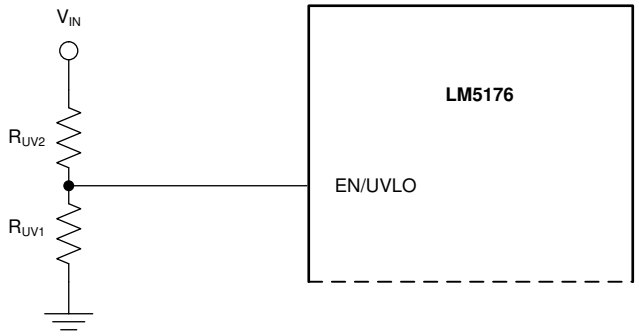


**Figure 7-2. UVLO Threshold Programming**

### 7.3.4 Soft-Start

The LM5176-Q1 soft-start time is programmed using a soft-start capacitor from the SS pin to AGND. When the converter is enabled, an internal current source ($I_{SS}$) charges the soft-start capacitor. When the SS pin voltage is below the feedback reference voltage $V_{REF}$, the soft-start pin controls the regulated FB voltage. Once SS exceeds $V_{REF}$, the soft-start interval is complete and the error amplifier is referenced to $V_{REF}$. The soft-start time is given by Equation 3:

$$t_{ss} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (3)$$

The soft-start capacitor is internally discharged when the converter is disabled because of EN/UVLO falling below the operating threshold or VCC falling below the VCC UV threshold. The soft-start pin is also discharged when the converter is in hiccup mode current limiting or in thermal shutdown. When average input or output current limiting is active, the soft-start capacitor is discharged by the constant current loop transconductance (gm) amplifier to limit either input or output current.

### 7.3.5 Overcurrent Protection

The LM5176-Q1 provides cycle-by-cycle current limit to protect against overcurrent and short circuit conditions. In buck operation, the sensed valley voltage across the CSG and CS pins is limited to $V_{CS(BUCK)}$. The high-side buck switch skips a cycle if the sensed voltage does not fall below this threshold during the buck switch off time. In boost operation, the maximum peak voltage across CS and CSG is limited to $V_{CS(BOOST)}$. If the peak current in the low-side boost switch causes the voltage across CS and CSG to exceed this threshold voltage, the boost switch is turned off for the remainder of the clock cycle.


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Applying the appropriate voltage to the MODE pin of the LM5176-Q1 enables hiccup mode fault protection (see *Section 7.4.2*). In the hiccup mode, the controller shuts down after detecting cycle-by-cycle current limiting for 128 consecutive cycles and the soft-start capacitor is discharged. The soft-start capacitor is automatically released after 4000 oscillator clock cycles and the controller restarts. If hiccup mode protection is not enabled through the MODE pin, the LM5176-Q1 will operate in cycle-by-cycle current limiting as long as the overload condition persists.

### 7.3.6 Average Input/Output Current Limiting

The LM5176-Q1 provides optional average current limiting capability to limit either the input or the output current of the DC/DC converter. The average current limiting circuit uses an additional current sense resistor connected in series with the input supply or output voltage of the converter. A current sense gm amplifier with inputs at the ISNS(+) and ISNS(-) pins monitors the voltage across the sense resistor and compares it with an internal 50-mV reference. If the drop across the sense resistor is greater than 50 mV, the gm amplifier gradually discharges the soft-start capacitor. When the soft-start capacitor discharges below the feedback reference voltage, $V_{REF}$, the output voltage of the converter decreases to limit the input or output current. The average current limiting feature can be used in applications requiring a regulated current from the input supply or into the load. The target constant current is given by Equation 4:

$$I_{CL(AVG)} = \frac{50\ mV}{R_{SNS}} \tag{4}$$

A filter network as shown in Figure 8-1 is often used across ISNS(+) and ISNS(-) pins to filter the ripple in the average current sense signal.

The average current loop can be disabled by shorting the ISNS(+) and ISNS(-) pins together to AGND.

### 7.3.7 Operation Above 40-V Input

For an application where input voltage is higher than 40 V, a 2-kΩ resistor in series with the VISNS pin is required as shown in Figure 8-1.

### 7.3.8 CCM Operation

The LM5176-Q1 works in continuous conduction mode (CCM). In CCM operation, the inductor current can flow in either direction and the controller switches at a fixed frequency regardless of the load current. The CCM operation is useful for noise-sensitive applications where a fixed switching eases filter design.

### 7.3.9 Frequency and Synchronization (RT/SYNC)

The LM5176-Q1 switching frequency can be programmed between 100 kHz and 600 kHz using a resistor from the RT/SYNC pin to AGND. The $R_T$ resistor is related to the nominal switching frequency ($F_{sw}$) by the Equation 5:

$$R_T = \frac{\left(\frac{1}{F_{sw}}\right) - 190\ ns}{116\ pF} \tag{5}$$

Figure 6-3 in the *Section 6.6* shows the relationship between the programmed switching frequency ($F_{sw}$) and the $R_T$ resistor.

The RT/SYNC pin can also be used for synchronizing the internal oscillator to an external clock signal. The external synchronization pulse is ac-coupled using a capacitor to the RT/SYNC pin. The external synchronization pulse frequency range is 75% to 125% of the resistor programmed frequency. A 50% duty cycle is acceptable for external SYNC.

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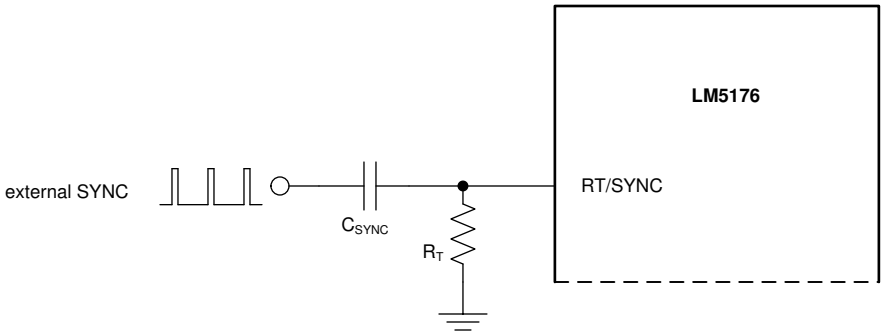


**Figure 7-3. Using External SYNC**

### 7.3.10 Frequency Dithering

The LM5176-Q1 provides an optional frequency dithering function that is enabled by connecting a capacitor from DITH to AGND. Figure 7-4 illustrates the dithering circuit. A triangular waveform centered at 1.22 V is generated across the $C_{DITH}$ capacitor. This triangular waveform modulates the oscillator frequency by 10% of the nominal frequency set by the $R_T$ resistor. The $C_{DITH}$ capacitance value sets the rate of the low frequency modulation. A lower $C_{DITH}$ capacitance will modulate the oscillator frequency at a faster rate than a higher capacitance. For the dithering circuit to effectively reduce peak EMI, the modulation rate must be much less than the oscillator frequency ($F_{sw}$). Equation 6 calculates the DITH pin capacitance required to set the modulation frequency, $F_{MOD}$. Connecting the DITH pin directly to AGND disables frequency dithering, and the internal oscillator operates at a fixed frequency set by the RT resistor. Dither is disabled when external SYNC is used.

$$C_{DITH} = \frac{10\ \mu A}{F_{MOD} \times 0.24\ V} \tag{6}$$

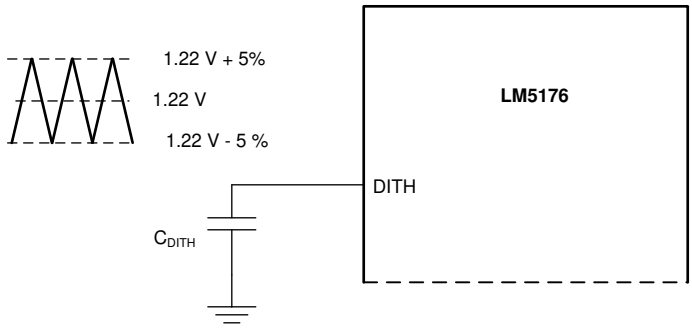


**Figure 7-4. Dither Operation**

### 7.3.11 Output Overvoltage Protection (OVP)

The LM5176-Q1 provides an output overvoltage protection (OVP) circuit that turns off the gate drives when the feedback voltage is above the output overvoltage threshold, $V_{OVP}$. Switching resumes once the feedback voltage falls below the OVP threshold. There is a small hysteresis to prevent chattering.

### 7.3.12 Power Good (PGOOD)

PGOOD is an open-drain output that is pulled low when the voltage at the FB pin is outside -9%/+10% of the nominal $V_{REF}$. The PGOOD internal N-Channel MOSFET pulldown strength is typically 4.2 mA. This pin can be connected to a voltage supply of up to 8 V through a pullup resistor.

### 7.3.13 Gm Error Amplifier

The LM5176-Q1 has a gm error amplifier for loop compensation. The gm amplifier output (COMP) range is 0.3 V to 3 V. Connect an $R_{c1}$-$C_{c1}$ compensation network between COMP and ground for type II (PI) compensation (see Figure 8-1). Another pole is usually added using $C_{c2}$ to suppress higher frequency noise and switching frequency ripple.


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The COMP output voltage ($V_{COMP}$) range limits the possible $V_{IN}$ and $I_{OUT}$ range for a given design. In buck mode, the maximum $V_{IN}$ for which the converter can regulate the output at no load is when $V_{COMP}$ reaches 0.3 V. Equation 7 gives $V_{COMP}$ as a function of $V_{IN}$ at no load in CCM buck mode:

$$V_{COMP(BUCK)} = 1.6\ V - A_{CS} \cdot R_{SENSE} \cdot \frac{V_{OUT}}{2 \cdot L1 \cdot F_{sw}} \cdot (1 - D_{BUCK}) - \frac{2\ \mu S \cdot (V_{IN} - V_{OUT}) + 6\ \mu A}{C_{SLOPE} \cdot F_{sw}} \cdot (1 - D_{BUCK}) \quad (7)$$

Where $D_{BUCK}$ in Equation 7 is the buck duty cycle given by:

$$D_{BUCK} = \frac{V_{OUT}}{V_{IN}} \quad (8)$$

A larger L1, lower slope ripple (higher $C_{SLOPE}$), smaller sense resistor ($R_{SENSE}$), and higher frequency can increase the maximum $V_{IN}$ range for buck operation.

For boost mode, the minimum $V_{IN}$ for which the converter can regulate the output at full load is when $V_{COMP}$ reaches 3 V. Equation 9 gives $V_{COMP}$ as a function of $V_{IN}$ in boost mode:

$$V_{COMP(BOOST)} = 1.6\ V + A_{CS} \cdot R_{SENSE} \cdot \left( I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}}{2 \cdot L1 \cdot F_{sw}} \cdot D_{BOOST} \right) + \frac{2\ \mu S \cdot (V_{OUT} - V_{IN}) + 5\ \mu A}{C_{SLOPE} \cdot F_{sw}} \cdot D_{BOOST} \quad (9)$$

Where $D_{BOOST}$ in the Equation 9 is the boost duty cycle given by:

$$D_{BOOST} = 1 - \frac{V_{IN}}{V_{OUT}} \quad (10)$$

A larger L1, lower slope ripple (higher $C_{SLOPE}$), smaller sense resistor ($R_{SENSE}$), and higher frequency can extend the minimum $V_{I\ N}$ range for boost operation.

### 7.3.14 Integrated Gate Drivers

The LM5176-Q1 provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HDRV1 and HDRV2 pins, and two ground referenced low-side drivers at the LDRV1 and LDRV2 pins. Each driver is capable of sourcing 1.8 A and sinking 2.2-A peak current. In buck operation, LDRV1 and HDRV1 are switched by the PWM controller while HDRV2 remains continuously on. In boost operation, LDRV2 and HDRV2 are switched while HDRV1 remains continuously on.

The low-side gate drivers are powered from VCC and the high-side gate drivers HDRV1 and HDRV2 are powered from bootstrap capacitors $C_{BOOT1}$ (between BOOT1 and SW1) and $C_{BOOT2}$ (between BOOT2 and SW2), respectively. The $C_{BOOT1}$ and $C_{BOOT2}$ capacitors are charged through external Schottky diodes connected to the VCC pin as shown in Figure 8-1.

In most applications, ceramic capacitors of 16 V or higher voltage rating and values between 0.1 µF and 0.22 µF are sufficient for $C_{BOOT1}$ and $C_{BOOT2}$.

### 7.3.15 Thermal Shutdown

The LM5176-Q1 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165°C (typical). The soft-start capacitor is discharged when thermal shutdown is triggered and the gate drivers are disabled. The converter automatically restarts when the junction temperature drops by the thermal shutdown hysteresis of 15°C below the thermal shutdown threshold.

## 7.4 Device Functional Modes

Refer to the *Section 7.3.3* section for the description of EN/UVLO pin function. The *Section 7.4.1* section lists the shutdown, standby, and operating modes for LM5176-Q1 as a function of EN/UVLO and VCC voltages.

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### 7.4.1 Shutdown, Standby, and Operating Modes

| EN/UVLO | VCC | DEVICE MODE |
|---|---|---|
| EN/UVLO < $V_{EN(STBY)}$ | — | Shutdown: VCC off, No switching |
| $V_{EN(STBY)}$ < EN/UVLO < $V_{EN(OP)}$ | — | Standby: VCC on, No switching |
| EN/UVLO > $V_{EN(OP)}$ | VCC < $V_{UV(VCC)}$ | Standby: VCC on, No switching |
| EN/UVLO > $V_{EN(OP)}$ | VCC > $V_{UV(VCC)}$ | Operating: VCC on, Switching enabled |

### 7.4.2 MODE Pin Configuration

The MODE pin is used to select hiccup mode current limit. The MODE selection is based on the voltages at the MODE pin. The MODE voltage is decided by the programming resistor $R_{MODE}$ between MODE and AGND, and the source current out of the MODE pin ($I_{MODE}$). MODE is latched during start-up.

| MODE PIN CONNECTION | HICCUP FAULT PROTECTION |
|---|---|
| $R_{MODE}$ to AGND = 200 kΩ or connect MODE to VCC | No Hiccup |
| $R_{MODE}$ to AGND = 93.1 kΩ | Hiccup Enabled |


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The LM5176-Q1 is a four-switch buck-boost controller. A quick-start tool on the LM5176-Q1 product webpage can be used to design a buck-boost converter using the LM5176-Q1. Alternatively, Webench® software can create a complete buck-boost design using the LM5176-Q1 and generate bill of materials, estimate efficiency, solution size, and cost of the complete solution. The *Section 8.2* describes a detailed step-by-step design procedure for a typical application circuit.

## 8.2 Typical Application

A typical application example is a buck-boost converter operating from a wide input voltage range of 6 V to 50 V and providing a stable 12-V output voltage with current capability of 6 A.

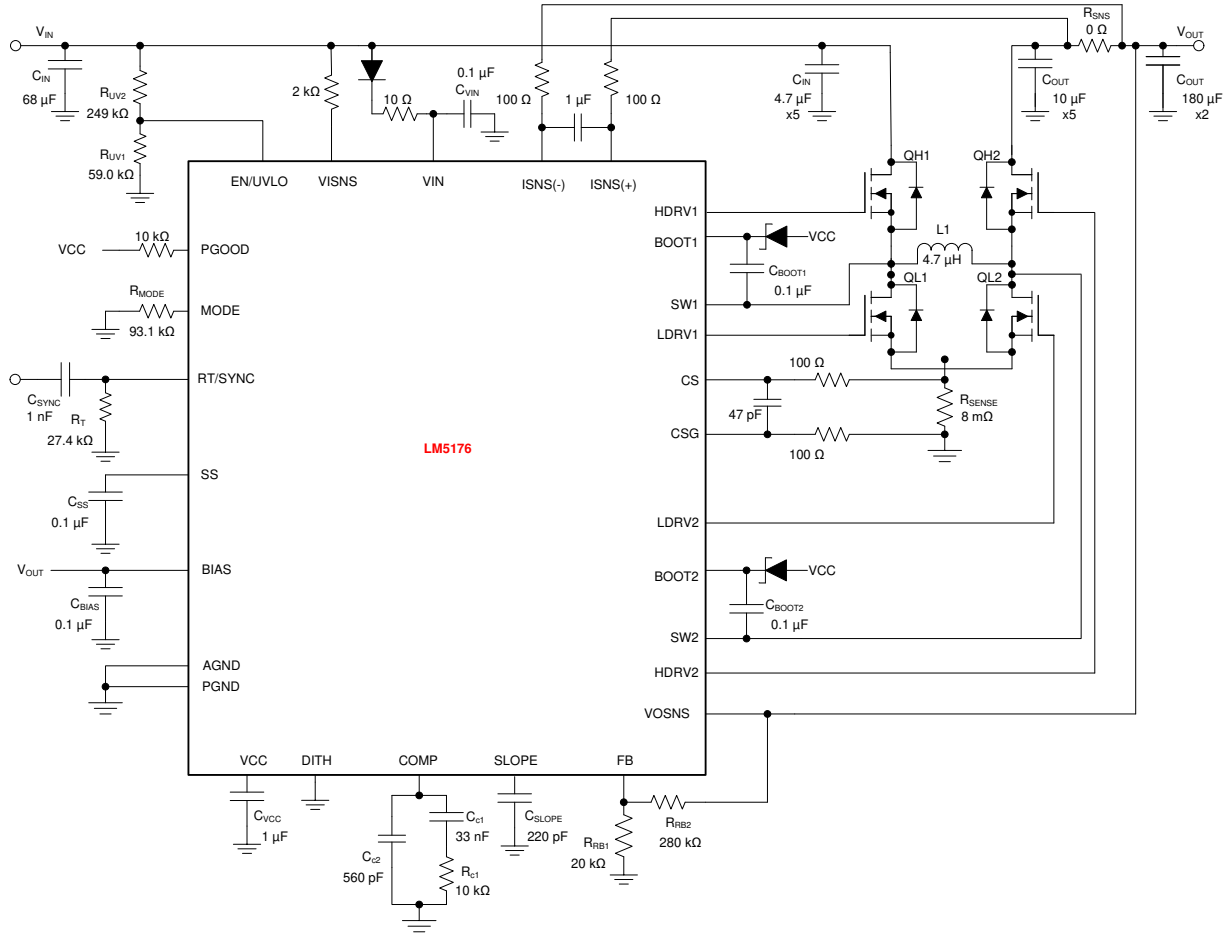


**Figure 8-1. LM5176-Q1 Four-Switch Buck Boost Application Schematic**

### 8.2.1 Design Requirements

For this design example, the following are used as the input parameters.

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input Voltage Range | 6 V to 50 V |
| Output | 12 V |
| Load Current | 6 A |
| Switching Frequency | 300 kHz |
| Mode | CCM, Hiccup |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Custom Design with WEBENCH Tools*

Click here to create a custom design using the LM5176-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your $V_{IN}$, $V_{OUT}$ and $I_{OUT}$ requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

#### *8.2.2.2 Frequency*

The switching frequency of LM5176-Q1 is set by an $R_T$ resistor connected from RT/SYNC pin to AGND. The $R_T$ resistor required to set the desired frequency is calculated using Equation 5 or Figure 6-3 . A 1% standard resistor of 27.4 kΩ is selected for $F_{sw}$ = 300 kHz.

#### *8.2.2.3 $V_{OUT}$*

The output voltage is set using a resistor divider to the FB pin. The internal reference voltage is 0.8 V. Normally the bottom resistor in the resistor divider is selected to be in the 1-kΩ to 100-kΩ range. Select

$$R_{FB1} = 20\ k\Omega \tag{11}$$

The top resistor in the feedback resistor divider is selected using Equation 12:

$$R_{FB2} = \frac{V_{OUT} - 0.8\ V}{0.8\ V} \times R_{FB1} = 280\ k\Omega \tag{12}$$

#### *8.2.2.4 Inductor Selection*

The inductor selection is based on consideration of both buck and boost modes of operation. For buck mode, inductor selection is based on limiting the peak-to-peak current ripple, $\Delta I_L$, to approximately 40% of the maximum inductor current at the maximum input voltage. The target inductance for buck mode is:

$$L_{BUCK} = \frac{(V_{IN(MAX)} - V_{OUT}) \times V_{OUT}}{0.4 \times I_{OUT(MAX)} \times F_{sw} \times V_{IN(MAX)}} = 12.7\,\mu H \tag{13}$$

For boost mode, the inductor selection is based on limiting the peak to peak current ripple, $\Delta I_L$, to approximately 30% of the maximum inductor current at the minimum input voltage. The target inductance for the boost mode is:


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$$L_{BOOST} = \frac{V_{IN(MIN)}^2 \times (V_{OUT} - V_{IN(MIN)})}{0.3 \times I_{OUT(MAX)} \times F_{sw} \times V_{OUT}^2} = 2.8\ \mu H \quad (14)$$

In this particular application, the buck inductance is larger. Choosing a larger inductance reduces the ripple current but also increases the size of the inductor. A larger inductor also reduces the achievable bandwidth of the converter by moving the right half plane zero to lower frequencies. Therefore, a judicious compromise should be made based on the application requirements. For this design, a 4.7-µH inductor is selected. With this inductor selection, the inductor current ripple is 6.5 A, 4.3 A, and 2.1 A, at $V_{IN}$ of 50 V, 24 V, and 6 V, respectively.

The maximum average inductor current occurs at the minimum input voltage and maximum load current:

$$I_{L(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MIN)}} = 13.3\ A \quad (15)$$

where

- 90% efficiency is assumed

The peak inductor current occurs at minimum input voltage and is given by:

$$I_{L(PEAK)} = I_{L(MAX)} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times L1 \times F_{sw} \times V_{OUT}} = 14.4\ A \quad (16)$$

To ensure sufficient output current, the current limit threshold must be set to allow the maximum load current in boost operation. The inductor peak current during overload depends on the current limit resistor, $R_{SENSE}$ (refer to the subsection on selecting $R_{SENSE}$). The peak inductor current in current limit when in boost mode is given by:

$$I_{L(PEAK,\ ILIMIT,\ BOOST)} = \frac{120\ mV}{R_{SENSE}} \quad (17)$$

The peak inductor current in current limit when in buck mode happens at high input voltage and is given by:

$$I_{L(PEAK,\ ILIMIT,\ BUCK)} = \frac{80\ mV}{R_{SENSE}} + \frac{\left(V_{IN(MAX)} - V_{OUT}\right)}{L1 \times F_{sw}} \times \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (18)$$

The peak inductor current in current limit is 15 A and 16.5 A in boost mode and buck mode, respectively. The inductor should be selected to handle this current.

#### *8.2.2.5 Output Capacitor*

In the boost mode, the output capacitor conducts high ripple current. The output capacitor RMS ripple current is given by Equation 19 where the minimum $V_{IN}$ corresponds to the maximum capacitor current.

$$I_{COUT(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad (19)$$

In this example, the maximum output ripple RMS current is $I_{COUT(RMS)}$ = 6 A. A 5-mΩ output capacitor ESR causes an output ripple voltage of 60 mV as given by:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(MIN)}} \times ESR \quad (20)$$

A 400-µF output capacitor causes a capacitive ripple voltage of 25 mV as given by:

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$$\Delta V_{RIPPLE(COUT)} = \frac{I_{OUT} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right)}{C_{OUT} \times F_{sw}} \quad (21)$$

Typically a combination of ceramic and bulk capacitors is needed to provide low ESR and high ripple current capacity. The complete schematic in Figure 8-1 shows a good starting point for $C_{OUT}$ for typical applications.

#### 8.2.2.6 Input Capacitor

In buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{D \times (1 - D)} \quad (22)$$

The maximum RMS current occurs at D = 0.5, which gives $I_{CIN(RMS)}$ = $I_{OUT}$ / 2 = 3 A. A combination of ceramic and bulk capacitors should be used to provide short path for high di/dt current and to reduce the output voltage ripple. The complete schematic in Figure 8-1 is a good starting point for $C_{IN}$ for typical applications.

#### 8.2.2.7 Sense Resistor ($R_{SENSE}$)

The current sense resistor between the CS and CSG pins should be selected to ensure that current limit is set high enough for both buck and boost modes of operation. For the buck operation, the current limit resistor is given by:

$$R_{SENSE(BUCK)} = \frac{80\ mV}{I_{OUT(MAX)}} = 13\ m\Omega \quad (23)$$

For the boost mode of operation, the current limit resistor is given by:

$$R_{SENSE(BOOST)} = \frac{120\ mV}{I_{L(PEAK)}} = 8.3\ m\Omega \quad (24)$$

The closest standard value of $R_{SENSE}$ = 8 mΩ is selected based on the boost mode operation.

The maximum power dissipation in $R_{SENSE}$ happens at $V_{IN(MIN)}$:

$$P_{RSENSE(MAX)} = \left(\frac{120\,mV}{R_{SENSE}}\right)^2 \cdot R_{SENSE} \cdot \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right) = 0.9\,W \quad (25)$$

Therefore, a sense resistor with 2-W power rating will be sufficient for this application.

For some application circuits, it can be required to add a filter network to attenuate noise in the CS and CSG sense lines. See Figure 8-1 for typical values. The filter resistance should not exceed 100 Ω.

#### 8.2.2.8 Slope Compensation

For stable current loop operation and to avoid subharmonic oscillations, the slope capacitor should be selected based on Equation 26:

$$C_{SLOPE} = gm_{SLOPE} \times \frac{L1}{R_{SENSE} \times A_{CS}} = 2\ \mu S \times \frac{4.7\ \mu H}{8\ m\Omega \times 5} = 235\ pF \quad (26)$$

This slope compensation results in “dead-beat” operation, in which the current loop disturbances die out in one switching cycle. Theoretically, a current mode loop is stable with half the “dead-beat” slope (twice the calculated slope capacitor value in Equation 26). A smaller slope capacitor results in larger slope signal which is better for noise immunity in the transition region ($V_{IN}$~$V_{OUT}$). A larger slope signal, however, restricts the achievable


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input voltage range for a given output voltage, switching frequency, and inductor. For this design, $C_{SLOPE}$ = 220 pF is selected for better transition region behavior while still providing the required $V_{IN}$ range. This selection of slope capacitor, inductor, switching frequency, and inductor satisfies the COMP range limitation explained in the *Section 7.3.13* section.

#### 8.2.2.9 UVLO

The UVLO resistor divider must be designed for turnon below 6 V. Selecting $R_{UV2}$ = 249 kΩ gives a UVLO hysteresis of 0.8 V based on Equation 2. The lower UVLO resistor is the selected using Equation 27:

$$R_{UV1} = \frac{R_{UV2} \times V_{EN(OP)}}{V_{IN(UV)} + I_{EN(STBY)} \times R_{UV2} - V_{EN(OP)}} \tag{27}$$

A standard value of 59.0 kΩ is selected for $R_{UV1}$.

When programming the UVLO threshold for lower input voltage operation, it is important to choose MOSFETs with gate (Miller) plateau voltage lower than the minimum $V_{IN}$.

#### 8.2.2.10 Soft-Start Capacitor

The soft-start time is programmed using the soft-start capacitor. The relationship between $C_{SS}$ and the soft-start time is given by:

$$t_{ss} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \tag{28}$$

$C_{SS}$ = 0.1 µF gives a soft-start time of 16 ms.

#### 8.2.2.11 Dither Capacitor

The dither capacitor sets the modulation frequency of the frequency dithering around the nominal switching frequency. A larger $C_{DITH}$ results in lower modulation frequency. For proper operation, the modulation frequency ($F_{MOD}$) must be much lower than the switching frequency. Use Equation 29 to select $C_{DITH}$ for the target modulation frequency.

$$C_{DITH} = \frac{10\ \mu A}{F_{MOD} \times 0.24\ V} \tag{29}$$

For the current design dithering is not being implemented. Therefore a 0-Ω resistor from the DITH pin to AGND disables this feature.

#### 8.2.2.12 MOSFETs QH1 and QL1

The input side MOSFETs QH1 and QL1 need to withstand the maximum input voltage of 50 V. In addition, they must withstand the transient spikes at SW1 during switching. Therefore, QH1 and QL1 should be rated for 60 V or higher. The gate plateau voltages of the MOSFETs should be smaller than the minimum input voltage of the converter, otherwise the MOSFETs may not fully enhance during startup or overload conditions.

The power loss in QH1 in the boost mode of operation is approximated by:

$$P_{COND(QH1)} = \left( I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \right)^2 \cdot R_{DSON(QH1)} \tag{30}$$

The power loss in QH1 in the buck mode of operation consists of both conduction and switching loss components given by Equation 31 and Equation 32, respectively:

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$$P_{COND(QH1)} = \left(\frac{V_{OUT}}{V_{IN}}\right) \cdot {I_{OUT}}^2 \cdot R_{DSON(QH1)} \quad (31)$$

$$P_{SW(QH1)} = \frac{1}{2} \cdot V_{IN} \cdot I_{OUT} \cdot (t_r + t_f) \cdot F_{sw} \quad (32)$$

The rise ($t_r$) and the fall ($t_f$) times are based on the MOSFET datasheet information or measured in the lab. Typically a MOSFET with smaller $R_{DSON}$ (smaller conduction loss) will have longer rise and fall times (larger switching loss).

The power loss in QL1 in the buck mode of operation is shown in Equation 33:

$$P_{COND(QL1)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot {I_{OUT}}^2 \cdot R_{DSON(QL1)} \quad (33)$$

#### 8.2.2.13 MOSFETs QH2 and QL2

The output side MOSFETs QH2 and QL2 see the output voltage of 12 V and additional transient spikes at SW2 during switching. Therefore, QH2 and QL2 should be rated for 20 V or more. The gate plateau voltages of the MOSFETs should be smaller than the minimum input voltage of the converter, otherwise the MOSFETs may not fully enhance during start-up or overload conditions.

The power loss in QH2 in the buck mode of operation is approximated by:

$$P_{COND(QH2)} = {I_{OUT}}^2 \cdot R_{DSON(QH2)} \quad (34)$$

The power loss in QL2 in the boost mode of operation consists of both conduction and switching loss components given by Equation 35 and Equation 36, respectively:

$$P_{COND(QL2)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}}\right)^2 \cdot R_{DSON(QL2)} \quad (35)$$

$$P_{SW(QL2)} = \frac{1}{2} \cdot V_{OUT} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}}\right) \cdot (t_r + t_f) \cdot F_{sw} \quad (36)$$

The rise ($t_r$) and the fall ($t_f$) times can be based on the MOSFET datasheet information or measured in the lab. Typically a MOSFET with smaller $R_{DSON}$ (lower conduction loss) has longer rise and fall times (larger switching loss).

The power loss in QH2 in the boost mode of operation is shown in Equation 37:

$$P_{COND(QH2)} = \frac{V_{IN}}{V_{OUT}} \cdot \left(I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}}\right)^2 \cdot R_{DSON(QH2)} \quad (37)$$

#### 8.2.2.14 Frequency Compensation

This section presents the control loop compensation design procedure for the LM5176-Q1 buck-boost controller. The LM5176-Q1 operates mainly in buck or boost modes, separated by a transition region, and therefore, the control loop design is done for both buck and boost operating modes. Then, a final selection of compensation is made based on the mode that is more restrictive from a loop stability point of view. Typically for a converter designed to go deep into both buck and boost operating regions, the boost compensation design is more restrictive due to the presence of a right half plane zero (RHPZ) in the boost mode.

The boost power stage output pole location is given by:


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$$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT} \times C_{OUT}}\right) = 398 \text{ Hz} \quad (38)$$

where

- $R_{OUT}$ = 2 Ω corresponds to the maximum load of 6 A

The boost power stage ESR zero location is given by:

$$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR} \times C_{OUT}}\right) = 79.6 \text{ kHz} \quad (39)$$

The boost power stage RHP zero location is given by:

$$f_{RHP} = \frac{1}{2\pi}\left(\frac{R_{OUT} \times (1 - D_{MAX})^2}{L1}\right) = 16.9 \text{ kHz} \quad (40)$$

where

- $D_{MAX}$ is the maximum duty cycle at the minimum $V_{IN}$

The buck power stage output pole location is given by:

$$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT} \times C_{OUT}}\right) = 199 \text{ Hz} \quad (41)$$

The buck power stage ESR zero location is the same as the boost power stage ESR zero.

It is clear from Equation 40 that RHP zero is the main factor limiting the achievable bandwidth. For a robust design, the crossover frequency should be less than 1/3 of the RHP zero frequency. Given the position of the RHP zero, a reasonable target bandwidth in boost operation is around 4 kHz:

$$f_{bw} = 4 \text{ kHz} \quad (42)$$

For some power stages, the boost RHP zero might not be as restrictive. This happens when the boost maximum duty cycle ($D_{MAX}$) is small, or when a really small inductor is used. In those cases, compare the limits posed by the RHP zero ($f_{RHP}$ / 3) with 1/20 of the switching frequency and use the smaller of the two values as the achievable bandwidth.

The compensation zero can be placed at 1.5 times the boost output pole frequency. Keep in mind that this locates the zero at three times the buck output pole frequency which results in approximately 30 degrees of phase loss before crossover of the buck loop and 15 degrees of phase loss at intermediate frequencies for the boost loop:

$$f_{zc} = 600 \text{ Hz} \quad (43)$$

If the crossover frequency is well below the RHP zero and the compensation zero is placed well below the crossover, the compensation gain resistor $R_{c1}$ is calculated using the approximation:

$$R_{c1} = \frac{2\pi \times f_{bw}}{gm_{EA}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times \frac{A_{CS} \times R_{SENSE} \times C_{OUT}}{1 - D_{MAX}} = 9.49 \text{ k}\Omega \quad (44)$$

where

- $D_{MAX}$ is the maximum duty cycle at the minimum $V_{IN}$ in boost mode
- $A_{CS}$ is the current sense amplifier gain

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The compensation capacitor $C_{c1}$ is then calculated from:

$$C_{c1} = \frac{1}{2 \times \pi \times f_{zc} \times R_{c1}} = 27.9 \text{ nF} \quad (45)$$

The standard values of compensation components are selected to be $R_{c1}$ = 10 kΩ and $C_{c1}$ = 33 nF.

A high frequency pole ($f_{pc2}$) is placed using a capacitor ($C_{c2}$) in parallel with $R_{c1}$ and $C_{c1}$. Set the frequency of this pole at seven to ten times of $f_{bw}$ to provide attenuation of switching ripple and noise on COMP while avoiding excessive phase loss at the crossover frequency. For a target $f_{pc2}$ = 28 kHz, $C_{c2}$ is calculated using Equation 46:

$$C_{c2} = \frac{1}{2 \times \pi \times f_{pc2} \times R_{c1}} = 568 \text{ pF} \quad (46)$$

Select a standard value of 560 pF for $C_{c2}$. These values provide a good starting point for the compensation design. Each design should be tuned in the lab to achieve the desired balance between stability margin across the operating range and transient response time.

### 8.2.3 Application Curves

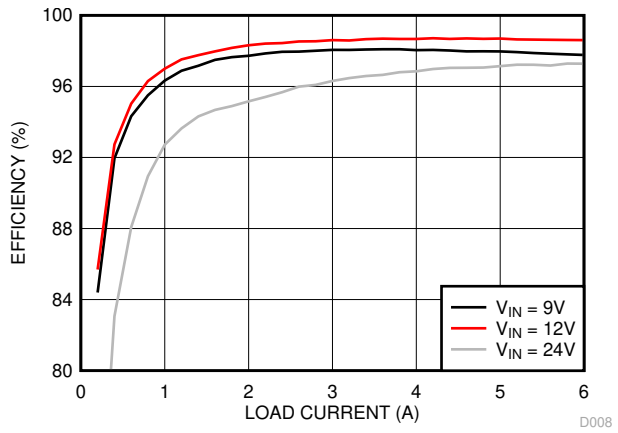


Figure 8-2. Efficiency vs Load

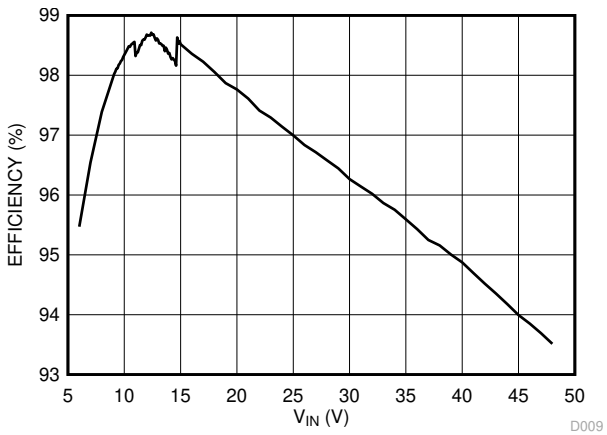


Figure 8-3. Efficiency vs Input Voltage

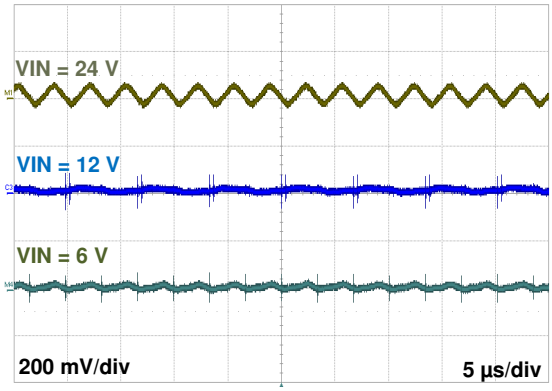


Figure 8-4. Output Voltage Ripple

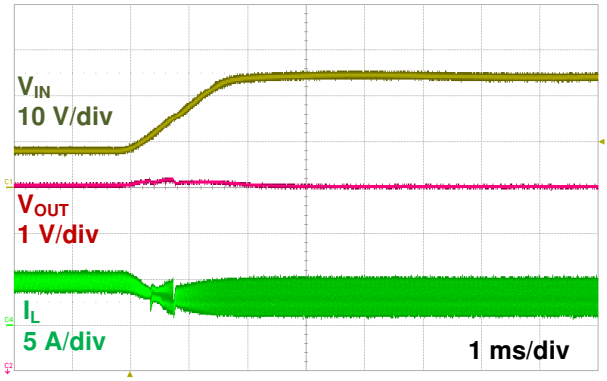


Figure 8-5. Line Transient Response (8 V - 24 V, $I_{OUT}$ = 2 A)

## 9 Power Supply Recommendations

The LM5176-Q1 is a power management device. The power supply for the device is any dc voltage source within the specified input range. The supply should also be capable of supplying sufficient current based on the maximum inductor current in boost mode operation. The input supply should be bypassed with additional


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electrolytic capacitor at the input of the application board to avoid ringing due to parasitic impedance of the connecting cables.

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# 10 Layout

## 10.1 Layout Guidelines

The basic PCB board layout requires separation of sensitive signal and power paths. This checklist must be followed to get good performance for a well-designed board.

- Place the power components including the input filter capacitor $C_{IN}$, the power MOSFETs QL1 and QH1, and the sense resistor $R_{SENSE}$ close together to minimize the loop area for input switching current in buck operation.
- Place the power components including the output filter capacitor $C_{OUT}$, the power MOSFETs QL2 and QH2, and the sense resistor $R_{SENSE}$ close together to minimize the loop area for output switching current in boost operation.
- Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the input and output capacitors. Place the smaller capacitors closer to the IC to provide a low impedance path for high di/dt switching currents.
- Minimize the SW1 and SW2 loop areas as these are high dv/dt nodes.
- Layout the gate drive traces and return paths as directly as possible. Layout the forward and return traces close together, either running side by side or on top of each other on adjacent layers to minimize the inductance of the gate drive path.
- Use Kelvin connections to $R_{SENSE}$ for the current sense signals CS and CSG and run lines in parallel from the $R_{SENSE}$ terminals to the IC pins. Avoid crossing noisy areas such as SW1 and SW2 nodes or high-side gate drive traces. Place the filter capacitor for the current sense signal as close to the IC pins as possible.
- Place the $C_{IN}$, $C_{OUT}$, and $R_{SENSE}$ ground pins as close as possible with thick ground trace and/or planes on multiple layers.
- Place the VCC bypass capacitor close to the controller IC, between the VCC and PGND pins. A 1-µF ceramic capacitor is typically used.
- Place the BIAS bypass capacitor close to the controller IC, between the BIAS and PGND pins. A 0.1-µF ceramic capacitor is typically used.
- Place the BOOT1 bootstrap capacitor close to the IC and connect directly to the BOOT1 to SW1 pins.
- Place the BOOT2 bootstrap capacitor close to the IC and connect directly to the BOOT2 to SW2 pins.
- Bypass the $V_{IN}$ pin to AGND with a low ESR ceramic capacitor located close to the controller IC. A 0.1-µF ceramic capacitor is typically used. When using external BIAS, use a diode between input rails and $V_{IN}$ pins to prevent reverse conduction when $V_{IN}$ < VCC.
- Connect the feedback resistor divider between the $C_{OUT}$ positive terminal and AGND pin of the IC. Place the components close to the FB pin.
- Use care to separate the power and signal paths so that no power or switching current flows through the AGND connections which can either corrupt the COMP, SLOPE, or SYNC signals, or cause dc offset in the FB sense signal. The PGND and AGND traces can be connected near the PGND pin, near the VCC capacitor PGND connection, or near the PGND connection of the CS, CSG pin current sense resistor.
- When using the average current loop, divide the overall capacitor ($C_{IN}$ or $C_{OUT}$) between the two sides of the sense resistor to ensure small cycle-by-cycle ripple. Place the average current loop filter capacitor close to the IC between the ISNS(+) and ISNS(-) pins.


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## 10.2 Layout Example

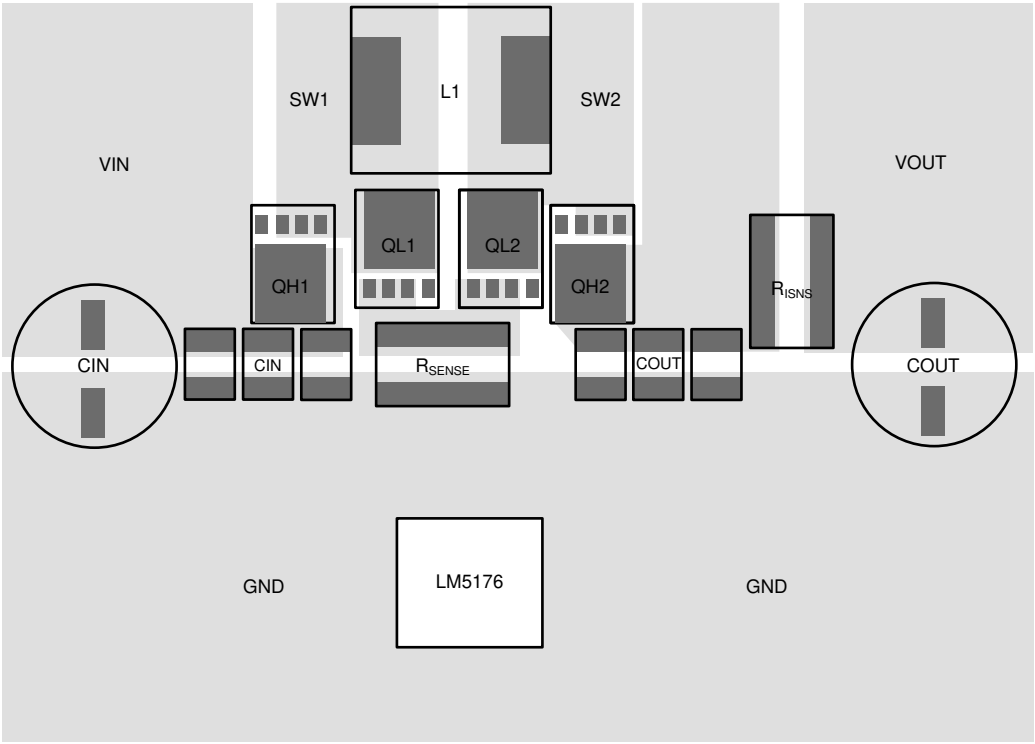


**Figure 10-1. LM5176-Q1 Power Stage Layout**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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### 11.1.2 Development Support

#### *11.1.2.1 Custom Design with WEBENCH Tools*

Click here to create a custom design using the LM5176-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your $V_{IN}$, $V_{OUT}$ and $I_{OUT}$ requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

Please visit TI homepage for latest technical document including application notes, user guides, and reference designs.

Texas Instruments, *Semiconductor and IC Package Thermal Metrics*

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM5176QPWPRQ1 | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | LM5176Q1 |
| LM5176QPWPRQ1.B | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | LM5176Q1 |
| LM5176QPWPTQ1 | Active | Production | HTSSOP (PWP) \| 28 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | LM5176Q1 |
| LM5176QPWPTQ1.B | Active | Production | HTSSOP (PWP) \| 28 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | LM5176Q1 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM5176-Q1 :**

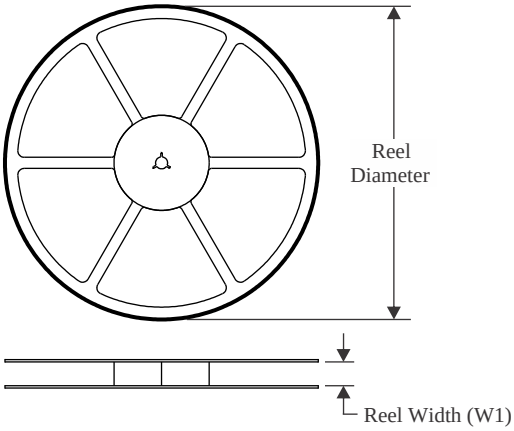
- Catalog : LM5176

NOTE: Qualified Version Definitions:

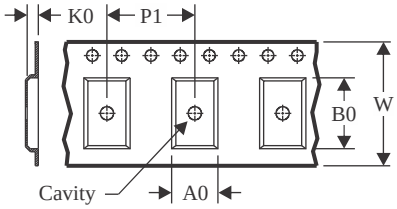
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

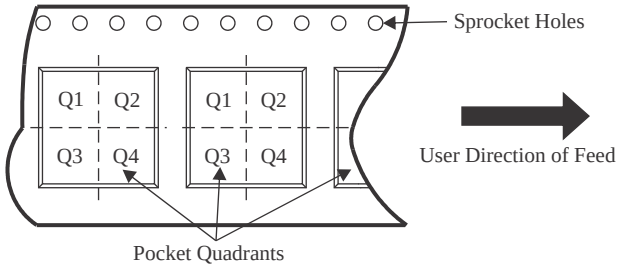



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

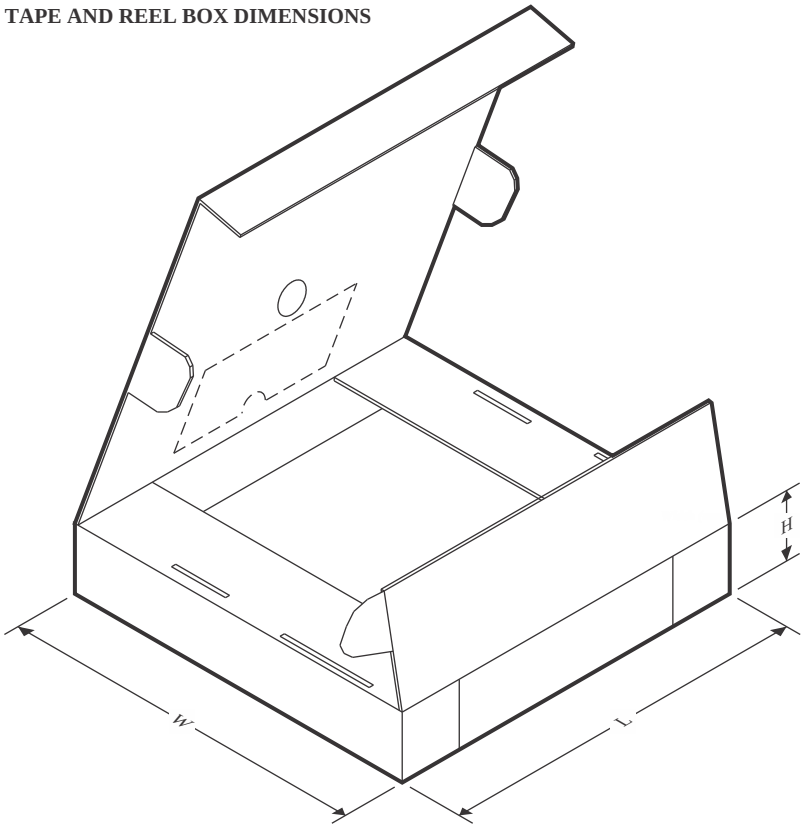
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5176QPWPRQ1 | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

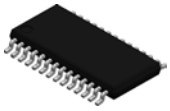



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM5176QPWPRQ1 | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |

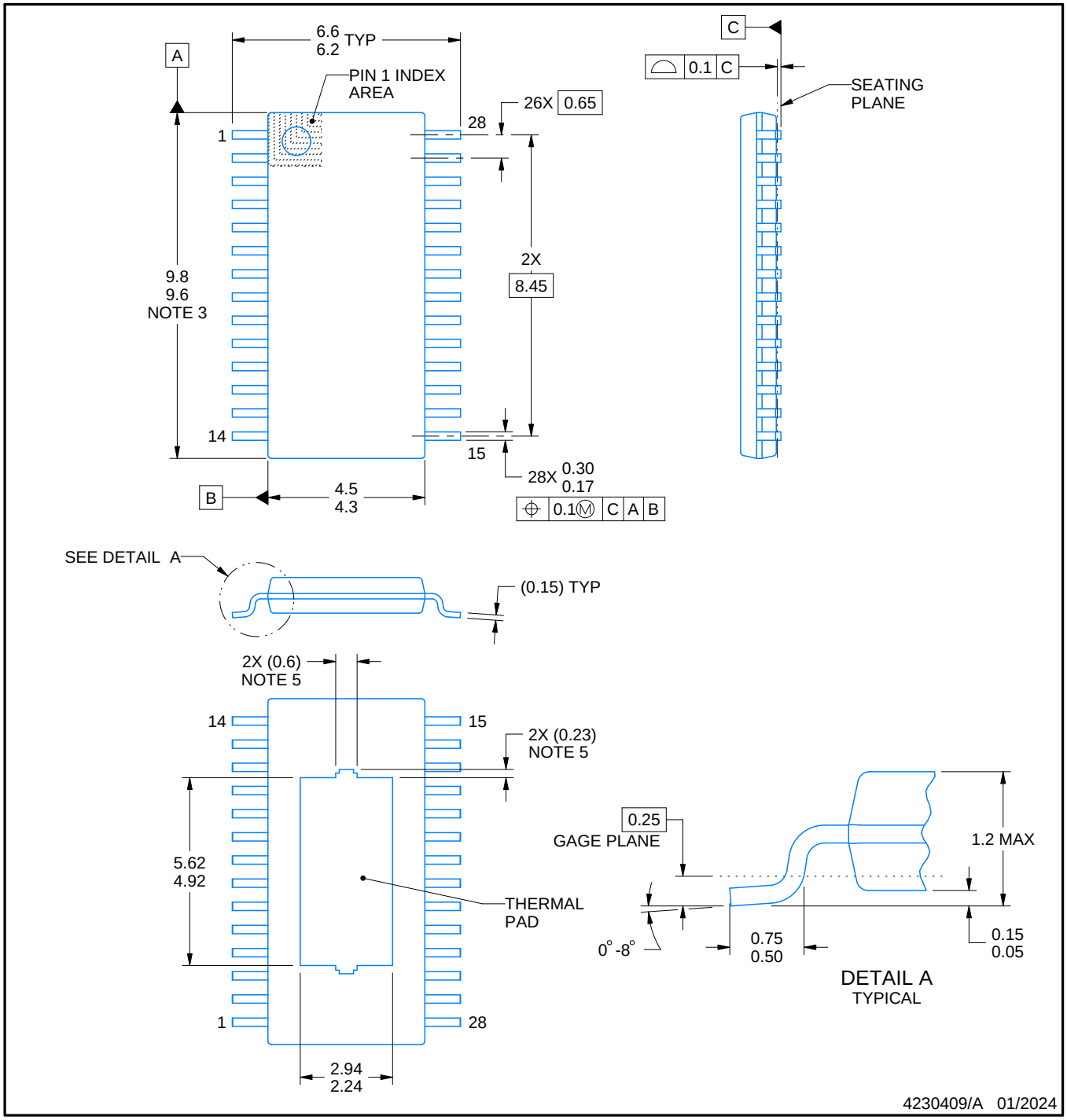
# PACKAGE OUTLINE

## PWP0028V



## PowerPAD™ TSSOP - 1.2 mm max height

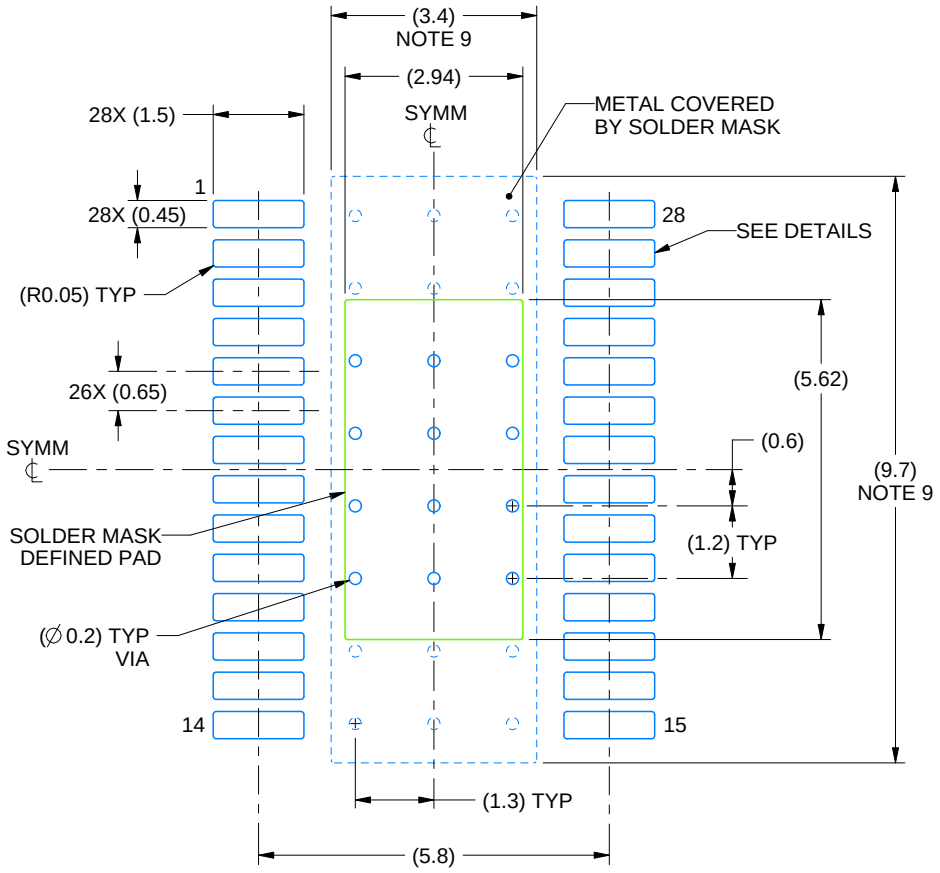
SMALL OUTLINE PACKAGE



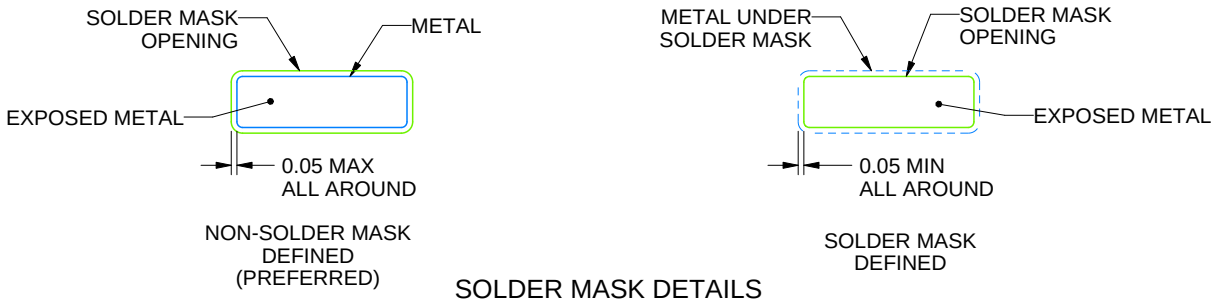

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X




SOLDER MASK DETAILS

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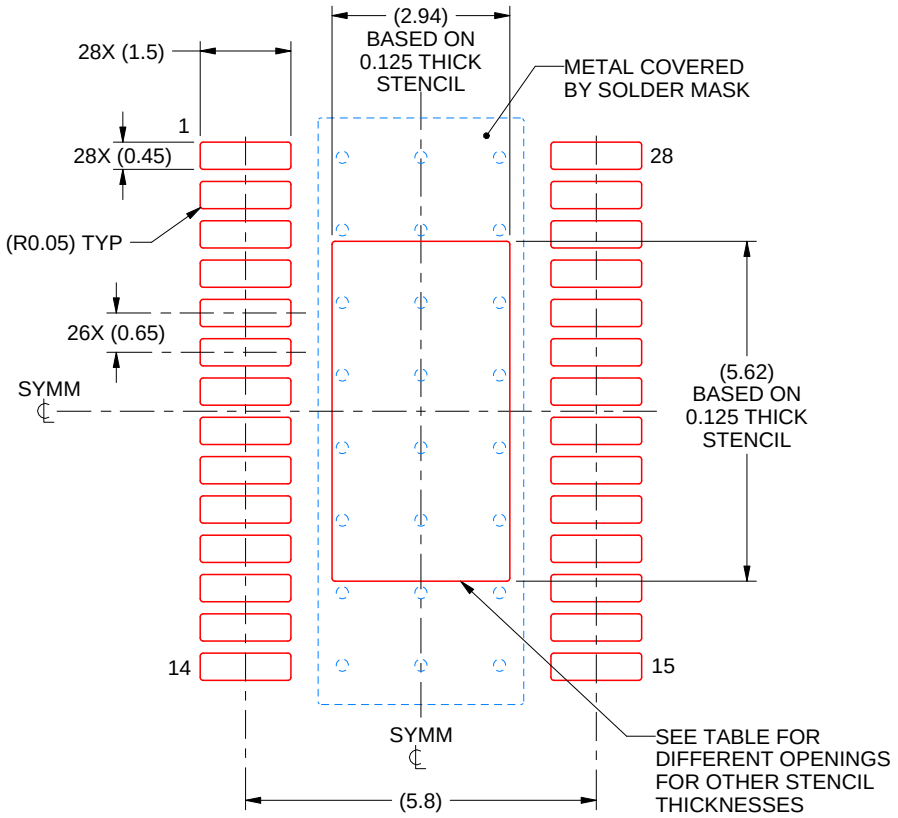
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.29 X 6.28 |
| 0.125 | 2.94 X 5.62 (SHOWN) |
| 0.15 | 2.68 X 5.13 |
| 0.175 | 2.48 X 4.75 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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