

## FOUR-CHANNEL AUTOMOTIVE DIGITAL AMPLIFIERS

Check for Samples: [TAS5414B-Q1](#), [TAS5424B-Q1](#)

### FEATURES

- **TAS5414B-Q1 – Single-Ended Input**
- **TAS5424B-Q1 – Differential Input**
- **Four-Channel Digital Power Amplifier**
- **Four Analog Inputs, Four BTL Power Outputs**
- **Typical Output Power at 10% THD+N**
  - 28 W/Ch Into 4  $\Omega$  at 14.4 V
  - 50 W/Ch Into 2  $\Omega$  at 14.4 V
  - 79 W/Ch Into 4  $\Omega$  at 24 V
  - 150 W/Ch Into 2  $\Omega$  at 24 V (PBTL)
- **Channels Can Be Paralleled (PBTL) for High Current Applications**
- **THD+N < 0.02%, 1 kHz, 1 W Into 4  $\Omega$**
- **Patented Pop- and Click-Reduction Technology**
  - Soft Muting With Gain Ramp Control
  - Common-Mode Ramping
- **Patented AM Interference Avoidance**
- **Patented Cycle-by-Cycle Current Limit**
- **75-dB PSRR**
- **Four-Address I<sup>2</sup>C Serial Interface for Device Configuration and Control**
- **Channel Gains: 12-dB, 20-dB, 26-dB, 32-dB**
- **Load Diagnostic Functions:**
  - Output Open and Shorted Load
  - Output-to-Power and -to-Ground Shorts
  - Patented Tweeter Detection
- **Protection and Monitoring Functions:**
  - Short-Circuit Protection
  - Load-Dump Protection to 50 V
  - Fortuitous Open Ground and Power Tolerant
  - Patented Output DC Level Detection While Music Playing
  - Over-temperature Protection
  - Over- and Undervoltage Conditions
  - Clip Detection

- **36-Pin PSOP3 (DKD) Power SOP Package With Heat Slug Up for the TAS5414B-Q1**
- **44-Pin PSOP3 (DKD) Power SOP Package With Heat Slug Up for the TAS5424B-Q1**
- **44-Pin PSOP3 (DKE) Low-Standoff Power SOP Package With Heat Slug Up for the TAS5424B-Q1**
- **64-Pin QFP (PHD) Power Package With Heat Slug Up for TAS5414B-Q1**
- **Designed for Automotive EMC Requirements**
- **Qualified According to AEC-Q100**
- **ISO9000:2002 TS16949 Certified**
- **–40°C to 105°C Ambient Temperature Range**

### APPLICATIONS

- **OEM/Retail Head Units and Amplifier Modules Where Feature Densities and System Configurations Require Reduction in Heat From the Audio Power Amplifier**

### DESCRIPTION

The TAS5414B-Q1 and TAS5424B-Q1 are four-channel digital audio amplifiers designed for use in automotive head units and external amplifier modules. They provide four channels at 23 W continuously into 4  $\Omega$  at less than 1% THD+N from a 14.4-V supply. Each channel can also deliver 38 W into 2  $\Omega$  at 1% THD+N. The TAS5414B-Q1 uses single-ended analog inputs, while the TAS5424B-Q1 employs differential inputs for increased immunity to common-mode system noise. The digital PWM topology of the device provides dramatic improvements in efficiency over traditional linear amplifier solutions. This reduces the power dissipated by the amplifier by a factor of ten under typical music playback conditions. The device incorporates all the functionality needed to perform in the demanding OEM applications area. They have built-in load diagnostic functions for detecting and diagnosing misconnected outputs to help to reduce test time during the manufacturing process.

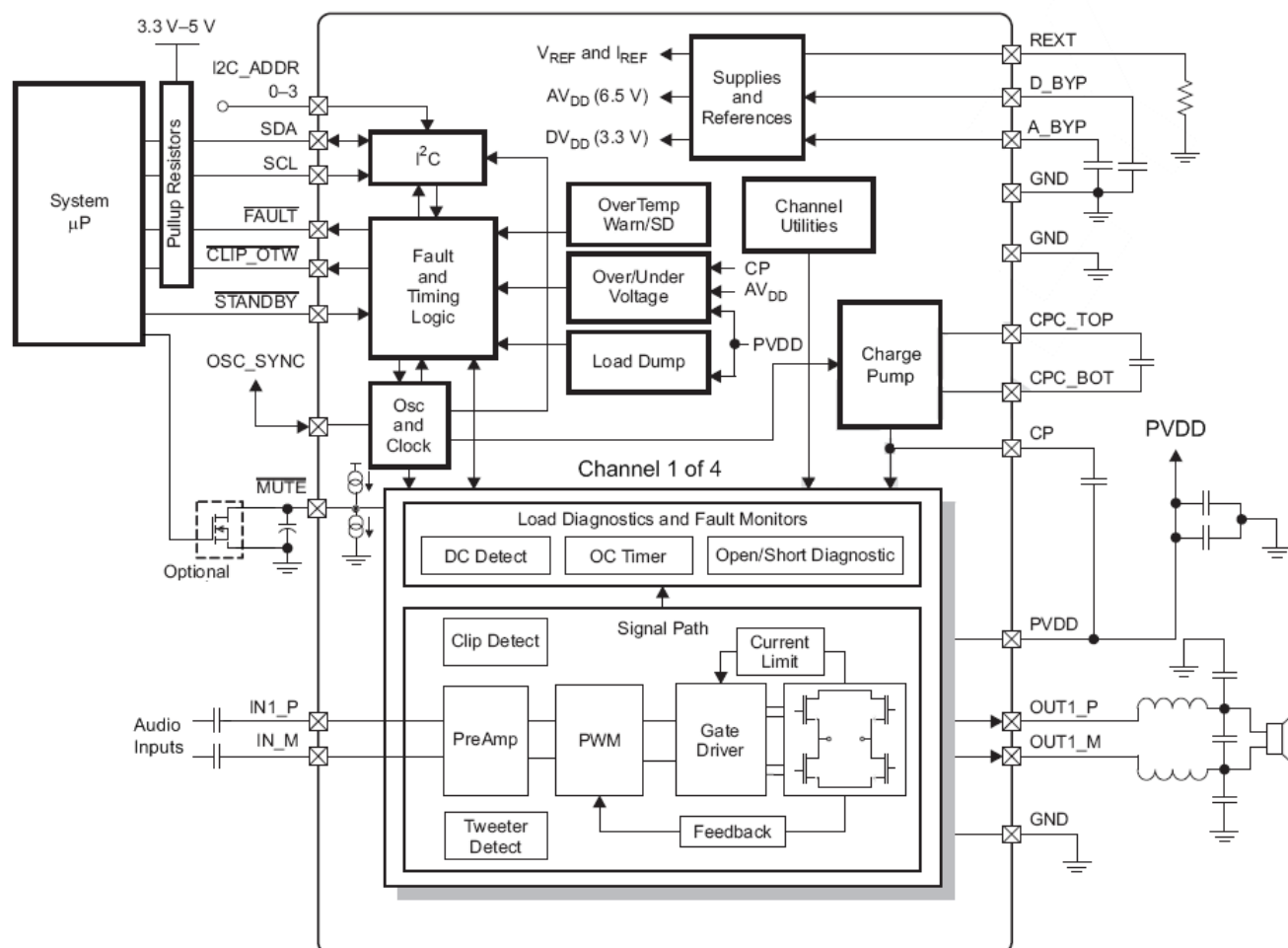


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

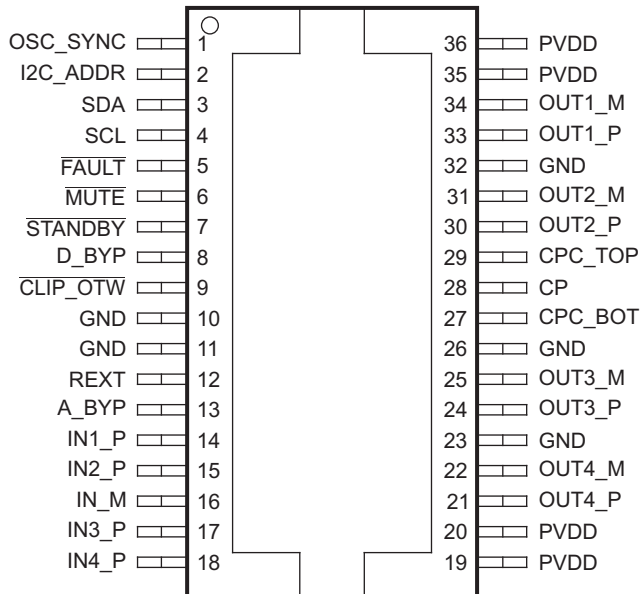
## FUNCTIONAL BLOCK DIAGRAM



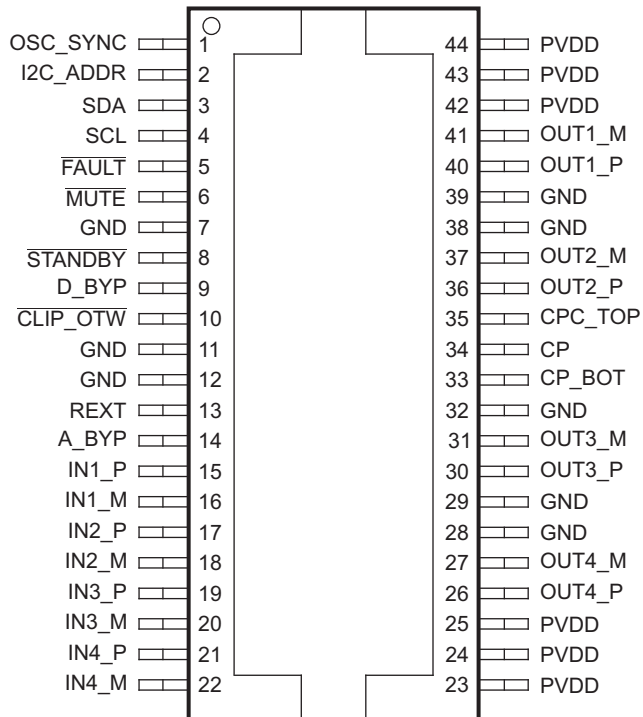
## PIN ASSIGNMENTS AND FUNCTIONS

The pin assignments are shown as follows.

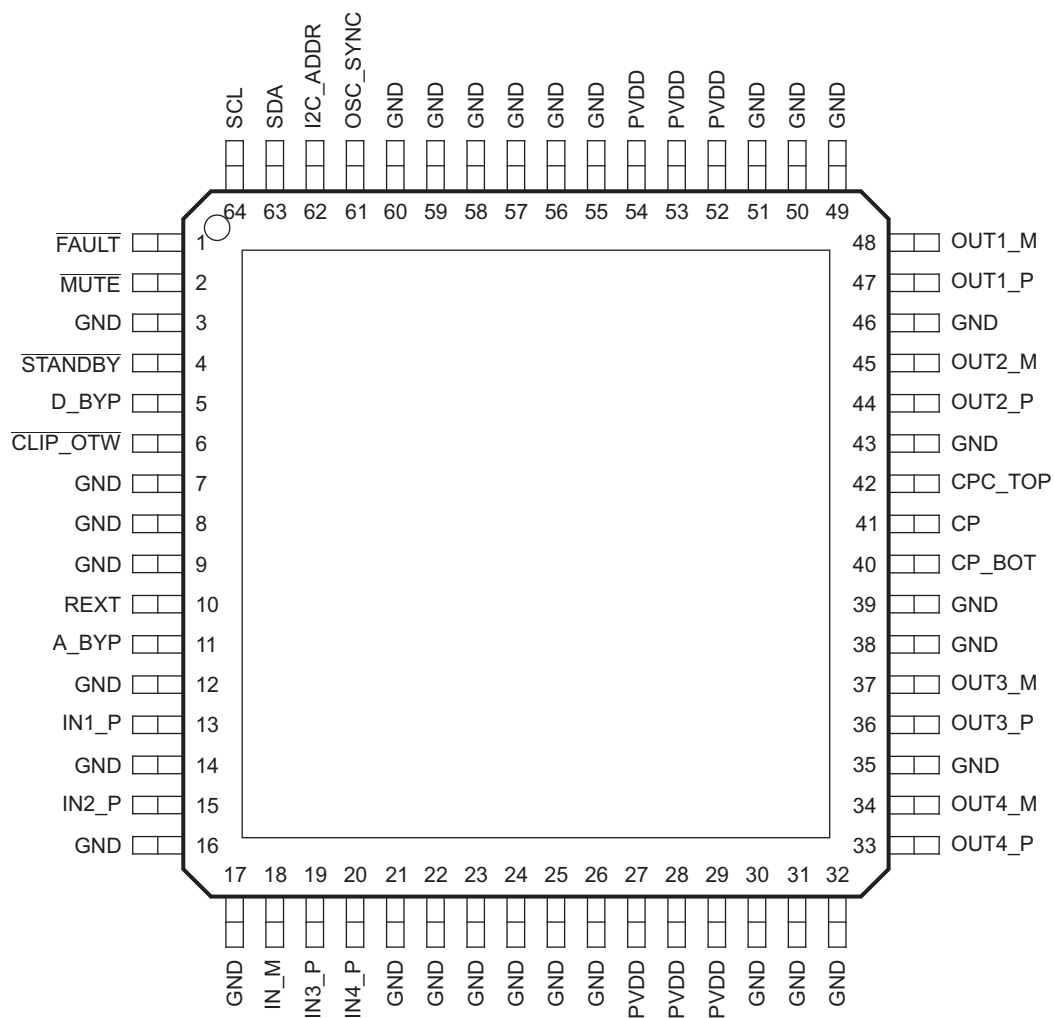
**TAS5414B  
DKD Package  
(Top View)**



**TAS5424B  
DKD Package  
(Top View)**



TAS5414B  
PHD Package  
(Top View)



**Table 1. PIN FUNCTIONS**

| NAME     | PIN                |                               |                                                                                                                        | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                    |
|----------|--------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------|---------------------|------------------------------------------------------------------------------------------------|
|          | DKD/DKE PACKAGE    | PHD PACKAGE                   |                                                                                                                        |                     |                                                                                                |
|          | TAS5414B-Q1 NO.    | TAS5424B-Q1 NO.               | TAS5414B-Q1 NO.                                                                                                        |                     |                                                                                                |
| A_BYP    | 13                 | 14                            | 11                                                                                                                     | PBY                 | Bypass pin for the AVDD analog regulator                                                       |
| CLIP_OTW | 9                  | 10                            | 6                                                                                                                      | DO                  | Reports CLIP, OTW, or both. It also reports tweeter detection during tweeter mode. Open-Drain. |
| CP       | 28                 | 34                            | 41                                                                                                                     | CP                  | Top of main storage capacitor for charge pump (bottom goes to PVDD)                            |
| CPC_BOT  | 27                 | 33                            | 40                                                                                                                     | CP                  | Bottom of flying capacitor for charge pump                                                     |
| CPC_TOP  | 29                 | 35                            | 42                                                                                                                     | CP                  | Top of flying capacitor for charge pump                                                        |
| D_BYP    | 8                  | 9                             | 5                                                                                                                      | PBY                 | Bypass pin for DVDD regulator output                                                           |
| FAULT    | 5                  | 5                             | 1                                                                                                                      | DO                  | Global fault output (open drain): UV, OV, OTSD, OCSD, DC                                       |
| GND      | 10, 11, 23, 26, 32 | 7, 11, 12, 28, 29, 32, 38, 39 | 3, 7, 8, 9, 12, 14, 16, 17, 21, 22, 23, 24, 25, 26, 30, 31, 32, 35, 38, 39, 43, 46, 49, 50, 51, 55, 56, 57, 58, 59, 60 | GND                 | Ground                                                                                         |
| I2C_ADDR | 2                  | 2                             | 62                                                                                                                     | AI                  | I <sup>2</sup> C address bit                                                                   |
| IN1_M    | N/A                | 16                            | N/A                                                                                                                    | AI                  | Inverting analog input for channel 1 (TAS5424B-Q1 only)                                        |
| IN1_P    | 14                 | 15                            | 13                                                                                                                     | AI                  | Non-inverting analog input for channel 1                                                       |
| IN2_M    | N/A                | 18                            | N/A                                                                                                                    | AI                  | Inverting analog input for channel 2 (TAS5424B-Q1 only)                                        |
| IN2_P    | 15                 | 17                            | 15                                                                                                                     | AI                  | Non-inverting analog input for channel 2                                                       |
| IN3_M    | N/A                | 20                            | N/A                                                                                                                    | AI                  | Inverting analog input for channel 3 (TAS5424B-Q1 only)                                        |
| IN3_P    | 17                 | 19                            | 19                                                                                                                     | AI                  | Non-inverting analog input for channel 3                                                       |
| IN4_M    | N/A                | 22                            | N/A                                                                                                                    | AI                  | Inverting analog input for channel 4 (TAS5424B-Q1 only)                                        |
| IN4_P    | 18                 | 21                            | 20                                                                                                                     | AI                  | Non-inverting analog input for channel 4                                                       |
| IN_M     | 16                 | N/A                           | 18                                                                                                                     | ARTN                | Signal return for the 4 analog channel inputs (TAS5414B-Q1 only)                               |
| MUTE     | 6                  | 6                             | 2                                                                                                                      | AI                  | Gain ramp control: mute (low), play (high)                                                     |
| OSC_SYNC | 1                  | 1                             | 61                                                                                                                     | DI/DO               | Oscillator input from master or output to slave amplifiers                                     |
| OUT1_M   | 34                 | 41                            | 48                                                                                                                     | PO                  | – polarity output for bridge 1                                                                 |
| OUT1_P   | 33                 | 40                            | 47                                                                                                                     | PO                  | + polarity output for bridge 1                                                                 |
| OUT2_M   | 31                 | 37                            | 45                                                                                                                     | PO                  | – polarity output for bridge 2                                                                 |
| OUT2_P   | 30                 | 36                            | 44                                                                                                                     | PO                  | + polarity output for bridge 2                                                                 |
| OUT3_M   | 25                 | 31                            | 37                                                                                                                     | PO                  | – polarity output for bridge 3                                                                 |
| OUT3_P   | 24                 | 30                            | 36                                                                                                                     | PO                  | + polarity output for bridge 3                                                                 |
| OUT4_M   | 22                 | 27                            | 34                                                                                                                     | PO                  | – polarity output for bridge 4                                                                 |
| OUT4_P   | 21                 | 26                            | 33                                                                                                                     | PO                  | + polarity output for bridge 4                                                                 |
| PVDD     | 19, 20, 35, 36     | 23, 24, 25, 42, 43, 44        | 27, 28, 29, 52, 53, 54                                                                                                 | PWR                 | PVDD supply                                                                                    |
| REXT     | 12                 | 13                            | 10                                                                                                                     | AI                  | Precision resistor pin to set analog reference                                                 |
| SCL      | 4                  | 4                             | 64                                                                                                                     | DI                  | I <sup>2</sup> C clock input from system I <sup>2</sup> C master                               |
| SDA      | 3                  | 3                             | 63                                                                                                                     | DI/DO               | I <sup>2</sup> C data I/O for communication with system I <sup>2</sup> C master                |
| STANDBY  | 7                  | 8                             | 4                                                                                                                      | DI                  | Active-low STANDBY pin. Standby (low), power up (high)                                         |

(1) DI = digital input, DO = digital output, AI = analog input, ARTN = analog signal return, PWR = power supply, PBY = power bypass, PO = power output, GND = ground, CP = charge pump.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)

|                                   |                                                                                                  |                                            | VALUE       | UNIT             |
|-----------------------------------|--------------------------------------------------------------------------------------------------|--------------------------------------------|-------------|------------------|
| PVDD                              | DC supply voltage range                                                                          | Relative to GND                            | –0.3 to 30  | V                |
| PVDD <sub>MAX</sub>               | Pulsed supply voltage range                                                                      | $t \leq 100$ ms exposure                   | –1 to 50    | V                |
| PVDD <sub>RAMP</sub>              | Supply voltage ramp rate                                                                         |                                            | 15          | V/ms             |
| I <sub>PVDD</sub>                 | Externally imposed dc supply current per PVDD or GND pin                                         |                                            | ±12         | A                |
| I <sub>PVDD_MAX</sub>             | Pulsed supply current per PVDD pin (one shot)                                                    | $t < 100$ ms                               | 17          | A                |
| I <sub>O</sub>                    | Maximum allowed dc current per output pin                                                        |                                            | ±13.5       | A                |
| I <sub>O_MAX</sub> <sup>(1)</sup> | Pulsed output current per output pin (single pulse)                                              | $t < 100$ ms                               | ±17         | A                |
| I <sub>IN_MAX</sub>               | Maximum current, all digital and analog input pins <sup>(2)</sup>                                | DC or pulsed                               | ±1          | mA               |
| I <sub>MUTE_MAX</sub>             | Maximum current on $\overline{\text{MUTE}}$ pin                                                  | DC or pulsed                               | ±20         | mA               |
| I <sub>IN_ODMAX</sub>             | Maximum sink current for open-drain pins                                                         |                                            | 7           | mA               |
| V <sub>LOGIC</sub>                | Input voltage range for pin relative to GND (SCL, SDA, I2C_ADDR pins)                            | Supply voltage range:<br>6 V < PVDD < 24 V | –0.3 to 6   | V                |
| V <sub>MUTE</sub>                 | Voltage range for $\overline{\text{MUTE}}$ pin relative to GND                                   | Supply voltage range:<br>6 V < PVDD < 24 V | –0.3 to 7.5 | V                |
| V <sub>STANDBY</sub>              | Input voltage range for $\overline{\text{STANDBY}}$ pin                                          | Supply voltage range:<br>6 V < PVDD < 24 V | –0.3 to 5.5 | V                |
| V <sub>OSC_SYNC</sub>             | Input voltage range for OSC_SYNC pin relative to GND                                             | Supply voltage range:<br>6 V < PVDD < 24 V | –0.3 to 3.6 | V                |
| V <sub>GND</sub>                  | Maximum voltage between GND pins                                                                 |                                            | ±0.3        | V                |
| V <sub>AIN_AC_MAX_5414</sub>      | Maximum ac-coupled input voltage for TAS5414B-Q1 <sup>(2)</sup> , analog input pins              | Supply voltage range:<br>6 V < PVDD < 24 V | 1.9         | V <sub>rms</sub> |
| V <sub>AIN_AC_MAX_5424</sub>      | Maximum ac-coupled differential input voltage for TAS5424B-Q1 <sup>(2)</sup> , analog input pins | Supply voltage range:<br>6 V < PVDD < 24 V | 3.8         | V <sub>rms</sub> |
| T <sub>J</sub>                    | Maximum operating junction temperature range                                                     |                                            | –55 to 150  | °C               |
| T <sub>stg</sub>                  | Storage temperature range                                                                        |                                            | –55 to 150  | °C               |

(1) Pulsed current ratings are maximum survivable currents externally applied to the device. High currents may be encountered during reverse battery, fortuitous open ground, and fortuitous open supply fault conditions.

(2) See [Application Information](#) section for information on analog input voltage and ac coupling.

**THERMAL CHARACTERISTICS**

| PARAMETER                                                                     | VALUE (Typical)                                                                                                                                               | UNIT |
|-------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| R <sub>θJC</sub> Junction-to-case (heat slug) thermal resistance, DKD package | 1.0                                                                                                                                                           | °C/W |
| R <sub>θJC</sub> Junction-to-case (heat slug) thermal resistance, PHD package | 1.2                                                                                                                                                           |      |
| R <sub>θJA</sub> Junction-to-ambient thermal resistance                       | This device is not intended to be used without a heatsink. Therefore, R <sub>θJA</sub> is not specified. See the <a href="#">Thermal Information</a> section. |      |
| Exposed pad dimensions, DKD package                                           | 13.8 × 5.8                                                                                                                                                    | mm   |
| Exposed pad dimensions, PHD package                                           | 8 × 8                                                                                                                                                         |      |

## ELECTROSTATIC DISCHARGE (ESD)

| PARAMETER                                  | Package | Pins                                              | VALUE<br>(Typical) | UNIT |
|--------------------------------------------|---------|---------------------------------------------------|--------------------|------|
| Human Body Model (HBM)<br>AEC-Q100-002     | All     | All                                               | 3000               | V    |
| Charged Device Model (CDM)<br>AEC-Q100-011 | DKD/DKE | Corner Pins excluding OSC_SYNC                    | 1000               |      |
|                                            |         | All other pins (including OSC_SYNC) except CP pin | 500                |      |
|                                            |         | CP Pin (Non-Corner Pin)                           | 400                |      |
|                                            | PHD     | Corner Pins excluding SCL                         | 750                |      |
|                                            |         | All Pins (including SCL) except CP and CP_Top     | 600                |      |
|                                            |         | CP and CP_Top Pins                                | 400                |      |
| Machine Model (MM)<br>AEC-Q100-003         | DKD/DKE |                                                   | 150                |      |
|                                            | PHD     |                                                   | 100                |      |

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                                         |                                                                                                                           |                                                                                  | MIN  | TYP      | MAX                   | UNIT |
|-----------------------------------------|---------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|------|----------|-----------------------|------|
| PVDD <sub>OP</sub>                      | DC supply voltage range relative to GND                                                                                   |                                                                                  | 6    | 14.4     | 24                    | V    |
| V <sub>AIN_5414</sub> <sup>(2)</sup>    | Analog audio input signal level (TAS5414B-Q1)                                                                             | AC-coupled input voltage                                                         | 0    |          | 0.25–1 <sup>(3)</sup> | Vrms |
| V <sub>AIN_5424</sub> <sup>(2)</sup>    | Analog audio input signal level (TAS5424B-Q1)                                                                             | AC-coupled input voltage                                                         | 0    |          | 0.5–2 <sup>(3)</sup>  | Vrms |
| T <sub>A</sub>                          | Ambient temperature                                                                                                       |                                                                                  | –40  |          | 105                   | °C   |
| T <sub>J</sub>                          | Junction temperature                                                                                                      | An adequate heat sink is required to keep T <sub>J</sub> within specified range. | –40  |          | 115                   | °C   |
| R <sub>L</sub>                          | Nominal speaker load impedance                                                                                            |                                                                                  | 2    | 4        |                       | Ω    |
| V <sub>PU</sub>                         | Pullup voltage supply (for open-drain logic outputs)                                                                      |                                                                                  | 3    | 3.3 or 5 | 5.5                   | V    |
| R <sub>PU_EXT</sub>                     | External pullup resistor on open-drain logic outputs                                                                      | Resistor connected between open-drain logic output and V <sub>PU</sub> supply    | 10   |          | 50                    | kΩ   |
| R <sub>PU_I2C</sub>                     | I <sup>2</sup> C pullup resistance on SDA and SCL pins                                                                    |                                                                                  | 1    | 4.7      | 10                    | kΩ   |
| R <sub>I2C_ADD</sub>                    | Total resistance of voltage divider for I <sup>2</sup> C address slave 1 or slave 2, connected between D_BYP and GND pins |                                                                                  | 10   |          | 50                    | kΩ   |
| R <sub>REXT</sub>                       | External resistance on REXT pin                                                                                           | 1% tolerance required                                                            | 19.8 | 20       | 20.2                  | kΩ   |
| C <sub>D_BYP</sub> , C <sub>A_BYP</sub> | External capacitance on D_BYP and A_BYP pins                                                                              |                                                                                  | 10   |          | 120                   | nF   |
| C <sub>OUT</sub>                        | External capacitance to GND on OUT_X pins                                                                                 |                                                                                  |      | 150      | 680                   | nF   |
| C <sub>IN</sub>                         | External capacitance to analog input pin in series with input signal                                                      |                                                                                  |      | 0.47     |                       | μF   |
| C <sub>FLY</sub>                        | Flying capacitor on charge pump                                                                                           |                                                                                  | 0.47 | 1        | 1.5                   | μF   |
| C <sub>P</sub>                          | Charge pump capacitor                                                                                                     | 50V needed for Load Dump                                                         | 0.47 | 1        | 1.5                   | μF   |
| C <sub>MUTE</sub>                       | MUTE pin capacitor                                                                                                        |                                                                                  | 100  | 220      | 1000                  | nF   |
| C <sub>OSCSYNC_MAX</sub>                | Allowed loading capacitance on OSC_SYNC pin                                                                               |                                                                                  |      | 75       |                       | pF   |

- (1) The *Recommended Operating Conditions* table specifies only that the device is functional in the given range. See the *Electrical Characteristics* table for specified performance limits.
- (2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB
- (3) Maximum recommended input voltage is determined by the gain setting.

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise noted):  $T_{Case} = 25^{\circ}C$ ,  $PVDD = 14.4 V$ ,  $R_L = 4 \Omega$ ,  $f_S = 417 kHz$ ,  $P_{out} = 1 W/ch$ ,  $R_{ext} = 20 k\Omega$ , AES17 Filter, default I<sup>2</sup>C settings, master mode operation (see application diagram)

| PARAMETER                         |                                                 | TEST CONDITIONS                                                               | MIN   | TYP  | MAX  | UNIT |
|-----------------------------------|-------------------------------------------------|-------------------------------------------------------------------------------|-------|------|------|------|
| OPERATING CURRENT                 |                                                 |                                                                               |       |      |      |      |
| IPVDD_IDLE                        | PVDD idle current                               | All four channels in MUTE mode                                                | 170   | 220  |      | mA   |
| IPVDD_HI-Z                        |                                                 | All four channels in Hi-Z mode                                                | 93    |      |      |      |
| IPVDD_STBY                        | PVDD standby current                            | STANDBY mode, T <sub>J</sub> ≤ 85°C                                           | 2     | 10   |      | µA   |
| OUTPUT POWER                      |                                                 |                                                                               |       |      |      |      |
| P <sub>OUT</sub>                  | Output power per channel                        | 4 Ω, PVDD = 14.4 V, THD+N ≤ 1%, 1 kHz, T <sub>c</sub> = 75°C                  | 23    |      |      | W    |
|                                   |                                                 | 4 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C                 | 25    | 28   |      |      |
|                                   |                                                 | 4 Ω, PVDD = 24 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C                   | 63    | 79   |      |      |
|                                   |                                                 | 2 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T <sub>c</sub> = 75°C                  | 38    |      |      |      |
|                                   |                                                 | 2 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C                 | 40    | 50   |      |      |
|                                   |                                                 | PBTL 2-Ω operation, PVDD = 24 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C    | 150   |      |      |      |
|                                   |                                                 | PBTL 1-Ω operation, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T <sub>c</sub> = 75°C  | 90    |      |      |      |
| EFF <sub>P</sub>                  | Power efficiency                                | 4 channels operating, 23-W output power/ch, L = 10 µH, T <sub>J</sub> ≤ 85°C  | 90%   |      |      |      |
| AUDIO PERFORMANCE                 |                                                 |                                                                               |       |      |      |      |
| V <sub>NOISE</sub>                | Noise voltage at output                         | Zero input, and A-weighting                                                   | 60    | 100  |      | µV   |
| Crosstalk                         | Channel crosstalk                               | P = 1W, f = 1 kHz, Enhanced Crosstalk Enabled via I <sup>2</sup> C (reg 0x10) | 70    | 85   |      | dB   |
| CMRR <sub>5424</sub>              | Common-mode rejection ratio (TAS5424B-Q1)       | f = 1 kHz, 1 Vrms referenced to GND, G = 26 dB                                | 60    | 75   |      | dB   |
| PSRR                              | Power supply rejection ratio                    | PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz                                           | 60    | 75   |      | dB   |
| THD+N                             | Total harmonic distortion + noise               | P = 1W, f = 1 kHz                                                             | 0.02% | 0.1% |      |      |
| f <sub>S</sub>                    | Switching frequency                             | Switching frequency selectable for AM interference avoidance                  | 336   | 357  | 378  | kHz  |
|                                   |                                                 |                                                                               | 392   | 417  | 442  |      |
|                                   |                                                 |                                                                               | 470   | 500  | 530  |      |
| R <sub>AIN</sub>                  | Analog input resistance                         | Internal shunt resistance on each input pin                                   | 63    | 85   | 106  | kΩ   |
| V <sub>IN_CM</sub>                | Common-mode input voltage                       | AC coupled common-mode input voltage (zero differential input)                | 1.3   |      |      | Vrms |
| V <sub>CM_INT</sub>               | Internal common-mode input bias voltage         | Internal bias applied to IN_M pin                                             | 3.3   |      |      | V    |
| G                                 | Voltage gain (V <sub>O</sub> /V <sub>IN</sub> ) | Source impedance = 0 Ω, gain measurement taken at 1 W of power per channel    | 11    | 12   | 13   | dB   |
|                                   |                                                 |                                                                               | 19    | 20   | 21   |      |
|                                   |                                                 |                                                                               | 25    | 26   | 27   |      |
|                                   |                                                 |                                                                               | 31    | 32   | 33   |      |
| G <sub>CH</sub>                   | Channel-to-channel variation                    | Any gain commanded                                                            | −1    | 0    | 1    | dB   |
| PWM OUTPUT STAGE                  |                                                 |                                                                               |       |      |      |      |
| R <sub>DSon</sub>                 | FET drain-to-source resistance                  | Not including bond wire resistance, T <sub>J</sub> = 25°C                     | 65    | 90   |      | mΩ   |
| V <sub>O_OFFSET</sub>             | Output offset voltage                           | Zero input signal, G = 26 dB                                                  | ±10   | ±50  |      | mV   |
| PVDD OVERVOLTAGE (OV) PROTECTION  |                                                 |                                                                               |       |      |      |      |
| V <sub>OV_SET</sub>               | PVDD overvoltage shutdown set                   |                                                                               | 24.6  | 26.4 | 28.2 | V    |
| V <sub>OV_CLEAR</sub>             | PVDD overvoltage shutdown clear                 |                                                                               | 24.4  | 25.9 | 27.4 |      |
| PVDD UNDERVOLTAGE (UV) PROTECTION |                                                 |                                                                               |       |      |      |      |
| V <sub>UV_SET</sub>               | PVDD undervoltage shutdown set                  |                                                                               | 4.9   | 5.3  | 5.6  | V    |
| V <sub>UV_CLEAR</sub>             | PVDD undervoltage shutdown clear                |                                                                               | 6.2   | 6.6  | 7.0  | V    |
| AVDD                              |                                                 |                                                                               |       |      |      |      |
| V <sub>A_BYP</sub>                | A_BYP pin voltage                               |                                                                               | 6.5   |      |      | V    |
| V <sub>A_BYP_UV_SET</sub>         | A_BYP UV voltage                                |                                                                               | 4.8   |      |      | V    |
| V <sub>A_BYP_UV_CLEAR</sub>       | Recovery voltage A_BYP UV                       |                                                                               | 5.3   |      |      | V    |
| DVDD                              |                                                 |                                                                               |       |      |      |      |
| V <sub>D_BYP</sub>                | D_BYP pin voltage                               |                                                                               | 3.3   |      |      | V    |

## ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted):  $T_{Case} = 25^{\circ}C$ ,  $PVDD = 14.4\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f_s = 417\text{ kHz}$ ,  $P_{out} = 1\text{ W/ch}$ ,  $R_{ext} = 20\text{ k}\Omega$ , AES17 Filter, default I<sup>2</sup>C settings, master mode operation (see application diagram)

| PARAMETER                                       |                                                                            | TEST CONDITIONS                                                   | MIN  | TYP  | MAX  | UNIT |
|-------------------------------------------------|----------------------------------------------------------------------------|-------------------------------------------------------------------|------|------|------|------|
| POWER-ON RESET (POR)                            |                                                                            |                                                                   |      |      |      |      |
| V <sub>POR</sub>                                | PVDD voltage for POR                                                       | I <sup>2</sup> C active above this voltage                        |      |      | 3.5  | V    |
| V <sub>POR_HY</sub>                             | PVDD recovery hysteresis voltage for POR                                   |                                                                   |      | 0.1  |      | V    |
| REXT                                            |                                                                            |                                                                   |      |      |      |      |
| V <sub>REXT</sub>                               | Rext pin voltage                                                           |                                                                   |      | 1.27 |      | V    |
| CHARGE PUMP (CP)                                |                                                                            |                                                                   |      |      |      |      |
| V <sub>CPUV_SET</sub>                           | CP undervoltage                                                            |                                                                   |      | 4.8  |      | V    |
| V <sub>CPUV_CLEAR</sub>                         | Recovery voltage for CP UV                                                 |                                                                   |      | 4.9  |      | V    |
| OVERTEMPERATURE (OT) PROTECTION                 |                                                                            |                                                                   |      |      |      |      |
| T <sub>OTW1_CLEAR</sub>                         | Junction temperature for overtemperature warning                           |                                                                   | 96   | 112  | 128  | °C   |
| T <sub>OTW1_SET</sub> / T <sub>OTW2_CLEAR</sub> |                                                                            |                                                                   | 106  | 122  | 138  |      |
| T <sub>OTW2_SET</sub> / T <sub>OTW3_CLEAR</sub> |                                                                            |                                                                   | 116  | 132  | 148  |      |
| T <sub>OTW3_SET</sub> / T <sub>OTSD_CLEAR</sub> |                                                                            |                                                                   | 126  | 142  | 158  |      |
| T <sub>OTSD</sub>                               | Junction temperature for overtemperature shutdown                          |                                                                   | 136  | 152  | 168  |      |
| T <sub>FB</sub>                                 | Junction temperature for overtemperature foldback                          | Per channel                                                       | 130  | 150  | 170  |      |
| CURRENT LIMITING PROTECTION                     |                                                                            |                                                                   |      |      |      |      |
| I <sub>LIM</sub>                                | Current limit (load current)                                               | Level 1                                                           | 5.5  | 7.3  | 9.0  | A    |
|                                                 |                                                                            | Level 2 (default)                                                 | 10.6 | 12.7 | 15.0 |      |
| OVERCURRENT (OC) SHUTDOWN PROTECTION            |                                                                            |                                                                   |      |      |      |      |
| I <sub>MAX</sub>                                | Maximum current (peak output current)                                      | Level 1                                                           | 7.8  | 9.8  | 12.2 | A    |
|                                                 |                                                                            | Level 2 (default), Any short to supply, ground, or other channels | 11.9 | 14.8 | 17.7 |      |
| TWEETER DETECT                                  |                                                                            |                                                                   |      |      |      |      |
| I <sub>TH_TW</sub>                              | Load current threshold for tweeter detect                                  |                                                                   | 330  | 445  | 560  | mA   |
| I <sub>LIM_TW</sub>                             | Load current limit for tweeter detect                                      |                                                                   |      | 2.1  |      | A    |
| STANDBY MODE                                    |                                                                            |                                                                   |      |      |      |      |
| V <sub>IH_STBY</sub>                            | STANDBY input voltage for logic-level high                                 |                                                                   | 2    |      |      | V    |
| V <sub>IL_STBY</sub>                            | STANDBY input voltage for logic-level low                                  |                                                                   |      |      | 0.7  | V    |
| I <sub>STBY_PIN</sub>                           | STANDBY pin current                                                        |                                                                   |      | 0.1  | 0.2  | µA   |
| MUTE MODE                                       |                                                                            |                                                                   |      |      |      |      |
| G <sub>MUTE</sub>                               | Output attenuation                                                         | MUTE pin ≤ 0.5 V + 200mS or I <sup>2</sup> C Mute Enabled         |      | 100  |      | dB   |
| DC DETECT                                       |                                                                            |                                                                   |      |      |      |      |
| V <sub>TH_DC_TOL</sub>                          | DC detect threshold tolerance                                              |                                                                   |      | 25   |      | %    |
| t <sub>DCD</sub>                                | DC detect step response time for four channels                             |                                                                   |      |      | 5.3  | s    |
| CLIP_OTW REPORT                                 |                                                                            |                                                                   |      |      |      |      |
| V <sub>OH_CLIPOTW</sub>                         | CLIP_OTW pin output voltage for logic level high (open-drain logic output) | External 47-kΩ pullup resistor to 3 V–5.5 V                       | 2.4  |      |      | V    |
| V <sub>OL_CLIPOTW</sub>                         | CLIP_OTW pin output voltage for logic level low (open-drain logic output)  |                                                                   |      |      | 0.5  | V    |
| t <sub>DELAY_CLIPDET</sub>                      | CLIP_OTW signal delay when output clipping detected                        |                                                                   |      |      | 20   | µs   |
| FAULT REPORT                                    |                                                                            |                                                                   |      |      |      |      |
| V <sub>OH_FAULT</sub>                           | FAULT pin output voltage for logic-level high (open-drain logic output)    | External 47-kΩ pullup resistor to 3 V–5.5 V                       | 2.4  |      |      | V    |
| V <sub>OL_FAULT</sub>                           | FAULT pin output voltage for logic-level low (open-drain logic output)     |                                                                   |      |      | 0.5  |      |
| OPEN/SHORT DIAGNOSTICS                          |                                                                            |                                                                   |      |      |      |      |

## ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted):  $T_{Case} = 25^{\circ}C$ ,  $PVDD = 14.4\text{ V}$ ,  $R_L = 4\ \Omega$ ,  $f_S = 417\text{ kHz}$ ,  $P_{out} = 1\text{ W/ch}$ ,  $R_{ext} = 20\text{ k}\Omega$ , AES17 Filter, default I<sup>2</sup>C settings, master mode operation (see application diagram)

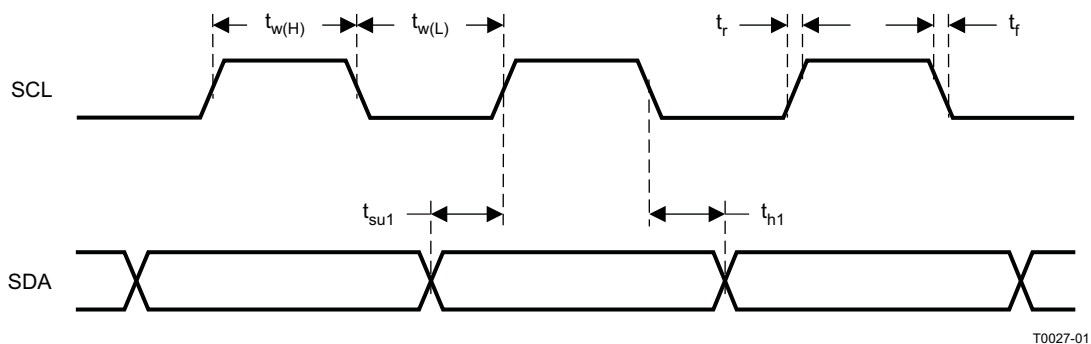
| PARAMETER                           |                                                                        | TEST CONDITIONS                                                                       | MIN  | TYP  | MAX  | UNIT               |
|-------------------------------------|------------------------------------------------------------------------|---------------------------------------------------------------------------------------|------|------|------|--------------------|
| R <sub>S2P</sub> , R <sub>S2G</sub> | Maximum resistance to detect a short from OUT pin(s) to PVDD or ground |                                                                                       |      |      | 200  | Ω                  |
| R <sub>OPEN_LOAD</sub>              | Minimum load resistance to detect open circuit                         | Including speaker wires                                                               | 300  | 740  | 1300 | Ω                  |
| R <sub>SHORTED_LOAD</sub>           | Maximum load resistance to detect short circuit                        | Including speaker wires                                                               | 0.5  | 1.0  | 1.5  | Ω                  |
| I <sup>2</sup> C ADDRESS DECODER    |                                                                        |                                                                                       |      |      |      |                    |
| t <sub>LATCH_I2CADDR</sub>          | Time delay to latch I <sup>2</sup> C address after POR                 |                                                                                       |      | 300  |      | μs                 |
| V <sub>I2C_ADDR</sub>               | Voltage on I2C_ADDR pin for address 0                                  | Connect to GND                                                                        | 0%   | 0%   | 15%  | V <sub>D_BYP</sub> |
|                                     | Voltage on I2C_ADDR pin for address 1                                  | External resistors in series between D_BYP and GND as a voltage divider               | 25%  | 35%  | 45%  |                    |
|                                     | Voltage on I2C_ADDR pin for address 2                                  |                                                                                       | 55%  | 65%  | 75%  |                    |
|                                     | Voltage on I2C_ADDR pin for address 3                                  | Connect to D_BYP                                                                      | 85%  | 100% | 100% |                    |
| I <sup>2</sup> C                    |                                                                        |                                                                                       |      |      |      |                    |
| t <sub>HOLD_I2C</sub>               | Power-on hold time before I <sup>2</sup> C communication               | <u>STANDBY</u> high                                                                   |      | 1    |      | ms                 |
| f <sub>SCL</sub>                    | SCL clock frequency                                                    |                                                                                       |      |      | 400  | kHz                |
| V <sub>IH_SCL</sub>                 | SCL pin input voltage for logic-level high                             | R <sub>PU_I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V                      | 2.1  |      | 5.5  | V                  |
| V <sub>IL_SCL</sub>                 | SCL pin input voltage for logic-level low                              |                                                                                       | −0.5 |      | 1.1  | V                  |
| V <sub>OH_SDA</sub>                 | SDA pin output voltage for logic-level high                            | I <sup>2</sup> C read, R <sub>I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V  | 2.4  |      |      | V                  |
| V <sub>OL_SDA</sub>                 | SDA pin output voltage for logic-level low                             | I <sup>2</sup> C read, 3-mA sink current                                              |      |      | 0.4  | V                  |
| V <sub>IH_SDA</sub>                 | SDA pin input voltage for logic-level high                             | I <sup>2</sup> C write, R <sub>I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V | 2.1  |      | 5.5  | V                  |
| V <sub>IL_SDA</sub>                 | SDA pin input voltage for logic-level low                              | I <sup>2</sup> C write, R <sub>I2C</sub> = 5-kΩ pullup, supply voltage = 3.3 V or 5 V | −0.5 |      | 1.1  | V                  |
| C <sub>i</sub>                      | Capacitance for SCL and SDA pins                                       |                                                                                       |      |      | 10   | pF                 |
| OSCILLATOR                          |                                                                        |                                                                                       |      |      |      |                    |
| V <sub>OH_OSCSYNC</sub>             | OSC_SYNC pin output voltage for logic-level high                       | I2C_ADDR pin set to MASTER mode                                                       | 2.4  |      |      | V                  |
| V <sub>OL_OSCSYNC</sub>             | OSC_SYNC pin output voltage for logic-level low                        |                                                                                       |      |      | 0.5  | V                  |
| V <sub>IH_OSCSYNC</sub>             | OSC_SYNC pin input voltage for logic-level high                        | I2C_ADDR pin set to SLAVE mode                                                        | 2    |      |      | V                  |
| V <sub>IL_OSCSYNC</sub>             | OSC_SYNC pin input voltage for logic-level low                         |                                                                                       |      |      | 0.8  | V                  |
| f <sub>OSC_SYNC</sub>               | OSC_SYNC pin clock frequency                                           | I2C_ADDR pin set to MASTER mode, f <sub>S</sub> = 500 kHz                             | 3.76 | 4.0  | 4.24 | MHz                |
|                                     |                                                                        | I2C_ADDR pin set to MASTER mode, f <sub>S</sub> = 417 kHz                             | 3.13 | 3.33 | 3.63 |                    |
|                                     |                                                                        | I2C_ADDR pin set to MASTER mode, f <sub>S</sub> = 357 kHz                             | 2.68 | 2.85 | 3.0  |                    |

## TIMING REQUIREMENTS FOR I<sup>2</sup>C INTERFACE SIGNALS

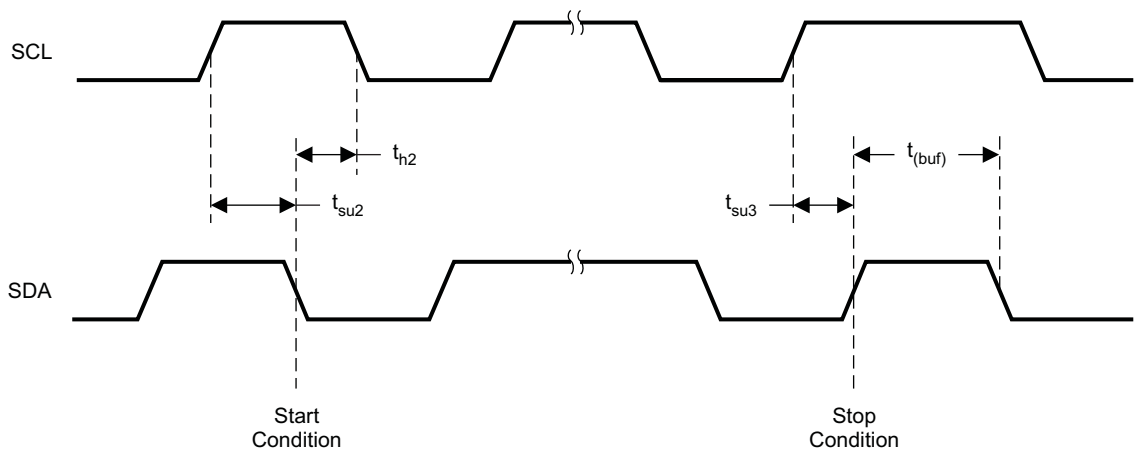
over recommended operating conditions (unless otherwise noted)

| PARAMETER  |                                                                      | MIN              | TYP | MAX | UNIT    |
|------------|----------------------------------------------------------------------|------------------|-----|-----|---------|
| $t_r$      | Rise time for both SDA and SCL signals                               |                  |     | 300 | ns      |
| $t_f$      | Fall time for both SDA and SCL signals                               |                  |     | 300 | ns      |
| $t_{w(H)}$ | SCL pulse duration, high                                             | 0.6              |     |     | $\mu$ s |
| $t_{w(L)}$ | SCL pulse duration, low                                              | 1.3              |     |     | $\mu$ s |
| $t_{su2}$  | Setup time for START condition                                       | 0.6              |     |     | $\mu$ s |
| $t_{h2}$   | START condition hold time after which first clock pulse is generated | 0.6              |     |     | $\mu$ s |
| $t_{su1}$  | Data setup time                                                      | 100              |     |     | ns      |
| $t_{h1}$   | Data hold time                                                       | 0 <sup>(1)</sup> |     |     | ns      |
| $t_{su3}$  | Setup time for STOP condition                                        | 0.6              |     |     | $\mu$ s |
| $C_B$      | Load capacitance for each bus line                                   |                  |     | 400 | pF      |

- (1) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.



**Figure 1. SCL and SDA Timing**



**Figure 2. Timing for Start and Stop Conditions**

## TYPICAL CHARACTERISTICS

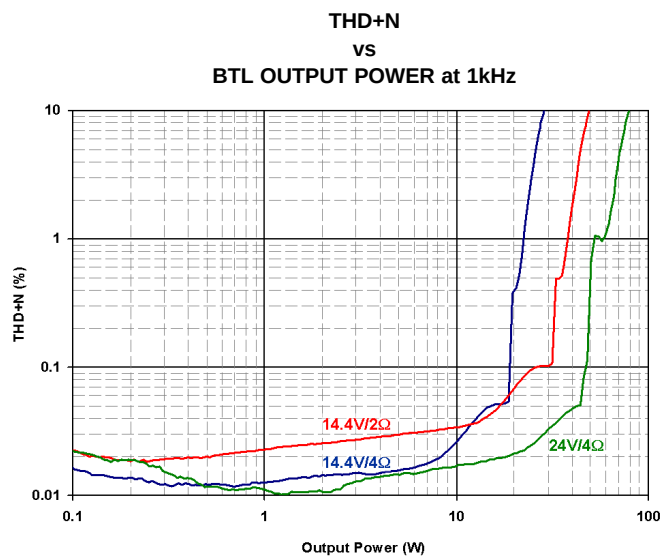


Figure 3.

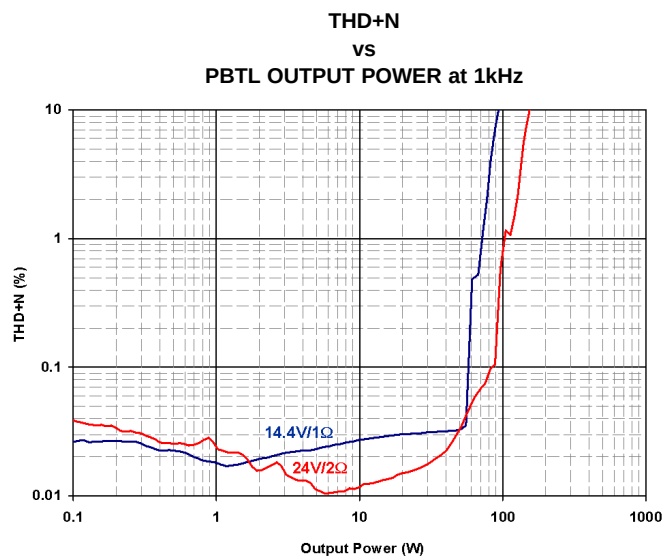


Figure 4.

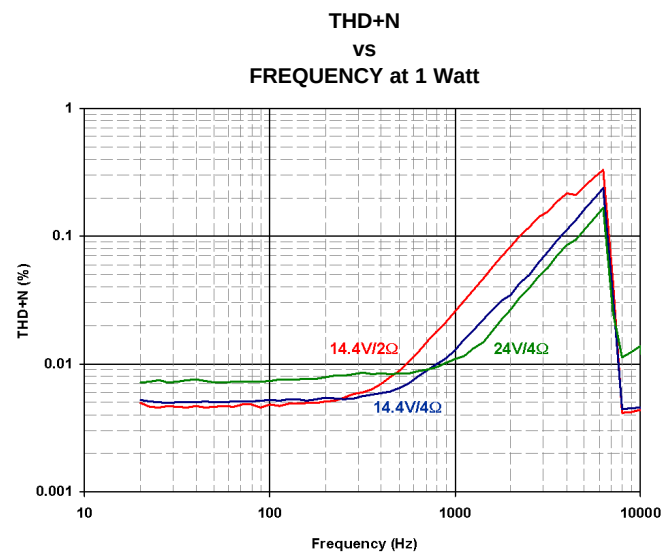


Figure 5.

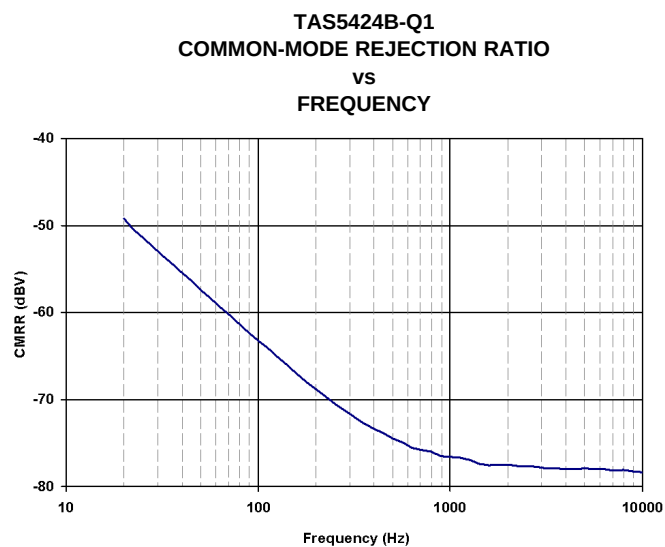


Figure 6.

## TYPICAL CHARACTERISTICS (continued)

CROSSTALK  
VS  
FREQUENCY

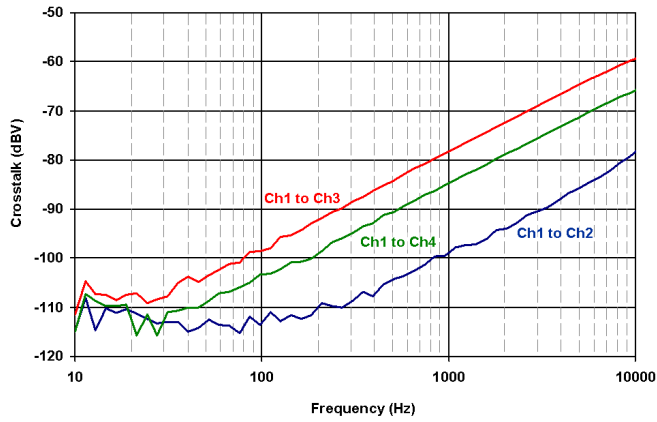


Figure 7.

NOISE FFT

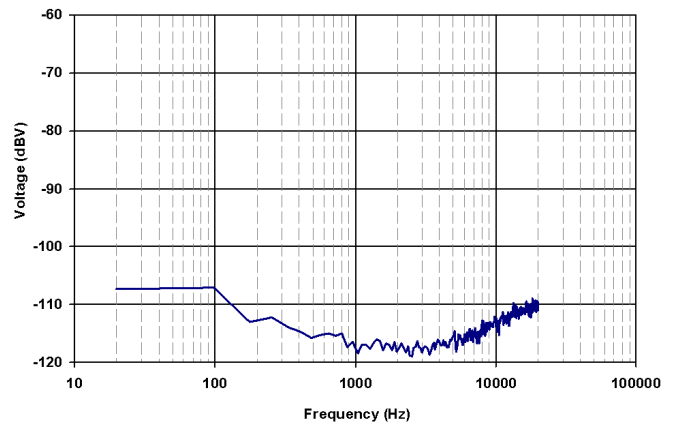


Figure 8.

EFFICIENCY,  
FOUR CHANNELS AT 4  $\Omega$  EACH

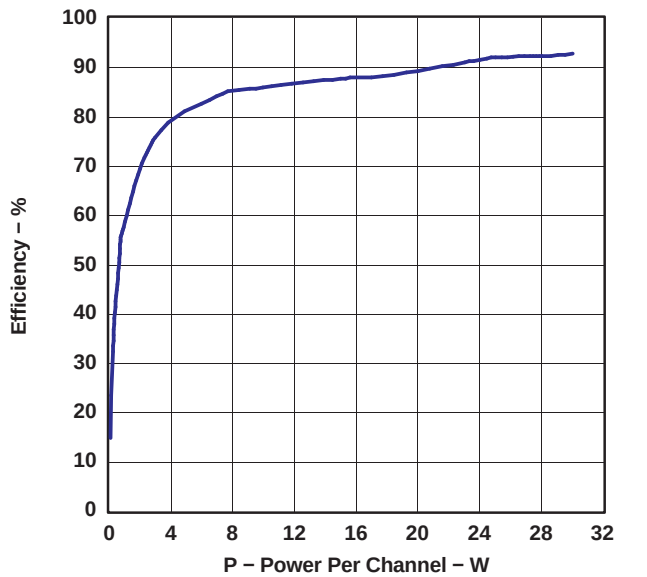


Figure 9.

DEVICE POWER DISSIPATION  
FOUR CHANNELS AT 4  $\Omega$  EACH

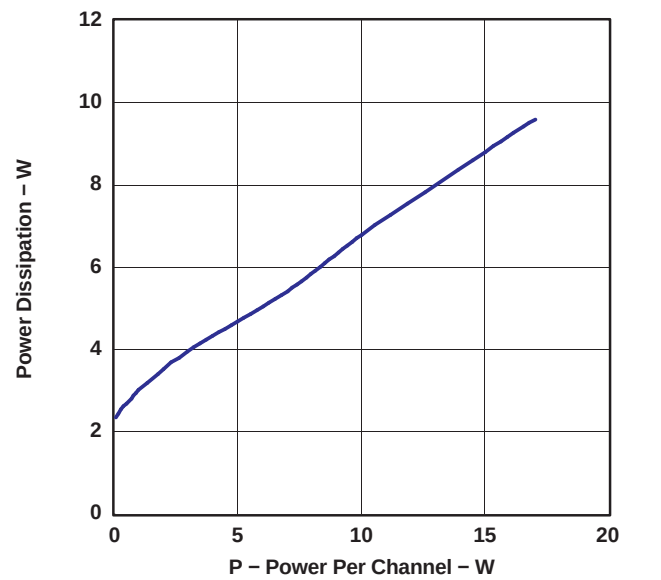


Figure 10.

## DESCRIPTION OF OPERATION

### OVERVIEW

The TAS5414B-Q1 and TAS5424B-Q1 are single-chip, four-channel, analog-input audio amplifiers for use in the automotive environment. The design uses an ultra-efficient class-D technology developed by Texas Instruments, but with changes needed by the automotive industry. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional class-AB solutions.

There are eight core design blocks:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I<sup>2</sup>C serial communication bus

### Preamplifier

The preamplifier is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance allows the use of low-cost input capacitors while still achieving extended low-frequency response. The preamplifier is powered by a dedicated, internally regulated supply, which gives it excellent noise immunity and channel separation. Also included in the preamp are:

1. **Mute Pop-and-Click Control**— The device ramps the gain gradually when a mute or play command is received. Another form of click and pop can be caused by the start or stopping of switching in a class-D amplifier. The TAS5414B-Q1 and TAS5424B-Q1 incorporate a patented method to reduce the pop energy during the switching startup and shutdown sequence. Fault conditions require rapid protection response by the TAS5414B-Q1 and the TAS5424B-Q1, which do not have time to ramp the gain down in a pop-free manner. The device transitions into Hi-Z mode when an OV, UV, OC, OT, or DC fault is encountered. Also, activation of the STANDBY pin may not be pop-free.
2. **Gain Control**—The four gain settings are set in the preamplifier via I<sup>2</sup>C control registers. The gain is set outside of the global feedback resistors of the device, thus allowing for stability of the system at all gain settings with properly loaded conditions.

### Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TAS5414B-Q1 and TAS5424B-Q1, the modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0–100% modulation capability. The patented PWM uses clipping recovery circuitry to eliminate the deep saturation characteristic of PWMs when the input signal exceeds the modulator waveform.

### Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high-current, full-bridge, power FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

### Power FETs

The BTL output for each channel comprises four rugged N-channel 30-V 65 mΩ FETs for high efficiency and maximum power transfer to the load. These FETs are designed to handle large voltage transients during load dump.

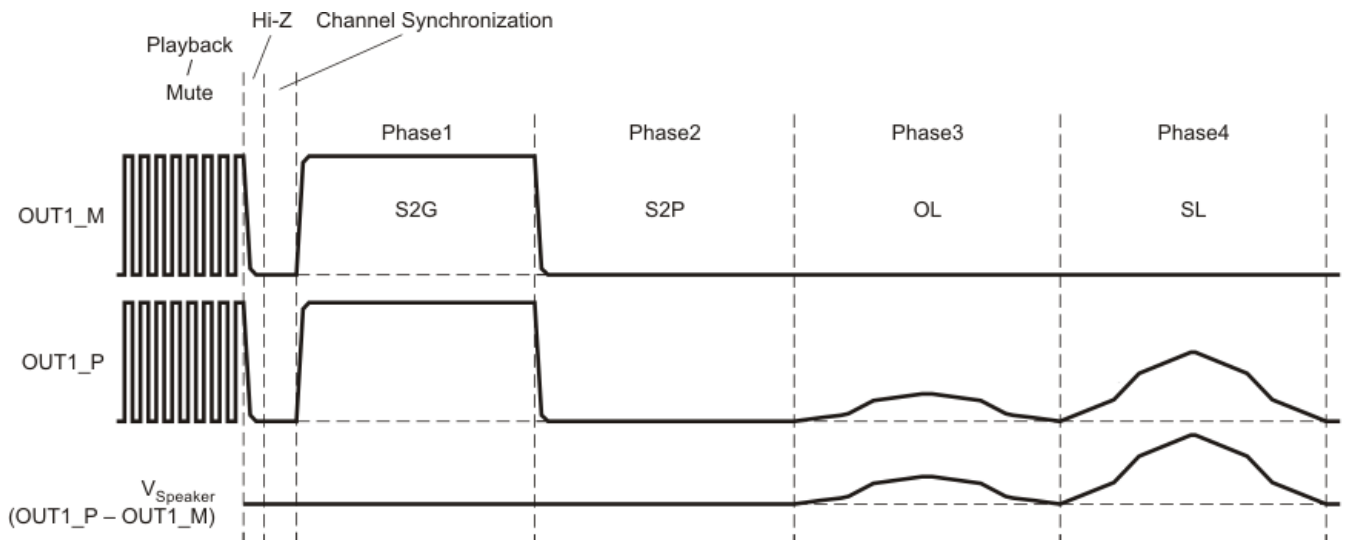
## Load Diagnostics

The device incorporates load diagnostic circuitry designed to help pinpoint the nature of output misconnections during installation. The TAS5414B-Q1 and the TAS5424B-Q1 include functions for detecting and determining the status of output connections. The following diagnostics are supported:

- Short to GND
- Short to PVDD
- Short across load
- Open load
- Tweeter detection

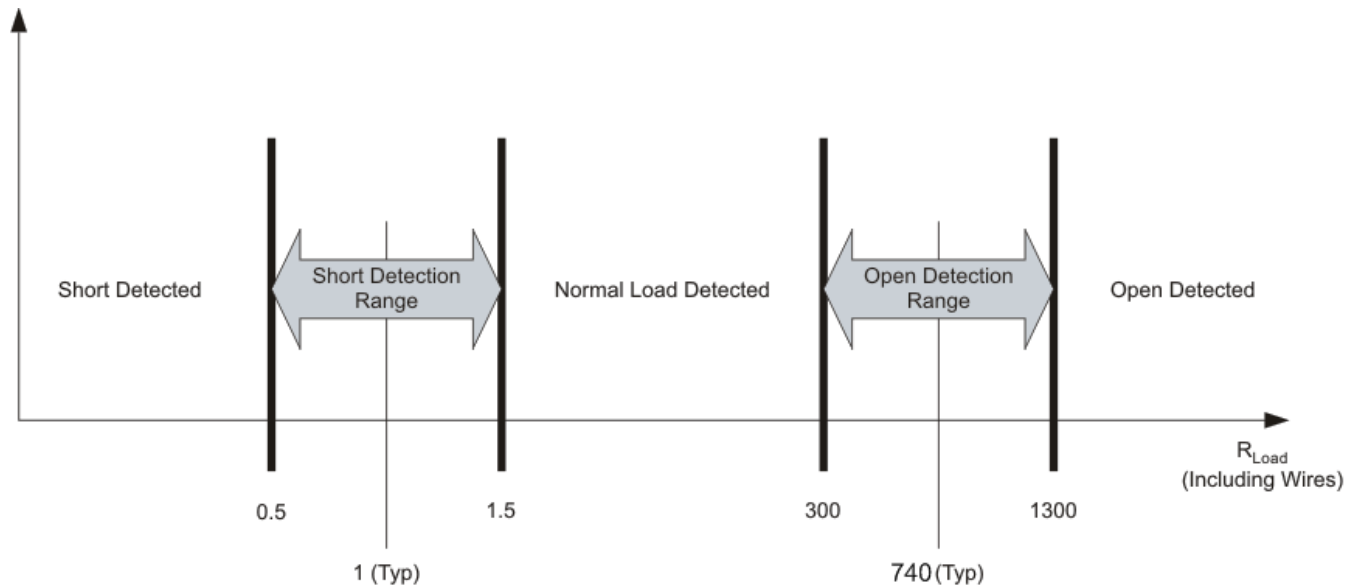
The presence of any of the short or open conditions is reported to the system via I<sup>2</sup>C register read. The tweeter detect status can be read from the CLIP\_OTW pin when properly configured.

1. **Output Short and Open Diagnostics**—The device contains circuitry designed to detect shorts and open conditions on the outputs. The load diagnostic function can only be invoked when the output is in the Hi-Z mode. There are four phases of test during load diagnostics and two levels of test. In the full level, all channels must be in the Hi-Z state. All four phases are tested on each channel, all four channels at the same time. When fewer than four channels are in Hi-Z, the reduced level of test is the only available option. In the reduced level, only short to PVDD and short to GND can be tested. Load diagnostics can occur at power up before the amplifier is moved out of Hi-Z mode. If the amplifier is already in play mode, it must *Mute* and then *Hi-Z* before the load diagnostic can be performed. By performing the mute function, the normal pop- and click-free transitions occur before the diagnostics begin. The diagnostics are performed as shown in Figure 11. Figure 12 shows the impedance ranges for the open-load and shorted-load diagnostics. The results of the diagnostic are read from the diagnostic register for each channel via I<sup>2</sup>C. With the default settings and MUTE capacitor the S2G and S2P phase take ~20mS each, the OL phase takes ~100mS, and the SL takes ~230mS.



T0188-01

**Figure 11. Load Diagnostics Sequence of Events**



M0067-01

**Figure 12. Open and Shorted Load Detection**

2. **Tweeter Detection**—Tweeter detection is an alternate operating mode that is used to determine the proper connection of a frequency dependent load (such as a speaker with a crossover). Tweeter detection is invoked via I<sup>2</sup>C, and all four channels should be tested individually. Tweeter detection uses the average cycle-by-cycle current limit circuit (see [CBC](#) section) to measure the current delivered to the load. The proper implementation of this diagnostic function is dependent on the amplitude of a user-supplied test signal and on the impedance versus frequency curve of the acoustic load. The system (external to the TAS5414B-Q1 and TAS5424B-Q1) must generate a signal to which the load will respond. The frequency and amplitude of this signal must be calibrated by the user to result in a current draw that is greater than the tweeter detection threshold when the load under test is present, and less than the detection threshold if the load is not properly connected. The current level for the tweeter detection threshold, as well as the maximum current that can safely be delivered to a load when in tweeter detection mode, can be found in the Electrical Characteristics section of the datasheet. The tweeter detection results are reported on the CLIP\_OTW pin during the application of the test signal. When tweeter detection is activated (indicating that the tested load is present), pulses on the CLIP\_OTW pin begin to toggle. The pulses on the CLIP\_OTW pins will report low whenever the current detection threshold is exceeded, and the pin will remain low until the threshold is no longer exceeded. The minimum low-pulse period that can be expected is equal to one period of the switching frequency. Having an input signal that increases the amount of time that the detector is activated (e. g. increasing the amplitude of the input signal) will increase the amount of time for which the pin reports low.  
**NOTE:** Because tweeter detection is an alternate *operating mode*, the channels to be tested must be placed in Play mode (via register 0x0C) after tweeter detection has been activated in order to commence the detection process. Additionally, the CLIP\_OTW pin must be set up via register 0x0A to report the results of tweeter detection.

## Protection and Monitoring

1. **Cycle-By-Cycle Current Limit (CBC)**—The CBC current-limiting circuit terminates each PWM pulse to limit the output current flow when the average current limit ( $I_{LIM}$ ) threshold is exceeded. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, where power is temporarily limited at the peaks of the musical signal and normal operation continues without disruption when the overload is removed. The TAS5414B-Q1 and TAS5424B-Q1 do not prematurely shut down in this condition. All four channels continue in play mode and pass signal.
2. **Overcurrent Shutdown (OCS)**—Under severe short-circuit events, such as a short to PVDD or ground, a peak-current detector is used, and the affected channel shuts down in 200  $\mu$ s to 390  $\mu$ s if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels are shut down in such a scenario.

The user may restart the affected channel via I<sup>2</sup>C. An OCSD event activates the fault pin, and the affected channel(s) are recorded in the I<sup>2</sup>C fault register. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

3. **DC Detect**—This circuit detects a dc offset continuously during normal operation at the output of the amplifier. If the dc offset reaches the level defined in the I<sup>2</sup>C registers for the specified time period, the circuit triggers. By default a dc detection event does not shut the output down. The shutdown function can be enabled or disabled via I<sup>2</sup>C. If enabled, the triggered channel shuts down, but the others remain playing and the FAULT pin is asserted. The dc level is defined in I<sup>2</sup>C registers.
4. **Clip Detect**—The clip detect circuit alerts the user to the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, a signal is passed to the CLIP\_OTW pin and it is asserted until the 100% duty-cycle PWM signal is no longer present. All four channels are connected to the same CLIP\_OTW pin. Through I<sup>2</sup>C, the CLIP\_OTW signal can be changed to clip-only, OTW-only, or both. A fourth mode, used only during diagnostics, is the option to report tweeter detection events on this pin (see the [Tweeter Detection](#) section). The microcontroller in the system can monitor the signal at the CLIP\_OTW pin and may be configured to reduce the volume to all four channels in an active clipping-prevention circuit.
5. **Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD) and Thermal Foldback**—By default, the CLIP\_OTW pin is set to indicate an OTW. This can be changed via I<sup>2</sup>C commands. If selected to indicate a temperature warning, the CLIP\_OTW pin is asserted when the die temperature reaches warning level 1 as shown in the electrical specs. The OTW has three temperature thresholds with a 10°C hysteresis. Each threshold is indicated in I<sup>2</sup>C register 0x04 bits 5, 6, and 7. The device still functions until the temperature reaches the OTSD threshold, at which time the outputs are placed into Hi-Z mode and the FAULT pin is asserted. I<sup>2</sup>C is still active in the event of an OTSD and the registers can be read for faults, but all audio ceases abruptly. After the OTSD resets the device can be turned back on through I<sup>2</sup>C. The OTW is still indicated until the temperature drops below warning level 1. The Thermal Foldback decreases the channel gain.
6. **Undervoltage (UV) and Power-on-Reset (POR)**—The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the FAULT pin is asserted and the I<sup>2</sup>C register is updated, depending on which voltage caused the event. Power-on-reset (POR) occurs when PVDD drops low enough. A POR event causes the I<sup>2</sup>C to go into a high-impedance state. After the device recovers from the POR event, the device must be re-initialized via I<sup>2</sup>C.
7. **Overvoltage (OV) and Load Dump**—The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the FAULT pin is asserted and the I<sup>2</sup>C register is updated. The device can withstand 50-V load-dump voltage spikes. Also depicted in this graph are the voltage thresholds for normal operation region, overvoltage operation region, and load-dump protection region. [Figure 11](#) shows the regions of operating voltage and the profile of the load dump event.

## Power Supply

The power for the device is most commonly provided by a car battery that can have a large voltage range. PVDD is a filtered battery voltage, and it is the supply for the output FETs and the low-side FET gate driver. The high-side FET gate driver is supplied by a charge pump (CP) supply. The charge pump supplies the gate drive voltage for all four channels. The analog circuitry is powered by AVDD, which is provided by an internal linear regulator. A 0.1µF/10V external bypass capacitor is needed at the A\_BYP pin for this supply. It is recommended that no external components except the bypass capacitor be attached to this pin. The digital circuitry is powered by DVDD, which is provided by an internal linear regulator. A 0.1µF/10V external bypass capacitor is needed at the D\_BYP pin. It is recommended that no external components except the bypass capacitor be attached to this pin.

The TAS5414B-Q1 and TAS5424B-Q1 can withstand fortuitous open ground and power conditions. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs. The diagnostic capability allows the speakers and speaker wires to be debugged, eliminating the need to remove the amplifier to diagnose the problem.

## I<sup>2</sup>C Serial Communication Bus

The device communicates with the system processor via the I<sup>2</sup>C serial communication bus as an I<sup>2</sup>C slave-only device. The processor can poll the device via I<sup>2</sup>C to determine the operating status. All fault conditions and detections are reported via I<sup>2</sup>C. There are also numerous features and operating conditions that can be set via I<sup>2</sup>C.

The I<sup>2</sup>C bus allows control of the following configurations:

- Independent gain control of each channel. The gain can be set to 12 dB, 20 dB, 26 dB, and 32 dB.
- Select AM non-interference switching frequency
- Select the function of OTW\_CLIP pin
- Enable or disable dc detect function with selectable threshold
- Place channel in Hi-Z (switching stopped) mode (mute)
- Select tweeter detect, set detect threshold and initiate function
- Initiate open/short load diagnostic
- Reset faults and return to normal switching operation from Hi-Z mode (unmute)

In addition to the standard SDA and SCL pins for the I<sup>2</sup>C bus, the TAS5414B-Q1 and the TAS5424B-Q1 include a single pin that allows up to four devices to work together in a system with no additional hardware required for communication or synchronization. The I2C\_ADDR pin sets the device in master or slave mode and selects the I<sup>2</sup>C address for that device. Tie I2C\_ADDR to DGND for master, to 1.2 Vdc for slave 1, to 2.4 Vdc for slave 2, and to D\_BYP for slave 3. The OSC\_SYNC pin is used to synchronize the internal clock oscillators and thereby avoid beat frequencies. An external oscillator can also be applied to this pin for external control of the switching frequency.

**Table 2. Table 7. I2C\_ADDR Pin Connection**

| DESCRIPTION                     | I2C_ADDR PIN CONNECTION                                                            | I <sup>2</sup> C ADDRESS |
|---------------------------------|------------------------------------------------------------------------------------|--------------------------|
| TAS5414B-Q1/5424 0 (OSC MASTER) | To SGND pin                                                                        | 0xD8/D9                  |
| TAS5414B-Q1/5424 1 (OSC SLAVE1) | 35% DVDD (resistive voltage divider between D_BYP pin and SGND pin) <sup>(1)</sup> | 0xDA/DB                  |
| TAS5414B-Q1/5424 2 (OSC SLAVE2) | 65% DVDD (resistive voltage divider between D_BYP pin and SGND pin) <sup>(1)</sup> | 0xDC/DD                  |
| TAS5414B-Q1/5424 3 (OSC SLAVE3) | To D_BYP pin                                                                       | 0xDE/DF                  |

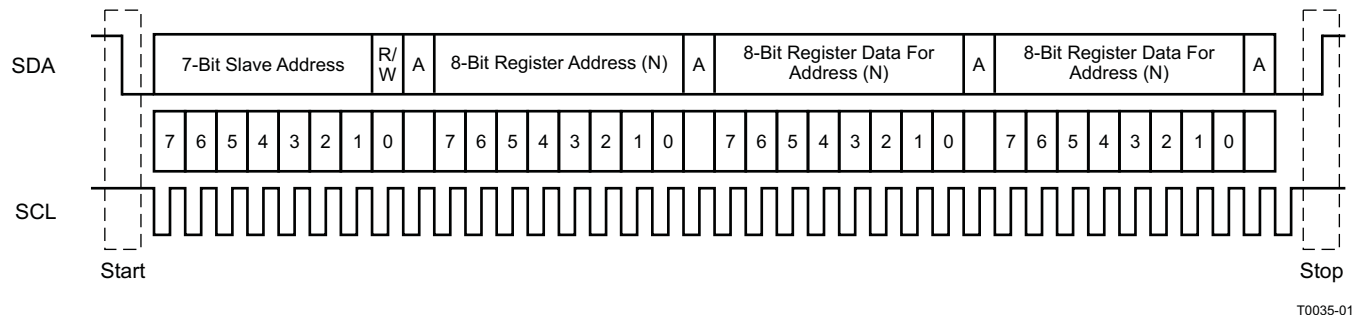
(1) R<sub>I2C\_ADDR</sub> with 5% or better tolerance is recommended.

## I<sup>2</sup>C Bus Protocol

The TAS5414B-Q1 and TAS5424B-Q1 have a bidirectional serial control interface that is compatible with the Inter IC (I<sup>2</sup>C) bus protocol and supports 400-kbps data transfer rates for random and sequential write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The I<sup>2</sup>C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in [Figure 13](#). The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The TAS5414B-Q1 and TAS5424B-Q1 hold SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the master

transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

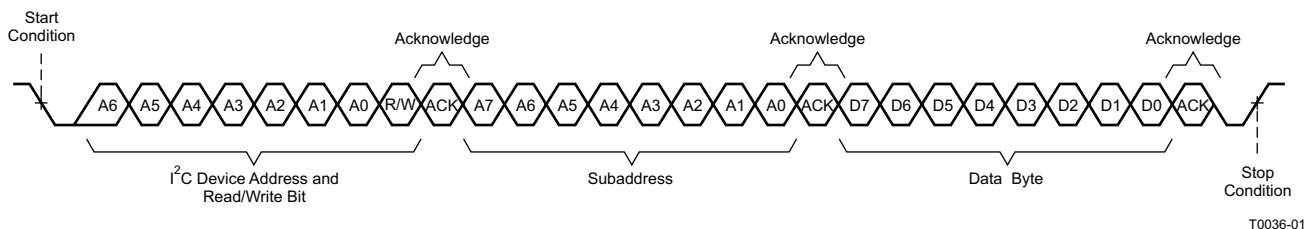


**Figure 13. Typical I²C Sequence**

Use the I2C\_ADDR pin (pin 2) to program the device for one of four addresses. These four addresses are licensed I²C addresses and do not conflict with other licensed I²C audio devices. To communicate with the TAS5414B-Q1 and the TAS5424B-Q1, the I²C master uses addresses shown in Figure 13. Read and write data can be transmitted using single-byte or multiple-byte data transfers.

## Random Write

As shown in Figure 14, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the TAS5414B-Q1 or TAS5424B-Q1 device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the TAS5414B-Q1 or TAS5424B-Q1 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5414B-Q1 or TAS5424B-Q1 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.



**Figure 14. Random Write Transfer**

## Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master device to TAS5414B-Q1 or TAS5424B-Q1 as shown in Figure 14. After receiving each data byte, the TAS5414B-Q1 or TAS5424B-Q1 responds with an acknowledge bit and the I²C subaddress is automatically incremented by one.

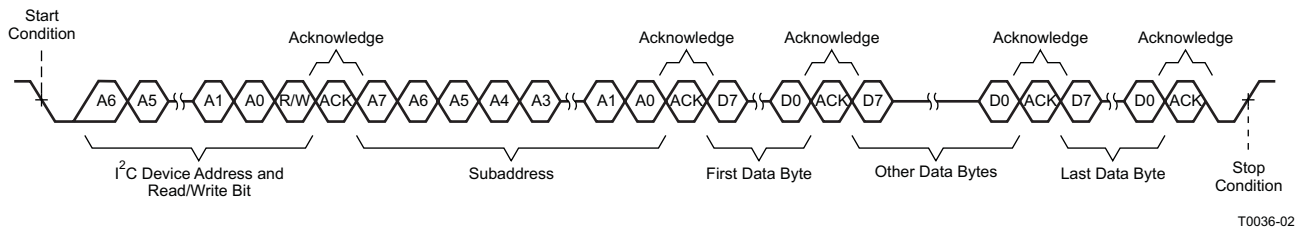


Figure 15. Sequential Write Transfer

## Random Read

As shown in Figure 16, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I<sup>2</sup>C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the TAS5414B-Q1 or TAS5424B-Q1 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5414B-Q1 or TAS5424B-Q1 address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5414B-Q1 or TAS5424B-Q1 again responds with an acknowledge bit. Next, the TAS5414B-Q1 or TAS5424B-Q1 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

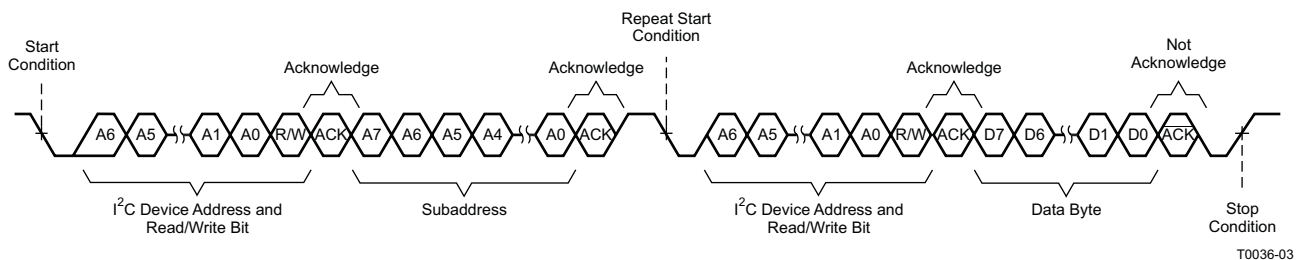


Figure 16. Random Read Transfer

## Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS5414B-Q1 or TAS5424B-Q1 to the master device as shown in Figure 17. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I<sup>2</sup>C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

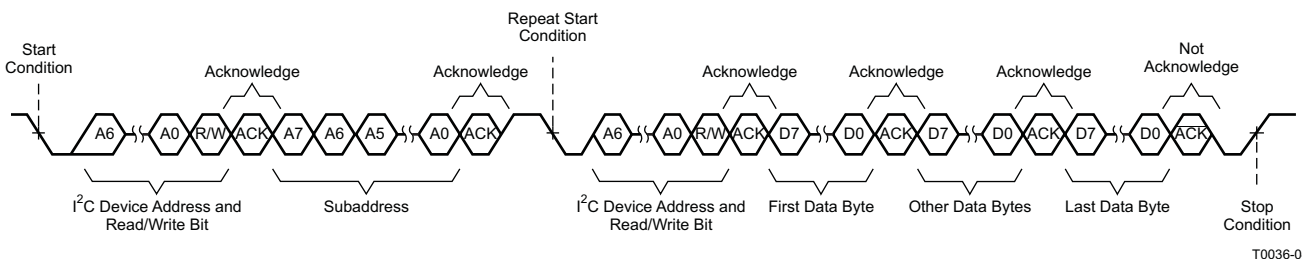


Figure 17. Sequential Read Transfer

**Table 3. TAS5414B-Q1/5424 I<sup>2</sup>C Addresses**

| DESCRIPTION                      |                        | FIXED ADDRESS |   |   |   |   | SELECTABLE WITH ADDRESS PIN |   | READ/WRITE BIT | I <sup>2</sup> C ADDRESS |
|----------------------------------|------------------------|---------------|---|---|---|---|-----------------------------|---|----------------|--------------------------|
|                                  |                        | MSB           | 6 | 5 | 4 | 3 | 2                           | 1 | LSB            |                          |
| TAS5414B-Q1/5424B 0 (OSC MASTER) | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 0                           | 0 | 0              | 0xD8                     |
|                                  | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 0                           | 0 | 1              | 0xD9                     |
| TAS5414B-Q1/5424B 1 (OSC SLAVE1) | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 0                           | 1 | 0              | 0xDA                     |
|                                  | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 0                           | 1 | 1              | 0xDB                     |
| TAS5414B-Q1/5424B 2 (OSC SLAVE2) | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 1                           | 0 | 0              | 0xDC                     |
|                                  | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 1                           | 0 | 1              | 0xDD                     |
| TAS5414B-Q1/5424B 3 (OSC SLAVE3) | I <sup>2</sup> C WRITE | 1             | 1 | 0 | 1 | 1 | 1                           | 1 | 0              | 0xDE                     |
|                                  | I <sup>2</sup> C READ  | 1             | 1 | 0 | 1 | 1 | 1                           | 1 | 1              | 0xDF                     |

**Table 4. I<sup>2</sup>C Address Register Definitions**

| ADDRESS    | R/W | REGISTER DESCRIPTION                                                       |
|------------|-----|----------------------------------------------------------------------------|
| 0x00       | R   | Latched fault register 1, global and channel fault                         |
| 0x01       | R   | Latched fault register 2, dc offset and overcurrent detect                 |
| 0x02       | R   | Latched diagnostic register 1, load diagnostics                            |
| 0x03       | R   | Latched diagnostic register 2, load diagnostics                            |
| 0x04       | R   | External status register 1, temperature and voltage detect                 |
| 0x05       | R   | External status register 2, Hi-Z and low-low state                         |
| 0x06       | R   | External status register 3, mute and play modes                            |
| 0x07       | R   | External status register 4, load diagnostics                               |
| 0x08       | R/W | External control register 1, channel gain select                           |
| 0x09       | R/W | External control register 2, over current control                          |
| 0x0A       | R/W | External control register 3, switching frequency and clip pin select       |
| 0x0B       | R/W | External control register 4, load diagnostic, master mode select           |
| 0x0C       | R/W | External control register 5, output state control                          |
| 0x0D       | R/W | External control register 6, output state control                          |
| 0x0E, 0x0F | -   | Not Used                                                                   |
| 0x10       | R/W | External control register 7, DC detect threshold selection                 |
| 0x13       | R   | External status register 5, over temperature shutdown and thermal foldback |

**Table 5. Fault Register 1 (0x00) Protection**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                         |
|----|----|----|----|----|----|----|----|--------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No protection-created faults, default value      |
| -  | -  | -  | -  | -  | -  | -  | 1  | Overtemperature warning has occurred             |
| -  | -  | -  | -  | -  | -  | 1  | -  | DC offset has occurred in any channel            |
| -  | -  | -  | -  | -  | 1  | -  | -  | Overcurrent shutdown has occurred in any channel |
| -  | -  | -  | -  | 1  | -  | -  | -  | Overtemperature shutdown has occurred            |
| -  | -  | -  | 1  | -  | -  | -  | -  | Charge pump undervoltage has occurred            |
| -  | -  | 1  | -  | -  | -  | -  | -  | AVDD, analog voltage, undervoltage has occurred  |
| -  | 1  | -  | -  | -  | -  | -  | -  | PVDD undervoltage has occurred                   |
| 1  | -  | -  | -  | -  | -  | -  | -  | PVDD overvoltage has occurred                    |

**Table 6. Fault Register 2 (0x01) Protection**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                    |
|----|----|----|----|----|----|----|----|---------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No protection-created faults, default value |
| -  | -  | -  | -  | -  | -  | -  | 1  | Overcurrent shutdown channel 1 has occurred |

**Table 6. Fault Register 2 (0x01) Protection (continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                    |
|----|----|----|----|----|----|----|----|---------------------------------------------|
| –  | –  | –  | –  | –  | –  | 1  | –  | Overcurrent shutdown channel 2 has occurred |
| –  | –  | –  | –  | –  | 1  | –  | –  | Overcurrent shutdown channel 3 has occurred |
| –  | –  | –  | –  | 1  | –  | –  | –  | Overcurrent shutdown channel 4 has occurred |
| –  | –  | –  | 1  | –  | –  | –  | –  | DC offset channel 1 has occurred            |
| –  | –  | 1  | –  | –  | –  | –  | –  | DC offset channel 2 has occurred            |
| –  | 1  | –  | –  | –  | –  | –  | –  | DC offset channel 3 has occurred            |
| 1  | –  | –  | –  | –  | –  | –  | –  | DC offset channel 4 has occurred            |

**Table 7. Diagnostic Register 1 (0x02) Load Diagnostics**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                         |
|----|----|----|----|----|----|----|----|--------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No load-diagnostic-created faults, default value |
| –  | –  | –  | –  | –  | –  | –  | 1  | Output short to ground channel 1 has occurred    |
| –  | –  | –  | –  | –  | –  | 1  | –  | Output short to PVDD channel 1 has occurred      |
| –  | –  | –  | –  | –  | 1  | –  | –  | Shorted load channel 1 has occurred              |
| –  | –  | –  | –  | 1  | –  | –  | –  | Open load channel 1 has occurred                 |
| –  | –  | –  | 1  | –  | –  | –  | –  | Output short to ground channel 2 has occurred    |
| –  | –  | 1  | –  | –  | –  | –  | –  | Output short to PVDD channel 2 has occurred      |
| –  | 1  | –  | –  | –  | –  | –  | –  | Shorted load channel 2 has occurred              |
| 1  | –  | –  | –  | –  | –  | –  | –  | Open load channel 2 has occurred                 |

**Table 8. Diagnostic Register 2 (0x03) Load Diagnostics**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                         |
|----|----|----|----|----|----|----|----|--------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No load-diagnostic-created faults, default value |
| –  | –  | –  | –  | –  | –  | –  | 1  | Output short to ground channel 3 has occurred    |
| –  | –  | –  | –  | –  | –  | 1  | –  | Output short to PVDD channel 3 has occurred      |
| –  | –  | –  | –  | –  | 1  | –  | –  | Shorted load channel 3 has occurred              |
| –  | –  | –  | –  | 1  | –  | –  | –  | Open load channel 3 has occurred                 |
| –  | –  | –  | 1  | –  | –  | –  | –  | Output short to ground channel 4 has occurred    |
| –  | –  | 1  | –  | –  | –  | –  | –  | Output short to PVDD channel 4 has occurred      |
| –  | 1  | –  | –  | –  | –  | –  | –  | Shorted load channel 4 has occurred              |
| 1  | –  | –  | –  | –  | –  | –  | –  | Open load channel 4 has occurred                 |

**Table 9. External Status Register 1 (0x04) Fault Detection**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                |
|----|----|----|----|----|----|----|----|---------------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No protection-created faults are present, default value |
| –  | –  | –  | –  | –  | –  | –  | 1  | PVDD overvoltage fault is present                       |
| –  | –  | –  | –  | –  | –  | 1  | –  | PVDD undervoltage fault is present                      |
| –  | –  | –  | –  | –  | 1  | –  | –  | AVDD, analog voltage fault is present                   |
| –  | –  | –  | –  | 1  | –  | –  | –  | Charge-pump voltage fault is present                    |
| –  | –  | –  | 1  | –  | –  | –  | –  | Overtemperature shutdown is present                     |
| –  | –  | 1  | –  | –  | –  | –  | –  | Overtemperature warning                                 |
| –  | 1  | 1  | –  | –  | –  | –  | –  | Overtemperature warning level 1                         |
| 1  | 0  | 1  | –  | –  | –  | –  | –  | Overtemperature warning level 2                         |
| 1  | 1  | 1  | –  | –  | –  | –  | –  | Overtemperature warning level 3                         |

**Table 10. External Status Register 2 (0x05) Output State of Individual Channels**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                                   |
|----|----|----|----|----|----|----|----|----------------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | Output is in Hi-Z mode, not in low-low mode <sup>(1)</sup> , default value |
| –  | –  | –  | –  | –  | –  | –  | 0  | Channel 1 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                               |
| –  | –  | –  | –  | –  | –  | 0  | –  | Channel 2 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                               |
| –  | –  | –  | –  | –  | 0  | –  | –  | Channel 3 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                               |
| –  | –  | –  | –  | 0  | –  | –  | –  | Channel 4 Hi-Z mode (0 = not Hi-Z, 1 = Hi-Z)                               |
| –  | –  | –  | 1  | –  | –  | –  | –  | Channel 1 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup>       |
| –  | –  | 1  | –  | –  | –  | –  | –  | Channel 2 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup>       |
| –  | 1  | –  | –  | –  | –  | –  | –  | Channel 3 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup>       |
| 1  | –  | –  | –  | –  | –  | –  | –  | Channel 4 low-low mode (0 = not low-low, 1 = low-low) <sup>(1)</sup>       |

(1) Low-low is defined as both outputs actively pulled to ground.

**Table 11. External Status Register 3 (0x06) Play and Mute Modes**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                              |
|----|----|----|----|----|----|----|----|-----------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | Mute mode is disabled, play mode disabled, default value, (Hi-Z mode) |
| –  | –  | –  | –  | –  | –  | –  | 1  | Channel 1 play mode is enabled                                        |
| –  | –  | –  | –  | –  | –  | 1  | –  | Channel 2 play mode is enabled                                        |
| –  | –  | –  | –  | –  | 1  | –  | –  | Channel 3 play mode is enabled                                        |
| –  | –  | –  | –  | 1  | –  | –  | –  | Channel 4 play mode is enabled                                        |
| –  | –  | –  | 1  | –  | –  | –  | –  | Channel 1 mute mode is enabled                                        |
| –  | –  | 1  | –  | –  | –  | –  | –  | Channel 2 mute mode is enabled                                        |
| –  | 1  | –  | –  | –  | –  | –  | –  | Channel 3 mute mode is enabled                                        |
| 1  | –  | –  | –  | –  | –  | –  | –  | Channel 4 mute mode is enabled                                        |

**Table 12. External Status Register 4 (0x07) Load Diagnostics**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                    |
|----|----|----|----|----|----|----|----|-------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | No channels are set in load diagnostics mode, default value |
| –  | –  | –  | –  | –  | –  | –  | 1  | Channel 1 is in load diagnostics mode                       |
| –  | –  | –  | –  | –  | –  | 1  | –  | Channel 2 is in load diagnostics mode                       |
| –  | –  | –  | –  | –  | 1  | –  | –  | Channel 3 is in load diagnostics mode                       |
| –  | –  | –  | –  | 1  | –  | –  | –  | Channel 4 is in load diagnostics mode                       |
| –  | –  | –  | 1  | –  | –  | –  | –  | Channel 1 is in Over Temperature Foldback                   |
| –  | –  | 1  | –  | –  | –  | –  | –  | Channel 2 is in Over Temperature Foldback                   |
| –  | 1  | –  | –  | –  | –  | –  | –  | Channel 3 is in Over Temperature Foldback                   |
| 1  | –  | –  | –  | –  | –  | –  | –  | Channel 4 is in Over Temperature Foldback                   |

**Table 13. External Control Register 1 (0x08) Gain Select**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                          |
|----|----|----|----|----|----|----|----|---------------------------------------------------|
| 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | Set gain for all channels to 26 dB, default value |
| –  | –  | –  | –  | –  | –  | 0  | 0  | Set channel 1 gain to 12 dB                       |
| –  | –  | –  | –  | –  | –  | 0  | 1  | Set channel 1 gain to 20 dB                       |
| –  | –  | –  | –  | –  | –  | 1  | 1  | Set channel 1 gain to 32 dB                       |
| –  | –  | –  | –  | 0  | 0  | –  | –  | Set channel 2 gain to 12 dB                       |
| –  | –  | –  | –  | 0  | 1  | –  | –  | Set channel 2 gain to 20 dB                       |
| –  | –  | –  | –  | 1  | 1  | –  | –  | Set channel 2 gain to 32 dB                       |
| –  | –  | 0  | 0  | –  | –  | –  | –  | Set channel 3 gain to 12 dB                       |
| –  | –  | 0  | 1  | –  | –  | –  | –  | Set channel 3 gain to 20 dB                       |
| –  | –  | 1  | 1  | –  | –  | –  | –  | Set channel 3 gain to 32 dB                       |

**Table 13. External Control Register 1 (0x08) Gain Select (continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                    |
|----|----|----|----|----|----|----|----|-----------------------------|
| 0  | 0  | –  | –  | –  | –  | –  | –  | Set channel 4 gain to 12 dB |
| 0  | 1  | –  | –  | –  | –  | –  | –  | Set channel 4 gain to 20 dB |
| 1  | 1  | –  | –  | –  | –  | –  | –  | Set channel 4 gain to 32 dB |

**Table 14. External Control Register 2(0x09) Over Current Control**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                     |
|----|----|----|----|----|----|----|----|--------------------------------------------------------------|
| 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | Current Limit Level 2 for all channels                       |
|    |    |    | 0  |    |    |    |    | Set Channel 1 Over Current Limit ( 0 - level 1, 1 - level 2) |
|    |    | 0  |    |    |    |    |    | Set Channel 2 Over Current Limit ( 0 - level 1, 1 - level 2) |
|    | 0  |    |    |    |    |    |    | Set Channel 3 Over Current Limit ( 0 - level 1, 1 - level 2) |
| 0  |    |    |    |    |    |    |    | Set Channel 4 Over Current Limit ( 0 - level 1, 1 - level 2) |
|    |    |    |    | X  | X  | X  | X  | Reserved                                                     |

**Table 15. External Control Register 3 (0x0A) Switching Frequency Select and Clip\_OTW Configuration**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                                           |
|----|----|----|----|----|----|----|----|------------------------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | Set $f_s = 417$ kHz, report clip and OTW, 45° phase, disable hard stop             |
| –  | –  | –  | –  | –  | –  | 0  | 0  | Set $f_s = 500$ kHz                                                                |
| –  | –  | –  | –  | –  | –  | 1  | 0  | Set $f_s = 357$ kHz                                                                |
| –  | –  | –  | –  | –  | –  | 1  | 1  | Invalid frequency selection (do not set)                                           |
| –  | –  | –  | –  | 0  | 0  | –  | –  | Configure $\overline{\text{CLIP\_OTW}}$ pin to report tweeter detect only          |
| –  | –  | –  | –  | 0  | 1  | –  | –  | Configure $\overline{\text{CLIP\_OTW}}$ pin to report clip detect only             |
| –  | –  | –  | –  | 1  | 0  | –  | –  | Configure $\overline{\text{CLIP\_OTW}}$ pin to report overtemperature warning only |
| –  | –  | –  | 1  | –  | –  | –  | –  | Enable hard-stop mode                                                              |
| –  | –  | 1  | –  | –  | –  | –  | –  | Set $f_s$ to a 180° phase difference between adjacent channels                     |
| –  | 1  | –  | –  | –  | –  | –  | –  | Send Sync Pulse from OSC_SYNC pin (Device must be in master mode)                  |
| X  | –  | –  | –  | –  | –  | –  | –  | Reserved                                                                           |

**Table 16. External Control Register 4 (0x0B) Load Diagnostics and Master/Slave Control**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                                                  |
|----|----|----|----|----|----|----|----|-------------------------------------------------------------------------------------------|
| 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | Clock output disabled, Master clock mode, DC Detection Enabled, Load diagnostics disabled |
| –  | –  | –  | –  | –  | –  | –  | 1  | Run channel 1 load diagnostics                                                            |
| –  | –  | –  | –  | –  | –  | 1  | –  | Run channel 2 load diagnostics                                                            |
| –  | –  | –  | –  | –  | 1  | –  | –  | Run channel 3 load diagnostics                                                            |
| –  | –  | –  | –  | 1  | –  | –  | –  | Run channel 4 load diagnostics                                                            |
| –  | –  | –  | 0  | –  | –  | –  | –  | Disable dc detection on all channels                                                      |
| –  | –  | 1  | –  | –  | –  | –  | –  | Enable tweeter-detect mode                                                                |
| –  | 0  | –  | –  | –  | –  | –  | –  | Enable slave mode (external oscillator must be provided)                                  |
| 1  | –  | –  | –  | –  | –  | –  | –  | Enable clock output on OSC_SYNC pin (valid only in master mode)                           |

**Table 17. External Control Register 5 (0x0C) Output Control**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                 |
|----|----|----|----|----|----|----|----|------------------------------------------|
| 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | All channels, Hi-Z, mute, reset disabled |
| –  | –  | –  | –  | –  | –  | –  | 0  | Set channel 1 to mute mode, non-Hi-Z     |
| –  | –  | –  | –  | –  | –  | 0  | –  | Set channel 2 to mute mode, non-Hi-Z     |
| –  | –  | –  | –  | –  | 0  | –  | –  | Set channel 3 to mute mode, non-Hi-Z     |
| –  | –  | –  | –  | 0  | –  | –  | –  | Set channel 4 to mute mode, non-Hi-Z     |

**Table 17. External Control Register 5 (0x0C) Output Control (continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                     |
|----|----|----|----|----|----|----|----|----------------------------------------------|
| –  | –  | –  | 0  | –  | –  | –  | –  | Set non-Hi-Z channels to play mode, (unmute) |
| –  | 1  | 1  | –  | –  | –  | –  | –  | Reserved                                     |
| 1  | –  | –  | –  | –  | –  | –  | –  | Reset device                                 |

**Table 18. External Control Register 6 (0x0D) Output Control**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                            |
|----|----|----|----|----|----|----|----|-------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | Low-low state disabled all channels |
| –  | –  | –  | –  | –  | –  | –  | 1  | Set channel 1 to low-low state      |
| –  | –  | –  | –  | –  | –  | 1  | –  | Set channel 2 to low-low state      |
| –  | –  | –  | –  | –  | 1  | –  | –  | Set channel 3 to low-low state      |
| –  | –  | –  | –  | 1  | –  | –  | –  | Set channel 4 to low-low state      |
| X  | X  | X  | X  | –  | –  | –  | –  | Reserved                            |

**Table 19. External Control Register 7 (0x10) Miscellaneous Selection**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                                                                                                   |
|----|----|----|----|----|----|----|----|--------------------------------------------------------------------------------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | Normal speed CM ramp, normal S2P & S2G timing, no delay between LDG phases, Crosstalk Enhancement Disabled, Default DC detect value (1.6V) |
| –  | –  | –  | –  | –  | –  | 0  | 0  | Minimum DC detect value (0.8V)                                                                                                             |
| –  | –  | –  | –  | –  | –  | 1  | 0  | Maximum DC detect value (2.4V)                                                                                                             |
| –  | –  | –  | –  | –  | 1  | –  | –  | Enable Crosstalk Enhancement                                                                                                               |
| –  | –  | –  | –  | 1  | –  | –  | –  | Adds a 20mS delay between load diagnostic phases                                                                                           |
| –  | –  | –  | 1  | –  | –  | –  | –  | Short-to-Power (S2P) and Short-to-Ground (S2G) Load Diagnostic phases take 4x longer                                                       |
| 1  | –  | –  | –  | –  | –  | –  | –  | Slower common mode (CM) ramp down from Mute mode                                                                                           |
|    | X  | X  |    |    |    |    |    | Reserved                                                                                                                                   |

**Table 20. External Status Register 5 (0x13) Over Temperature and Thermal Foldback Status**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION                                                            |
|----|----|----|----|----|----|----|----|---------------------------------------------------------------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | Default Over temperature foldback status, no channel is in foldback |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | Channel 1 in thermal foldback                                       |
| 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | Channel 2 in thermal foldback                                       |
| 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | Channel 3 in thermal foldback                                       |
| 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | Channel 4 in thermal foldback                                       |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | Channel 1 in Over temperature shutdown                              |
| 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | Channel 2 in Over temperature shutdown                              |
| 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | Channel 3 in Over temperature shutdown                              |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | Channel 4 in Over temperature shutdown                              |

## Hardware Control Pins

There are four discrete hardware pins for real-time control and indication of device status.

**FAULT** pin: This active-low open-drain output pin indicates the presence of a fault condition that requires the device to go into the Hi-Z mode or standby mode. When this pin is asserted, the device has protected itself and the system from potential damage. The exact nature of the fault can be read via I<sup>2</sup>C with the exception of PVDD under-voltage faults below POR in which case the I<sup>2</sup>C bus is no longer operational. However, the fault is still indicated due to the fact that the **FAULT** pin is asserted.

**CLIP\_OTW** pin: This active-low open-drain pin is configured via I<sup>2</sup>C to indicate one of the following conditions: overtemperature warning, the detection of clipping, or the logical OR of both of these conditions. During tweeter detect diagnostics, this pin also is asserted when a tweeter is present.

**MUTE** pin: This active-low pin is used for hardware control of the mute/unmute function for all four channels. Capacitor C<sub>MUTE</sub> is used to control the time constant for the gain ramp needed to produce a pop- and click-free mute function. For pop- and click-free operation, the mute function should be implemented through I<sup>2</sup>C commands. The use of a hard mute with an external transistor does not ensure pop- and click-free operation, and is not recommended unless an *emergency hard mute* function is required in case of a loss of I<sup>2</sup>C control. The C<sub>MUTE</sub> capacitor may not be shared between multiple devices.

**STANDBY** pin: When this active-low pin is asserted, the device goes into a complete shutdown, and current draw is limited to 2 µA, typical. It can be used to shut down the device rapidly. If all channels are in Hi-Z the device will enter standby in ~1mS and if not a quick ramp down will occur that takes ~20mS. The outputs are ramped down quickly if not already in Hi-Z so externally biasing the **MUTE** pin will prevent the device from entering standby. All I<sup>2</sup>C register content is lost when this pin is asserted. The I<sup>2</sup>C bus goes into the high-impedance state when the **STANDBY** pin is asserted.

## EMI Considerations

Automotive level EMI performance depends on both careful integrated circuit design and good system level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

The design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The phase between channels is I<sup>2</sup>C selectable to either 45° or 180°, to reduce EMI caused by high-current switching. The design also incorporates circuitry that optimizes output transitions that cause EMI.

## AM Radio Avoidance

To reduce interference in the AM radio band, the device has the ability to change the switching frequency via I<sup>2</sup>C commands. The recommended frequencies are listed in [Table 21](#). The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio.

**Table 21. Recommended Switching Frequencies for AM Mode Operation**

| US                 |                           | EUROPEAN           |                           |
|--------------------|---------------------------|--------------------|---------------------------|
| AM FREQUENCY (kHz) | SWITCHING FREQUENCY (kHz) | AM FREQUENCY (kHz) | SWITCHING FREQUENCY (kHz) |
| 540 - 670          | 417                       | 522 - 675          | 417                       |
| 680 - 980          | 500                       | 676 - 945          | 500                       |
| 990 - 1180         | 417                       | 946 - 1188         | 417                       |
| 1190 - 1420        | 500                       | 1189 - 1422        | 500                       |
| 1430 - 1580        | 417                       | 1423 - 1584        | 417                       |
| 1590 - 1700        | 500                       | 1585 - 1701        | 500                       |

## Operating Modes and Faults

The operating modes and faults are depicted in the following tables.

**Table 22. Operating Modes**

| STATE NAME | OUTPUT FETS         | CHARGE PUMP | OSCILLATOR | I <sup>2</sup> C | AVDD and DVDD |
|------------|---------------------|-------------|------------|------------------|---------------|
| STANDBY    | Hi-Z, floating      | Stopped     | Stopped    | Stopped          | OFF           |
| Hi-Z       | Hi-Z, weak pulldown | Active      | Active     | Active           | ON            |
| Mute       | Switching at 50%    | Active      | Active     | Active           | ON            |

**Table 22. Operating Modes (continued)**

| STATE NAME       | OUTPUT FETS          | CHARGE PUMP | OSCILLATOR | I <sup>2</sup> C | AVDD and DVDD |
|------------------|----------------------|-------------|------------|------------------|---------------|
| Normal operation | Switching with audio | Active      | Active     | Active           | ON            |

**Table 23. Global Faults and Actions**

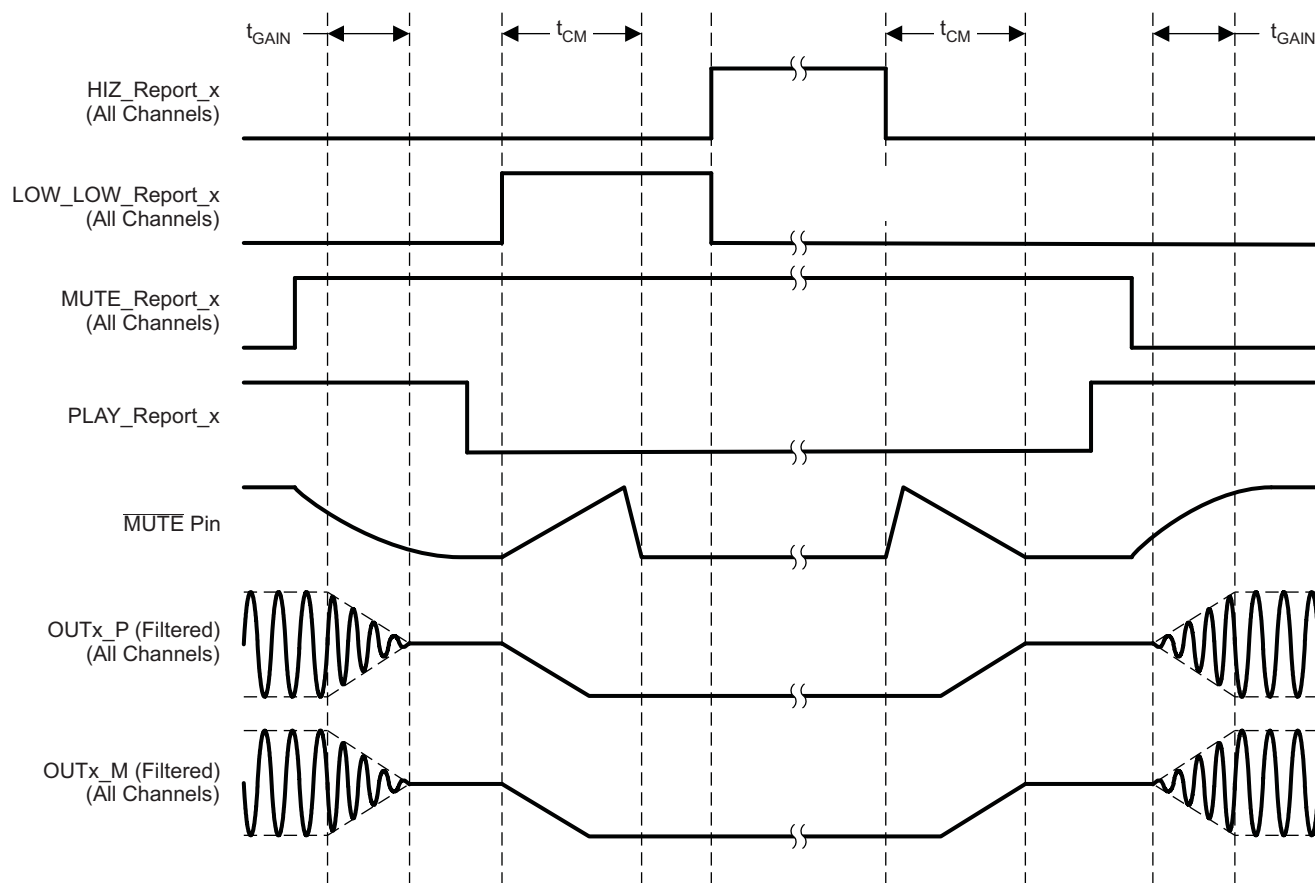
| FAULT/<br>EVENT | FAULT/EVENT<br>CATEGORY | MONITORING<br>MODES | REPORTING<br>METHOD                                    | ACTION<br>TYPE      | ACTION<br>RESULT | LATCHED/<br>SELF-<br>CLEARING |
|-----------------|-------------------------|---------------------|--------------------------------------------------------|---------------------|------------------|-------------------------------|
| POR             | Voltage fault           | All                 | $\overline{\text{FAULT}}$ pin                          | Hard mute (no ramp) | Standby          | Self-clearing                 |
| UV              |                         | Hi-Z, mute, normal  | $\text{I}^2\text{C} + \overline{\text{FAULT}}$ pin     |                     | Hi-Z             | Latched                       |
| CP UV           |                         |                     |                                                        |                     |                  |                               |
| OV              |                         | All                 | $\overline{\text{FAULT}}$ pin                          |                     | Standby          | Self-clearing                 |
| Load dump       |                         |                     |                                                        |                     |                  |                               |
| OTW             | Thermal warning         | Hi-Z, mute, normal  | $\text{I}^2\text{C} + \overline{\text{CLIP\_OTW}}$ pin | None                | None             | Self-clearing                 |
| OTSD            | Thermal fault           | Hi-Z, mute, normal  | $\text{I}^2\text{C} + \overline{\text{FAULT}}$ pin     | Hard mute (no ramp) | Standby          | Latched                       |

**Table 24. Channel Faults and Actions**

| FAULT/<br>EVENT           | FAULT/EVENT<br>CATEGORY | MONITORING<br>MODES               | REPORTING<br>METHOD                                     | ACTION<br>TYPE | ACTION<br>RESULT  | LATCHED/<br>SELF-<br>CLEARING |
|---------------------------|-------------------------|-----------------------------------|---------------------------------------------------------|----------------|-------------------|-------------------------------|
| Open/short<br>diagnostic  | Diagnostic              | Hi-Z (I <sup>2</sup> C activated) | I <sup>2</sup> C                                        | None           | None              | Latched                       |
| Clipping                  | Warning                 | Mute / Play                       | $\overline{\text{CLIP\_OTW}}$ pin                       | None           | None              | Self-clearing                 |
| CBC load current<br>limit | Online protection       |                                   |                                                         | Current Limit  | Start OC<br>timer | Self-clearing                 |
| OC fault                  | Output channel fault    |                                   | I <sup>2</sup> C + $\overline{\text{FAULT}}$ pin        | Hard mute      | Hi-Z              | Latched                       |
| DC detect                 |                         |                                   |                                                         | Hard mute      | Hi-Z              | Latched                       |
| OT Foldback               | Warning                 |                                   | I <sup>2</sup> C + $\overline{\text{CLIP\_OTW}}$<br>pin | Reduce Gain    | None              | Self-clearing                 |

## Audio Shutdown and Restart Sequence

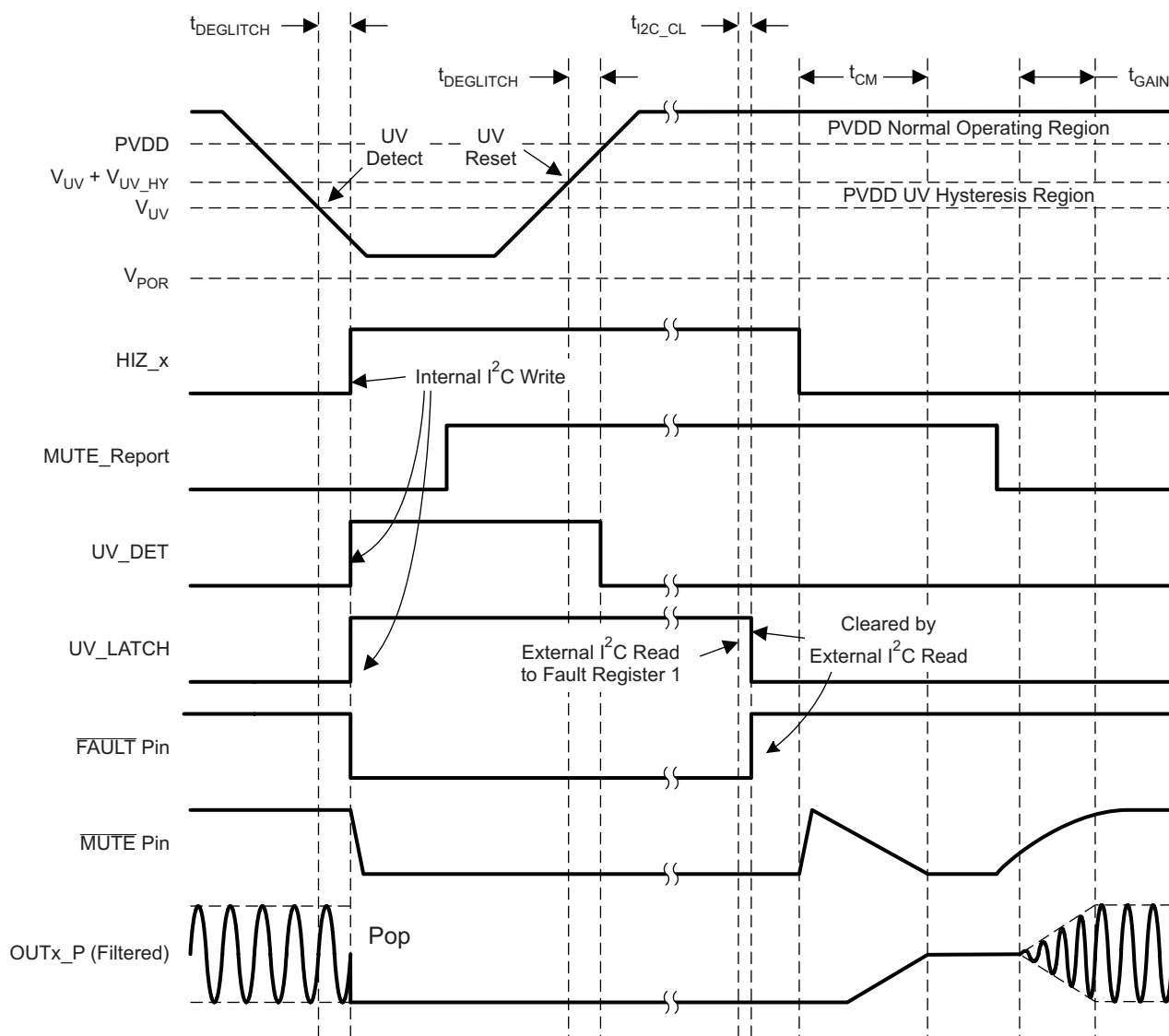
The gain ramp of the filtered output signal and the updating of the I<sup>2</sup>C registers correspond to the MUTE pin voltage during the ramping process. The length of time that the MUTE pin takes to complete its ramp is dictated by the value of the external capacitor on the MUTE pin. With the default 220nF capacitor the turn-on common mode ramp takes ~26mS and the gain ramp takes ~76mS.



T0192-02

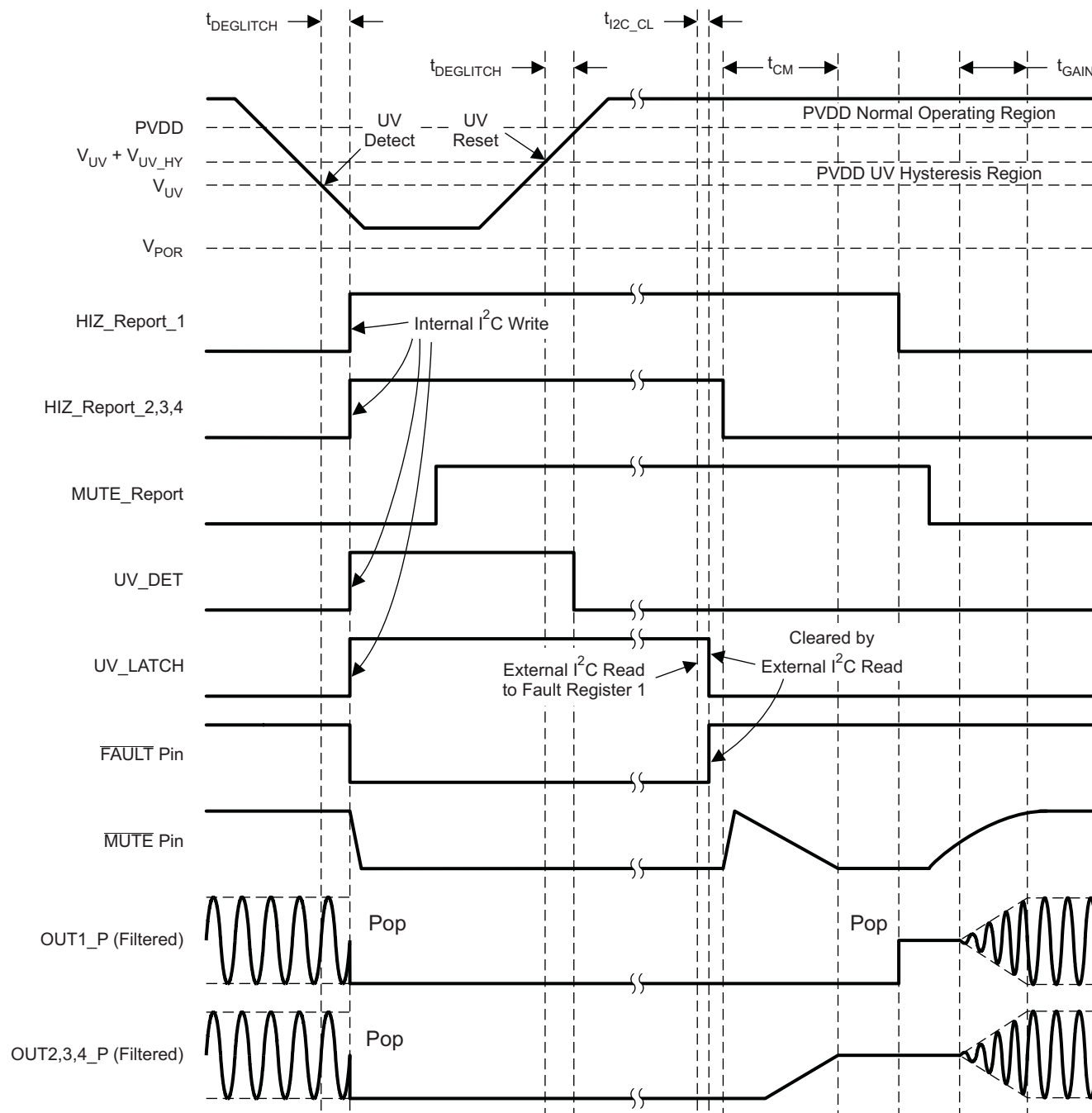
**Figure 18. Click- and Pop-Free Shutdown and Restart Sequence Timing Diagram**

## Latched Fault Shutdown and Restart Sequence Control



T0194-02

**Figure 19. Latched Global Fault Shutdown and Restart Timing Diagram  
(UV Shutdown and Recovery)**



T0195-02

Figure 20. Latched Global Fault Shutdown and Individual Channel Restart Timing Diagram (UV Shutdown and Recovery)

## APPLICATION INFORMATION

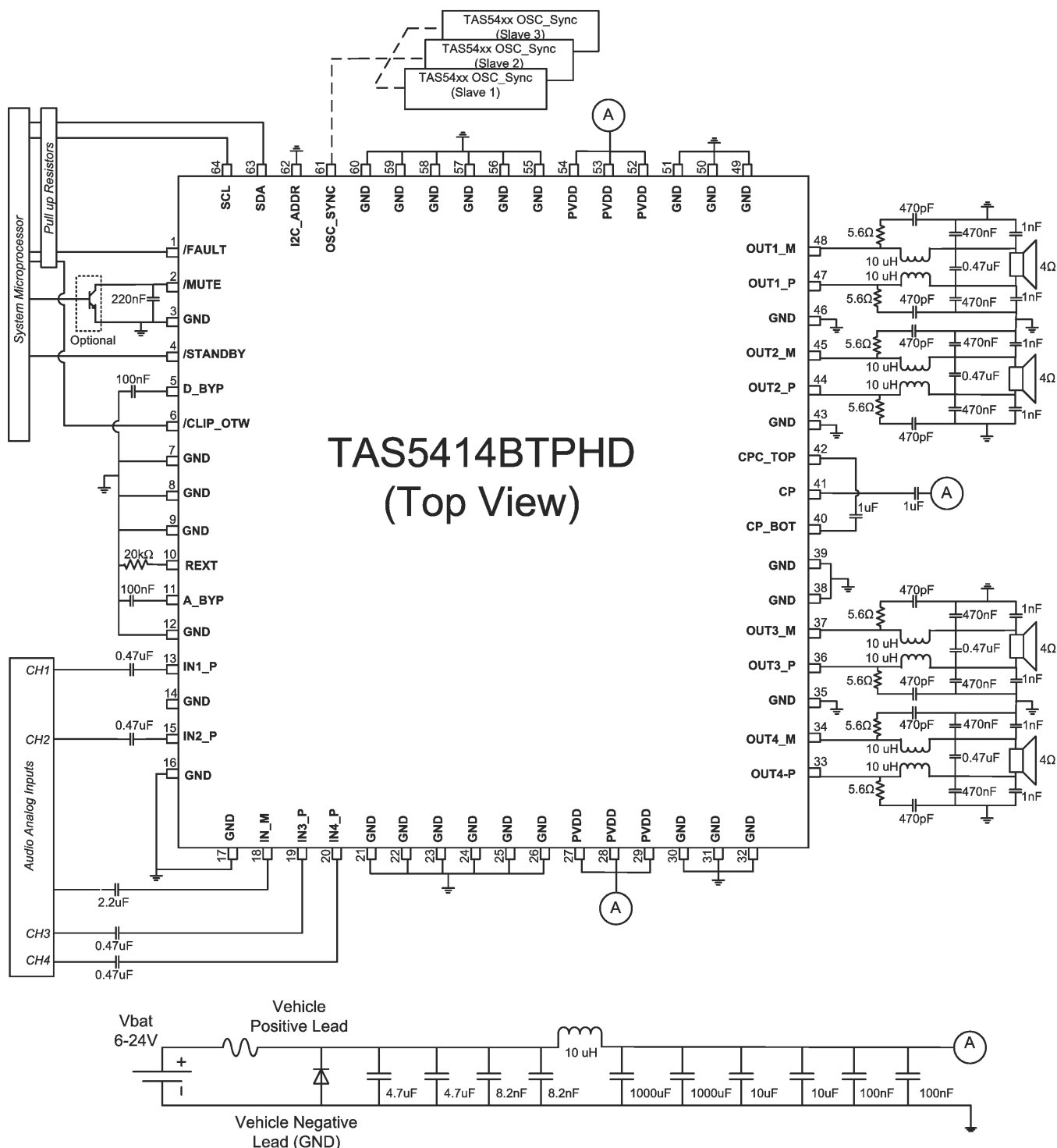


Figure 21. TAS5414B-Q1 Typical Application Schematic

### Parallel Operation (PBTL)

The device can drive more current paralleling BTL channels on the load side of the LC output filter. For parallel operation, identical I<sup>2</sup>C settings are required for any two paralleled channels in order to have reliable system

performance and even power dissipation on multiple channels. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, etc.) should be sent to the paralleled channels at the same time. Load diagnostic is also supported for parallel connection. Paralleling on the device side of the LC output filter is not supported, and can result in device failure. When paralleling channels it is important to monitor channels for thermal foldback and lower the system gain for paralleled channels.

## Input Filter Design

For the TAS5424B-Q1 device, the input filter for a single channel's P and M inputs should be identical. For the TAS5414B-Q1 the IN\_M pin should have an impedance to GND that is equivalent to the parallel combination of the input impedances of all IN\_P channels combined, including any source impedance from the previous stage in the system design. For example, if each of the 4 IN\_P channels have a 1 $\mu$ F DC blocking capacitor, 1k $\Omega$  of series resistance due to an input RC filter, and 1k $\Omega$  of source resistance from the DAC supplying the audio signal, then the IN\_M channel should have a 4 $\mu$ F capacitor in series with a 500 $\Omega$  resistor to GND (4 x 1 $\mu$ F in parallel = 4 $\mu$ F; 4 x 2k $\Omega$  in parallel = 500 $\Omega$ ).

## Demodulation Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal. The main purpose of the demodulation filter is to attenuate the high-frequency components of the output signals that are out of the audio band. Design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N needs, the selection of the inductors used in the output filter should be carefully considered. The rule is that the inductance should stay above 10% of the inductance value within the range of peak current seen at maximum output power in the system design.

## Line Driver Applications

In many automotive audio applications the end user would like to use the same head unit to drive either a speaker (with several Ohms of impedance) or an external amplifier (with several kOhms of impedance). The design is capable of supporting both applications; however, the output filter and system must be designed to handle the expected output load conditions.

## Thermal Information

The thermally augmented package is designed to interface directly to heat sinks using a thermal interface compound (for example, Artic Silver, Ceramique thermal compound.) The heat sink then absorbs heat from the ICs and couples it to the local air. If louvers or fans are supplied, this process can reach equilibrium and heat can be continually removed from the ICs. Because of the device efficiency heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

R $_{\theta JA}$  is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- R $_{\theta JC}$  (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in  $^{\circ}\text{C-in}^2/\text{W}$  or  $^{\circ}\text{C-mm}^2/\text{W}$ ). The area thermal resistance of the example thermal grease with a 0.001-inch (0.0254-mm) thick layer is about 0.007 $^{\circ}\text{C-in}^2/\text{W}$  (4.52 $^{\circ}\text{C-mm}^2/\text{W}$ ). The approximate exposed heat slug size is as follows:

|                 |                                             |
|-----------------|---------------------------------------------|
| 36/44-pin PSOP3 | 0.124 in <sup>2</sup> (80 mm <sup>2</sup> ) |
| 64-pin QFP      | 0.099 in <sup>2</sup> (64 mm <sup>2</sup> ) |

Dividing the example thermal grease area resistance by the area of the heat slug gives the actual resistance through the thermal grease for both parts:

|                 |          |
|-----------------|----------|
| 36/44-pin PSOP3 | 0.06°C/W |
| 64-pin QFP      | 0.07°C/W |

The thermal resistance of thermal pads is generally considerably higher than a thin thermal grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance generally is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus, for a single monaural channel in the IC, the system  $R_{\theta JA} = R_{\theta JC} + \text{thermal grease resistance} + \text{heat sink resistance}$ .

The following table indicates modeled parameters for one device on a heat sink. The junction temperature is set at 115°C while delivering 20 W<sub>rms</sub> per channel into 4-Ω loads with no clipping. It is assumed that the thermal grease is about 0.001 inches (0.0254 mm) thick.

| Device                                          | 36-Pin PSOP3 |
|-------------------------------------------------|--------------|
| Ambient temperature                             | 25°C         |
| Power to load                                   | 20 W × 4     |
| Power dissipation                               | 1.90 W × 4   |
| ΔT inside package                               | 7.6°C        |
| ΔT through thermal grease                       | 0.46°C       |
| Required heatsink thermal resistance            | 10.78°C/W    |
| Junction temperature                            | 115°C        |
| System $R_{\theta JA}$                          | 11.85°C/W    |
| $R_{\theta JA} \times \text{power dissipation}$ | 90°C         |

### Electrical Connection of Heat Slug and Heat Sink

The heat sink connected to the heat slug of the device should be connected to GND or left floating. The heat slug should not be connected to any other electrical node.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier  | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|------------------|------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TAS5414BTDKDRQ1</a> | Obsolete      | Production           | HSSOP (DKD)   36 | -                      | -           | Call TI                              | Call TI                           | -40 to 105   | TAS5414BQ1          |
| <a href="#">TAS5414BTPHDQ1</a>  | Active        | Production           | HTQFP (PHD)   64 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414BTQ1         |
| TAS5414BTPHDQ1.A                | Active        | Production           | HTQFP (PHD)   64 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414BTQ1         |
| TAS5414BTPHDQ1.B                | Active        | Production           | HTQFP (PHD)   64 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414BTQ1         |
| <a href="#">TAS5414BTPHDRQ1</a> | Active        | Production           | HTQFP (PHD)   64 | 1000   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414BTQ1         |
| TAS5414BTPHDRQ1.A               | Active        | Production           | HTQFP (PHD)   64 | 1000   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414BTQ1         |
| TAS5414BTPHDRQ1.B               | Active        | Production           | HTQFP (PHD)   64 | 1000   SMALL T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | TAS5414BTQ1         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

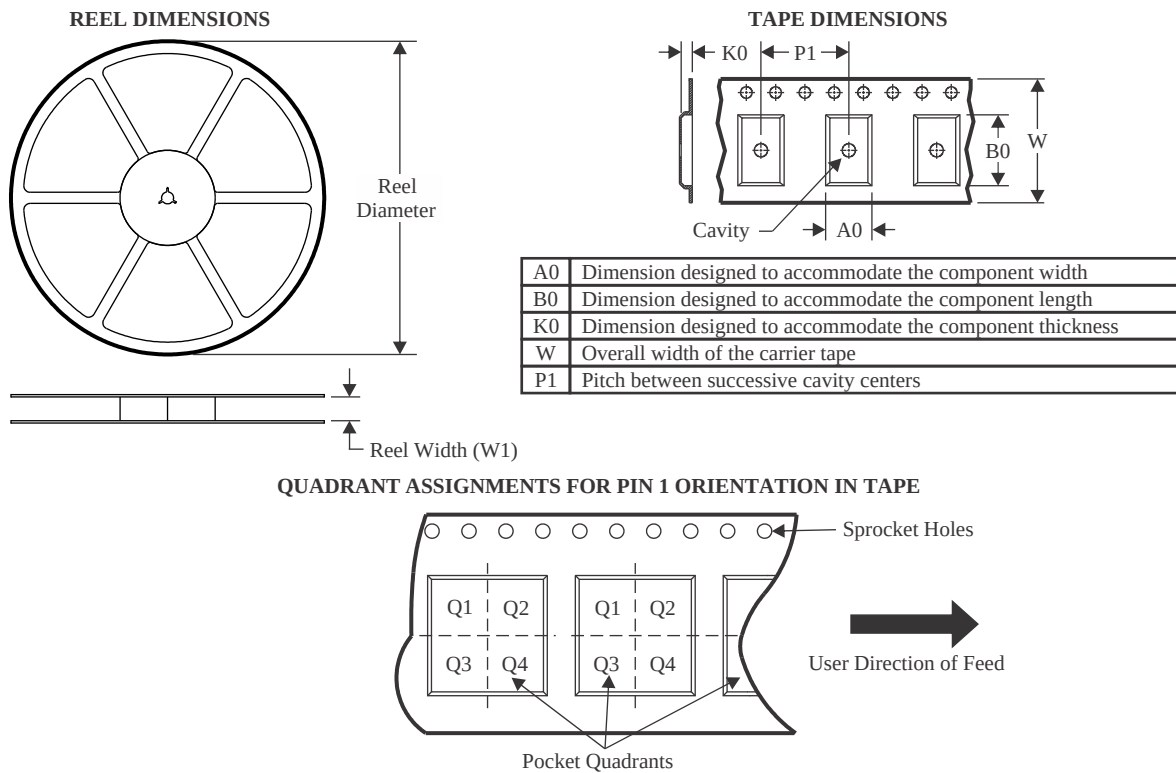
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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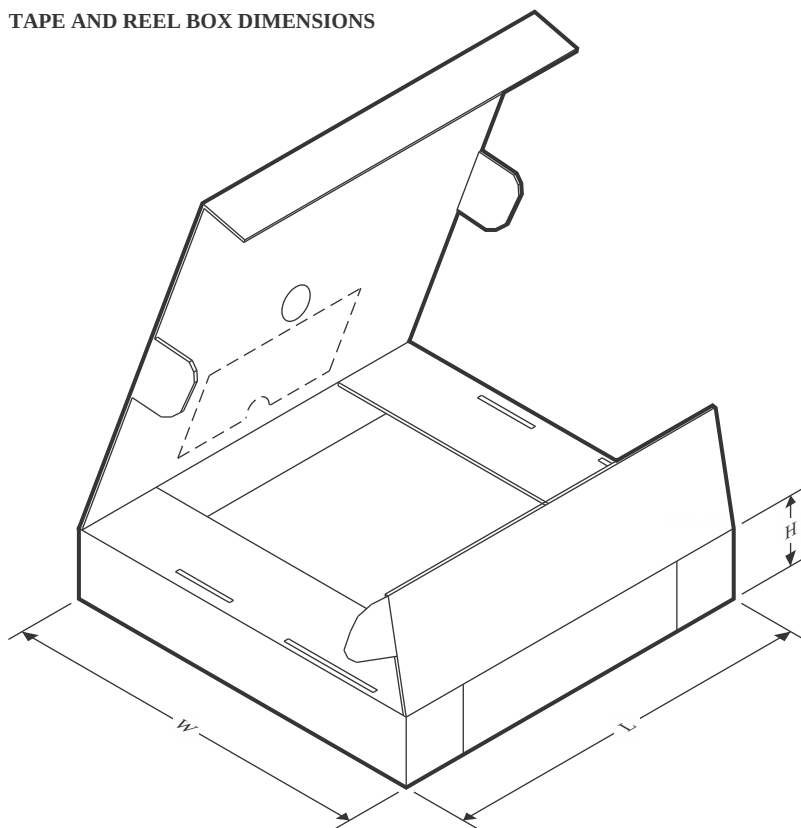
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS5414BTPHDRQ1 | HTQFP        | PHD             | 64   | 1000 | 330.0              | 24.4               | 17.0    | 17.0    | 1.5     | 20.0    | 24.0   | Q2            |

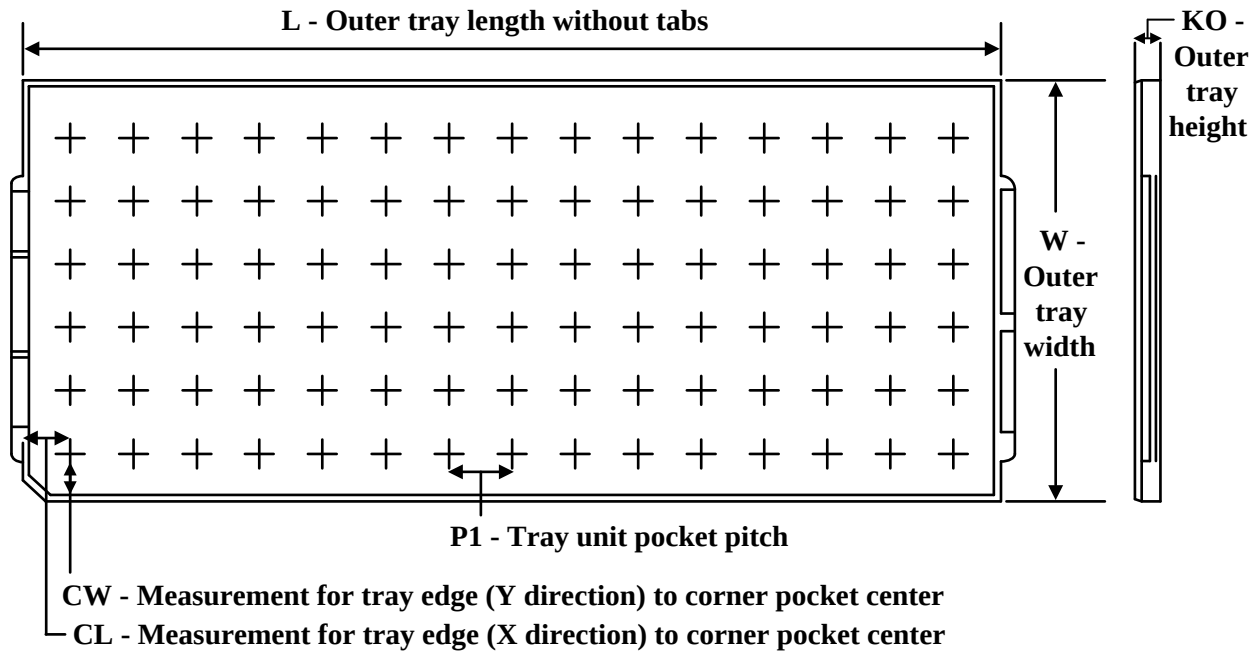
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS5414BTPHDRQ1 | HTQFP        | PHD             | 64   | 1000 | 350.0       | 350.0      | 43.0        |

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| TAS5414BTPHDQ1   | PHD          | HTQFP        | 64   | 90  | 6 X 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |
| TAS5414BTPHDQ1.A | PHD          | HTQFP        | 64   | 90  | 6 X 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |
| TAS5414BTPHDQ1.B | PHD          | HTQFP        | 64   | 90  | 6 X 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |

## GENERIC PACKAGE VIEW

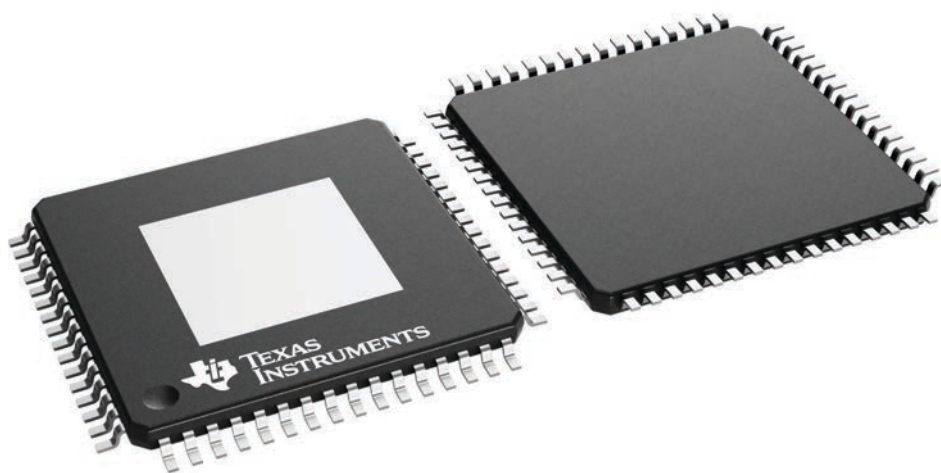
**PHD 64**

**HTQFP - 1.2 mm max height**

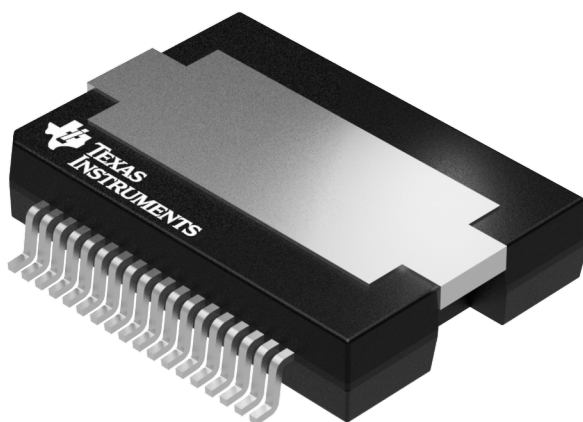
14 x 14, 0.8 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224851/B



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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