# ADS9226 16-Bit, Dual, Low-Latency, Simultaneous-Sampling SAR ADC

## 1 Features

- High resolution, high throughput:
  - 16 bits, 2.048 MSPS
- Fast response time with low latency: 488 ns
- Two simultaneously sampled channels
- Unipolar, pseudo-differential inputs
- Excellent DC and AC performance:
  - 16-bits, no missing codes
  - ±2.75-LSB max INL
  - 90.8-dB SNR, –100-dB THD
- Wide analog supply range from 4 V to 5.5 V
- Integrated reference buffers
- SPI-compatible serial interface
- Extended temperature range: –40°C to +125°C
- Small footprint: 5-mm × 5-mm VQFN

## 2 Applications

- Servo drive position feedback
- Servo drive power-stage modules
- Telecom optical modules
- Power quality analyzers
- DC/AC power supplies, electronic loads

## 3 Description

The ADS9226 is a 16-bit, dual-channel, simultaneous-sampling, analog-to-digital converter (ADC) with an integrated reference buffer. The device can operate on a single 5-V supply and supports unipolar, pseudo-differential analog input signals with excellent DC and AC specifications.

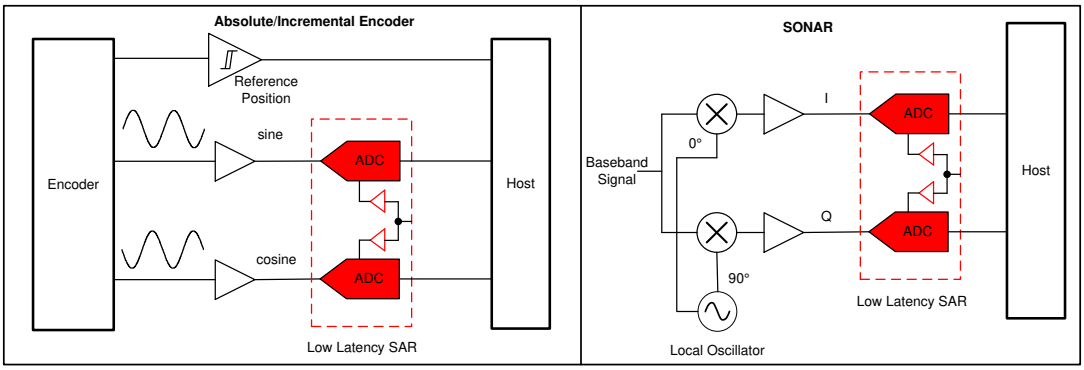
The device supports an SPI-compatible serial (enhanced-SPI) interface, making the device easy to pair with a diversity of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs).

The device comes in a space-saving, 5-mm × 5-mm, VQFN package. The ADS9226 is specified for the extended temperature range of –40°C to +125°C.

**Device Information** (1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ADS9226 | VQFN (32) | 5.00 mm × 5.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.




**Typical Application Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

**1 Features**.....1
**2 Applications**.....1
**3 Description**.....1
**4 Revision History**.....2
**5 Pin Configuration and Functions**.....3
Pin Functions.....3
**6 Specifications**.....5
6.1 Absolute Maximum Ratings.....5
6.2 ESD Ratings.....5
6.3 Recommended Operating Conditions.....5
6.4 Thermal Information.....6
6.5 Electrical Characteristics.....6
6.6 Timing Requirements.....8
6.7 Switching Characteristics.....8
6.8 Timing Diagrams.....9
6.9 Typical Characteristics.....11
**7 Detailed Description**.....15
7.1 Overview.....15
7.2 Functional Block Diagram.....15
7.3 Feature Description.....16
7.4 Device Functional Modes.....20
**8 Application and Implementation**.....22
8.1 Application Information.....22
8.2 Typical Application.....24
**9 Power Supply Recommendations**.....26
**10 Layout**.....27
10.1 Layout Guidelines.....27
10.2 Layout Example.....28
**11 Device and Documentation Support**.....29
11.1 Related Documentation.....29
11.2 Receiving Notification of Documentation Updates.....29
11.3 Support Resources.....29
11.4 Trademarks.....29
11.5 Electrostatic Discharge Caution.....29
11.6 Glossary.....29
**12 Mechanical, Packaging, and Orderable Information**.....29

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| July 2020 | * | Initial release. |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## 5 Pin Configuration and Functions

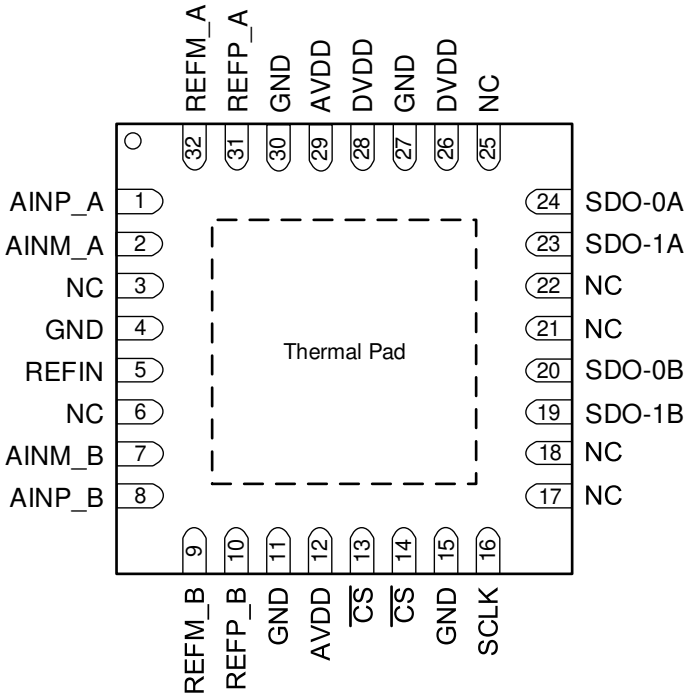


**Figure 5-1. RHB Package, 5-mm × 5-mm, 32-Pin VQFN, Top View**

### Pin Functions

| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AINM_A | 2 | Analog input | Negative analog input for channel A. |
| AINM_B | 7 | Analog input | Negative analog input for channel B. |
| AINP_A | 1 | Analog input | Positive analog input for channel A. |
| AINP_B | 8 | Analog input | Positive analog input for channel B. |
| AVDD | 12, 29 | Power supply | Analog power-supply pin. Short pins 12 and 29 together.<br>Place a 1-µF decoupling capacitor between pins 11 and 12.<br>Place a 1-µF decoupling capacitor between pins 29 and 30. |
| $\overline{CS}$ | 13, 14 | Digital input | Chip-select input pin; active low.<br>The device takes control of the data bus when $\overline{CS}$ is low.<br>The SDO-xy pins go to Hi-Z when $\overline{CS}$ is high.<br>Connect these pins together externally with a short trace. |
| DVDD | 26, 28 | Power supply | Interface power-supply pin.<br>Place a 1-µF decoupling capacitor between pins 27 and 26 and pins 27 and 28. |
| GND | 4, 11, 15, 27, 30 | Power supply | Device ground. |
| NC | 3, 6, 17, 18, 21, 22, 25 | No connection | No external connection. |

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| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| REFIN | 5 | Analog input | Reference voltage for the ADC. |
| REFM_A | 32 | Analog input | ADC_A negative reference input.<br>Externally connect to the device GND. |
| REFM_B | 9 | Analog input | ADC_B negative reference input.<br>Externally connect to the device GND. |
| REFP_A | 31 | Analog output | Positive output of reference buffer A. ADC_A positive reference input.<br>Place a 10-µF decoupling capacitor between pins 31 and 32. |
| REFP_B | 10 | Analog output | Positive output of reference buffer B. ADC_B positive reference input.<br>Place a 10-µF decoupling capacitor between pins 9 and 10. |
| SCLK | 16 | Digital input | Clock input pin for the serial interface. |
| SDO-0A | 24 | Digital output | Data output 0 for channel A. |
| SDO-0B | 20 | Digital output | Data output 0 for channel B. |
| SDO-1A | 23 | Digital output | Data output 1 for channel A. |
| SDO-1B | 19 | Digital output | Data output 1 for channel B. |
| Thermal pad | | Supply | Exposed thermal pad. TI recommends connecting this pin to the printed circuit board (PCB) ground. |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| AVDD to GND | | –0.3 | 6 | V |
| DVDD to GND | | –0.3 | 6 | V |
| Digital input pins | | GND – 0.3 | DVDD + 0.3 | V |
| Digital output pins | | GND – 0.3 | DVDD + 0.3 | V |
| AINP_A, AINP_B to GND, AINM_A, AINM_B to GND | | –0.3 | AVDD + 0.3 | V |
| REFM_A, REFM_B | | GND – 0.1 | GND + 0.1 | V |
| REFP_A, REFP_B to GND | | GND – 0.3 | AVDD + 0.3 | V |
| Reference input voltage | REFIN to GND | –0.3 | AVDD + 0.3 | V |
| Input or output current to any pin except power-supply pin | | –10 | 10 | mA |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| AVDD | | | 4 | 5 | 5.5 | V |
| DVDD | | Operating | 1.65 | 3 | 5.5 | V |
| | | SCLK > 20 MHz | 2.35 | 3 | 5.5 | |
| **EXTERNAL REFERENCE INPUT** | | | | | | |
| $V_{REFIN}$ | External reference input voltage | | 1.4 | AVDD/2 | AVDD/1.75 – 0.2 | V |
| **ANALOG INPUTS** | | | | | | |
| FSR | Full-scale input range | | $–V_{REFIN}$ | | $V_{REFIN}$ | V |
| $V_{INP_x}$ | Absolute input voltage AINP_x[1] | | –0.1 | | AVDD + 0.1 | V |
| $V_{INM_x}$ | Absolute input voltage AINM_x[2] | | $V_{REFIN}$ – 0.1 | $V_{REFIN}$ | $V_{REFIN}$ + 0.1 | V |
| **TEMPERATURE RANGE** | | | | | | |
| $T_A$ | Ambient temperature | | –40 | 25 | 125 | °C |

(1) AINP_x refers to AINP_A and AINP_B positive input pins for ADC_A and ADC_B respectively.
(2) AINM_x refers to AINM_A and AINM_B positive input pins for ADC_A and ADC_B respectively.

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## 6.4 Thermal Information

| THERMAL METRIC[1] | | ADS9226 RHB (VQFN) 32 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 29 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 17.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 9.4 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 9.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

at AVDD = 4 V to 5.5 V, DVDD = 3.3 V, $V_{REFIN}$ = AVDD / 2 and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A$ = –40°C to +125°C; typical values at $T_A$ = 25°C and AVDD = 5 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT** | | | | | | |
| $I_{IN}$ | Analog input leakage current | | | ±1 | | µA |
| $C_i$ | Input capacitance | Sample mode | | 16 | | pF |
| | | Hold mode | | 1 | | |
| BW | Analog input bandwidth | –3-dB input signal | | 52 | | MHz |
| | | –0.1-dB input signal | | 4.2 | | |
| **DC ACCURACY** | | | | | | |
| | Resolution | No missing codes | 16 | | | bit |
| DNL | Differential nonlinearity | | –0.55 | ±0.25 | 0.55 | LSB |
| INL | Integral nonlinearity | | –2.75 | ±1 | 2.75 | LSB |
| $E_O$ | Offset error | | –9 | ±2 | 9 | LSB |
| | Offset error matching | | | ±0.5 | | LSB |
| $\Delta E_O/\Delta T$ | Offset error temperature drift | | | 1 | | ppm/°C |
| $G_E$ | Gain error | | –0.027 | ±0.01 | 0.027 | %FSR |
| | Gain error matching | | | 0.2 | | %FSR |
| $\Delta G_E/\Delta T$ | Gain drift | | | 5 | | ppm/°C |
| | Transition noise | Mid code, PFS – 1000, NFS + 1000 | | 0.675 | | LSB |
| **AC ACCURACY** | | | | | | |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 2 kHz | 88 | 90.8 | | dB |
| | | $f_{IN}$ = 100 kHz | | 90 | | |
| SINAD | Signal-to-noise plus distortion | $f_{IN}$ = 2 kHz | 87 | 90.5 | | dB |
| | | $f_{IN}$ = 100 kHz | | 89.6 | | |
| THD | Total harmonic distortion | $f_{IN}$ = 2 kHz | | –100 | | dB |
| | | $f_{IN}$ = 100 kHz | | –95 | | |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 2 kHz | | 105 | | dB |
| | | $f_{IN}$ = 100 kHz | | 100 | | |
| ISOXT | Channel to channel isolation | $f_{IN_ADCA}$ = 15 kHz at 10% FSR<br>$f_{IN_ADCB}$ = 25 kHz at 100% FSR | | –115 | | dB |


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| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INTERNAL REFERENCE BUFFER** | | | | | | |
| $G_{REFBUF}$ | Reference buffer gain | | | 1.75 | | V/V |
| | Reference buffer output offset ($V_{REFP_x}$ - $V_{REFIN}$)(1) | | –1 | 0 | 1 | mV |
| | Reference buffer output offset temperature drift | | | 10 | | µV/C |
| | Reference buffer output mismatch ($V_{REFP_A}$ - $V_{REFP_B}$) | | –500 | ±50 | 500 | µV |
| $C_{REFP_x}$ | Reference buffer output capacitor | For specified performance, between each pair of REFP_x and REFM_x | 7 | 10 | 27 | µF |
| **DIGITAL INPUTS** | | | | | | |
| $V_{IH}$ | High-level input voltage | DVDD > 2.3 V | 0.7 × DVDD | | DVDD +0.3 | V |
| $V_{IL}$ | Low-level intput voltage | | –0.3 | | 0.3 × DVDD | V |
| $V_{IH}$ | High-level input voltage | DVDD ≤ 2.3 V | 0.8 × DVDD | | DVDD +0.3 | V |
| $V_{IL}$ | Low-level intput voltage | | –0.3 | | 0.2 × DVDD | V |
| **DIGITAL OUTPUTS** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 500-µA source | 0.8 × DVDD | | DVDD | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = 500-µA sink | 0 | | 0.2 × DVDD | V |
| **POWER SUPPLY** | | | | | | |
| $I_{AVDD}$ | Analog supply current | AVDD = 5 V, $f_{DATA}$ = 2.048 MSPS | | 16.5 | 20 | mA |
| | | AVDD = 5 V, no conversion | | 9 | | |
| PSRR | Power supply rejection ratio | 100-$mV_{p-p}$ ripple on AVDD, frequency < 100 kHz | | 70 | | dB |

(1) REFP_x refers to the REFP_A and REFP_B reference pins for the ADC_A and ADC_B respectively.

## 6.6 Timing Requirements

at AVDD = 4 V to 5.5 V, DVDD = 2.35 V to 5.5 V and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A$ = –40°C to +125°C; typical values at $T_A$ = 25°C, AVDD = 5 V and DVDD = 3.3 V

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **CONVERSION CONTROL** | | | | | |
| $t_{Cycle}$ | Cycle time | 488 | | | ns |
| $f_{Sample}$ | Sampling rate | | | 2048 | kSPS |
| $t_{ACQ}$ | Acquisition time | $t_{CYCLE}$ - 160 | | | ns |
| $t_{WH_\overline{CS}}$ | Pulse duration: $\overline{CS}$ high | 15 | | | ns |
| $t_{WL_\overline{CS}}$ | Pulse duration: $\overline{CS}$ low | 15 | | | ns |
| **SPI MODES** | | | | | |
| $f_{CLK}$ | Serial clock frequency | | | 32.768 | MHz |
| $t_{CLK}$ | Serial clock time period | 1/ $f_{CLK}$ | | | |
| $t_{PH_CLK}$ | SCLK high time | 0.45 | | 0.55 | $t_{CLK}$ |
| $t_{PL_CLK}$ | SCLK low time | 0.45 | | 0.55 | $t_{CLK}$ |
| $t_{SU_CSCK}$ | Setup time: $\overline{CS}$ faling to first SCLK capture edge | 14 | | | ns |
| $t_{HT_CKCS}$ | Delay time: last SCLK launch edge to $\overline{CS}$ rising | 8 | | | ns |

## 6.7 Switching Characteristics

at AVDD = 4 V to 5.5 V, DVDD = 2.35 V to 5.5 V and maximum throughput (unless otherwise noted); minimum and maximum values at $T_A$ = –40°C to +125°C; typical values at $T_A$ = 25°C, AVDD = 5 V and DVDD = 3.3 V

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **CONVERSION** | | | | | |
| $t_{CONV}$ | Conversion time | | | 422 | ns |
| **SPI MODES** | | | | | |
| $t_{DEN_CSDO}$ | Delay time: $\overline{CS}$ falling to data valid on SDO-x | | | 14 | ns |
| $t_{DZ_CSDO}$ | Delay time: $\overline{CS}$ rising edge to SDO-x tristate | | | 13 | ns |
| $t_{D_CKDO}$ | Delay time: SCLK launch edge to next data valid on SDO-x | | | 16 | ns |


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## 6.8 Timing Diagrams

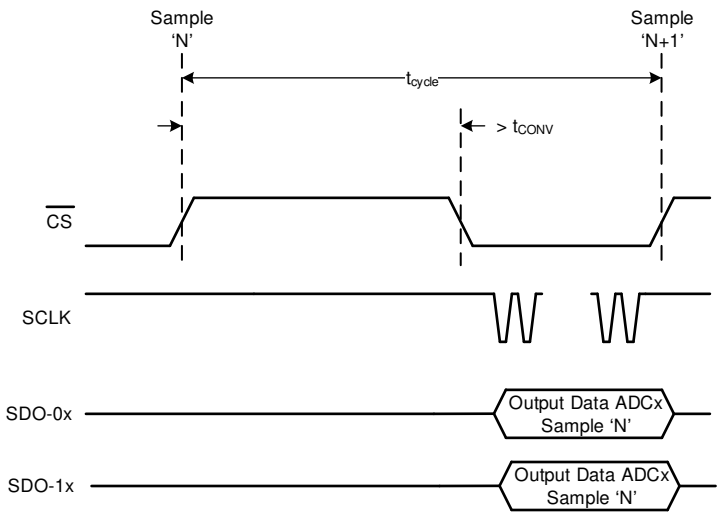


**Figure 6-1. Conversion Control Latency-0 Data Capture**

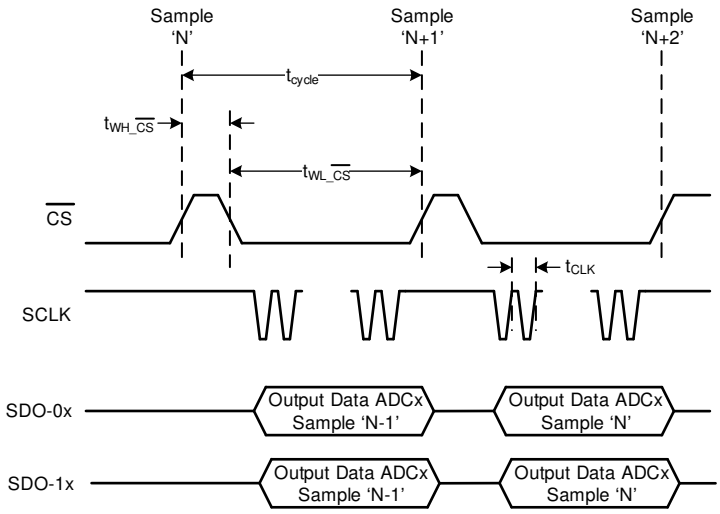


**Figure 6-2. Conversion Control Latency-1 Data Capture**

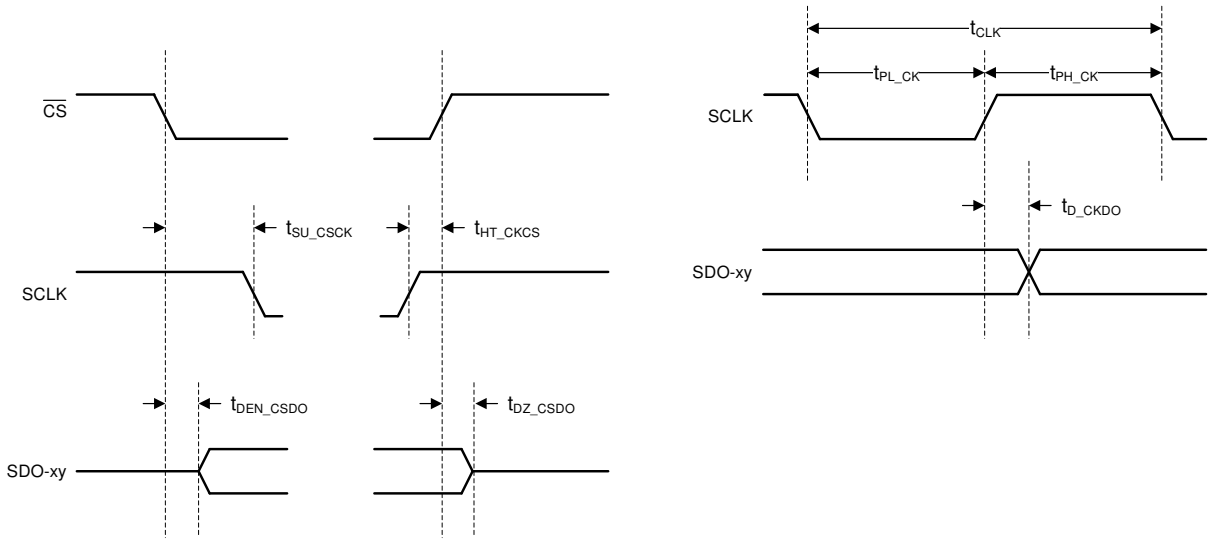


**Figure 6-3. SPI-Compatible Serial Interface Timing**


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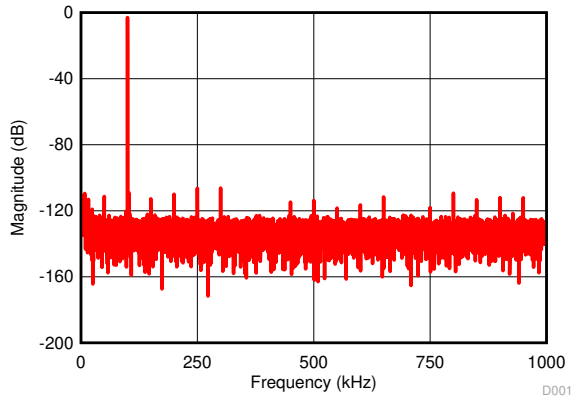
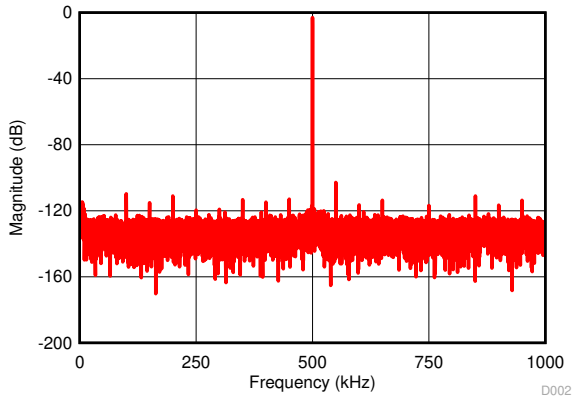
## 6.9 Typical Characteristics

at $T_A$ = 25°C, AVDD = 5 V, DVDD = 3.3 V, $V_{REFIN}$ = 2.5 V, and $f_{Sample}$ = 2.048 MSPS (unless otherwise noted)



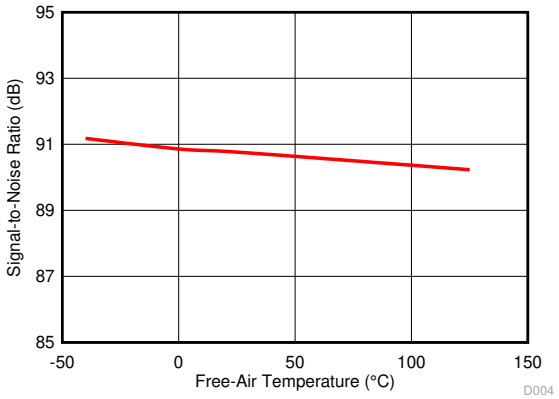

$f_{IN}$ = 100 kHz, SNR = 90.1 dB, THD = –99.3 dB

**Figure 6-4. Typical FFT at $f_{IN}$ = 100 kHz**



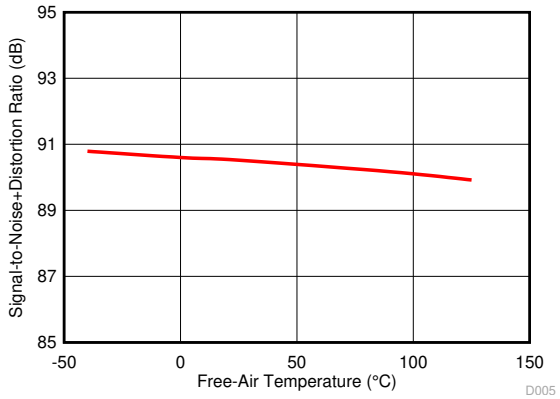

$f_{IN}$ = 500 kHz, SNR = 90 dB, THD = –90.9 dB

**Figure 6-5. Typical FFT at $f_{IN}$ = 500 kHz**



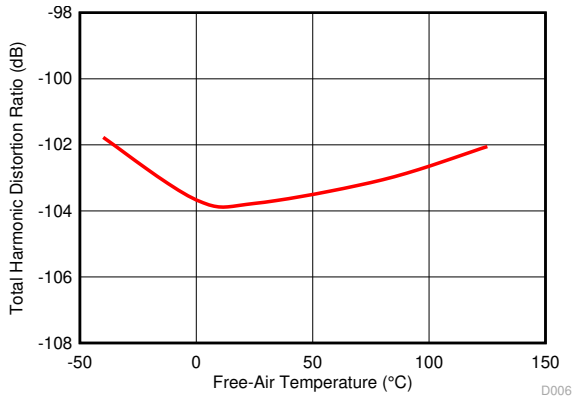

$f_{IN}$ = 2 kHz

**Figure 6-6. SNR vs Free-Air Temperature**




$f_{IN}$ = 2 kHz

**Figure 6-7. SINAD vs Free-Air Temperature**




$f_{IN}$ = 2 kHz

**Figure 6-8. THD vs Free-Air Temperature**

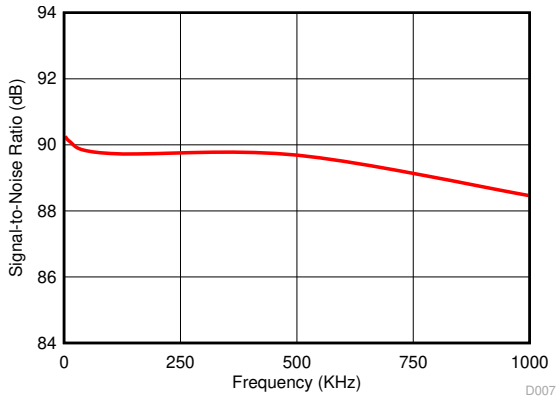



**Figure 6-9. SNR vs Input Frequency**

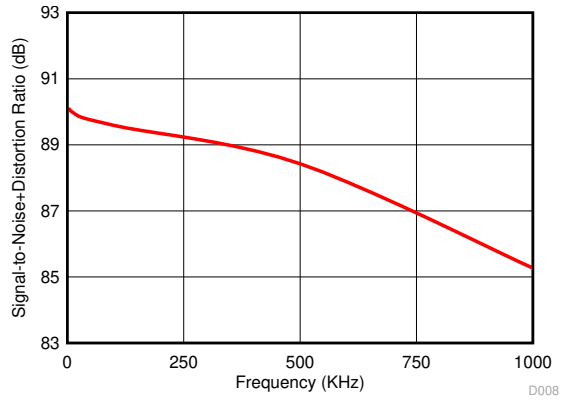



**Figure 6-10. SINAD vs Input Frequency**

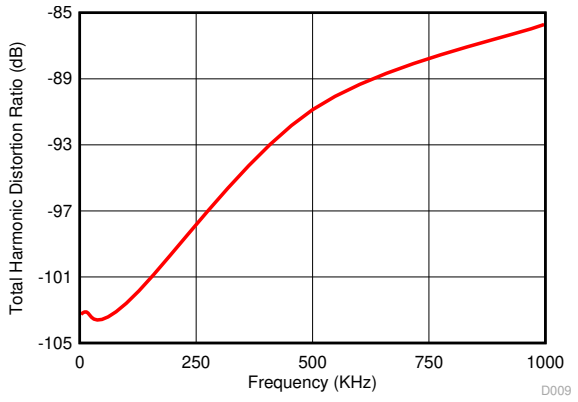
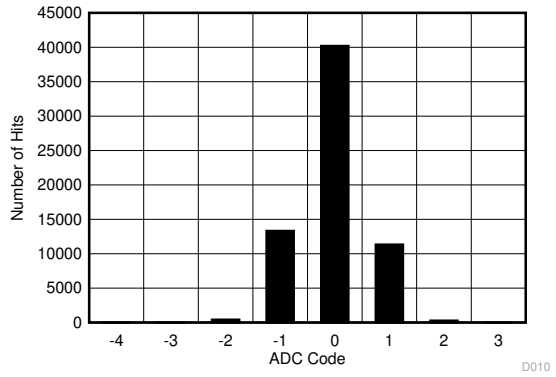



**Figure 6-11. THD vs Input Frequency**




Standard deviation = 0.65 LSB

**Figure 6-12. DC Input Histogram**

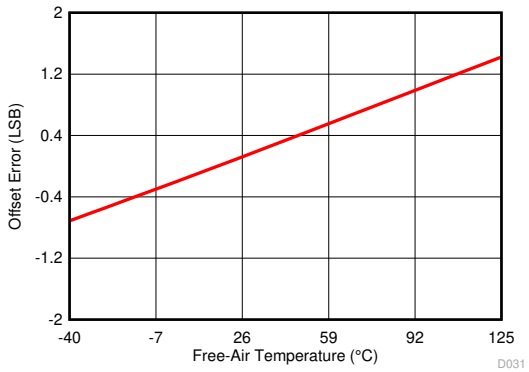



**Figure 6-13. Offset Error vs Free-Air Temperature**

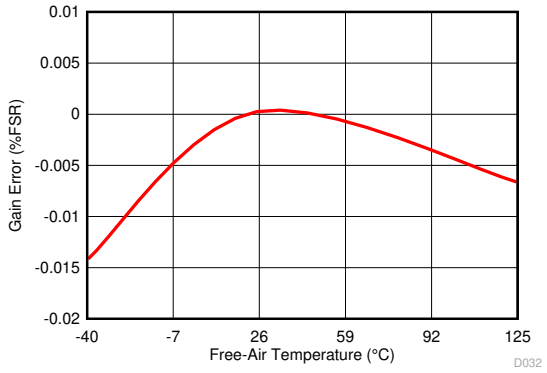



**Figure 6-14. Gain Error vs Free-Air Temperature**

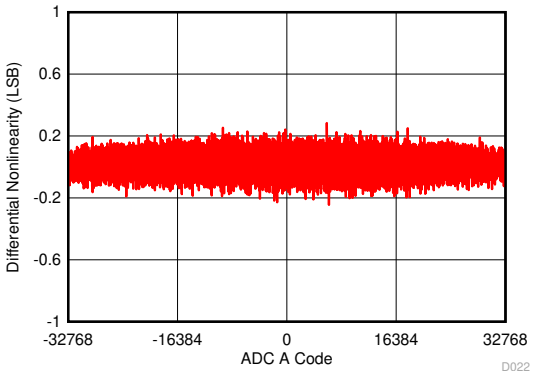



**Figure 6-15. Typical DNL ADC A**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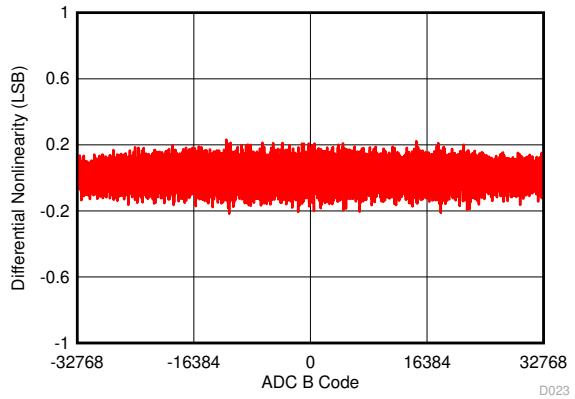


**Figure 6-16. Typical DNL ADC B**

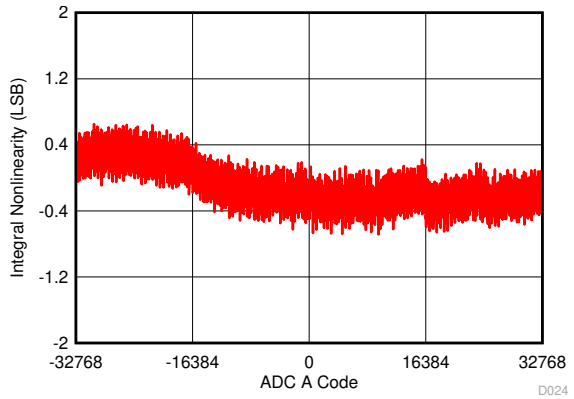


**Figure 6-17. Typical INL ADC A**

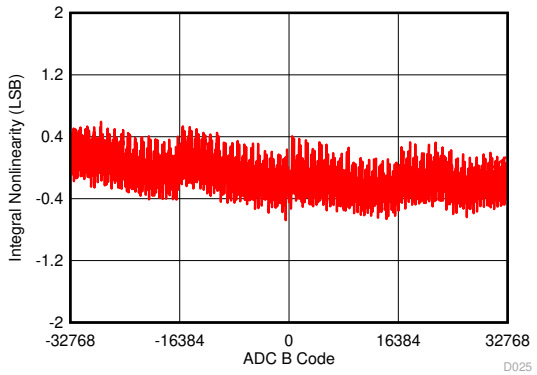


**Figure 6-18. Typical INL ADC B**

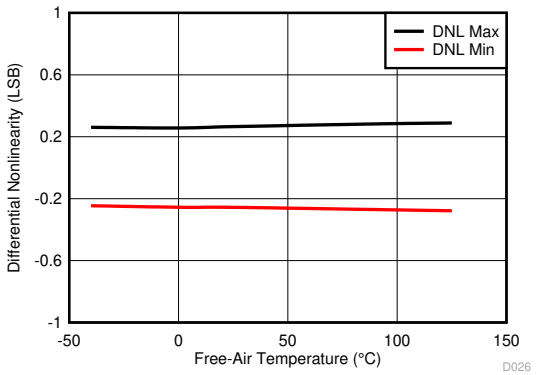


**Figure 6-19. DNL vs Free-Air Temperature**

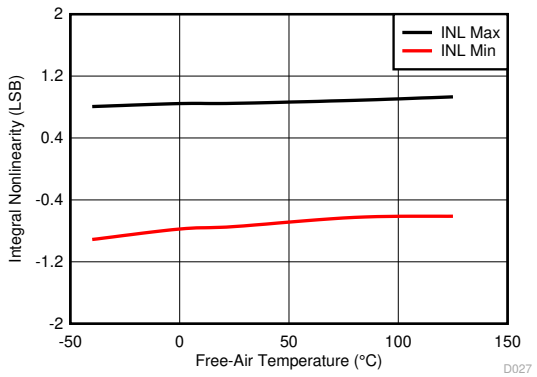


**Figure 6-20. INL vs Free-Air Temperature**

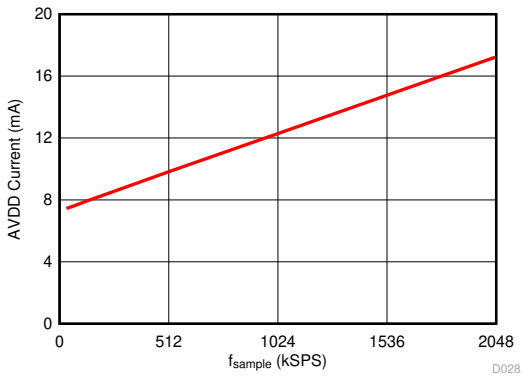


**Figure 6-21. Dynamic AVDD Current vs Sampling Rate**

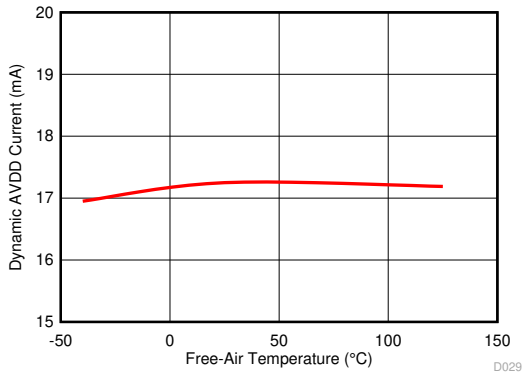


**Figure 6-22. Dynamic AVDD Current vs Free-Air Temperature**

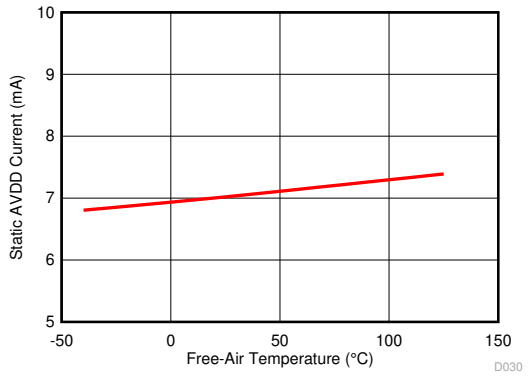


**Figure 6-23. Static AVDD Current vs Free-Air Temperature**


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# 7 Detailed Description

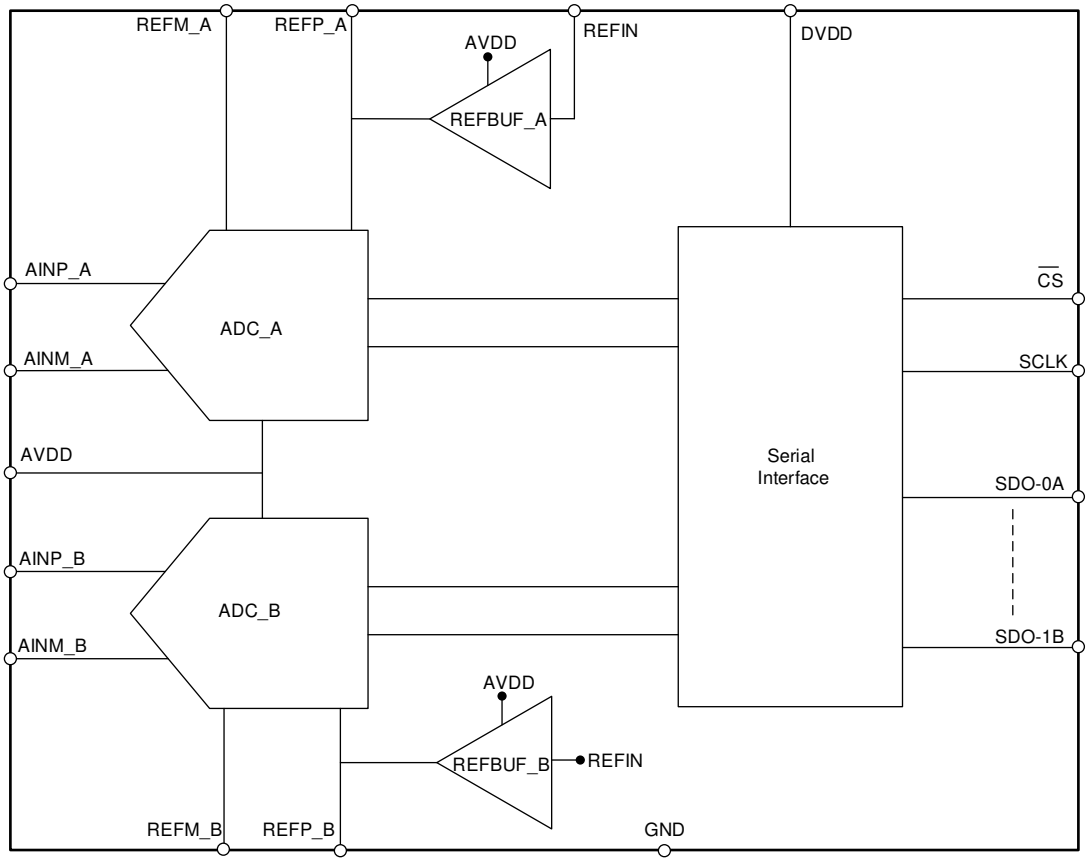
## 7.1 Overview

The ADS9226 is a 16-bit, dual-channel, high-speed, simultaneous-sampling, analog-to-digital converter (ADC). The device supports pseudo-differential input signals and a full-scale range equal to 2 × $V_{REFIN}$ .

When a conversion is initiated, the difference between the AINP_x and AINM_x pins is sampled on the internal capacitor array. The device uses an internal clock to perform conversions. During the conversion process, both analog inputs are disconnected from the internal circuit. At the end of the conversion process, the device reconnects the sampling capacitors to the AINP_x and AINM_x pins and enters an acquisition phase. The device includes reference buffers to provide the charge required by the ADCs during conversion.

The device includes a traditional serial programming interface (SPI)-compatible serial interface to interface with a variety of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs).

## 7.2 Functional Block Diagram



## 7.3 Feature Description

From a functional perspective, the device is comprised of five modules: two converters (ADC_A, ADC_B), two reference buffers (REFBUF_A, REFBUF_B), and the serial interface, as illustrated in Section 7.2.

The converter module samples and converts the analog input into an equivalent digital output code. The reference buffers provide the charge required by the converters for the conversion process. The serial interface module facilitates communication and data transfer between the device and the host controller.

### 7.3.1 Converter Modules

As shown in Figure 7-1, both converter modules sample the analog input signal (provided between the AINP_x and AINM_x pins), compare this signal with the reference voltage (between the pair of REFP_x and REFM_x pins), and generate an equivalent digital output code. The converter modules receive the $\overline{CS}$ input from the interface module, and output the ADCST signal and the conversion result back to the interface module.

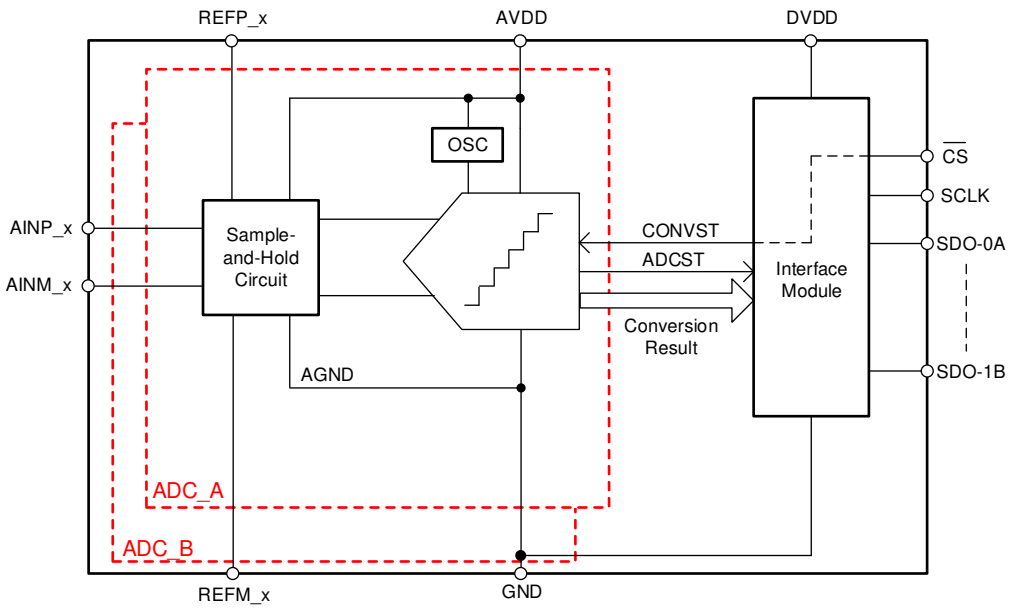



**Figure 7-1. Converter Modules**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#### 7.3.1.1 Analog Input With Sample-and-Hold

This device supports unipolar, pseudo-differential analog input signals. Figure 7-2 shows a small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by a resistance ($R_{S1}$ and $R_{S2}$, typically 120 Ω) in series with an ideal switch ($SW_1$ and $SW_2$). The sampling capacitors, $C_{S1}$ and $C_{S2}$, are typically 16 pF.

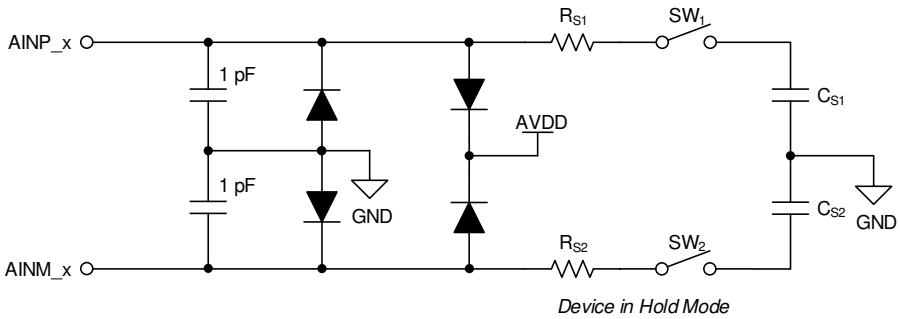


**Figure 7-2. Analog Input Structure for Converter Module**

During the acquisition process, both inputs are individually sampled on $C_{S1}$ and $C_{S2}$, respectively. During the conversion process, both converters convert for the respective voltage difference between the sampled values: $V_{AINP_x} – V_{INM_x}$.

Equation 1 and Equation 2 provide the full-scale input range (FSR) and bias voltage ($V_{BIAS}$) at the negative input), supported at the analog inputs for the reference voltage ($V_{REFIN}$ ) on the REFIN pin.

$$FSR = \pm V_{REFIN} = 2 \times V_{REFIN} \quad (1)$$

$$V_{BIAS} = V_{REFIN} \pm 0.1\ V \quad (2)$$

### 7.3.1.2 ADC Transfer Function

This device supports unipolar, pseudo-differential input signals. The device output is in two's complement format. Figure 7-3 and Table 7-1 show the ideal transfer characteristics for the device. Equation 3 gives the least significant bit (LSB) for the ADC.

$$1\ \text{LSB} = \text{FSR} / 2^n \tag{3}$$

where

- FSR is defined in Equation 1
- n = Resolution of the device

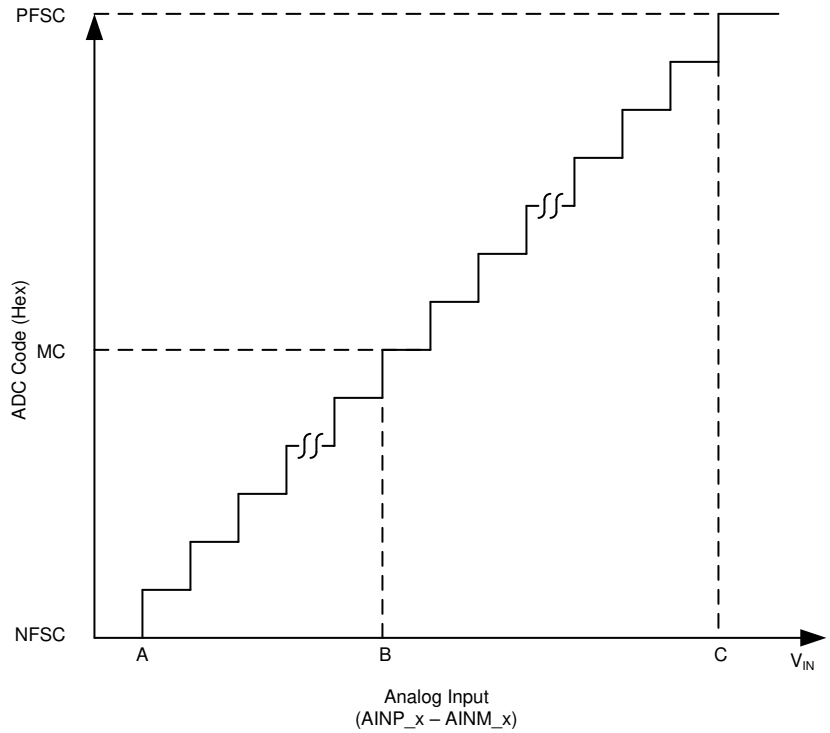


**Figure 7-3. Ideal Transfer Characteristics**

**Table 7-1. Transfer Characteristics**

| STEP | INPUT VOLTAGE (AINP_x-AINM_x) | CODE | DESCRIPTION | IDEAL OUTPUT CODE (R = 16) |
|---|---|---|---|---|
| A | ≤ –($V_{REF}$ – 0.5 LSB) | NFSC | Negative full-scale code | 8000 |
| B | – 0.5 LSB to 0.5 LSB | MC | Mid code | 0000 |
| C | ≥ ($V_{REF}$ – 1.5 LSB) | PFSC | Positive full-scale code | 7FFF |


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### 7.3.2 External Reference Voltage

The device requires an external reference voltage of the value $V_{REFIN}$ , as specified in Section 6. Figure 7-4 shows the connections for using the device with an external reference. A reference without an integrated buffer can be used because of the high input impedance of the REFIN pin.

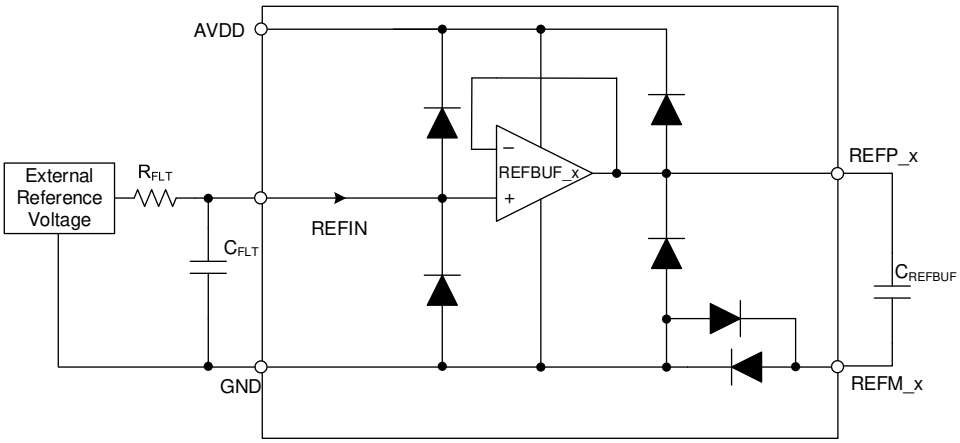


**Figure 7-4. Connection Diagram for Reference and Reference Buffers**

### 7.3.3 Reference Buffers

On the $\overline{CS}$ rising edge, both converters start converting the sampled value on the analog input, and the internal capacitors are switched to the REFP_x pins. Most of the switching charge required during the conversion process is provided by the external decoupling capacitor $C_{REFP_x}$. If the charge lost from $C_{REFP_x}$ is not replenished before the next $\overline{CS}$ rising edge, the subsequent conversion occurs with this different reference voltage and causes a proportional error in the output code. To eliminate these errors, the internal reference buffers of the device maintains the voltage on the REFP_x pins.

All performance characteristics of the device are specified with the internal reference buffer and a specified value of $C_{REFP_x}$. As shown in Figure 7-4, place a decoupling capacitor $C_{REFP_x}$ between the REFP_x pins and the REFM_x pin as close to the device as possible.

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## 7.4 Device Functional Modes

This device supports two functional states: acquisition phase (ACQ) and conversion phase (CNV).

### 7.4.1 ACQ State

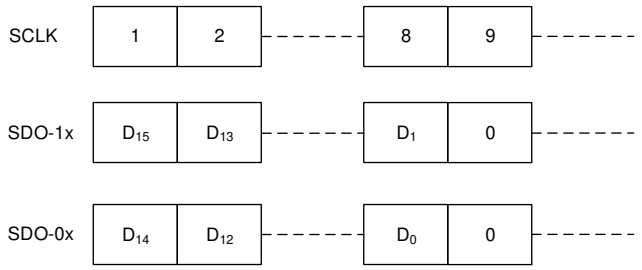
In ACQ state, the device acquires the analog input signal. The device enters ACQ state at power-up, when coming out of power down and by the ADCST signal (internal). A $\overline{CS}$ rising edge takes the device from ACQ state to CNV state.

### 7.4.2 CNV State

The device moves from ACQ state to CNV state and starts conversion on a rising edge of the $\overline{CS}$ pin. The conversion process uses an internal clock. The host must provide a minimum time of $t_{CYCLE}$ between two subsequent start of conversions.

### 7.4.3 Output Data Word

The output data word consists of a conversion result of N bits where N = 16 for the ADS9226. The output data word D[N-1:0], as shown in Figure 7-5, is left-justified and split into two data lines (SDO-xy) for each ADC.




For ADC_A, x = A. For ADC_B, x = B.

**Figure 7-5. Output Data Word**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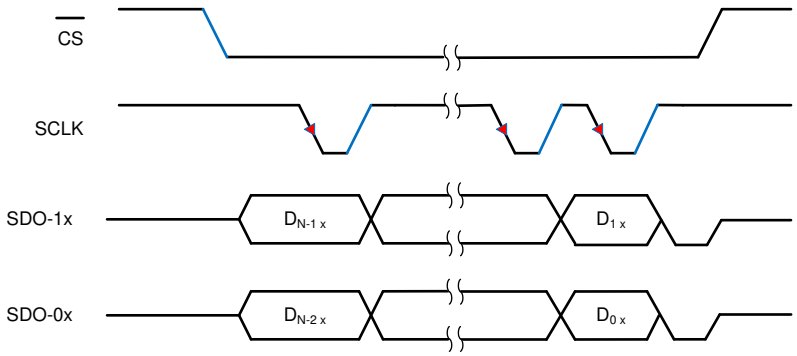
### 7.4.4 Conversion Control and Data Transfer Frame

A data transfer frame starts with a falling edge of the $\overline{CS}$ signal. In any frame, the clocks provided on the SCLK pin are used to transfer the output data for the completed conversion. The device has two SDOs (SDO-0x and SDO-1x) for each ADC. For ADC_A, the device provides data on SDO-0A and SDO-1A, whereas for ADC_B, the device provides data on SDO-0B and SDO-1B. The most significant bit ($D_{n-1x}$) of the output data is launched on the SDO-1x pins and the MSB-1 ($D_{n-2x}$) bit is launched on the SDO-0x pins on the falling edge of $\overline{CS}$, any subsequent output bits are launched on the rising edges provided on SCLK. When all output bits of the conversion result are shifted out, the device launches 0's on the subsequent SCLK rising edges. The data transfer frame ends with a rising edge of the $\overline{CS}$ signal. For detailed timing specifications, see Section 6 and Figure 7-6.

The $\overline{CS}$ pulse high time determines if the data being read back is with a 0 sample latency or a 1 sample latency. See Figure 6-1 and Figure 6-2 for the respective timing diagrams. The maximum-rated sampling rate of 2.048 MSPS is achieved with a latency-1 data capture.




For ADC_A, x = A. For ADC_B, x = B.

**Figure 7-6. Data Transfer Frame for Reading Data**

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR) analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section presents general principles for designing these circuits, followed by an application circuit designed using the ADS9226.

### 8.1.1 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a charge-kickback filter. The amplifier is used for signal conditioning of the input signal and the low output impedance of the amplifier provides a buffer between the signal source and the switched-capacitor inputs of the ADC. The charge-kickback filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC, and band-limits the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of the ADS9226.

#### *8.1.1.1 Charge-Kickback Filter*

The charge-kickback filter is an RC filter at the input pins of the ADC that filters the broadband noise from the front-end drive circuitry and attenuates the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, $C_{FLT}$ (as shown in Figure 8-1), is connected from each input pin of the ADC to ground. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 20 times the specified value of the ADC sampling capacitance. For the ADS9226, the input sampling capacitance is equal to 16 pF; therefore, for optimal performance, keep $C_{FLT}$ greater than 320 pF. This capacitor must be a COG- or NPO-type. The type of dielectric used in COG or NPO ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

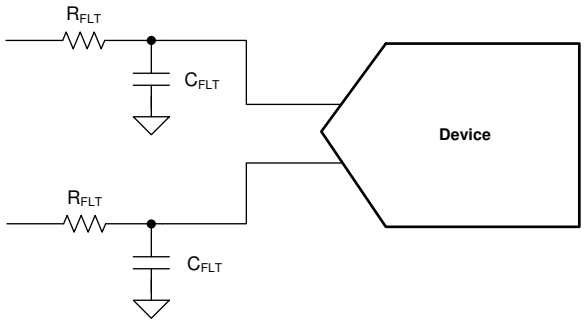



**Figure 8-1. Charge-Kickback Filter**

Driving capacitive loads can degrade the phase margin of the input amplifier, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors ($R_{FLT}$) are used at the output of the amplifiers. A higher value of $R_{FLT}$ helps with amplifier stability, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of $R_{FLT}$ requires balancing the stability of the driver amplifier and distortion performance of the design. Always verify the stability and settling behavior of the driving amplifier and charge-kickback filter by TINA-TI™ SPICE simulation. Keep the tolerance of the selected resistors less than 1% to keep the inputs balanced.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### 8.1.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type, as well as the performance goals, of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- Small-signal bandwidth. Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the ADC sample-and-hold capacitor and the RC filter (the charge-kickback filter) at the inputs of the ADC. Higher bandwidth amplifiers offer faster settling times when driving the capacitive load of the charge-kickback filter, thus reducing harmonic distortion at higher input frequencies. Equation 4 describes the unity-gain bandwidth (UGB) of the amplifier to be selected in order to maintain the overall stability of the input driver circuit:

$$UGB \geq 4 \times \left( \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \tag{4}$$

- Distortion. Both the ADC and the input driver introduce distortion in a data acquisition block. Equation 5 shows that to make sure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB less than the distortion of the ADC:

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \tag{5}$$

- Noise. Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. Generally, to make sure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Equation 6 explains that noise from the input driver circuit is band-limited by designing a low cutoff frequency, charge-kickback filter:

$$N_G \times \sqrt{2} \times \sqrt{\left( \frac{V_{1/f_AMP_PP}}{6.6} \right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \tag{6}$$

  where

  - $V_{1/f_AMP_PP}$ is the peak-to-peak flicker noise in µV
  - $e_{n_RMS}$ is the amplifier broadband noise density in nV/$\sqrt{Hz}$
  - $f_{-3dB}$ is the 3-dB bandwidth of the charge-kickback filter
  - $N_G$ is the noise gain of the front-end circuit that is equal to 1 in a buffer configuration
- Settling Time. For DC signals with fast transients that are common in a multiplexed application, the input signal must settle within an 16-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Settling accuracy for DC transients directly translates to the linear performance for AC input signals, especially those that may use the ADC full-scale range. Typically, amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 16-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA-TI SPICE simulations before selecting the amplifier.

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## 8.2 Typical Application

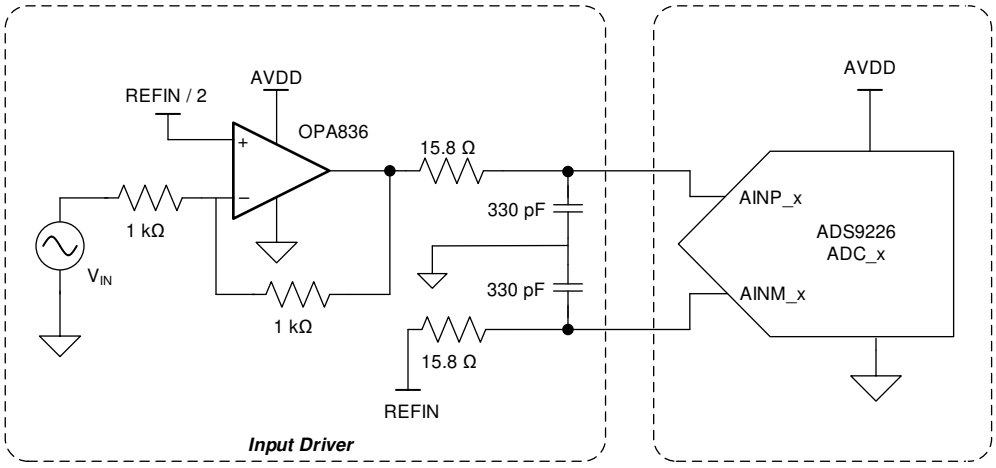


**Figure 8-2. Typical Connection Diagram of the ADS9226 Application Circuit**

### 8.2.1 Design Requirements

The design parameters are listed in Table 8-1 for this example.

**Table 8-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| ADC sample rate | 2 MSPS |
| Analog input signal | 2 kHz, ±2.5 V, pseudo-differential |
| SNR | > 87 dB |
| THD | < –100 dB |
| Power supply | 5-V analog, 3.3-V digital |

### 8.2.2 Detailed Design Procedure

Figure 8-2 shows an application circuit for this example. The device incorporates two independently matched reference buffers for each ADC. Decouple the reference buffer outputs (the REFP_A and REFP_B pins) with the REFM_A and REFM_B pins, respectively, with 10-µF decoupling capacitors. The circuit in Figure 8-2 shows a pseudo-differential data acquisition (DAQ) block optimized for low distortion and noise using the OPA836 and the ADS9226. The single-ended inputs are level-shifted and driven using a high-bandwidth, low-distortion, operational amplifier configured with a gain of –1 V/V and an optimal RC charge-kickback filter before going to the ADC. Generally, the distortion from the input driver must be at least 10 dB less than the ADC distortion. Therefore, these circuits use the OPA836 as an input driver that provides exceptional AC performance because of its extremely low-distortion and high bandwidth specifications. In addition, the components of the charge-kickback filter are selected to keep the noise from the front-end circuit low without adding distortion.


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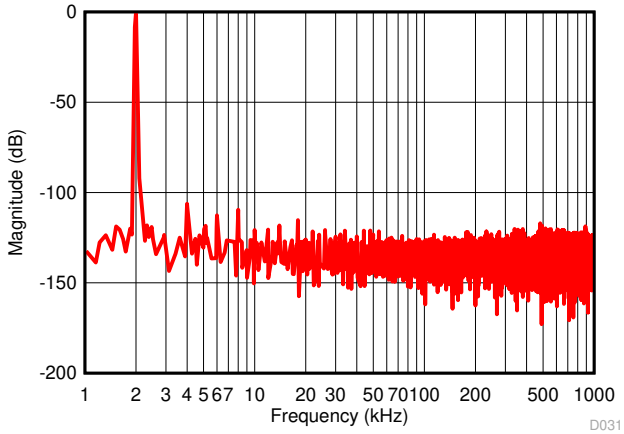
### 8.2.3 Application Curve

Figure 8-3 provides the typical FFT for the circuit shown in Figure 8-2.




SNR = 89.9 dB, THD = –102.9 dB

**Figure 8-3. Typical FFT With a 2-kHz Signal**

## 9 Power Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. The reference buffers and converter modules (ADC_A and ADC_B) operate on AVDD. The serial interface operates on DVDD. AVDD and DVDD can be independently set to any value within their permissible ranges.

As shown in Figure 9-1, connect pins 12 and 29 together and place 1-µF decoupling capacitors between pin 12 (AVDD) and pin 11 (GND), and between pin 29 (AVDD) and pin 30 (GND). To decouple the DVDD supply, place a 1-µF decoupling capacitor between pin 28 (DVDD) and pin 27 (GND), and between pin 26 (DVDD) and pin 27 (GND).

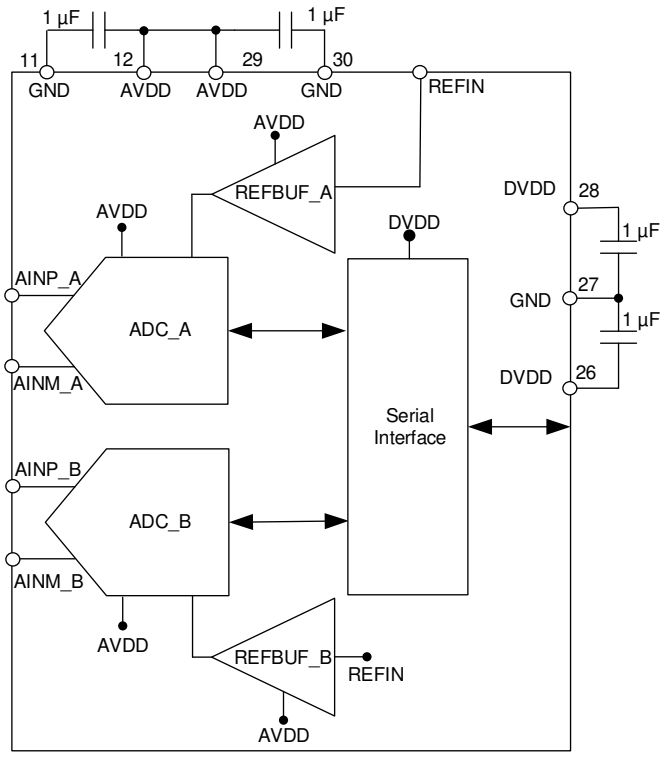



**Figure 9-1. Power-Supply Decoupling**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# 10 Layout

## 10.1 Layout Guidelines

This section provides some layout guidelines for achieving optimum performance with the ADS9226.

### 10.1.1 Signal Path

Route the analog input signals in opposite directions to the digital connections. The reference decoupling components are kept away from the switching digital signals. This arrangement prevents noise generated by digital switching activity from coupling to sensitive analog signals.

### 10.1.2 Grounding and PCB Stack-Up

Low inductance grounding is critical for achieving optimum performance. Grounding inductance is kept below 1 nH with 15-mil grounding vias and a printed circuit board (PCB) layout design that has at least four layers. Place all critical components of the signal chain on the top layer with a solid analog ground from subsequent inner layers to minimize via length to ground.

### 10.1.3 Decoupling of Power Supplies

Place the decoupling capacitors on AVDD and DVDD within 20 mil from the respective pins, and use a 15-mil via to ground from each capacitor. Avoid placing vias between any supply pin and the respective decoupling capacitor.

### 10.1.4 Reference Decoupling

Dynamic currents are present at the REFP_x and REFM_x pins during the conversion phase, and excellent decoupling is required to achieve optimum performance. Place a 10-µF, X7R-grade, ceramic capacitor with at least a 10-V rating. Select 0603- or 0805-size capacitors to keep equivalent series inductance (ESL) low. Connect the REFM_x pins to the decoupling capacitor before a ground via. Also place decoupling capacitors on the REFby2 pin.

### 10.1.5 Analog Input Decoupling

Dynamic currents are also present at the pseudo-differential analog inputs of the ADS9226. Use C0G- or NPO-type capacitors to decouple these inputs because with these types of capacitors, capacitance stays almost constant over the full input voltage range. Lower-quality capacitors (such as X5R and X7R) have large capacitance changes over the full input-voltage range that may cause degradation in the performance of the device.

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## 10.2 Layout Example

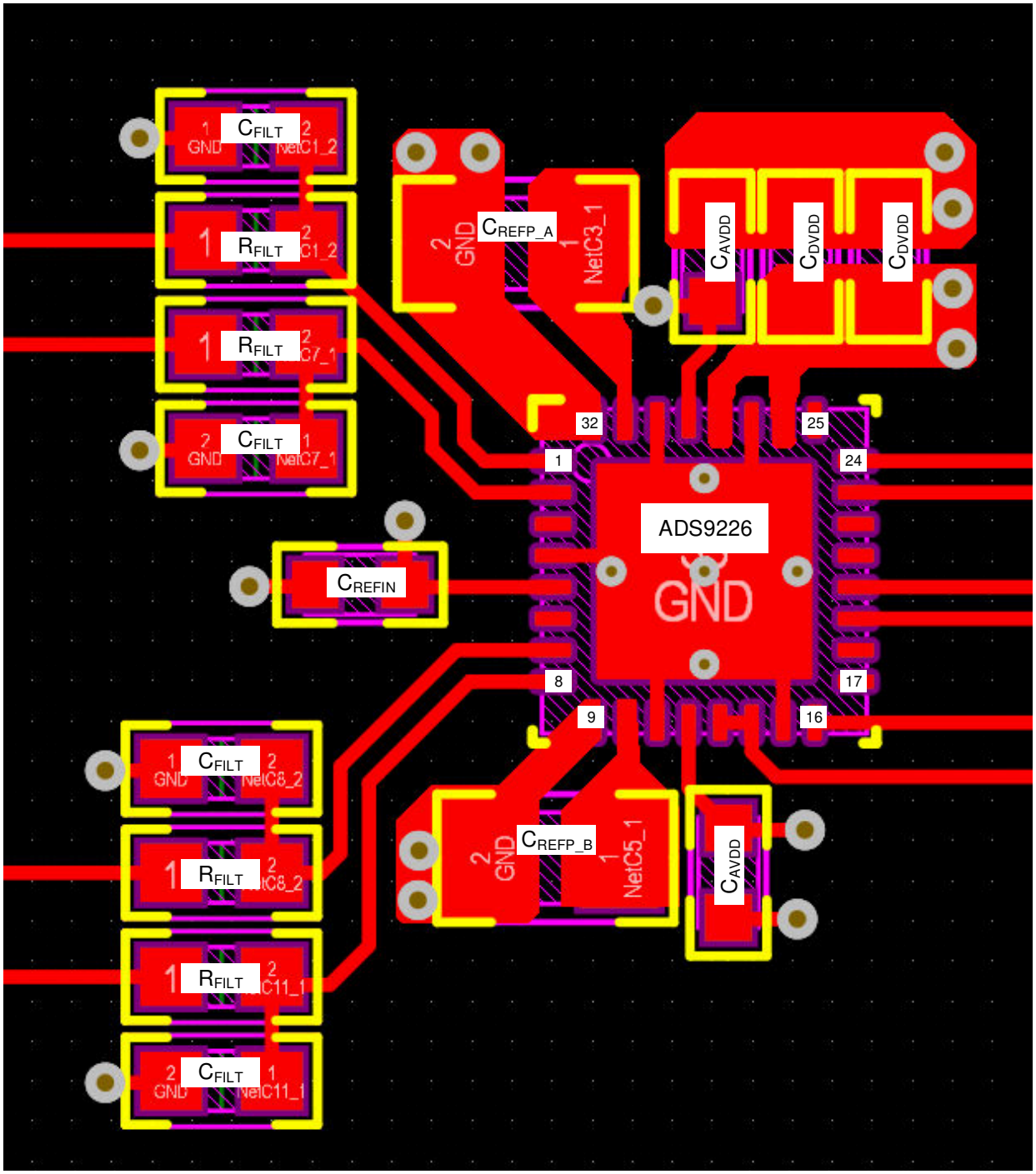


**Figure 10-1. Example Layout for the ADS9226**


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# 11 Device and Documentation Support

## 11.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *OPAx836 Very Low Power, Rail-ro-Rail Out Operational Amplifiers* data sheet

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

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## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADS9226IRHBR | Active | Production | VQFN (RHB) \| 32 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | ADS9226 |
| ADS9226IRHBR.B | Active | Production | VQFN (RHB) \| 32 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | ADS9226 |
| ADS9226IRHBT | Active | Production | VQFN (RHB) \| 32 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | ADS9226 |
| ADS9226IRHBT.B | Active | Production | VQFN (RHB) \| 32 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | ADS9226 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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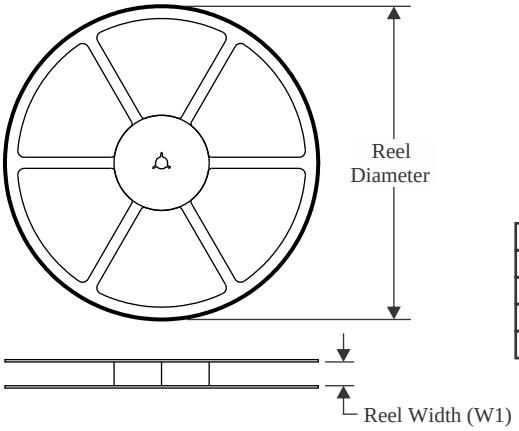
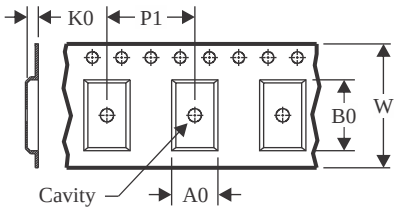
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

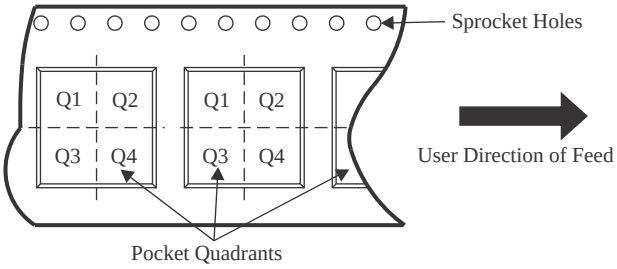



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

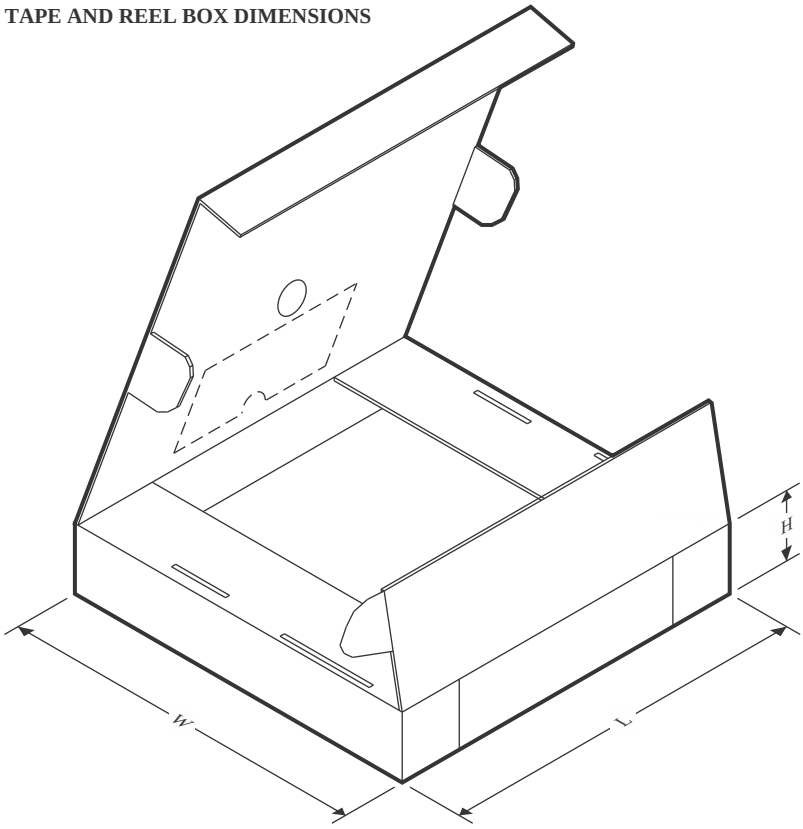
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS9226IRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS9226IRHBR | VQFN | RHB | 32 | 3000 | 350.0 | 350.0 | 43.0 |

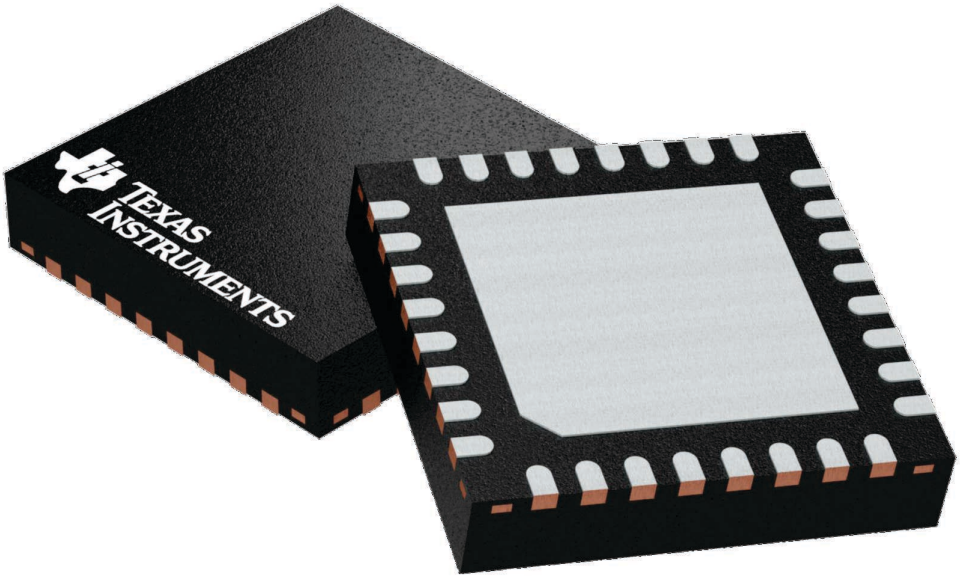
# GENERIC PACKAGE VIEW

## RHB 32

## VQFN - 1 mm max height

**5 x 5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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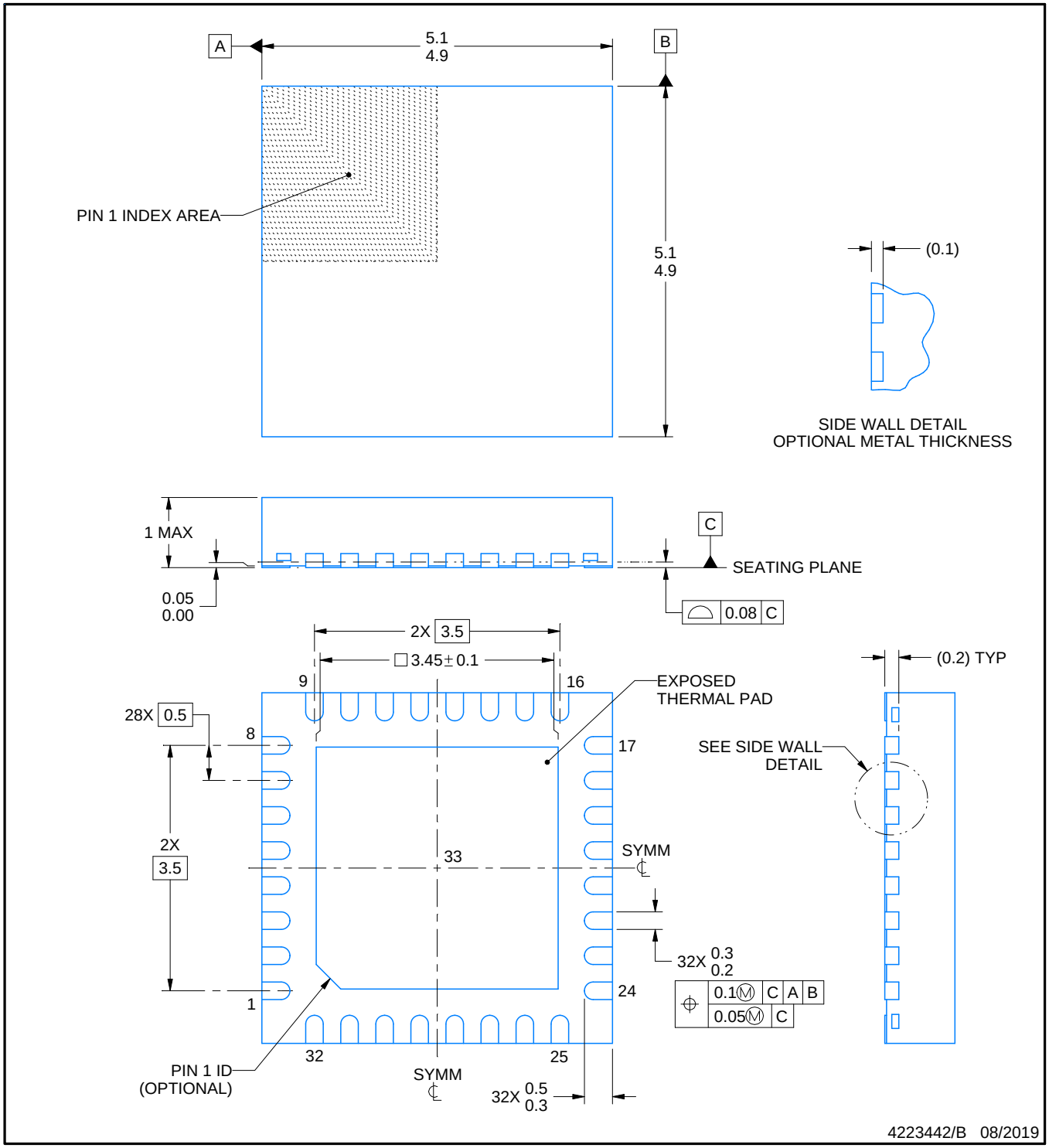
# RHB0032E

# PACKAGE OUTLINE

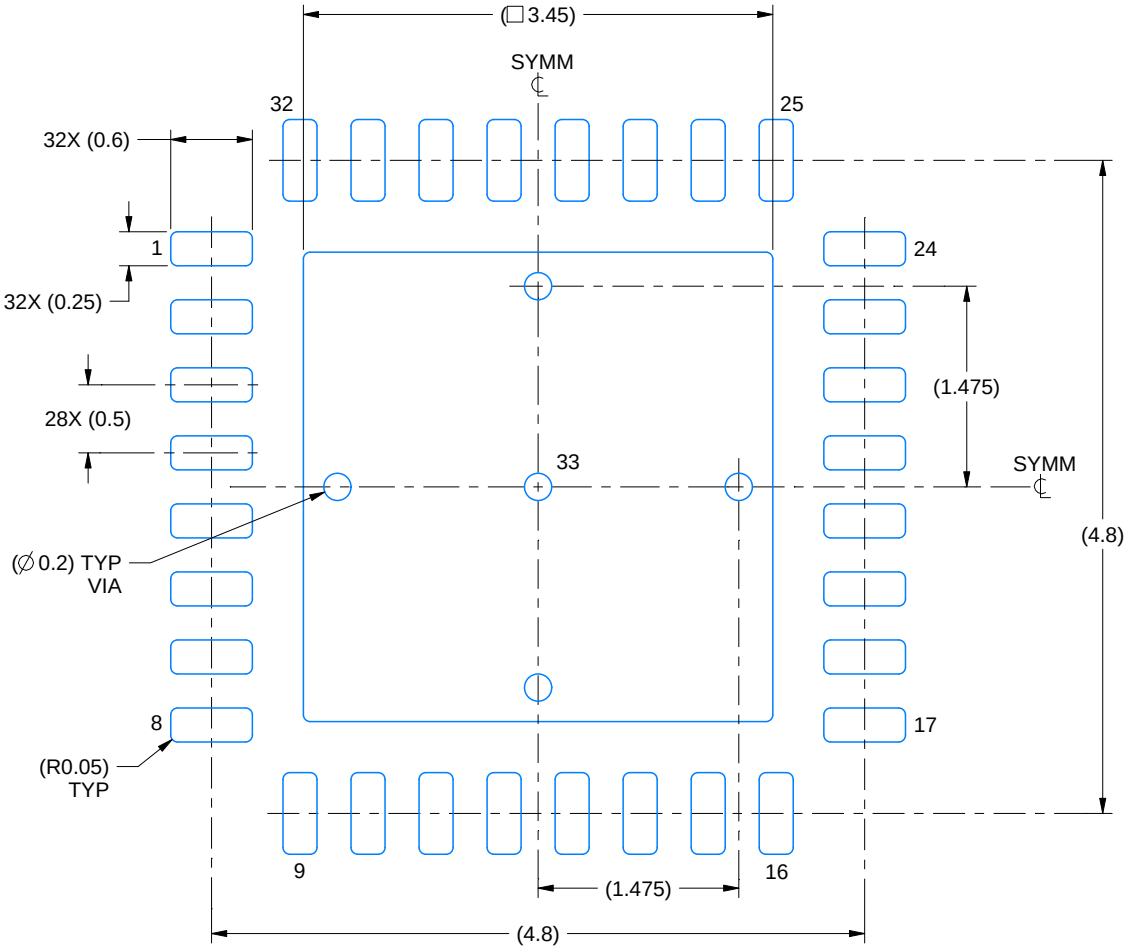
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

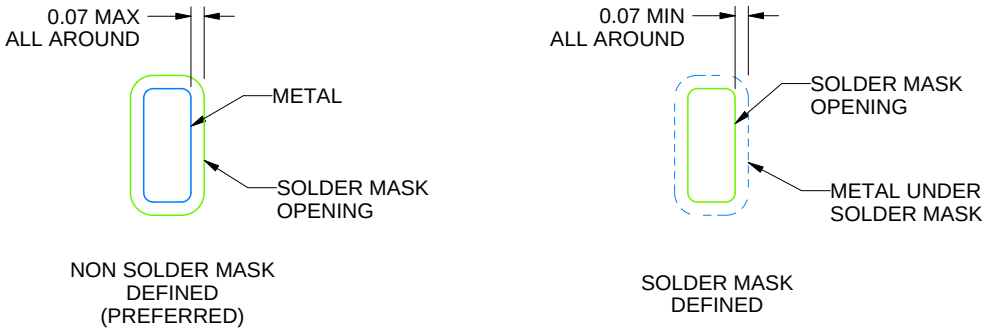



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:18X

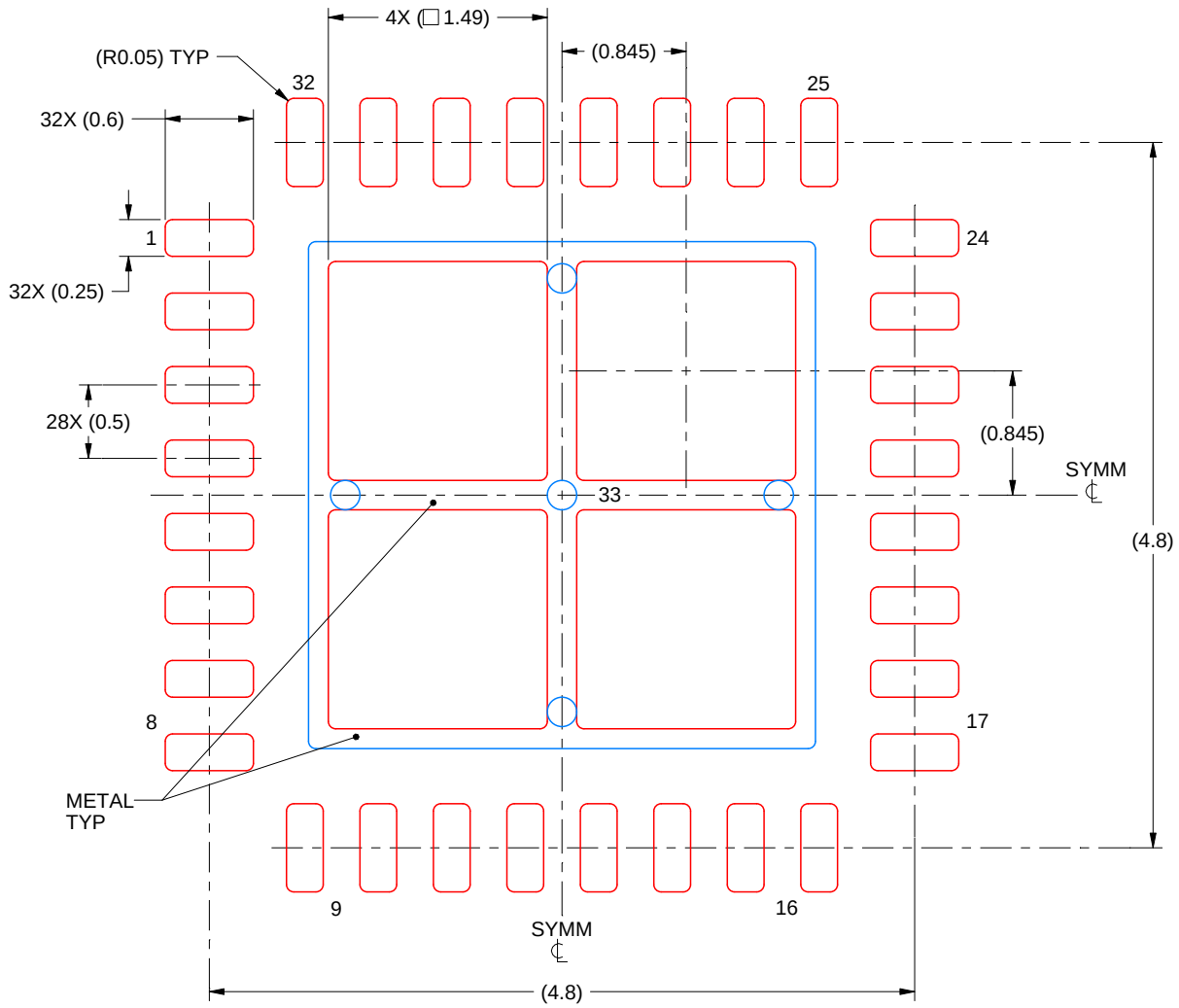



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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