SNx4ACT10 Triple 3-Input Positive-NAND Gates

1 Features

- 4.5V to 5.5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Max t_{pd} of 9.5ns at 5V
- Inputs are TTL-voltage compatible

2 Applications

- Alarm/tamper detect circuit
- S-R latch

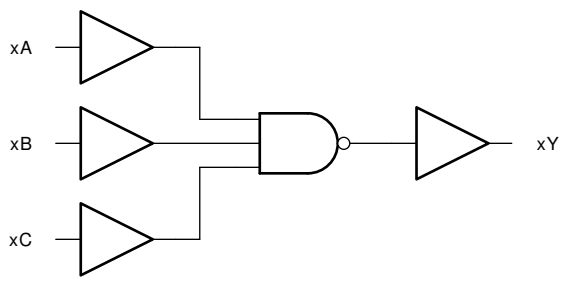
3 Description

The SNx4ACT10 devices contain three independent 3-input NAND gates. The devices perform the Boolean functions $Y = \overline{A \bullet B \bullet C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN54ACT10	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
	J (CDIP, 14)	19.55mm × 7.60mm	19.55mm × 6.71mm
	W (CFP, 14)	9.21mm × 7.11mm	9.21mm × 6.29mm
SN74ACT10	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	N (PDIP, 14)	19.3mm × 9.4mm	19.3mm × 6.35mm
	DB (SSOP, 14)	6.2mm x 7.8mm	6.2mm x 5.3mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm

(1) For more information, see the Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Gate (Positive Logic)

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4 Pin Configuration and Functions

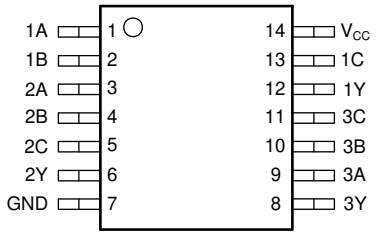

Figure 4-1. J , W Package (Top View)

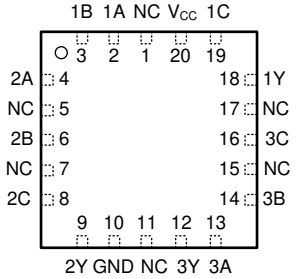

Figure 4-2. FK Package (Top View)

Pin Functions

PIN			TYPE[(1)]	DESCRIPTION
NAME	PDIP , CDIP NO.	LCCC NO.		
1A	1	2	I	Channel 1, Input A
1B	2	3	I	Channel 1, Input B
2A	3	4	I	Channel 2, Input A
2B	4	6	I	Channel 2, Input B
2C	5	8	I	Channel 2, Input C
2Y	6	9	O	Channel 2, Output Y
GND	7	10	G	Ground
3Y	8	12	O	Channel 3, Output Y
3A	9	13	I	Channel 3, Input A
3B	10	14	I	Channel 3, Input B
3C	11	16	I	Channel 3, Input C
1Y	12	18	O	Channel 1, Output Y
1C	13	19	I	Channel 1, Input C
V_{CC}	14	20	P	Positive Supply
NC		1, 5, 7, 11, 15, 17	—	Not internally connected

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

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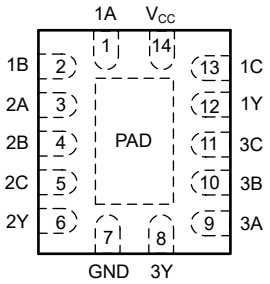

Figure 4-3. SN74ACT10 BQA Package (Top View)

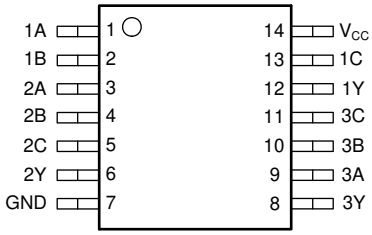

Figure 4-4. SN74ACT10 D , PW , N , DB Package (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
2A	3	I	Channel 2, Input A
2B	4	I	Channel 2, Input B
2C	5	I	Channel 2, Input C
2Y	6	O	Channel 2, Output Y
GND	7	G	Ground
3Y	8	O	Channel 3, Output Y
3A	9	I	Channel 3, Input A
3B	10	I	Channel 3, Input B
3C	11	I	Channel 3, Input C
1Y	12	O	Channel 1, Output Y
1C	13	I	Channel 1, Input C
V_{CC}	14	P	Positive Supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.
(2) BQA package only.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I [2]	Input voltage range		−0.5	V_{CC} + 0.5	V
V_O [2]	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

(over recommended operating free-air temperature range (unless otherwise noted)[1]

		SN54ACT10		SN74ACT10		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate		8		8	ns/V
TA	Operating free-air temperature	−55	125	−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the *Implications of Slow or Floating CMOS Inputs* application note.

5.3 Thermal Information

THERMAL METRIC[1]		SNx4ACT10						UNIT
		D (SOIC)	DB	N	NS	PW (TSSOP)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	96	80	76	145.7	91.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54ACT10		SN74ACT10		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I_{OH} = −50 mA (1)	5.5 V				3.85				
	I_{OH} = −75 mA (1)	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V		0.001	0.1		0.1		0.1	V
		5.5 V		0.001	0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA(1)	5.5 V					1.65			
	I_{OL} = 75 mA(1)	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	µA
ΔI_{CC} (2)	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.6			1.6		1.5	mA
C_i	V_I = V_{CC} or GND	5 V		2.6						pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5V ± 0.5V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54ACT10		SN74ACT10		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	9	1	10	1	10	ns
t_{PHL}			1	6.5	9	1	905	1	905	

5.6 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	25	pF

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5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

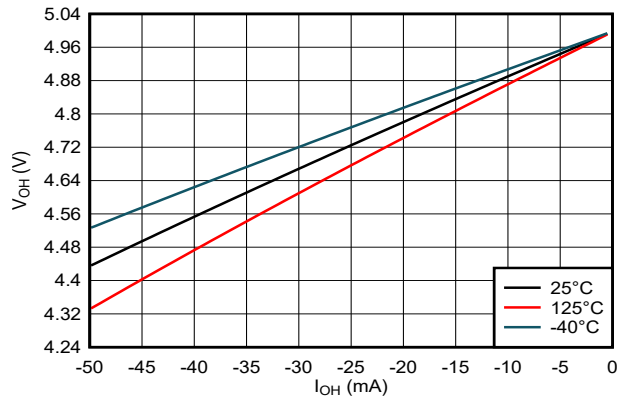


Figure 5-1. Output Voltage vs Current in HIGH State; 5V Supply

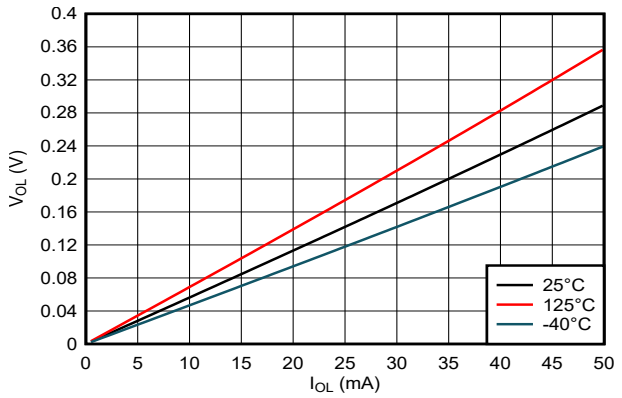
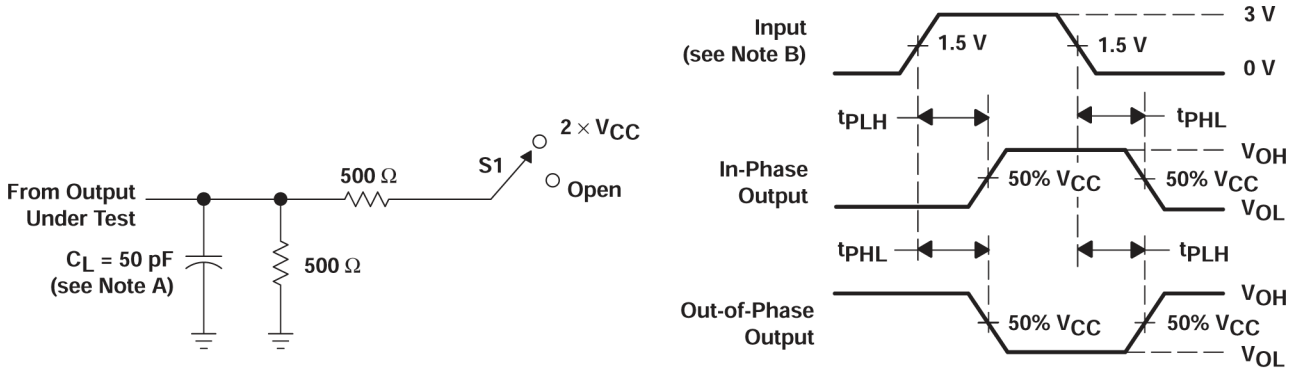


Figure 5-2. Output Voltage vs Current in LOW State; 5V Supply

6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r v 2.5 ns, t_f v 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open

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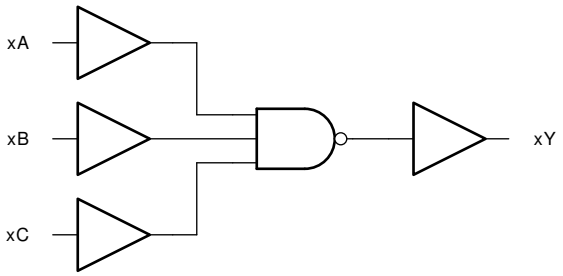
7 Detailed Description

7.1 Overview

This device contains three independent 3-input NAND gates. Each gate performs the Boolean function $Y = \overline{A \bullet B \bullet C}$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

7.3.3 Clamp Diode Structure

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

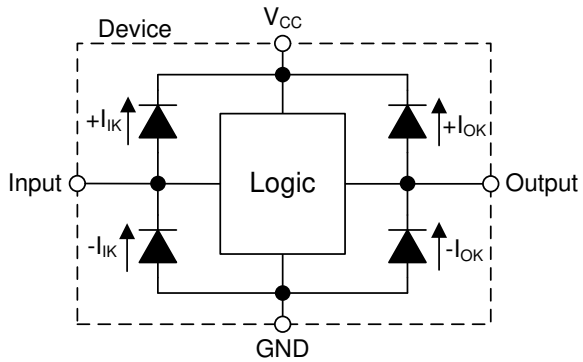


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

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8 Device Functional Modes

Table 8-1. Function Table

INPUTS			OUTPUT Y
A	B	C	
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, two 3-input NAND gates are used to create an active-low SR latch as shown in Figure 9-1. The additional gate can be used elsewhere in the system, or the inputs can be grounded and left unused.

The SNx4ACT10 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

9.2 Typical Application

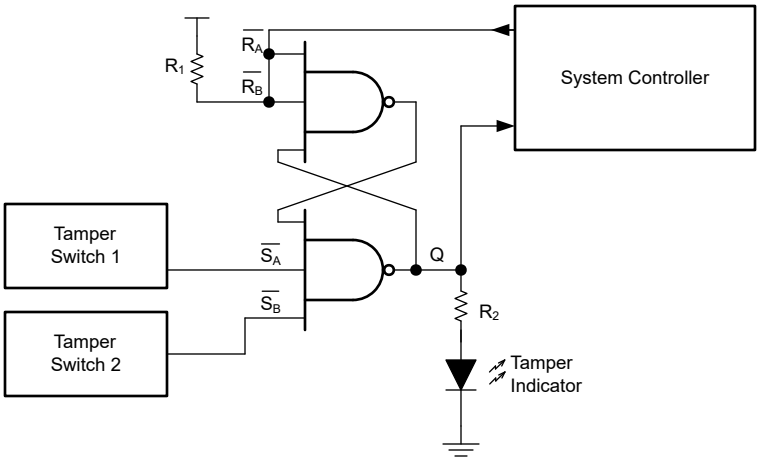

Figure 9-1. Typical Application Block Diagram

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9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SNx4ACT10 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4ACT10 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SNx4ACT10 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SNx4ACT10 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4ACT10 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SNx4ACT10 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4ACT10 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

9.2.3 Application Curves

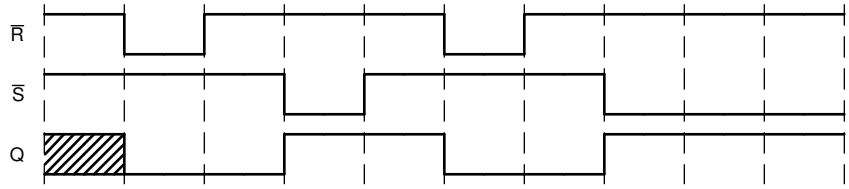

Figure 9-2. Application timing diagram

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9.2.4 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.2.5 Layout

9.2.5.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

9.2.5.2 Layout Example

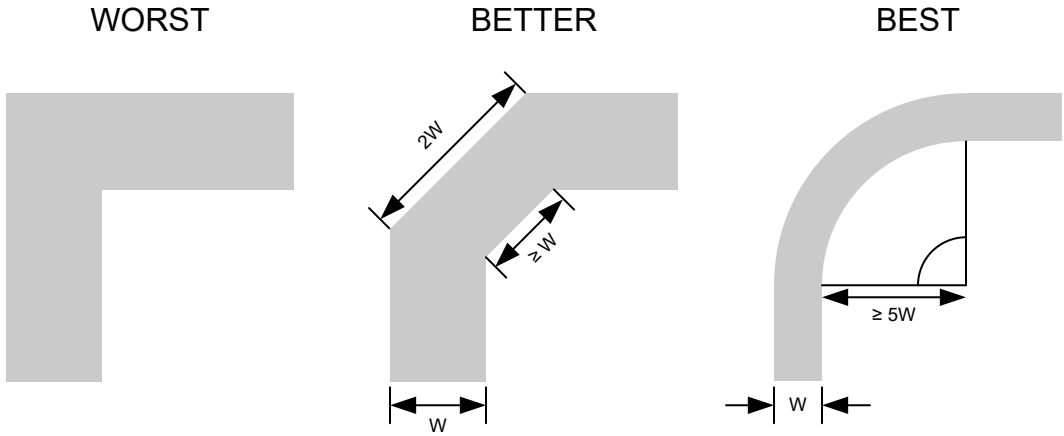

Figure 9-3. Example Trace Corners for Improved Signal Integrity

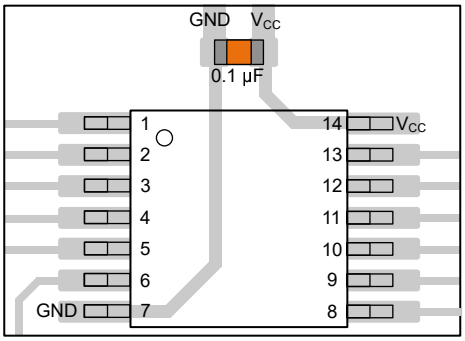

Figure 9-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

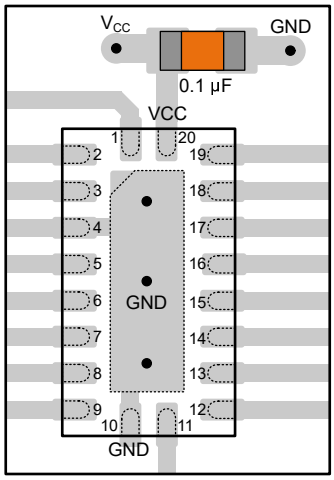

Figure 9-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

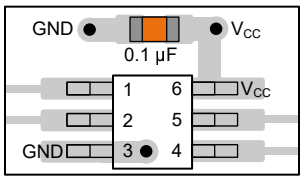

Figure 9-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

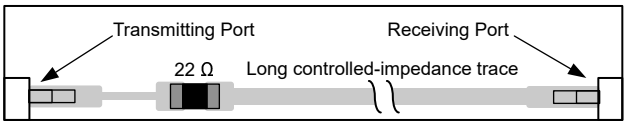

Figure 9-7. Example Damping Resistor Placement for Improved Signal Integrity

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2024) to Revision E (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added BQA package to *Device Information*	1
• Added BQA package to *Thermal Information*	5

Changes from Revision C (October 2003) to Revision D (July 2024)	Page
• Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

• Updated RθJA values: PW = 113 to 145.7, all values in °C/W.....5

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9218201M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201M2A SNJ54ACT 10FK
5962-9218201MCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201MCA SNJ54ACT10J
5962-9218201MDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201MDA SNJ54ACT10W
SN74ACT10BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD10
SN74ACT10D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	ACT10
SN74ACT10DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD10
SN74ACT10DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD10
SN74ACT10DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT10
SN74ACT10DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT10
SN74ACT10DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT10
SN74ACT10N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT10N
SN74ACT10N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74ACT10N
SN74ACT10PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	AD10
SN74ACT10PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD10
SNJ54ACT10FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201M2A SNJ54ACT 10FK
SNJ54ACT10FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201M2A SNJ54ACT 10FK
SNJ54ACT10J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201MCA SNJ54ACT10J

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ACT10J.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201MC A SNJ54ACT10J
SNJ54ACT10W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201MD A SNJ54ACT10W
SNJ54ACT10W.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9218201MD A SNJ54ACT10W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ACT10, SN74ACT10 :

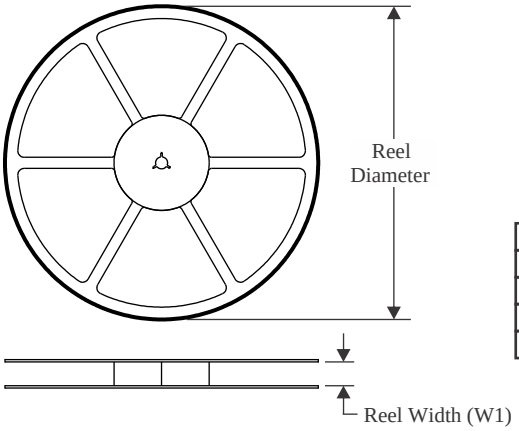
- Catalog : SN74ACT10
- Automotive : SN74ACT10-Q1, SN74ACT10-Q1
- Military : SN54ACT10

NOTE: Qualified Version Definitions:

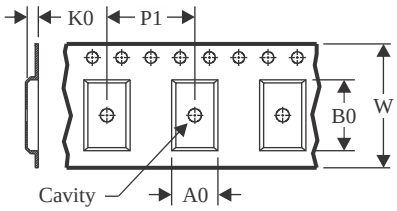
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

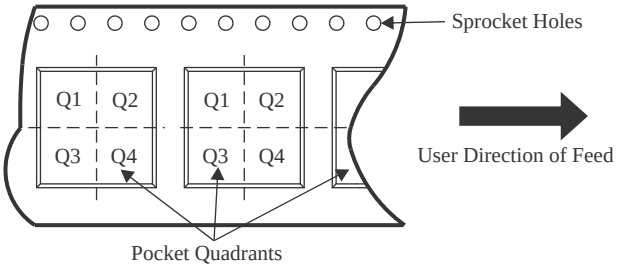


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

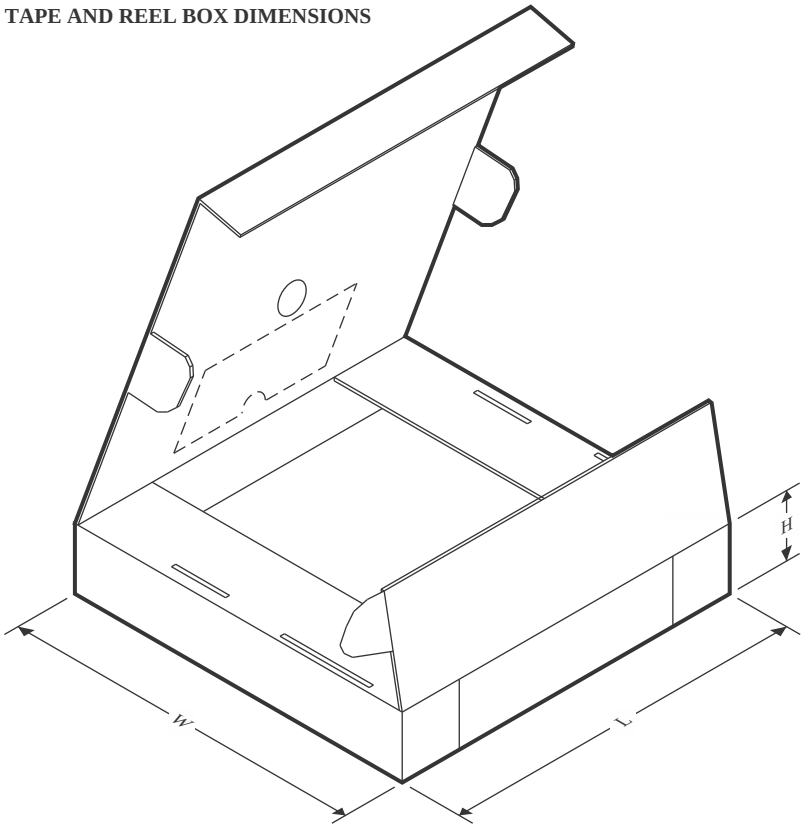
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT10BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74ACT10DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT10DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT10PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT10PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

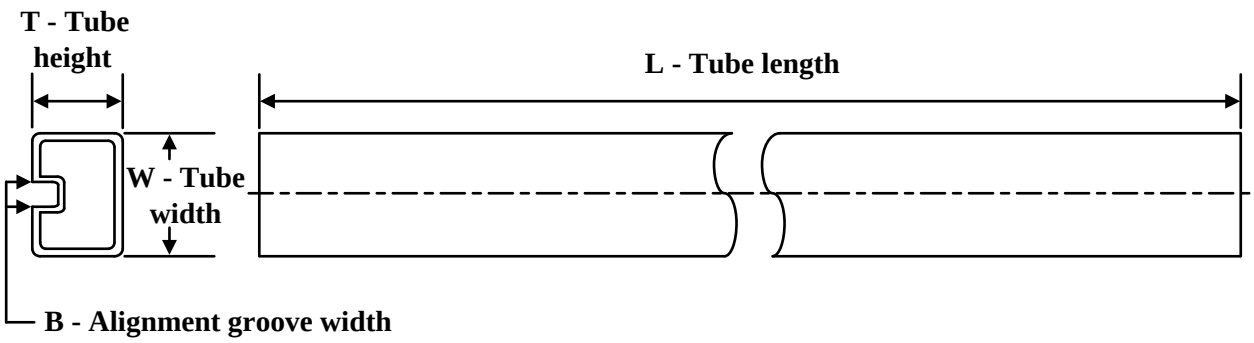
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

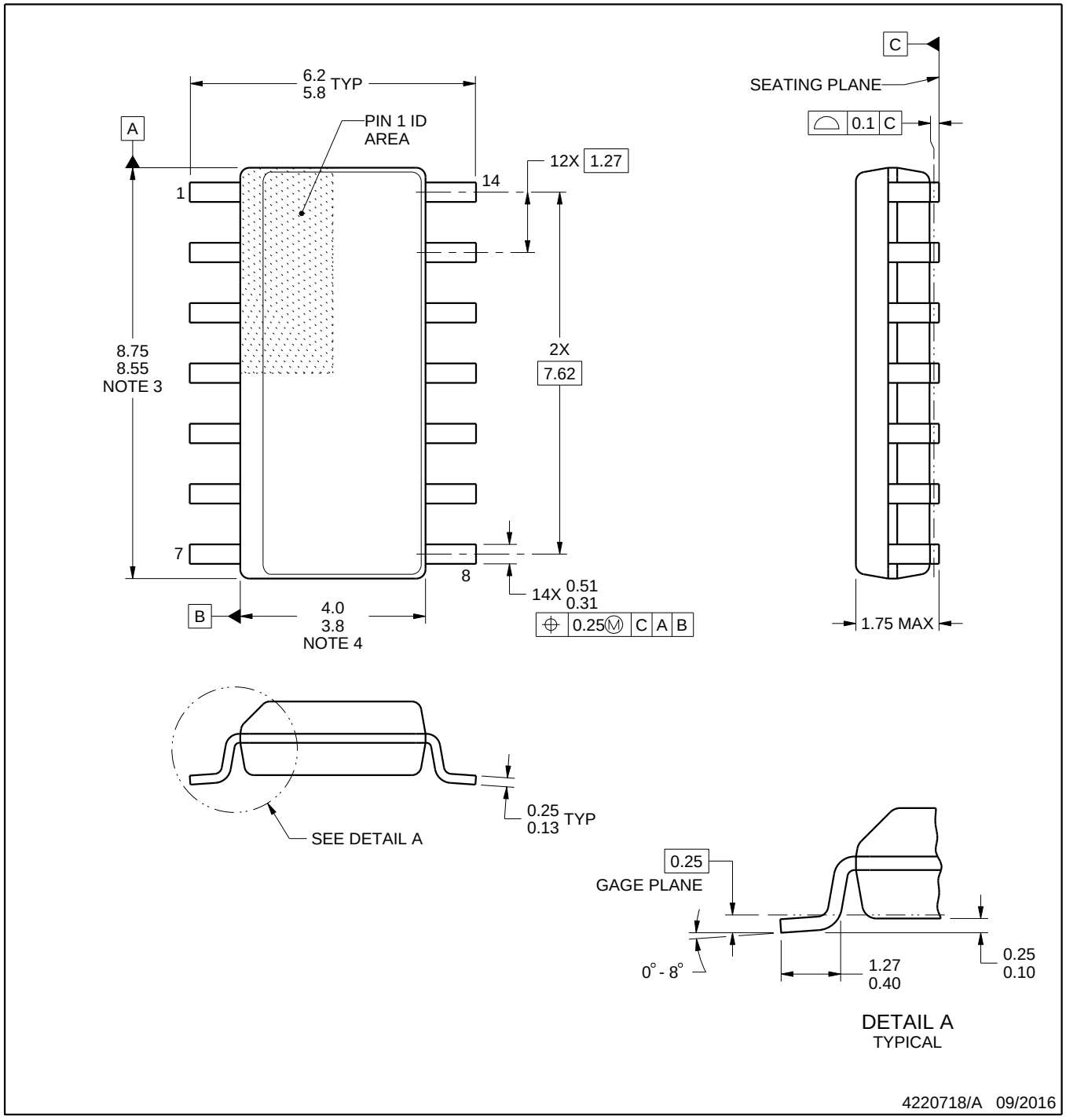
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT10BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74ACT10DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74ACT10DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74ACT10PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74ACT10PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



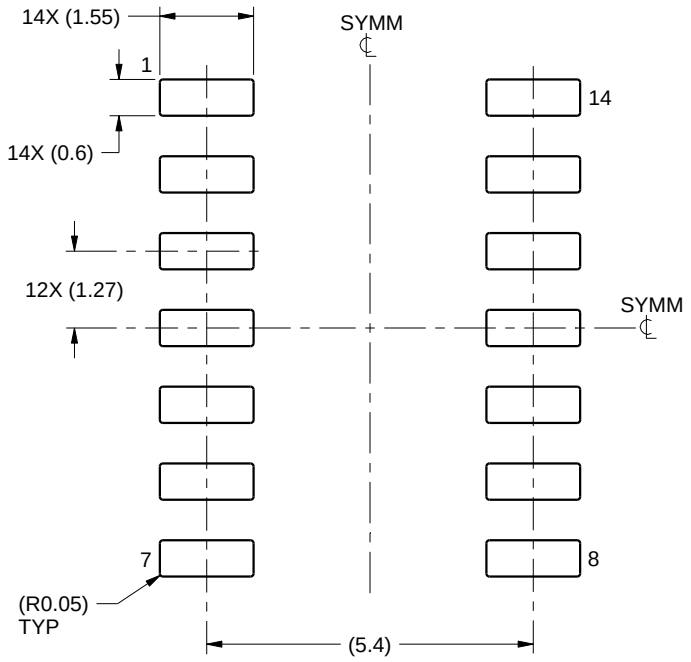
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9218201M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9218201MDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ACT10N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT10N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT10N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT10N.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ACT10FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT10FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT10W	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54ACT10W.A	W	CFP	14	25	506.98	26.16	6220	NA

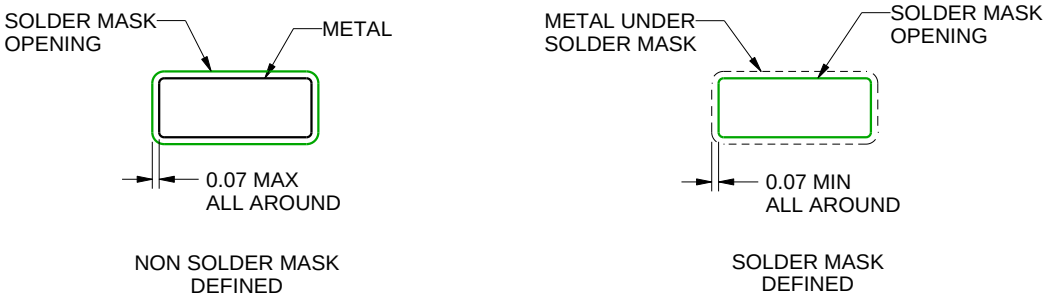


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

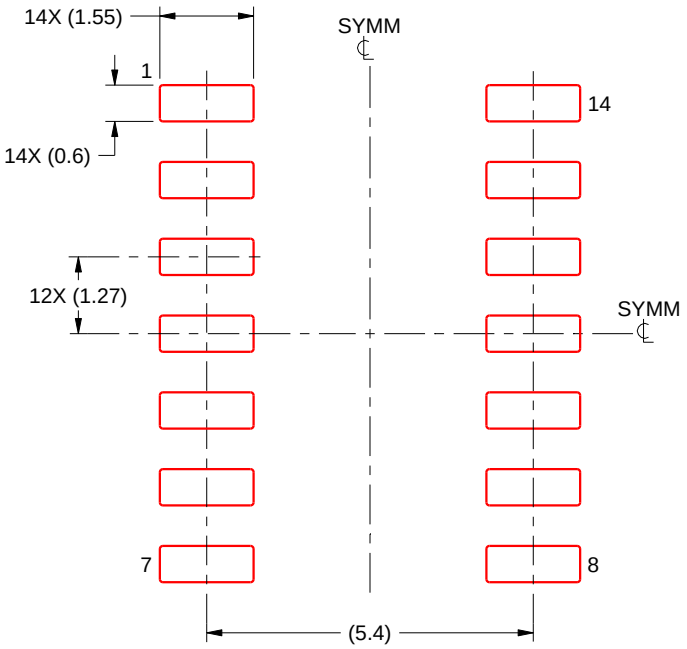


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

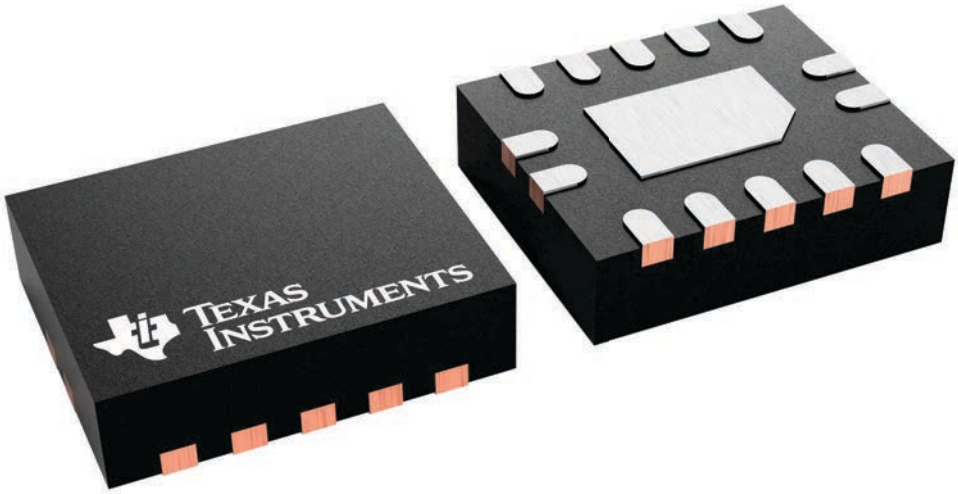
BQA 14

WQFN - 0.8 mm max height

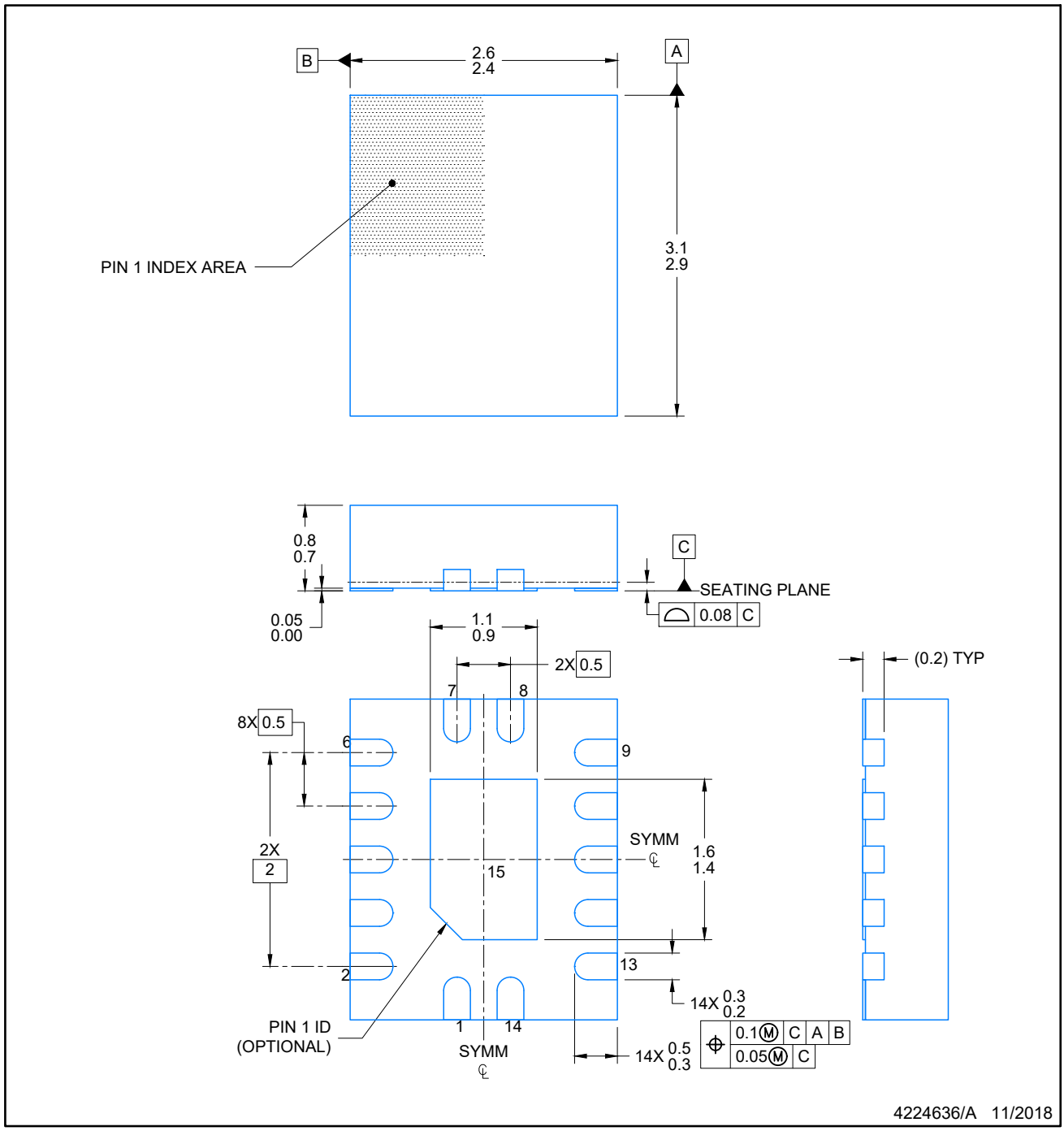
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

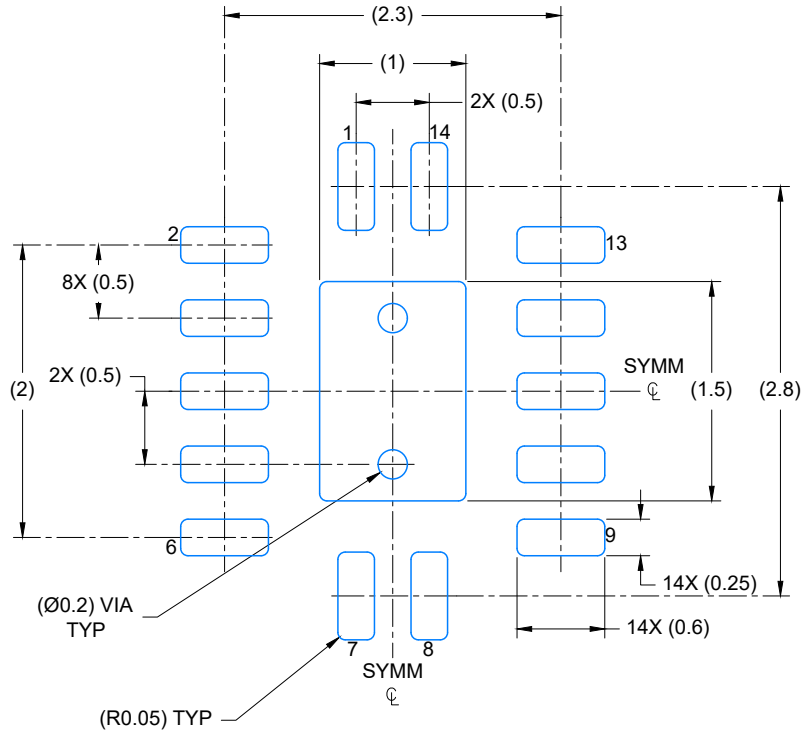


4227145/A

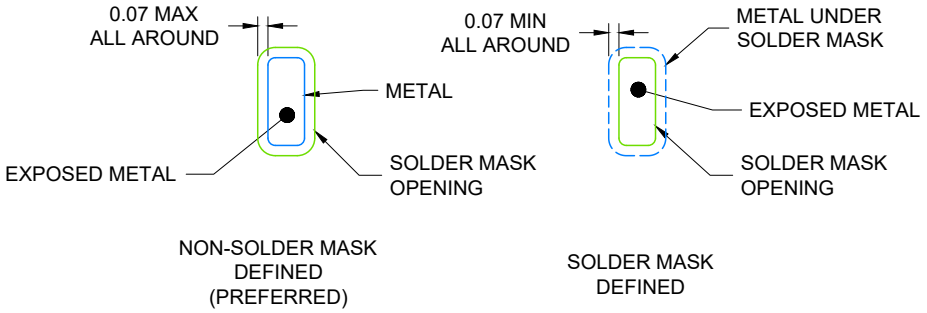


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



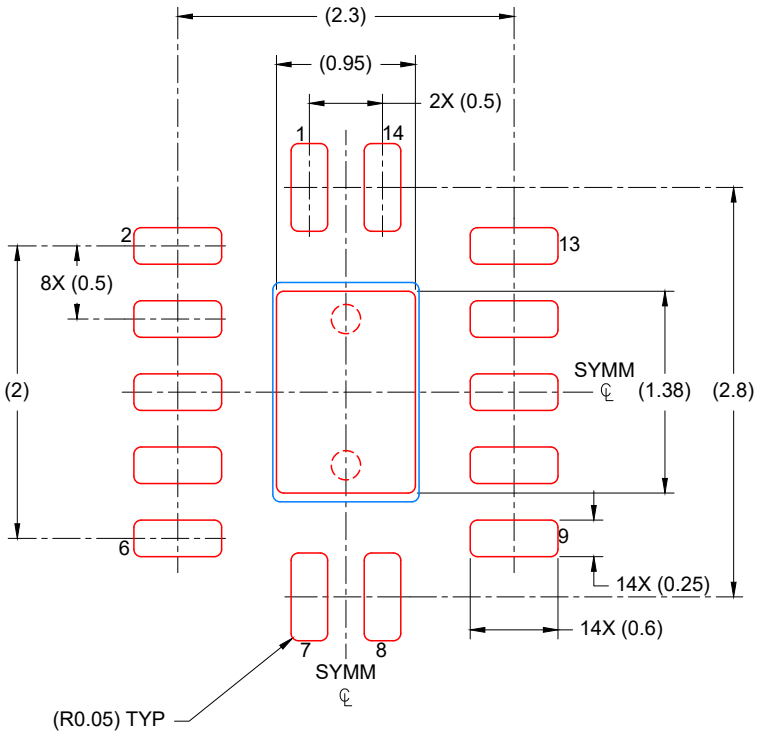
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

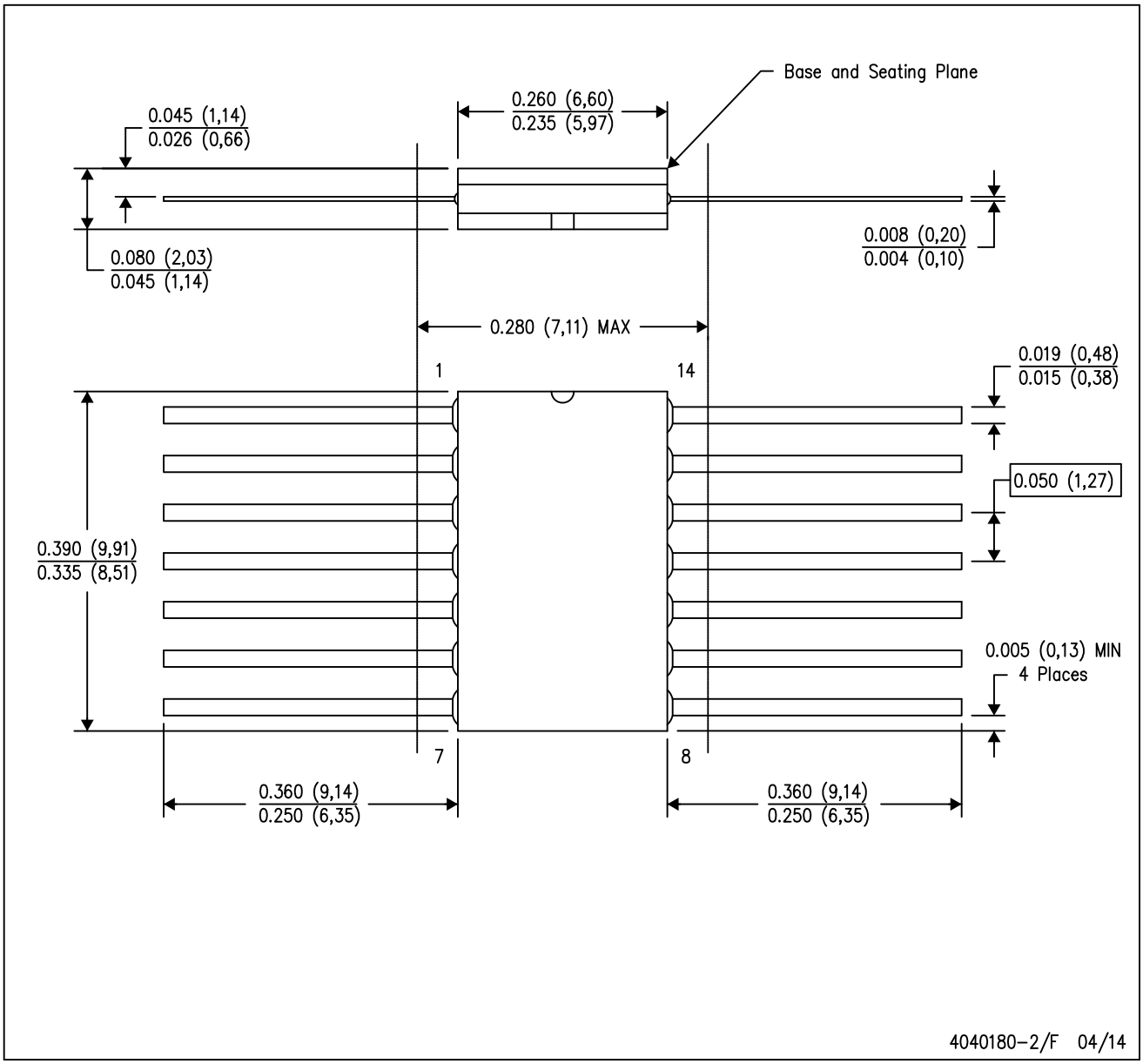
EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

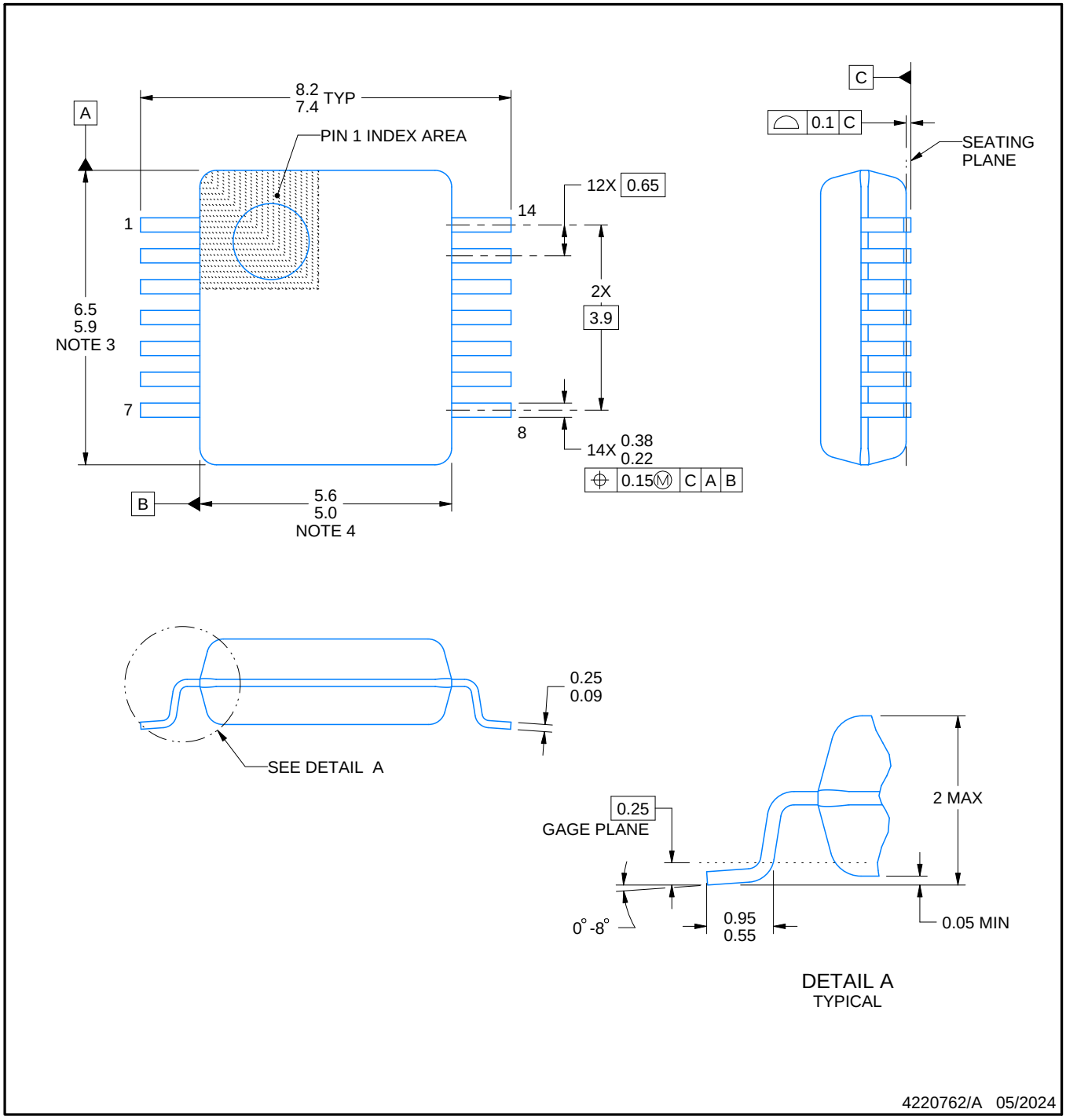
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

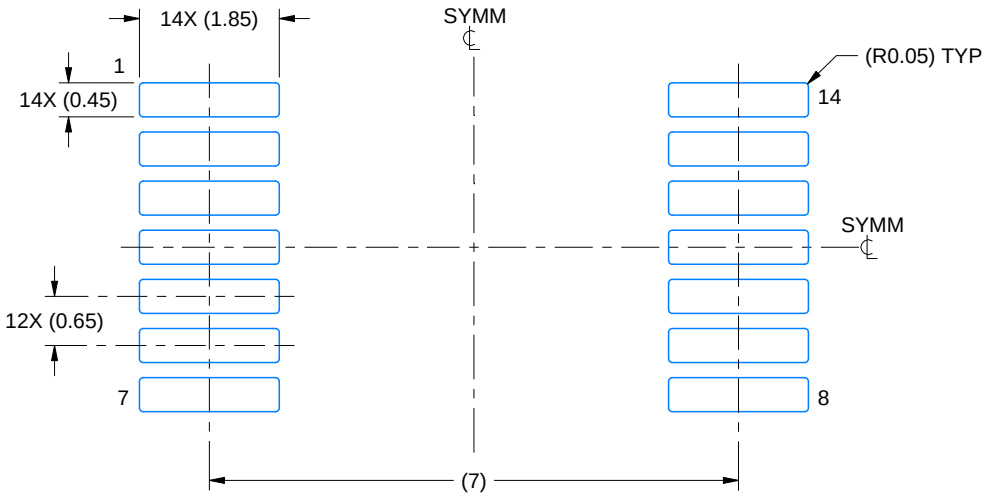


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

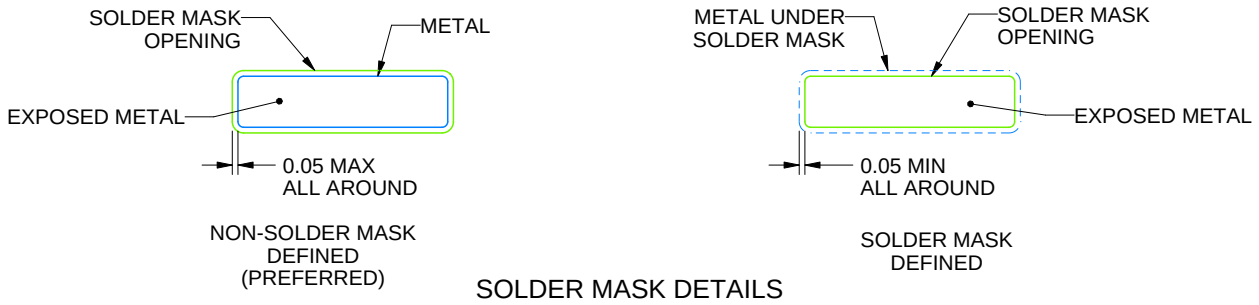


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

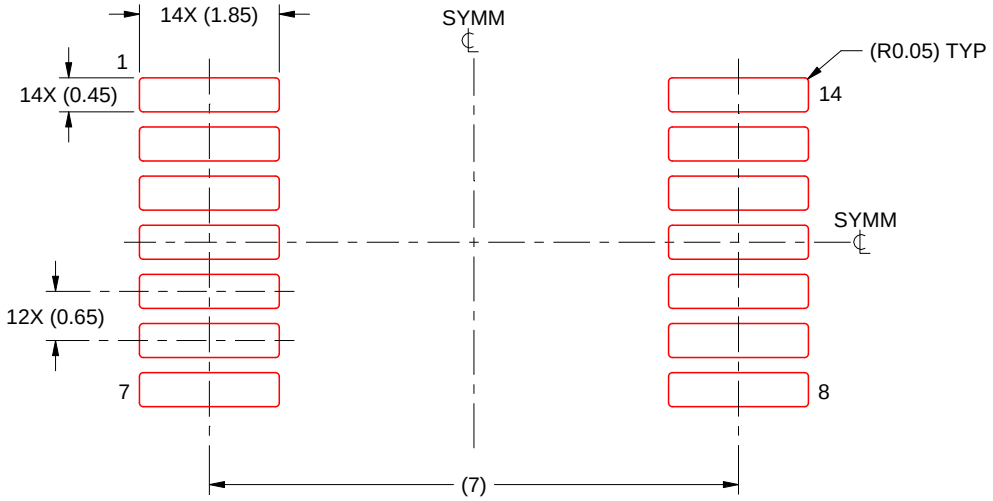


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

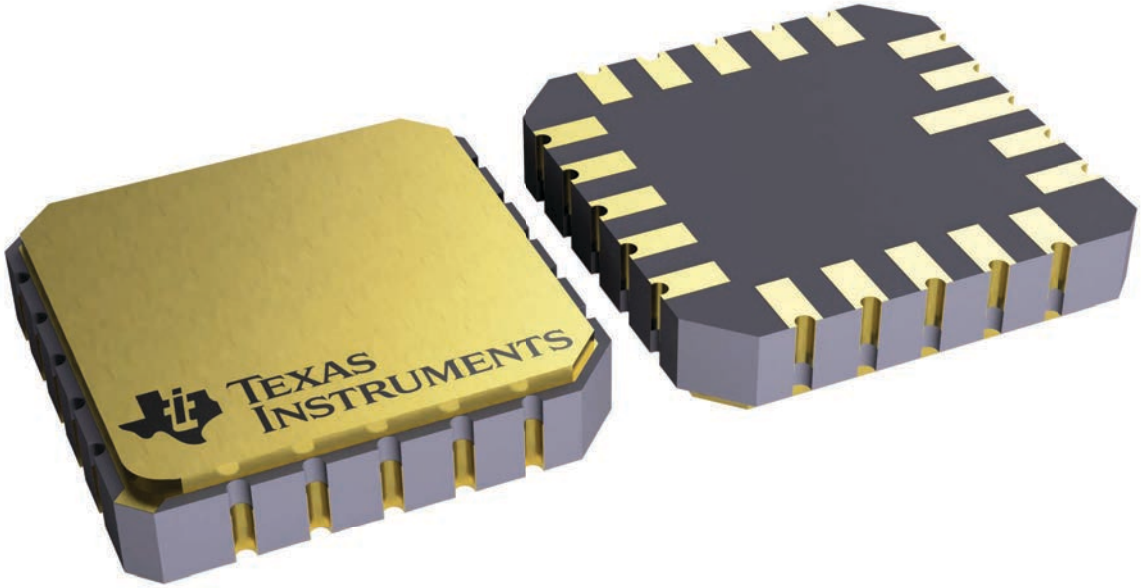
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

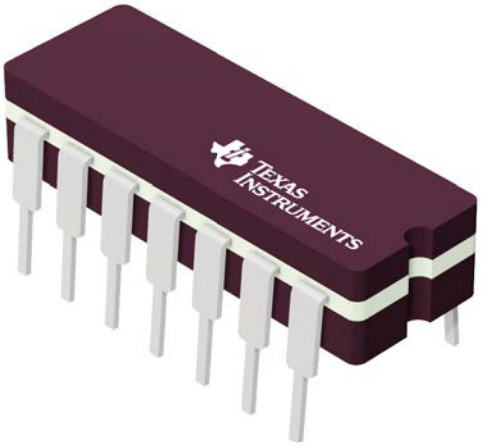
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

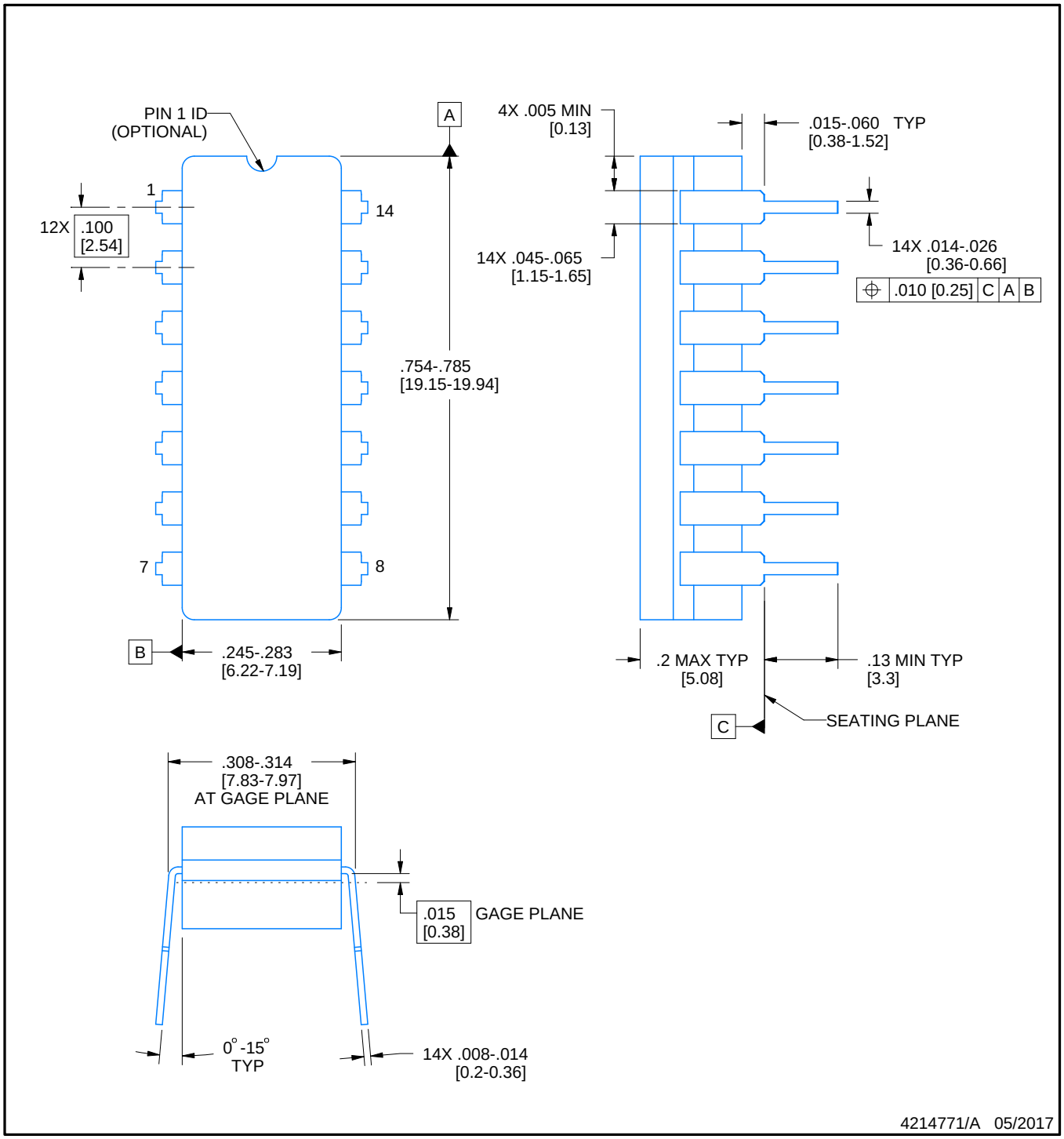
4040083-5/G

PACKAGE OUTLINE

J0014A

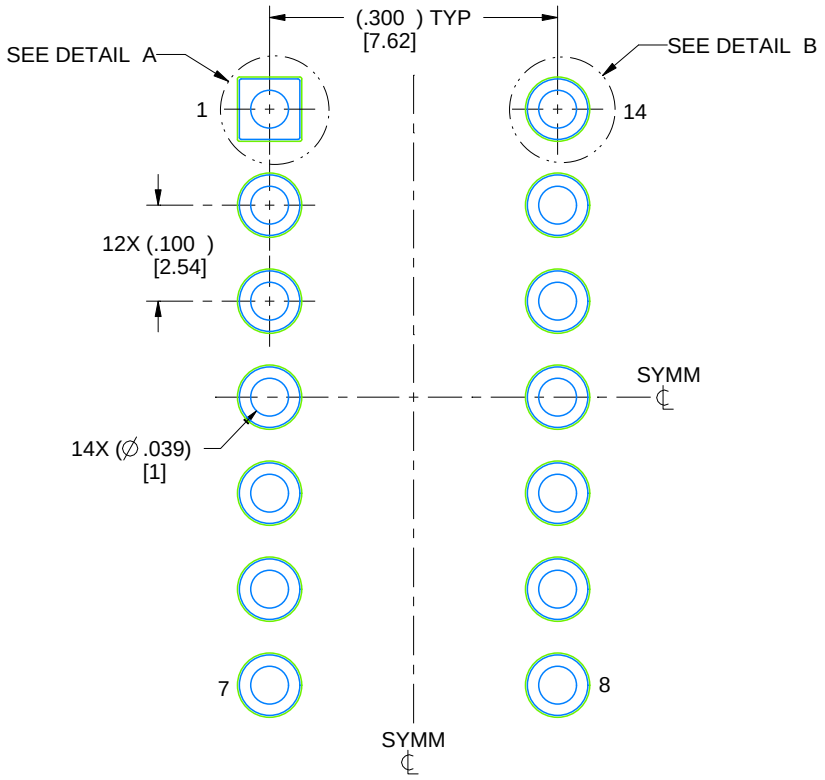
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

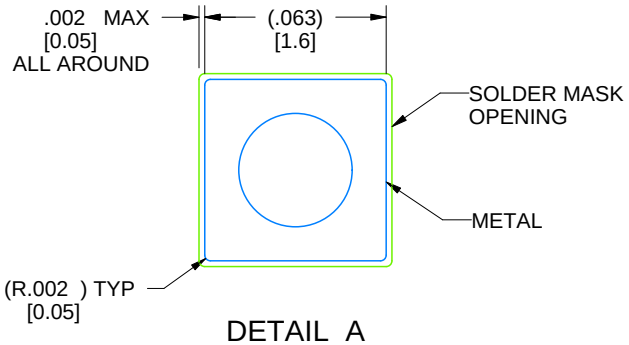


NOTES:

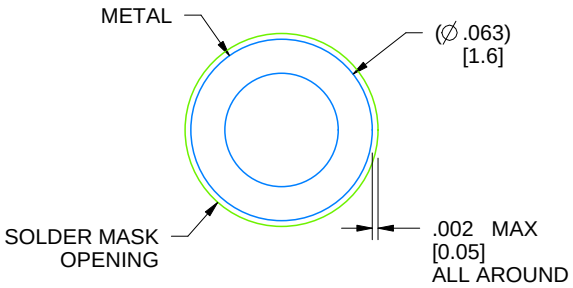
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X

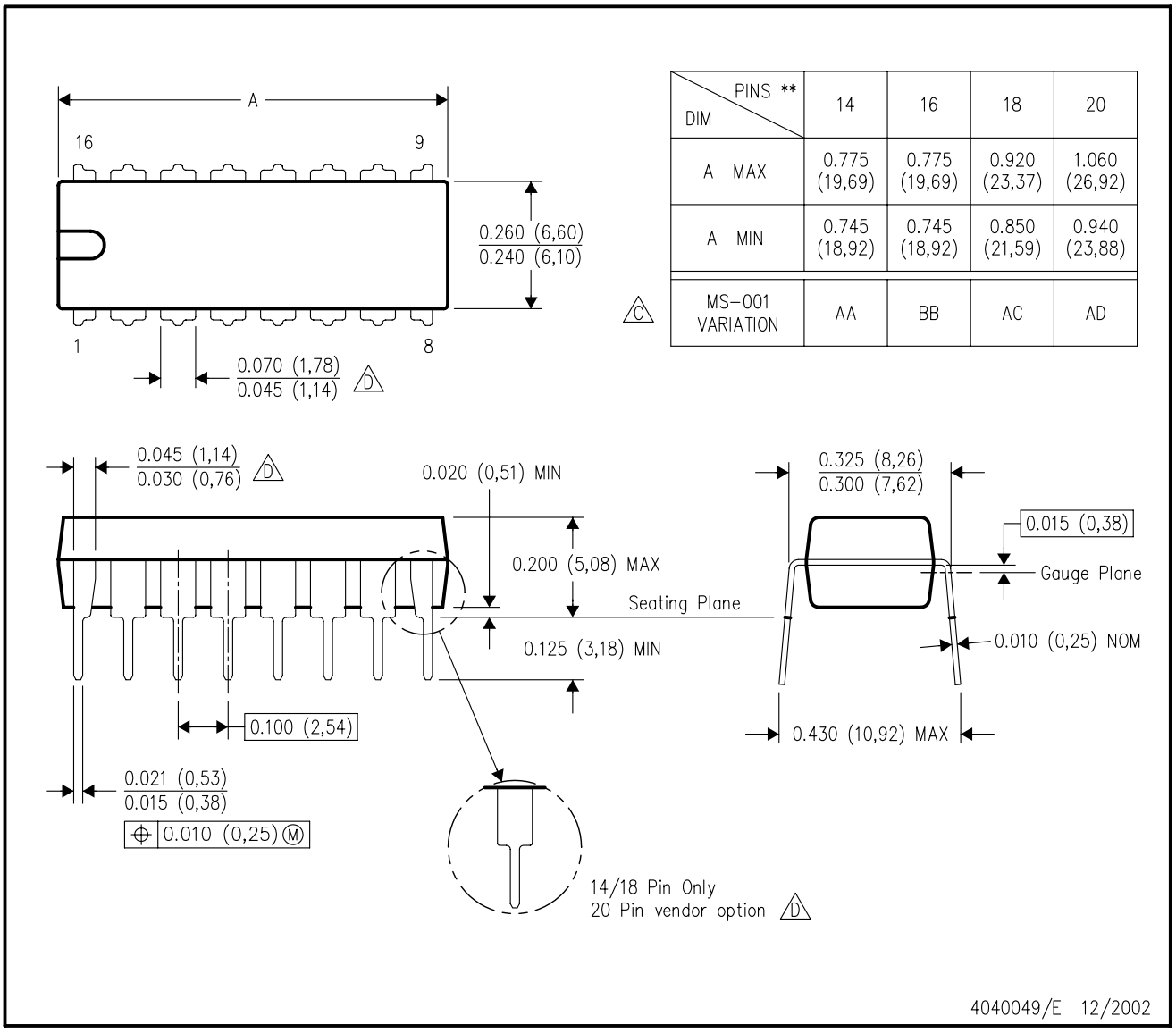


DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

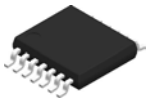
16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

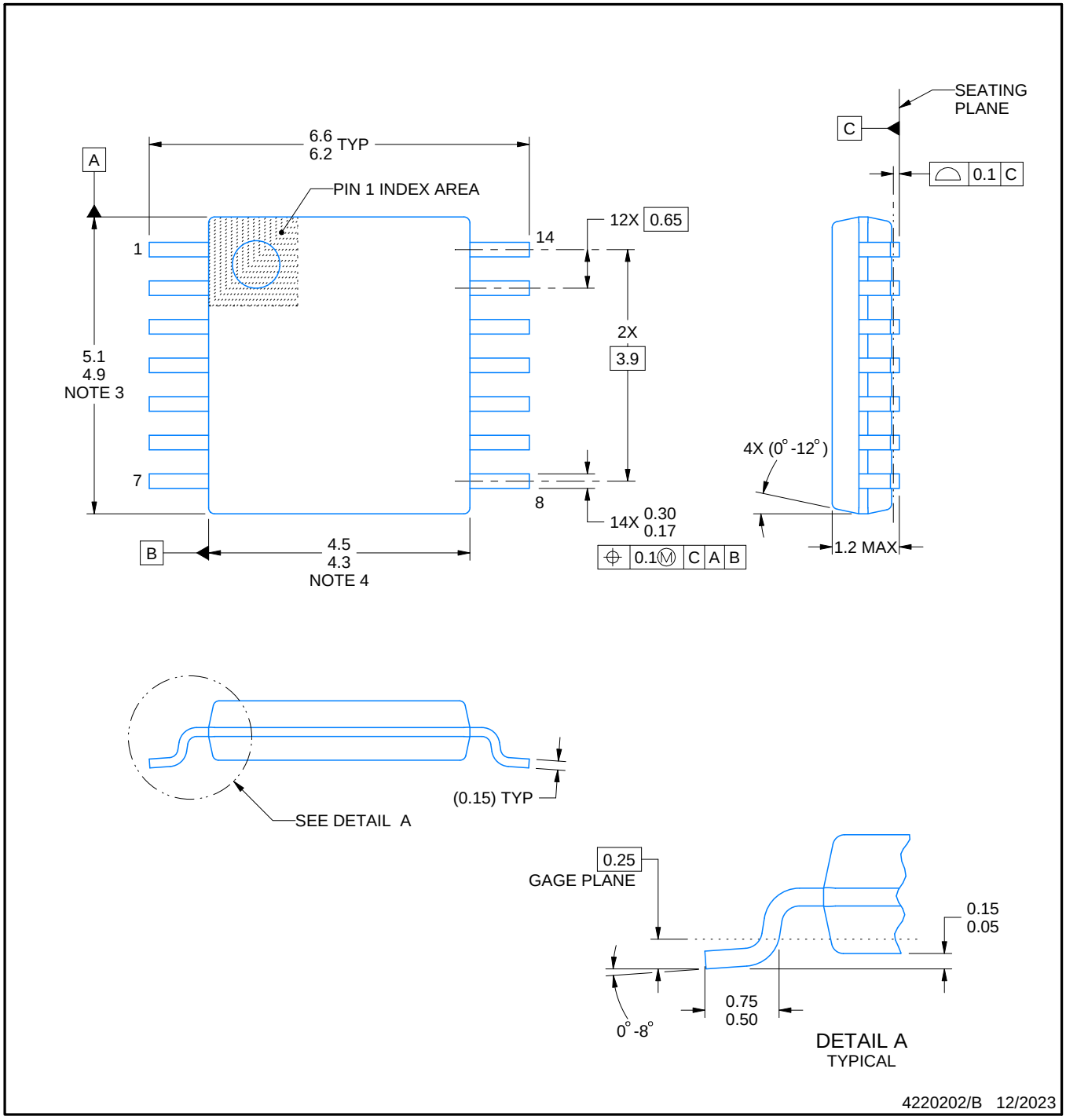
PW0014A



PACKAGE OUTLINE

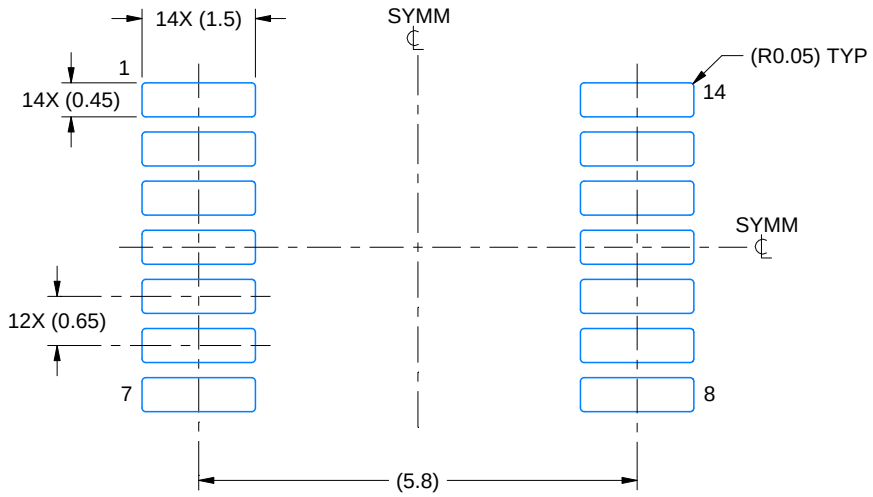
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

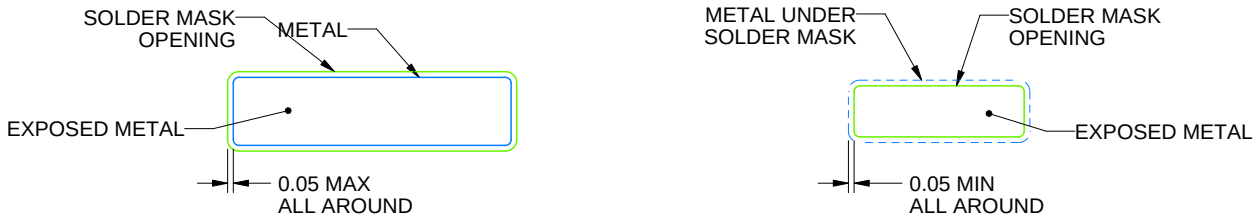


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

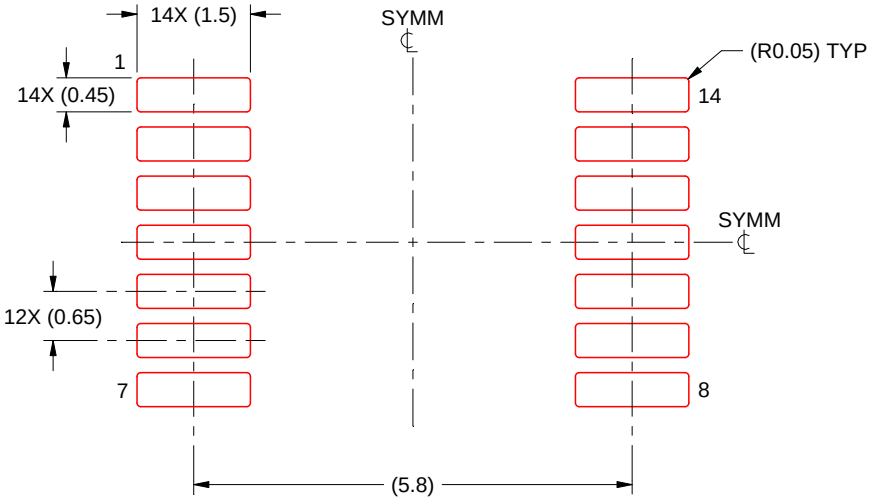
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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