

# SN54ABT823, SN74ABT823 9-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS158E – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art **EPIC-IIB™** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Buffered Control Inputs to Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (NT) and Ceramic (JT) DIPs

## description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

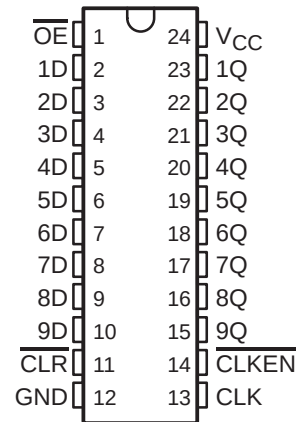
With the clock-enable ( $\overline{\text{CLKEN}}$ ) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking  $\overline{\text{CLKEN}}$  high disables the clock buffer, thus latching the outputs. Taking the clear ( $\overline{\text{CLR}}$ ) input low causes the nine Q outputs to go low, independently of the clock.

A buffered output-enable ( $\overline{\text{OE}}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

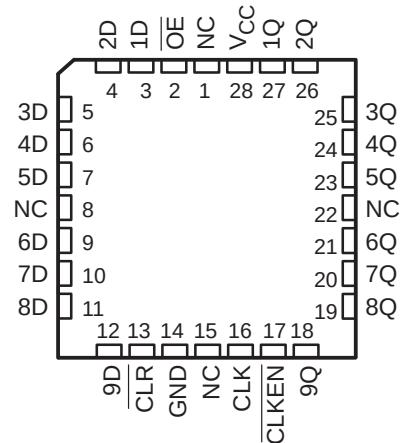
When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT823 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT823 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT823 . . . JT OR W PACKAGE  
SN74ABT823 . . . DB, DW, OR NT PACKAGE  
(TOP VIEW)



SN54ABT823 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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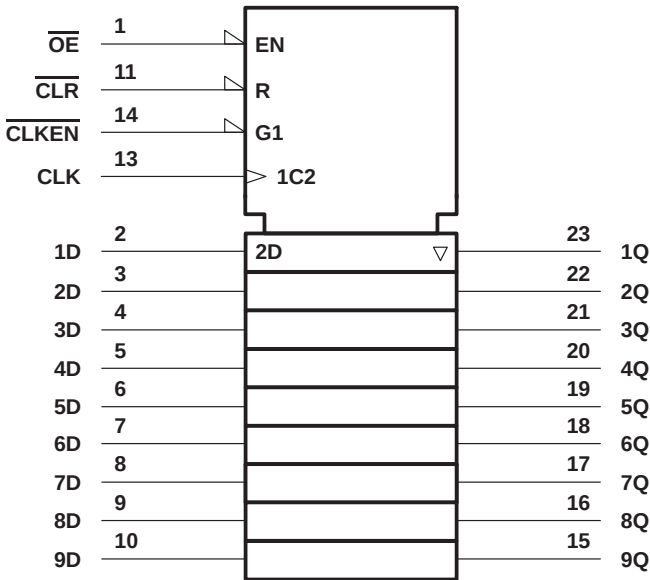
SN54ABT823, SN74ABT823  
9-BIT BUS-INTERFACE FLIP-FLOPS  
WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each flip-flop)

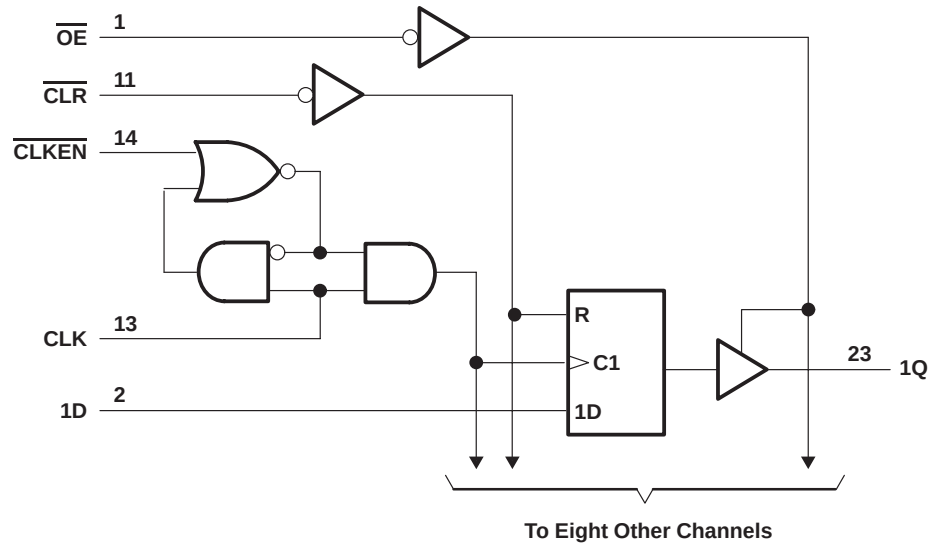
| INPUTS |     |       |     |   | OUTPUT<br>Q    |
|--------|-----|-------|-----|---|----------------|
| OE     | CLR | CLKEN | CLK | D |                |
| L      | L   | X     | X   | X | L              |
| L      | H   | L     | ↑   | H | H              |
| L      | H   | L     | ↑   | L | L              |
| L      | H   | H     | X   | X | Q <sub>0</sub> |
| H      | X   | X     | X   | X | Z              |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DB, DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                           |                 |
|---------------------------------------------------------------------------|-----------------|
| Supply voltage range, $V_{CC}$                                            | –0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1)                                   | –0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ | –0.5 V to 5.5 V |
| Current into any output in the low state, $I_O$ : SN54ABT823              | 96 mA           |
| SN74ABT823                                                                | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                               | –18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                              | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package         | 104°C/W         |
| DW package                                                                | 81°C/W          |
| NT package                                                                | 67°C/W          |
| Storage temperature range, $T_{stg}$                                      | –65°C to 150°C  |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

# SN54ABT823, SN74ABT823

## 9-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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#### recommended operating conditions (see Note 3)

|                     |                                    | SN54ABT823 |                 | SN74ABT823 |                 | UNIT |
|---------------------|------------------------------------|------------|-----------------|------------|-----------------|------|
|                     |                                    | MIN        | MAX             | MIN        | MAX             |      |
| V <sub>CC</sub>     | Supply voltage                     | 4.5        | 5.5             | 4.5        | 5.5             | V    |
| V <sub>IH</sub>     | High-level input voltage           | 2          |                 | 2          |                 | V    |
| V <sub>IL</sub>     | Low-level input voltage            |            | 0.8             |            | 0.8             | V    |
| V <sub>I</sub>      | Input voltage                      | 0          | V <sub>CC</sub> | 0          | V <sub>CC</sub> | V    |
| I <sub>OH</sub>     | High-level output current          |            | –24             |            | –32             | mA   |
| I <sub>OL</sub>     | Low-level output current           |            | 48              |            | 64              | mA   |
| Δt/Δv               | Input transition rise or fall rate |            | 5               |            | 5               | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 | 200        |                 | 200        |                 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     | –55        | 125             | –40        | 85              | °C   |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS                                                                      | T <sub>A</sub> = 25°C    |      |                  | SN54ABT823 |                  | SN74ABT823 |                  | UNIT |
|---------------------|--------------------------------------------------------------------------------------|--------------------------|------|------------------|------------|------------------|------------|------------------|------|
|                     |                                                                                      | MIN                      | TYP† | MAX              | MIN        | MAX              | MIN        | MAX              |      |
| V <sub>IK</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = –18 mA                                     |                          |      | –1.2             |            | –1.2             |            | –1.2             | V    |
| V <sub>OH</sub>     | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = –3 mA                                     | 2.5                      |      |                  | 2.5        |                  | 2.5        |                  | V    |
|                     | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = –3 mA                                       | 3                        |      |                  | 3          |                  | 3          |                  |      |
|                     | V <sub>CC</sub> = 4.5 V                                                              | I <sub>OH</sub> = –24 mA | 2    |                  | 2          |                  |            |                  |      |
|                     |                                                                                      | I <sub>OH</sub> = –32 mA | 2*   |                  |            |                  | 2          |                  |      |
| V <sub>OL</sub>     | V <sub>CC</sub> = 4.5 V                                                              | I <sub>OL</sub> = 48 mA  |      | 0.55             |            | 0.55             |            |                  | V    |
|                     |                                                                                      | I <sub>OL</sub> = 64 mA  |      | 0.55*            |            |                  |            | 0.55             |      |
| V <sub>hys</sub>    |                                                                                      |                          | 100  |                  |            |                  |            |                  | mV   |
| I <sub>I</sub>      | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND                     |                          |      | ±1               |            | ±1               |            | ±1               | μA   |
| I <sub>OZPU</sub> ‡ | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                          |      | ±50              |            | ±50              |            | ±50              | μA   |
| I <sub>OZPD</sub> ‡ | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$   |                          |      | ±50              |            | ±50              |            | ±50              | μA   |
| I <sub>OZH</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V   |                          |      | 10 <sup>§</sup>  |            | 10 <sup>§</sup>  |            | 10 <sup>§</sup>  | μA   |
| I <sub>OZL</sub>    | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V   |                          |      | –10 <sup>§</sup> |            | –10 <sup>§</sup> |            | –10 <sup>§</sup> | μA   |
| I <sub>off</sub>    | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                        |                          |      | ±100             |            |                  |            | ±100             | μA   |
| I <sub>CEX</sub>    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      |                          |      | 50               |            | 50               |            | 50               | μA   |
| I <sub>O</sub> ¶    | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      | –50                      | –140 | –180             | –50        | –180             | –50        | –180             | mA   |
| I <sub>CC</sub>     | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND | Outputs high             |      | 1                | 250        | 250              | 250        | 250              | μA   |
|                     |                                                                                      | Outputs low              |      | 24               | 38         | 38               | 38         | 38               | mA   |
|                     |                                                                                      | Outputs disabled         |      | 0.5              | 250        | 250              | 250        | 250              | μA   |
| ΔI <sub>CC</sub> #  | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |                          |      | 1.5              |            | 1.5              |            | 1.5              | mA   |
| C <sub>i</sub>      | V <sub>I</sub> = 2.5 V or 0.5 V                                                      |                          |      | 4                |            |                  |            |                  | pF   |
| C <sub>O</sub>      | V <sub>O</sub> = 2.5 V or 0.5 V                                                      |                          |      | 7                |            |                  |            |                  | pF   |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



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**9-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

|                    |                                  | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     | SN54ABT823 |     | SN74ABT823 |     | UNIT |
|--------------------|----------------------------------|-----------------------------------------------------|-----|------------|-----|------------|-----|------|
|                    |                                  | MIN                                                 | MAX | MIN        | MAX | MIN        | MAX |      |
| $f_{\text{clock}}$ | Clock frequency                  | 0                                                   | 125 | 0          | 125 | 0          | 125 | MHz  |
| $t_w$              | Pulse duration                   | CLR low                                             | 5.5 | 5.5        | 5.5 |            |     | ns   |
|                    |                                  | CLK high                                            | 2.9 | 2.9        | 2.9 |            |     |      |
|                    |                                  | CLK low                                             | 3.8 | 3.8        | 3.8 |            |     |      |
| $t_{\text{su}}$    | Setup time before CLK $\uparrow$ | CLR inactive                                        | 2.5 | 2.5        | 2.5 |            |     | ns   |
|                    |                                  | Data                                                | 2.1 | 2.1        | 2.1 |            |     |      |
|                    |                                  | CLKEN high                                          | 2   | 2          | 2   |            |     |      |
|                    |                                  | CLKEN low                                           | 3.3 | 3.3        | 3.3 |            |     |      |
| $t_h$              | Hold time after CLK $\uparrow$   | Data                                                | 1.3 | 1.3        | 1.3 |            |     | ns   |
|                    |                                  | CLKEN high                                          | 1   | 1          | 1   |            |     |      |
|                    |                                  | CLKEN low                                           | 2   | 2          | 2   |            |     |      |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER        | FROM<br>(INPUT)        | TO<br>(OUTPUT) | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     |                | SN54ABT823 |     | SN74ABT823 |                | UNIT |
|------------------|------------------------|----------------|-----------------------------------------------------|-----|----------------|------------|-----|------------|----------------|------|
|                  |                        |                | MIN                                                 | TYP | MAX            | MIN        | MAX | MIN        | MAX            |      |
| $f_{\text{max}}$ |                        |                | 125                                                 | 200 |                | 125        |     | 125        |                | MHz  |
| $t_{\text{PLH}}$ | CLK                    | Q              | 2.1                                                 | 4.3 | 5.9            | 2.1        | 8.1 | 2.1        | 6.8            | ns   |
| $t_{\text{PHL}}$ |                        |                | 2.2                                                 | 4.4 | 6.1            | 2.2        | 7   | 2.2        | 6.7            |      |
| $t_{\text{PHL}}$ | CLR                    | Q              | 2                                                   | 4.1 | 6.3            | 2          | 7.3 | 2          | 7.1            | ns   |
| $t_{\text{PZH}}$ | $\overline{\text{OE}}$ | Q              | 1                                                   | 3   | 4.7 $^\dagger$ | 1          | 6.3 | 1          | 6 $^\dagger$   | ns   |
| $t_{\text{PZL}}$ |                        |                | 2.2                                                 | 4.1 | 5.6            | 2.2        | 6.6 | 2.2        | 6.5 $^\dagger$ |      |
| $t_{\text{PHZ}}$ | $\overline{\text{OE}}$ | Q              | 2.7                                                 | 4.8 | 6.5 $^\dagger$ | 2.7        | 7.7 | 2.7        | 7.5 $^\dagger$ | ns   |
| $t_{\text{PLZ}}$ |                        |                | 1.9                                                 | 5   | 6.4            | 1.9        | 7.4 | 1.9        | 6.9            |      |

$^\dagger$  This data sheet limit may vary among suppliers.

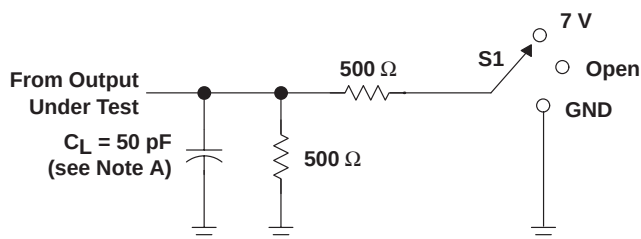
# SN54ABT823, SN74ABT823

## 9-BIT BUS-INTERFACE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

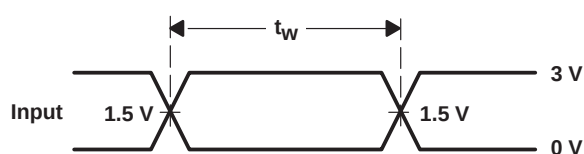
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#### PARAMETER MEASUREMENT INFORMATION

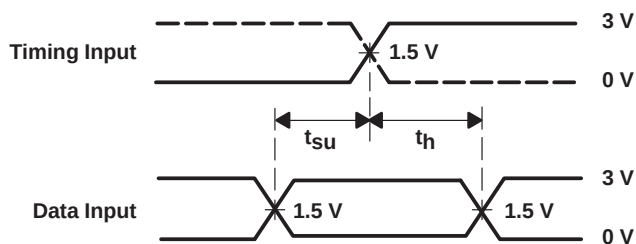


LOAD CIRCUIT

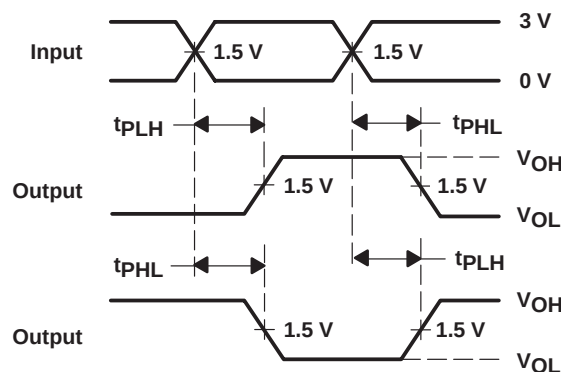
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



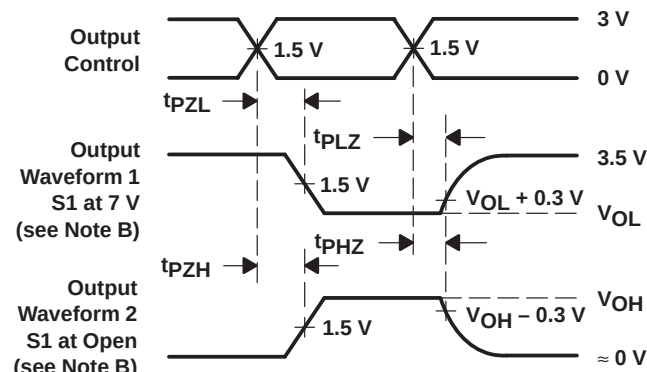
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                      |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------------|
| <a href="#">5962-9450801Q3A</a> | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9450801Q3A<br>SNJ54<br>ABT823FK |
| <a href="#">SN74ABT823DBR</a>   | Active        | Production           | SSOP (DB)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB823                                    |
| SN74ABT823DBR.B                 | Active        | Production           | SSOP (DB)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB823                                    |
| SN74ABT823DBRG4                 | Active        | Production           | SSOP (DB)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB823                                    |
| SN74ABT823DBRG4.B               | Active        | Production           | SSOP (DB)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AB823                                    |
| <a href="#">SN74ABT823DW</a>    | Active        | Production           | SOIC (DW)   24 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT823                                   |
| SN74ABT823DW.B                  | Active        | Production           | SOIC (DW)   24 | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT823                                   |
| <a href="#">SN74ABT823DWR</a>   | Active        | Production           | SOIC (DW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT823                                   |
| SN74ABT823DWR.B                 | Active        | Production           | SOIC (DW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ABT823                                   |
| <a href="#">SNJ54ABT823FK</a>   | Active        | Production           | LCCC (FK)   28 | 42   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9450801Q3A<br>SNJ54<br>ABT823FK |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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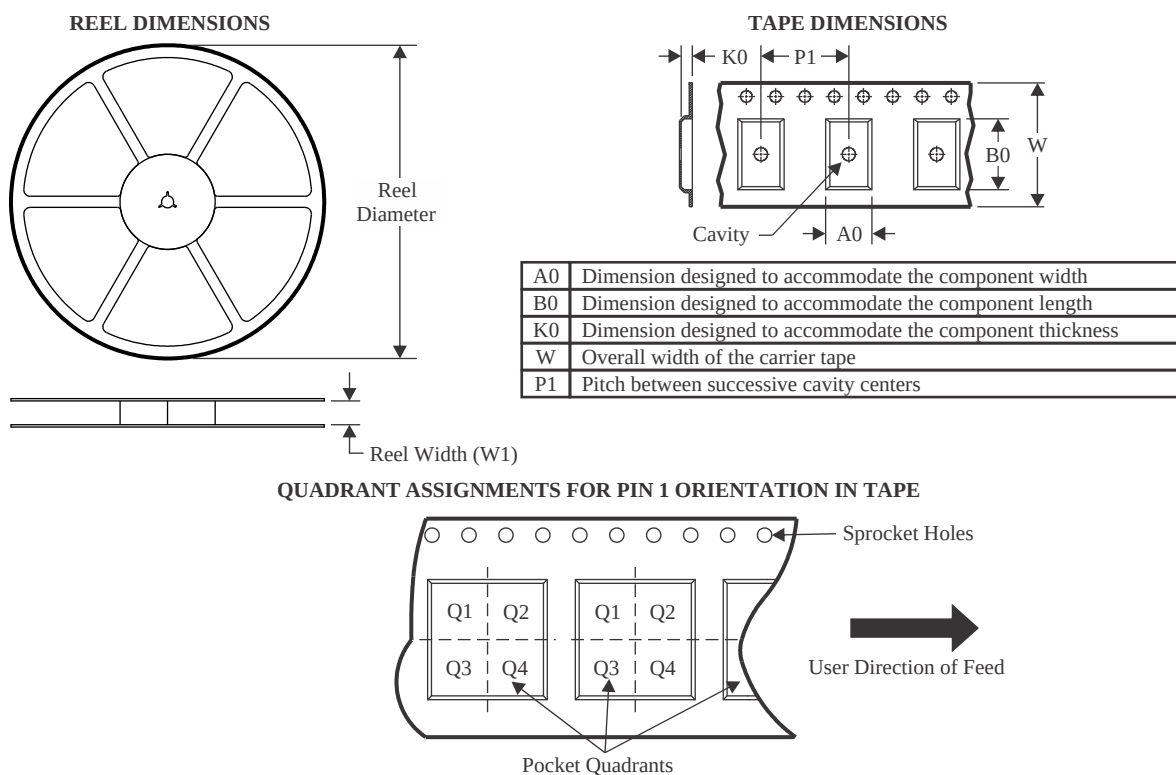
**OTHER QUALIFIED VERSIONS OF SN54ABT823, SN74ABT823 :**

- Catalog : [SN74ABT823](#)
- Military : [SN54ABT823](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

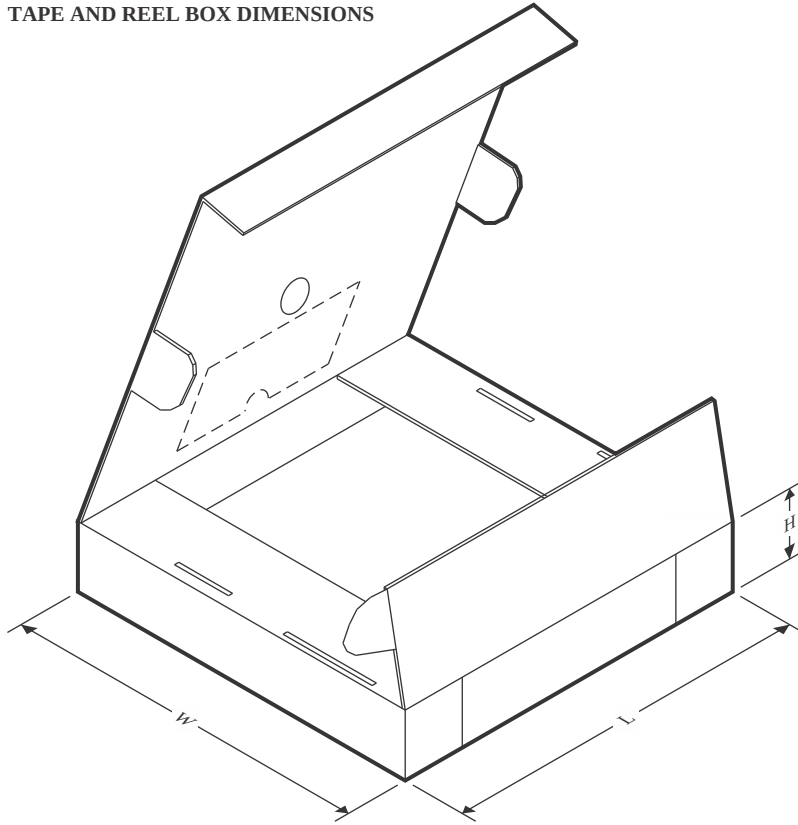
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT823DBR   | SSOP         | DB              | 24   | 2000 | 330.0              | 16.4               | 8.2     | 8.8     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT823DBRG4 | SSOP         | DB              | 24   | 2000 | 330.0              | 16.4               | 8.2     | 8.8     | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ABT823DWR   | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |

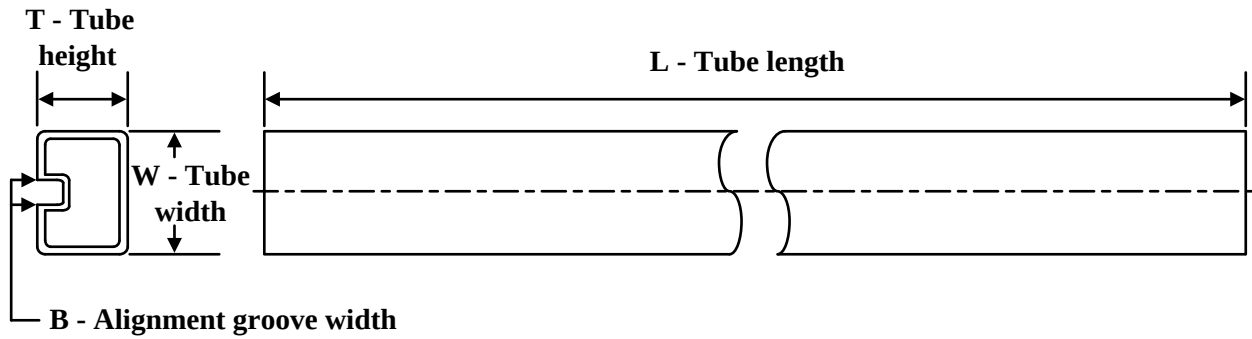
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT823DBR   | SSOP         | DB              | 24   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ABT823DBRG4 | SSOP         | DB              | 24   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ABT823DWR   | SOIC         | DW              | 24   | 2000 | 350.0       | 350.0      | 43.0        |

## TUBE



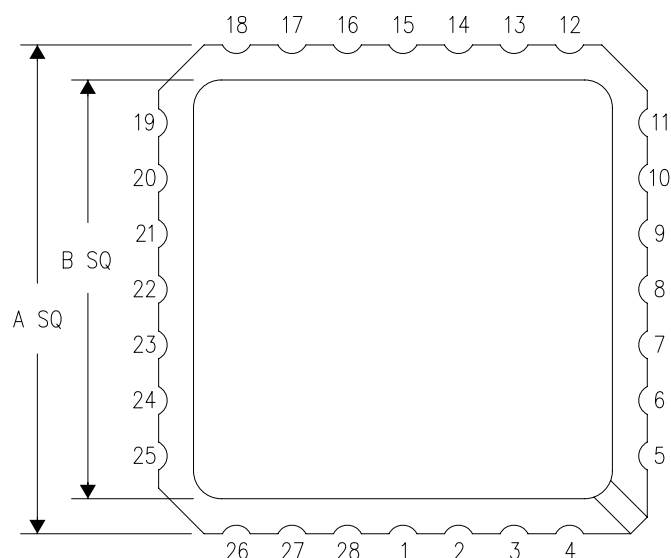
\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ABT823DW   | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN74ABT823DW.B | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |

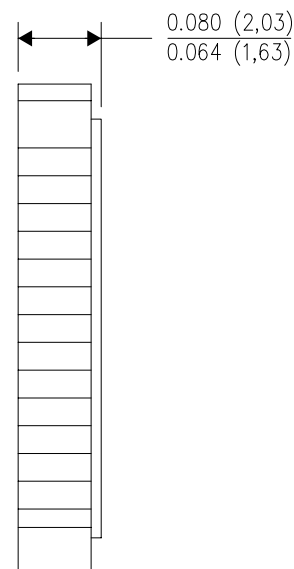
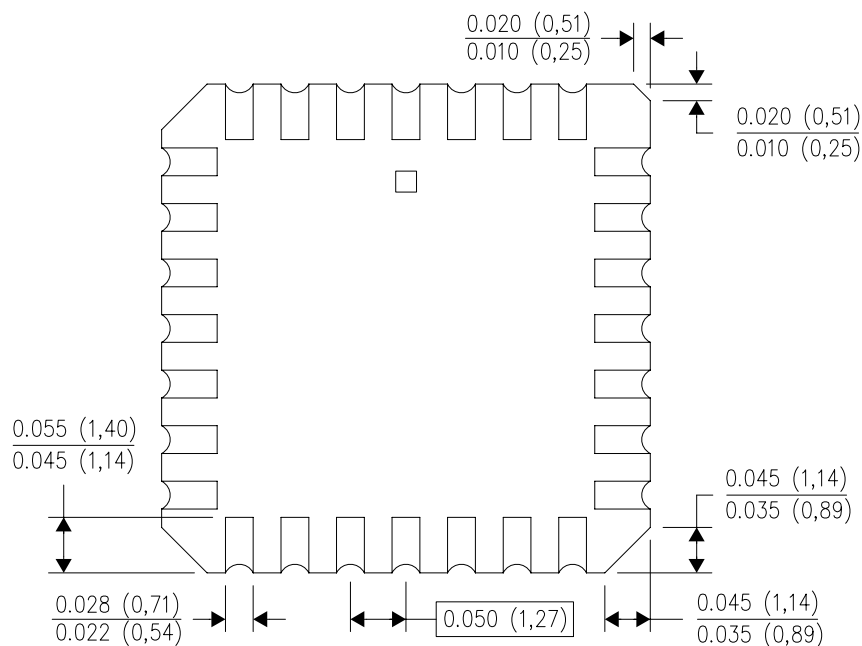
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |

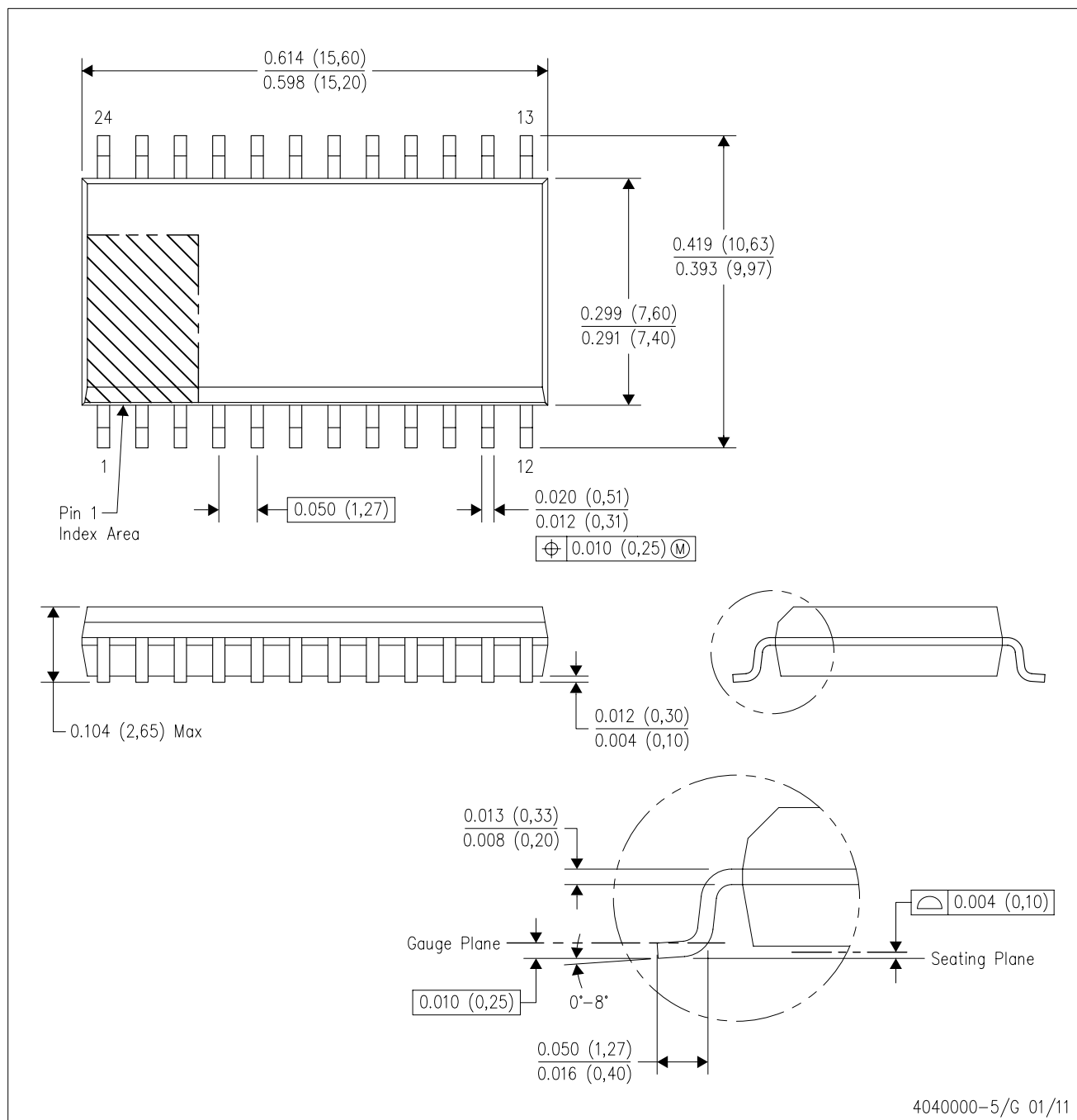


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

DW (R-PDSO-G24)

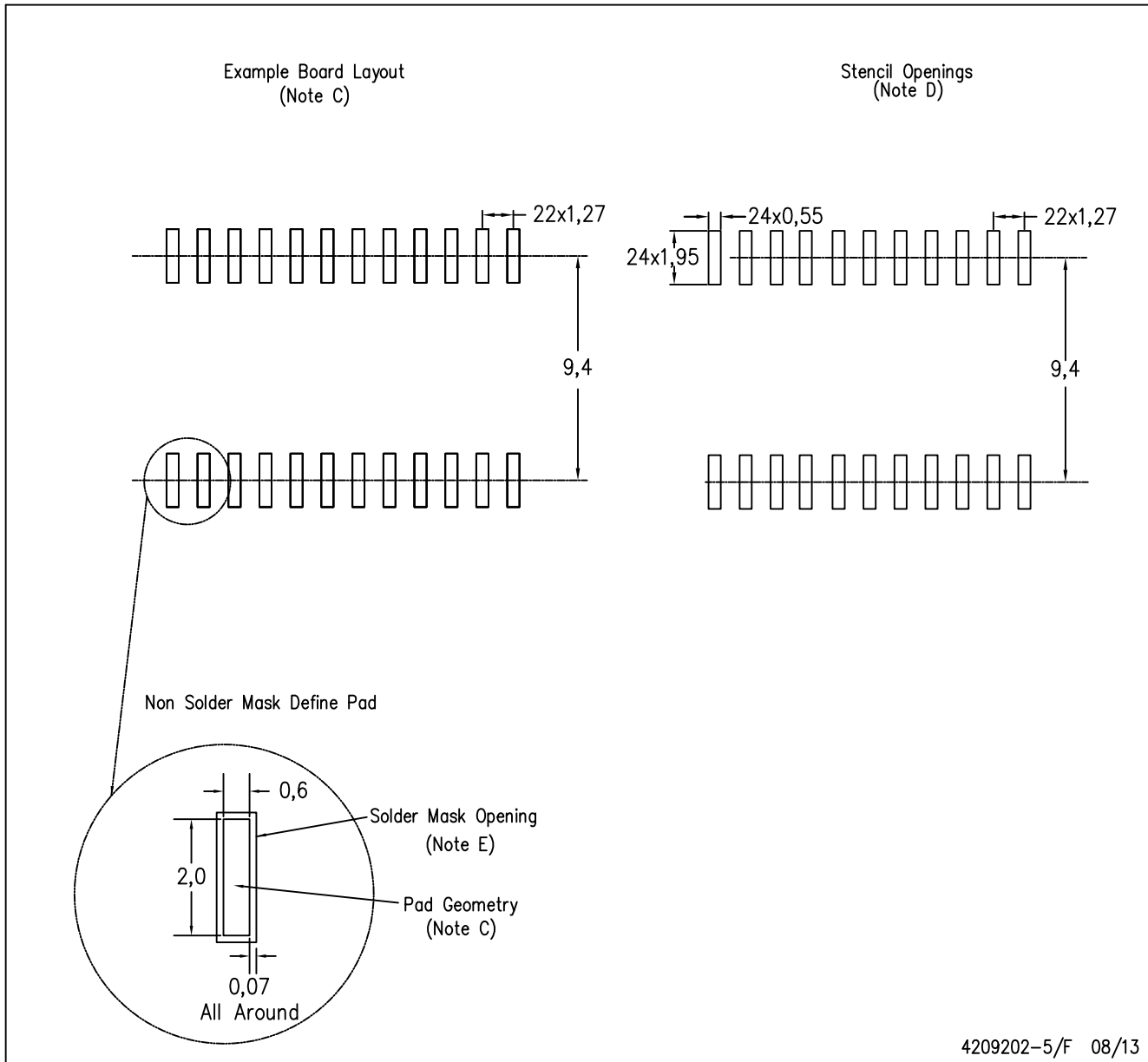
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

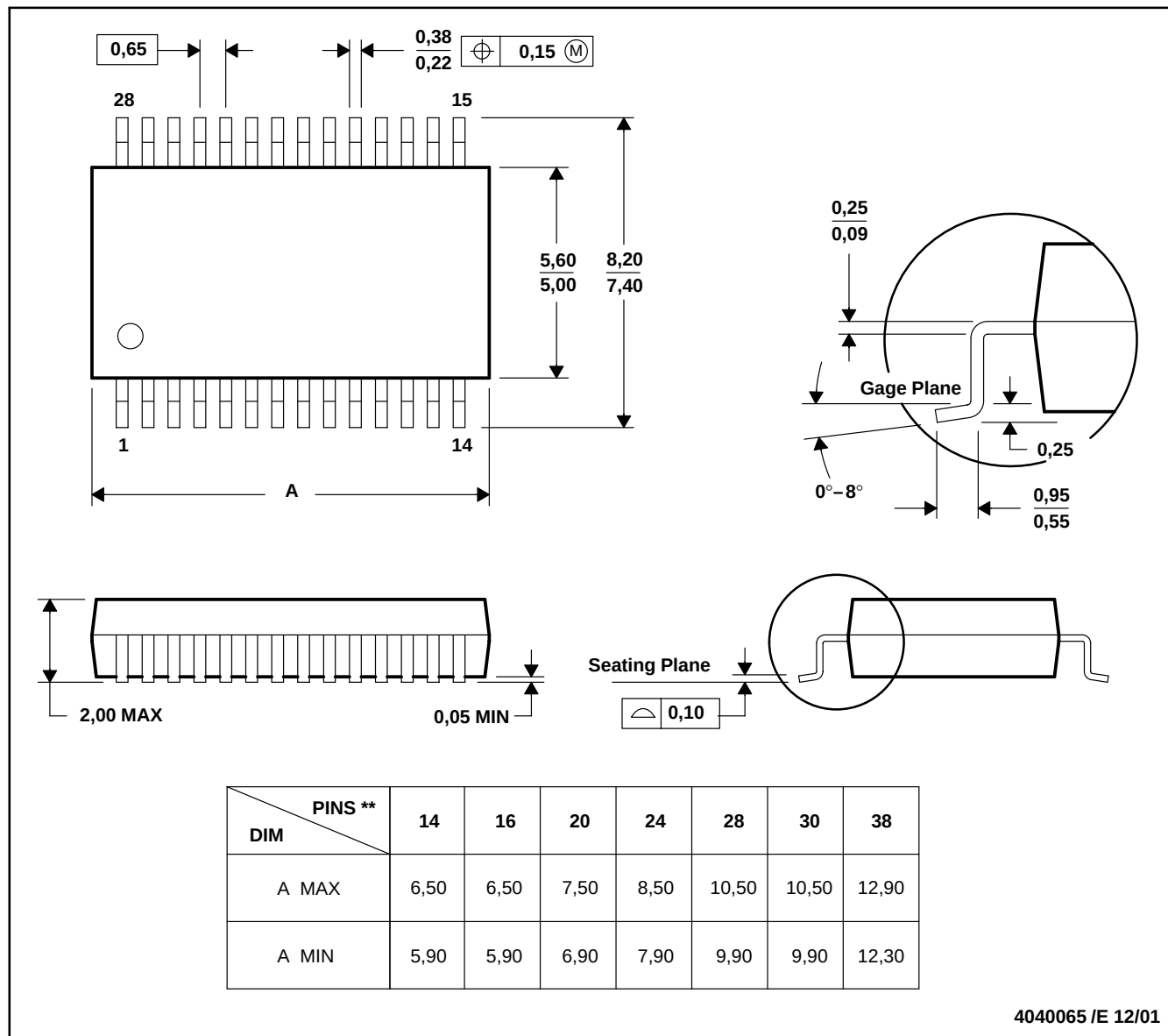


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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