CD4054B, CD4055B, CD4056B Types

CMOS Liquid-Crystal Display Drivers

High-Voltage Types (20-Volt Rating)

CD4054B – 4-Segment Display Driver
CD4055B – BCD to 7-Segment Decoder/Driver with "Display-Frequency" Output
CD4056B – BCD to 7-Segment Decoder/Driver with Strobed-Latch Function

■ CD4055B and CD4056B types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signal swings (V_{DD} to V_{SS}) may be as small as 0 to –3 V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be as large as from 0 to –15V. If V_{DD} to V_{EE} exceeds 15 V, V_{DD} to V_{SS} should be at least 4V (0 to –4V).

The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The CD4055B provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The CD4056B provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the CD4055B and CD4056B provides displays of 0 to 9 as well as L, P, H, A, –, and a blank position.

The CD4054B provides level shifting similar to the CD4055B and CD4056B independently strobed latches, and common DF control on 4 signal lines. The CD4054B is intended to provide drive-signal compatibility with the CD4055B and CD4056B 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any CD4054B output line by connecting the corresponding input and strobe lines to a low and high level, respectively and applying a square wave to DF_{IN}. The CD4054B may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0 V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to –5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus, the input and output swings can be selected independently of each other over a 3-to-18 V range. V_{SS} may be connected to V_{EE} when no level-shift function is required.

For the CD4054B and CD4056B, data are transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low.

Whenever the level-shifting function is required, the CD4055B can be used by itself to drive a liquid-crystal display (Fig.16 and Fig.20). The CD4056B, however, must be used together with a CD4054B to provide the common DF output (Fig.19). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig.18. Fig.17 is common to all three types.

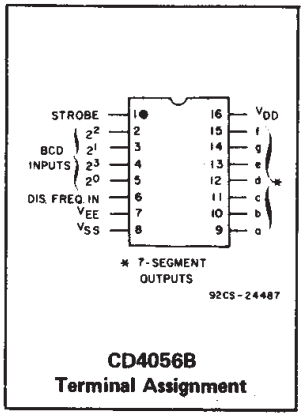
The CD4054B-, CD4055B-, and CD4056B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4054B- and CD4056B-series types also are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix).

Features:

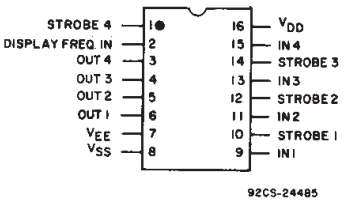
- **Operation of liquid crystals with CMOS circuits provides ultra-low-power displays**
- **Equivalent ac output drive for liquid-crystal displays – no external capacitor required**
- **Voltage doubling across display, e.g. $V_{DD} - V_{EE} = 18$ V results in effective 36 V p-p drive across selected display segments**
- **Low- or high-output level dc drive for other types of displays**
- **On-chip logic-level conversion for different input- and output-level swings**
- **Full decoding of all input combinations: 0-9, L, H, P, A,–, and blank positions**
- **Strobed-latch function—CD4054B Series and CD4056B Series**
- **DISPLAY-FREQUENCY (DF) output for liquid-crystal common-line drive signal—CD4055B Series (CD4054B Series also: see introductory text)**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (over full package temperature range):**
  1 V at $V_{DD} = 5$ V
  2 V at $V_{DD} = 10$ V
  2.5 V at $V_{DD} = 15$ V
- **5-V, 10-V, and 15-V parametric ratings**

Applications

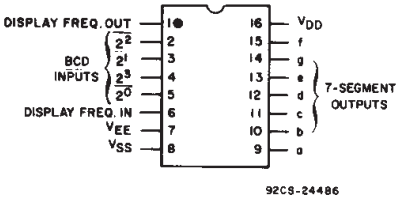
- **General-purpose displays**
- **Calculators and meters**
- **Wall and table clocks**
- **Industrial control panels**
- **Portable lab instruments**
- **Panel meters**
- **Auto dashboard displays**
- **Appliance control panels**



CD4056B Terminal Assignment



CD4054B Terminal Assignment



CD4055B Terminal Assignment

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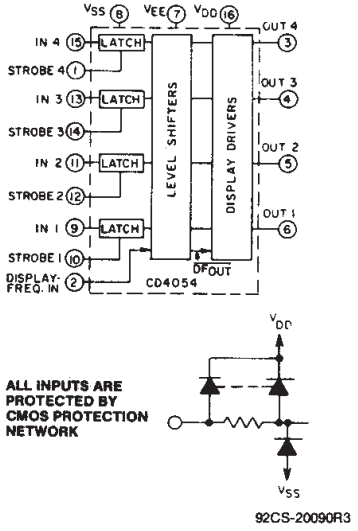


Fig.1 – CD4054B functional diagram.

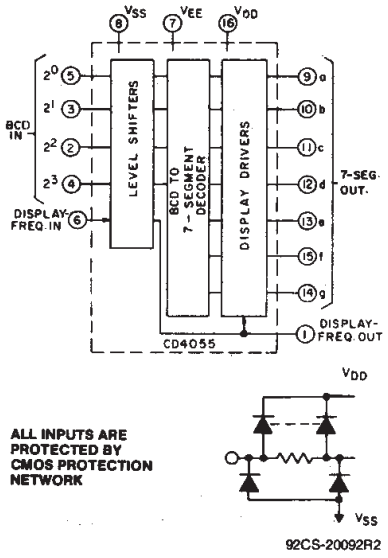


Fig.2 – CD4055B functional diagram.

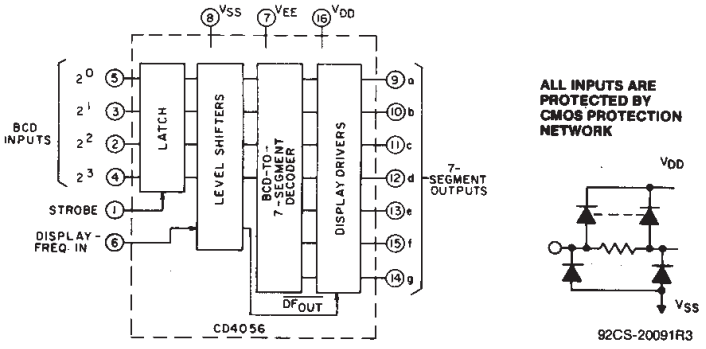


Fig.3 – CD4056B functional diagram.

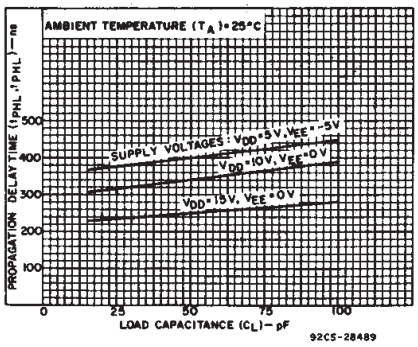


Fig.4 – Typical propagation delay time vs. load capacitance for CD4054B.

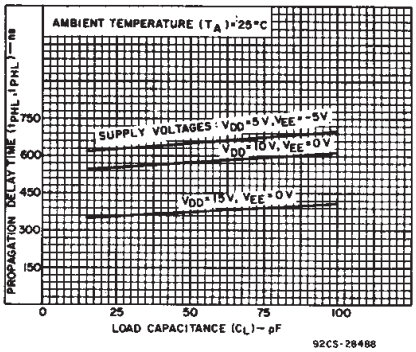


Fig.5 – Typical propagation delay time vs. load capacitance for CD4055 and CD4056B.

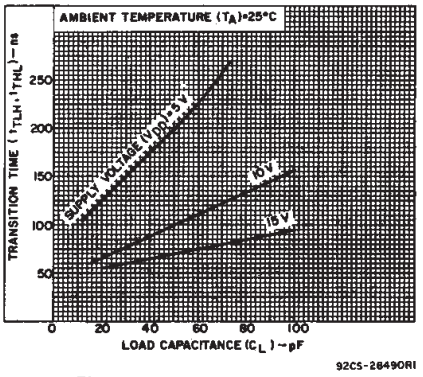


Fig.6 – Typical transition time vs. load capacitance.

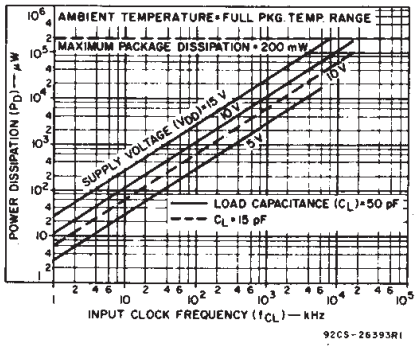


Fig.7 – Typical input clock frequency vs. power dissipation.

CD4054B TRUTH TABLE

DF	IN	ST	OUT
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0
X	X	0	*

X = Don't Care.

*Depends upon the input mode previously applied when ST = 1.

TRUTH TABLE FOR CD4055B and CD4056B

INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	
0	0	0	1	0	1	1	0	0	0	0	
0	0	1	0	1	1	0	1	1	0	1	
0	0	1	1	1	1	1	1	0	0	1	
0	1	0	0	0	1	1	0	0	1	1	
0	1	0	1	1	0	1	1	0	1	1	
0	1	1	0	1	0	1	1	1	1	1	
0	1	1	1	1	1	1	0	0	0	0	
1	0	0	0	1	1	1	1	1	1	1	
1	0	0	1	1	1	1	1	0	1	1	
1	0	1	0	0	0	0	1	1	1	0	
1	0	1	1	0	1	1	0	1	1	1	
1	1	0	0	1	1	0	0	1	1	1	
1	1	0	1	1	1	1	0	1	1	1	
1	1	1	0	0	0	0	0	0	0	1	—
1	1	1	1	0	0	0	0	0	0	0	BLANK

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55°	−40°	+85°	+125°	+25°C Min.	Typ.	Max.	Units
Quiescent Device Current, I_{DD} MAX.	-5	0			5	5		150	150	–	0.04	5	μA
	0	0			10	10		300	300	–	0.04	10	
	0	0			15	20		600	600	–	0.04	20	
	0	0			20	100		3000	3000	–	0.08	100	
Output Voltage: Low Level, V_{OL} MAX.	0	0		0,5	5	0.05				–	0	0.05	V
	0	0		0,10	10	0.05				–	0	0.05	
	0	0		0,15	15	0.05				–	0	0.05	
High Level, V_{OH} MIN.	0	0		0,5	5	4.95				4.95	5	–	
	0	0		0,10	10	9.95				9.95	10	–	
	0	0		0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} MAX.	0	0	0.5, 4.5		5	1.5				–	–	1.5	
	0	0	1,9		10	3				–	–	3	
	0	0	1.5,13.5		15	4				–	–	4	
Input High Voltage, V_{IH} MIN.	-5	0	0.5,4.5		5	3.5				3.5	–	–	
	0	0	1,9		10	7				7	–	–	
	0	0	1.5,13.5		15	11				11	–	–	
Output Low (Sink) Current, I_{OL}	-5	0	-4.5		5	0.98	0.92	0.67	0.55	0.8	1.6	–	mA
	0	0	0.5		10	0.98	0.92	0.67	0.55	0.8	1.6	–	
	0	0	1.5		15	3.6	3.4	2.4	2	2.9	5.8	–	
Output High (Source) Current, I_{OH}	-5	0	4.5		5	-0.6	-0.55	-0.35	-0.3	-0.45	-0.9	–	
	0	0	9.5		10	-0.6	-0.55	-0.35	-0.3	-0.45	-0.9	–	
	0	0	13.5		15	-1.9	-1.8	-1.2	-1.1	-1.5	-3	–	
Input Current, I_{IN}	0	0	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

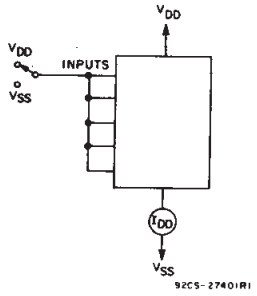


Fig. 11 – Quiescent-device-current test circuit.

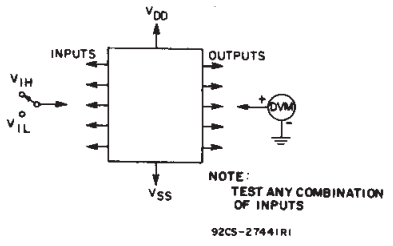


Fig. 12 – Input-voltage test circuit.

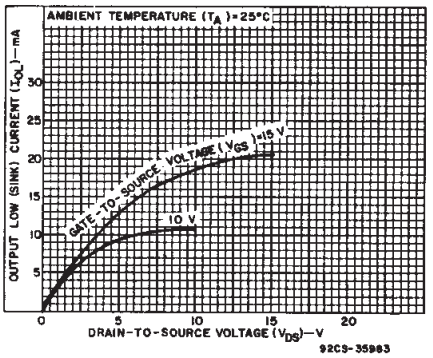


Fig.8 – Typical n-channel output low (sink) current characteristics.

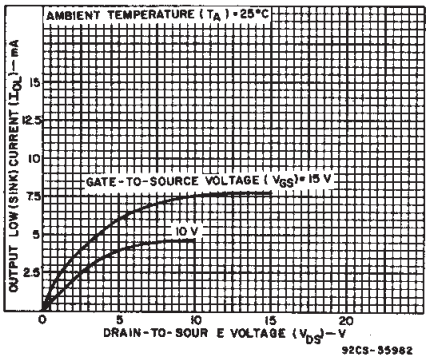


Fig.9 – Minimum n-channel output low (sink) current characteristics.

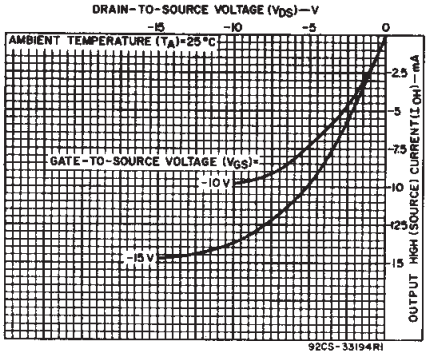


Fig.10 – Typical p-channel output high (source) current characteristics.

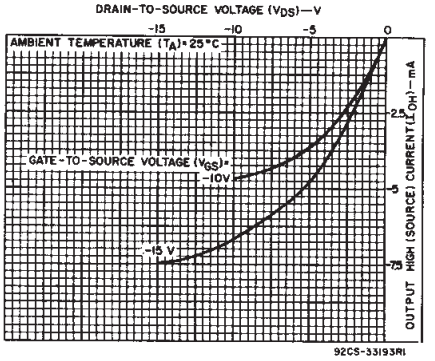


Fig. 13 – Minimum p-channel output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ kΩ

CHARACTERISTIC	CONDITIONS V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS ALL PACKAGE TYPES CD4054 Typ.	CD4054 Max.	CD4055,CD4056 Typ.	CD4055,CD4056 Max.	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH} (Any Input to Any Output)	−5	0	5	400	800	650	1300	ns
	0	0	10	340	680	575	1150	
	0	0	15	250	500	375	750	
Transition Time, t_{THL}, t_{TLH} (Any Output)	−5	0	5	100	200	100	200	ns
	0	0	10	100	200	100	200	
	0	0	15	75	150	75	150	
Minimum Data Setup Time, t_S*	−5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
			15	35	70	35	70	
Minimum Strobe Pulse Width, t_W*	−5	0	5	110	220	110	220	ns
	0	0	10	50	100	50	100	
	0	0	15	35	70	35	70	
Input Capacitance, C_{IN} (Any Input)	–	–	–	5	7.5	5	7.5	pF

* CD4054 and CD4056 only.

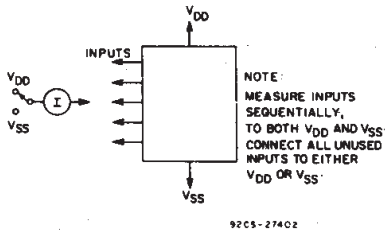


Fig. 14 – Input-current test circuit.

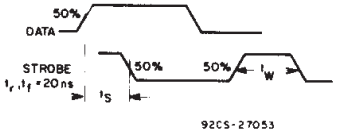


Fig. 15 – Data setup time and strobe pulse duration.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^oC$ (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply Voltage Range: (At T_A = Full Package Temperature Range)				3	18	V
Setup Time (t_s)●	−5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	
Strobe Pulse Width (t_W)●	−5	0	5	220	–	ns
	0	0	10	100	–	
	0	0	15	70	–	

● For CD4054 and CD4056 only.

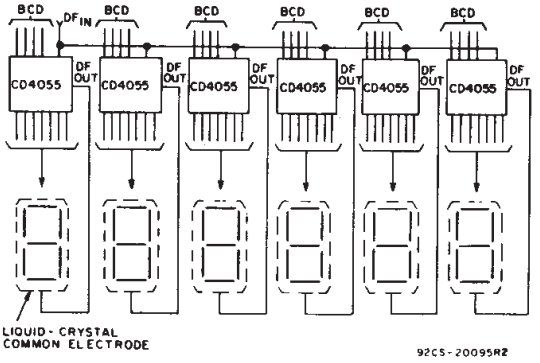
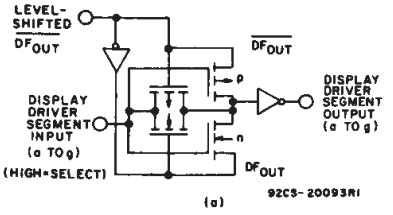


Fig. 16 – Clock display: $V_{DD} = 0$ V, $V_{SS} = -5$ V, $V_{EE} = -15$ V, $DF_{IN} = 30$ Hz square wave.



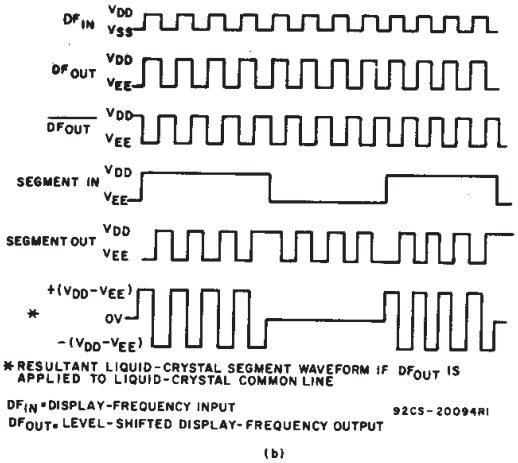


Fig. 17 – Display-driver circuit for one segment line and waveforms.

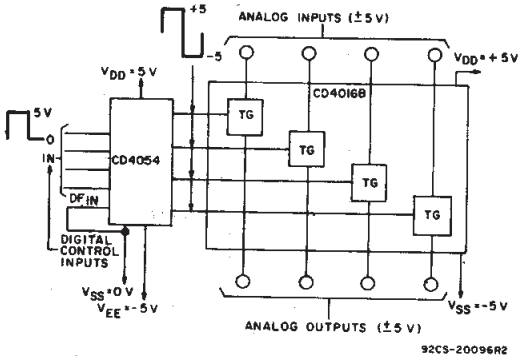


Fig. 18 – Digital (0 to +5 V) to bidirectional analog control (+5 to −5 V) level shifter.

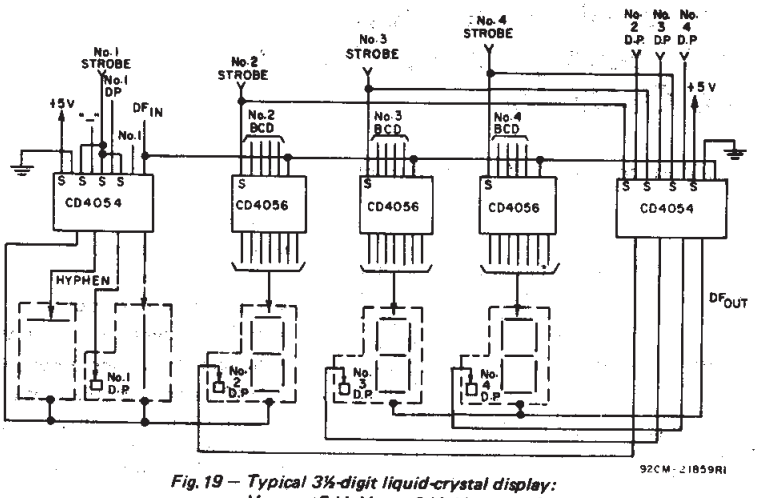


Fig. 19 – Typical 3½-digit liquid-crystal display: V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = −10 V, DF_{IN} = 30 Hz square wave.

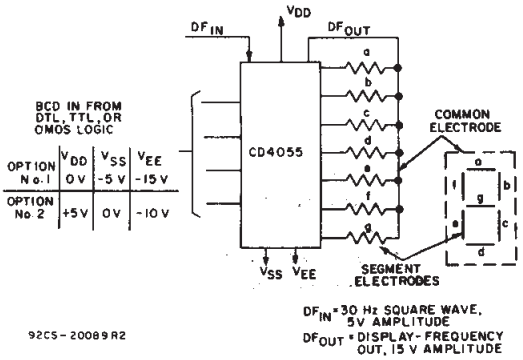


Fig. 20 – Single-digit liquid-crystal display.

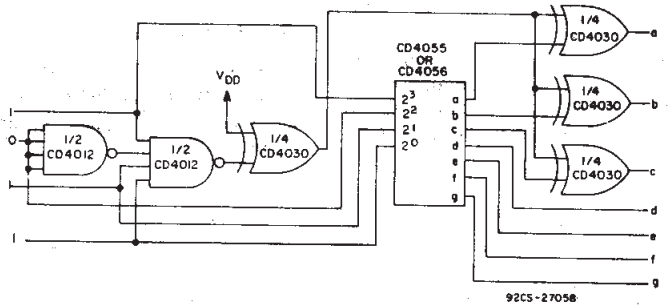


Fig. 21 – Conversion of "H" display to "F" display.

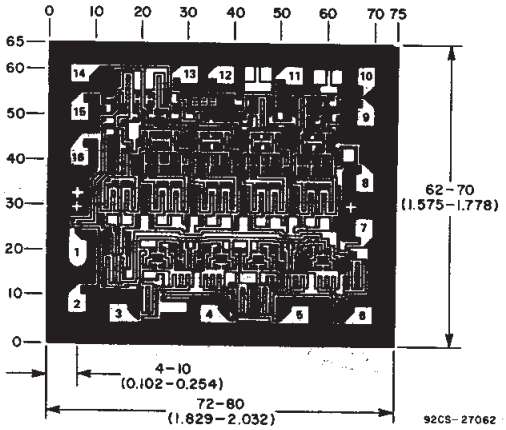
In addition to the letters L, H, P, and A (See the truth table), five other letters can be displayed through the use of simple logic circuits preceding and following the CD4055B or CD4056B devices. Fig. 21 is an example of a circuit that converts an "H" display (code 1011) to an "F" display.

One condition that must be met is that $V_{EE}=V_{SS}$. If $V_{EE}\neq V_{SS}$, the CD4054B must be used to level shift in the appropriate places.

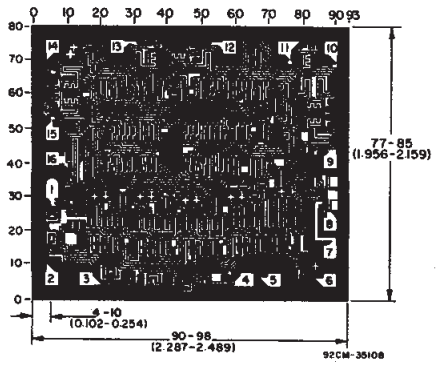
In a similar manner the letters C, E, J, and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive.

The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is preknowledge that only letters are to be displayed.

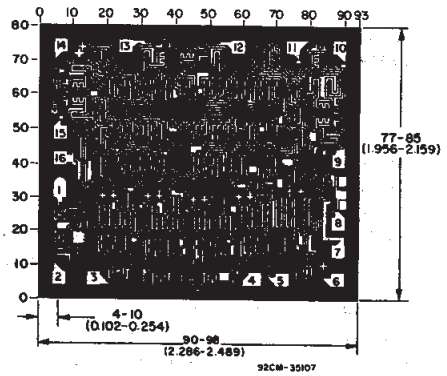
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Dimensions and pad layout for CD4054BH.



Dimensions and pad layout for CD4055BH



Dimensions and pad layout for CD4056BH

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4054BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4054BE
CD4054BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4054BE
CD4054BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4054BF3A
CD4054BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4054BF3A
CD4054BM	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4054BM
CD4054BM96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4054BM
CD4054BM96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4054BM
CD4054BPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM054B
CD4054BPW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM054B
CD4055BE	Last Time Buy	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4055BE
CD4055BM	Last Time Buy	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4055BM
CD4055BPW	Last Time Buy	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM055B
CD4056BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4056BE
CD4056BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4056BE
CD4056BF3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4056BF3A
CD4056BF3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4056BF3A
CD4056BM	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4056BM
CD4056BM96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM
CD4056BM96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM
CD4056BMT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD4056BM
CD4056BPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM056B
CD4056BPW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM056B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4054B, CD4054B-MIL, CD4056B, CD4056B-MIL :

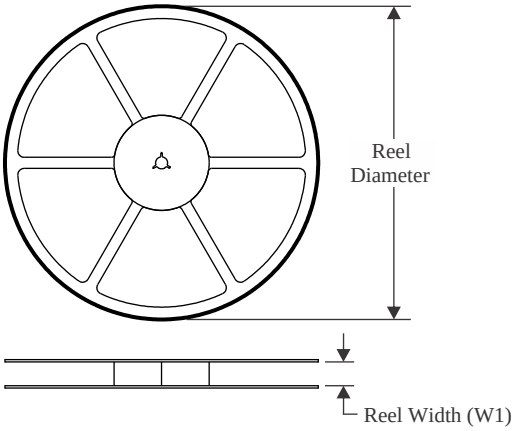
- Catalog : CD4054B, CD4056B
- Military : CD4054B-MIL, CD4056B-MIL

NOTE: Qualified Version Definitions:

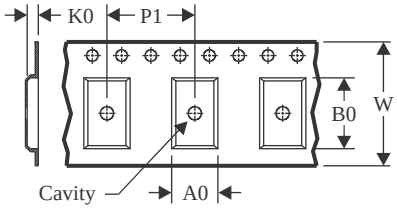
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

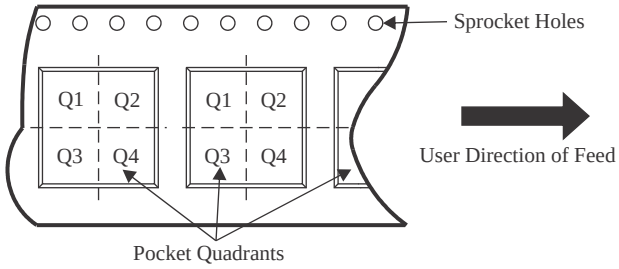


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

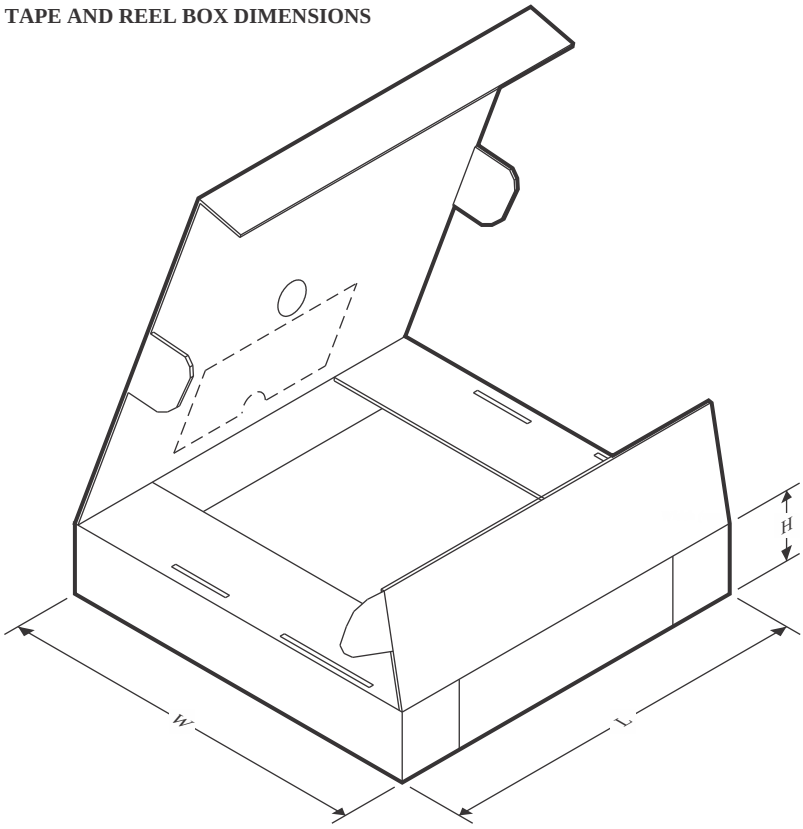
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4054BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4056BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

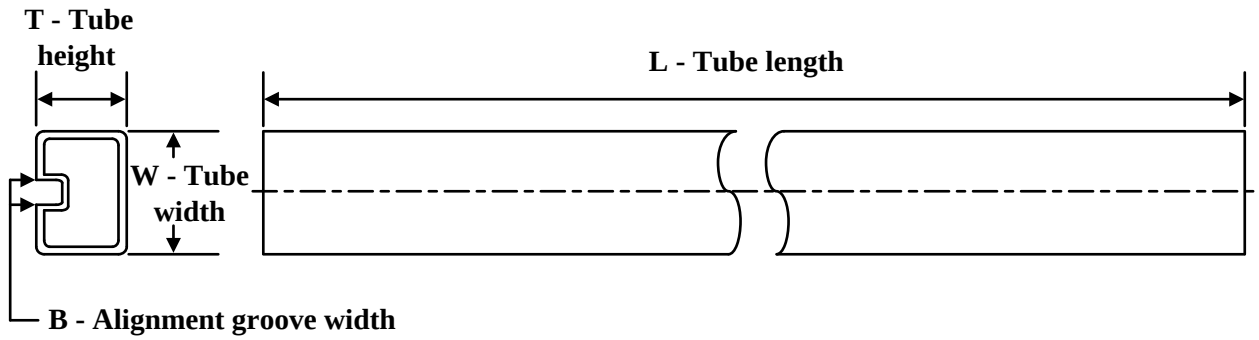
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4054BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4056BM96	SOIC	D	16	2500	340.5	336.1	32.0

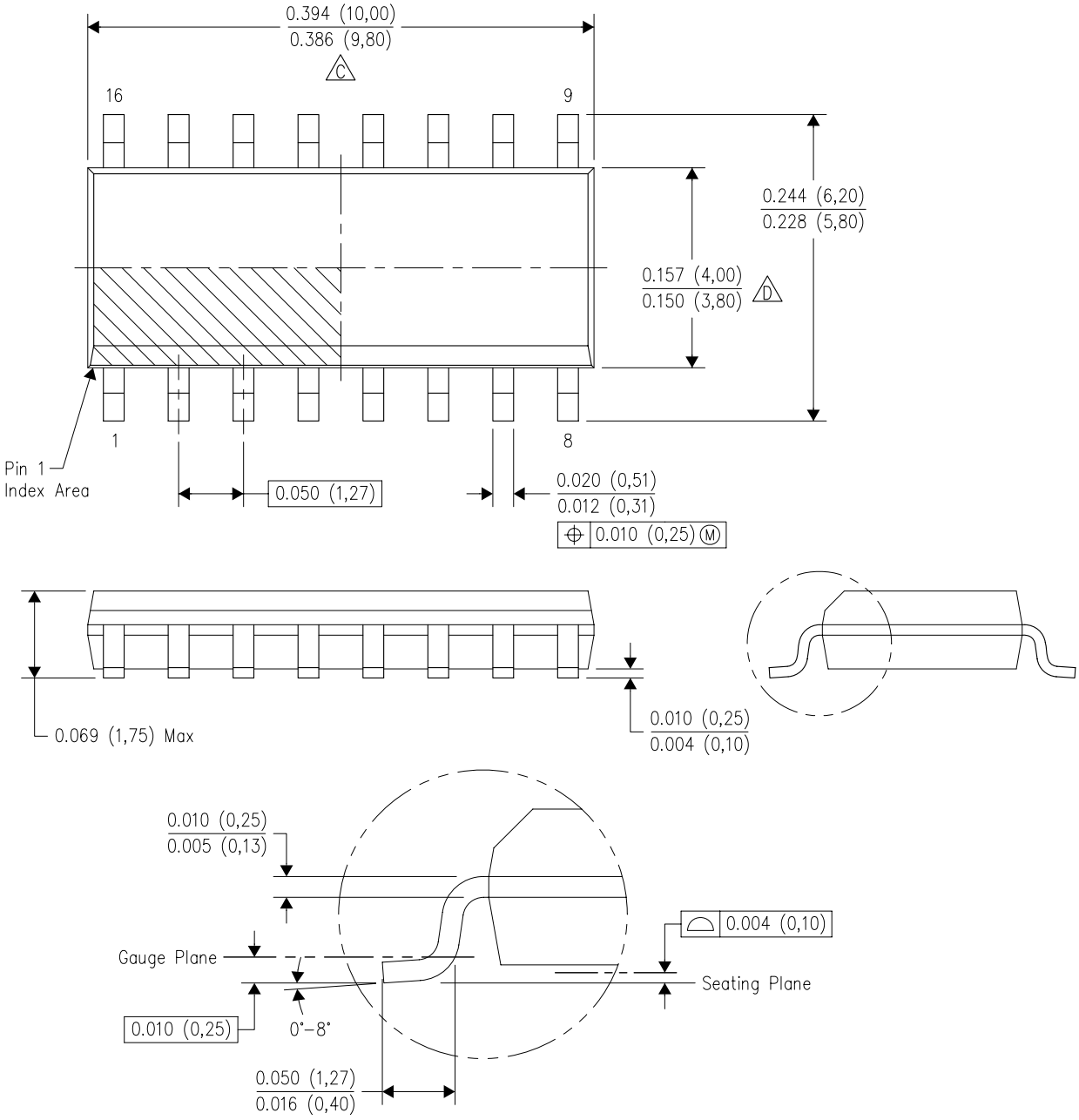
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4054BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4054BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4054BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4054BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4054BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4054BPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4055BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4055BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4055BM	D	SOIC	16	40	507	8	3940	4.32
CD4055BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4056BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4056BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4056BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4056BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4056BPW	PW	TSSOP	16	90	530	10.2	3600	3.5
CD4056BPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



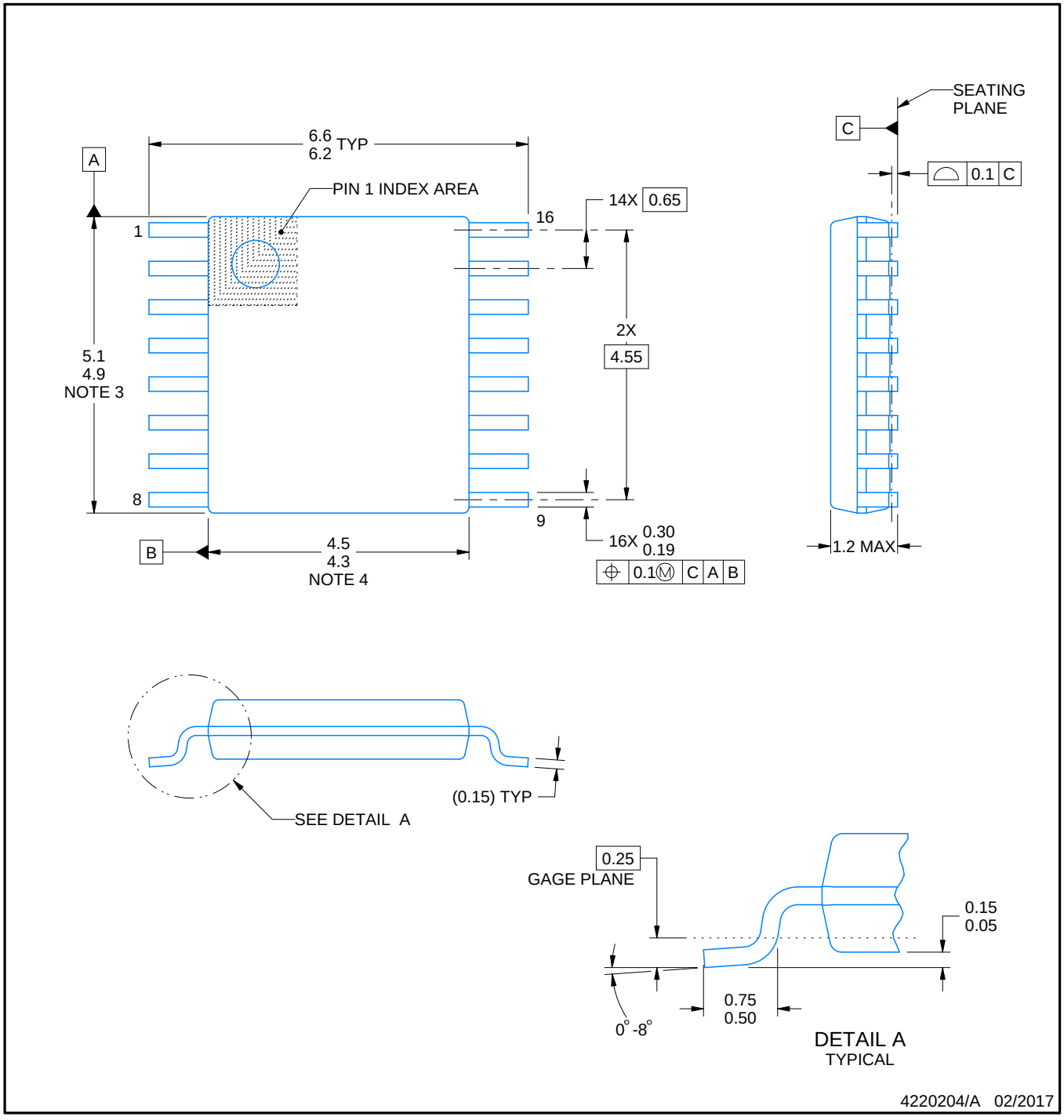
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

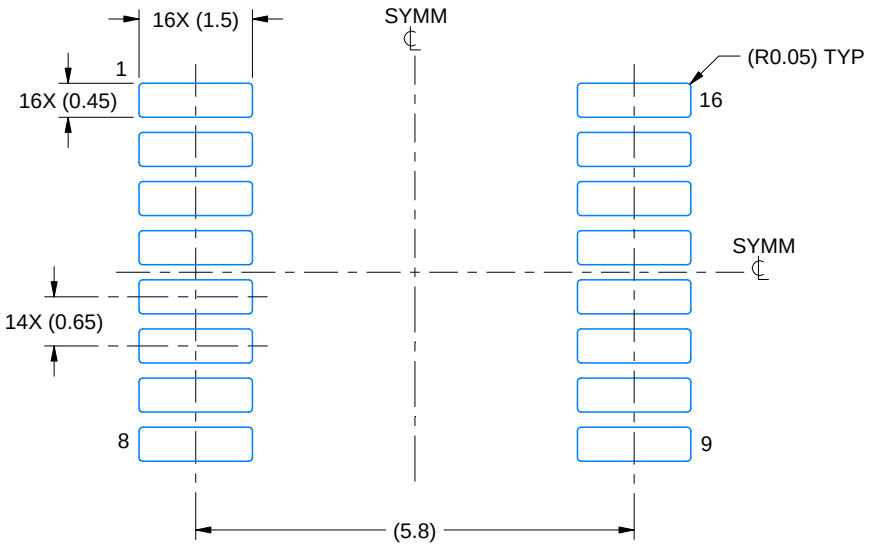
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



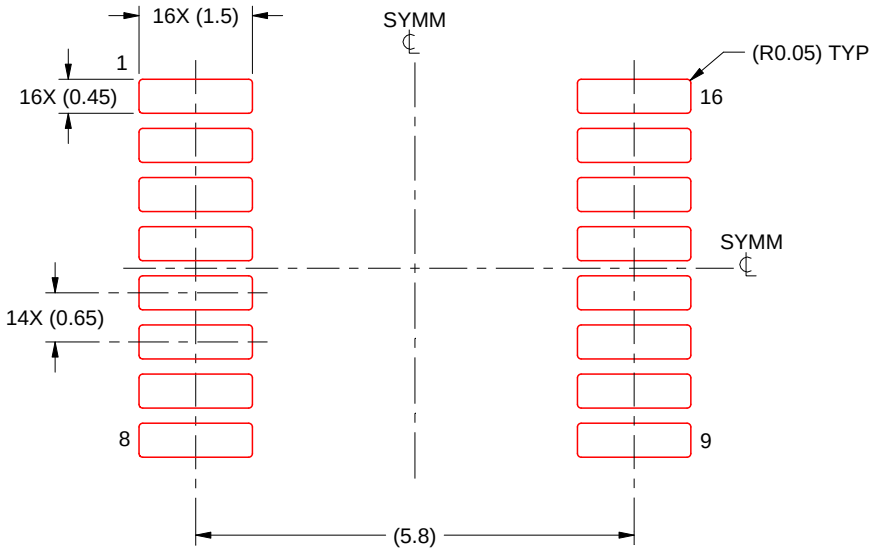
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

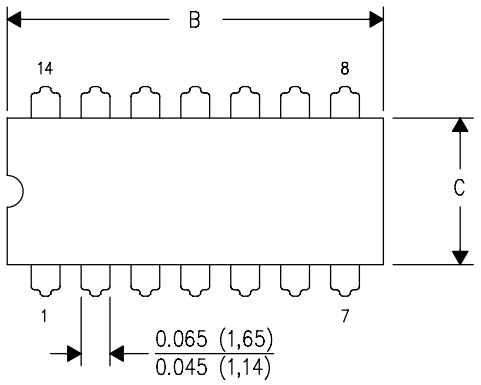
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

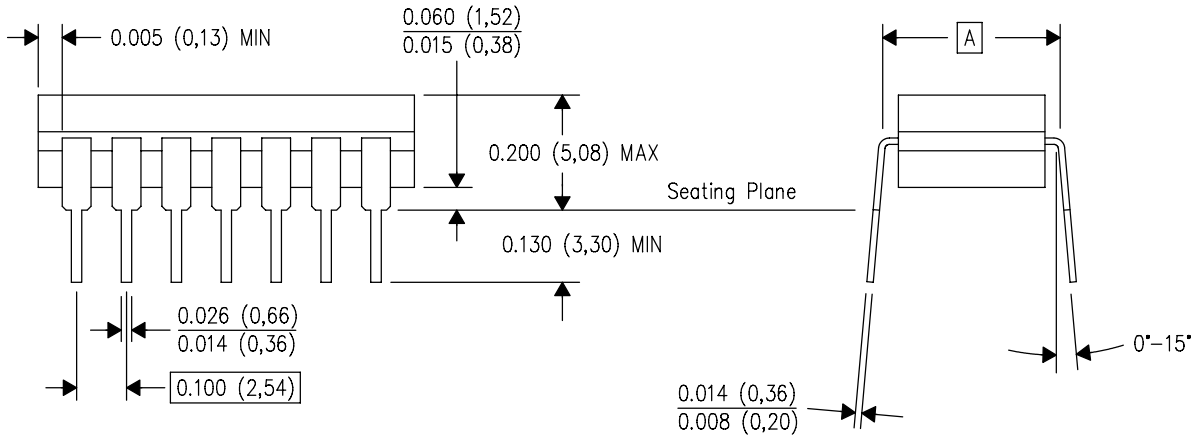
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



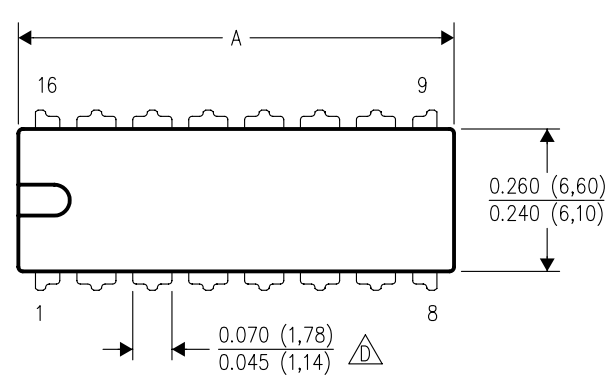
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

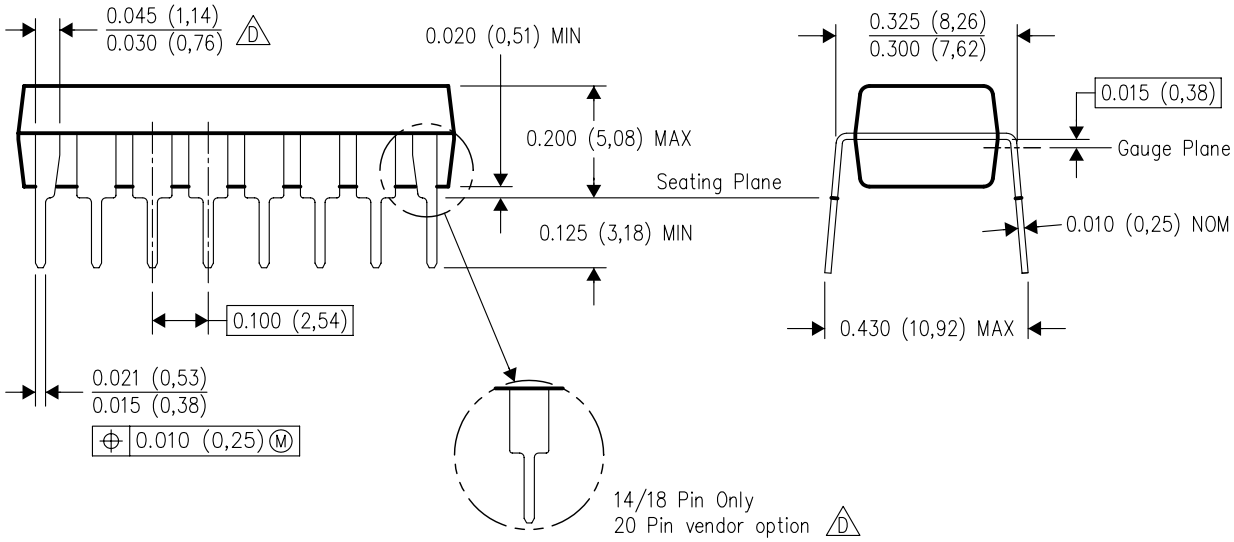
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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