TLV243x-Q1 Advanced LinCMOS™ Rail-to-Rail Output Wide-Input-Voltage Operational Amplifiers

1 Features

- Qualified for automotive applications
- ESD protection exceeds 2000V per MIL-STD-883, method 3015; exceeds 200V using machine model (C = 200pF, R = 0)
- Output swing includes both supply rails
- Extended common-mode input voltage range: 0V to 4.5V (minimum) at 5V single supply
- No phase inversion
- Low noise: 18nV/$\sqrt{Hz}$ (typical) at f = 1kHz
- Low input offset voltage: 950µV (maximum) at T_A = 25°C (TLV243xA-Q1)
- Low input bias current: 1pA (typical)
- Very low supply current: 125µA per channel (maximum)
- 600Ω output drive
- Macromodel included

2 Applications

- Battery management unit
- ADAS domain controller
- Brake system

3 Description

The TLV243x and TLV243xA are low-voltage operational amplifier from Texas Instruments. The common-mode input voltage range for each device is extended over the typical CMOS amplifiers making them suitable for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3V and 5V supplies and is optimized for low-voltage operation. The TLV243x only requires 100µA (typical) of supply current per channel, making it ideal for battery-powered applications. The TLV243x also has increased output drive over previous rail-to-rail operational amplifiers and can drive 600Ω loads for telecom applications.

The other members in the TLV243x family are the high-power, TLV244x, and micro-power, TLV2422, versions.

The TLV243x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV243xA is available and has a maximum input offset voltage of 950 µV.

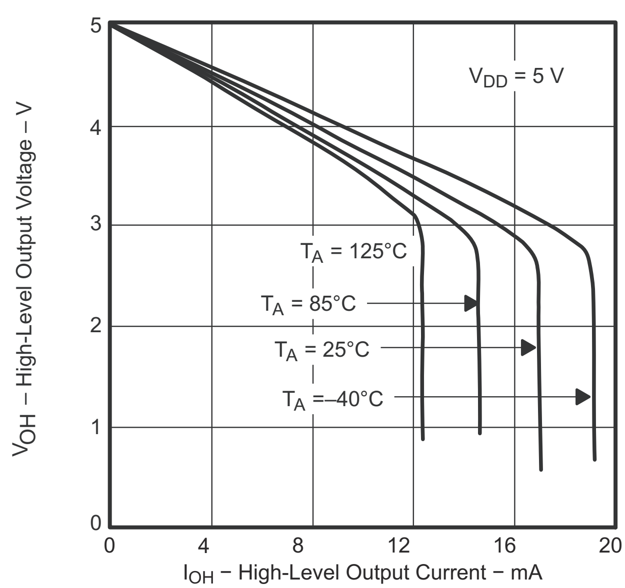
If the design requires single operational amplifiers, see the TI TLV2211, TLV2221, or TLV2231 for rail-to-rail output operational amplifiers in a SOT-23 package. The small size and low power consumption of the TLV22xx devices are designed for high density, battery-powered equipment.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TLV2432-Q1, TLV2432A-Q1	D (SOIC, 8)	4.9mm × 6mm
TLV2434A-Q1	D (SOIC, 8)	4.9mm × 6mm
	PW (TSSOP, 14)	5mm × 6.4mm

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

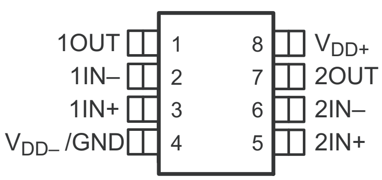


4 Ordering Information

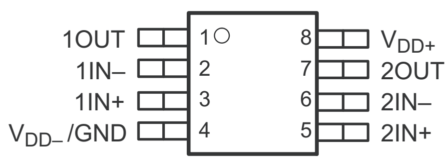
T_A	V_{IO}max AT 25°C	PACKAGE[(2)]		ORDERABLE PART NUMBER [(1)]	TOP-SIDE MARKING
–40°C to 125°C	950 µV	SOIC – D	Tape and reel	TLV2432AQDRQ1	2432AQ
		TSSOP – PW	Tape and reel	TLV2432AQPWRQ1	PREVIEW
	2.5 mV	SOIC – D	Tape and reel	TLV2432QDRQ1	2432Q1
		TSSOP – PW	Tape and reel	TLV2432QPWRQ1	PREVIEW
	950 µV	SOIC – D	Tape and reel	TLV2434AQDRQ1	2434AQ
		TSSOP – PW	Tape and reel	TLV2434AQPWRQ1	2434AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

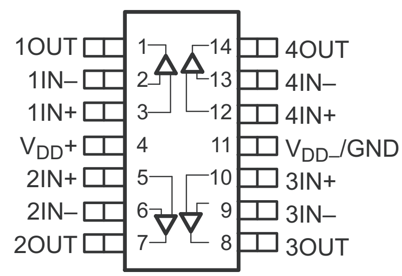
TLV2432
D PACKAGE
(TOP VIEW)

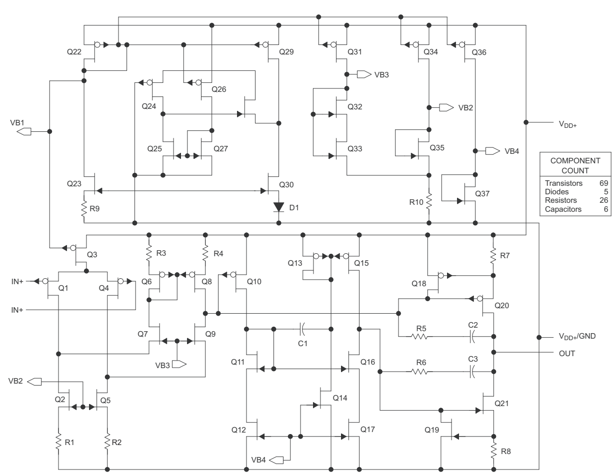


TLV2432
PW PACKAGE
(TOP VIEW)



TLV2434
D OR PW PACKAGE
(TOP VIEW)





Equivalent Schematic (Each Amplifier)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
V_{DD}	Supply voltage[(2)]		12	V
V_{ID}	Differential input voltage[(3)]		$\pm V_{DD}$	
I_I	Input current (any input)		±5	mA
I_O	Output current		±50	mA
	Total current into V_{DD+}		±50	mA
	Total current out of V_{DD-}		±50	mA
	Duration of short-circuit current at (or below) 25°C[(4)]	Unlimited		
	Continuous total dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range: Q suffix	–40	125°C	
T_{stg}	Storage temperature range	–65	150°C	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below V_{DD-} – 0.3 V.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

5.2 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14)	1022 mW	7.6 mW/°C	900 mW	777 mW	450 mW
PW (8)	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW (14)	720 mW	5.6 mW/°C	634 mW	547 mW	317 mW

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.7	10	V
V_I	Input voltage	V_{DD-}	V_{DD+} – 0.8	V
V_{IC}	Common-mode input voltage	V_{DD-}	V_{DD+} – 0.5	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Electrical Characteristics: V_{DD} = 3 V

at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, $V_{DD\pm}$ = ±1.5 V, R_S = 50 Ω	TLV243x	25°C		300	2000	µV
				Full range			2500	
			TLV243xA	25°C		300	950	
				Full range			1600	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±1.5 V, R_S = 50 Ω	25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift(3)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 2.5	–0.25 to 2.75		V
				Full range	0.2 to 2.2			
V_{OH}	High-level output voltage	I_O = –100 µA		25°C		2.98		V
		I_O = –3 mA		25°C		2.5		
				Full range	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V	I_{OL} = 100 µA	25°C		0.02		V
			I_{OL} = 3 mA	25°C		0.83		
				Full range			1	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 2 V	R_L = 2 kΩ(2)	25°C	1.5	2.5		V/mV
				Full range	0.5			
			R_L = 1 MΩ(2)	25°C		750		
r_{id}	Differential input resistance			25°C		1000		GΩ
r_i	Common-mode input resistance			25°C		1000		GΩ
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} MIN, R_S = 50 Ω	V_O = 1.5 V,	25°C	63	83		dB
				Full range	63			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load		25°C		115	150	µA
				Full range			175	

(1) Full range is –40°C to 125°C.
(2) Referenced to 2.5 V.
(3) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5.5 Operating Characteristics: V_{DD} = 3 V

at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A [1]	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 1 V to 2 V, R_L = 2 kΩ[2], C_L = 100 pF[2]		25°C	0.15	0.25		V/µs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		120		nV/√Hz
		f = 1 kHz				22		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		µV
		f = 0.1 Hz to 10 Hz				4		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 2 kΩ[2], f = 1 kHz	A_V = 1	25°C		0.65%		
			A_V = 10			0.5%		
	Gain-bandwidth product	f = 10 kHz, R_L = 2 kΩ, C_L = 100 pF[2]		25°C		0.5		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 2 kΩ, A_V = 1, C_L = 100 pF[2]		25°C		220		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 2 kΩ[2], C_L = 100 pF[2]	To 0.1%	25°C		1.5		µs
			To 0.01%			3.2		
φ_m	Phase margin at unity gain	R_L = 2kΩ[2], C_L = 100 pF[2]		25°C		62°		
	Gain margin	R_L = 2kΩ[2], C_L = 100 pF[2]		25°C		11		dB

(1) Full range is –40°C to 125°C.
(2) Referenced to 2.5 V

5.6 Electrical Characteristics: V_{DD} = 5 V

V_{DD} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A [1]	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, $V_{DD\pm}$ = ±2.5 V, R_S = 50 Ω	TLV243x	25°C		300	2000	µV
				Full range			2500	
			TLV243xA	25°C		300	950	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD\pm}$ = ±1.5 V, R_S = 50 Ω	25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift[3]			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV, R_S = 50 Ω		25°C	0 to 4.5	–0.25 to 4.75		V
				Full range	0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		4.97		V
		I_{OH} = –5 mA		25°C	4	4.35		
				Full range	4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 100 µA	25°C		0.01		V
			I_{OL} = 5 mA	25°C		0.8		
				Full range			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 2 kΩ[2]	25°C	2.5	3.8		V/mV
				Full range	0.5			
			R_L = 1 MΩ[2]	25°C		950		
r_{id}	Differential input resistance			25°C		1000		GΩ
r_i	Common-mode input resistance			25°C		1000		GΩ
c_i	Common-mode input capacitance	f = 10 MHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} MIN, V_O = 2.5 V, R_S = 50 Ω		25°C	63	90		dB
				Full range	63			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load		25°C		115	150	µA
				Full range			175	

(1) Full range is –40°C to 125°C.
(2) Referenced to 2.5 V
(3) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5.7 Operating Characteristics: V_{DD} = 5 V

V_{DD} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A [1]	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, R_L = 2 kΩ[2], C_L = 100 pF[2]		25°C	0.15	0.25		V/µs
				Full range	0.1			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz				18		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		µV
		f = 0.1 Hz to 10 Hz				2.8		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5V, f = 1 kHz, R_L = 600 Ω[2]	A_V = 1	25°C		0.045%		
			A_V = 10			0.4%		
	Gain-bandwidth product	f = 10 kHz, R_L = 600 Ω[2], C_L = 100 pF[2]		25°C		0.55		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 2 kΩ[2], C_L = 100 pF[2]		25°C		100		kHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 2 kΩ[2], C_L = 100 pF[2]	To 0.1%	25°C		6.4		µs
			To 0.01%			13.1		
φ_m	Phase margin at unity gain	R_L = 2 kΩ[2], C_L = 100 pF[2]		25°C		66°		
	Gain margin	R_L = 2 kΩ[2], C_L = 100 pF[2]		25°C		11		dB

(1) Full range is –40°C to 125°C.
(2) Referenced to 2.5 V

5.8 Typical Characteristics

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	3,4
		vs Common-mode input voltage	5,6
α_{VIO}	Input offset voltage temperature coefficient	Distribution	7,8
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	9
V_{OH}	High-level output voltage	vs High-level output current	10,11
V_{OL}	Low-level output voltage	vs Low-level output current	12,13
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	14
I_{OS}	Short-circuit output current	vs Supply voltage	15
		vs Free-air temperature	16
V_{ID}	Differential input voltage	vs Output voltage	17, 18
	Differential gain	vs Load resistance	19
A_{VD}	Large-signal differential voltage amplification	vs Frequency	20, 21
	Differential voltage amplification	vs Free-air temperature	22, 23
z_o	Output impedance	vs Frequency	24, 25
CMRR	Common-mode rejection ratio	vs Frequency	26
		vs Free-air temperature	27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	28, 29
		vs Free-air temperature	30
I_{DD}	Supply current	vs Supply voltage	31
SR	Slew rate	vs Load capacitance	32
		vs Free-air temperature	33
V_O	Inverting large-signal pulse response		34, 35
	Voltage-follower large-signal pulse response		36, 37
	Inverting small-signal pulse response		38, 39
	Voltage-follower small-signal pulse response		40, 41
V_n	Equivalent input noise voltage	vs Frequency	42, 43
	Noise voltage (referred to input)	Over a 10-second period	44
THD + N	Total harmonic distortion plus noise	vs Frequency	45, 46
	Gain-bandwidth product	vs Free-air temperature	47
		vs Supply voltage	48
φ_m	Phase margin	vs Frequency	20, 21
		vs Load capacitance	49
	Gain margin	vs Load capacitance	50
B_1	Unity-gain bandwidth	vs Load capacitance	51

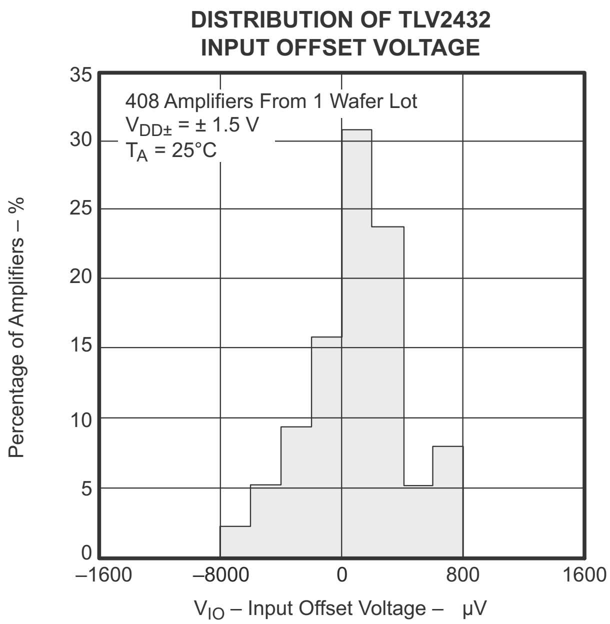


Figure 5-1.

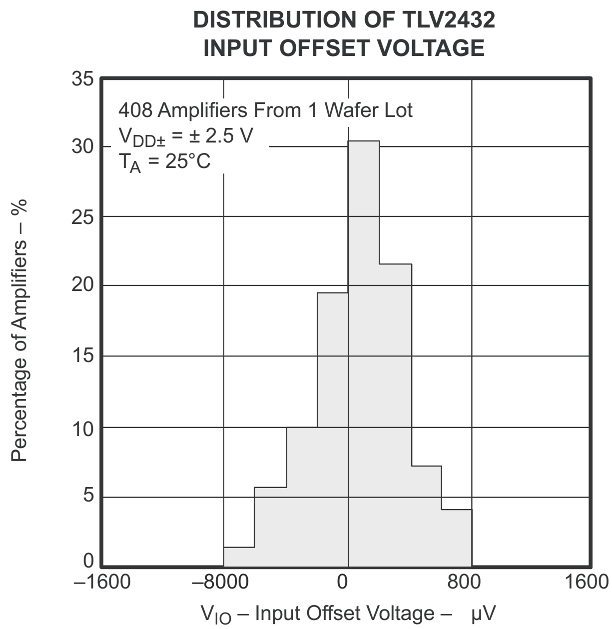


Figure 5-2.

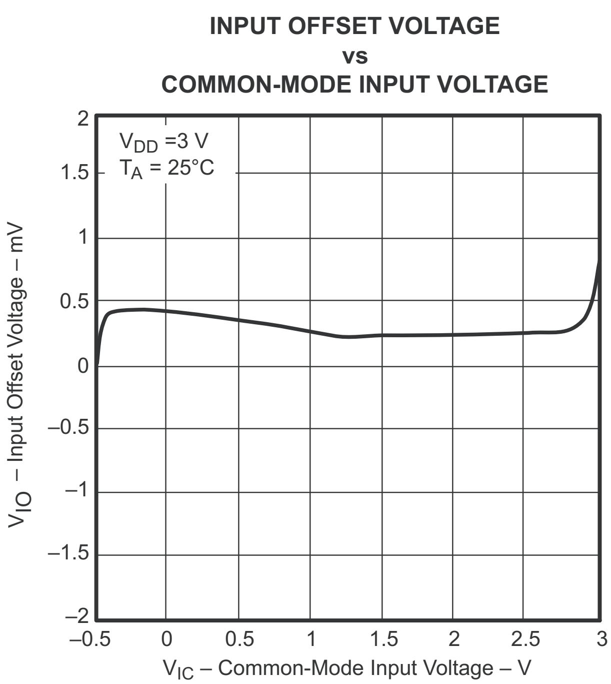


Figure 5-3.

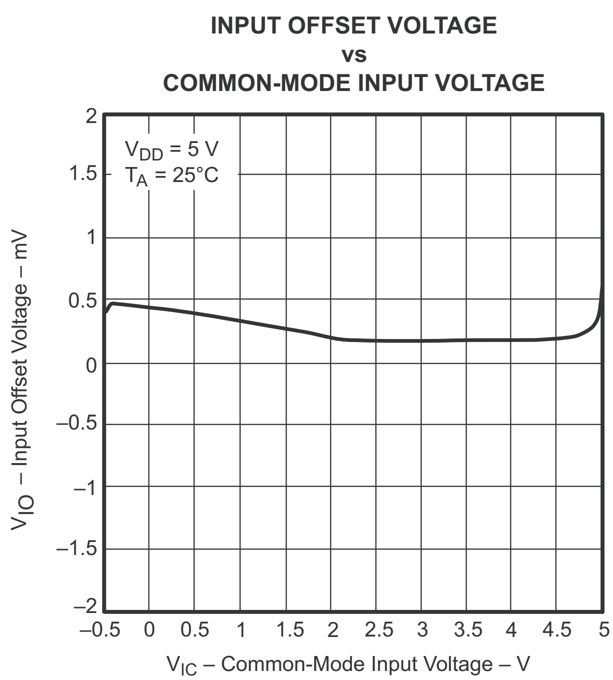


Figure 5-4.

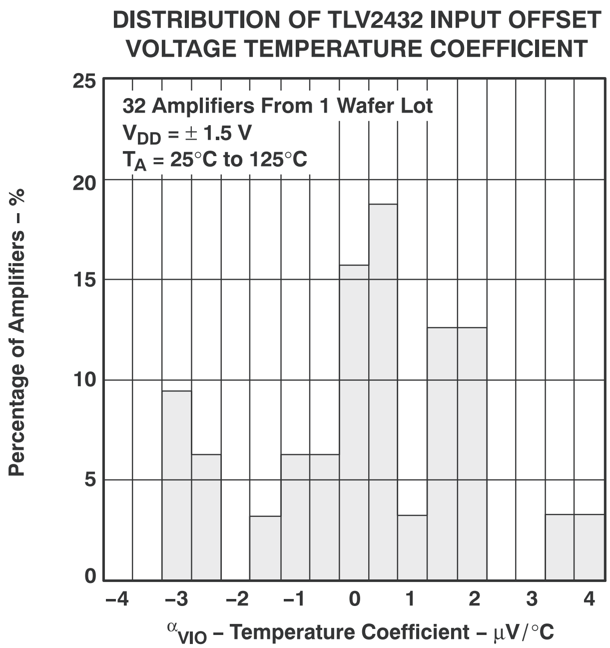


Figure 5-5.

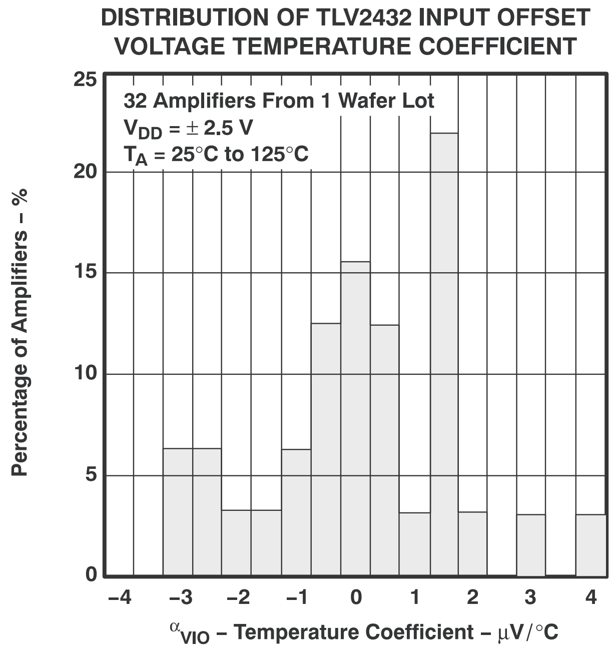


Figure 5-6.

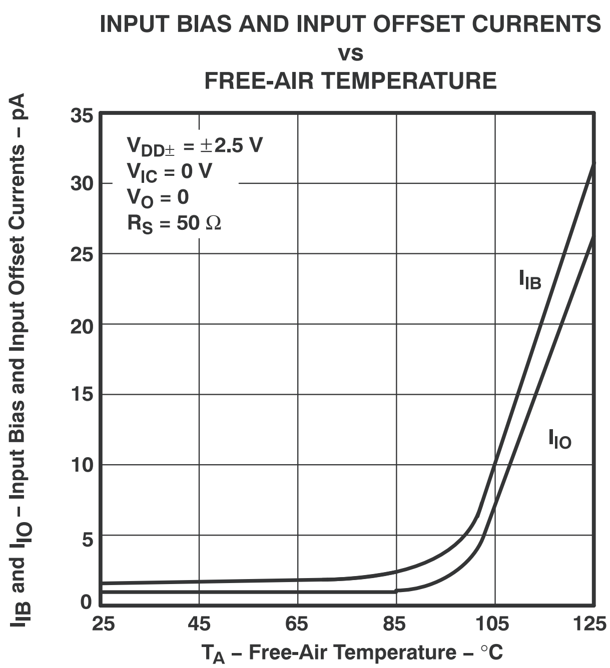


Figure 5-7.

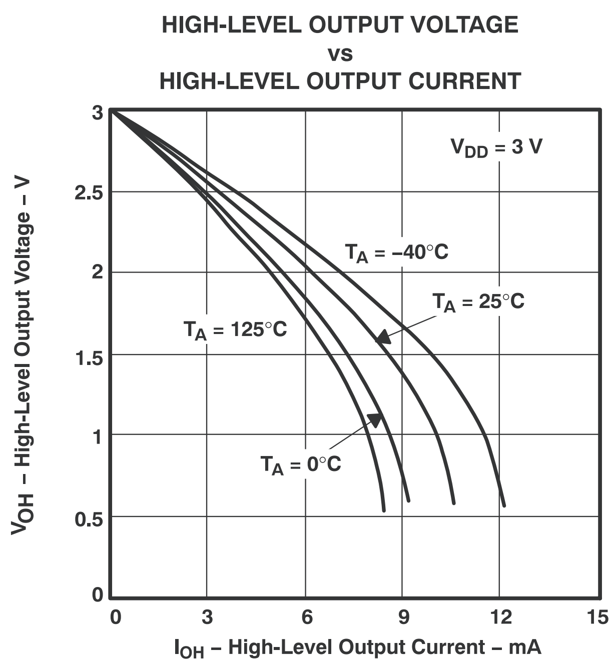


Figure 5-8.

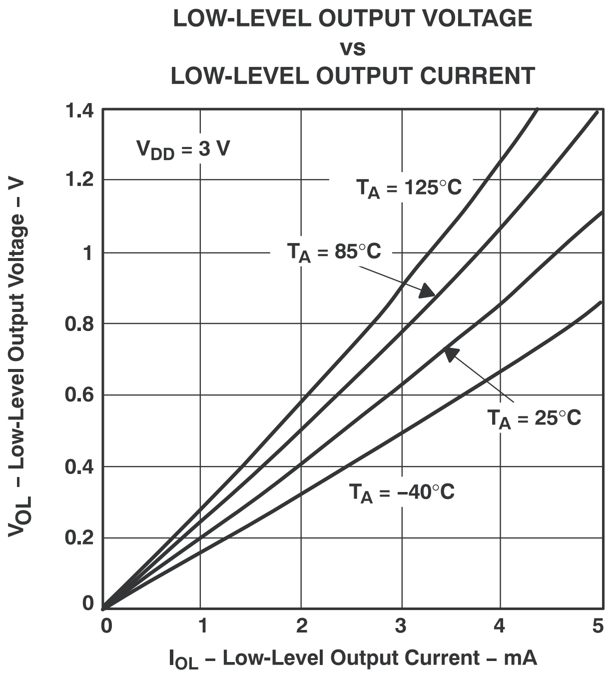


Figure 5-9.

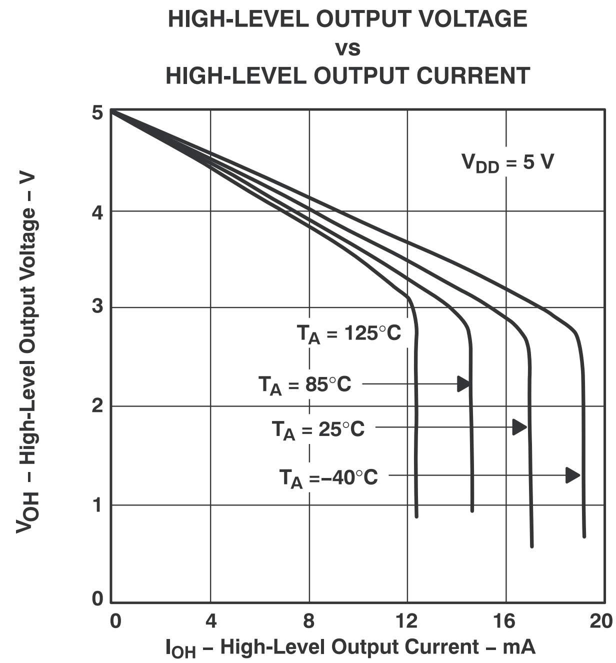


Figure 5-10.

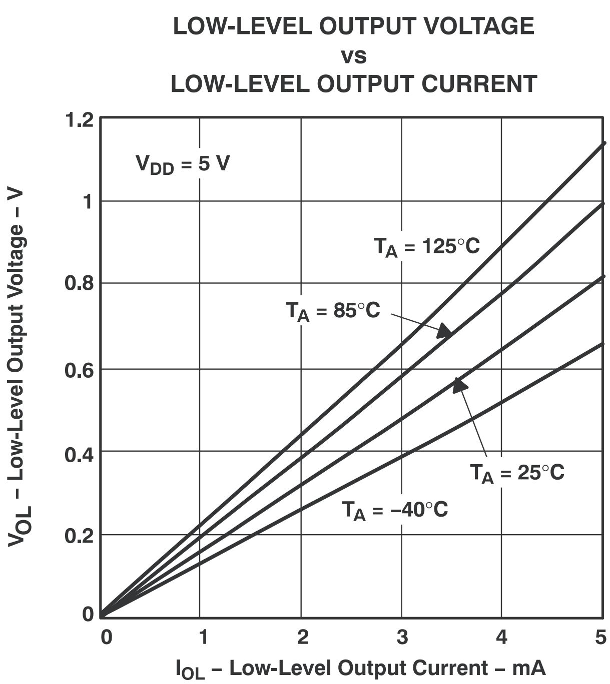


Figure 5-11.

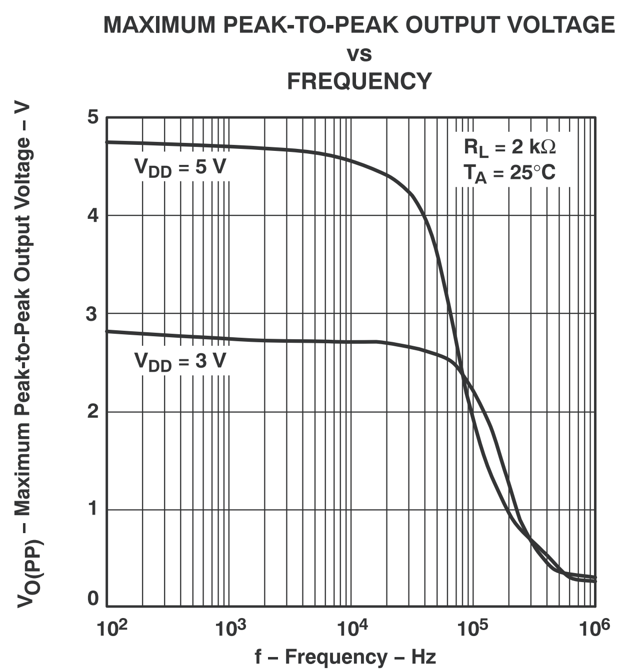


Figure 5-12.

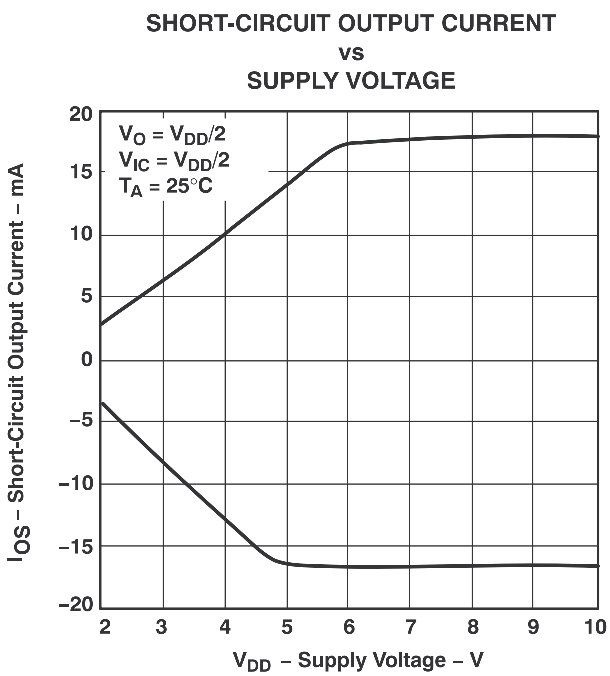


Figure 5-13.

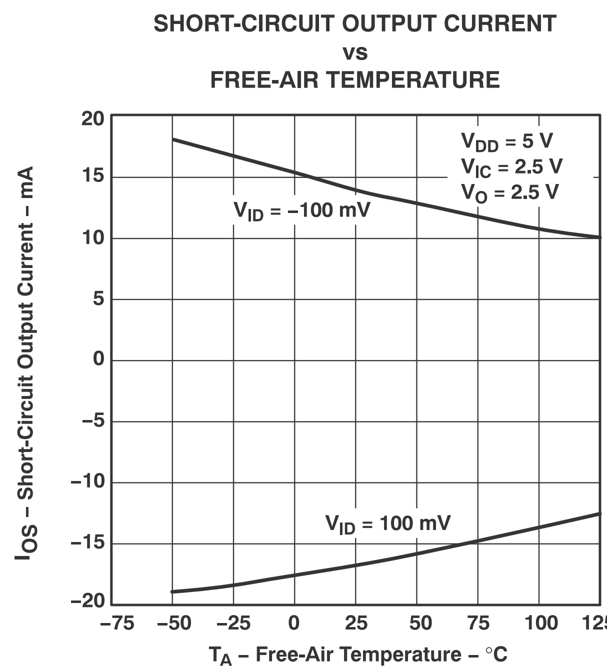


Figure 5-14.

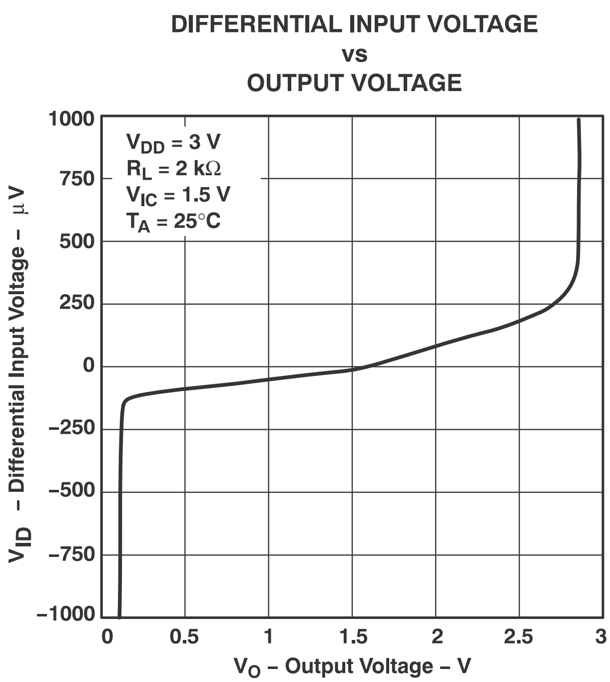


Figure 5-15.

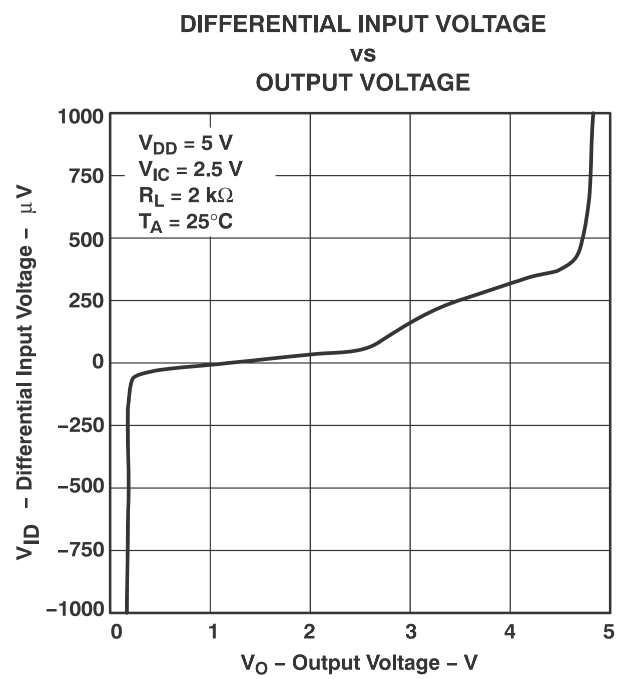


Figure 5-16.

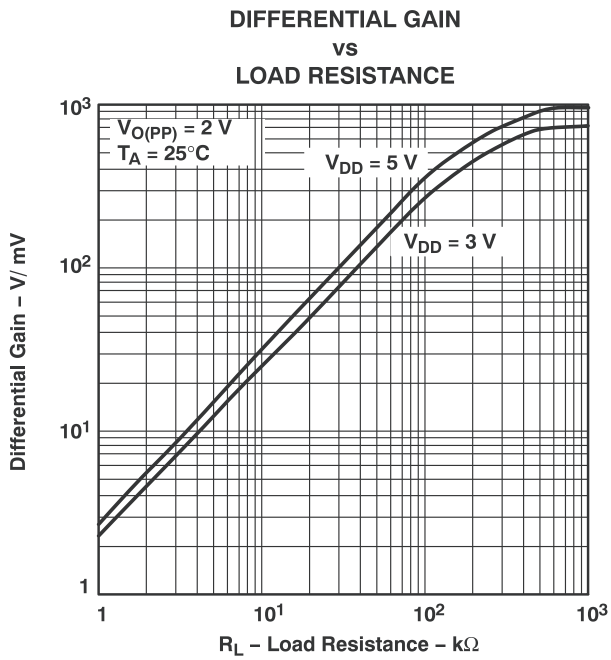


Figure 5-17.

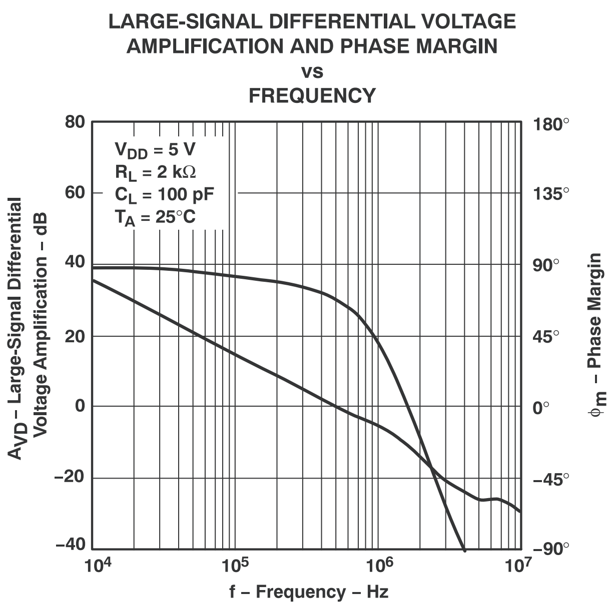


Figure 5-18.

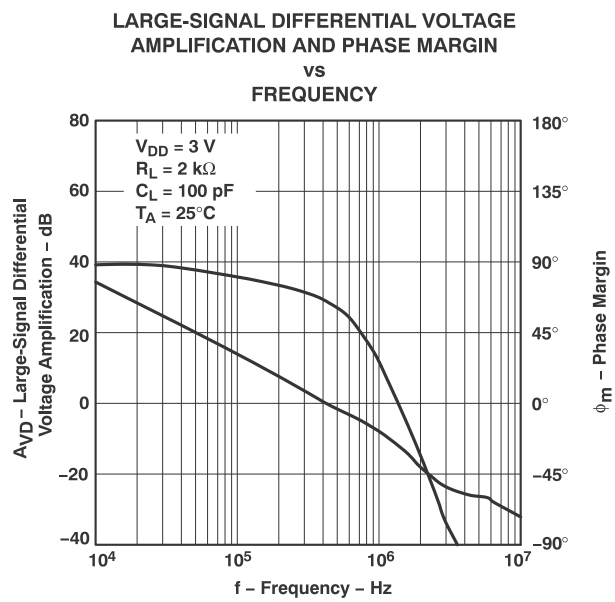


Figure 5-19.

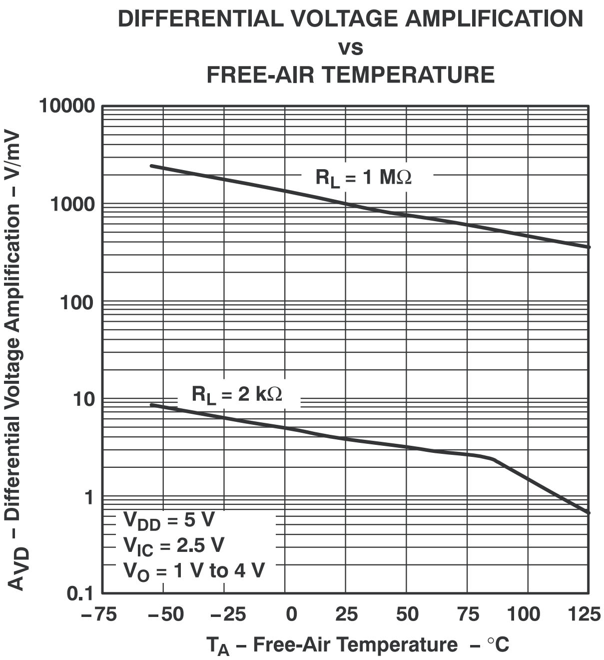


Figure 5-20.

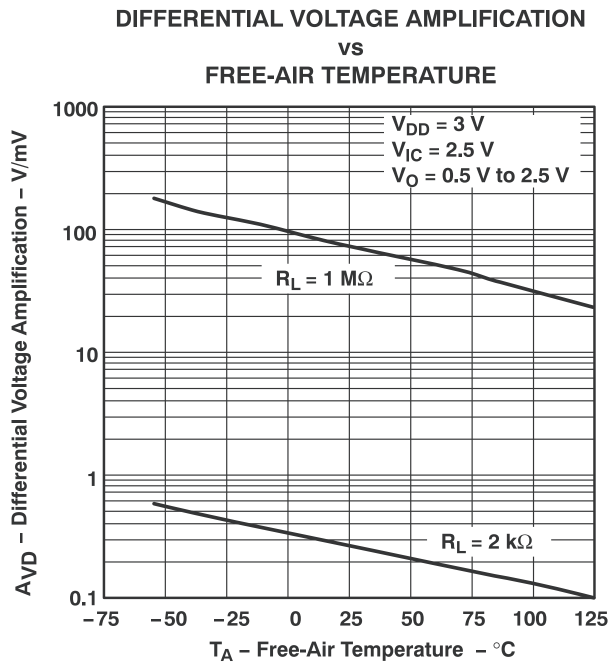


Figure 5-21.

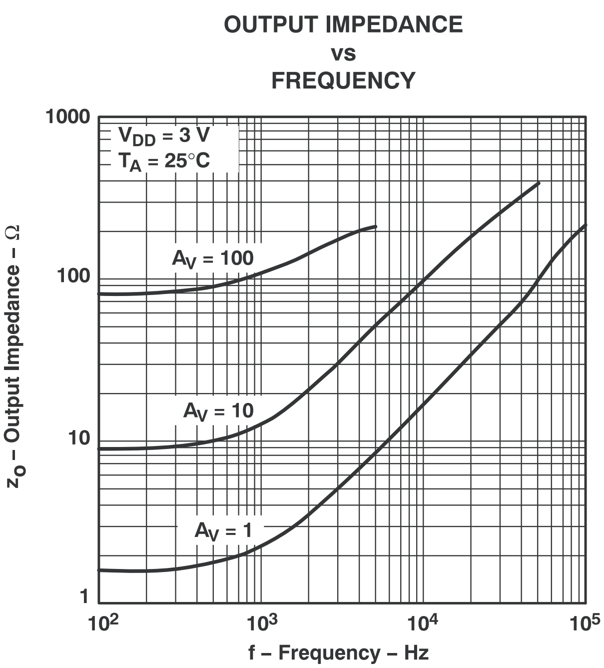


Figure 5-22.

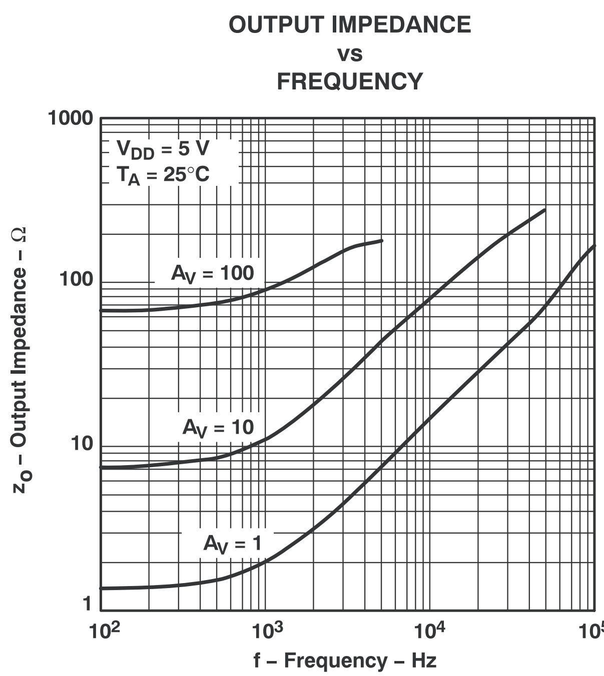


Figure 5-23.

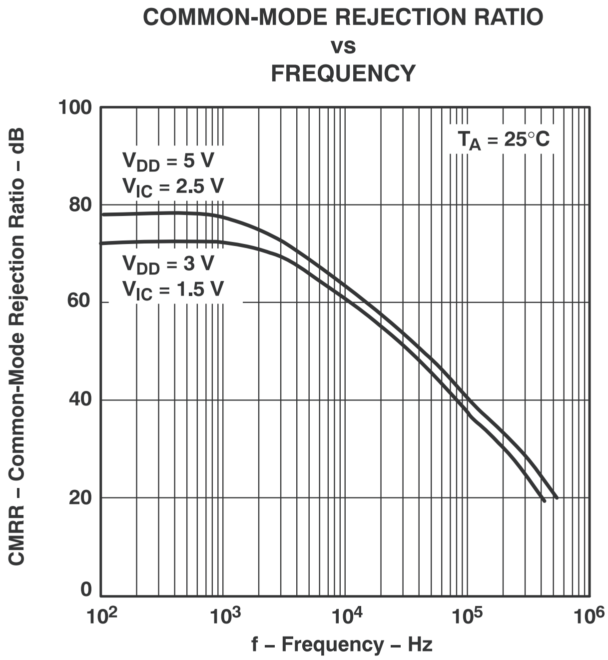


Figure 5-24.

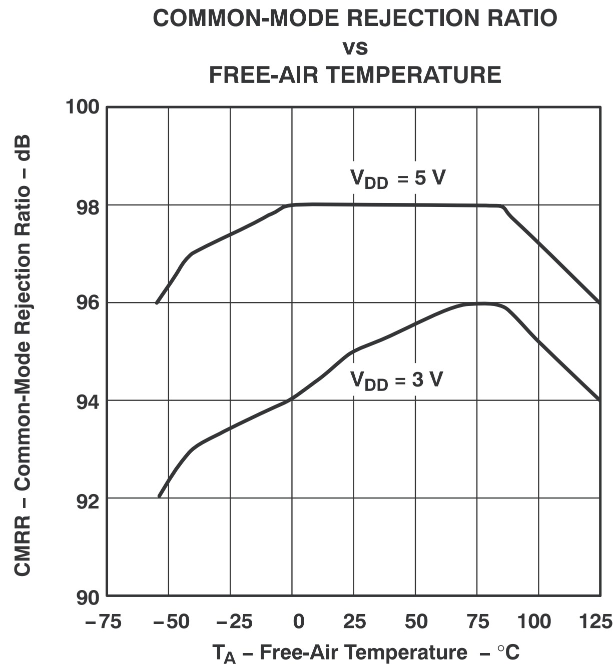


Figure 5-25.

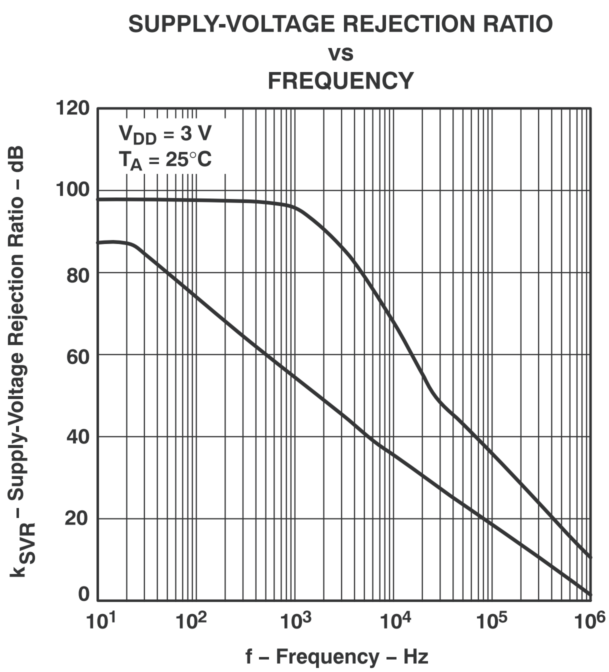


Figure 5-26.

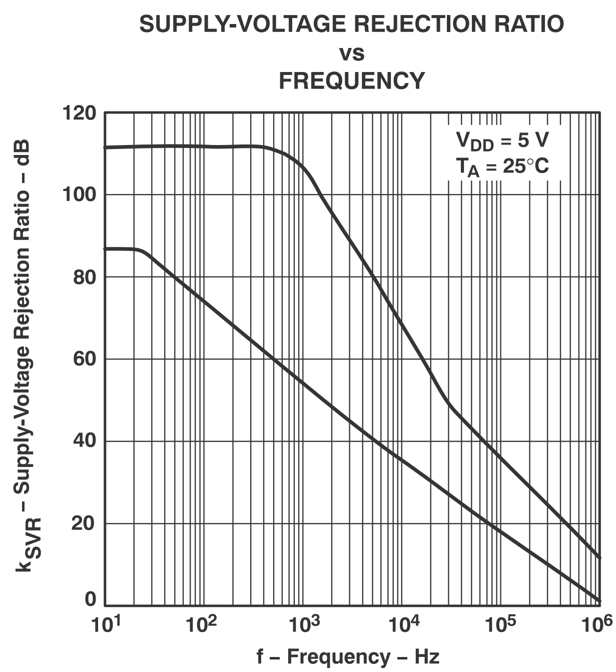


Figure 5-27.

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

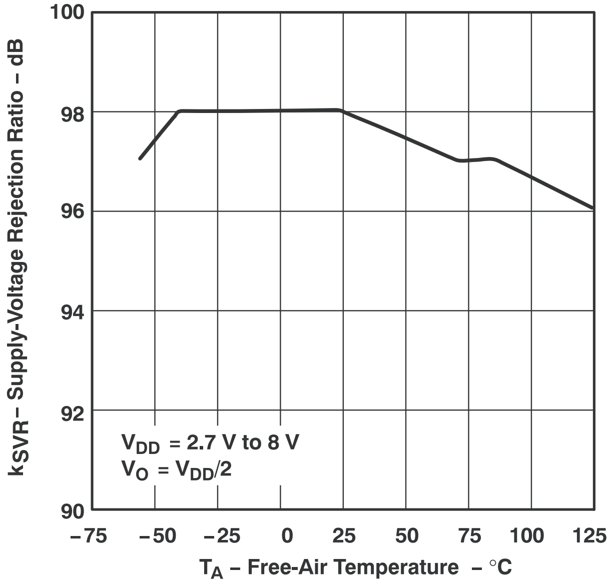


Figure 5-28.

SUPPLY CURRENT vs SUPPLY VOLTAGE

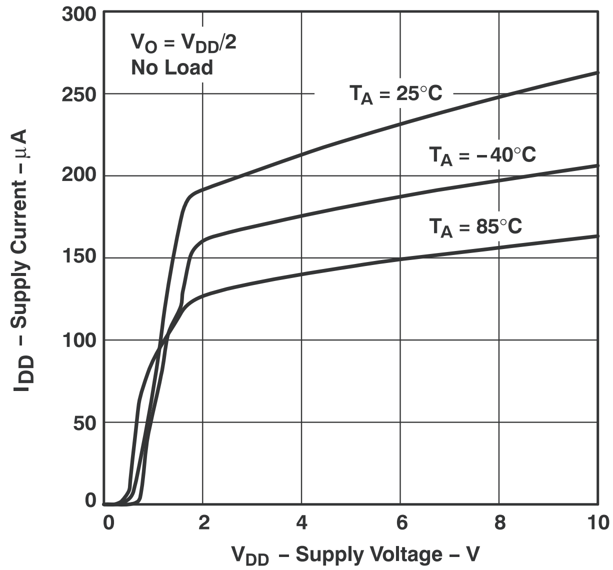


Figure 5-29.

SLEW RATE vs LOAD CAPACITANCE

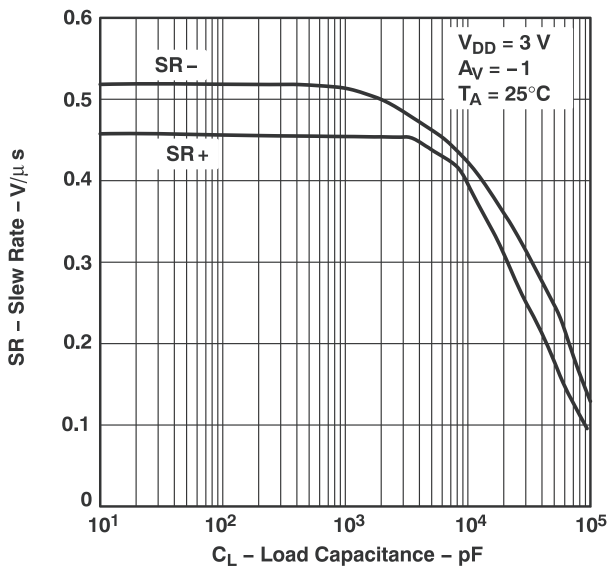


Figure 5-30.

SLEW RATE vs FREE-AIR TEMPERATURE

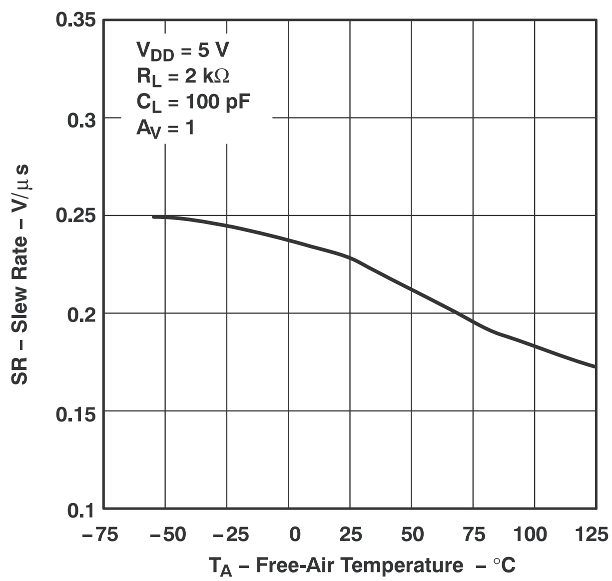


Figure 5-31.

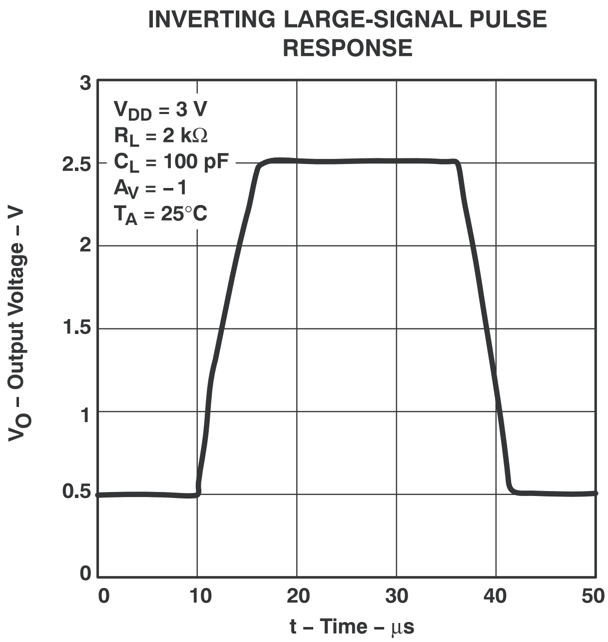


Figure 5-32.

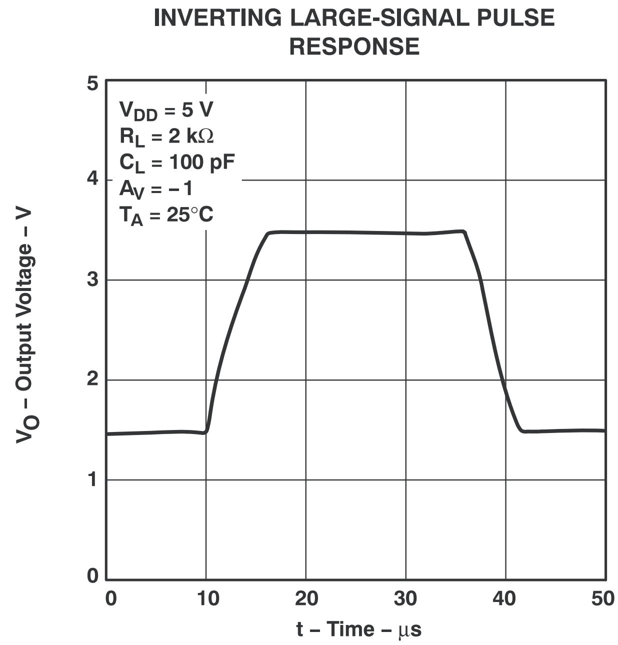


Figure 5-33.

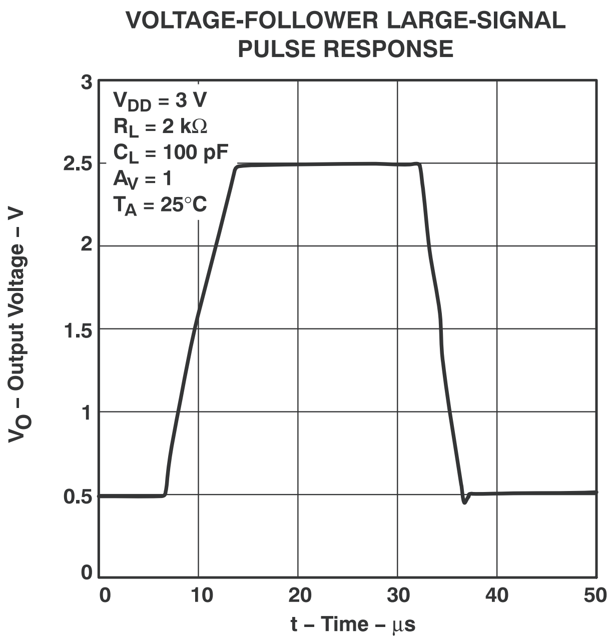


Figure 5-34.

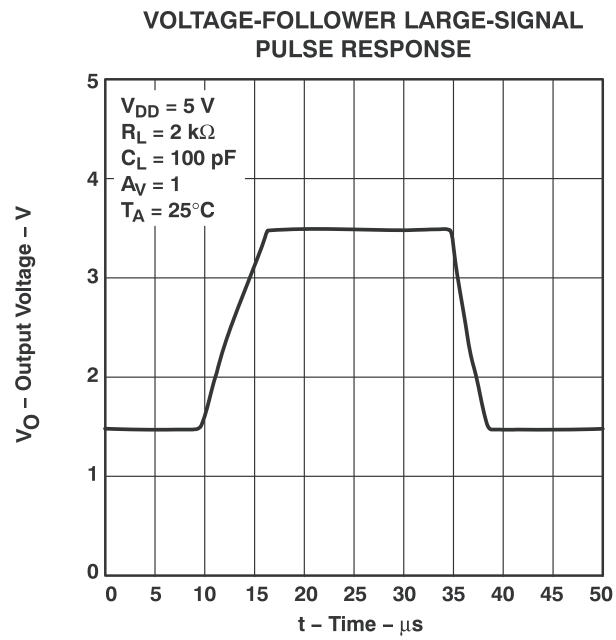


Figure 5-35.

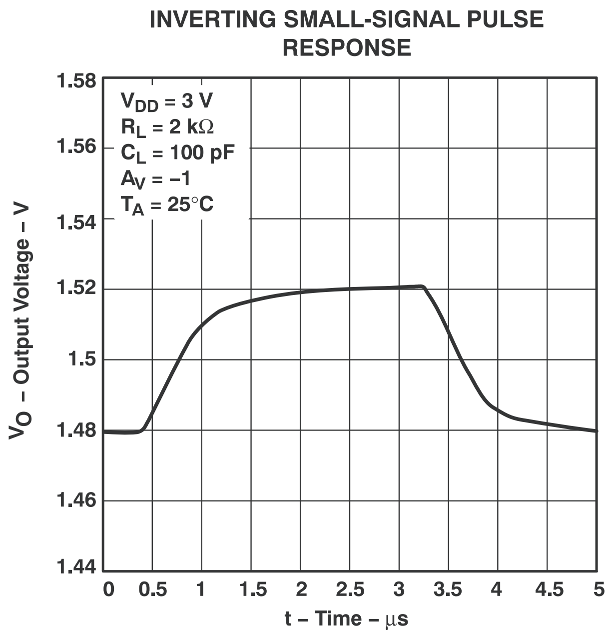


Figure 5-36.

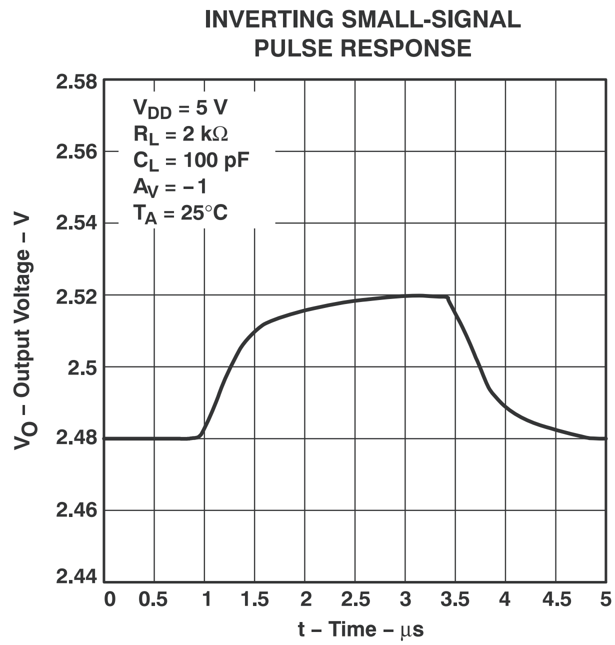


Figure 5-37.

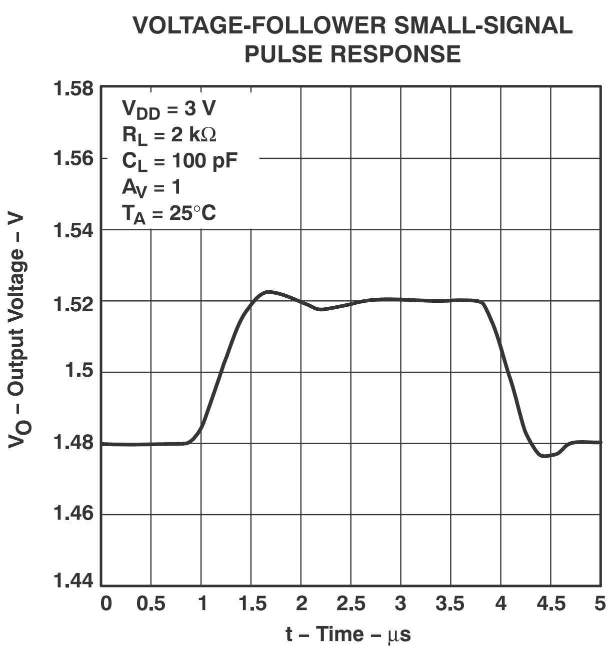


Figure 5-38.

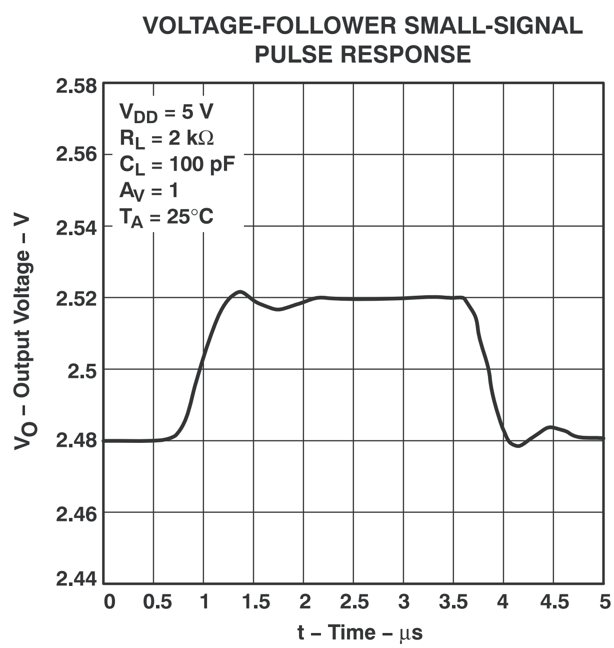


Figure 5-39.

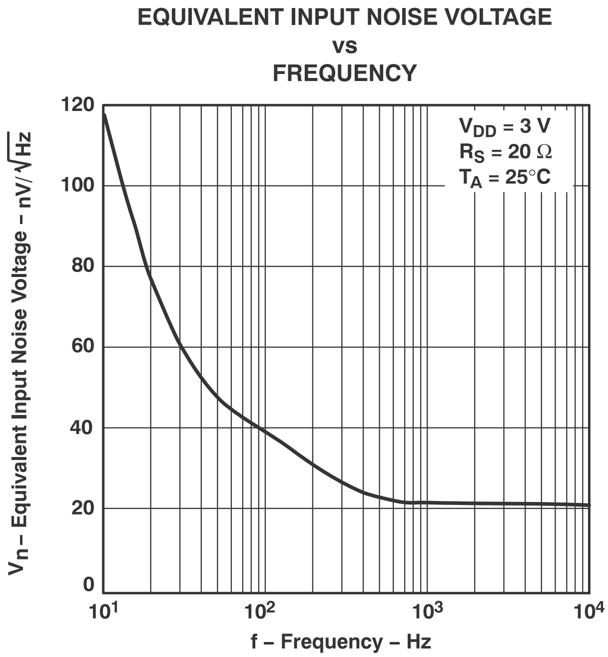


Figure 5-40.

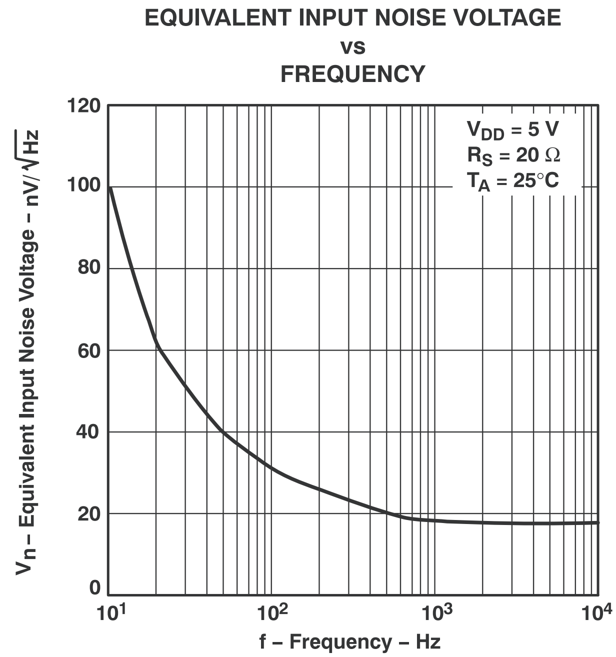


Figure 5-41.

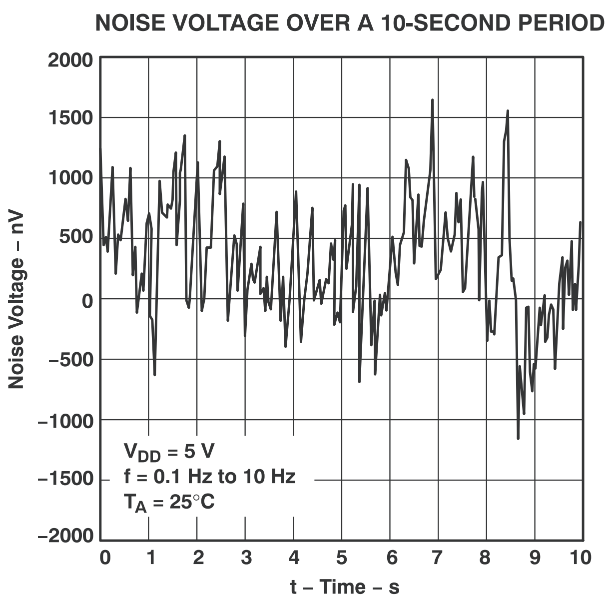


Figure 5-42.

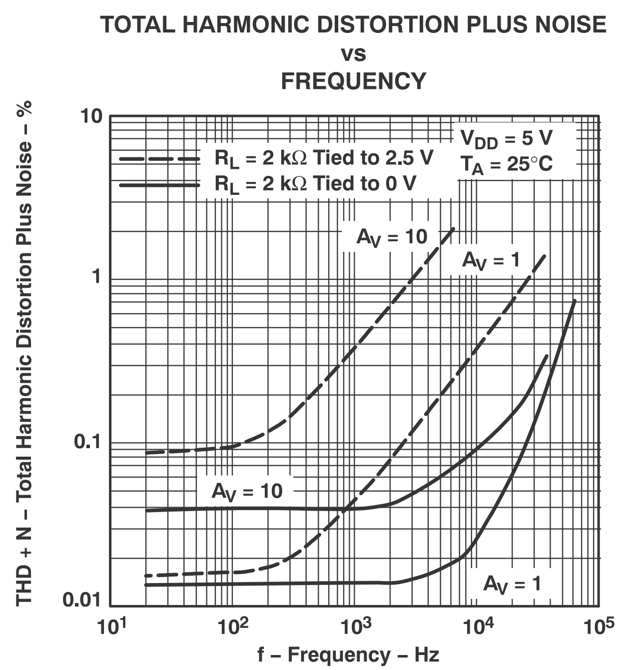


Figure 5-43.

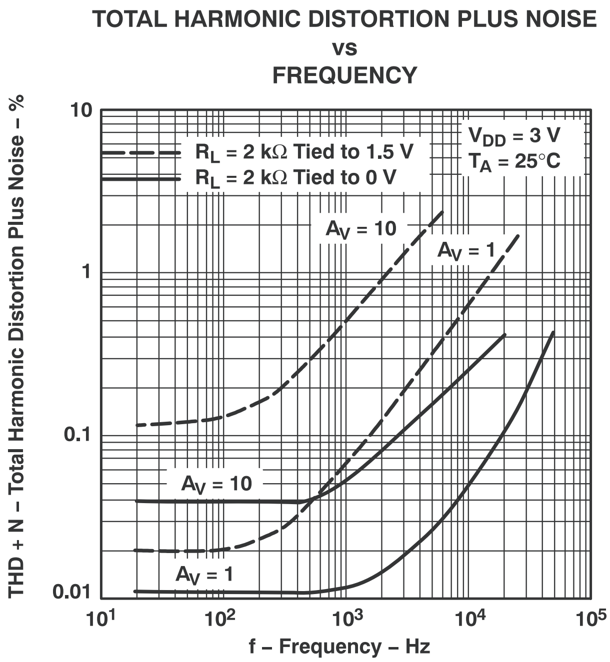


Figure 5-44.

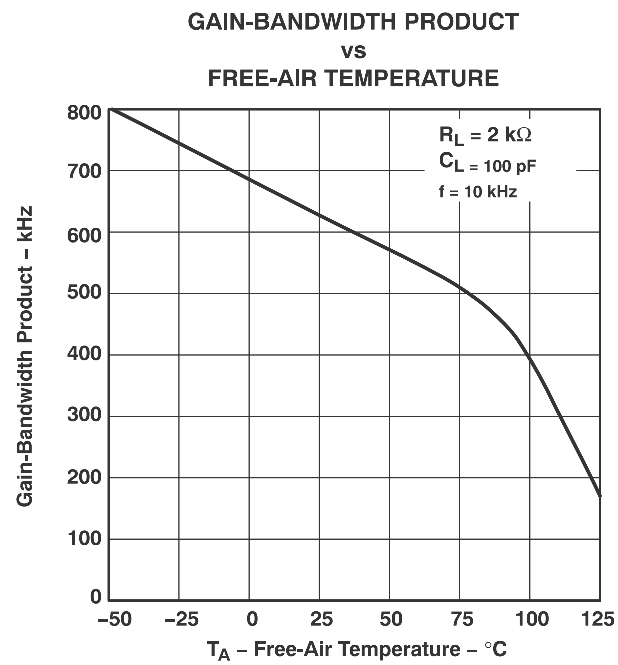


Figure 5-45.

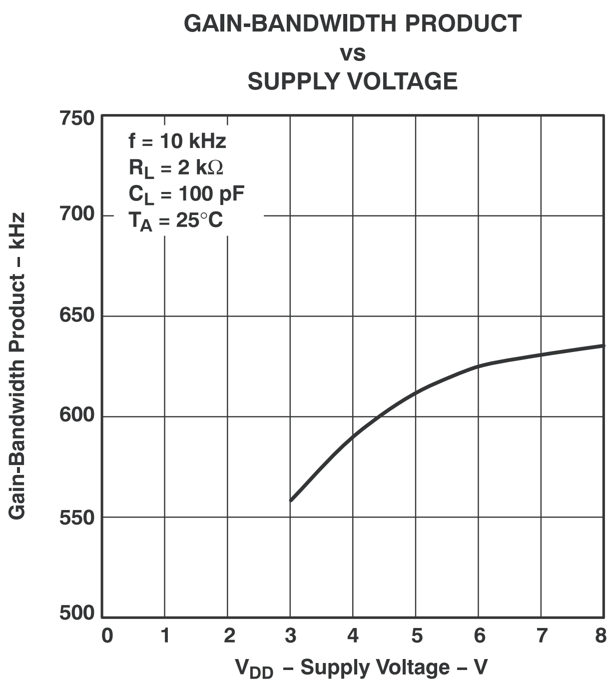


Figure 5-46.

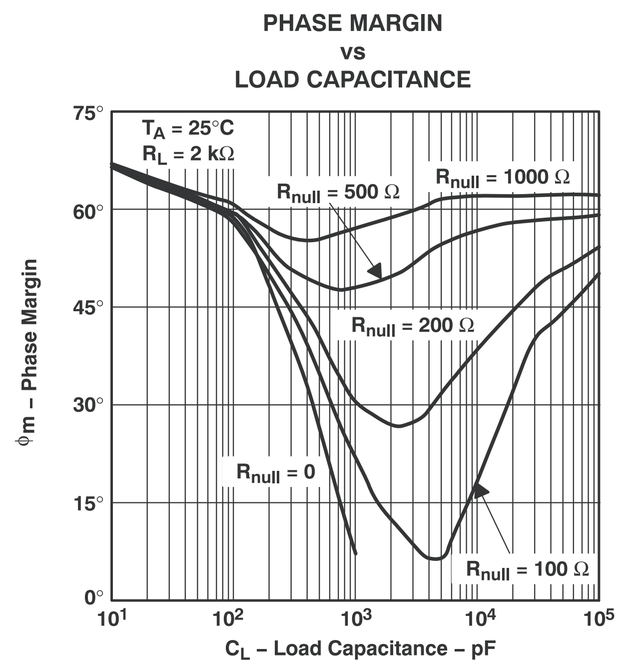


Figure 5-47.

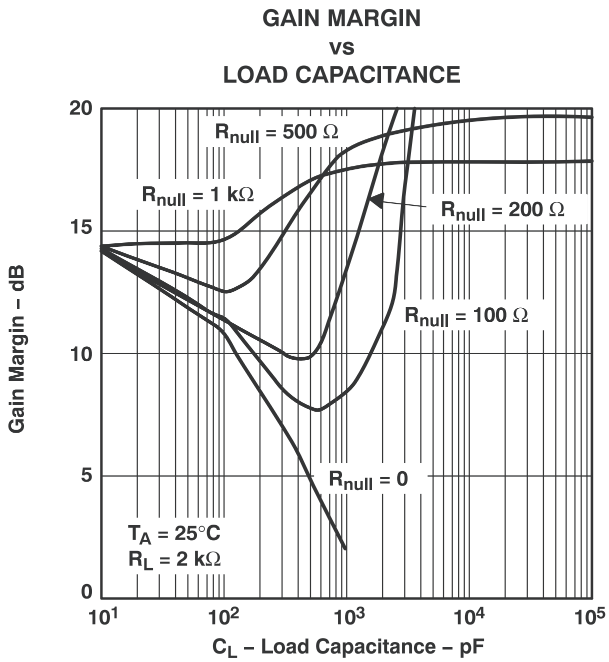


Figure 5-48.

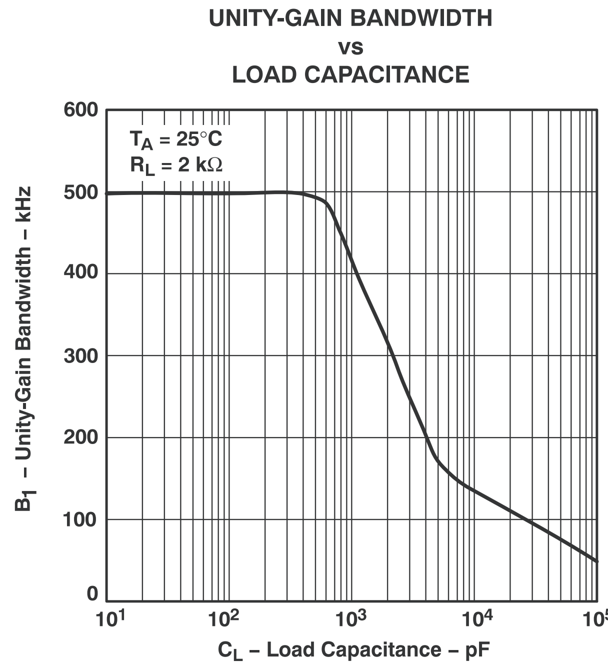


Figure 5-49.

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

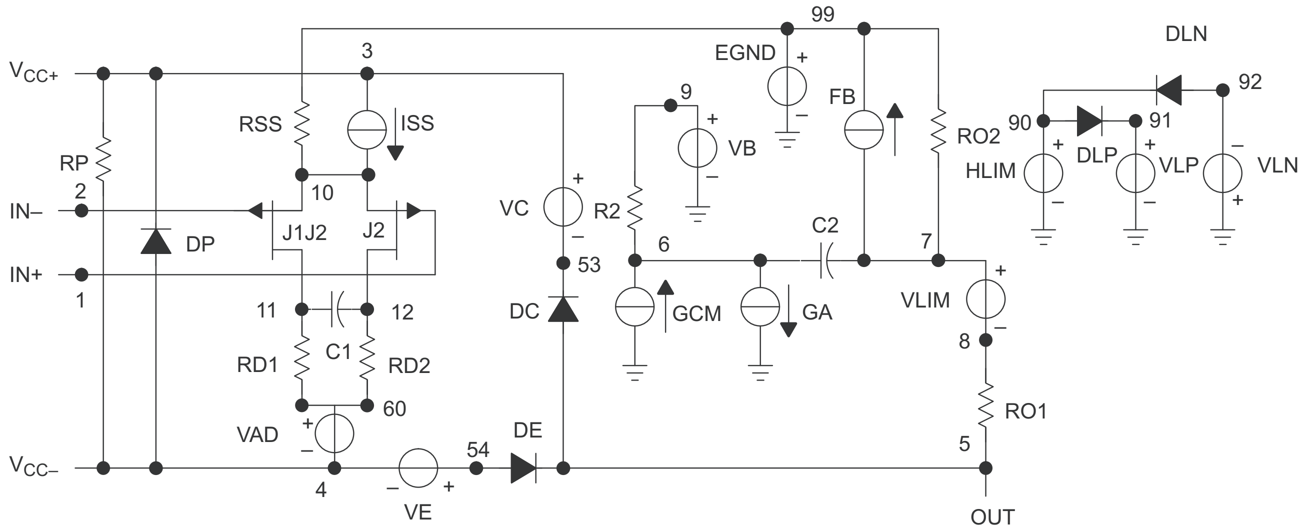
6.1 Application Information

6.1.1 Macromodel Information

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel [1]and subcircuit in Figure 6-1 were generated using the TLV243x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

[1] G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).




```
.SUBCKT TLV2432 1 2 3 4 5
C1      11   12   3.560E–12
C2      6    7    15.00E–12
DC      5    53   DX
DE      54   5    DX
DLP     90   91   DX
DLN     92   90   DX
DP      4    3    DX
EGND    99   0    POLY (2) (3,0) (4,0) 0 .5 .5
FB      7    99   POLY (5) VB VC VE VLP
+ VLN 0 21.04E6 –30E6 30E6 30E6 –30E6
GA      6    0    11   12 47.12E–6
GCM     0    6    10   99 4.9E–9
ISS     3    10   DC 8.250E–6
HLIM    90   0    VLIM 1K
J1      11   2    10 JX
J2      12   1    10 JX
R2      6    9    100.0E3
RD1     60   11   21.22E3
RD2     60   12   21.22E3
R01     8    5    120
R02     7    99   120
RP      3    4    26.04E3
RSS     10   99   24.24E6
VAD     60   4    –.6
VB      9    0    DC 0
VC      3    53   DC .65
VE      54   4    DC .65
VLIM    7    8    DC 0
VLP     91   0    DC 1.4
VLN     0    92   DC 9.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=281E–6
+ VTO=–.065)
.ENDS
```

Figure 6-1. Boyle Macromodel and Subcircuit

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

Advanced LinCMOS™ and TI E2E™ are trademarks of Texas Instruments.
Microsim Parts™ is a trademark of MicroSim.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2011) to Revision C (July 2025) — **Page**

- Updated the numbering, formatting, tables, figures and cross-references throughout the document to reflect modern datasheet standards.................... 1
- Deleted the TLV2434-Q1 preview device from *Ordering Information*.................... 2
- Changed *Electrical Characteristics: V_{DD} = 3 V* common-mode rejection ratio minimum value from: 70dB to: 63dB.................... 4
- Changed *Electrical Characteristics: V_{DD} = 3 V* supply current (per channel) typical value for 25°C from: 98μA to: 115μA.................... 4
- Changed *Electrical Characteristics: V_{DD} = 3 V* supply current (per channel) maximum value for 25°C from: 125μA to: 150μA.................... 4
- Changed *Electrical Characteristics: V_{DD} = 3 V* supply current (per channel) maximum value for the full temperature range from: 130μA to: 175μA.................... 4
- Changed *Electrical Characteristics: V_{DD} = 5 V* common-mode rejection ratio minimum value from: 70dB to: 63dB.................... 6
- Changed *Electrical Characteristics: V_{DD} = 5 V* supply current (per channel) typical value for 25°C from: 100μA to: 115μA.................... 6
- Changed *Electrical Characteristics: V_{DD} = 5 V* supply current (per channel) maximum value for 25°C from: 125μA to: 150μA.................... 6

- Changed *Electrical Characteristics: V_{DD} = 5 V* supply current (per channel) maximum value for full temperature range from: 135µA to: 175µA..........6

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2432AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2432AQ
TLV2432AQDRQ1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TLV2432AQDRQ1	2432AQ
TLV2432QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2432Q1
TLV2432QDRG4Q1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TLV2432QDRG4Q1	2432Q1
TLV2434AQDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2434AQ
TLV2434AQDRQ1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TLV2434AQDRQ1	2434AQ
TLV2434AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2434AQ
TLV2434AQPWRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	NIPDAU	Level-3-260C-168 HR	See TLV2434AQPWRQ1	2434AQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

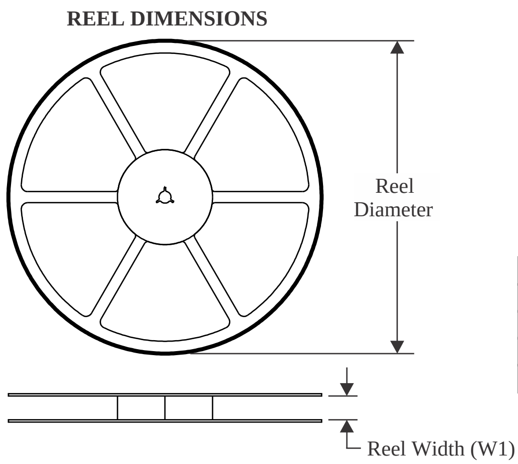
OTHER QUALIFIED VERSIONS OF TLV2432-Q1, TLV2432A-Q1, TLV2434A-Q1 :

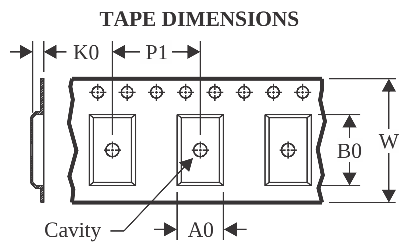
- Catalog : TLV2432, TLV2432A, TLV2434A

NOTE: Qualified Version Definitions:

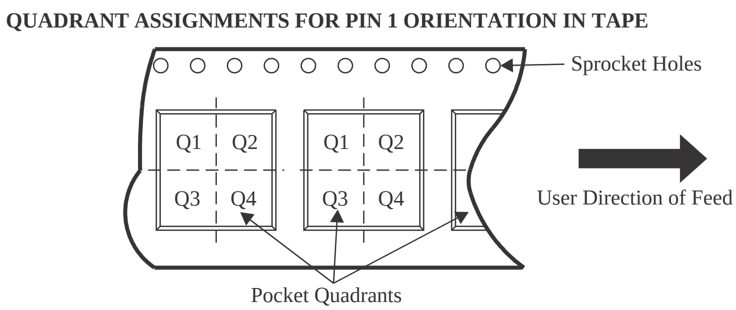
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





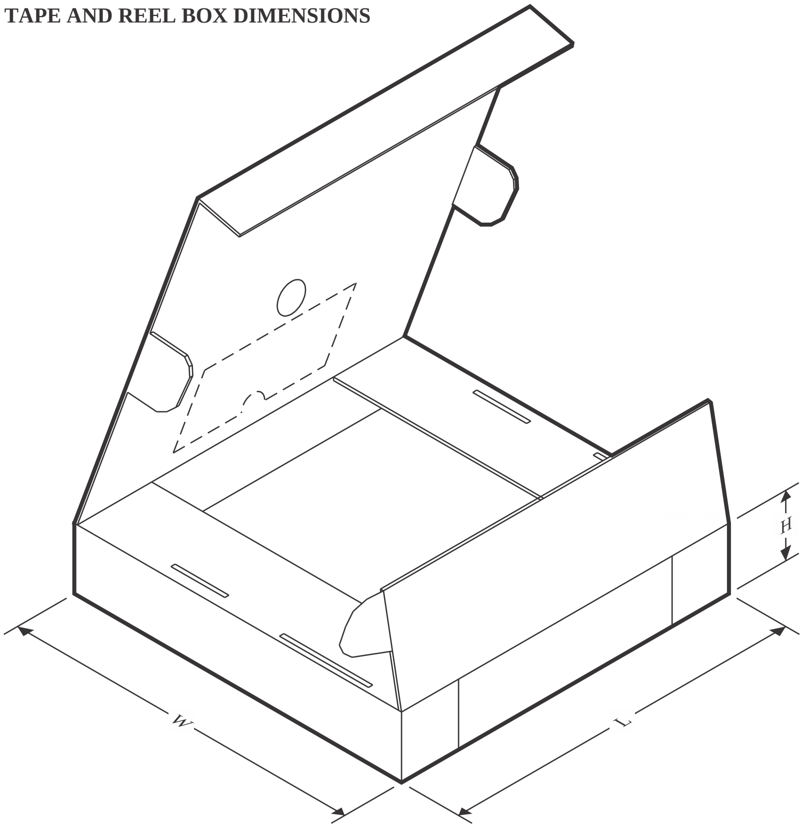
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

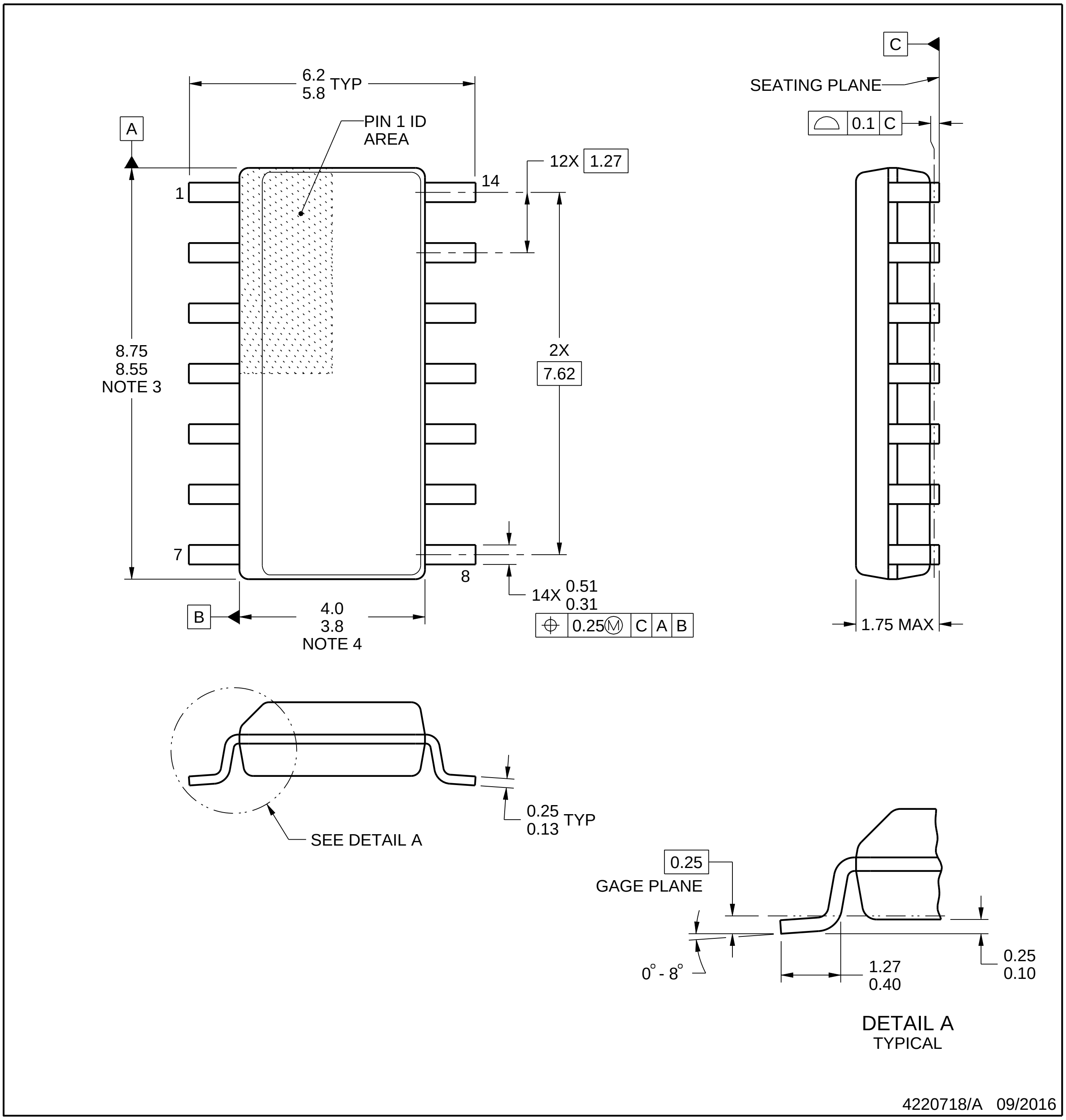
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2434AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2434AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



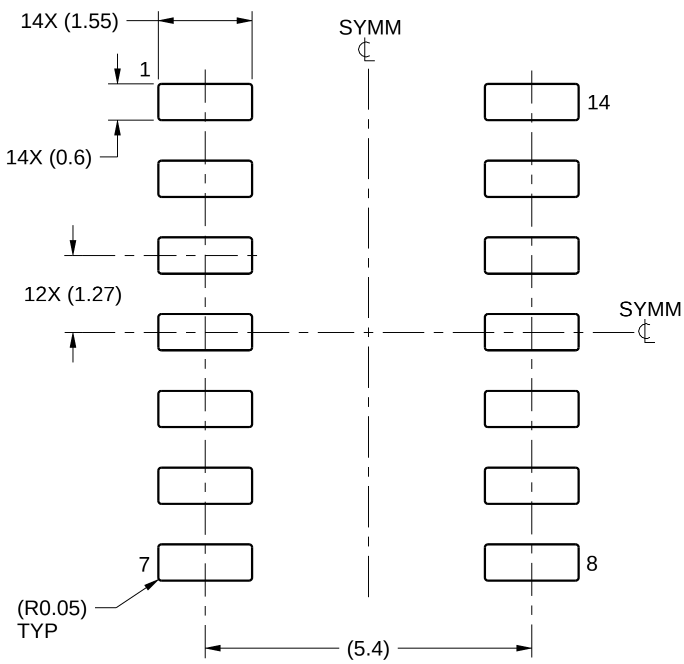
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2434AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2434AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

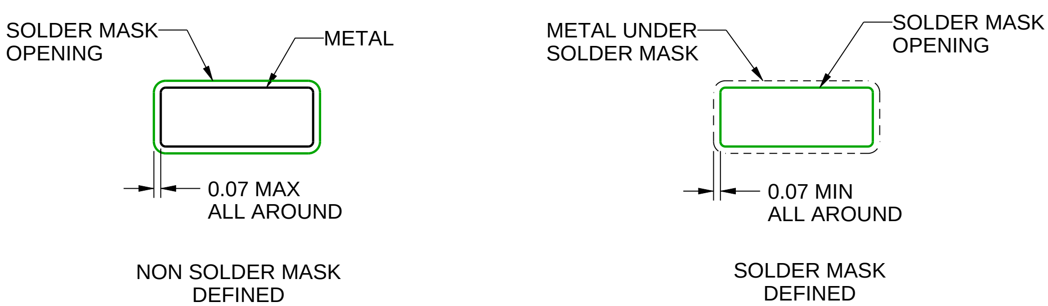


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

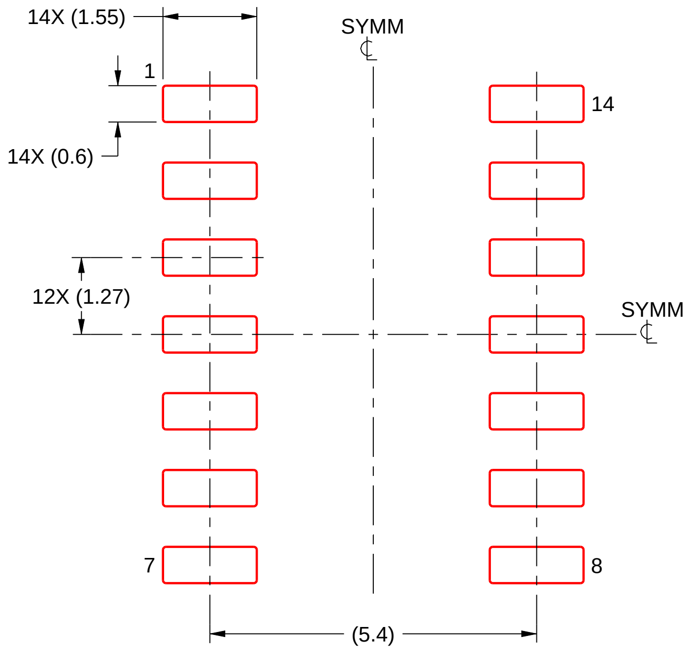


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

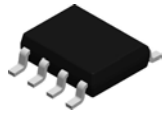


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

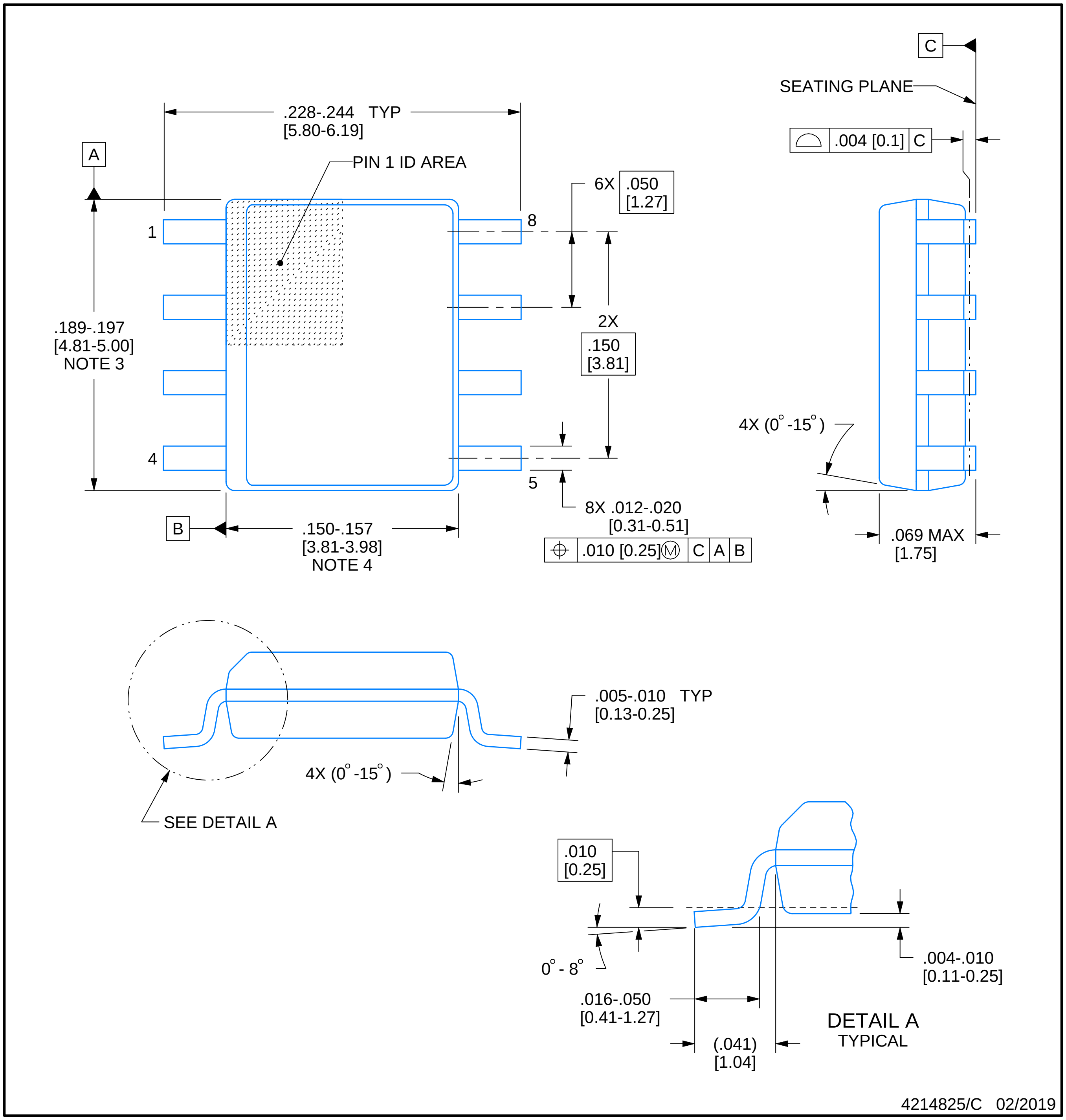


PACKAGE OUTLINE

D0008A

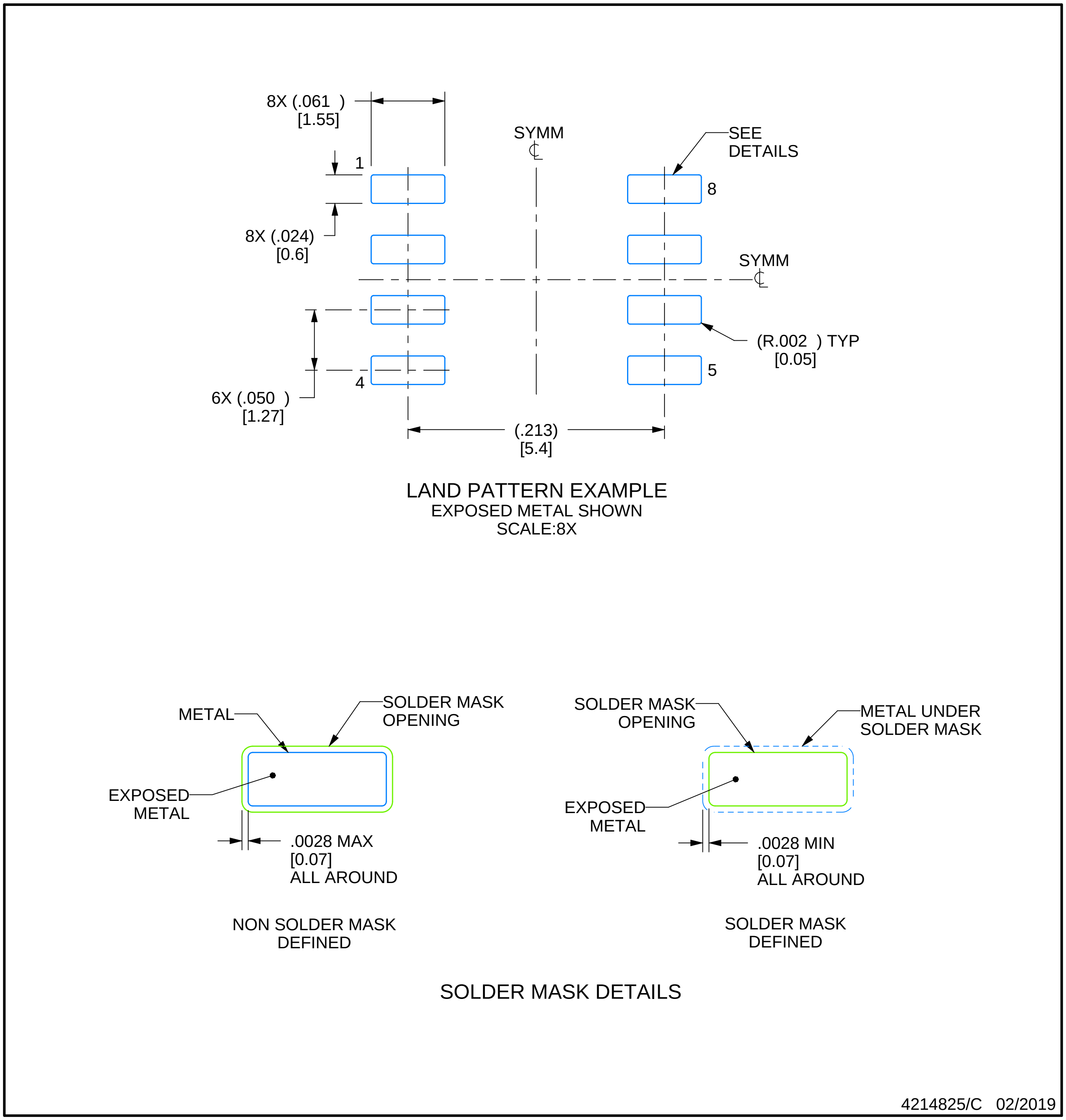
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



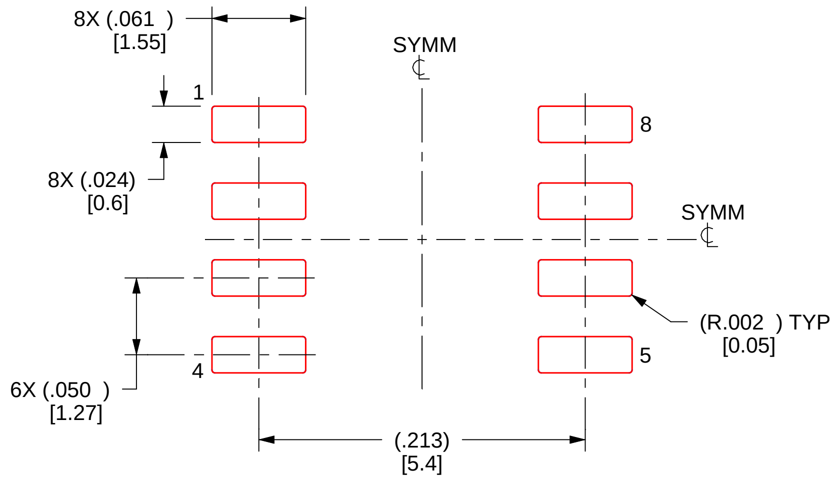
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

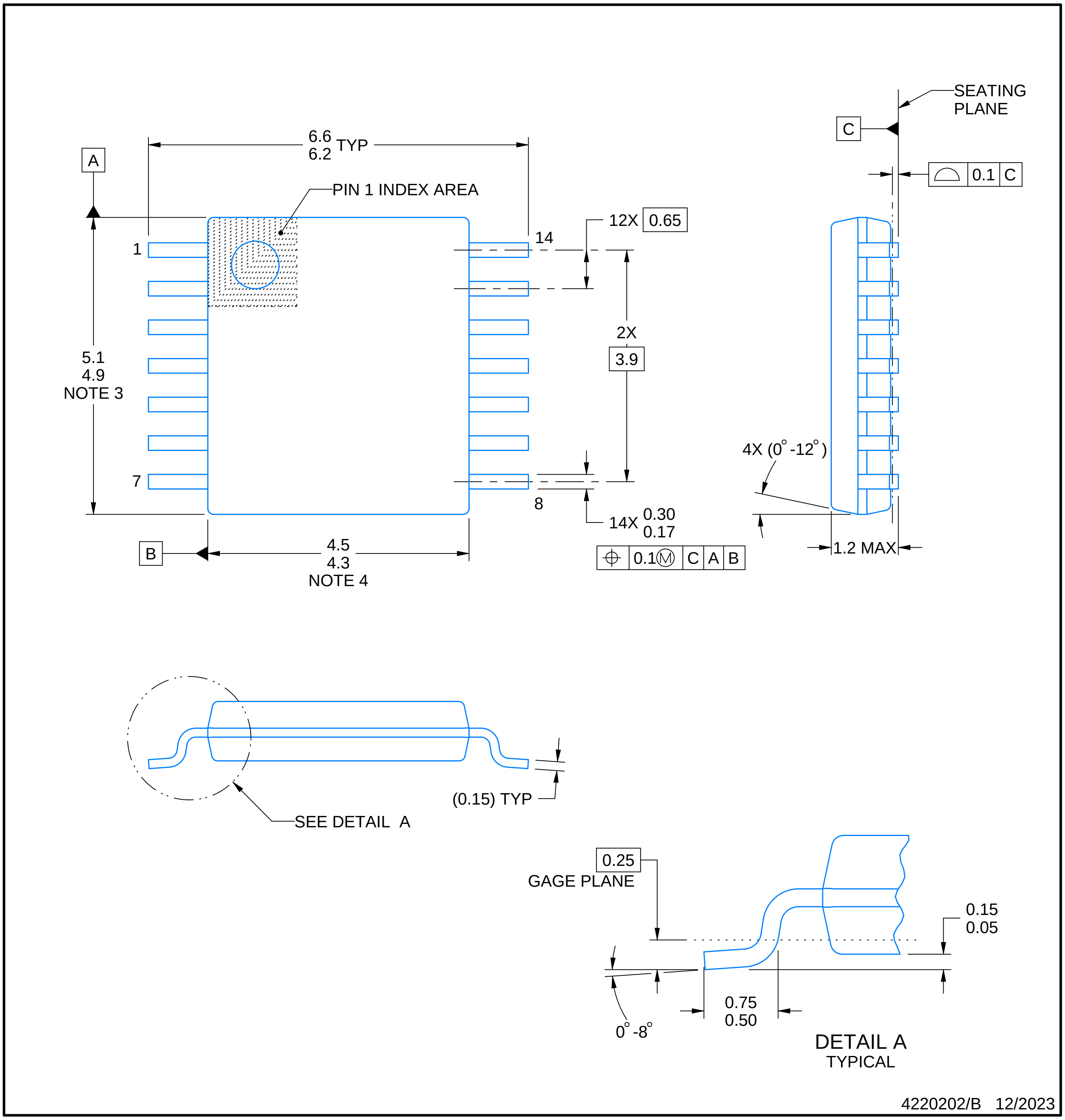


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

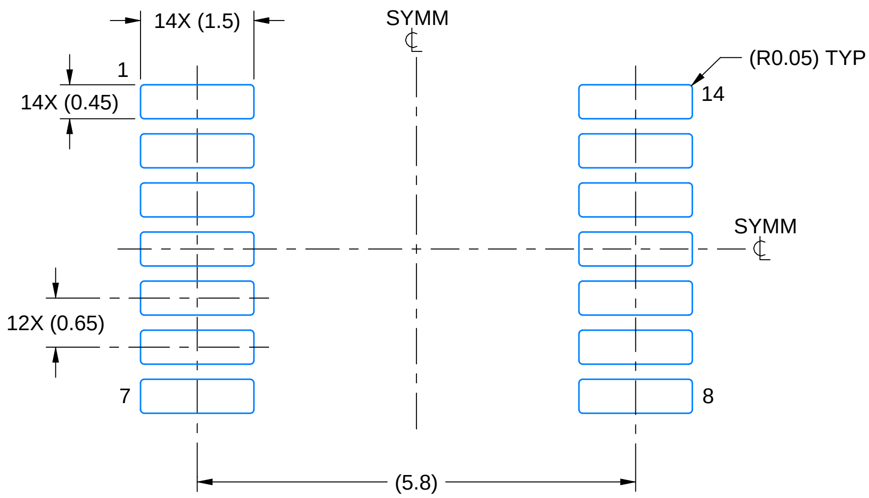
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

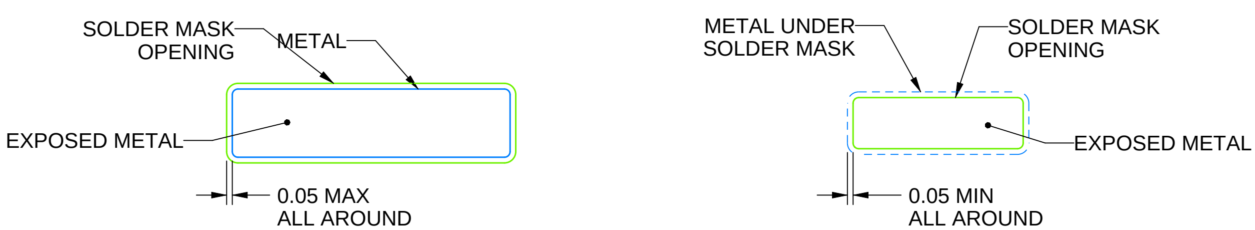


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

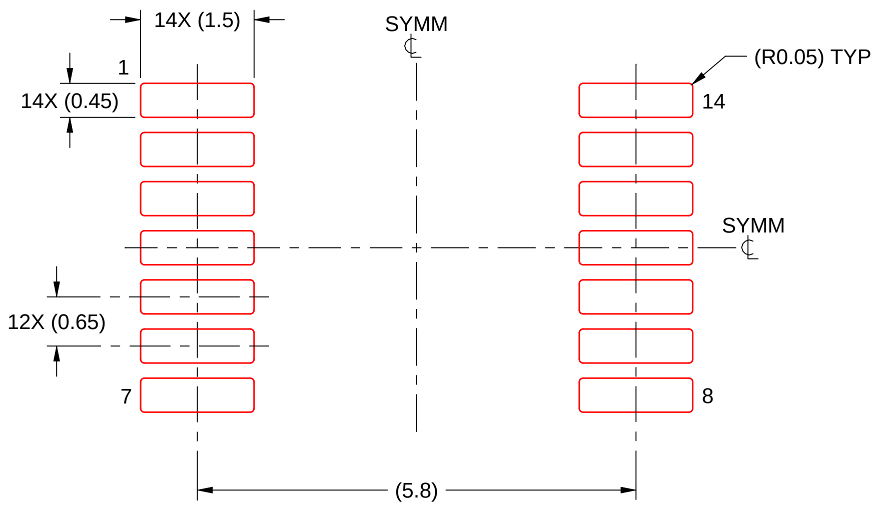
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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