

DS80EP100 5 to 12.5 Gbps, Power-Saver Equalizer for Backplanes and Cables

Check for Samples: [DS80EP100](#)

FEATURES

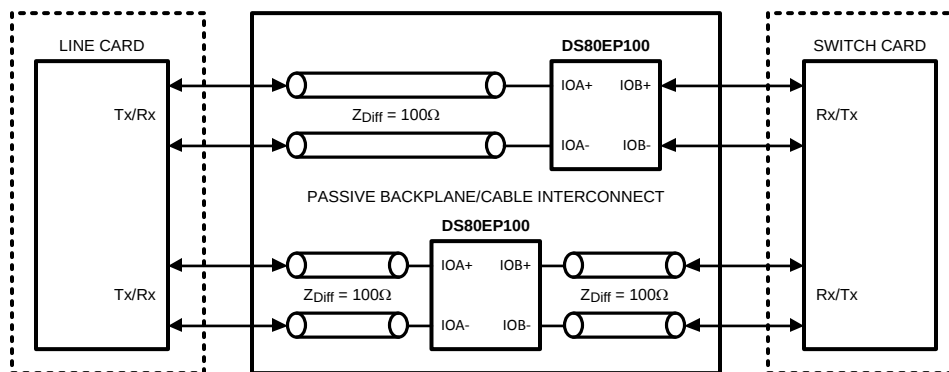
- 5 to 12.5 Gbps Operation
- No Power or Ground Required
- Equalization Effective Anywhere in Data Path
- Equalizes CML, LV-PECL, LVDS Signals
- Symmetric I/O Structures Provide Equal Boost for Bi-directional Operation
- 7 dB Maximum Boost
- Code Independent, 8b/10b or Scrambled
- Supports Both Bi-level and Multi-level Signaling
- Extends Reach Over Backplanes and Cables
- Compatible with PCI-Express Gen1 and Gen2
- Compatible with XAU1
- Will Operate in Series with Existing Active Equalizer
- Easy to Handle 6 Pin WSON

DESCRIPTION

TI's Power-saver equalizer compensates for transmission medium losses and minimizes medium-induced deterministic jitter. Performance is guaranteed over the full range of 5 to 12.5 Gbps. The DS80EP100 requires no power to operate. The equalizer operates anywhere in the data path to minimize media-induced deterministic jitter in both FR4 traces and cable applications. Symmetric I/O structures support full duplex or half duplex applications. Linear compensation is provided independent of line coding or protocol. The device is ideal for both bi-level and multi-level signaling.

The equalizer is available in a 6 pin leadless WSON package with a space saving 2.2 mm X 2.5 mm footprint. This tiny package provides maximum flexibility in placement and routing of the Power-saver equalizer.

Simplified Application Diagram



Note: The DS80EP100 provides the flexibility of passing the data from either side of the device. It can be placed anywhere in the data path.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2007–2013, Texas Instruments Incorporated

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O Type ⁽¹⁾	Description
High speed differential I/O			
IOA- IOA+	3 1	I/O	Symmetric differential I/O
IOB- IOB+	4 6	I/O	Symmetric differential I/O
NC Exposed Pad	2, 5 DAP	N/A	Reserved. Do not connect.

(1) I = Input / O = Output

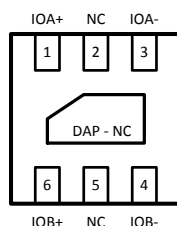
Connection Diagram

Figure 1. Bottom View
2.2mm x 2.5mm 6-Pin WSON Package
See Package Number NHK0014A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾⁽²⁾

INPUT/OUTPUT	(IOA+ and IOB+) or (IOA- and IOB-)	+2V
	(IOA+ and IOA-) or (IOB+ and IOB-)	+4V
	(IOA+ and IOB-) or (IOA- and IOB+)	+4V
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature Soldering, 4 sec		+260°C
ESD Rating	HBM, 1.5 kΩ, 100 pF	1.3kV

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Ambient Temperature	-40	25	+85	°C
Bit Rate	5		12.5	Gbps

Electrical Characteristics ⁽¹⁾

Over recommended operating conditions unless other specified. All parameters are guaranteed by test, statistical analysis or design.

Symbol	Parameter	Conditions	Min	Typ ⁽²⁾	Max	Units
V _{IN}	Input voltage swing	See ⁽³⁾		1000	3600	mVp-p
	Equalization	6.25 GHz relative to 100MHz		6		dB
R _{LI}	Differential input return loss	100 MHz – 6.25 GHz, with fixture's effect de-embedded		15		dB
R _{LO}	Differential output return loss	100 MHz – 6.25 GHz, with fixture's effect de-embedded IOA+, or IOB+ = static high.		15		dB
R _{IN}	Input Impedance	Differential across IOA+ and IOA-, or IOB+ and IOB-, Z _{LOAD} = 100Ω		100		Ω
R _O	Output Impedance	Differential across IOA+ and IOA-, or IOB+ and IOB-, Z _{SOURCE} = 100Ω		100		Ω
	Through Response	Relative to ideal load, see Figure 3 for setup	See Figure 4 and Table 1 for limits			
R1	Resistance IOA+ to IOA- and IOB+ to IOB-	No load, high impedance on all ports		150		Ω
R2	Resistance IOA+ to IOB+ and IOA- to IOB-	No load, high impedance on all ports		50		Ω
R3	Resistance IOA+ to IOB- and IOA- to IOB+	No load, high impedance on all ports		150		Ω
	DC Gain (IOA/IOB or IOB/IOA)	Z _{LOAD} = 100Ω		0.4		
DJ1	Residual deterministic jitter	5 Gbps, 20 in of 6mil microstrip FR4 See ⁽⁴⁾		0.15		Ulp-p
DJ2	Residual deterministic jitter	6.25 Gbps, 20 in of 6mil microstrip FR4 See ⁽⁴⁾ ⁽⁵⁾		0.15	0.20	Ulp-p
DJ3	Residual deterministic jitter	8 Gbps, 20 in of 6mil microstrip FR4 See ⁽⁴⁾ ⁽⁵⁾		0.15	0.20	Ulp-p
DJ4	Residual deterministic jitter	10 Gbps, 20 in of 6mil microstrip FR4 See ⁽⁴⁾		0.15		Ulp-p
DJ5	Residual deterministic jitter	12.5 Gbps, 14 in of 6mil microstrip FR4 See ⁽⁴⁾		0.15		Ulp-p

- (1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
- (2) Typical values represent most likely parametric norms, TA = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
- (3) Differential signal to Equalizer, measured at the input to a transmission line, see point A of [Figure 2](#). The transmission line is Z₀ = 100Ω, 6-mil, microstrip in FR4 material.
- (4) Deterministic jitter is measured at the differential outputs (point C of [Figure 2](#)), minus the deterministic jitter before the test channel (point A of [Figure 2](#)). Test pattern: PRBS- 7 .
- (5) Specification is guaranteed by characterization and is not tested in production.

TEST SETUP DIAGRAMS

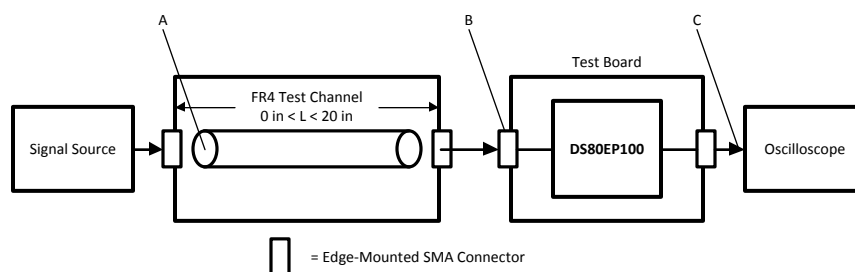


Figure 2. Transient Test Setup Diagram

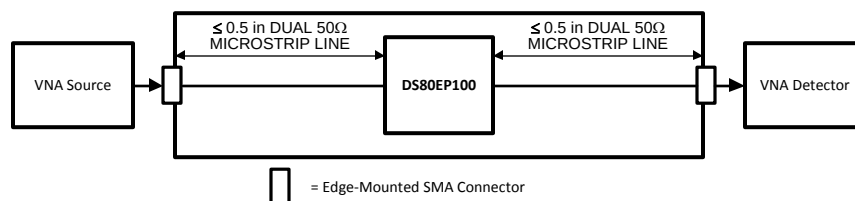


Figure 3. Frequency Response Test Circuit

Typical Equalizer Transfer Function

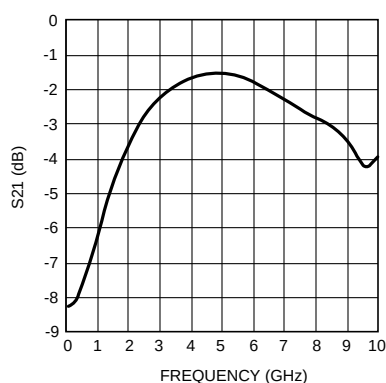


Figure 4. Typical Equalizer Transfer Function

Table 1. Typical Through Response

Frequency (GHz)	DS80EP100 Attenuation Typ (dB)
0.1	-8.25
0.5	-7.64
1	-6.12
1.5	-4.68
2	-3.57
3	-2.22
4	-1.66
5	-1.53
6	-1.77
7	-2.28
8	-2.8
9	-3.47
10	-3.91

Block Diagram

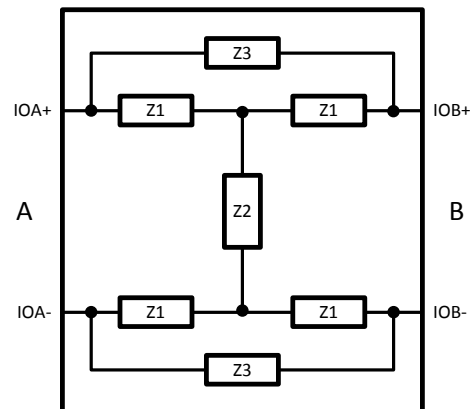


Figure 5. Simplified Block Diagram

APPLICATION INFORMATION

DS80EP100 DEVICE DESCRIPTION

The DS80EP100 Power-Saver equalizer is a passive network circuit composed of resistive, capacitive, and inductive components (See [Figure 5](#)). A Differential bridged T-network compensates for the transmission medium losses and minimizes medium-induced deterministic jitter with FR4 and cables. The equalizer attenuates low frequency signals and is a bandpass filter at the resonant frequency. The response is linear and symmetric.

I/O TERMINATIONS

The DS80EP100 I/O impedance is 100Ω differential. The equalizer is designed for 100Ω-balanced differential signals and is not intended for single-ended transmission.

LINEAR COMPENSATION

The unique linear compensation feature of the DS80EP100 combined with the tiny package allows maximum flexibility in placement. The equalizer can be placed anywhere in the data path and will provide the same compensation at the receiving circuit. (See [Simplified Application Diagram](#))

SYMMETRIC I/O STRUCTURES

The symmetry of the passive equalization network allows bi-directional operation. Signals receive equal compensation regardless of the direction of data flow. (See [Figure 5](#)).

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS AND NO CONNECT PADS

The differential I/Os must have a controlled differential impedance of 100Ω. It is preferable to route all differential lines exclusively on one layer of the board. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Differential signals should be routed away from other signals and noise sources on the printed circuit board. Pin 2, Pin 5, and the center DAP have to be left as no connect. Therefore, do not connect the landing pads of these pins to the power or ground plane. See AN-1187 for additional information on the WSON package.

Typical Characteristics

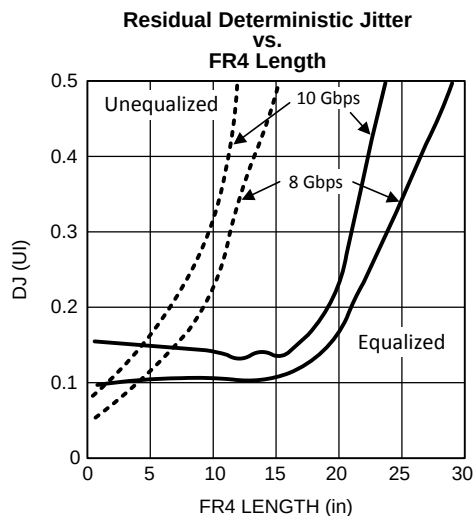


Figure 6.

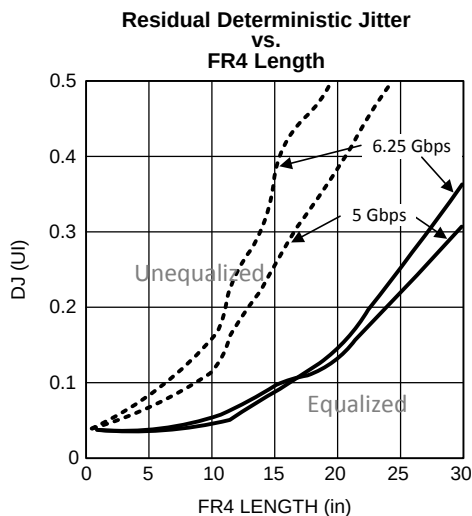


Figure 7.

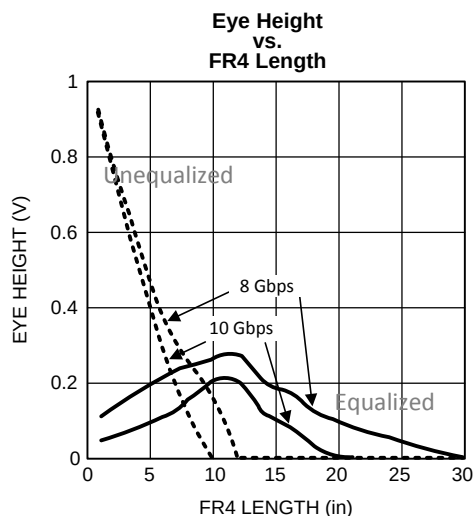


Figure 8.

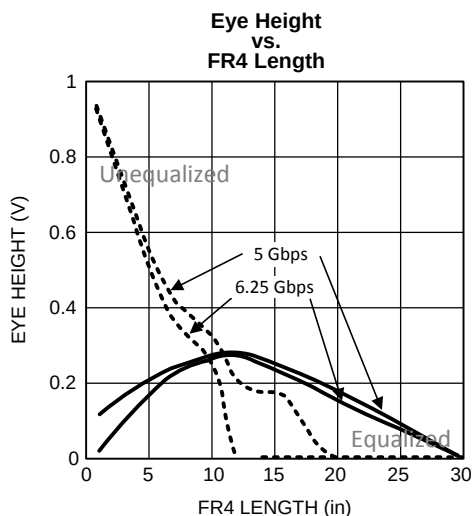
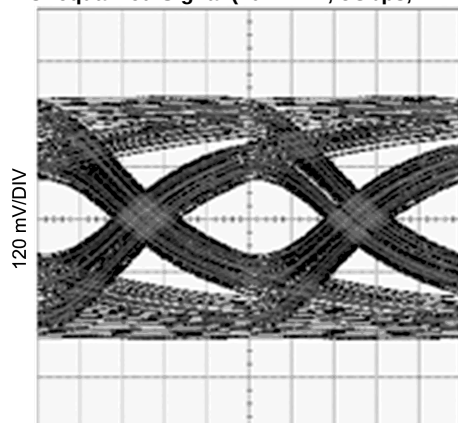


Figure 9.

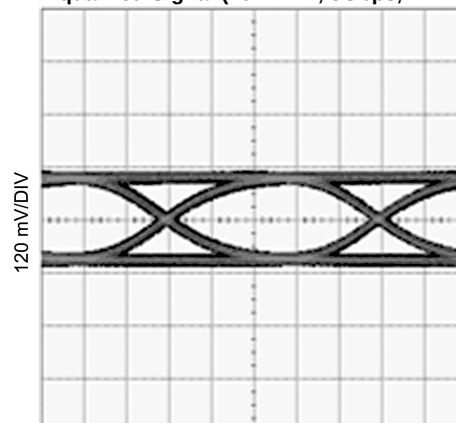
Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter

Unequalized Signal (20in FR4, 5Gbps, PRBS7)



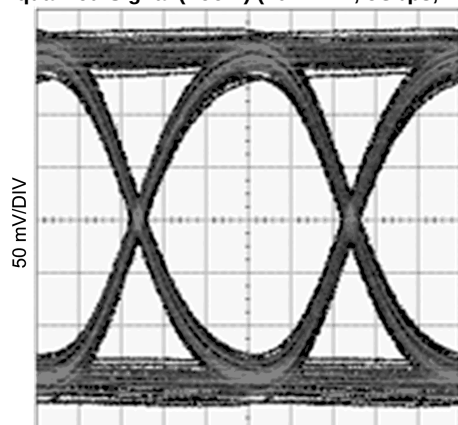
40 ps/DIV
Figure 10.

Equalized Signal (20in FR4, 5Gbps, PRBS7)



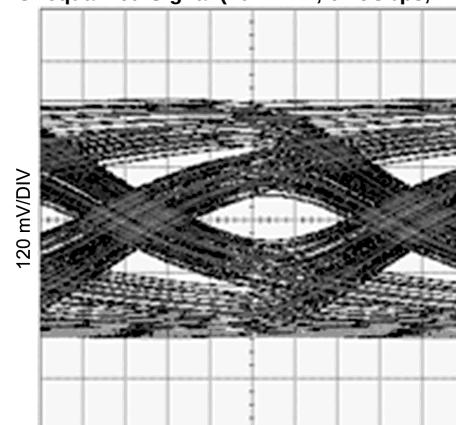
40 ps/DIV
Figure 11.

Equalized Signal (Zoom) (20in FR4, 5Gbps, PRBS7)



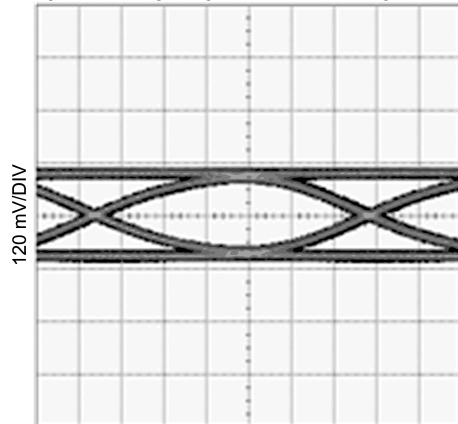
40 ps/DIV
Figure 12.

Unequalized Signal (20in FR4, 6.25Gbps, PRBS7)



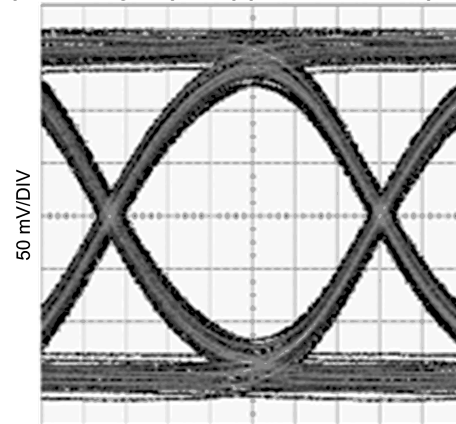
25 ps/DIV
Figure 13.

Equalized Signal (20in FR4, 6.25Gbps, PRBS7)



25 ps/DIV
Figure 14.

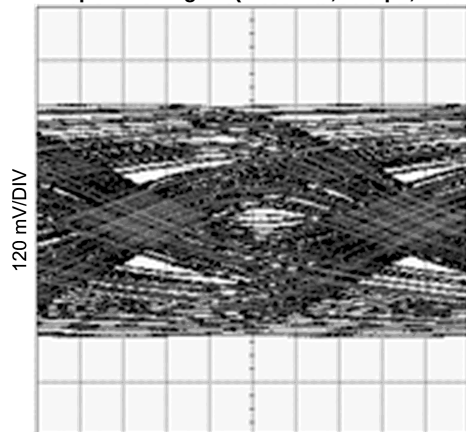
Equalized Signal (Zoom) (20in FR4, 6.26Gbps, PRBS7)



25 ps/DIV
Figure 15.

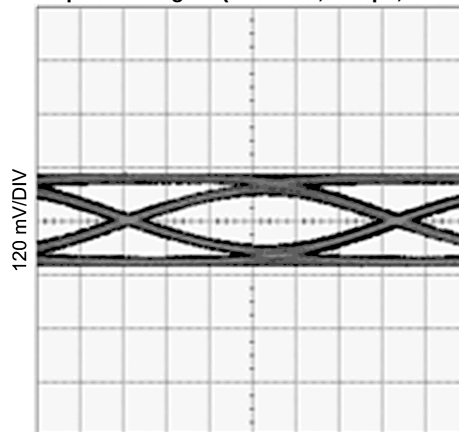
Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter (continued)

Unequalized Signal (20in FR4, 8Gbps, PRBS7)



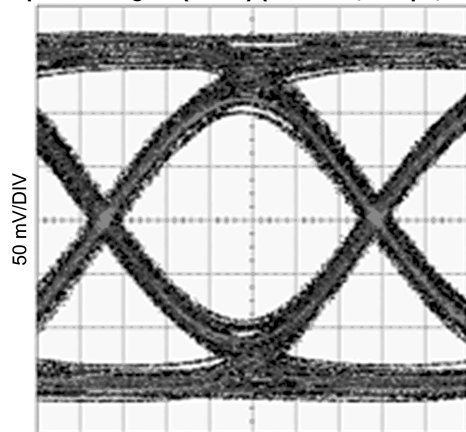
20 ps/DIV
Figure 16.

Equalized Signal (20in FR4, 8Gbps, PRBS7)



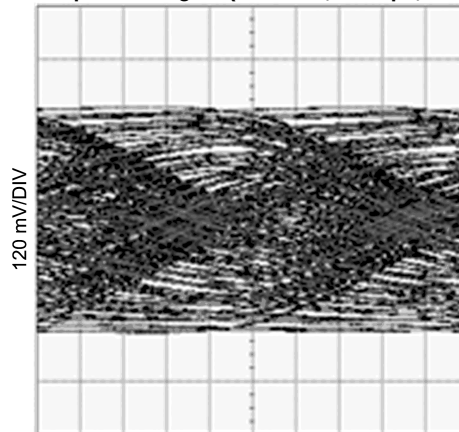
20 ps/DIV
Figure 17.

Equalized Signal (Zoom) (20in FR4, 8Gbps, PRBS7)



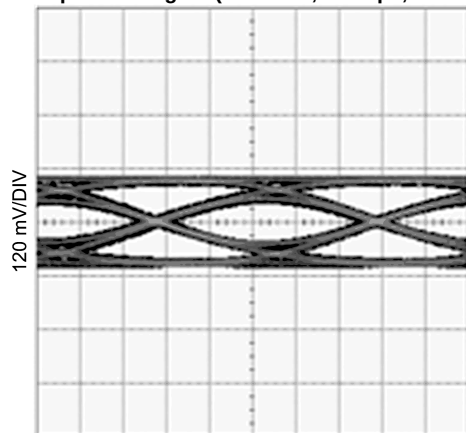
20 ps/DIV
Figure 18.

Unequalized Signal (20in FR4, 10Gbps, PRBS7)



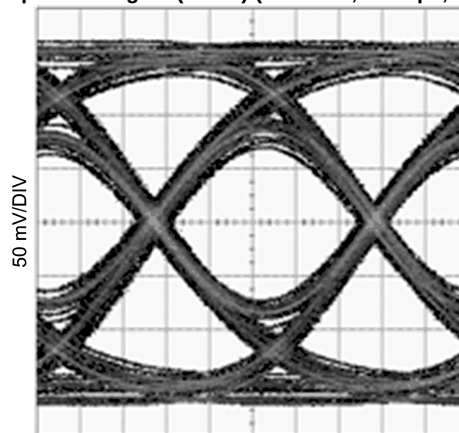
20 ps/DIV
Figure 19.

Equalized Signal (20in FR4, 10Gbps, PRBS7)



20 ps/DIV
Figure 20.

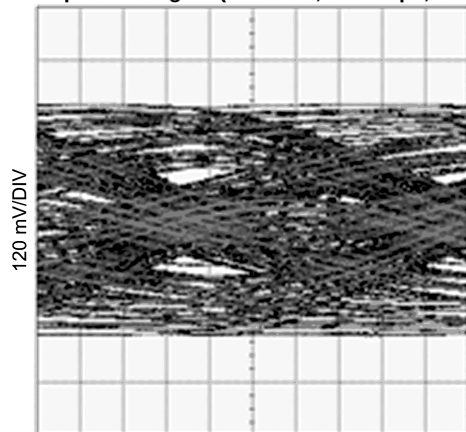
Equalized Signal (Zoom) (20in FR4, 10Gbps, PRBS7)



20 ps/DIV
Figure 21.

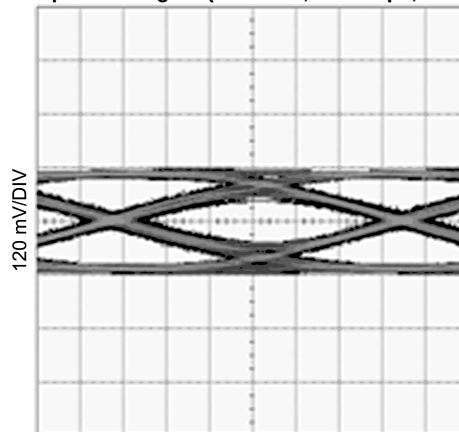
Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter (continued)

Unequalized Signal (14in FR4, 12.5Gbps, PRBS7)



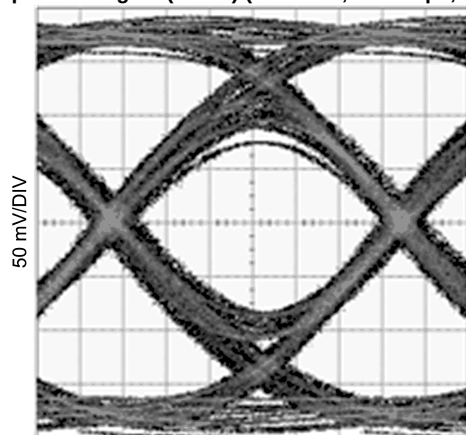
12.5 ps/DIV
Figure 22.

Equalized Signal (14in FR4, 12.5Gbps, PRBS7)



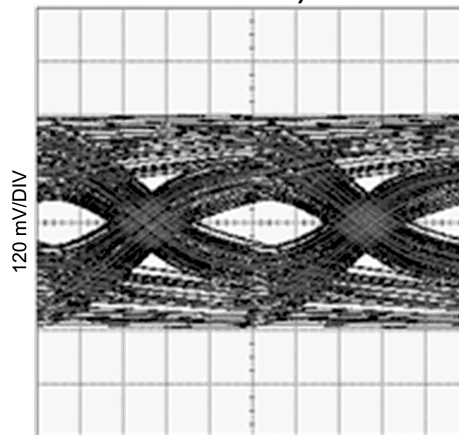
12.5 ps/DIV
Figure 23.

Equalized Signal (Zoom) (14in FR4, 12.5Gbps, PRBS7)



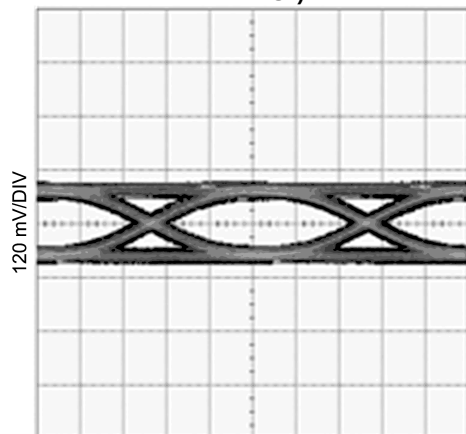
12.5 ps/DIV
Figure 24.

Unequalized Signal (5m 26AWG Twin-AX Cable, 5Gbps, PRBS7)



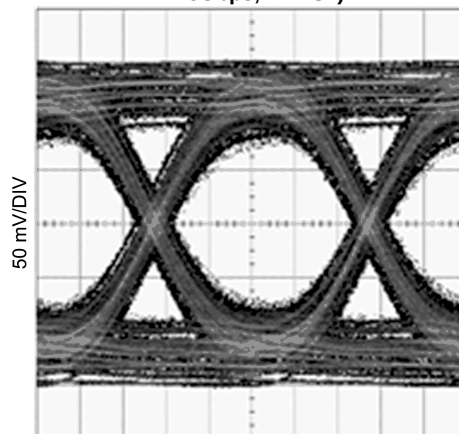
40 ps/DIV
Figure 25.

Equalized Signal (5m 26AWG Twin-AX Cable, 5Gbps, PRBS7)



40 ps/DIV
Figure 26.

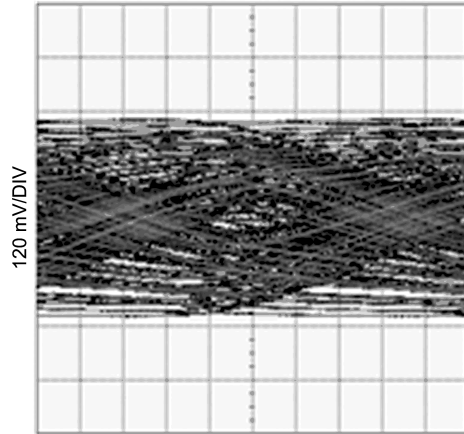
Equalized Signal (Zoom) (5m 26AWG Twin-AX Cable, 5Gbps, PRBS7)



40 ps/DIV
Figure 27.

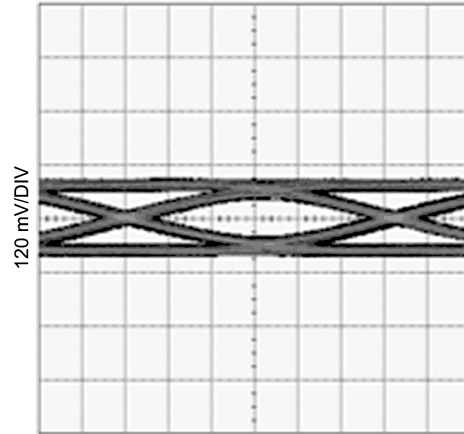
Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter (continued)

Unequalized Signal (5m 26AWG Twin-AX Cable, 8Gbps, PRBS7)



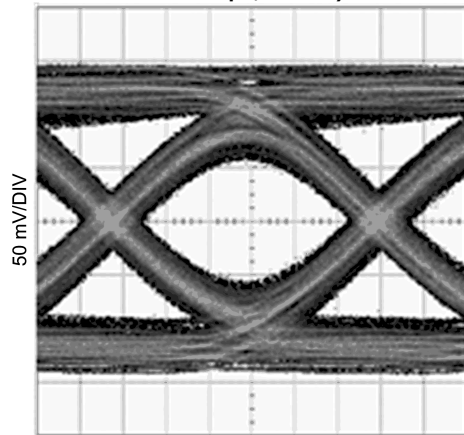
20 ps/DIV
Figure 28.

Equalized Signal (5m 26AWG Twin-AX Cable, 8Gbps, PRBS7)



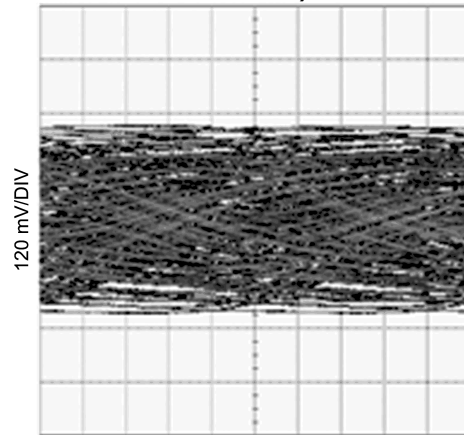
20 ps/DIV
Figure 29.

Equalized Signal (Zoom) (5m 26AWG Twin-AX Cable, 8Gbps, PRBS7)



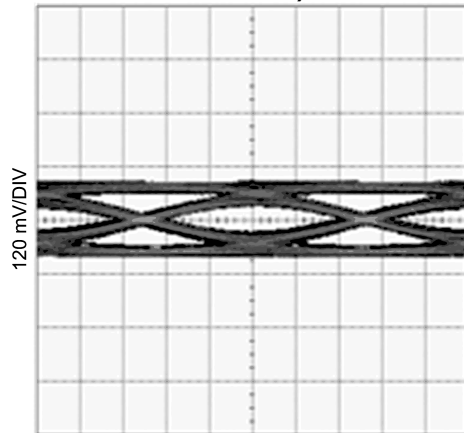
20 ps/DIV
Figure 30.

Unequalized Signal (5m 26AWG Twin-AX Cable, 10Gbps, PRBS7)



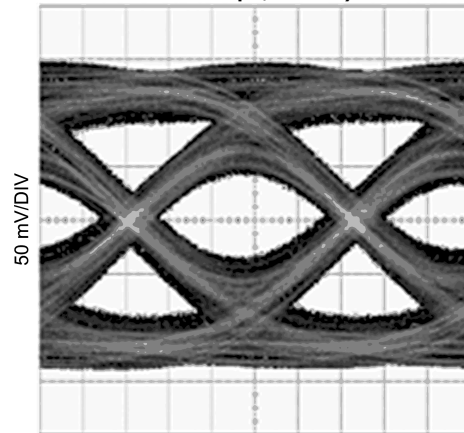
20 ps/DIV
Figure 31.

Equalized Signal (5m 26AWG Twin-AX Cable, 10Gbps, PRBS7)



20 ps/DIV
Figure 32.

Equalized Signal (Zoom) (5m 26AWG Twin-AX Cable, 10Gbps, PRBS7)



20 ps/DIV
Figure 33.

REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS80EP100SD/NOPB	Active	Production	WSO (NGF) 6	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	80S
DS80EP100SD/NOPB.A	Active	Production	WSO (NGF) 6	1000 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	80S

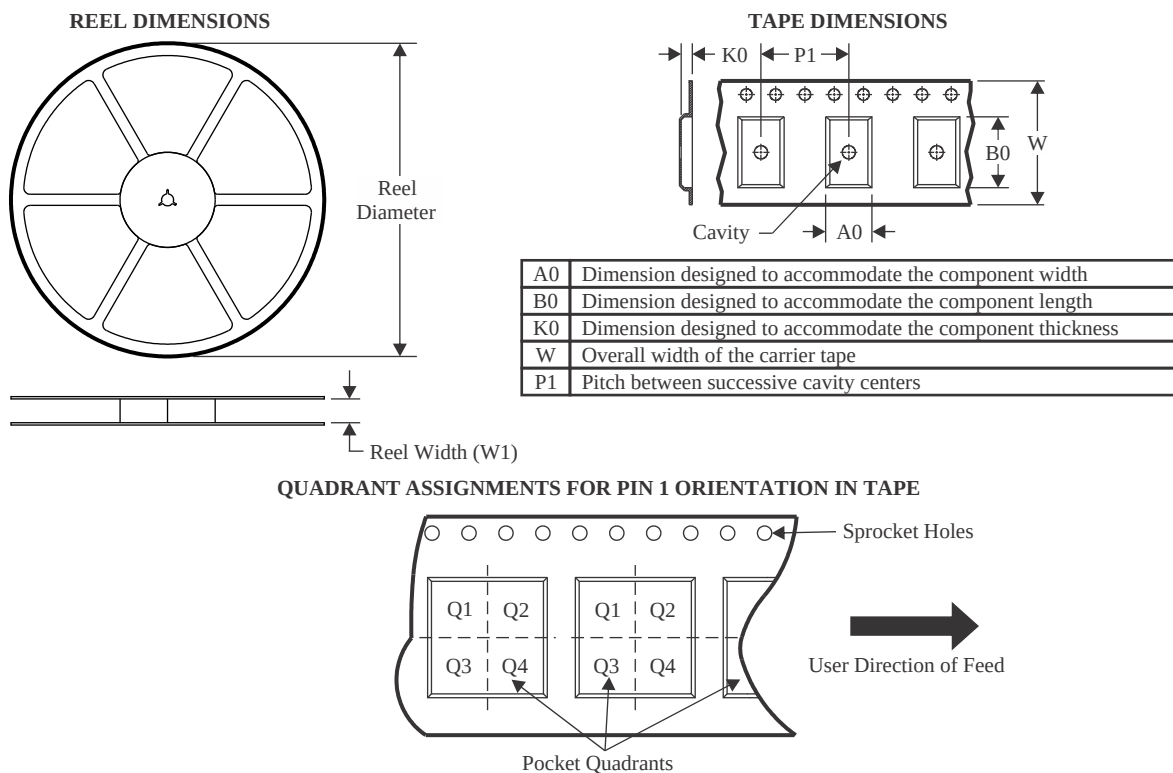
- ⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).
- ⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- ⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- ⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- ⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- ⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

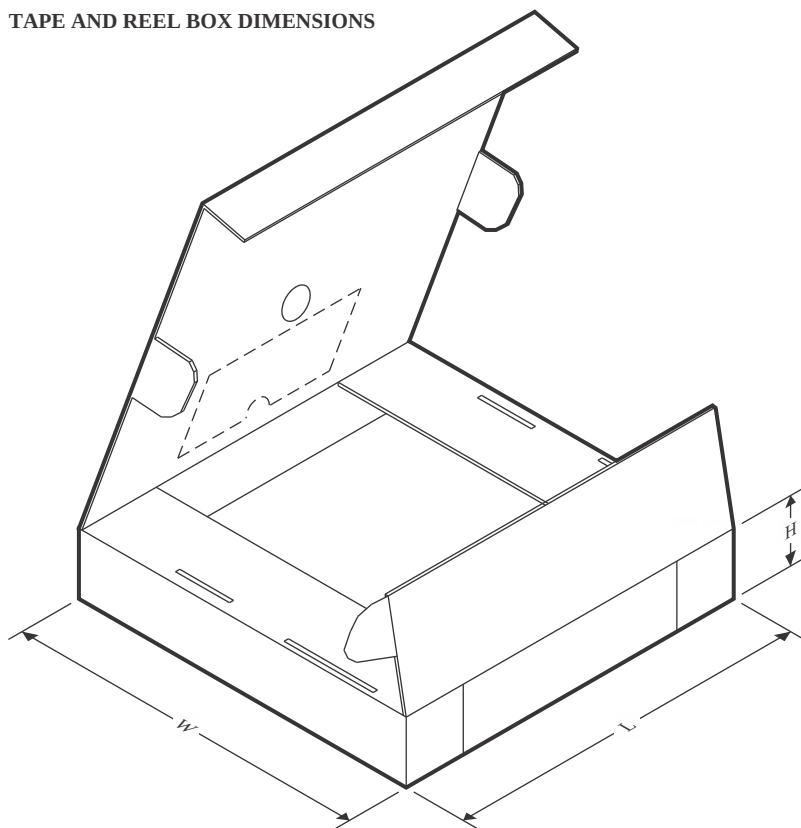
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS80EP100SD/NOPB	WSO	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1

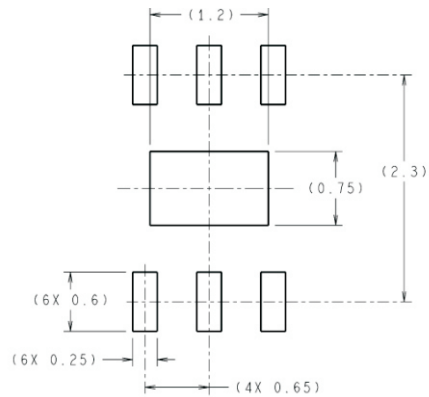
TAPE AND REEL BOX DIMENSIONS



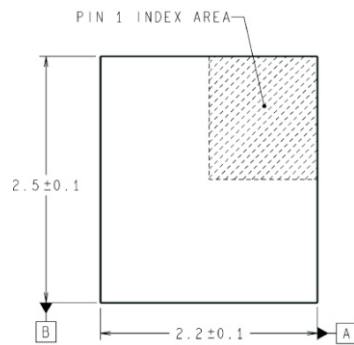
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS80EP100SD/NOPB	WS0N	NGF	6	1000	210.0	185.0	35.0

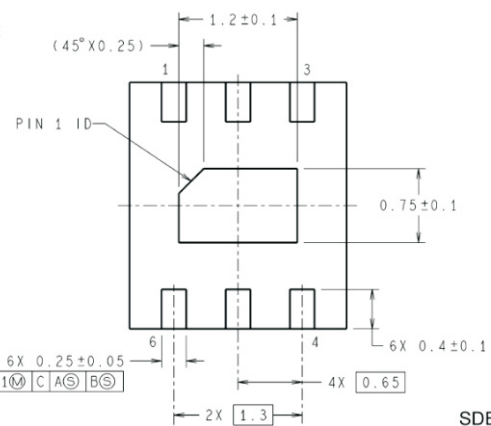
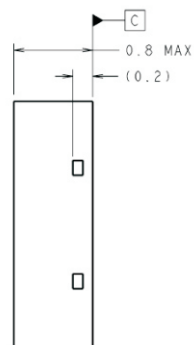
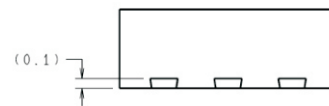
NGF0006A



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SDB06A (Rev A)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated