# 4.5V to 18V Input, 6-A Synchronous Step-Down Converter with Eco-mode™

**Check for Samples: TPS56628**

## FEATURES

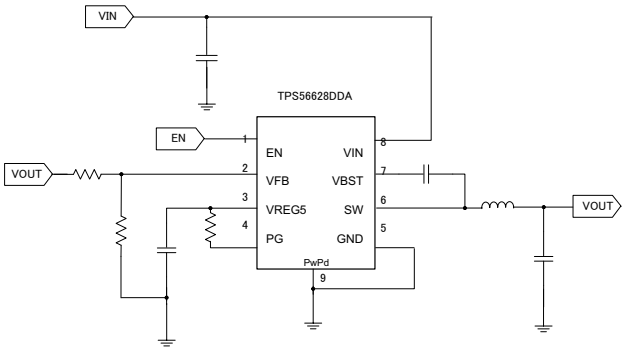
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide $V_{IN}$ Input Voltage Range: 4.5 V to 18 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications – 36 mΩ (High Side) and 28 mΩ (Low Side)**
- **High Efficiency, less than 10 µA at shutdown**
- **High Initial Bandgap Reference Accuracy**
- **Pre-Biased Soft Start**
- **650-kHz Switching Frequency ($f_{SW}$)**
- **Cycle By Cycle Over Current Limit**
- **Auto-Skip Eco-mode™ for High Efficiency at Light Load**
- **Power Good Output**
- **Fixed Soft Start: 1.0 ms**

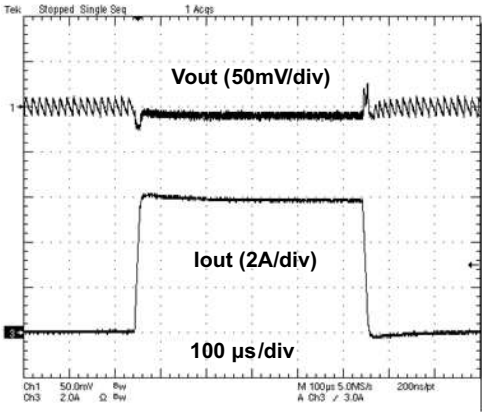
## APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
  - **Digital TV Power Supply**
  - **High Definition Blu-ray Disc™ Players**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**

## DESCRIPTION

The TPS56628 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS56628 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS56628 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS56628 to maintain high efficiency during lighter load conditions. The TPS56628 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 5.5 V. The TPS56628 is available in the 8-pin DDA package, and designed to operate from –40°C to 85°C.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)(2)(3)

| $T_A$ | PACKAGE | ORDERABLE PART NUMBER | PIN | TRANSPORT MEDIA |
|---|---|---|---|---|
| –40°C to 85°C | DDA | TPS56628DDA | 8 | Tube |
| | | TPS56628DDAR | | Tape and Reel |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All package options have Cu NIPDAU lead/ball finish.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Input voltage range | VIN, EN | –0.3 | 20 | V |
| | VBST | –0.3 | 26 | |
| | VBST (10 ns transient) | –0.3 | 28 | |
| | VBST (vs SW) | –0.3 | 6.5 | |
| | VFB, PG | –0.3 | 6.5 | |
| | SW | –2 | 20 | |
| | SW (10 ns transient) | –3 | 22 | |
| Output voltage range | VREG5 | –0.3 | 6.5 | V |
| Voltage from GND to thermal pad, $V_{diff}$ | | –0.2 | 0.2 | V |
| Electrostatic discharge | Human Body Model (HBM) | | 2 | kV |
| | Charged Device Model (CDM) | | 500 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC | | TPS56628 DDA (8 PINS) | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 43.5 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 49.4 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 25.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 25.5 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 5.2 | |


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## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage range | | 4.5 | 18 | V |
| $V_I$ | Input voltage range | VBST | –0.1 | 24 | V |
| | | VBST (10 ns transient) | –0.1 | 27 | |
| | | VBST(vs SW) | –0.1 | 6.0 | |
| | | PG | –0.1 | 5.7 | |
| | | EN | –0.1 | 18 | |
| | | VFB | –0.1 | 5.5 | |
| | | SW | –1.8 | 18 | |
| | | SW (10 ns transient) | –3 | 22 | |
| $V_O$ | Output voltage range | VREG5 | –0.1 | 5.7 | V |
| $I_O$ | Output Current range | $I_{VREG5}$ | 0 | 5 | mA |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{VIN}$ | Operating - non-switching supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 5 V, $V_{FB}$ = 0.8 V | | 950 | 1400 | µA |
| $I_{VINSDN}$ | Shutdown supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 0 V | | 3 | 10 | µA |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{EN}$ | EN high-level input voltage | EN | 1.6 | | | V |
| | EN low-level input voltage | EN | | | 0.6 | V |
| $R_{EN}$ | EN pin resistance to GND | $V_{EN}$ = 12 V | 200 | 400 | 800 | kΩ |
| **$V_{FB}$ VOLTAGE** | | | | | | |
| $V_{FBTH}$ | $V_{FB}$ threshold voltage | $T_A$ = 25°C, $V_O$ = 1.05 V, $I_O$ = 10 mA, Eco-mode™ operation | | 772 | | mV |
| | | $T_A$ = 25°C, $V_O$ = 1.05 V, continuous mode operation | 757 | 765 | 773 | mV |
| | | $T_A$ = -40 to 85°C, $V_O$ = 1.05 V, continuous mode operation(1) | 751 | | 779 | mV |
| $I_{VFB}$ | $V_{FB}$ input current | $V_{FB}$ = 0.8 V, $T_A$ = 25°C | | 0 | ±0.15 | µA |
| **$V_{REG5}$ OUTPUT** | | | | | | |
| $V_{VREG5}$ | $V_{REG5}$ output voltage | $T_A$ = 25°C, 6 V < $V_{IN}$ < 18 V, 0 < $I_{VREG5}$ < 5 mA | 5.2 | 5.5 | 5.7 | V |
| $I_{VREG5}$ | Output current | $V_{IN}$ = 6 V, $V_{REG5}$ = 4.0 V, $T_A$ = 25°C | 20 | | | mA |
| **$V_{FB}$ VOLTAGE AND DISCHARGE RESISTANCE** | | | | | | |
| $R_{DISCHG}$ | $V_{OUT}$ discharge resistance | EN = 0 V, SW = 0.5 V, $T_A$ = 25°C | | 500 | 800 | Ω |
| **MOSFET** | | | | | | |
| $R_{DS(on)}$ | High side switch resistance | 25°C, $V_{BST}$ - SW = 5.5 V | | 36 | | mΩ |
| | Low side switch resistance | 25°C | | 28 | | mΩ |
| **CURRENT LIMIT** | | | | | | |
| $I_{OCL}$ | Current limit | L out = 1.5 µH(1) | 6.6 | 7.3 | 8.9 | A |

(1) Not production tested.

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## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature (2) | | 165 | | °C |
| | | Hysteresis (2) | | 35 | | |
| **ON-TIME TIMER CONTROL** | | | | | | |
| $t_{ON}$ | On time | $V_{IN}$ = 12 V, $V_O$ = 1.05 V | | 150 | | ns |
| $t_{OFF(MIN)}$ | Minimum off time | $T_A$ = 25°C, $V_{FB}$ = 0.7 V | | 260 | 310 | ns |
| **SOFT START** | | | | | | |
| $T_{SS}$ | Soft-start time | Internal soft-start time | 0.7 | 1.0 | 1.3 | ms |
| **POWER GOOD** | | | | | | |
| $V_{THPG}$ | PG threshold | VFB rising (Good) | 85% | 90% | 95% | |
| | | VFB falling (Fault) | | 85% | | |
| IPG | PG sink current | PG = 5 V | 2 | 4 | | mA |
| **HICCUP AND OVER-VOLTAGE PROTECTION** | | | | | | |
| $V_{OVP}$ | Output OVP threshold | OVP Detect (L > H) | | 125% | | |
| $V_{HICCUP}$ | Output Hiccup threshold | Hiccup detect (H > L) | | 65% | | |
| $T_{HICCUPDELAY}$ | Output Hiccup delay | To hiccup state | | 250 | | µs |
| $T_{HICCUPENDELAY}$ | Output Hiccup Enable delay | Relative to soft-start time | | x1.7 | | |
| **UVLO** | | | | | | |
| UVLO | UVLO threshold | Wake up $V_{REG5}$ voltage | 3.45 | 3.75 | 4.05 | V |
| | | Hysteresis $V_{REG5}$ voltage | 0.13 | 0.32 | 0.48 | |

(2) Not production tested.


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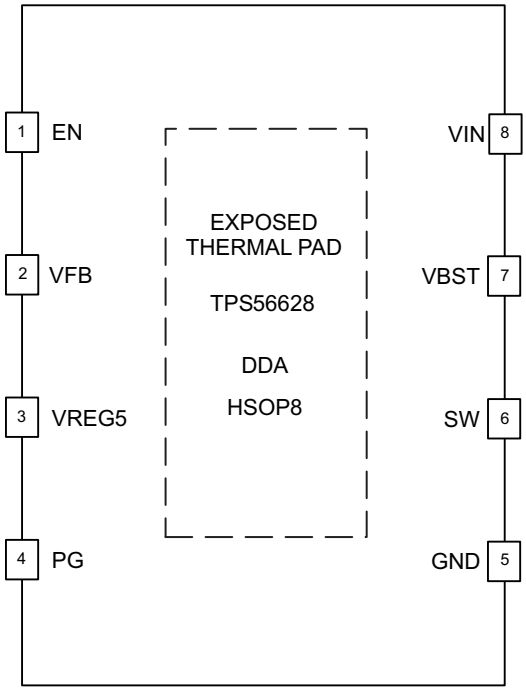
## DEVICE INFORMATION

**DDA PACKAGE**
**(TOP VIEW)**




## PIN FUNCTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| EN | 1 | Enable input control. EN is active high and must be pulled up to enable the device. |
| VFB | 2 | Converter feedback input. Connect to output voltage with feedback resistor divider. |
| VREG5 | 3 | 5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low. |
| PG | 4 | Open drain power good output |
| GND | 5 | Ground pin. Power ground return for switching circuit. Connect sensitive VFB returns to GND at a single point. |
| SW | 6 | Switch node connection between high-side NFET and low-side NFET. |
| VBST | 7 | Supply input for the high-side FET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST. |
| VIN | 8 | Input voltage supply pin. |
| Exposed Thermal Pad | Back side | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND. |

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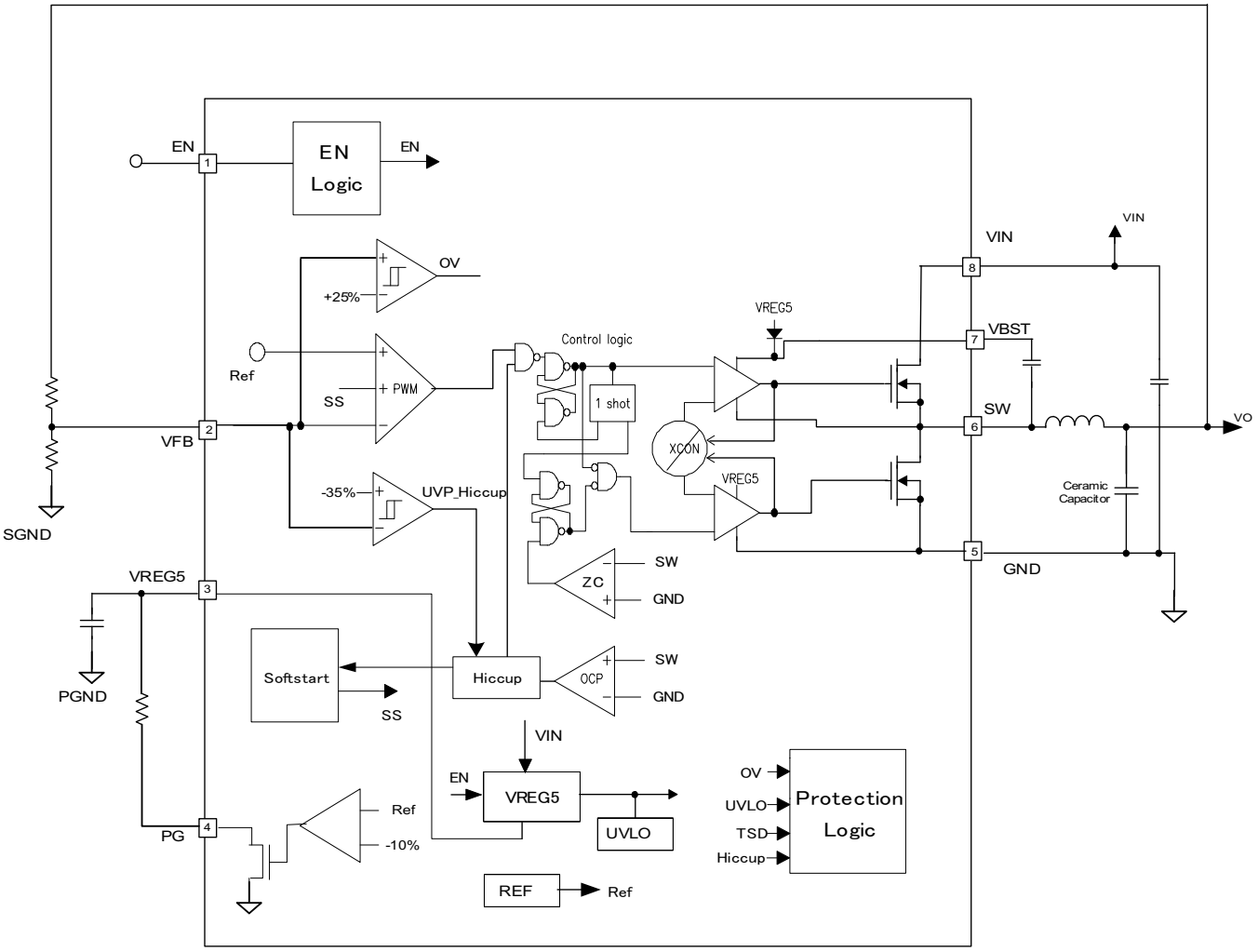
## FUNCTIONAL BLOCK DIAGRAM





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## OVERVIEW

The TPS56628 is a 6-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs with Auto-Skip mode to improve light load efficiency. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types. The PG output can be used for sequence operation.

## DETAILED DESCRIPTION

### PWM Operation

The main control loop of the TPS56628 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### PWM Frequency and Adaptive On-Time Control

TPS56628 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS56628 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

### Auto-Skip Eco-mode™ Control

The TPS56628 is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point where its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converters runs in discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot fsw} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (1)$$

### Soft Start and Pre-Biased Soft Start

The TPS56628 has an internal 1.0 ms soft-start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS56628 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage $V_{FB}$), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage ($V_O$) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

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### Power Good

The power-good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. The power good output, PG is an open drain output. If the feedback voltage goes under 15% of the target value, the power good signal becomes low. Rpg resistor value, which is connected between PG and VREG5, is required from 25kΩ to 150kΩ.

### Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{OUT}$. The TPS56628 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current is higher than the over-current threshold also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage becomes lower than 65% of the target voltage, the UVP comparator detects it. After 250 µs detecting the UVP voltage, device will shut down and re-start after approximately 12ms hiccup time

When the over-current condition is removed, the output voltage returns to the regulated value.

### Overvoltage Protection

TPS56628 detects overvoltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 x times the soft start time. When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET driver and the low-side MOSFET driver turn off. This function is non-latch operation.

### UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS56628 is shut off. This protection is non-latching.

### Thermal Shutdown

TPS56628 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.


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## TYPICAL CHARACTERISTICS

VIN = 12 V, $V_O$ = 1.05V, $T_A$ = 25°C (unless otherwise noted).

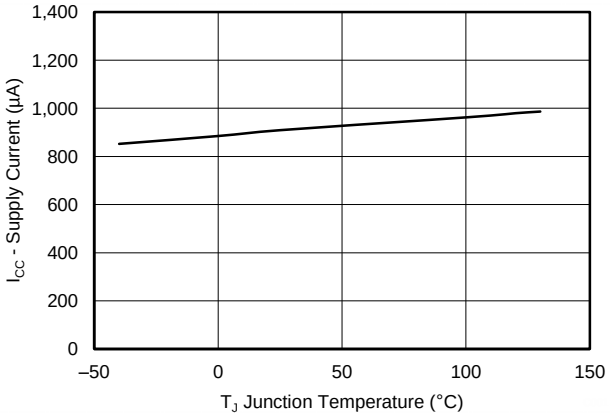


**Figure 1. SUPPLY CURRENT vs JUNCTION TEMPERATURE**

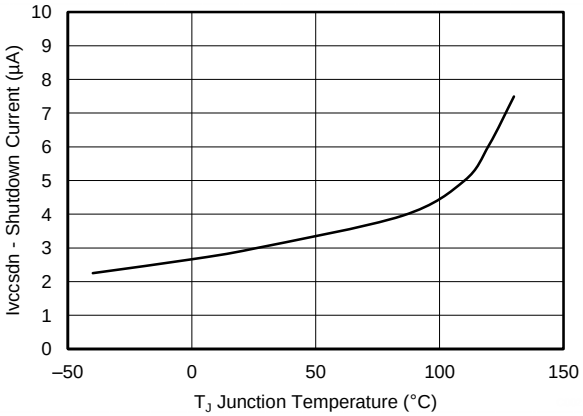


**Figure 2. VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE**

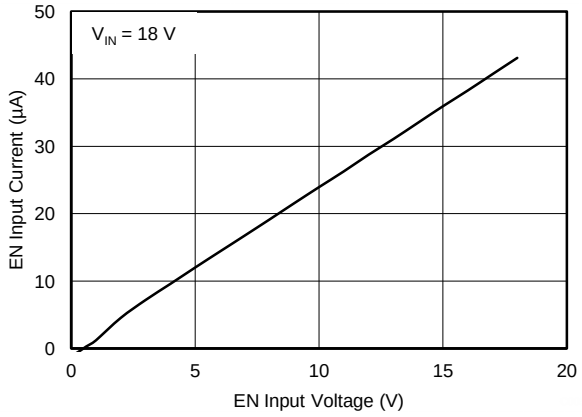


**Figure 3. EN CURRENT vs EN VOLTAGE**

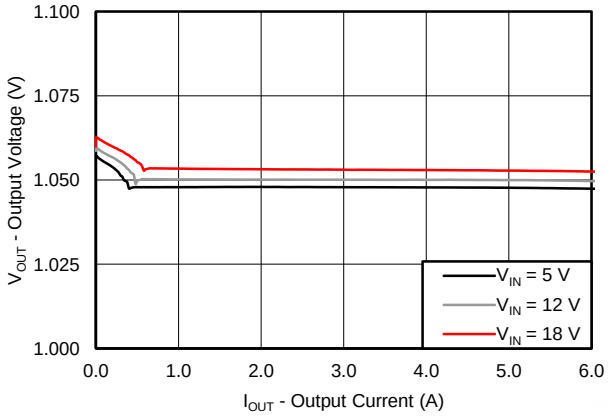


**Figure 4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT**

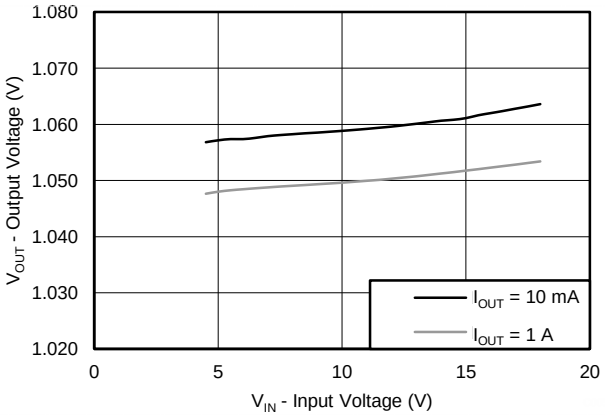


**Figure 5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE**

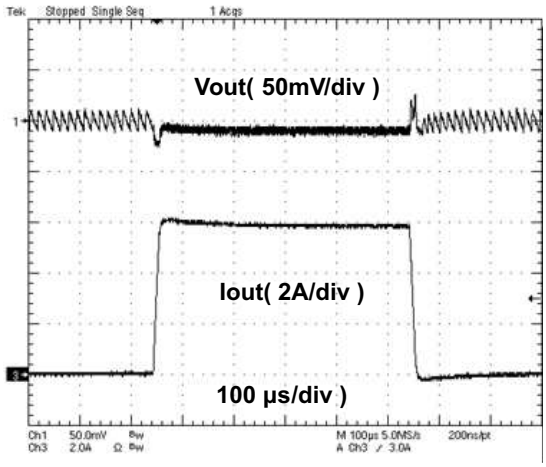


**Figure 6. 1.05-V, LOAD TRANSIENT RESPONSE**

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## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $V_O$ = 1.05V, $T_A$ = 25°C (unless otherwise noted).

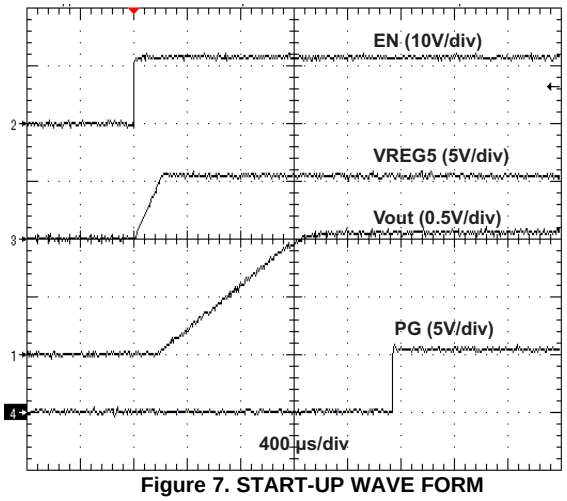


Figure 7. START-UP WAVE FORM

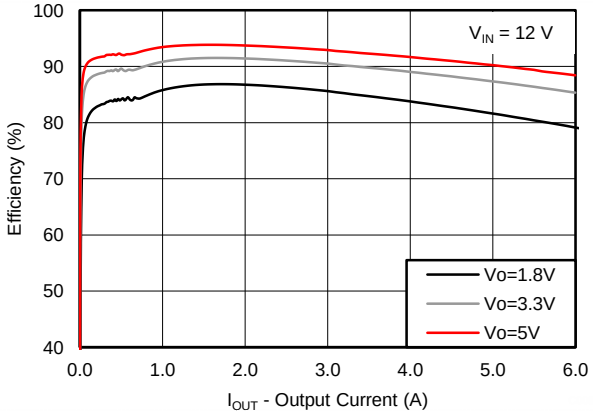


Figure 8. EFFICIENCY vs OUTPUT CURRENT

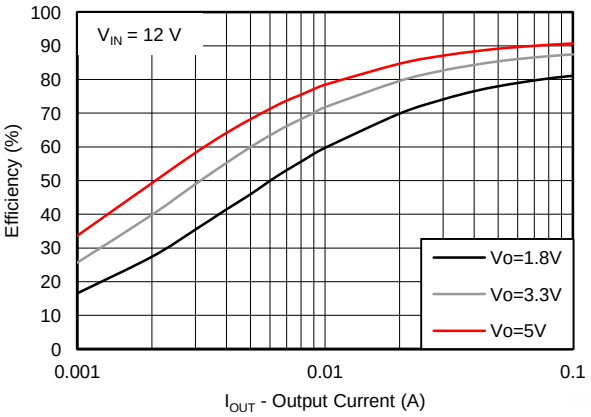


Figure 9. LIGHT LOAD EFFICIENCY vs OUTPUT CURRENT

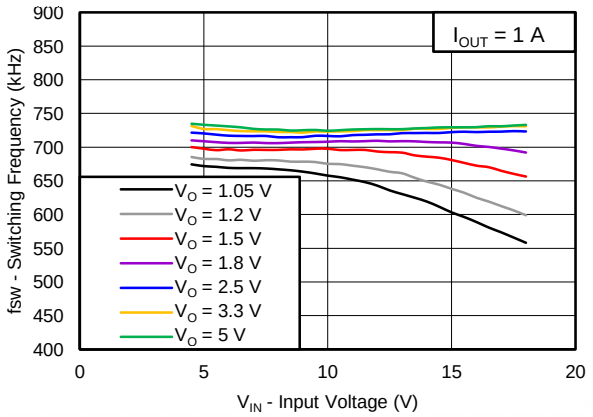


Figure 10. SWITCHING FREQUENCY vs INPUT VOLTAGE

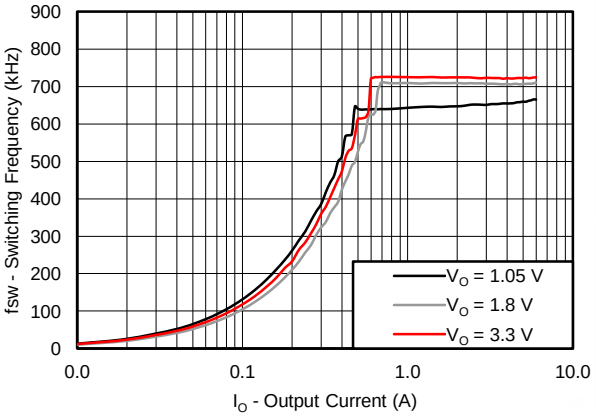


Figure 11. SWITCHING FREQUENCY vs OUTPUT CURRENT

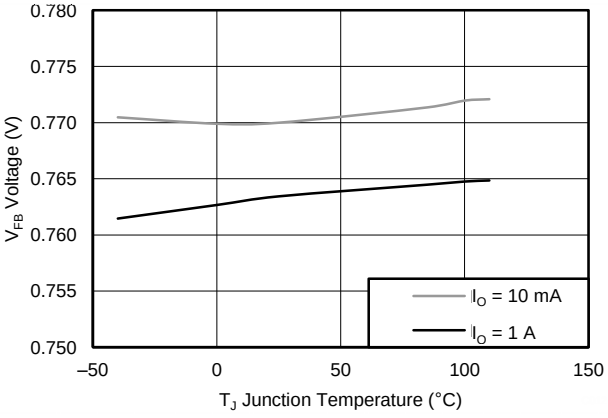


Figure 12. VFB VOLTAGE vs JUNCTION TEMPERATURE


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## TYPICAL CHARACTERISTICS (continued)

VIN = 12 V, $V_O$ = 1.05V, $T_A$ = 25°C (unless otherwise noted).

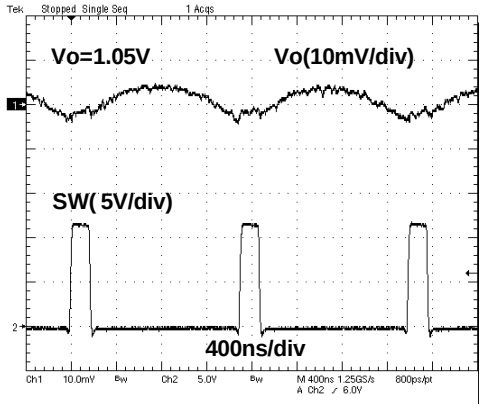


**Figure 13. VOLTAGE RIPPLE AT OUTPUT ($I_O$ = 6 A)**

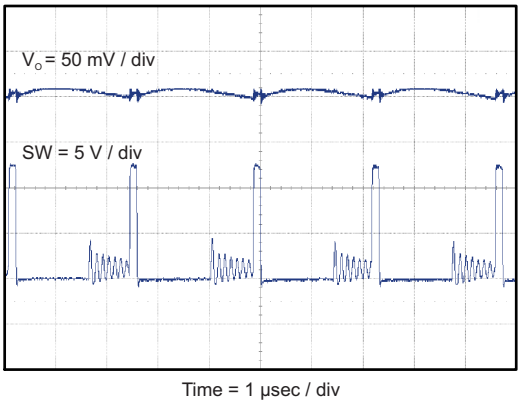


**Figure 14. DCM VOLTAGE RIPPLE AT OUTPUT ($I_O$ = 30 mA)**

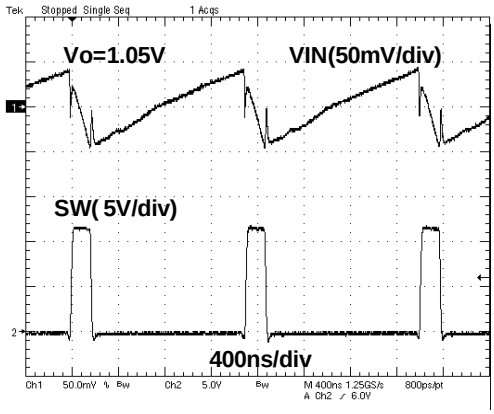


**Figure 15. VOLTAGE RIPPLE AT INPUT ($I_O$ = 6 A)**

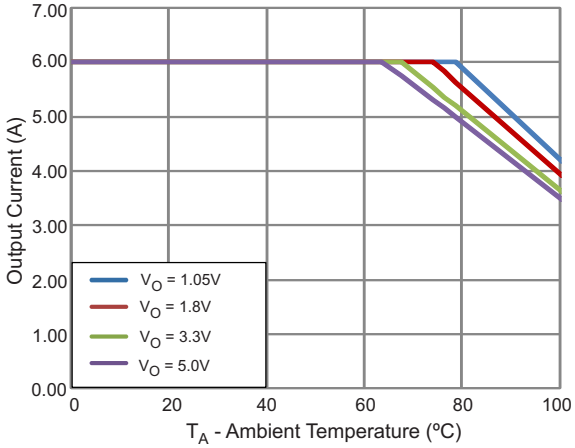


**Figure 16. OUTPUT CURRENT vs AMBIENT TEMPERATURE**

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## DESIGN GUIDE

### Step-By-Step Design Procedure

To begin the design process, the user must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

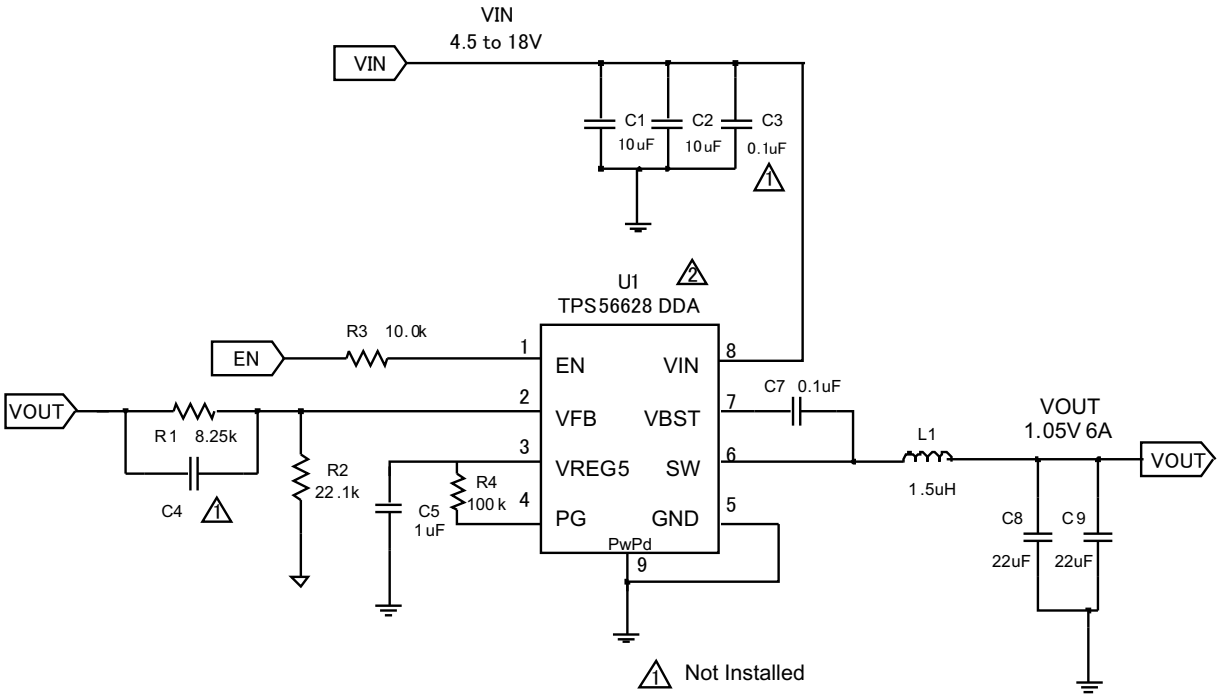


**Figure 17. Shows the Schematic Diagram for This Design Example.**

### Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate $V_{OUT}$.

To improve efficiency at light loads consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

### Output Filter Selection

The output filter used with the TPS56628 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$


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At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS56628. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1

**Table 1. Recommended Component Values**

| Output Voltage (V) | R1 (kΩ) | R2 (kΩ) | C4 (pF)(1) | | | L1 (µH) | | | C8 + C9 (µF) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | MAX |
| 1 | 6.81 | 22.1 | 5 | 150 | 220 | 1.0 | 1.5 | 4.7 | 22 | 68 |
| 1.05 | 8.25 | 22.1 | 5 | 150 | 220 | 1.0 | 1.5 | 4.7 | 22 | 68 |
| 1.2 | 12.7 | 22.1 | 5 | | 100 | 1.0 | 1.5 | 4.7 | 22 | 68 |
| 1.5 | 21.5 | 22.1 | 5 | | 68 | 1.0 | 1.5 | 4.7 | 22 | 68 |
| 1.8 | 30.1 | 22.1 | 5 | | 22 | 1.2 | 1.5 | 4.7 | 22 | 68 |
| 2.5 | 49.9 | 22.1 | 5 | | 22 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 3.3 | 73.2 | 22.1 | 2 | | 22 | 1.8 | 2.2 | 4.7 | 22 | 68 |
| 5 | 124 | 22.1 | 2 | | 22 | 2.2 | 3.3 | 4.7 | 22 | 68 |

(1) Optional

For higher output voltages, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 650 kHz for $f_{SW}$. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{IPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{Ipeak} = I_O + \frac{I_{Ipp}}{2} \quad (5)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{IPP}^2} \quad (6)$$

For this design example, the calculated peak current is 6.51 A and the calculated RMS current is 6.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56628 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22µF to 68µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4A.

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### Input Capacitor Selection

The TPS56628 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C3) from pin 8 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

### Bootstrap Capacitor Selection

A 0.1 µF. ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

### VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

## THERMAL INFORMATION

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly attached to an external heatsink. The thermal pad must be soldered to the printed circuit board (PCB). After soldering, the PCB can be used as a heartsick. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heartsick structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see the Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

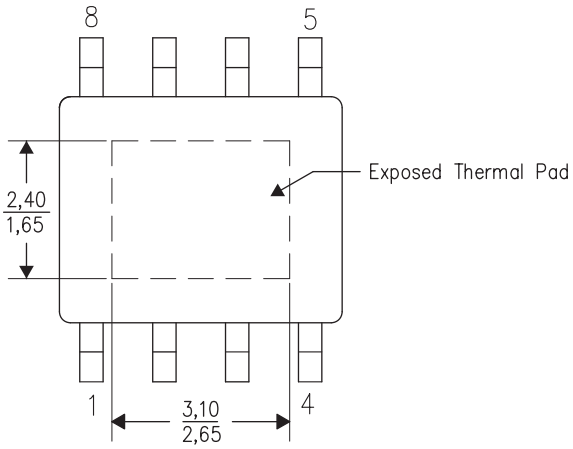


**Figure 18. Thermal Pad Dimensions**


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## LAYOUT CONSIDERATIONS

1. The TPS56628 can supply large load currents up to 6 A, so heat dissipation may be a concern. The top side area of PCB adjacent to the TPS56628 should be filled with ground as much as possible to dissipate heat.
2. The bottom side area directly below the IC should a dedicated ground area. It should be directly connected to the thermal pad of the device using vias as shown. The ground area should be as large as practical. Additional internal layers can be dedicated as ground planes and connected to the vias as well.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN, SW, and PGND (POWERGROUND) broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor should be placed near the device, and connected PGND.
11. Output capacitor should be connected to a broad pattern of the PGND.
12. Voltage feedback loop should be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to ANALOG GROUND.
14. Providing sufficient via is preferable for VIN, SW and PGND connection.
15. VFB node should be as short as possible.
16. VIN Capacitor should be placed as near as possible to the device.

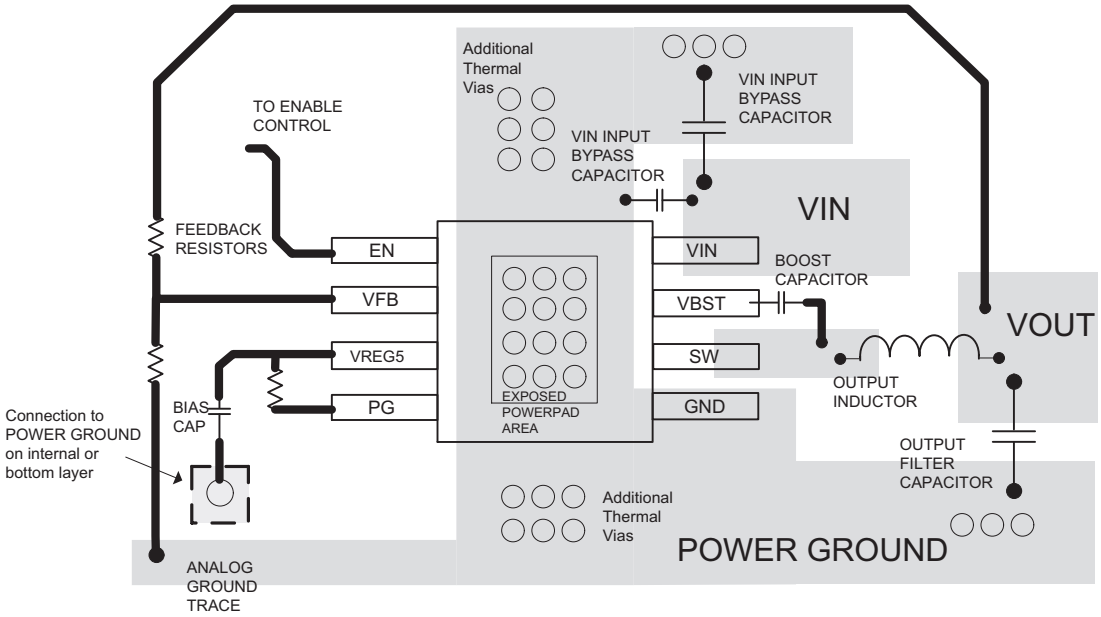


**Figure 19. PCB Layout**

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## REVISION HISTORY

NOTE: Page numbers of current version may vary from previous versions.

**Changes from Original (October 2013) to Revision A** **Page**

- Deleted "The device also features an adjustable soft start time." from the Description. ..... 1
- Deleted "GND" spec from Output Voltage Range in the Absolute Maximum Ratings table. ..... 2
- Deleted "GND" spec from Input Voltage Range in the Recommended Operating Conditions table.. ..... 3
- Deleted "$T_J$" spec from the Recommended Operating Conditions table. ..... 3
- Changed $V_{THPG}$ spec for VFB falling (Fault) condition from "65%" to "85%" in Electrical Characteristics table ..... 4
- Changed GND pin description from "SS and VFB" to "VFB" in the Pin Functions table. ..... 5
- Changed input names from "PGND" to "GND" at the ZC and OCP comparators in the Functional Block Diagram graphic ..... 6
- Changed text string from "constant on-time" to "adaptive on-time" in the 1st paragraph of PWM Operation. ..... 7
- Changed text string from "detects over and under voltage" to "detects overvoltage" in the Overvoltage Protection section. ..... 8
- Added $V_O$ = 1.05V to Conditions statement for the Typical Characteristics graphs. ..... 9
- Changed time scale callout from "100 µs/div" to "400 µs/div" on Figure 7 ..... 10
- Added $V_O$ = 1.05V to Conditions statement for the Typical Characteristics graphs. ..... 10
- Added $V_O$ = 1.05V to Conditions statement for the Typical Characteristics graphs. ..... 11
- Deleted "-950 mv dc offset" text string from signal trace label; and changed SW label from "10 V/div" to "5 V/div" on Figure 14 ..... 11
- Changed some itemized notes in the Layout Considerations section for clarification. ..... 15


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS56628DDA | Active | Production | SO PowerPAD (DDA) \| 8 | 75 \| TUBE | Yes | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | 56628 |
| TPS56628DDA.A | Active | Production | SO PowerPAD (DDA) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 56628 |
| TPS56628DDAR | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | 56628 |
| TPS56628DDAR.A | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 56628 |
| TPS56628DDARG4 | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 56628 |
| TPS56628DDARG4.A | Active | Production | SO PowerPAD (DDA) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 56628 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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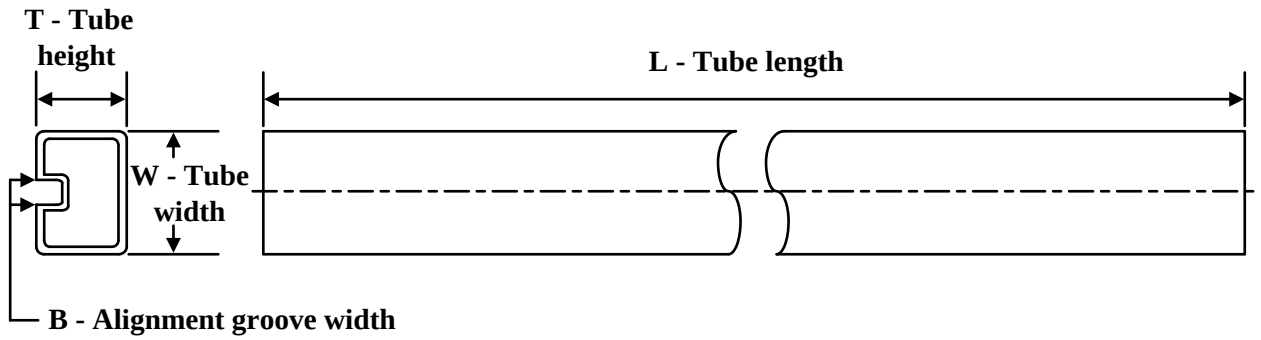
## TUBE

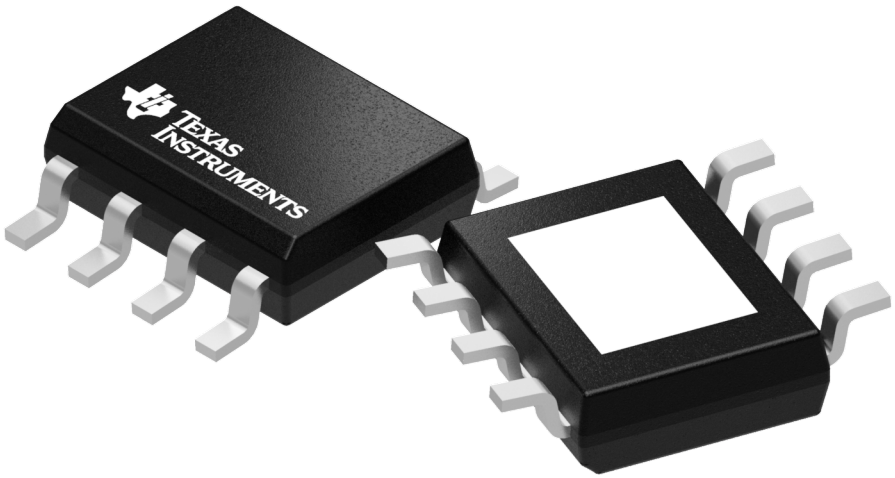



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS56628DDA | DDA | HSOIC | 8 | 75 | 517 | 7.87 | 635 | 4.25 |
| TPS56628DDA.A | DDA | HSOIC | 8 | 75 | 517 | 7.87 | 635 | 4.25 |

# DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



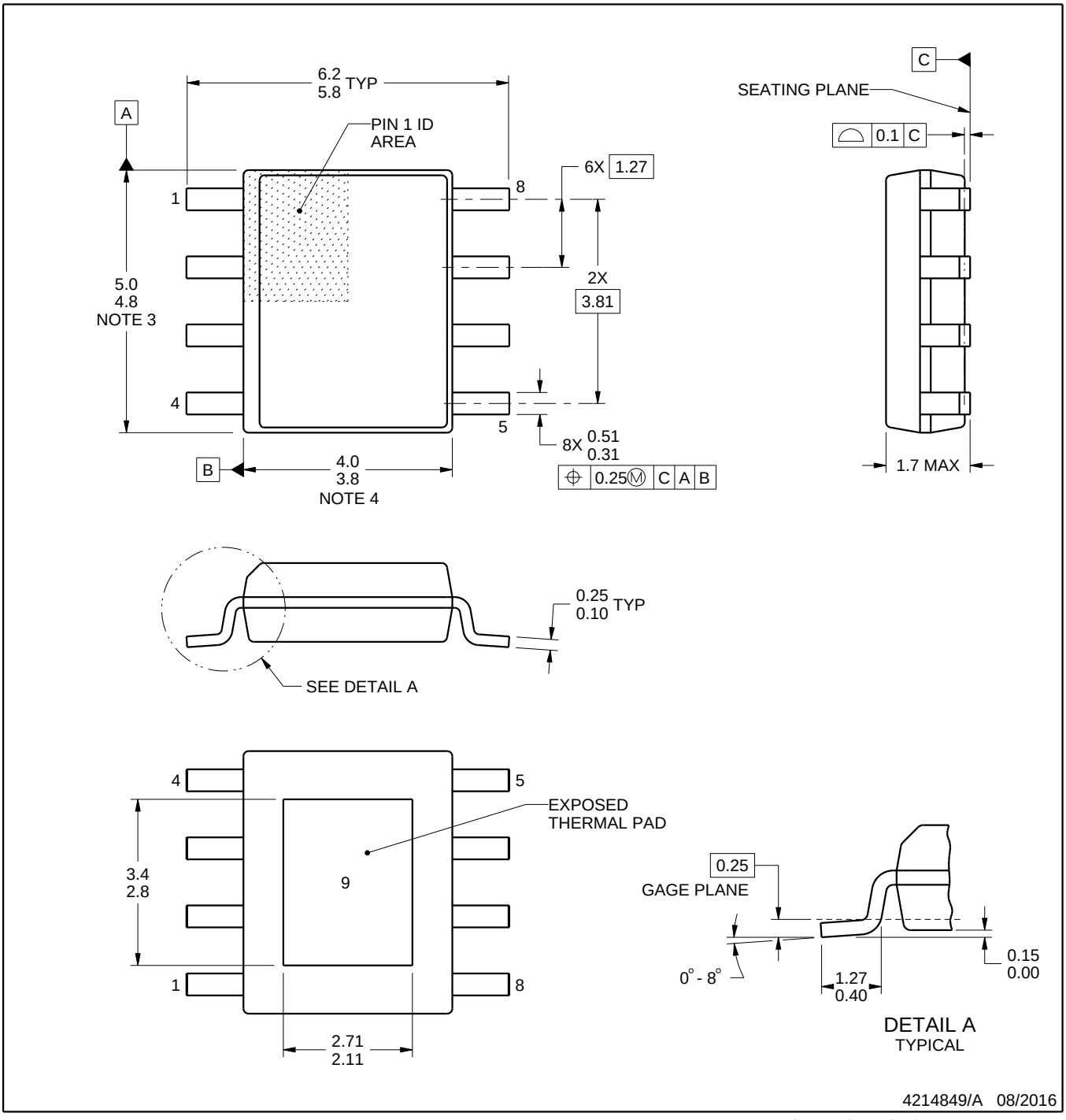

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE

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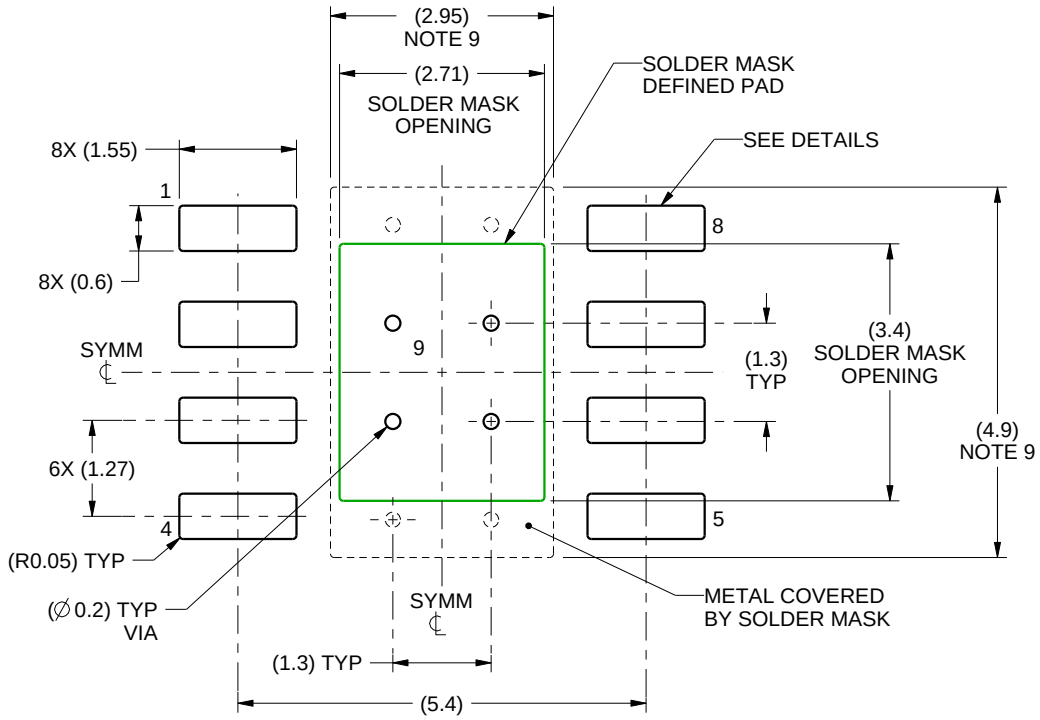
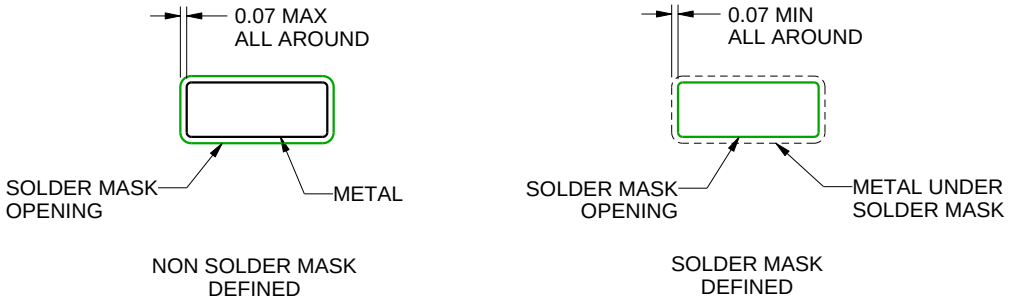
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.




LAND PATTERN EXAMPLE
SCALE:10X




SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

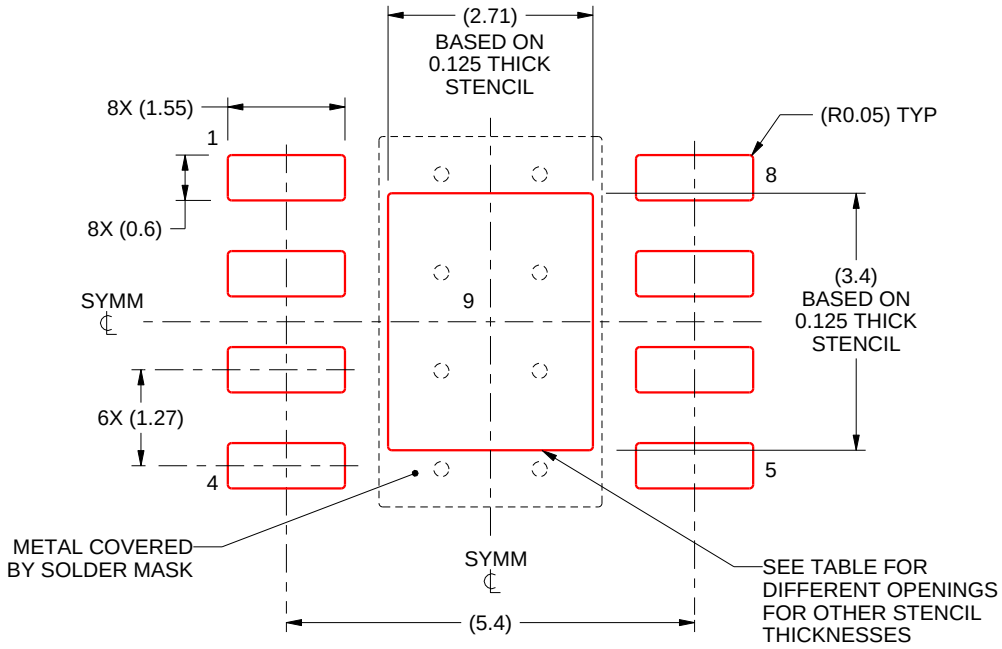
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DDA0008B

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

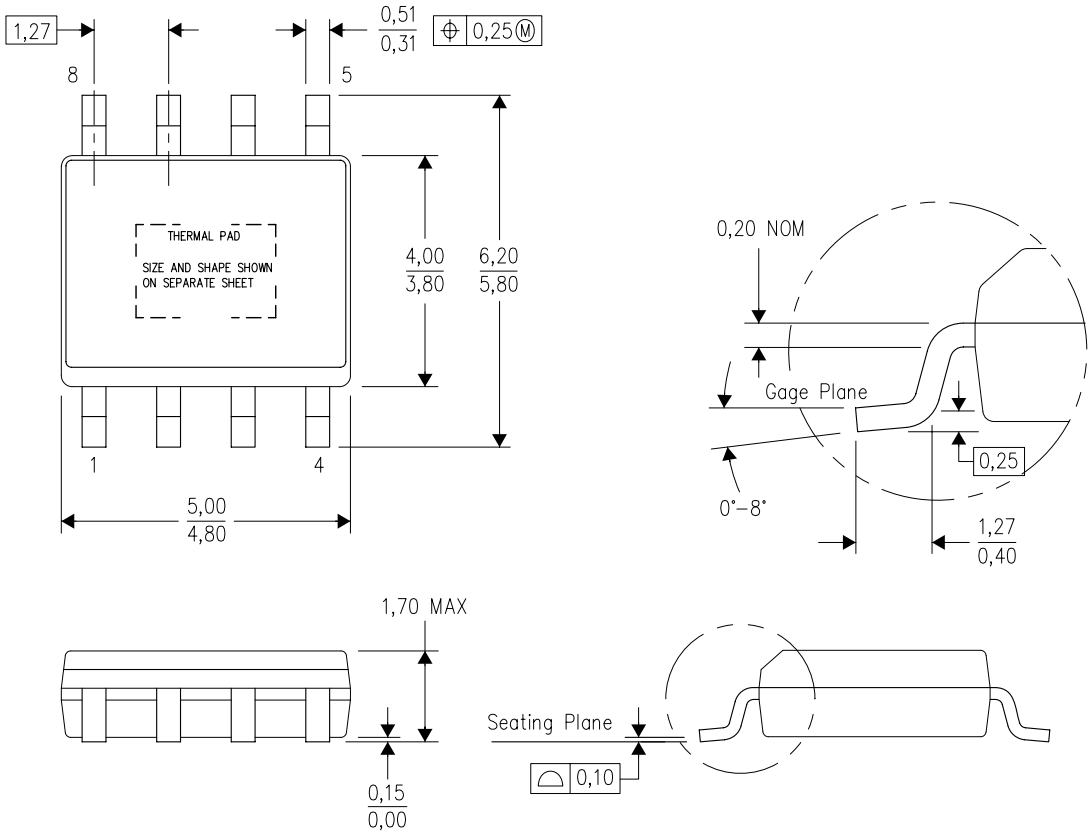
| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.03 X 3.80 |
| 0.125 | 2.71 X 3.40 (SHOWN) |
| 0.150 | 2.47 X 3.10 |
| 0.175 | 2.29 X 2.87 |

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

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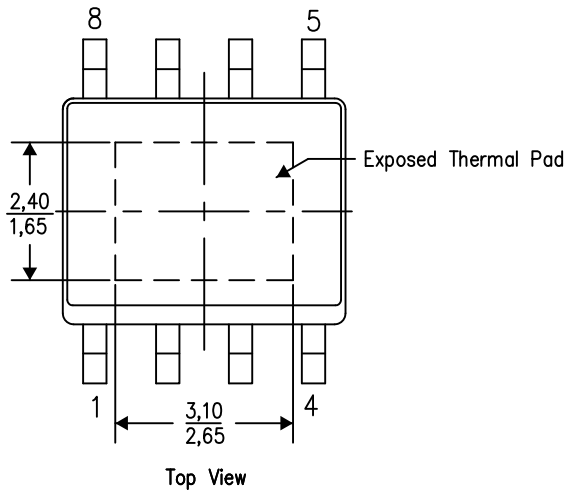
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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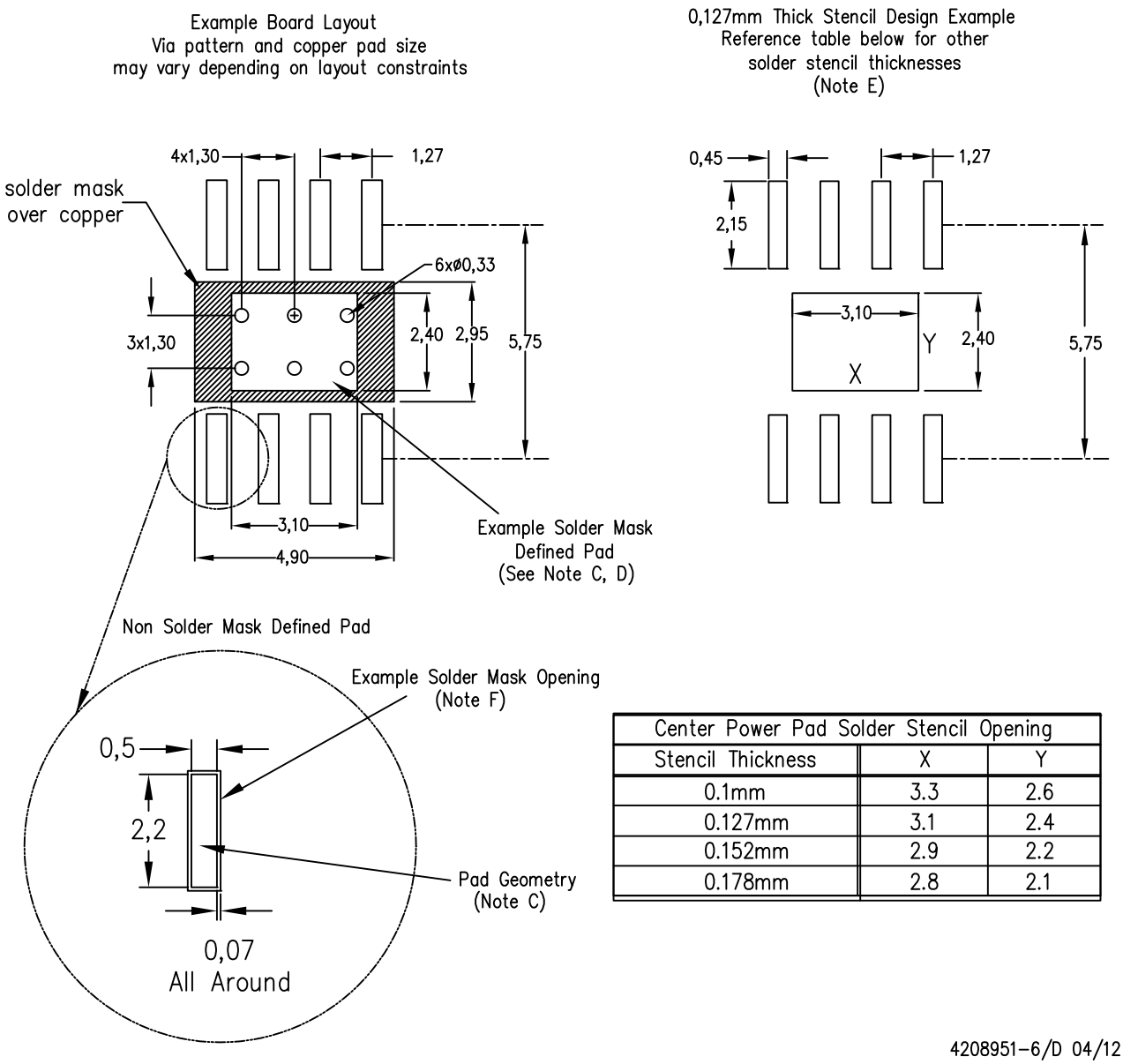
# DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 3.3 | 2.6 |
| 0.127mm | 3.1 | 2.4 |
| 0.152mm | 2.9 | 2.2 |
| 0.178mm | 2.8 | 2.1 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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