PCM1822 Stereo Channel, 32-Bit, 192-kHz, Burr-Brown™ Audio ADC

1 Features

- Stereo high-performance ADC:
  - 2-channel analog microphones or line-in
- ADC line and microphone differential and single-ended input performance:
  - PCM1822 dynamic range:
    - 117-dB, dynamic range enhancer enabled
    - 111-dB, dynamic range enhancer disabled
  - THD+N: –95 dB
- 1-V_{RMS} full-scale input
- ADC sample rate (f_S) = 8 kHz to 192 kHz
- Hardware pin control configurations
- Linear-phase or low-latency filter selection
- Flexible audio serial data interface:
  - Master or slave interface selection
  - 32-bits, 2-channel TDM
  - 32-bits, 2-channel I^2S
- Automatic power-down upon loss of audio clocks
- Integrated high-performance audio PLL
- Single-supply operation: 3.3 V
- I/O-supply operation: 3.3 V or 1.8 V
- Power consumption for 3.3-V AVDD supply:
  - 19.6 mW/channel at 16-kHz sample rate
  - 21.3 mW/channel at 48-kHz sample rate

2 Applications

- Smart Speakers
- DVD recorders and players
- AV receivers
- Video conference systems
- IP network cameras

3 Description

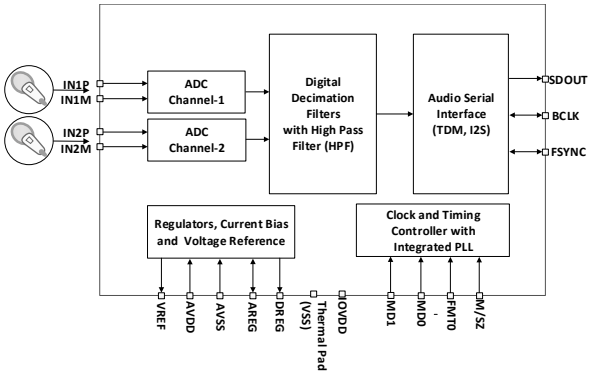
The PCM1822 is a high-performance, Burr-Brown™ audio analog-to-digital converter (ADC) that supports simultaneous sampling of up to two analog channels. The device supports single-ended and differential line and microphone inputs with a 1-V_{RMS} full-scale signal. The device integrates a phase-locked loop (PLL), a DC removal high-pass filter (HPF), and supports sample rates up to 192 kHz. The device supports time-division multiplexing (TDM) or I^2S audio formats, selectable with the hardware pin level. Additionally, the PCM1822 supports master and slave mode selection for the audio bus interface operation. These integrated high-performance features, along with the ability to be powered from a single supply of 3.3 V, make the device an excellent choice for cost-sensitive, space-constrained audio systems in far-field microphone recording applications.

The PCM1822 is specified from –40°C to +125°C, and is offered in a 20-pin WQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1822	WQFN (20)	3.00 mm × 3.00 mm with 0.5-mm pitch

(1) For all available packages, see the package option addendum at the end of the data sheet.



Simplified Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Device Comparison Table....3
6 Pin Configuration and Functions....4
7 Specifications....5
7.1 Absolute Maximum Ratings....5
7.2 ESD Ratings....5
7.3 Recommended Operating Conditions....5
7.4 Thermal Information....6
7.5 Electrical Characteristics....6
7.6 Timing Requirements: TDM or I²S Interface....7
7.7 Switching Characteristics: TDM or I²S Interface....8
7.8 Typical Characteristics....9
8 Detailed Description....13
8.1 Overview....13
8.2 Functional Block Diagram....13
8.3 Feature Description....14
8.4 Device Functional Modes....27
9 Application and Implementation....28
9.1 Application Information....28
9.2 Typical Application....28
10 Power Supply Recommendations....31
11 Layout....32
11.1 Layout Guidelines....32
11.2 Layout Example....32
12 Device and Documentation Support....33
12.1 Receiving Notification of Documentation Updates....33
12.2 Support Resources....33
12.3 Trademarks....33
12.4 Electrostatic Discharge Caution....33
12.5 Glossary....33
13 Mechanical, Packaging, and Orderable Information....33

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Table 4-1.

Date	Revision	Notes
May 2022	*	Initial release

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5 Device Comparison Table

FEATURE	PCM1820	PCM1821	PCM1822	TLV320ADC3120	TLV320ADC5120	TLV320ADC6120
Control interface	Pin control			I^2C		
Digital audio serial interface	TDM or I^2S			TDM or I^2S or left-justified (LJ)		
Audio analog channel	2					
Digital microphone channel	Not available			4		
Programmable MICBIAS voltage	N/A			Yes		
Dynamic range (DRE disabled)	113 dB	106 dB	111dB	106 dB	108 dB	113 dB
Dynamic range (DRE enabled)	123 dB	Not available	117dB	Not available	120 dB	123 dB
ADC SNR with DRE	123 dB	N/A	117dB	N/A	120 dB	123 dB
Input Voltage	$2V_{rms}$		$1V_{rms}$	$2V_{rms}$		
Input Type	Differential	Differential/Single-Ended				
Input impedance	2.5 kΩ	10 kΩ	2.5 kΩ	2.5 kΩ, 10 kΩ, 20 kΩ		
Compatibility	Pin-to-pin, package, drop-in replacements of each other			Pin-to-pin, package, and control registers compatible; drop-in replacements of each other		
Package	WQFN (RTE), 20-pin, 3.00 mm × 3.00 mm (0.5-mm pitch)					

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6 Pin Configuration and Functions

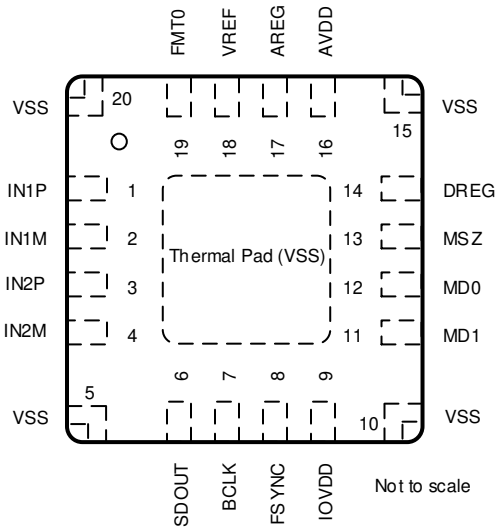


Figure 6-1. RTE Package, 20-Pin WQFN With Exposed Thermal Pad, Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN1P	Analog input	Analog input 1P pin.
2	IN1M	Analog input	Analog input 1M pin.
3	IN2P	Analog input	Analog input 2P pin.
4	IN2M	Analog input	Analog input 2M pin.
5	VSS	Analog Supply	Short this pin directly to the board ground plane.
6	SDOUT	Digital output	Audio serial data interface bus output.
7	BCLK	Digital I/O	Audio serial data interface bus bit clock.
8	FSYNC	Digital I/O	Audio serial data interface bus frame synchronization signal.
9	IOVDD	Digital supply	Digital I/O power supply (1.8 V or 3.3 V, nominal).
10	VSS	Analog supply	Short this pin directly to the board ground plane.
11	MD1	Digital input	Device configuration mode select 1 pin.
12	MD0	Digital input	Device configuration mode select 0 pin.
13	MSZ	Digital input	Audio interface bus master or slave select pin.
14	DREG	Digital supply	Digital regulator output voltage for digital core supply (1.5 V, nominal).
15	VSS	Analog supply	Short this pin directly to the board ground plane.
16	AVDD	Analog supply	Analog power (3.3 V, nominal).
17	AREG	Analog supply	Analog on-chip regulator output voltage for analog supply (1.8 V, nominal).
18	VREF	Analog	Analog reference voltage filter output.
19	FMT0	Digital input	Audio interface format select pin referred to AVDD supply.
20	VSS	Analog supply	Short this pin directly to the board ground plane.
Thermal Pad (VSS)		Ground supply	Thermal pad shorted to internal device ground. Short thermal pad directly to board ground plane.

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7 Specifications

7.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
	AREG to AVSS	–0.3	2.0	
	IOVDD to VSS (thermal pad)	–0.3	3.9	
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	AVDD + 0.3	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD, AREG(1)	Analog supply voltage AVDD to AVSS (AREG is generated using onchip regulator) - AVDD 3.3-V operation	3.0	3.3	3.6	V
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation	1.65	1.8	1.95	
INPUTS					
	Analog input pins and FMT0 voltage to VSS	0		AVDD	V
	Digital input pins voltage(except FMT0) to VSS (thermal pad)	0		IOVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C
OTHERS					
	Digital input pin used as MCLK input clock frequency			36.864	MHz
C_L	Digital output load capacitance		20	50	pF

(1) AVSS and VSS (thermal pad): all ground pins must be tied together and must not differ in voltage by more than 0.2 V.

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7.4 Thermal Information

THERMAL METRIC[1]		PCM182x RTE (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC CONFIGURATION						
	AC input impedance	Input pins INxP or INxM		2.5		kΩ
ADC PERFORMANCE FOR LINE, MICROPHONE INPUT RECORDING : AVDD 3.3-V OPERATION						
	Full-scale AC signal voltage Differential/Single Ended	AC-coupled input		1		V_{RMS}
SNR	Signal-to-noise ratio, A-weighted[1] [2]	IN1 differential/single-ended input selected and AC signal shorted to ground, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 18 dB)	110	117		dB
		IN1 differential/single-ended input selected and AC signal shorted to ground, DRE disabled	105	111		
DR	Dynamic range, A-weighted[2]	IN1 differential/single-ended input selected and –60-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 18 dB)		117		dB
		IN1 differential/single-ended input selected and –60-dB full-scale AC signal input, DRE disabled		111		
THD+N	Total harmonic distortion[2] [3]	IN1 differential/single-ended input selected and –1-dB full-scale AC signal input, DRE enabled (DRE_LVL = –36 dB, DRE_MAXGAIN = 18 dB)		–95	–80	dB
		IN1 differential/single-ended input selected and –1-dB full-scale AC signal input, DRE disabled		–95		
ADC OTHER PARAMETERS						
	Output data sample rate		7.35		192	kHz
	Output data sample word length				32	Bits
	Interchannel isolation	–1-dB full-scale AC-signal input to non measurement channel		–124		dB
	Interchannel gain mismatch	–6-dB full-scale AC-signal input		0.1		dB
	Gain drift[4]	Across temperature range -40°C to 125°C		50		ppm/°C
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.02		Degrees
	Phase drift[5]	1-kHz sinusoidal signal, across temperature range -40°C to 125°C		0.0005		Degrees/°C
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		102		dB
CMRR	Common-mode rejection ratio	Differential microphone input selected, 100-mV_{PP}, 1-kHz signal on both pins and measure level at output		45		dB
DIGITAL I/O						

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at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level digital input logic voltage threshold	All digital pins except FMT0, IOVDD 1.8-V operation	–0.3		0.30 × IOVDD	V
		All digital pins except FMT0, IOVDD 3.3-V operation	–0.3		0.8	
		FMT0 Pin	–0.3		0.8	V
V_{IH}	High-level digital input logic voltage threshold	All digital pins except FMT0, IOVDD 1.8-V operation	0.7 × IOVDD		IOVDD + 0.3	V
		All digital pins except FMT0, IOVDD 3.3-V operation	2.1		IOVDD + 0.3	
		FMT0 Pin	2.1		AVDD + 0.3	V
V_{OL}	Low-level digital output voltage	All digital pins, I_{OL} = –2 mA, IOVDD 1.8-V operation			0.45	V
		All digital pins, I_{OL} = –2 mA, IOVDD 3.3-V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins, I_{OH} = 2 mA, IOVDD 1.8-V operation	IOVDD – 0.45			V
		All digital pins, I_{OH} = 2 mA, IOVDD 3.3-V operation	2.4			
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0 V	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption with all Clocks disabled	AVDD = 3.3 V, internal AREG		0.5		mA
I_{IOVDD}		All external clocks stopped, IOVDD = 3.3 V		0.5		µA
I_{IOVDD}		All external clocks stopped, IOVDD = 1.8 V		0.3		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 16-kHz, BCLK = 256 × f_S and DRE disabled	AVDD = 3.3 V, internal AREG		11.9		mA
I_{IOVDD}		IOVDD = 3.3 V		0.05		
I_{IOVDD}		IOVDD = 1.8 V		0.02		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 48-kHz, BCLK = 256 × f_S and DRE disabled	AVDD = 3.3 V, internal AREG		12.9		mA
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		
I_{AVDD}	Current consumption with ADC 2-channel operating at f_S 48-kHz, BCLK = 256 × f_S and DRE enabled	AVDD = 3.3 V, internal AREG		14		mA
I_{IOVDD}		IOVDD = 3.3 V		0.1		
I_{IOVDD}		IOVDD = 1.8 V		0.05		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with a 20-kHz, low-pass filter and, where noted, an A-weighted filter. Failure to use such a filter may result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) For best distortion performance, use input AC-coupling capacitors with a low-voltage-coefficient.
(4) Gain drift =gain_variation(in temperature range)/ typical gain value(gain at room temperature) / temperature range × 10^6 measured with gain in linear scale.
(5) Phase drift =phase_deviation(in temperature range)/ (temperature range).

7.6 Timing Requirements: TDM or I²S Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		25			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		25			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time(2)			10	ns

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time(2)			10	ns

(1) The BCLK minimum high or low pulse duration can be relaxed to 14 ns (to meet the timing specifications), if the SDOUT data line is latched on the same BCLK edge polarity as the edge used by the device to transmit SDOUT data.
(2) BCLK maximum rise and fall time can be relaxed to 13ns if BCLK frequency used in the system is below 20MHz. This can cause noise increase due to higher clock jitter.

7.7 Switching Characteristics: TDM or I²S Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT	3		18	ns
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT			18	ns
$f_{(BCLK)}$	BCLK output clock frequency: master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration: master mode		14			ns
$t_{L(BCLK)}$	BCLK low pulse duration: master mode		14			ns
$t_{d(FSYNC)}$	BCLK to FSYNC delay: master mode	50% of BCLK to 50% of FSYNC	3		18	ns
$t_{r(BCLK)}$	BCLK rise time: master mode	10% - 90% rise time			8	ns
$t_{f(BCLK)}$	BCLK fall time: master mode	90% - 10% fall time			8	ns

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

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7.8 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

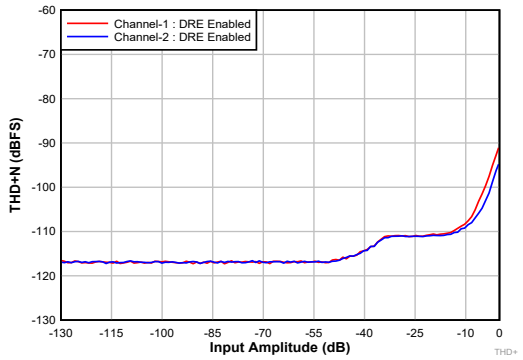


Figure 7-1. Differential Input: THD+N vs Input Amplitude With DRE Enabled

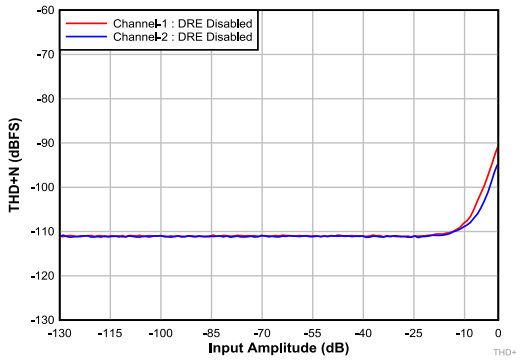


Figure 7-2. Differential Input: THD+N vs Input Amplitude With DRE Disabled

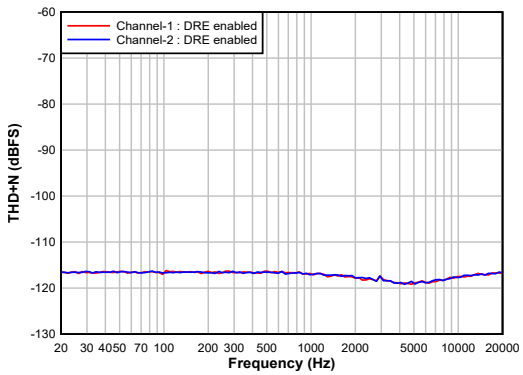


Figure 7-3. Differential Input: DR vs Input Frequency With DRE Enabled

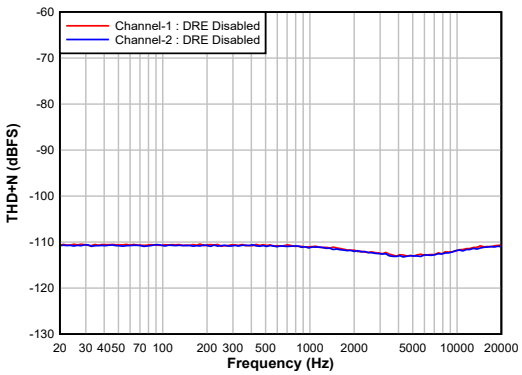


Figure 7-4. Differential Input: DR vs Input Frequency With DRE Disabled

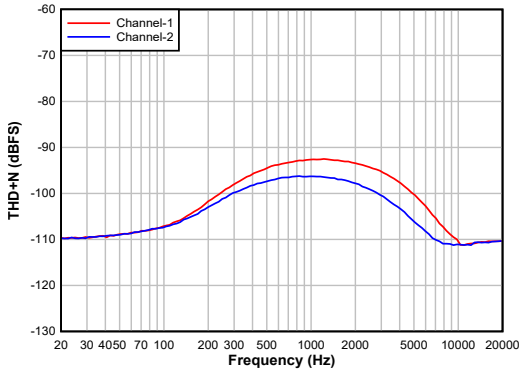


Figure 7-5. Differential Input: THD+N vs Input Frequency With a –1-dBr Input

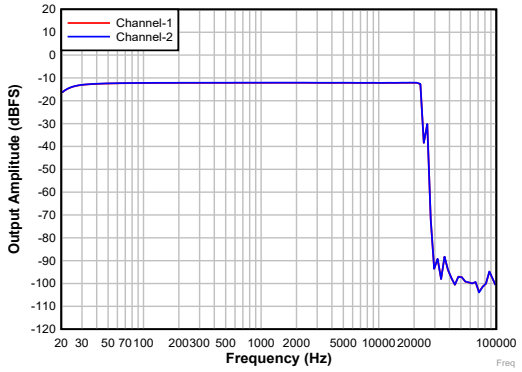


Figure 7-6. Differential Input: Frequency Response With a –12-dBr Input

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7.8 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

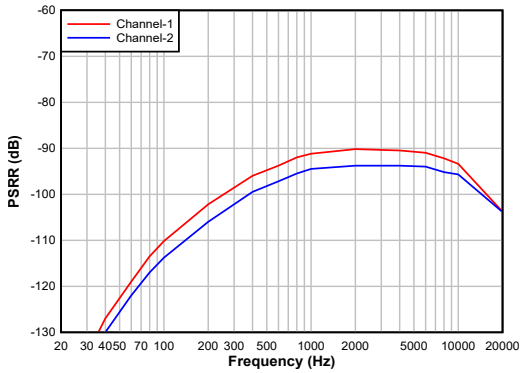


Figure 7-7. Power-Supply Rejection Ratio vs Ripple Frequency With a 100-mV_{PP} Amplitude

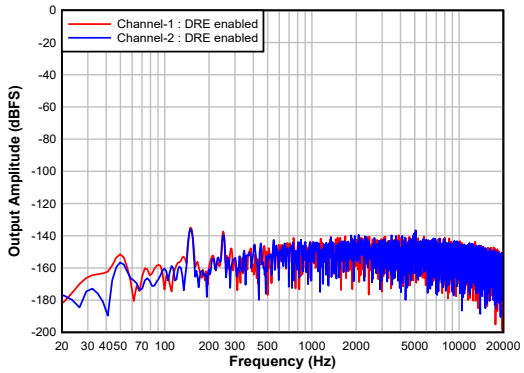


Figure 7-8. Differential Input: FFT With Idle Input and DRE Enabled

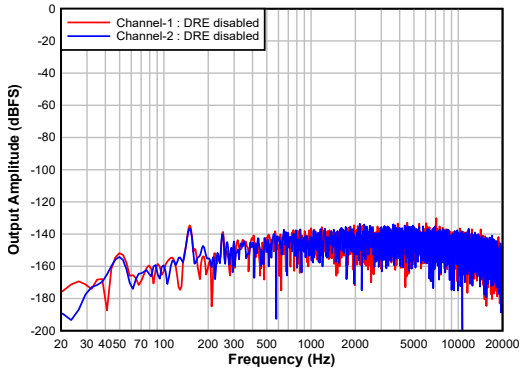


Figure 7-9. Differential Input: FFT With Idle Input and DRE Disabled

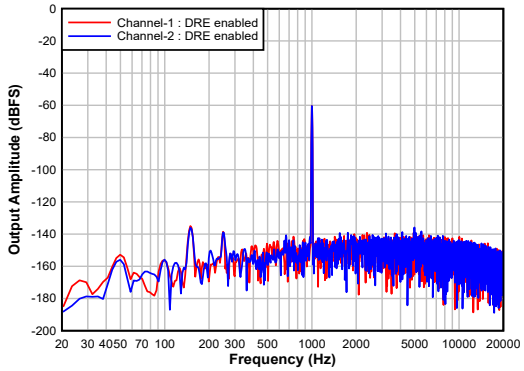


Figure 7-10. Differential Input: FFT With a –60-dBr Input and DRE Enabled

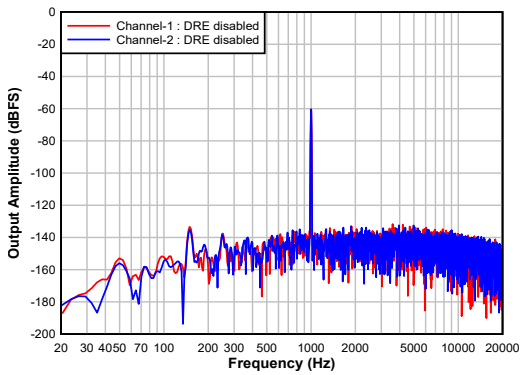


Figure 7-11. Differential Input: FFT With a –60-dBr Input and DRE Disabled

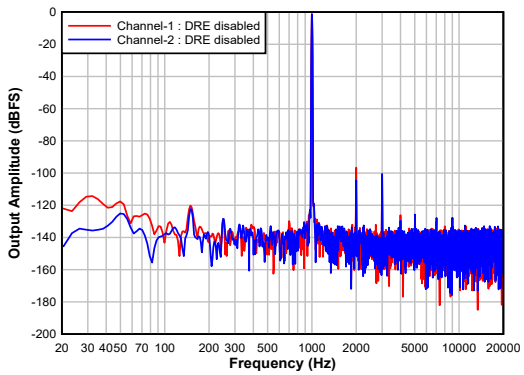


Figure 7-12. Differential Input: FFT With a –1-dBr Input

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7.8 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

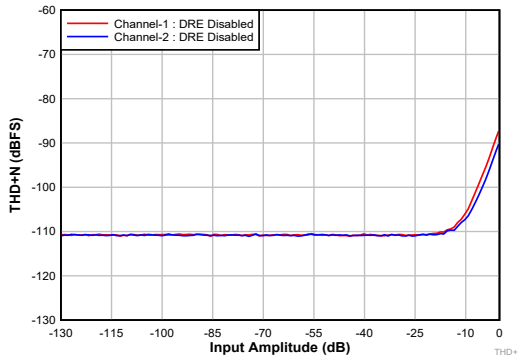


Figure 7-13. Single-Ended Input: THD+N vs Input Amplitude With DRE Disabled

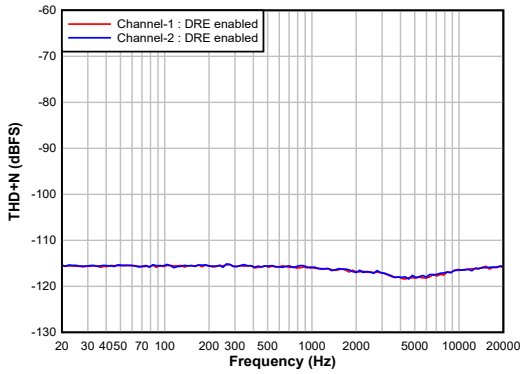


Figure 7-14. Single-ended Input: DR vs Input Frequency With DRE Enabled

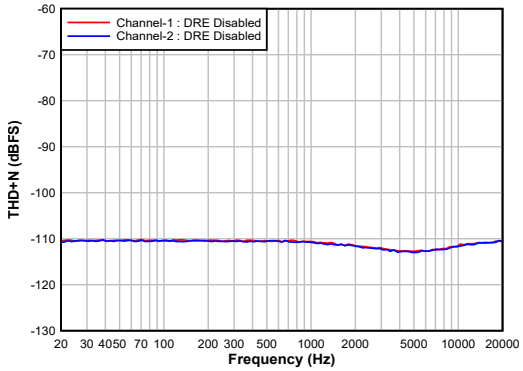


Figure 7-15. Single-Ended Input: DR vs Input Frequency With DRE Disabled

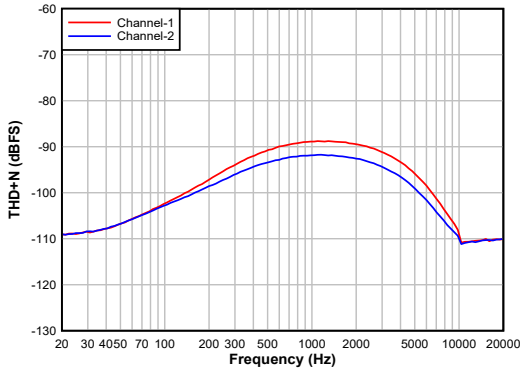


Figure 7-16. Single-Ended Input: THD+N vs Input Frequency With a –1-dBr Input

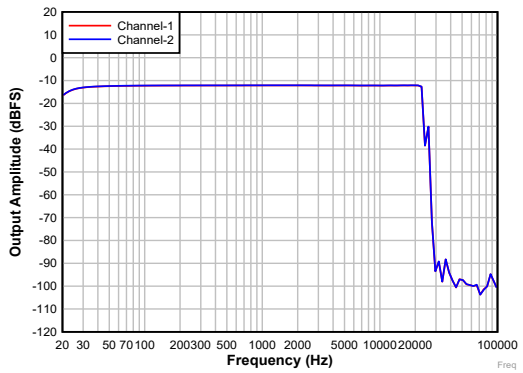


Figure 7-17. Single-ended Input: Frequency Response With a –12-dBr Input

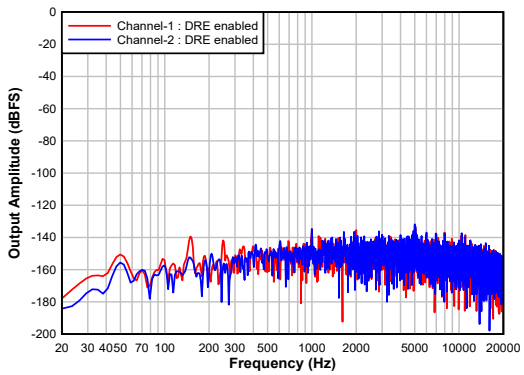


Figure 7-18. Single-ended Input: FFT With Idle Input and DRE Enabled

7.8 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 × f_S, TDM slave mode, PLL on, DRE_LVL = –36 dB, channel gain = 0 dB, and linear phase decimation filter (unless otherwise noted); all performance measurements are done with a 20-kHz, low-pass filter, and an A-weighted filter

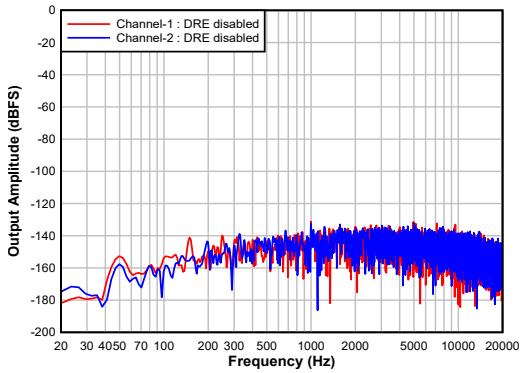


Figure 7-19. Single-ended Input: FFT With Idle Input and DRE Disabled

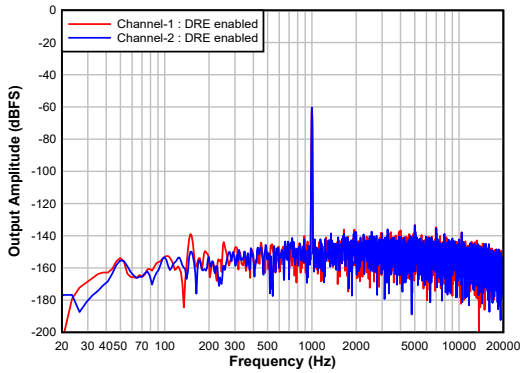


Figure 7-20. Single-ended Input: FFT With a –60-dBr Input and DRE Enabled

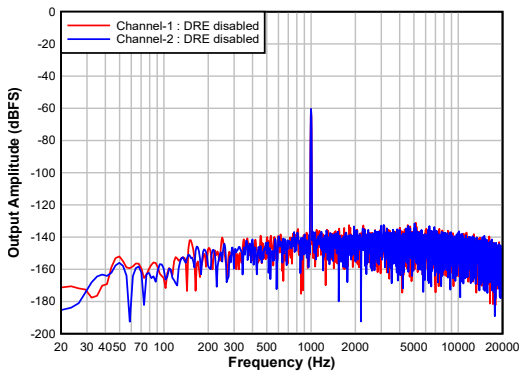


Figure 7-21. Single-ended Input: FFT With a –60-dBr Input and DRE Disabled

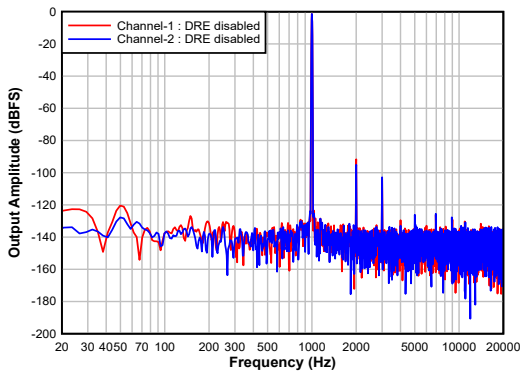


Figure 7-22. Single-ended Input: FFT With a –1-dBr Input

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8 Detailed Description

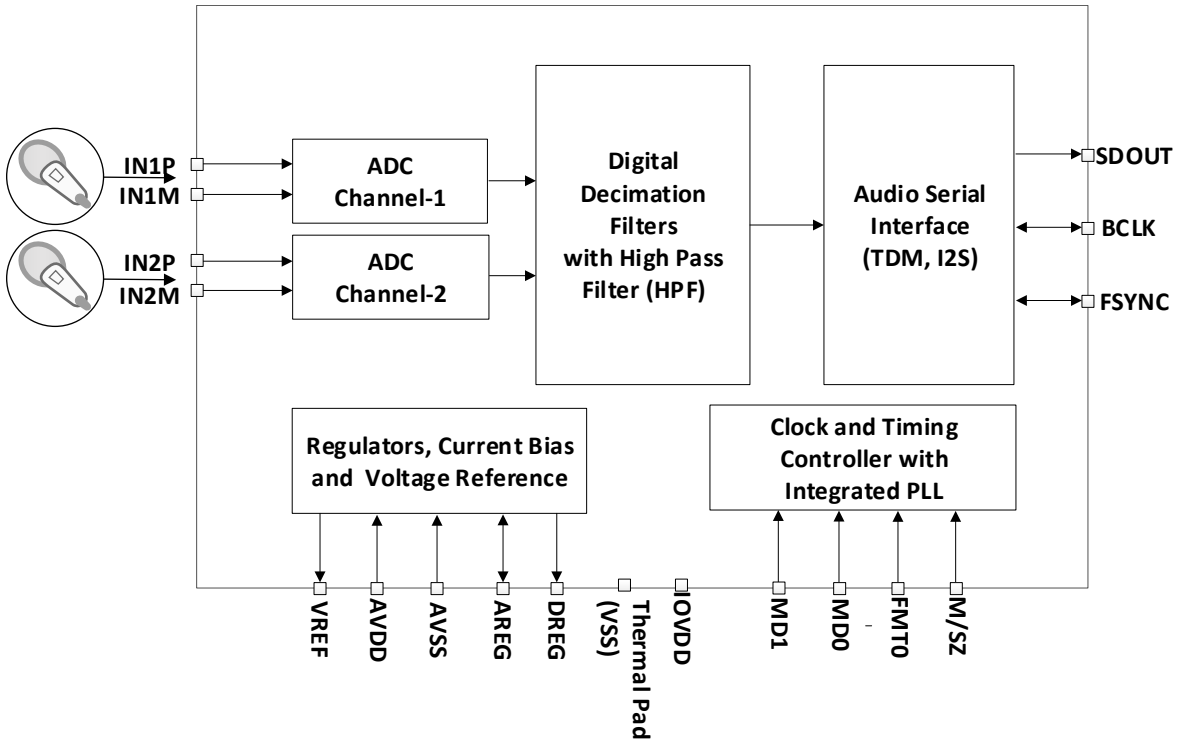
8.1 Overview

The PCM1822 is a high-performance, low-power, stereo-channel, audio analog-to-digital converter (ADC) with flexible audio interface control options. This device is intended for applications in voice-activated systems, AV receivers, tv and blu-ray players, professional microphones, audio conferencing, portable computing, communication, and entertainment applications. The high dynamic range of the device enables far-field audio recording with high fidelity. This device integrates a host of features that reduces cost, board space, and power consumption in space-constrained applications. The device features are controlled through hardware by pulling pins high or low with resistors or a controller general-purpose inut/output (GPIO). The PCM1822 also supports a power-down and reset function by means of halting the system clock.

The PCM1822 consists of the following blocks and features:

- Stereo-channel, multibit, high-performance delta-sigma (ΔΣ) ADC
- Differential/Single-Ended audio inputs with a 1-V_{RMS} full-scale signal
- Hardware pin control operation to select the device features
- Audio bus serial interface master or slave select option
- Audio bus serial interface format select option
- Slave mode supports the audio bus serial interface up to 192 kHz sampling
- Slave mode supports a dynamic range enhancer (DRE) with 117-dB dynamic range for the PCM1822
- Slave mode supports decimation filters with linear-phase or low-latency filter selection
- Master mode operation supported using a system clock of 256 × f_S or 512 × f_S
- Power-down function by means of halting the audio clocks
- Integrated high-pass filter (HPF) that removes the DC component of the input signal
- Integrated low-jitter phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply, 3.3-V operation

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Hardware Control

The device supports simple hardware-pin-controlled options to select a specific mode of operation and audio interface for a given system. The MSZ, MD0, MD1, and FMT0 pins allow the device to be controlled by either pullup or pulldown resistors.

8.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the PCM1822 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for the I^2S, and the pin-selectable master-slave configurability for bus clock lines.

The device supports an audio bus master or slave mode of operation using the hardware pin MSZ. In slave mode, FSYNC and BCLK work as input pins whereas in master mode, FSYNC and BCLK work as output pins generated by the device. Table 8-1 shows the master and slave mode selection using the MSZ pin.

Table 8-1. Master and Slave Mode Selection

MSZ	MASTER AND SLAVE SELECTION
Low	Slave mode of operation
High	Master ode of operation

The bus protocol TDM or I^2S format can be selected by using the FMT0 pin. As shown in Table 8-2, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with an output channel data word-length of 32 bits.

Table 8-2. Audio Serial Interface Format

FMT0	AUDIO SERIAL INTERFACE FORMAT
Low	2-channel output with inter IC sound (I^2S) mode
High	2-channel output with time division multiplexing (TDM) mode

8.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. Figure 8-1 to Figure 8-4 illustrate the protocol timing for TDM operation with various configurations.

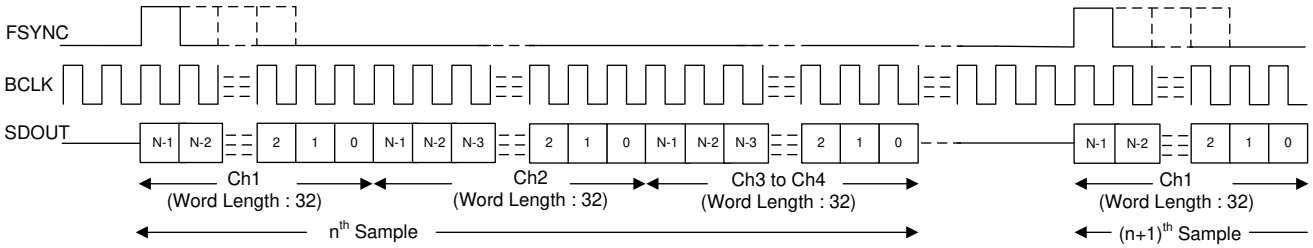


Figure 8-1. TDM Mode Protocol Timing (FMT0 = LOW) In Slave Mode

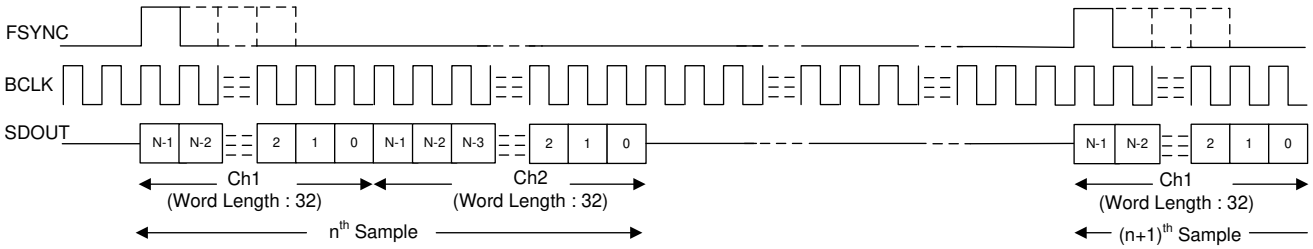


Figure 8-2. TDM Mode Protocol Timing (FMT0 = HIGH) In Slave Mode

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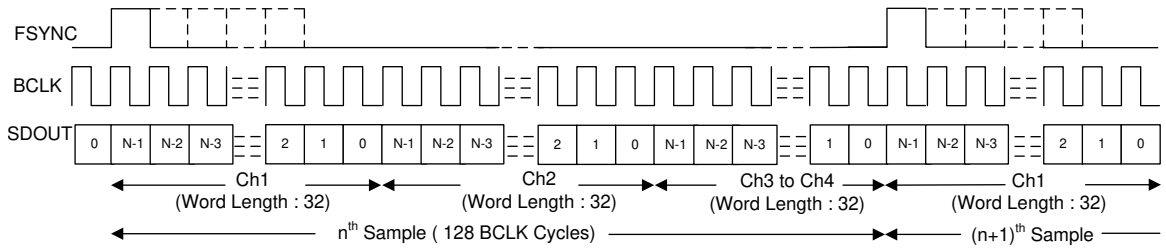


Figure 8-3. TDM Mode Protocol Timing (FMT0 = LOW) In Master Mode

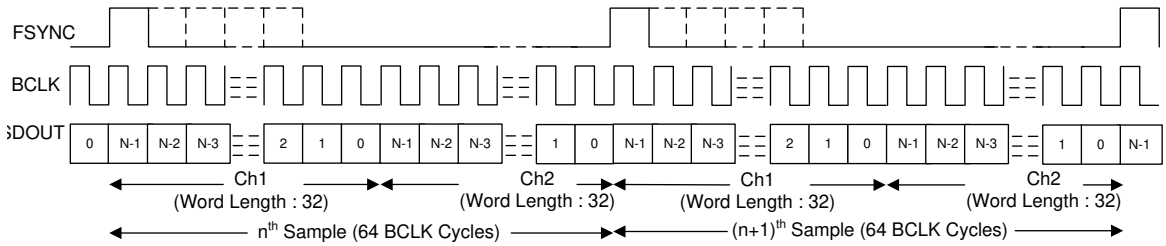


Figure 8-4. TDM Mode Protocol Timing (FMT0 = HIGH) In Master Mode

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the 32-bits word length of the output channel data. The device transmits a zero data value on SDOUT for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well.

8.3.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. In master mode, FSYNC is transmitted on the rising edge of BCLK. Figure 8-5 and Figure 8-6 show the protocol timing for I^2S operation in slave and master mode of operation.

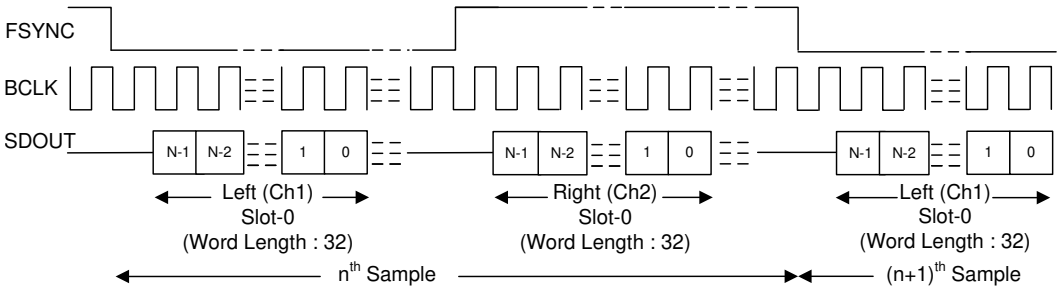


Figure 8-5. I^2S Mode Protocol Timing in Slave Mode

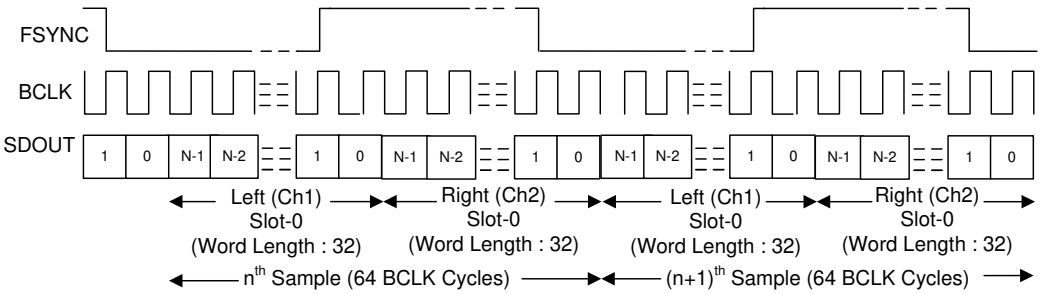


Figure 8-6. I^2S Protocol Timing In Master Mode

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For proper operation of the audio bus in I^2S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the 32-bits word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the 32-bits data word length. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the 32-bits data word length. The device transmit zero data value on SDOUT for the extra unused bit clock cycles.

8.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC modulator and digital filter engine, as well as other control blocks.

In slave mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 8-3 and Table 8-4 list the supported FSYNC and BCLK frequencies.

Table 8-3. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**

Table 8-4. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)						
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**

In the master mode of operation, the device uses the MD1 pin (as the system clock, MCLK) as the reference input clock source with a supported system clock frequency option of either 256 × f_S or 512 × f_S as configured using the MD0 pin. Master mode supports f_S rates of 44.1 kHz and 48 kHz. Table 8-5 shows the system clock selection for the master mode using the MD0 pin.

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Table 8-5. System Clock Selection for the Master Mode

MD0	SYSTEM CLOCK SELECTION (Valid for Master Mode Only)
LOW	System clock with frequency 256 × f_S connected to the MD1 pin as MCLK
HIGH	System clock with frequency 512 × f_S connected to the MD1 pin as MCLK

See Table 8-7 and Table 8-20 for the MD0 and MD1 pin function in the slave mode of operation.

8.3.4 Input Channel Configurations

The device consists of two pairs of analog input pins (INxP and INxM) as differential inputs for the recording channel. The device supports simultaneous recording of up to two channels using the high-performance stereo ADC. The input source for the analog pins can be from electret condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs must be capacitively coupled (AC-coupled) to the device and, for best distortion performance, use the low-voltage coefficient capacitors for AC coupling. The typical input impedance for the PCM1822 is 2.5 kΩ for the INxP or INxM pins. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has a quick charge scheme to speed up the charging of the coupling capacitor at power-up. The default value of the quick-charge timing is set for a coupling capacitor up to 1 µF.

8.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The PCM1822 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1-µF capacitor connected from the VREF pin to analog ground (AVSS). The value of this reference voltage, VREF, is set to 2.75 V, which in turn supports a 2-V_{RMS} differential full-scale input to the device. The required minimum AVDD voltage for this VREF voltage is 3 V. Do not connect any external load to a VREF pin.

8.3.6 Signal-Chain Processing

The PCM1822 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the PCM1822 optimized for a variety of end-equipments and applications that require multichannel audio capture. Figure 8-7 shows a conceptual block diagram for the PCM1822 that highlights the various building blocks used in the signal chain, and how the blocks interact in the signal chain. The PCM1822 does not support DRE.

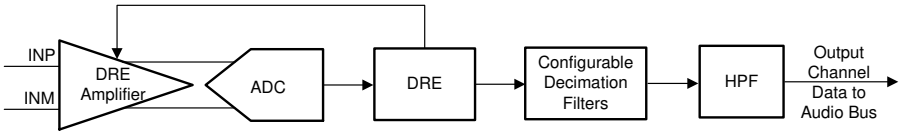


Figure 8-7. Signal-Chain Processing Flowchart

The front-end dynamic range enhancer (DRE) gain amplifier in the PCM1822 is very low noise, with a 117-dB dynamic range performance. Along with a low-noise and low-distortion, multibit, delta-sigma ADC, the front-end DRE gain amplifier enables the PCM1822 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device supports an input signal bandwidth up to 80 kHz, which allows the high-frequency non-audio signal to be recorded by using a 176.4-kHz (or higher) sample rate.

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8.3.6.1 Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a fixed high-pass filter (HPF) with –3-dB cut-off frequency of 0.00025 × f_S. The HPF is not a channel-independent filter but is globally applicable for all the ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. Table 8-6 shows the fixed –3-dB cutoff frequency value. Figure 8-8 shows a frequency response plot for the HPF filter.

Table 8-6. HPF Cutoff Frequency Value

-3-dB CUTOFF FREQUENCY VALUE	-3-dB CUTTOFF FREQUENCY AT 16 kHz SAMPLE RATE	-3-dB CUTTOFF FREQUENCY AT 48 kHz SAMPLE RATE
0.00025 × f_S	4 Hz	12 Hz

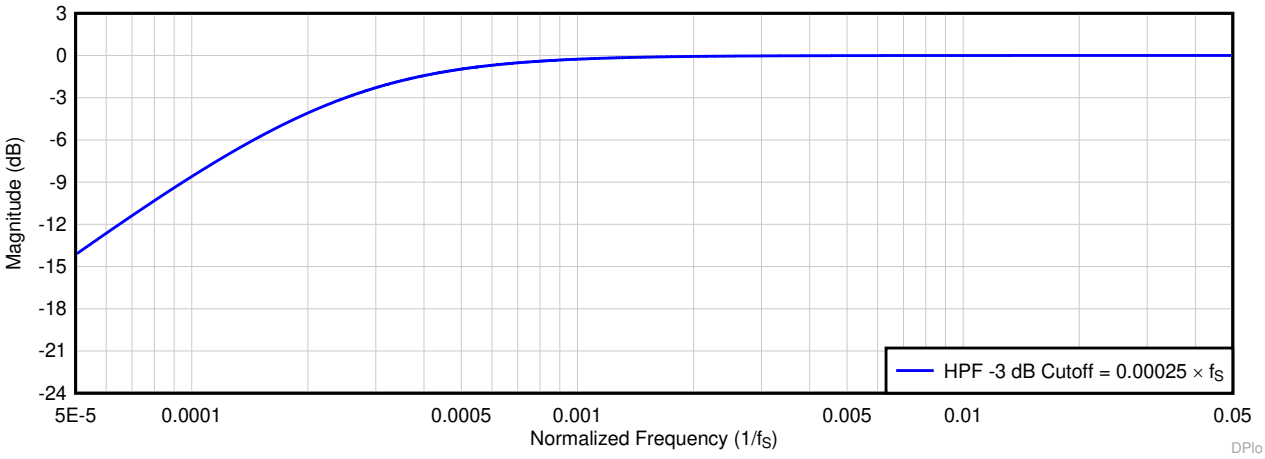


Figure 8-8. HPF Filter Frequency Response Plot

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8.3.6.2 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filter can be chosen from two different types only in slave mode, depending on the required frequency response, group delay, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by the MD0 pin. Table 8-7 shows the decimation filter mode selection for the record channel.

Table 8-7. Decimation Filter Mode Selection for the Record Channel

MD0	DECIMATION FILTER MODE SELECTION (Supported Only in Slave Mode)
LOW	Linear phase filters are used for the decimation in slave mode. For master mode, the device always use linear phase filters for the decimation.
HIGH	Low latency filters are used for the decimation in slave mode. For master mode, the device always use linear phase filters for the decimation.

8.3.6.2.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

8.3.6.2.1.1 Sampling Rate: 8 kHz or 7.35 kHz

Figure 8-9 and Figure 8-10 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 8 kHz or 7.35 kHz. Table 8-8 lists the specifications for a decimation filter with an 8-kHz or 7.35-kHz sampling rate.

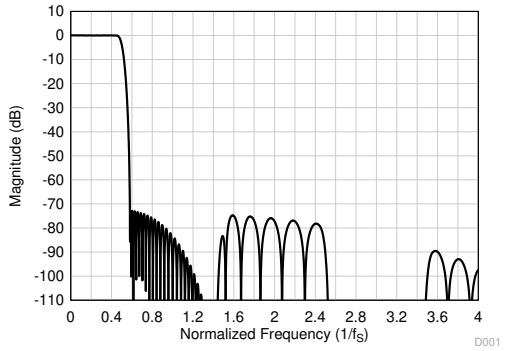


Figure 8-9. Linear Phase Decimation Filter Magnitude Response

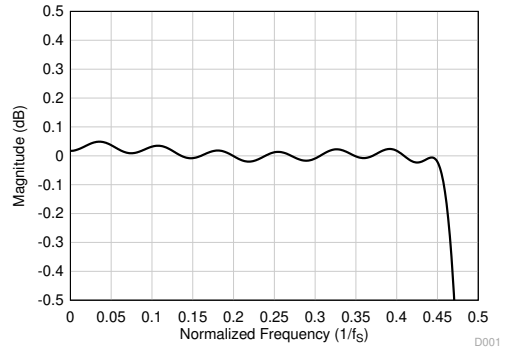


Figure 8-10. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-8. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	72.7			dB
	Frequency range is 4 × f_S onwards	81.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

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8.3.6.2.1.2 Sampling Rate: 16 kHz or 14.7 kHz

Figure 8-11 and Figure 8-12 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 8-9 lists the specifications for a decimation filter with an 16-kHz or 14.7-kHz sampling rate.

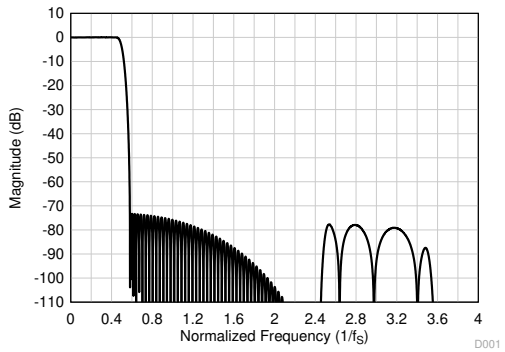


Figure 8-11. Linear Phase Decimation Filter Magnitude Response

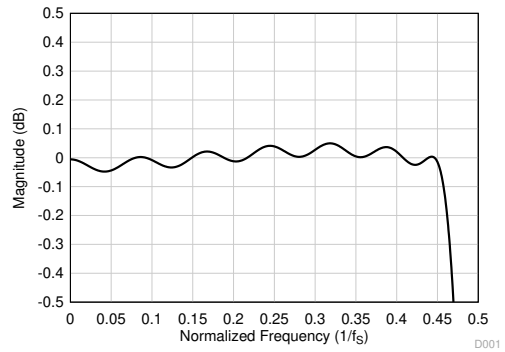


Figure 8-12. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-9. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.3			dB
	Frequency range is 4 × f_S onwards	95.0			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		15.7		1/f_S

8.3.6.2.1.3 Sampling Rate: 24 kHz or 22.05 kHz

Figure 8-13 and Figure 8-14 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 8-10 lists the specifications for a decimation filter with an 24-kHz or 22.05-kHz sampling rate.

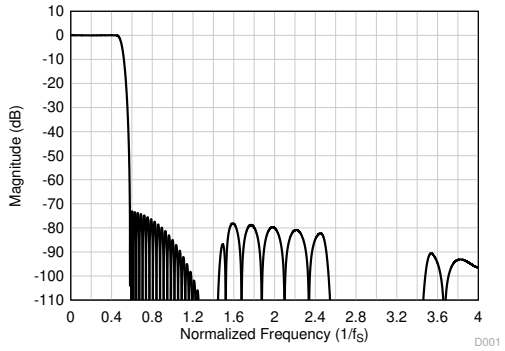


Figure 8-13. Linear Phase Decimation Filter Magnitude Response

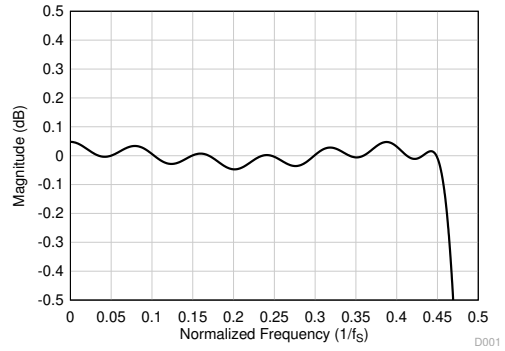


Figure 8-14. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-10. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.0			dB
	Frequency range is 4 × f_S onwards	96.4			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.6		1/f_S

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8.3.6.2.1.4 Sampling Rate: 32 kHz or 29.4 kHz

Figure 8-15 and Figure 8-16 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 8-11 lists the specifications for a decimation filter with an 32-kHz or 29.4-kHz sampling rate.

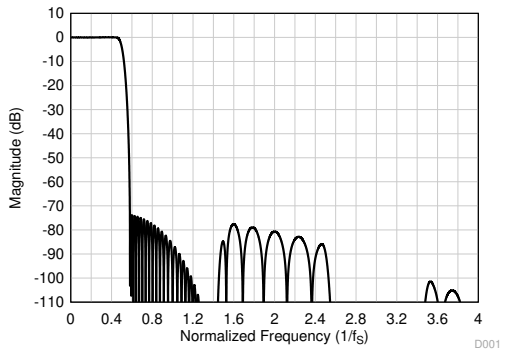


Figure 8-15. Linear Phase Decimation Filter Magnitude Response

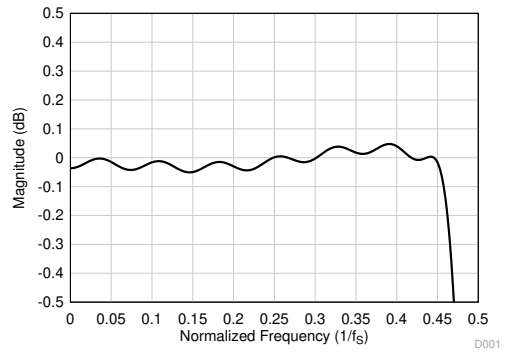


Figure 8-16. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-11. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.7			dB
	Frequency range is 4 × f_S onwards	107.2			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		1/f_S

8.3.6.2.1.5 Sampling Rate: 48 kHz or 44.1 kHz

Figure 8-17 and Figure 8-18 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 8-12 lists the specifications for a decimation filter with an 48-kHz or 44.1-kHz sampling rate.

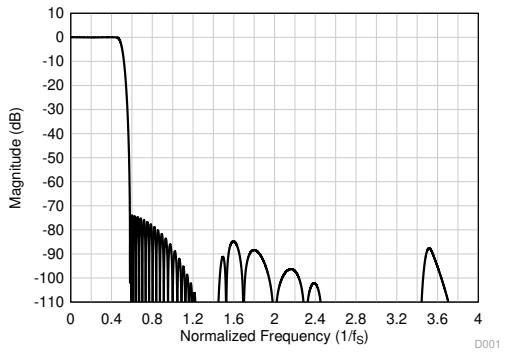


Figure 8-17. Linear Phase Decimation Filter Magnitude Response

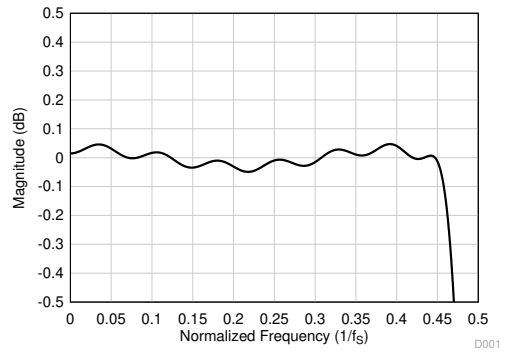


Figure 8-18. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-12. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.8			dB
	Frequency range is 4 × f_S onwards	98.1			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

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8.3.6.2.1.6 Sampling Rate: 96 kHz or 88.2 kHz

Figure 8-19 and Figure 8-20 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 8-13 lists the specifications for a decimation filter with an 96-kHz or 88.2-kHz sampling rate.

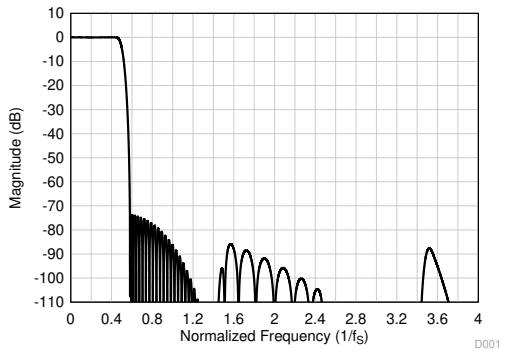


Figure 8-19. Linear Phase Decimation Filter Magnitude Response

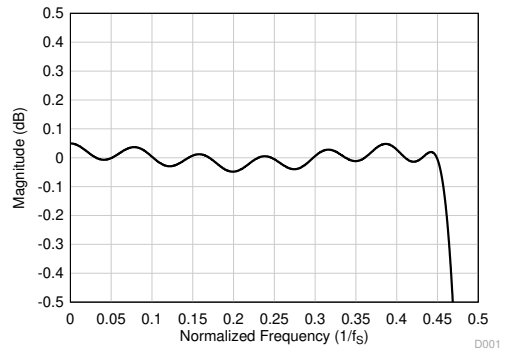


Figure 8-20. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-13. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	73.6			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.1		1/f_S

8.3.6.2.1.7 Sampling Rate: 192 kHz or 176.4 kHz

Figure 8-21 and Figure 8-22 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 192 kHz or 176.4 kHz. Table 8-14 lists the specifications for a decimation filter with an 192-kHz or 176.4-kHz sampling rate.

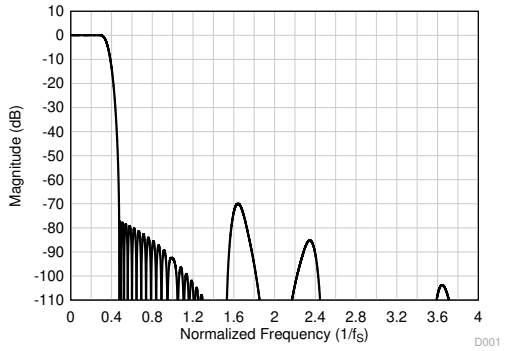


Figure 8-21. Linear Phase Decimation Filter Magnitude Response

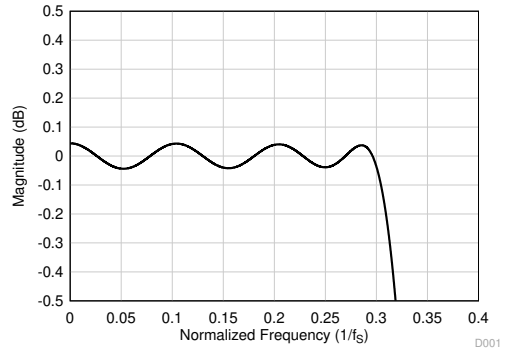


Figure 8-22. Linear Phase Decimation Filter Pass-Band Ripple

Table 8-14. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.3 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.473 × f_S to 4 × f_S	70.0			dB
	Frequency range is 4 × f_S onwards	111.0			
Group delay or latency	Frequency range is 0 to 0.3 × f_S		11.9		1/f_S

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8.3.6.2.2 Low-Latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the PCM1822 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the 0.365 × f_S frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

8.3.6.2.2.1 Sampling Rate: 16 kHz or 14.7 kHz

Figure 8-23 shows the magnitude response and Figure 8-24 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 8-15 lists the specifications for a decimation filter with a 16-kHz or 14.7-kHz sampling rate.

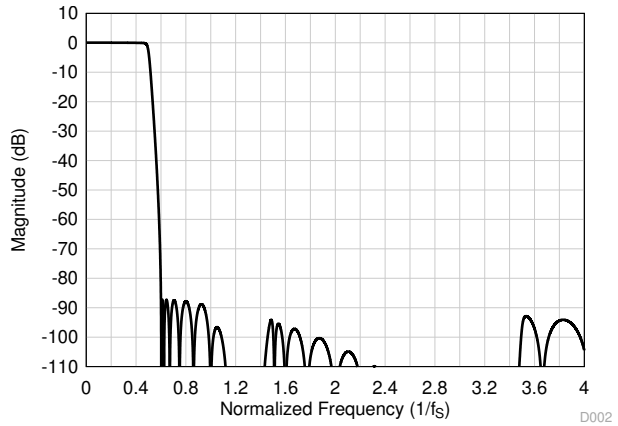


Figure 8-23. Low-Latency Decimation Filter Magnitude Response

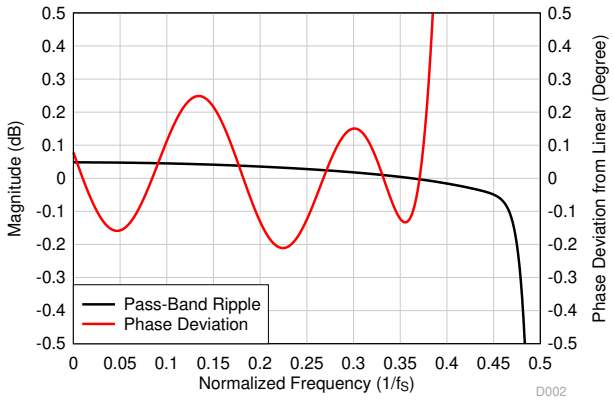


Figure 8-24. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-15. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.451 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.61 × f_S onwards	87.3			dB
Group delay or latency	Frequency range is 0 to 0.363 × f_S		7.6		1/f_S
Group delay deviation	Frequency range is 0 to 0.363 × f_S	–0.022		0.022	1/f_S
Phase deviation	Frequency range is 0 to 0.363 × f_S	–0.21		0.25	Degrees

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8.3.6.2.2.2 Sampling Rate: 24 kHz or 22.05 kHz

Figure 8-25 shows the magnitude response and Figure 8-26 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 8-16 lists the specifications for a decimation filter with a 24-kHz or 22.05-kHz sampling rate.

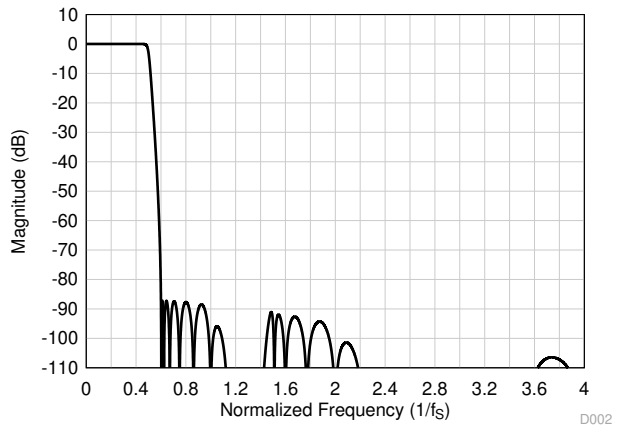


Figure 8-25. Low-Latency Decimation Filter Magnitude Response

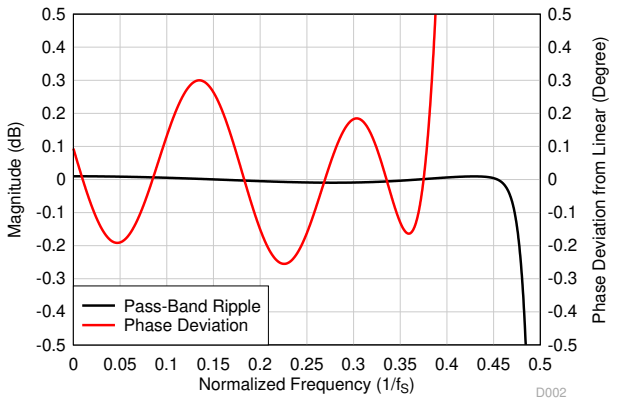


Figure 8-26. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-16. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.459 × f_S	–0.01		0.01	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	87.2			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.5		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

8.3.6.2.2.3 Sampling Rate: 32 kHz or 29.4 kHz

Figure 8-27 shows the magnitude response and Figure 8-28 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 8-17 lists the specifications for a decimation filter with a 32-kHz or 29.4-kHz sampling rate.

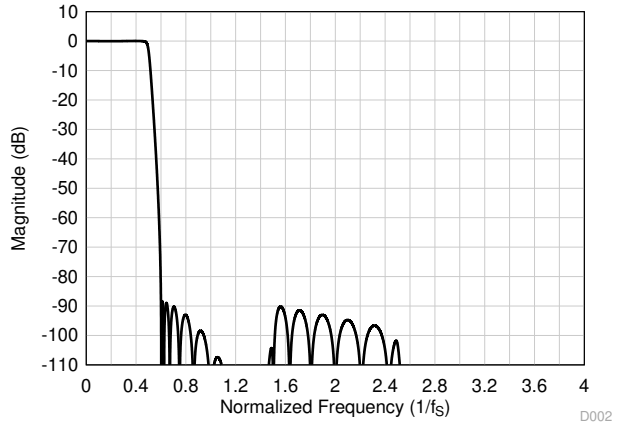


Figure 8-27. Low-Latency Decimation Filter Magnitude Response

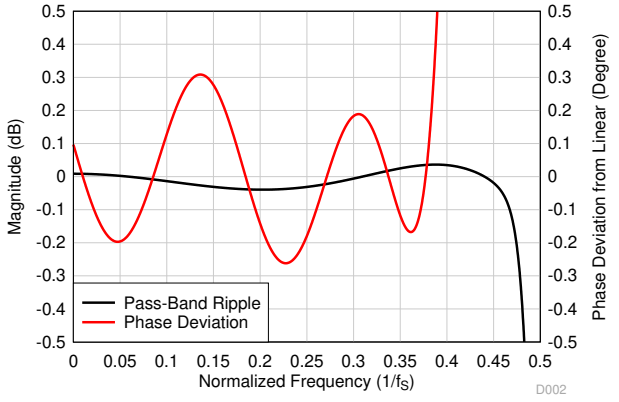


Figure 8-28. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

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Table 8-17. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.457 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	88.3			dB
Group delay or latency	Frequency range is 0 to 0.368 × f_S		8.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.368 × f_S	–0.026		0.026	$1/f_S$
Phase deviation	Frequency range is 0 to 0.368 × f_S	–0.26		0.31	Degrees

8.3.6.2.2.4 Sampling Rate: 48 kHz or 44.1 kHz

Figure 8-29 shows the magnitude response and Figure 8-30 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 8-18 lists the specifications for a decimation filter with a 48-kHz or 44.1-kHz sampling rate.

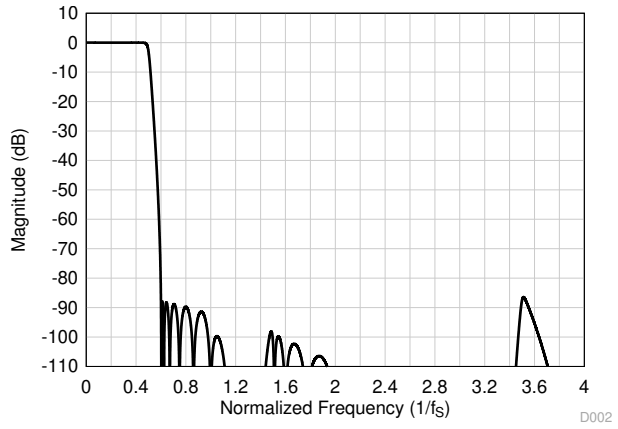


Figure 8-29. Low-Latency Decimation Filter Magnitude Response

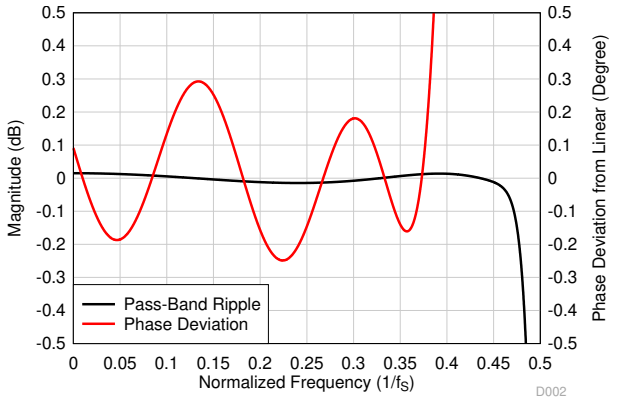


Figure 8-30. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-18. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.015		0.015	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.4			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.25		0.30	Degrees

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8.3.6.2.2.5 Sampling Rate: 96 kHz or 88.2 kHz

Figure 8-31 shows the magnitude response and Figure 8-32 shows the pass-band ripple and phase deviation for a decimation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 8-19 lists the specifications for a decimation filter with a 96-kHz or 88.2-kHz sampling rate.

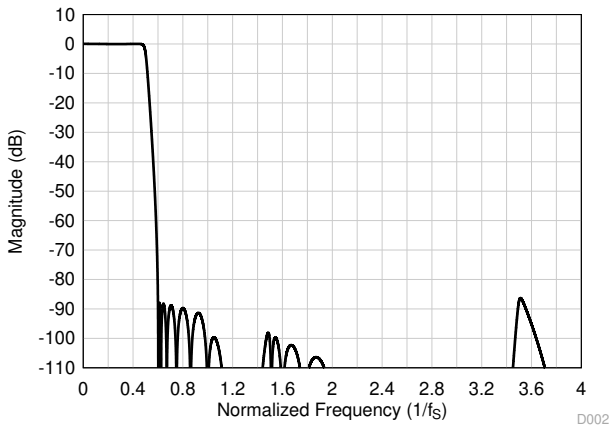


Figure 8-31. Low-Latency Decimation Filter Magnitude Response

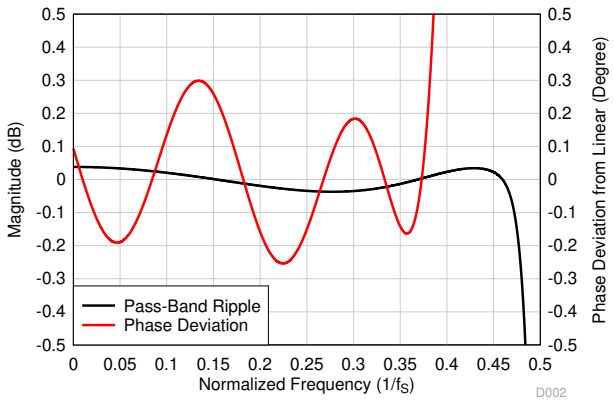


Figure 8-32. Low-Latency Decimation Filter Pass-Band Ripple and Phase Deviation

Table 8-19. Low-Latency Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.466 × f_S	–0.04		0.04	dB
Stop-band attenuation	Frequency range is 0.6 × f_S onwards	86.3			dB
Group delay or latency	Frequency range is 0 to 0.365 × f_S		7.7		$1/f_S$
Group delay deviation	Frequency range is 0 to 0.365 × f_S	–0.027		0.027	$1/f_S$
Phase deviation	Frequency range is 0 to 0.365 × f_S	–0.26		0.30	Degrees

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8.3.7 Dynamic Range Enhancer (DRE)

The device integrates an ultra-low noise front-end DRE gain amplifier with 117-dB dynamic range performance with a low-noise, low-distortion, multibit delta-sigma (ΔΣ) ADC with a 111-dB dynamic range. The dynamic range enhancer (DRE) is a digitally assisted algorithm to boost the overall channel performance. The DRE monitors the incoming signal amplitude and accordingly adjusts the internal DRE amplifier gain automatically. The DRE achieves a complete-channel dynamic range as high as 117 dB. At a system level, the DRE scheme enables far-field, high-fidelity recording of audio signals in very quiet environments and low-distortion recording in loud environments.

The DRE can be enabled only in slave mode by driving the MD1 pin high. Table 8-20 shows the DRE selection for the record channel.

Table 8-20. DRE Selection for the Record Channel

MD1	DRE SELECTION (Supported Only in Slave Mode)
Low	The DRE is disabled in slave mode. For master mode, the DRE is always disabled.
High	The DRE is enabled with DRE_LVL = –36 dB and DRE_MAXGAIN = 18 dB in slave mode. For master mode, the DRE is always disabled.

This algorithm is implemented with very low latency and all signal chain blocks are designed to minimize any audible artifacts that may occur resulting from dynamic gain modulation. The target signal threshold level (DRE_LVL), at which the DRE is triggered, is fixed to the –36-dB input signal level. The DRE gain range can be dynamically modulated by using DRE_MAXGAIN, which is fixed to 18 dB to maximize the benefit of the DRE in real-world applications and to minimize any audible artifacts.

Enabling the DRE for processing increases the power consumption of the device because of increased signal processing. Therefore, disable the DRE for low-power critical applications. Furthermore, the DRE is not supported for output sample rates greater than 48 kHz.

8.4 Device Functional Modes

8.4.1 Active Mode

The device wakes up in active mode when AVDD and IOVDD are available. Configure all hardware control pins (MSZ, MD0, MD1, and FMT0) for the device desired mode of operation before enabling clocks for the device.

In active mode, when the audio clocks are available, the device automatically powers up all ADC channels and starts transmitting data over the audio serial interface. If the clocks are stopped, then the device auto powers down the ADC channels.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The PCM1822 is a multichannel, high-performance audio analog-to-digital converter (ADC) that supports output sample rates of up to 192 kHz. The device supports up to two analog microphones for simultaneous recording applications.

The PCM1822 configuration is supported using various hardware pin control options. The device supports a highly flexible, audio serial interface (TDM and I^2S) to transmit audio data seamlessly in the system across devices.

9.2 Typical Application

Figure 9-1 shows a typical configuration of the PCM1822 for an application using stereo analog microelectrical-mechanical system (MEMS) microphones for simultaneous recording operation with a time-division multiplexing (TDM) audio data slave interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

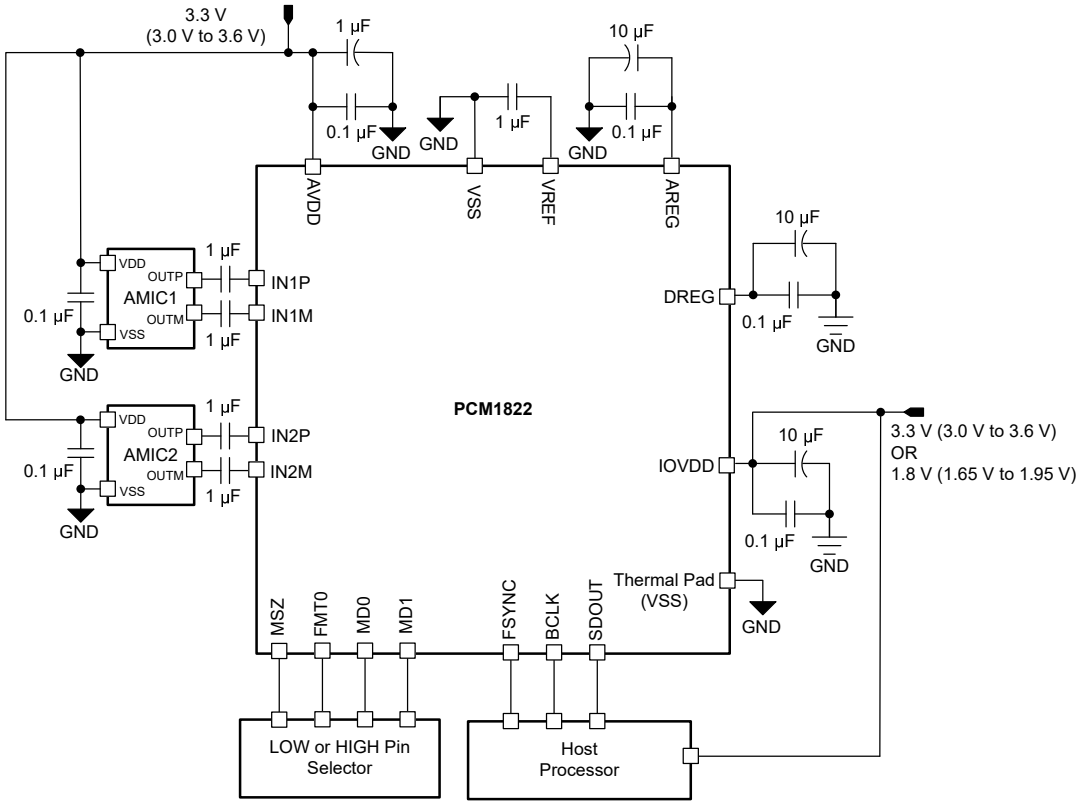


Figure 9-1. Two-Channel Analog Microphone Recording Diagram for 3.3-V AVDD Operation

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9.2.1 Design Requirements

Table 9-1 lists the design parameters for this application.

Table 9-1. Design Parameters

KEY PARAMETER	SPECIFICATION: 3.3-V AVDD OPERATION
AVDD	3.3 V
AVDD supply current consumption	12.9 mA (two-channel recording, f_S = 48 kHz)
IOVDD	1.8 V or 3.3 V

9.2.2 Detailed Design Procedure

This section describes the necessary steps to configure the PCM1822 for this specific application. The following steps provide a sequence of steps that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power-up the IOVDD and AVDD power supplies
   b. The device now goes into low-power mode
2. Configure the pins for correct configuration:
   a. Connect the MSZ, FMT0, MD0, and MD1 pin voltages for the desired configuration
   b. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      See the *Phase-Locked Loop (PLL) and Clock Generation* section for supported sample rates and the BCLK to FSYNC ratio
   c. The device recording data are now sent to the host processor via the audio serial data bus
3. Stop the clocks to stop recording of data at any time

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9.2.3 Application Curves

Measurements are done on the EVM by feeding the device analog input signal using audio precision and with a 3.3-V AVDD supply.

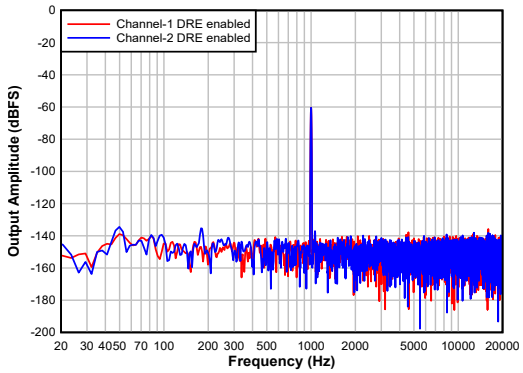


Figure 9-2. FFT With a –60-dBr Input With DRE Enabled

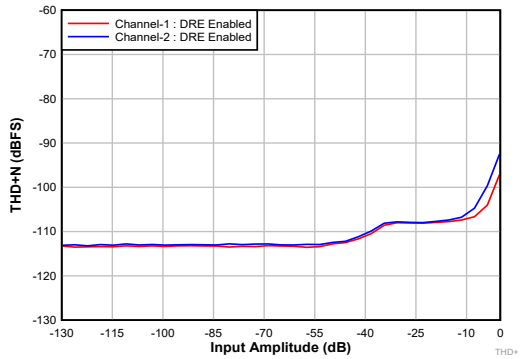


Figure 9-3. THD+N vs Input Amplitude With DRE Enabled

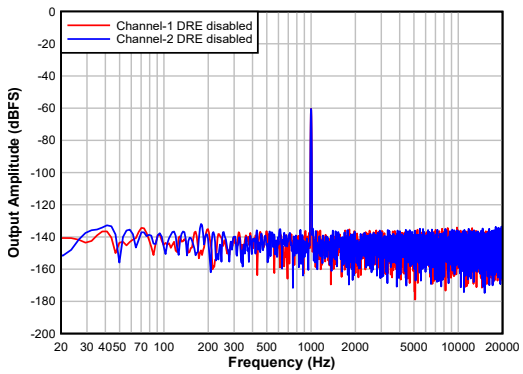


Figure 9-4. FFT With a –60-dBr Input With DRE Disabled

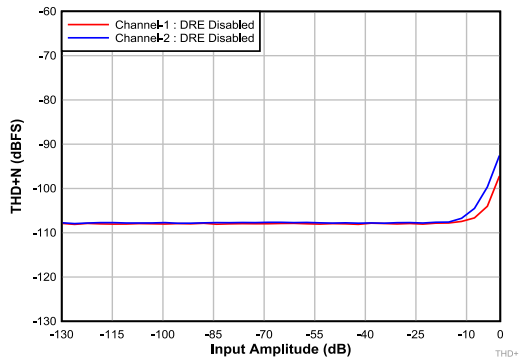


Figure 9-5. THD+N vs Input Amplitude With DRE Disabled

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10 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, do not provide any clocks until the IOVDD and AVDD supply voltage settles to a stable and supported operating voltage range. Provide the clocks (FSYNC and BCLK) only when all hardware control pins (MSZ, MD0, MD1, FMT0, and FMT1) are driven to the voltage level for the device desired mode of operation.

For the supply power-up requirement, t_1 and t_2 must be at least 100 µs. For the supply power-down requirement, t_3 and t_4 must be at least 10 ms. This timing (as shown in Figure 10-1) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into hardware shutdown mode.

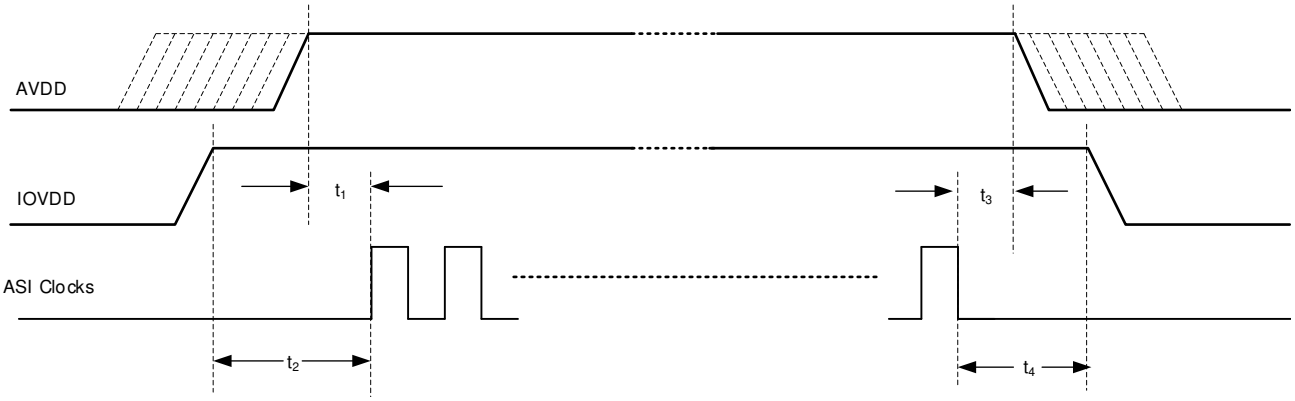


Figure 10-1. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 1 V/µs and that the wait time between a power-down and a power-up event is at least 100 ms.

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11 Layout

11.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for optimal performance.
- Directly short the VREF external capacitor ground terminal to the AVSS pin without using any vias for this connection trace.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

11.2 Layout Example

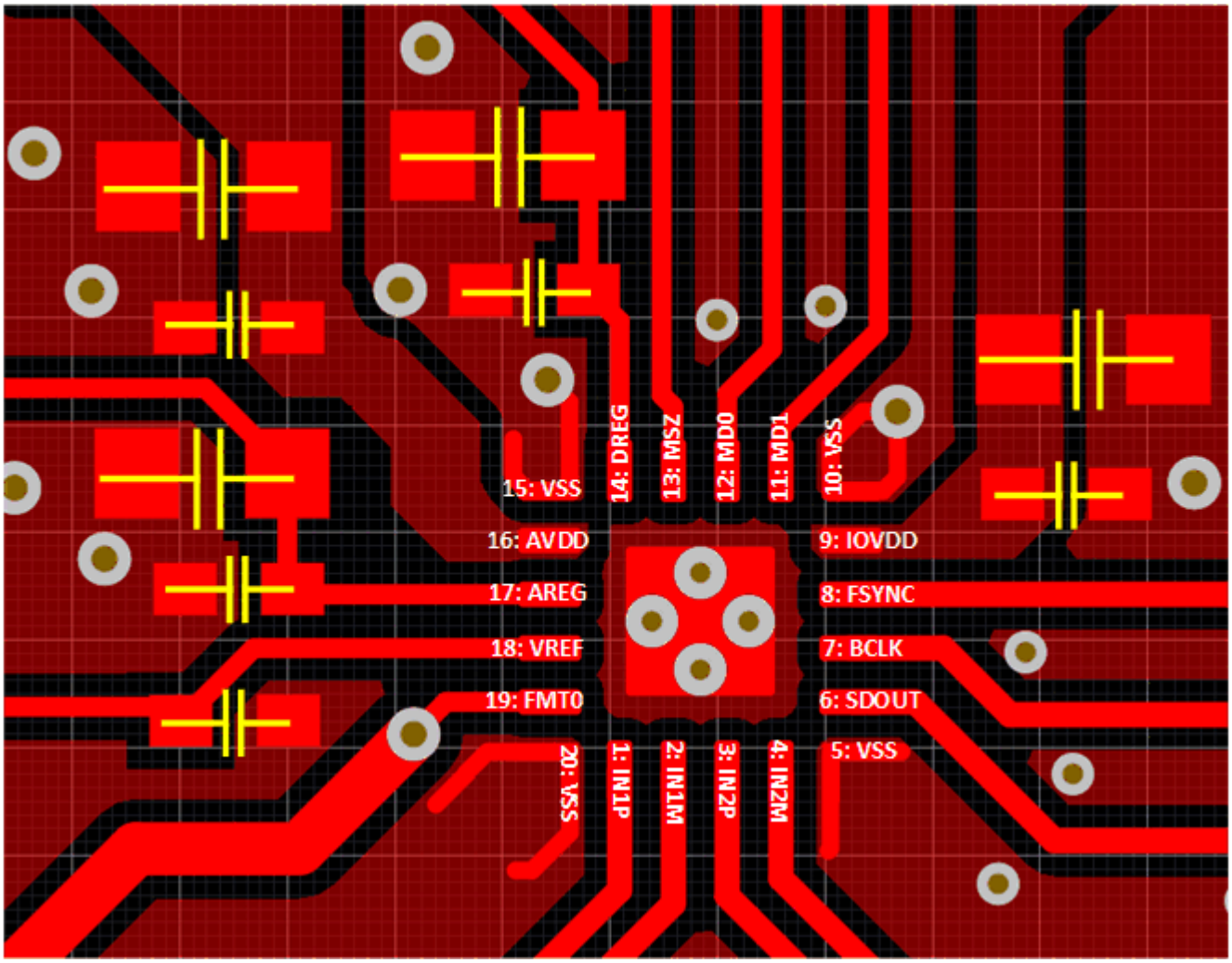


Figure 11-1. Example Layout

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1822IRTER	Active	Production	WQFN (RTE) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PC1822
PCM1822IRTER.A	Active	Production	WQFN (RTE) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PC1822

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF PCM1822 :

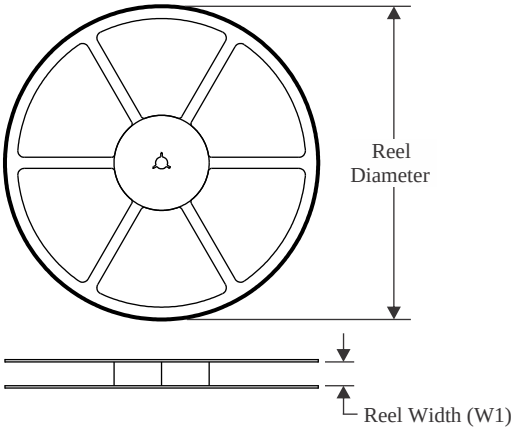
- Automotive : PCM1822-Q1

NOTE: Qualified Version Definitions:

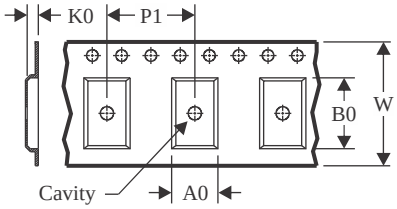
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

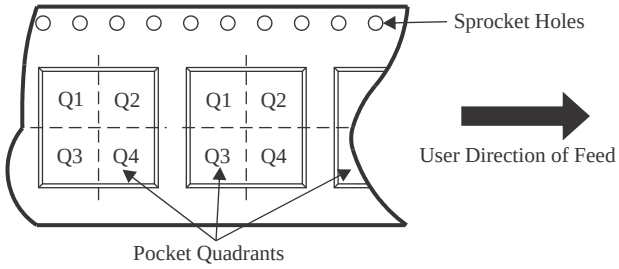


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

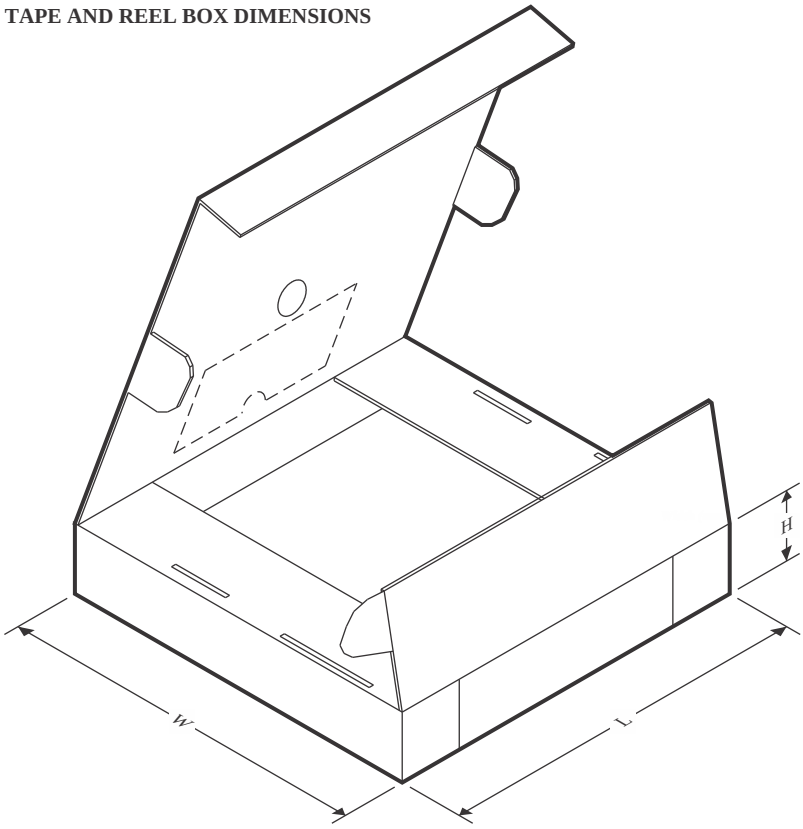
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1822IRTER	WQFN	RTE	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

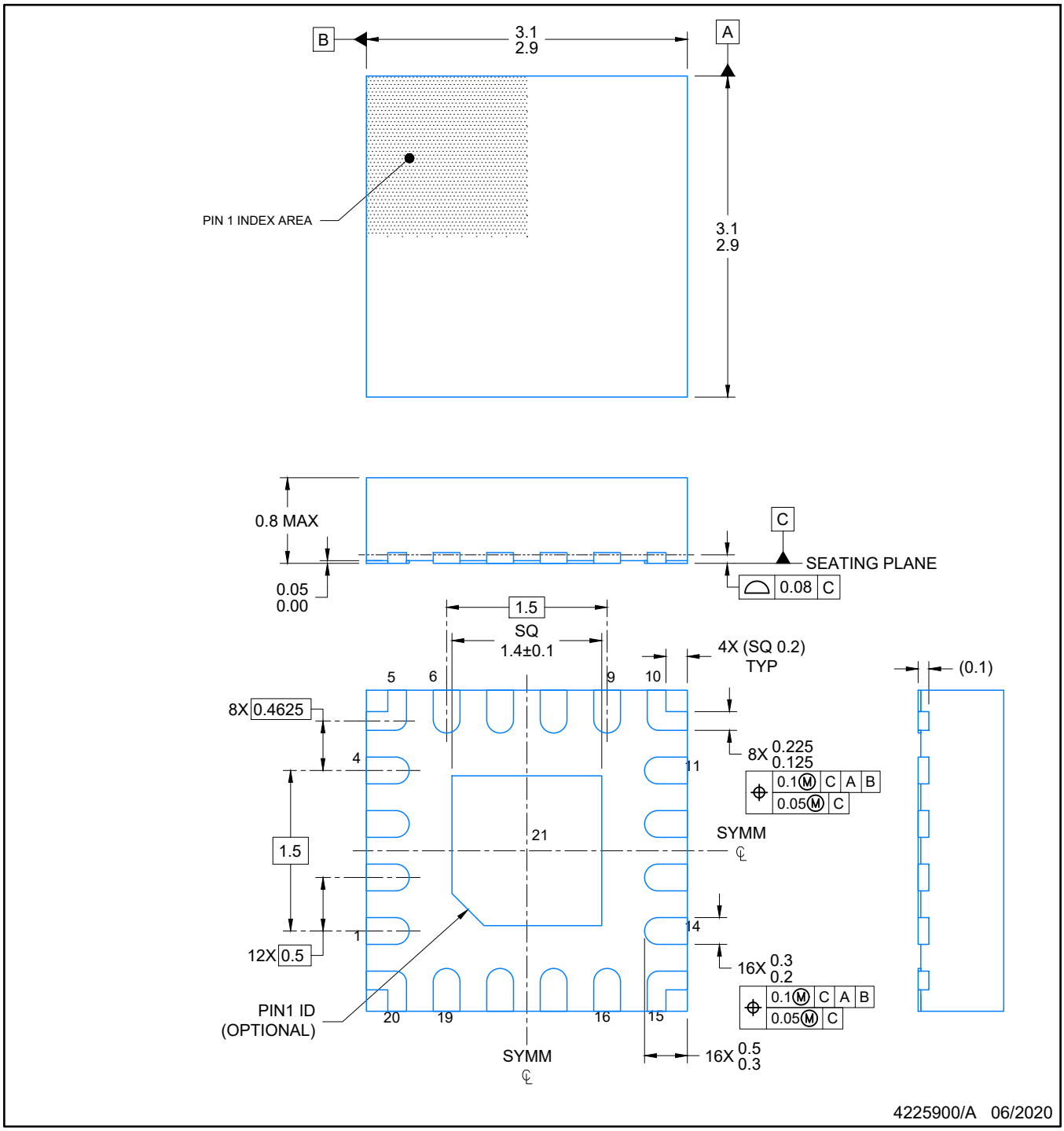
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1822IRTER	WQFN	RTE	20	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RTE0020A

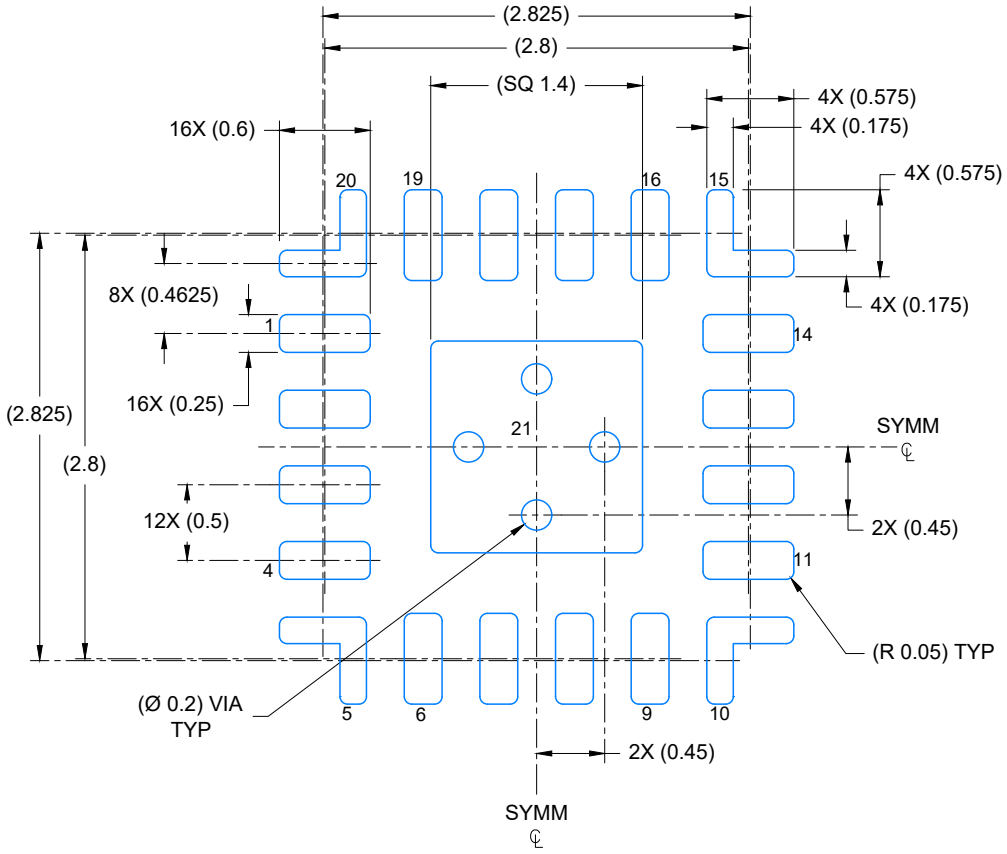
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

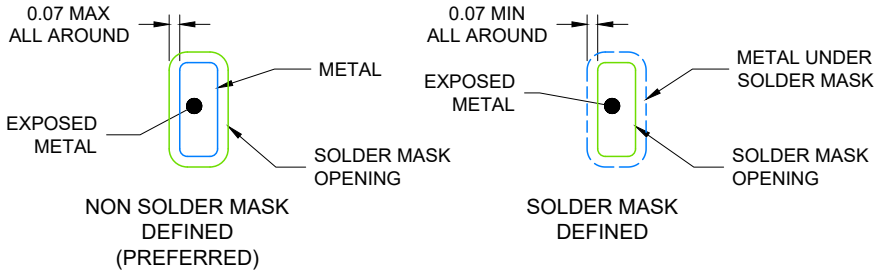


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

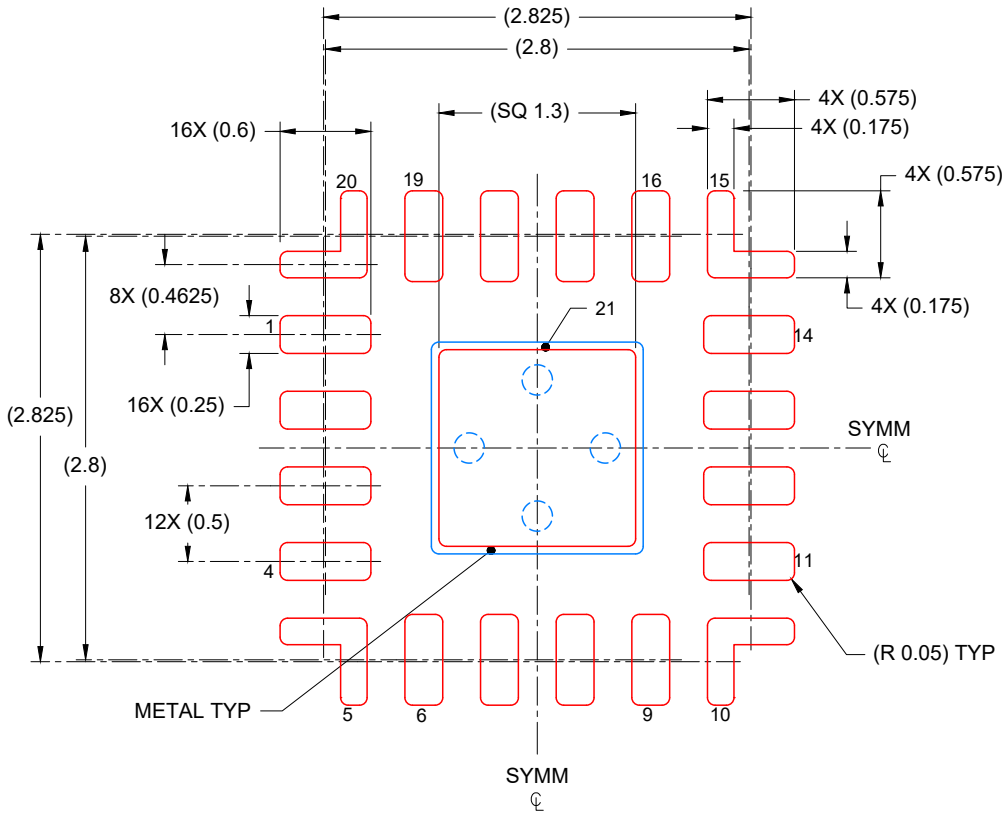


SOLDER MASK DETAILS

4225900/A 06/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
86% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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