AMC1305x-Q1
High-Precision, Reinforced Isolated Delta-Sigma Modulators

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Temperature Grade 1: –40°C to +125°C
  - HBM ESD Classification Level 2
  - CDM ESD Classification Level C6
- Pin-Compatible Family With:
  - ±50-mV or ±250-mV Input Voltage Ranges
  - CMOS or LVDS Digital Interface Options
- Excellent DC Performance:
  - Offset Error: ±50 µV or ±150 µV (max)
  - Offset Drift: 1.3 µV/°C (max)
  - Gain Error: ±0.3% (max)
  - Gain Drift: ±40 ppm/°C (max)
- Safety-Related Certifications:
  - 7000-V_{PK} Reinforced Isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 5000-V_{RMS} Isolation for 1 Minute per UL1577
  - CAN/CSA No. 5A-Component Acceptance Service Notice
- Transient Immunity: 15 kV/µs (min)
- High Electromagnetic Field Immunity (see Application Note SLLA181A)
- External 5-MHz to 20-MHz Clock Input

2 Applications

- Shunt-Based Current Sensing or Resistor-Divider-Based Voltage Sensing In:
  - Traction Inverters
  - Onboard Chargers (OBC)
  - DC-DC Converters
  - Battery Management Systems (BMS)

3 Description

The AMC1305-Q1 device is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-10, UL1577, and CSA standards. Used in conjunction with isolated power supplies, the device prevents noise currents on a high common-mode voltage line from entering the local system ground and interfering with or damaging low voltage circuitry.

The AMC1305-Q1 is optimized for direct connection to shunt resistors or other low voltage level signal sources and supports excellent dc and ac performance. Shunt resistors are typically used to sense currents in traction inverters, onboard chargers, or other such automotive applications. By using an appropriate digital filter (that is, as integrated on the TMS320F2837x) to decimate the bit stream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB (13.8 ENOB) at a data rate of 78 kSPS.

On the high-side, the modulator is supplied with a nominal voltage of 5 V (AVDD), whereas the isolated digital interface operates from a 3.3-V or 5-V power supply (DVDD).

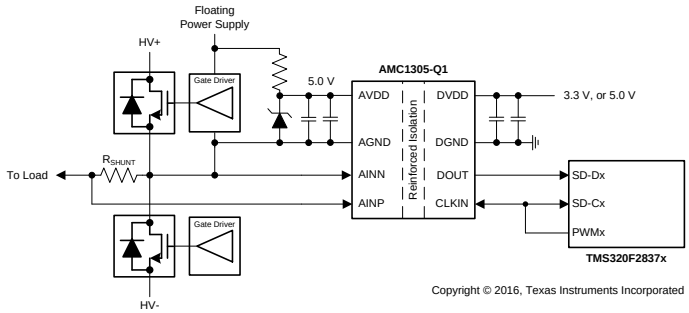
The AMC1305-Q1 is available in a wide-body SOIC-16 (DW) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1305x-Q1	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

DATE	REVISION	NOTES
February 2017	*	Initial release.

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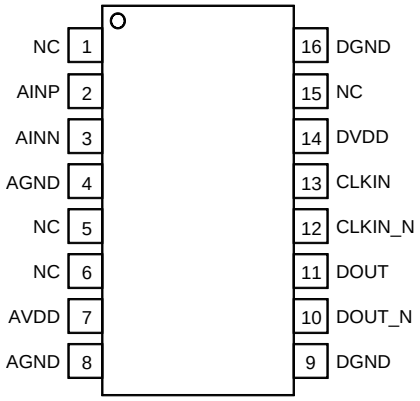
5 Device Comparison Table

PART NUMBER	INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	SNR (sinc^3 Filter, 78 kSPS)	OUTPUT INTERFACE
AMC1305L25-Q1	±250 mV	25 kΩ	82 dB	LVDS
AMC1305M05-Q1	±50 mV	5 kΩ	76 dB	CMOS
AMC1305M25-Q1	±250 mV	25 kΩ	82 dB	CMOS

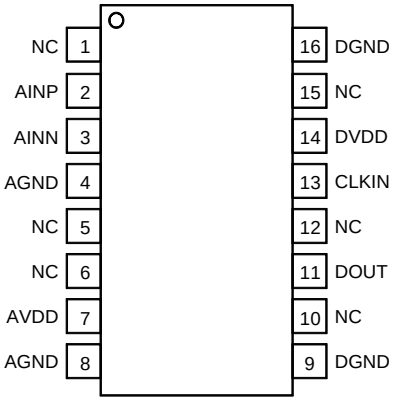
6 Pin Configurations and Functions

DW Package
16-Pin SOIC
Top View



LVDS Versions (AMC1305L25-Q1)

DW Package
16-Pin SOIC
Top View



CMOS Versions (AMC1305Mx-Q1)

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	4	—	This pin is internally connected to pin 8 and can be left unconnected or tied to high-side ground
	8	—	High-side ground reference
AINN	3	I	Inverting analog input
AINP	2	I	Noninverting analog input
AVDD	7	—	High-side power supply, 4.5 V to 5.5 V. See the *Power-Supply Recommendations* section for decoupling recommendations.
CLKIN	13	I	Modulator clock input, 5 MHz to 20.1 MHz
CLKIN_N	12	I	AMC1305L25-Q1 only: inverted modulator clock input
DGND	9, 16	—	Controller-side ground reference
DOUT	11	O	Modulator data output
DOUT_N	10	O	AMC1305L25-Q1 only: inverted modulator data output
DVDD	14	—	Controller-side power supply, 3.0 to 5.5 V
NC	1	—	This pin can be connected to AVDD or can be left unconnected
	5	—	This pin can be left unconnected or tied to AGND only
	6, 10, 12	—	These pins have no internal connection (pins 10 and 12 on the AMC1305Mx-Q1 only).
	15	—	This pin can be left unconnected or tied to DVDD only

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7 Specifications

7.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, AVDD to AGND or DVDD to DGND	–0.3	6.5	V
Analog input voltage at AINP, AINN	AGND – 6	AVDD + 0.5	V
Digital input voltage at CLKIN, CLKIN_N	DGND – 0.3	DVDD + 0.3	V
Input current to any pin except supply pins	–10	10	mA
Maximum virtual junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2500	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	High-side (analog) supply voltage	4.5	5.0	5.5	V
DVDD	Controller-side (digital) supply voltage	3.0	3.3	5.5	V
T_A	Operating ambient temperature range	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		AMC1305x-Q1 DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = 5.5 V, DVDD = 5.5 V, LVDS, R_{LOAD} = 100 Ω	89.1	mW
P_{D1}	Maximum power dissipation (high-side supply)	AVDD = 5.5 V	45.1	mW
P_{D2}	Maximum power dissipation (low-side supply)	DVDD = 5.5 V, LVDS, R_{LOAD} = 100 Ω	44	mW

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7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	Minimum air gap (clearance)(1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	Minimum external tracking (creepage)(1)	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0135 mm)	0.027	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar or unipolar)	1414	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	1000	V_{RMS}
		At dc voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 1697\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM} = 2263\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM} = 2652\ V_{PK}$, t_m = 1 s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	1.2	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_S = 150°C	> 10^9	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS} or 7000 V_{DC}, t = 60 s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves or ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

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7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60095 (VDE 0860): 2005-11	Recognized under UL1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
File number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry may allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 80.2°C/W, AVDD = DVDD = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 3			283	mA
		θ_{JA} = 80.2°C/W, AVDD = DVDD = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 3			432	mA
P_S	Safety input, output, or total power	θ_{JA} = 80.2°C/W, T_J = 150°C, T_A = 25°C, see Figure 4			1558 (1)	mW
T_S	Maximum safety temperature				150	°C

(1) Input, output, or the sum of input and output power must not exceed this value.

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

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7.9 Electrical Characteristics: AMC1305M05-Q1

All minimum and maximum specifications at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 3.0 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Maximum differential voltage input range (AINP-AINN)			±62.5		mV
FSR	Specified linear full-scale range (AINP-AINN)		–50		50	mV
V_{CM}	Operating common-mode input range		–0.032		AVDD – 2	V
C_{ID}	Differential input capacitance			2		pF
I_{IB}	Input current	Inputs shorted to AGND	–97	–72	-57	µA
R_{ID}	Differential input resistance			5		kΩ
I_{OS}	Input offset current			±5		nA
CMTI	Common-mode transient immunity		15			kV/µs
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–104		dB
		f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–75		
BW	Input bandwidth			800		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(1)	Resolution: 16 bits	–5	±1.5	5	LSB
E_O	Offset error	Initial, at 25°C	–50	±2.5	50	µV
TCE_O	Offset error thermal drift(2)		–1.3		1.3	µV/°C
E_G	Gain error	Initial, at 25°C	–0.3%	–0.02%	0.3%	
TCE_G	Gain error thermal drift(3)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	V_{AVDD} from 4.5 to 5.5V, at dc		105		dB
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	76	81		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	76	81		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz		–90	–83	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	83	92		dB
DIGITAL INPUTS/OUTPUTS						
External Clock						
f_{CLKIN}	Input clock frequency		5	20	20.1	MHz
$Duty_{CLKIN}$	Duty cycle	5 MHz ≤ f_{CLKIN} ≤ 20.1 MHz	40%	50%	60%	
CMOS Logic Family, CMOS with Schmitt-Trigger						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	–1		1	µA
C_{IN}	Input capacitance			5		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance	f_{CLKIN} = 20 MHz		30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.

(2) Offset error drift is calculated using the box method as described by the following equation: $TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$

(3) Gain error drift is calculated using the box method as described by the following equation: $TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$

Electrical Characteristics: AMC1305M05-Q1 (continued)

All minimum and maximum specifications at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 3.0 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	High-side supply voltage		4.5	5.0	5.5	V
I_{AVDD}	High-side supply current			6.5	8.2	mA
P_{AVDD}	High-side power dissipation			32.5	45.1	mW
DVDD	Controller-side supply voltage		3.0	3.3	5.5	V
I_{DVDD}	Controller-side supply current	3.0 V ≤ DVDD ≤ 3.6 V		2.7	4.0	mA
		4.5 V ≤ DVDD ≤ 5.5 V		3.2	5.5	
P_{DVDD}	Controller-side power dissipation	3.0 V ≤ DVDD ≤ 3.6 V		8.9	14.4	mW
		4.5 V ≤ DVDD ≤ 5.5 V		16.0	30.3	

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7.10 Electrical Characteristics: AMC1305x25-Q1

All minimum and maximum specifications at T_A = –40°C to 125°C, AVDD = 4.5 V to 5.5 V, DVDD = 3.0 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Maximum differential voltage input range (AINP-AINN)			±312.5		mV
FSR	Specified linear full-scale range (AINP-AINN)		–250		250	mV
V_{CM}	Operating common-mode input range		–0.16		AVDD – 2	V
C_{ID}	Differential input capacitance			1		pF
I_{IB}	Input current	Inputs shorted to AGND	–82	–60	–48	µA
R_{ID}	Differential input resistance			25		kΩ
I_{OS}	Input offset current			±5		nA
CMTI	Common-mode transient immunity		15			kV/µs
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–95		dB
		f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–76		
BW	Input bandwidth			1000		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(1)	Resolution: 16 bits	–4	±1.5	4	LSB
E_O	Offset error	Initial, at 25°C	–150	±40	150	µV
TCE_O	Offset error thermal drift(2)		–1.3		1.3	µV/°C
E_G	Gain error	Initial, at 25°C	–0.3	–0.02	0.3	%FS
TCE_G	Gain error thermal drift(3)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	V_{AVDD} from 4.5 V to 5.5 V, at dc		90		dB
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	82	85		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	80	84		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz		–90	–83	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	83	92		dB
DIGITAL INPUTS/OUTPUTS						
External Clock						
f_{CLKIN}	Input clock frequency		5	20	20.1	MHz
$Duty_{CLKIN}$	Duty cycle	5 MHz ≤ f_{CLKIN} ≤ 20.1 MHz	40%	50%	60%	
CMOS Logic Family (AMC1305M25-Q1), CMOS with Schmitt-Trigger						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	–1		1	µA
C_{IN}	Input capacitance			5		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance	f_{CLKIN} = 20 MHz		30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or as a percent of the specified linear full-scale range FSR.

(2) Offset error drift is calculated using the box method as described by the following equation: $TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$

(3) Gain error drift is calculated using the box method as described by the following equation: $TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$

Electrical Characteristics: AMC1305x25-Q1 (continued)

All minimum and maximum specifications at T_A = –40°C to 125°C, AVDD = 4.5 V to 5.5 V, DVDD = 3.0 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5.0 V, and DVDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Logic Family (AMC1305L25-Q1)						
V_{OD}	Differential output voltage	R_{LOAD} = 100 Ω	250	350	450	mV
V_{OCM}	Output common-mode voltage		1.125	1.23	1.375	V
I_S	Output short-circuit current				24	mA
V_{ICM}	Input common-mode voltage	V_{ID} = 100 mV	0.05	1.25	3.25	V
V_{ID}	Differential input voltage		100	350	600	mV
I_{IN}	Input current	DGND ≤ V_{IN} ≤ 3.3 V	–24	0	20	µA
POWER SUPPLY						
AVDD	High-side supply voltage		4.5	5.0	5.5	V
I_{AVDD}	High-side supply current			6.5	8.2	mA
P_{AVDD}	High-side power dissipation			32.5	45.1	mW
DVDD	Controller-side supply voltage		3.0	3.3	5.5	V
I_{DVDD}	Controller-side supply current	AMC1305L25-Q1, R_{LOAD} = 100 Ω		6.1	8.0	mA
		AMC1305M25-Q1, 3.0 ≤ DVDD ≤ 3.6 V, C_{LOAD} = 5 pF		2.7	4.0	
		AMC1305M25-Q1, 4.5 ≤ DVDD ≤ 5.5 V, C_{LOAD} = 5 pF		3.2	5.5	
P_{DVDD}	Controller-side power dissipation	AMC1305L25-Q1, R_{LOAD} = 100 Ω		20.1	44.0	mW
		AMC1305M25-Q1, 3.0 ≤ DVDD ≤ 3.6 V, C_{LOAD} = 5 pF		8.9	14.4	
		AMC1305M25-Q1, 4.5 ≤ DVDD ≤ 5.5 V, C_{LOAD} = 5 pF		16.0	30.3	

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7.11 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLKIN, CLKIN_N clock period	49.75	50	200	ns
t_{HIGH}	CLKIN, CLKIN_N clock high time	19.9	25	120	ns
t_{LOW}	CLKIN, CLKIN_N clock low time	19.9	25	120	ns
t_D	Falling edge of CLKIN, CLKIN_N to DOUT, DOUT_N valid delay, C_{LOAD} = 5 pF	0		15	ns
t_{ISTART}	Interface startup time (DVDD at 3.0 V min to DOUT, DOUT_N valid with AVDD ≥ 4.5 V)	32		32	CLKIN cycles
t_{ASTART}	Analog startup time (AVDD step up to 4.5 V with DVDD ≥ 3.0 V)		1		ms

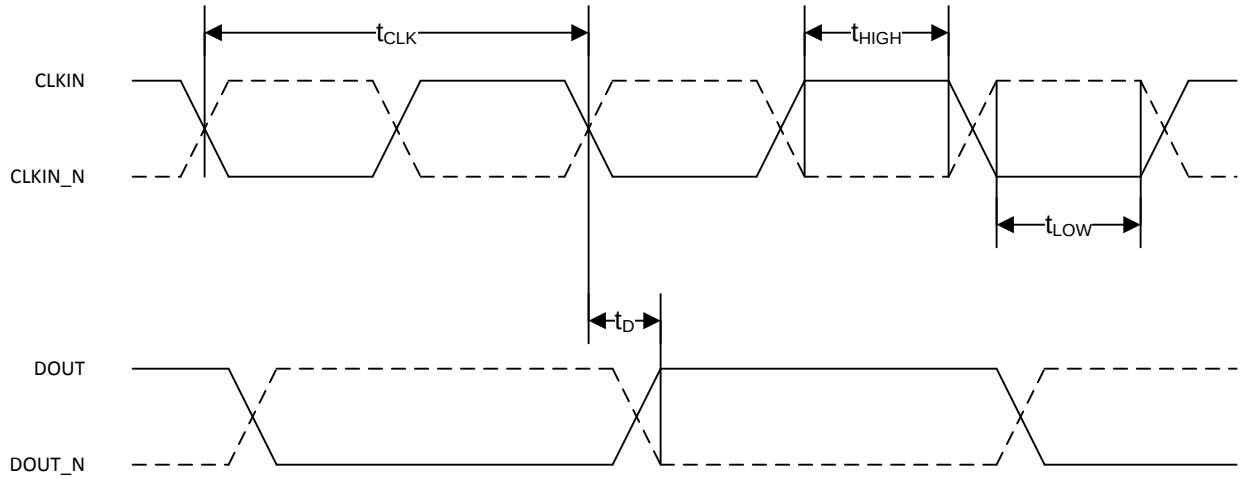


Figure 1. Digital Interface Timing

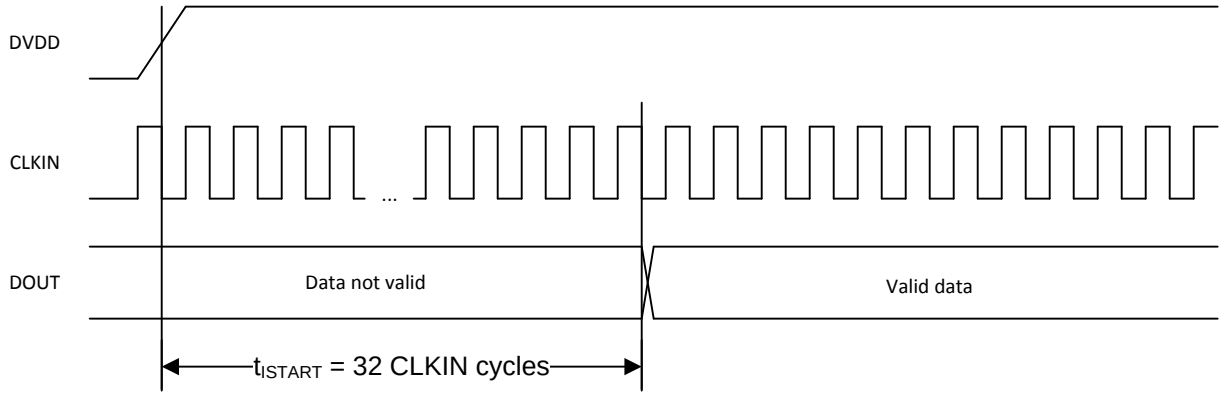


Figure 2. Digital Interface Startup Timing

7.12 Insulation Characteristics Curves

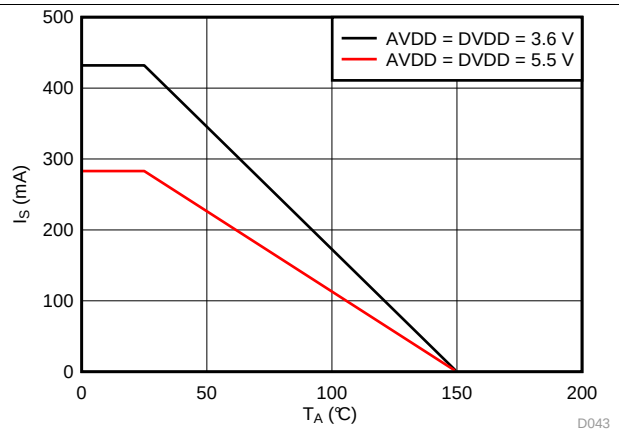


Figure 3. Thermal Derating Curve for Safety Limiting Current per VDE

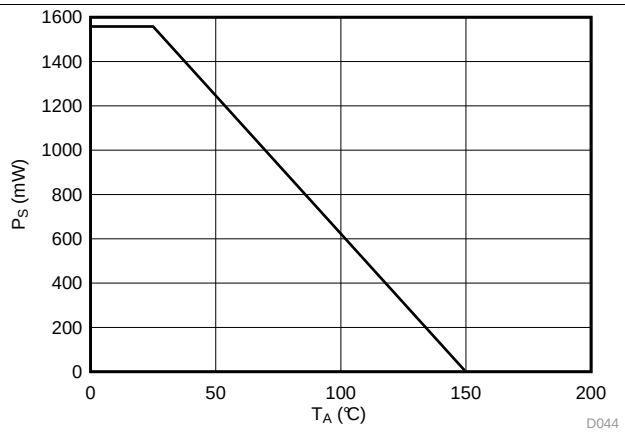
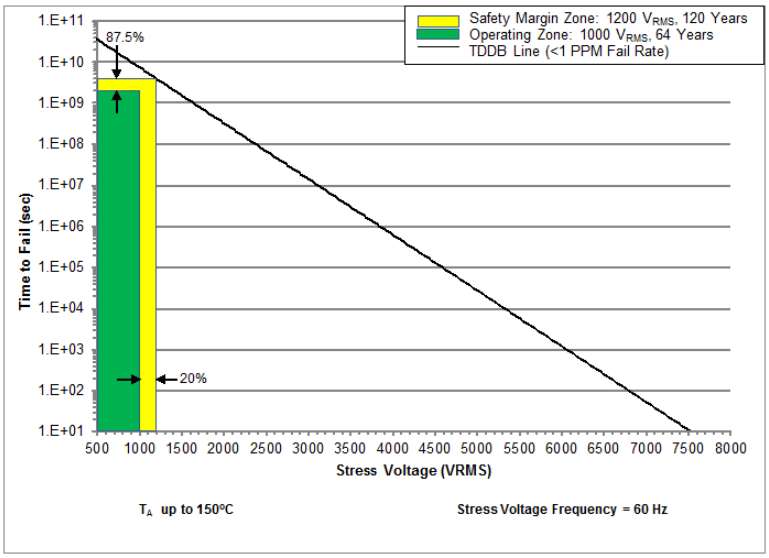


Figure 4. Thermal Derating Curve for Safety Limiting Power per VDE



T_A up to 150°C, stress voltage frequency = 60 Hz

Figure 5. Reinforced Isolation Capacitor Lifetime Projection

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7.13 Typical Characteristics

At T_A = 25°C, AVDD = 5.0 V, DVDD = 3.3 V, AINP = –250 mV to 250 mV, AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

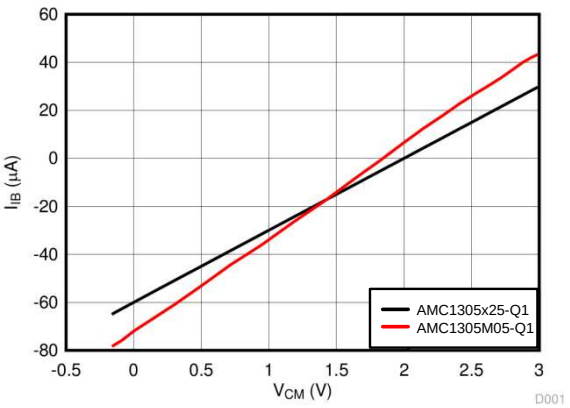


Figure 6. Input Current vs Input Common-Mode Voltage

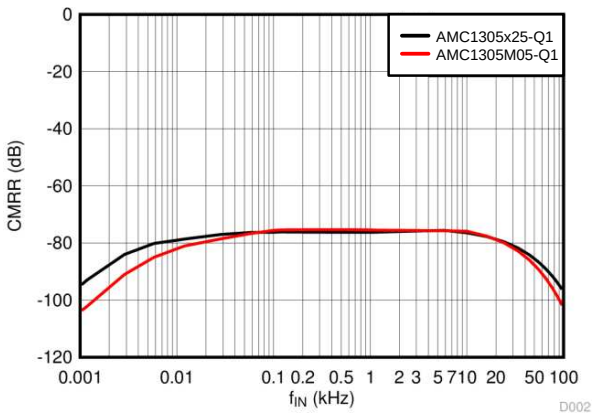


Figure 7. Common-Mode Rejection Ratio vs Input Signal Frequency

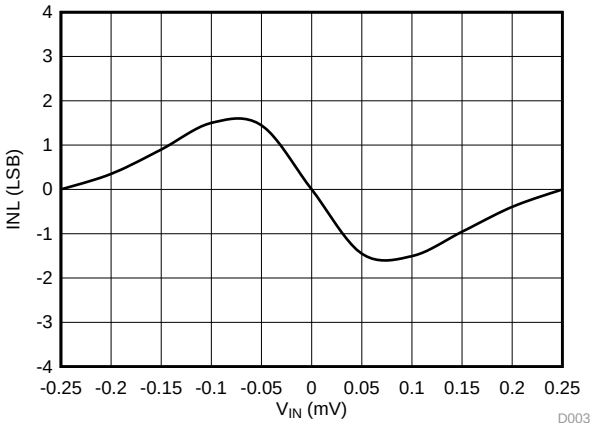


Figure 8. Integral Nonlinearity vs Input Signal Amplitude

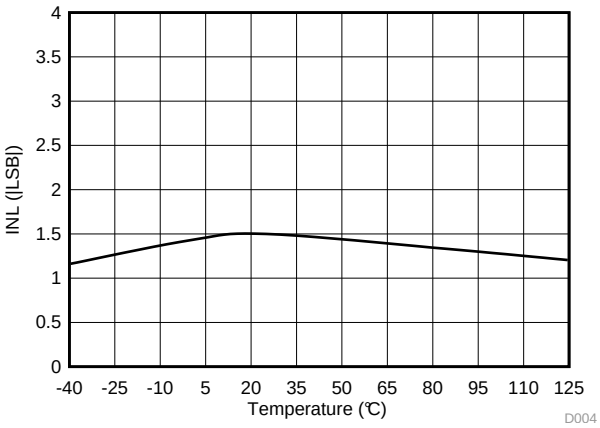
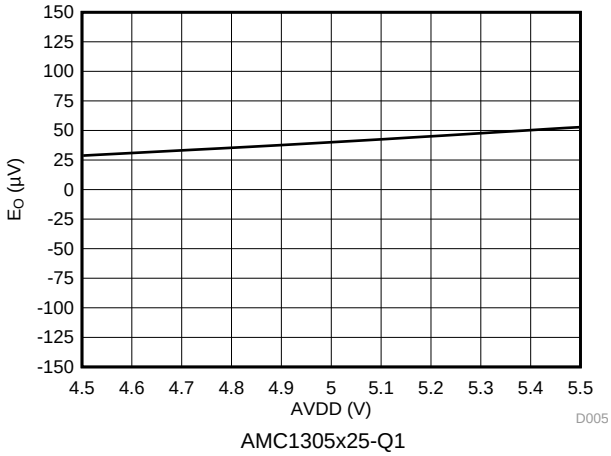
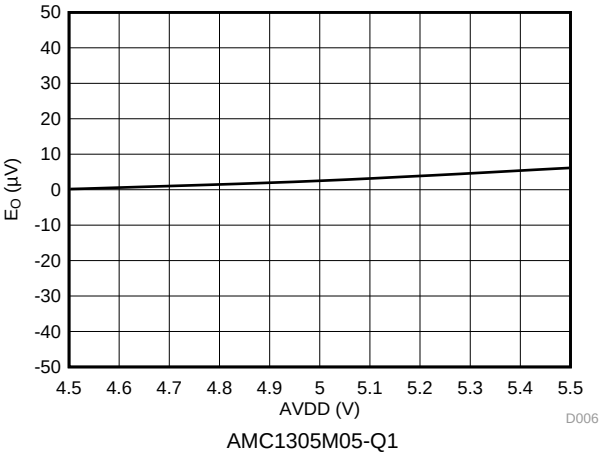


Figure 9. Integral Nonlinearity vs Temperature



AMC1305x25-Q1

Figure 10. Offset Error vs High-Side Supply Voltage



AMC1305M05-Q1

Figure 11. Offset Error vs High-Side Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 5.0 V, DVDD = 3.3 V, AINP = –250 mV to 250 mV, AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

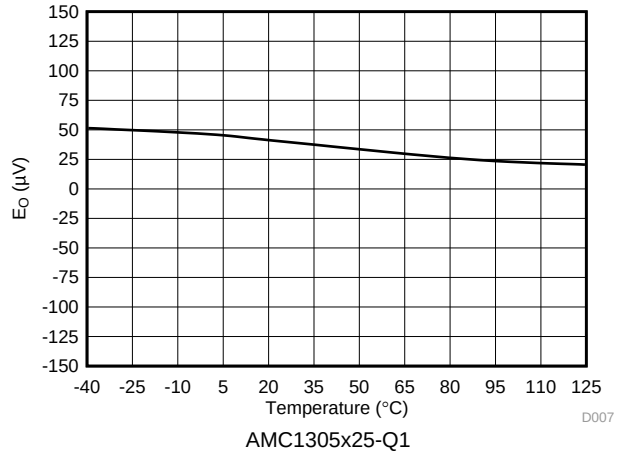


Figure 12. Offset Error vs Temperature

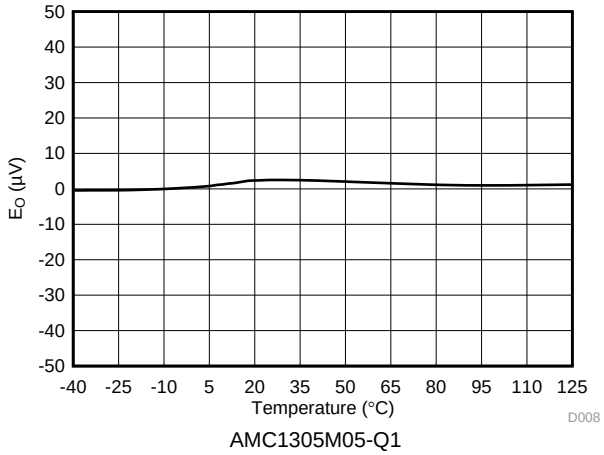


Figure 13. Offset Error vs Temperature

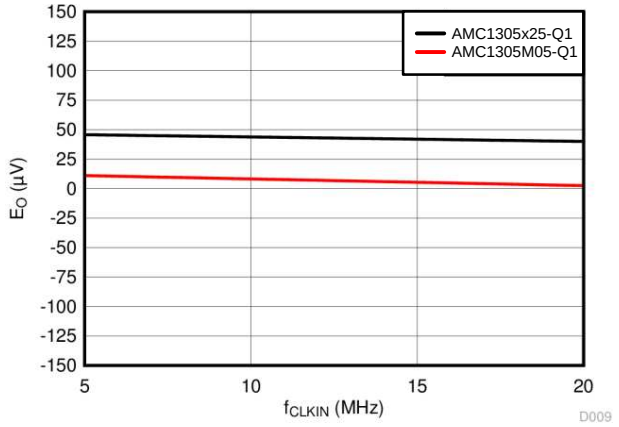


Figure 14. Offset Error vs Clock Frequency

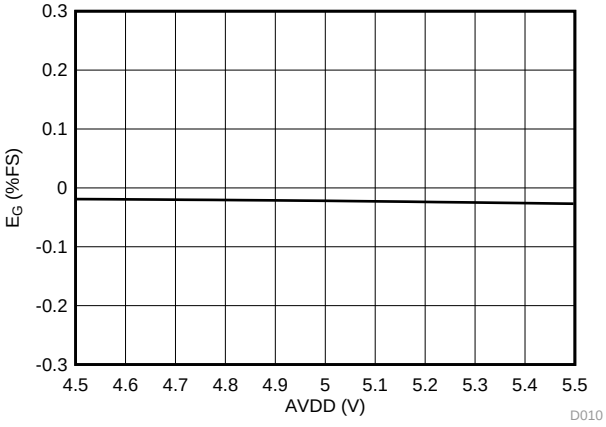


Figure 15. Gain Error vs High-Side Supply Voltage

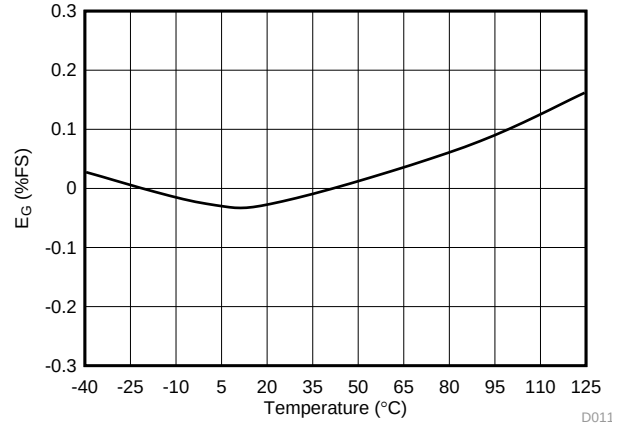


Figure 16. Gain Error vs Temperature

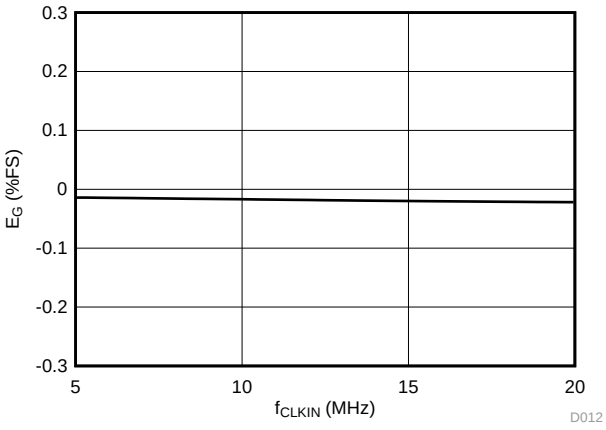


Figure 17. Gain Error vs Clock Frequency

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 5.0 V, DVDD = 3.3 V, AINP = –250 mV to 250 mV, AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

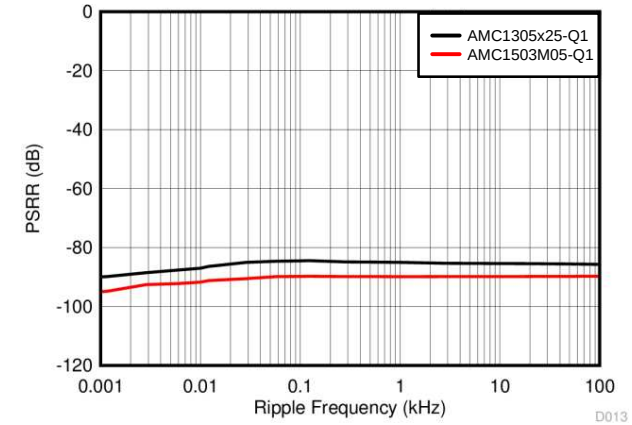

Figure 18. Power-Supply Rejection Ratio vs Ripple Frequency

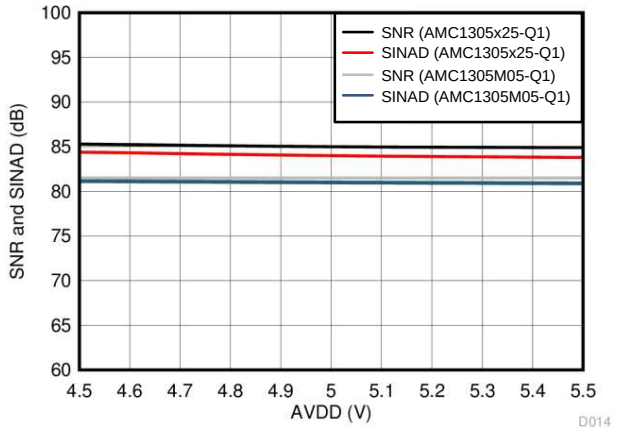

Figure 19. SNR and SINAD vs High-Side Supply Voltage

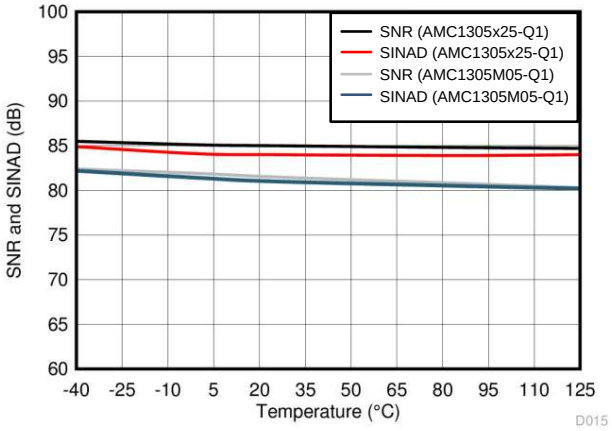

Figure 20. SNR and SINAD vs Temperature

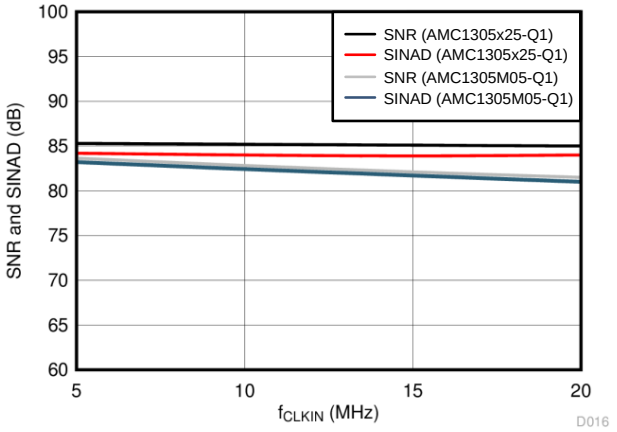

Figure 21. SNR and SINAD vs Clock Frequency

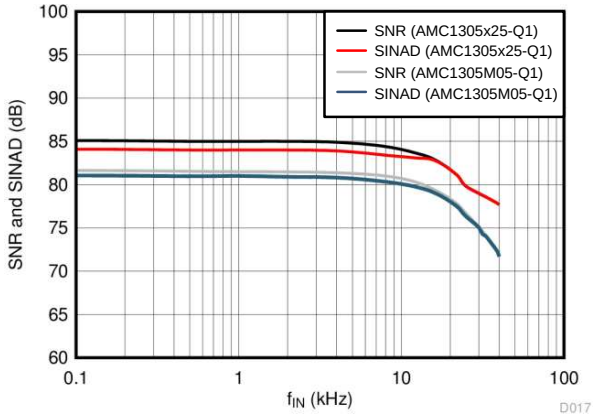

Figure 22. SNR and SINAD vs Input Signal Frequency

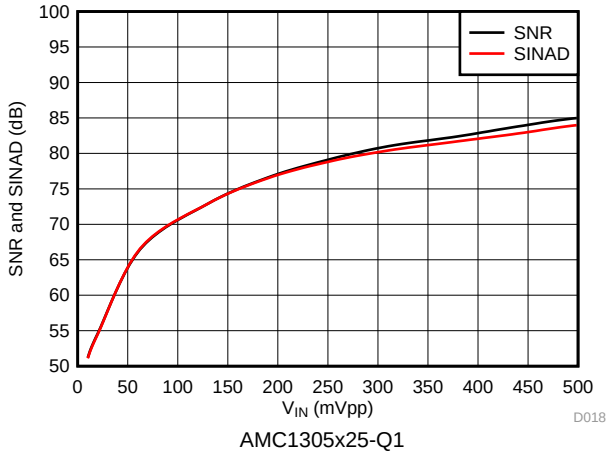

Figure 23. SNR and SINAD vs Input Signal Amplitude

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 5.0 V, DVDD = 3.3 V, AINP = –250 mV to 250 mV, AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

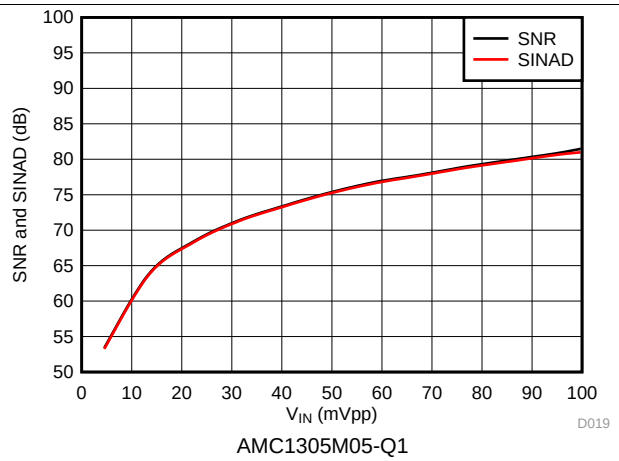

Figure 24. SNR and SINAD vs Input Signal Amplitude

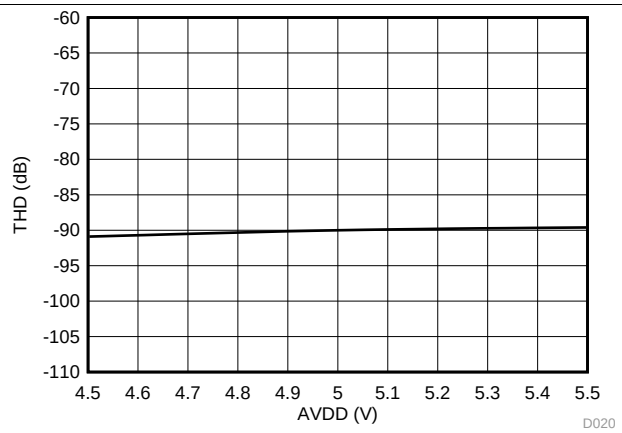

Figure 25. Total Harmonic Distortion vs High-Side Supply Voltage

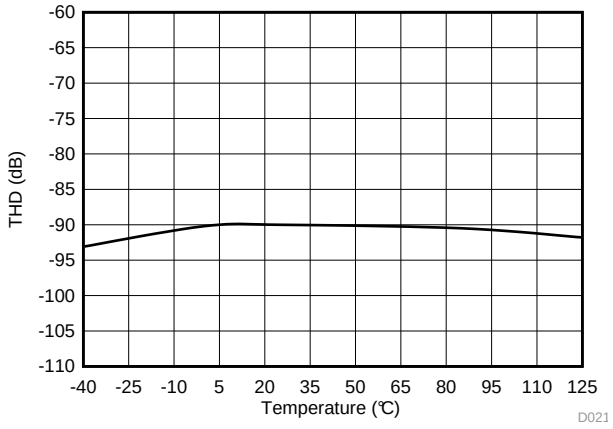

Figure 26. Total Harmonic Distortion vs Temperature

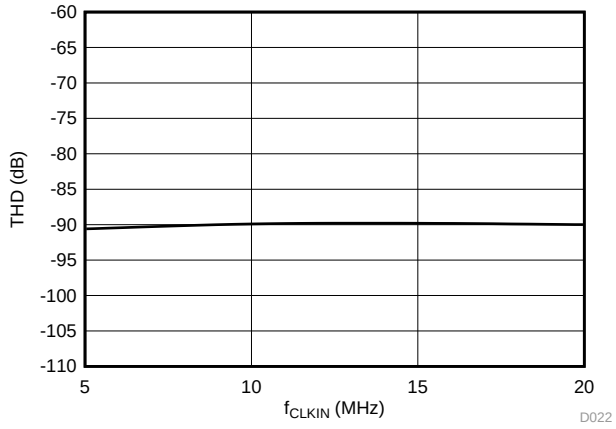

Figure 27. Total Harmonic Distortion vs Clock Frequency

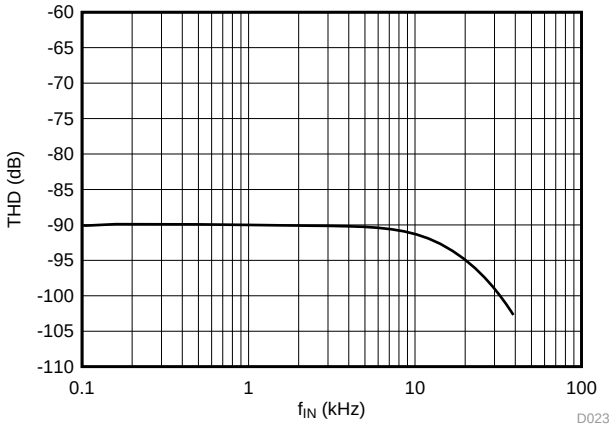

Figure 28. Total Harmonic Distortion vs Input Signal Frequency

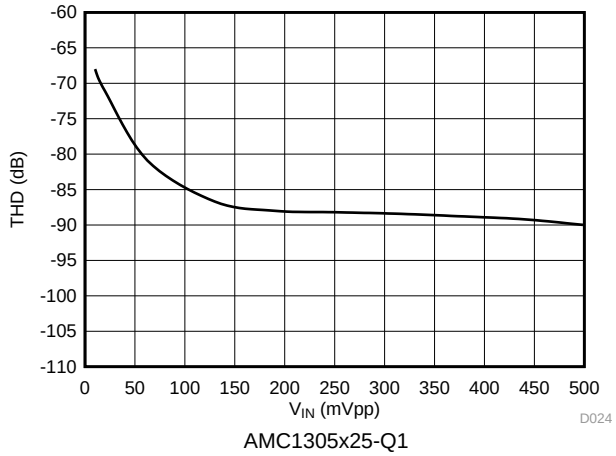

Figure 29. Total Harmonic Distortion vs Input Signal Amplitude

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 5.0 V, DVDD = 3.3 V, AINP = –250 mV to 250 mV, AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

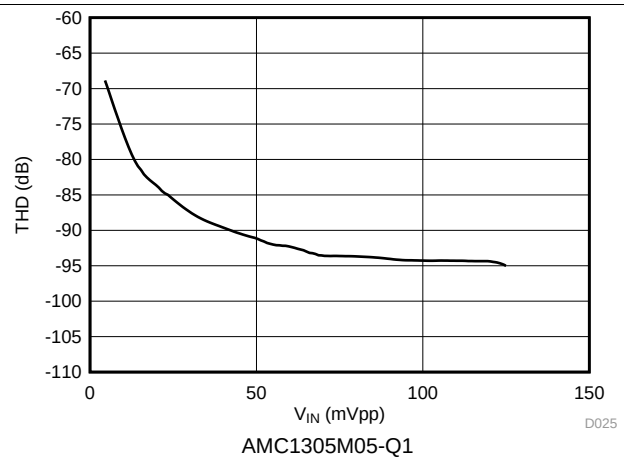


Figure 30. Total Harmonic Distortion vs Input Signal Amplitude

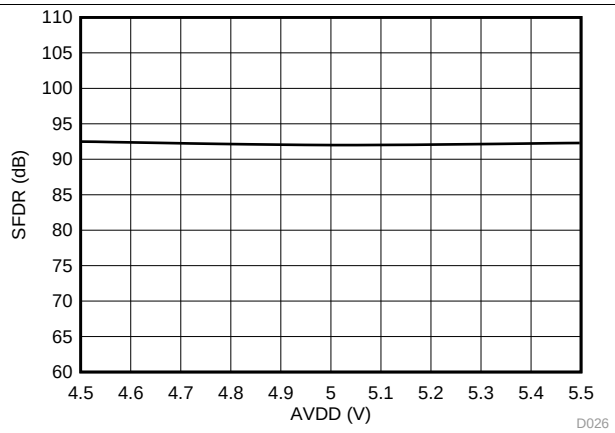


Figure 31. Spurious-Free Dynamic Range vs High-Side Supply Voltage

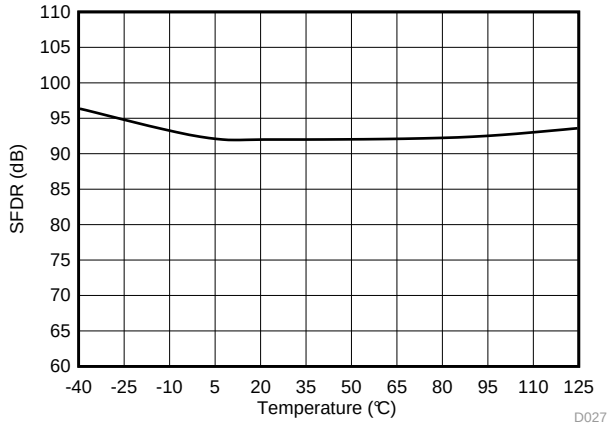


Figure 32. Spurious-Free Dynamic Range vs Temperature

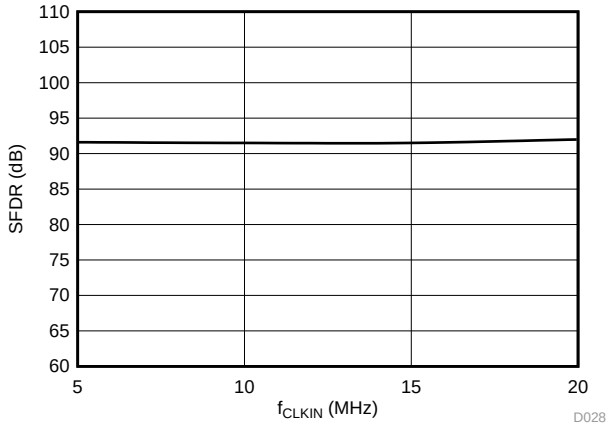


Figure 33. Spurious-Free Dynamic Range vs Clock Frequency

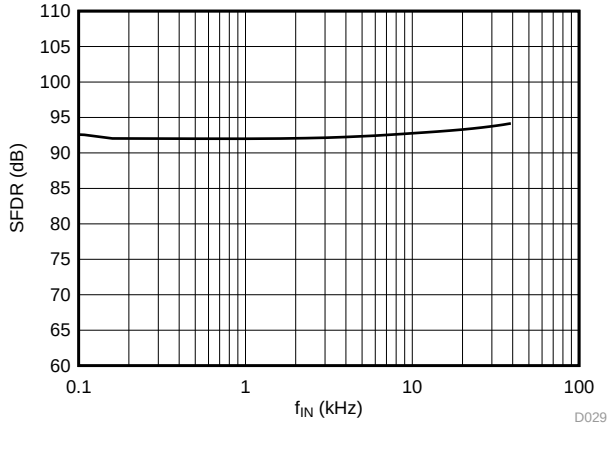


Figure 34. Spurious-Free Dynamic Range vs Input Signal Frequency

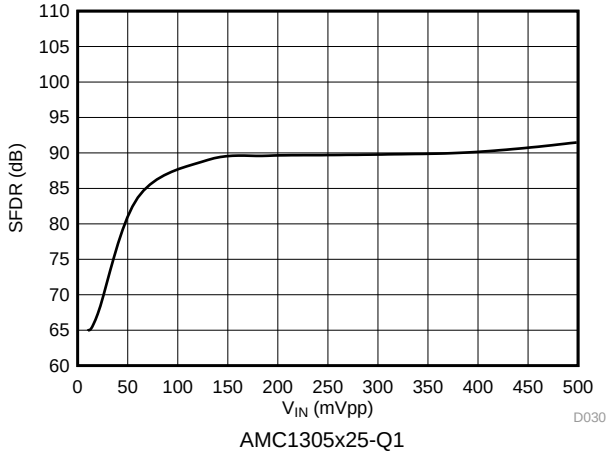
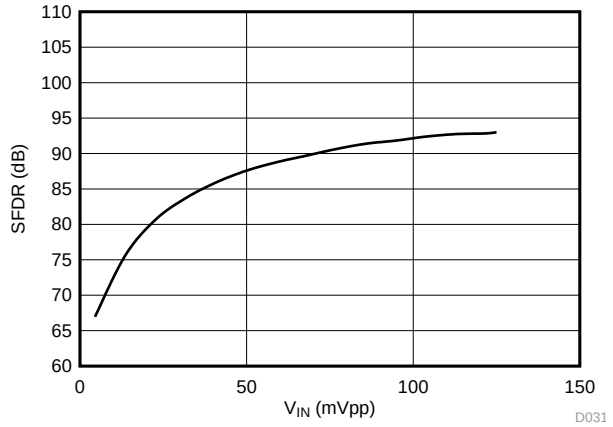


Figure 35. Spurious-Free Dynamic Range vs Input Signal Amplitude

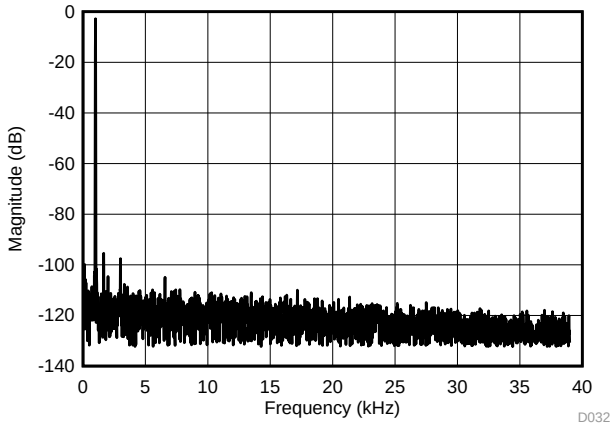
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 5.0 V, DVDD = 3.3 V, AINP = –250 mV to 250 mV, AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.



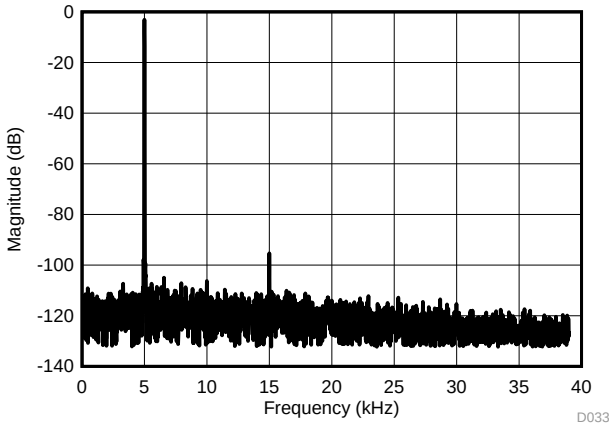
AMC1305M05-Q1

Figure 36. Spurious-Free Dynamic Range vs Input Signal Amplitude



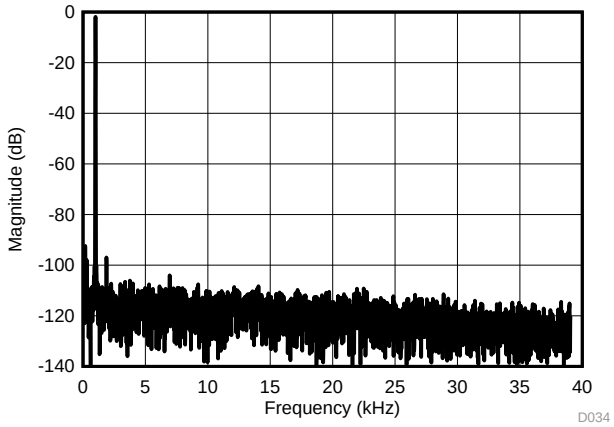
AMC1305x25-Q1, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 37. Frequency Spectrum with 1-kHz Input Signal



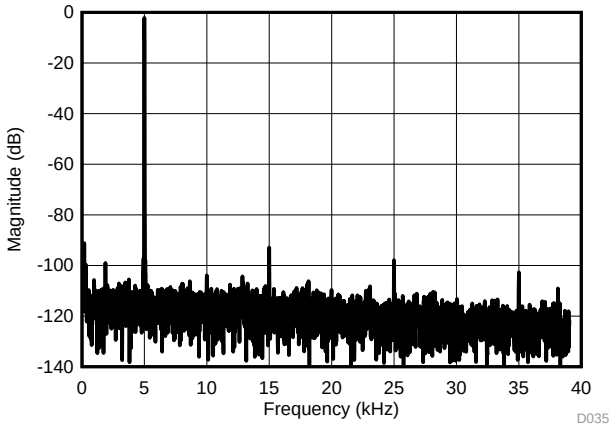
AMC1305x25-Q1, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 38. Frequency Spectrum with 5-kHz Input Signal



AMC1305M05-Q1, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 39. Frequency Spectrum with 1-kHz Input Signal



AMC1305M05-Q1, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 40. Frequency Spectrum with 5-kHz Input Signal

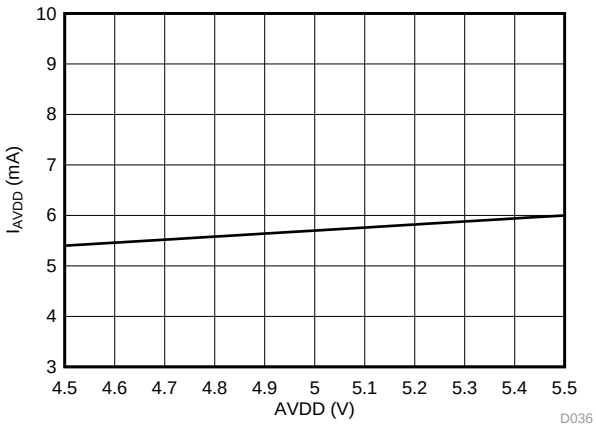


Figure 41. High-Side Supply Current vs High-Side Supply Voltage

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Typical Characteristics (continued)

At T_A = 25°C, AVDD = 5.0 V, DVDD = 3.3 V, AINP = –250 mV to 250 mV, AINN = 0 V, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256, unless otherwise noted.

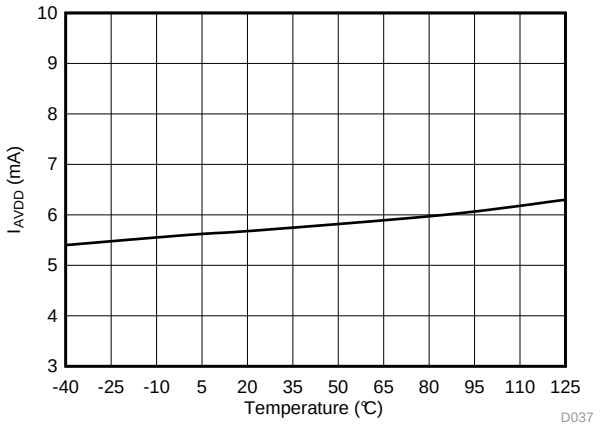


Figure 42. High-Side Supply Current vs Temperature

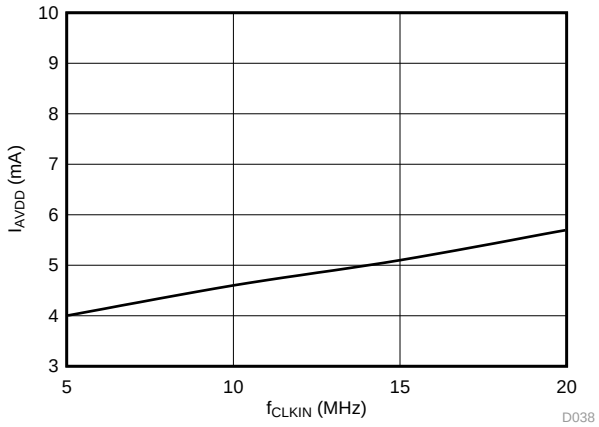


Figure 43. High-Side Supply Current vs Clock Frequency

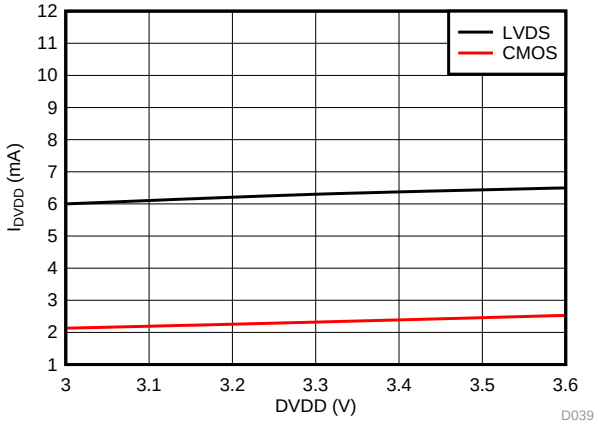


Figure 44. Controller-Side Supply Current vs Controller-Side Supply Voltage (3.3 V, nom)

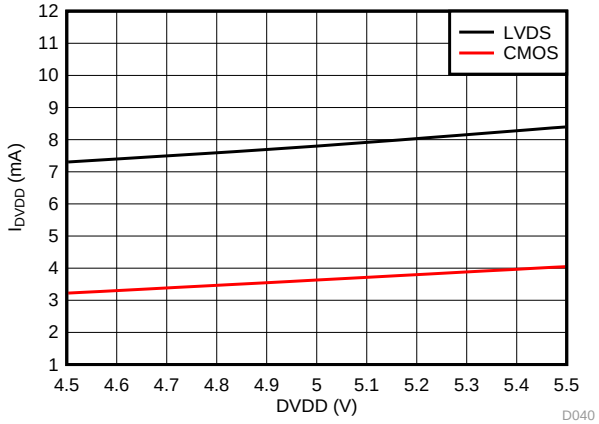


Figure 45. Controller-Side Supply Current vs Controller-Side Supply Voltage (5 V, nom)

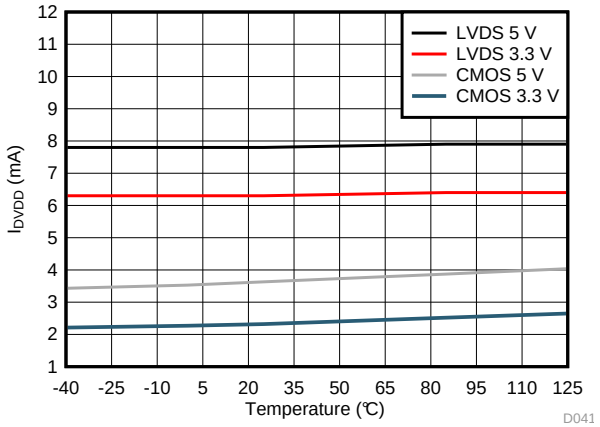


Figure 46. Controller-Side Supply Current vs Temperature

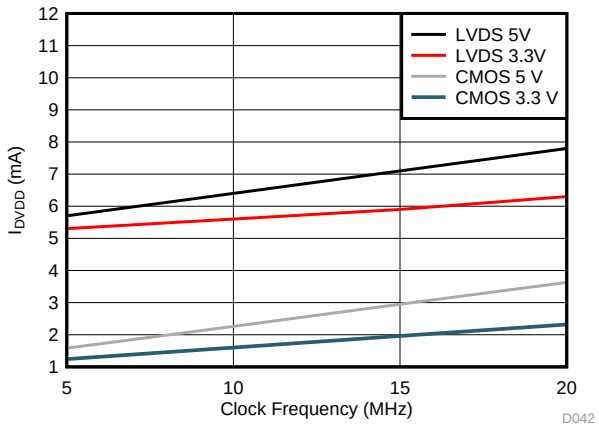


Figure 47. Controller-Side Supply Current vs Clock Frequency

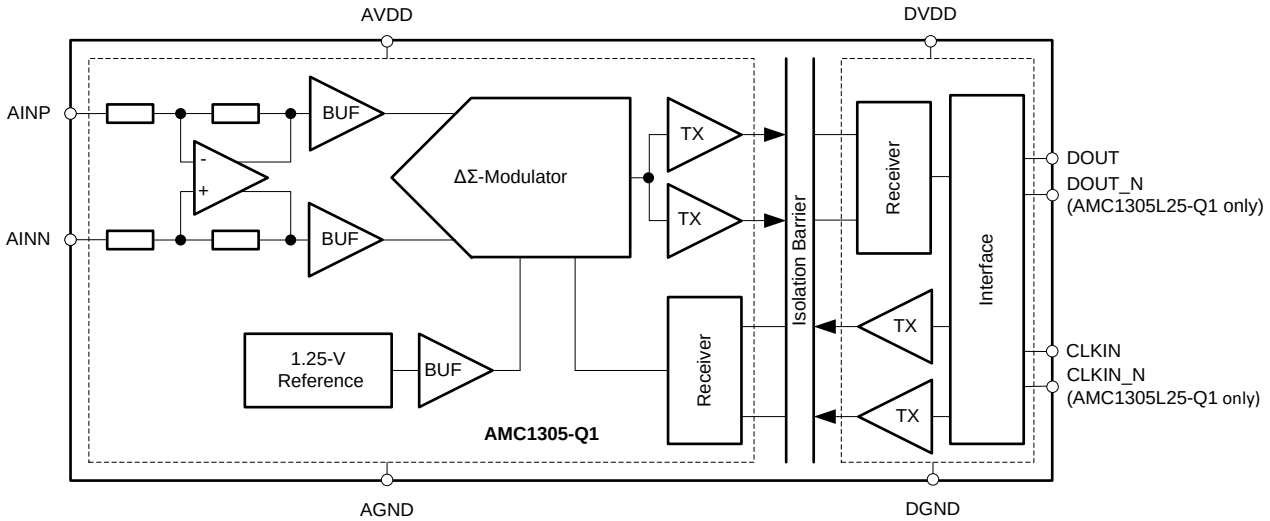
8 Detailed Description

8.1 Overview

The differential analog input (AINP and AINN) of the AMC1305-Q1 is a fully-differential amplifier feeding the switched-capacitor input of a second-order delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The isolated data output (DOUT) of the converter provides a stream of digital ones and zeros synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 5 MHz to 20.1 MHz. The time average of this serial bit-stream output is proportional to the analog input voltage.

The *Functional Block Diagram* section shows a detailed block diagram of the AMC1305-Q1. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the application report *ISO72x Digital Isolator Magnetic-Field Immunity* (SLLA181A), available for download at www.ti.com. The external clock input simplifies the synchronization of multiple current-sense channels on the system level. The extended frequency range of up to 20.1 MHz supports higher performance levels compared to other solutions available on the market.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Analog Input

The AMC1305-Q1 incorporates front-end circuitry that contains a differential amplifier and sampling stage, followed by a ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 for devices with a specified input voltage range of ±250 mV (for the AMC1305x25-Q1), or to a factor of 20 for devices with a ±50-mV input voltage range (for the AMC1305M05-Q1), resulting in a differential input impedance of 5 kΩ (for the AMC1305M05-Q1) or 25 kΩ (for the AMC1305x25-Q1).

Consider the input impedance of the AMC1305-Q1 in designs with high-impedance signal sources that can cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance. Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier causes an offset that depends on the actual amplitude of the input signal. See the *Isolated Voltage Sensing* section for more details on reducing these effects.

There are two restrictions on the analog input signals (AINP and AINN). First, if the input voltage exceeds the range of AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) protection diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±250 mV (for the AMC1305x25-Q1) or ±50 mV (for the AMC1305M05-Q1), and within the specified input common-mode range.

8.3.2 Modulator

The modulator implemented in the AMC1305-Q1 is a second-order, switched-capacitor, feed-forward ΔΣ modulator, such as the one conceptualized in Figure 48. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage V_5, causing the integrators to progress in the opposite direction while forcing the value of the integrator output to track the average value of the input.

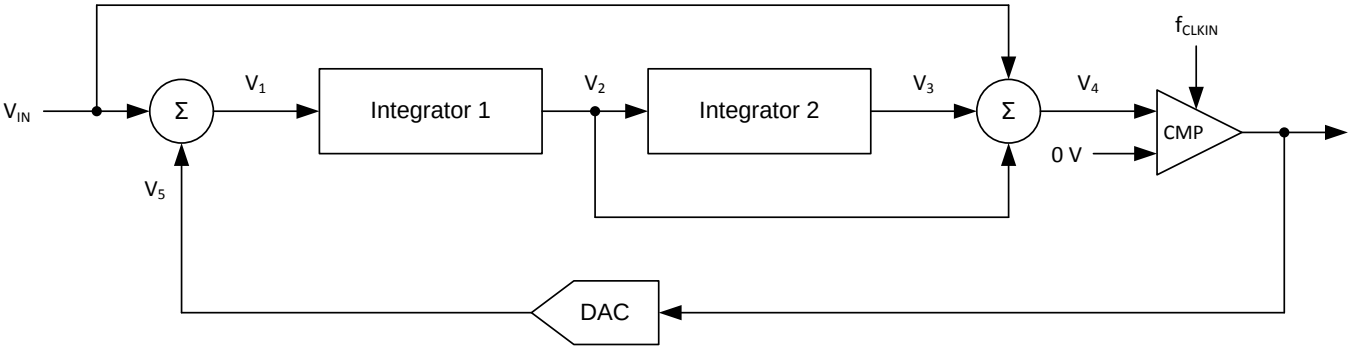

Figure 48. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies; see Figure 49. Therefore, use a low-pass digital filter at the output of the device to increase overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller family TMS320F2837x offers a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1305-Q1 family. Alternatively, a field-programmable gate array (FPGA) can be used to implement the digital filter.

Feature Description (continued)

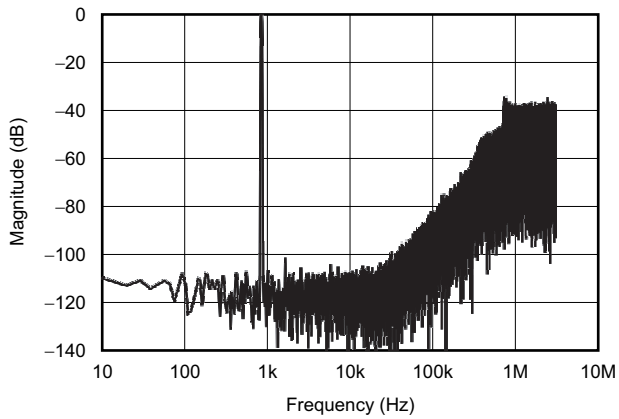

Figure 49. Quantization Noise Shaping

8.3.3 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 250 mV (for the AMC1305x25-Q1) or 50 mV (for the AMC1305M05-Q1) produces a stream of ones and zeros that are high 90% of the time. A differential input of –250 mV (–50 mV for the AMC1305M05-Q1) produces a stream of ones and zeros that are high 10% of the time. These input voltages are also the specified linear ranges of the different AMC1305-Q1 versions with performance as specified in this document. If the input voltage value exceeds these ranges, the output of the modulator shows non-linear behavior while the quantization noise increases. The output of the modulator would clip with a stream of only zeros with an input less than or equal to –312.5 mV (–62.5 mV for the AMC1305M05-Q1) or with a stream of only ones with an input greater than or equal to 312.5 mV (62.5 mV for the AMC1305M05-Q1). In this case, however, the AMC1305-Q1 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Fail-Safe Output* section for more details). The input voltage versus the output modulator signal is shown in Figure 50.

The density of ones in the output bit-stream for any input voltage value (with the exception of a full-scale input signal as described in *Output Behavior in Case of Full-Scale Input*) can be calculated using Equation 1:

$$\frac{V_{IN} + V_{Clipping}}{2 * V_{Clipping}} \tag{1}$$

The AMC1305-Q1 system clock is typically 20 MHz and is provided externally at the CLKIN pin. Data are synchronously provided at 20 MHz at the DOUT pin. Data change at the CLKIN falling edge. For more details, see the *Switching Characteristics* table.

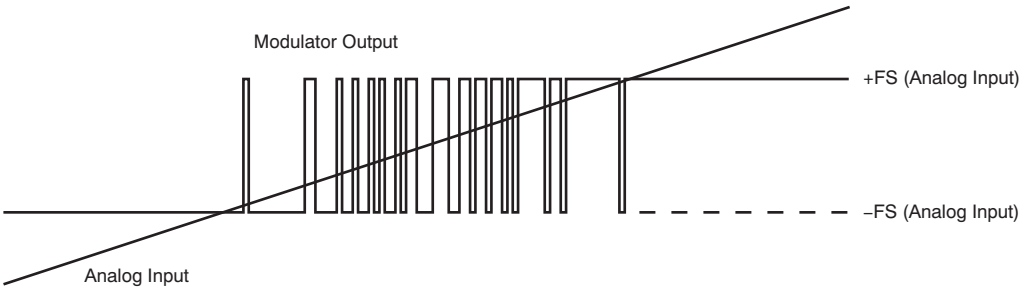

Figure 50. Analog Input versus AMC1305-Q1 Modulator Output

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8.4 Device Functional Modes

8.4.1 Fail-Safe Output

In the case of a missing high-side supply voltage (AVDD), the output of a ΔΣ modulator is not defined and could cause a system malfunction. In systems with high safety requirements, this behavior is not acceptable. Therefore, the AMC1305-Q1 implements a fail-safe output function that ensures the device maintains its output level in case of a missing AVDD, as shown in Figure 51.

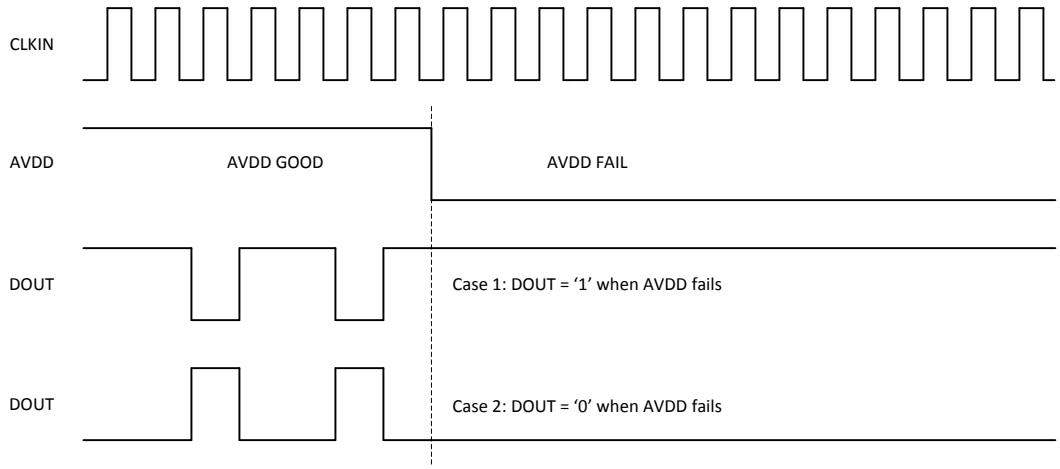

Figure 51. Fail-Safe Output of the AMC1305-Q1

8.4.2 Output Behavior in Case of Full-Scale Input

If a full-scale input signal is applied to the AMC1305-Q1 (that is, $V_{IN} \geq V_{Clipping}$), the device generates a single one or zero every 128 bits at DOUT, depending on the actual polarity of the signal being sensed, as shown in Figure 52.

In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.

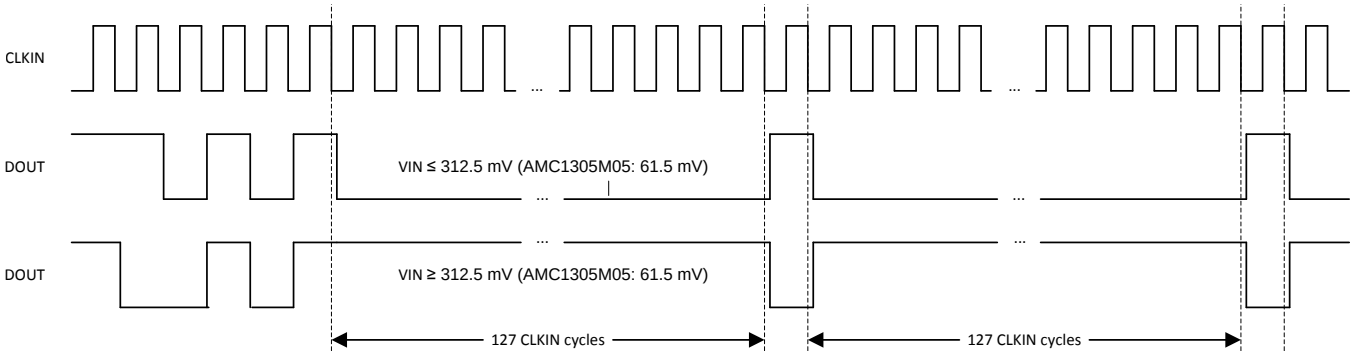

Figure 52. Overrange Output of the AMC1305-Q1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Digital Filter Usage

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 2:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a sinc^3 filter with an over-sampling ratio (OSR) of 256 and an output word width of 16 bits.

$$SNR = 1.76dB + 6.02dB * ENOB \tag{3}$$

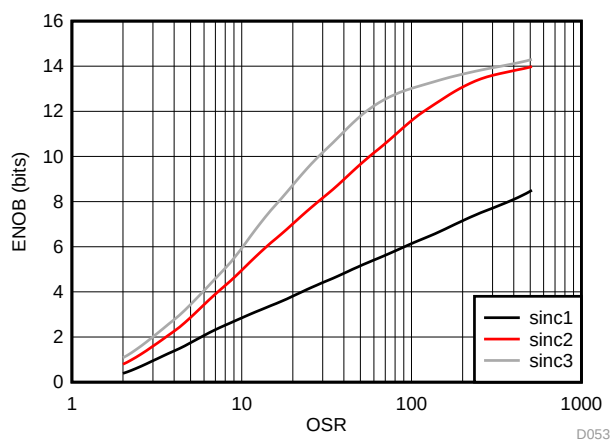

Figure 53. Measured Effective Number of Bits versus Oversampling Ratio

An example code for an implementation of a sinc^3 filter in an FPGA, see the application note *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications* (SBAA094), available for download at www.ti.com.

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9.2 Typical Applications

9.2.1 Traction Inverter Application

Because to their high ac and dc performance, isolated ΔΣ modulators are being widely used in new generation traction inverter designs. Traction inverters are critical parts of electrical and hybrid electrical vehicles. The input structure of the AMC1305-Q1 is optimized for use with low-impedance shunt resistors and is therefore tailored for isolated current sensing using shunts.

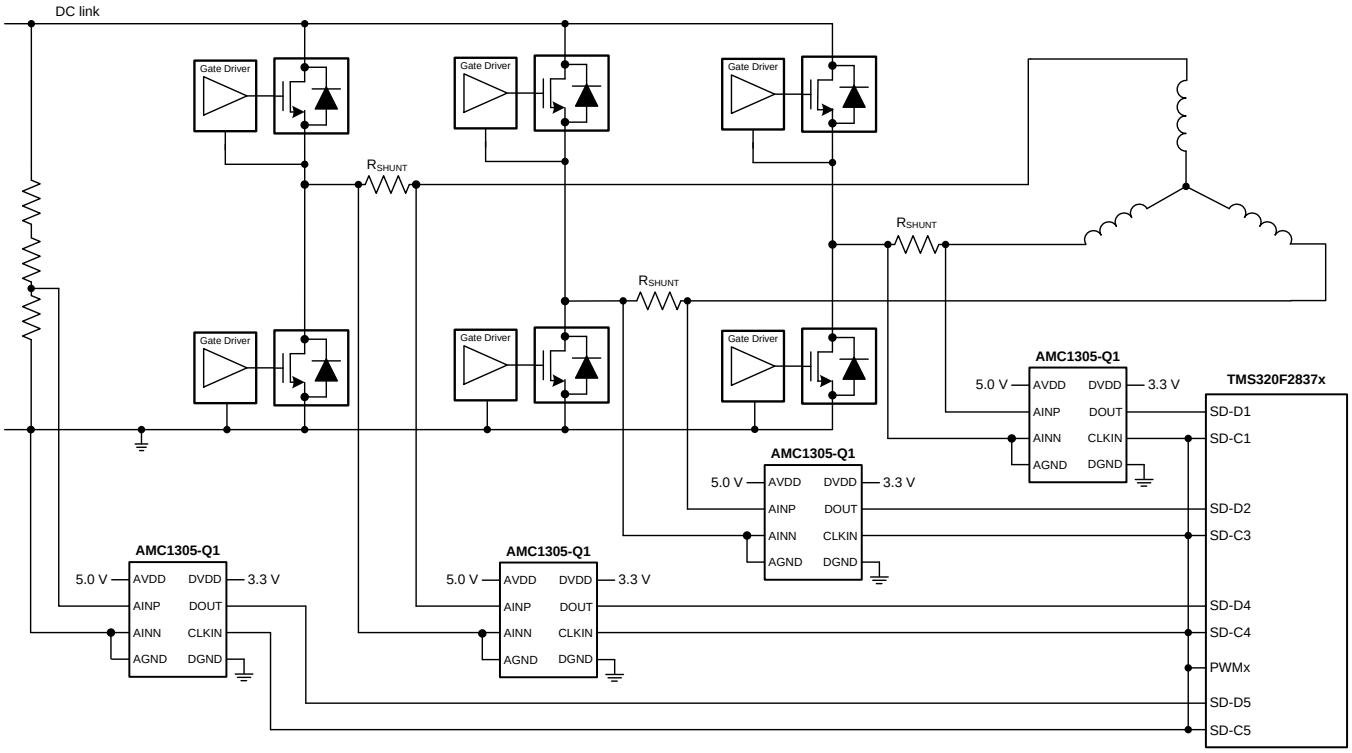

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Figure 54. The AMC1305-Q1 in a Traction Inverter Application

9.2.1.1 Design Requirements

A typical operation of the device in a traction inverter application is shown in Figure 54. When the inverter stage is part of a motor drive system, measurement of the motor phase current is done via the shunt resistors (R_{SHUNT}). Depending on the system design, either all three or only two phase currents are sensed.

In this example, an additional fourth AMC1305-Q1 is used to support isolated voltage sensing of the dc link. This high voltage is reduced using a high-impedance resistive divider before being sensed by the device across a smaller resistor. The value of this resistor can degrade the performance of the measurement, as described in the *Isolated Voltage Sensing* section.

9.2.1.2 Detailed Design Procedure

The usually recommended RC filter in front of a ΔΣ modulator to improve signal-to-noise performance of the signal path, is not required for the AMC1305-Q1. By design, the input bandwidth of the analog front-end of the device is limited to 1 MHz.

For modulator output bit-stream filtering, a device from TI's TMS320F2837x family of dual-core MCUs is recommended. This family supports up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.

Typical Applications (continued)

9.2.1.3 Application Curve

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on its order; that is, a $sinc^3$ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK}$ / OSR). Therefore, for overcurrent protection, filter types other than $sinc^3$ can be a better choice; an alternative is the $sinc^2$ filter. Figure 55 compares the settling times of different filter orders.

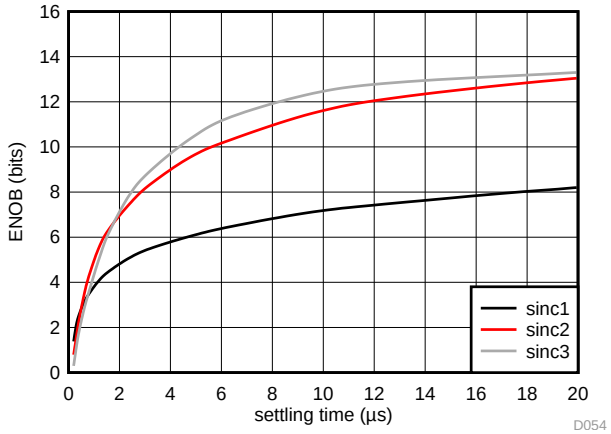

Figure 55. Measured Effective Number of Bits versus Settling Time

The delay time of the sinc filter with a continuous signal is half of its settling time.

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Typical Applications (continued)

9.2.2 Isolated Voltage Sensing

The AMC1305-Q1 is optimized for usage in current-sensing applications using low-impedance shunts. However, the device can also be used in isolated voltage-sensing applications if the impact of the (usually higher) impedance of the resistor used in this case is considered.

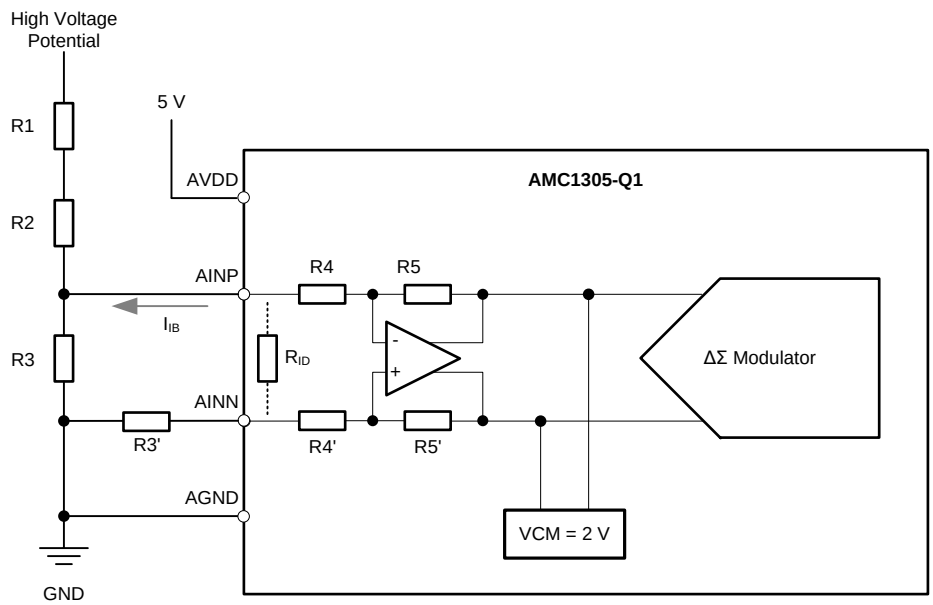

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Figure 56. Using AMC1305-Q1 for Isolated Voltage Sensing

9.2.2.1 Design Requirements

Figure 56 shows a simplified circuit typically used in high-voltage sensing applications. The high impedance resistors (R1 and R2) are used as voltage dividers and dominate the current value definition. The resistance of the sensing resistor R3 is chosen to meet the input voltage range of the AMC1305-Q1. This resistor and the differential input impedance of the device (the AMC1305x25-Q1 is 25 kΩ, the AMC1305M05-Q1 is 5 kΩ) also create a voltage divider that results in an additional gain error. With the assumption of R1, R2, and R_{IN} having a considerably higher value than R3, the resulting total gain error can be estimated using Equation 4, with E_G being the gain error of the AMC1305-Q1.

$$\left|E_{Gtot}\right| = \left|E_G\right| + \frac{R_3}{R_{IN}} \tag{4}$$

This gain error can be easily minimized during the initial system level gain calibration procedure.

9.2.2.2 Detailed Design Procedure

As indicated in Figure 56, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 2 V. This voltage results in a bias current I_{IB} through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value range of this current is specified in the Electrical Characteristics table. This bias current generates additional offset error that depends on the value of the resistor R3. Because the value of this bias current depends on the actual common-mode amplitude of the input signal (as shown in Figure 57), the initial system offset calibration does not minimize its effect. Therefore, in systems with high accuracy requirements TI recommends using a series resistor at the negative input (AINN) of the AMC1305-Q1 with a value equal to the shunt resistor R3 (that is R3' = R3 in Figure 56) to eliminate the effect of the bias current.

Typical Applications (continued)

This additional series resistor (R3') influences the gain error of the circuit. The effect can be calculated using Equation 5 with R5 = R5' = 50 kΩ and R4 = R4' = 2.5 kΩ (for the AMC1305M05-Q1) or 12.5 kΩ (for the AMC1305x25-Q1).

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'}\right) * 100\% \tag{5}$$

9.2.2.3 Application Curve

Figure 57 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1305-Q1.

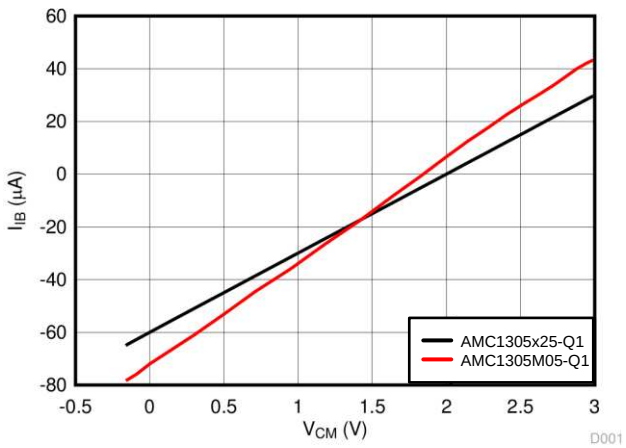

Figure 57. Input Current vs Input Common-Mode Voltage

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10 Power-Supply Recommendations

In a typical traction inverter application, the high-side power supply (AVDD) for the device is derived from the floating power supply of the upper gate driver. For lowest cost, a Zener diode can be used to limit the voltage to 5 V ±10%. Alternatively a low-cost low-drop regulator (LDO), for example the LP2951-xx-Q1, can be used to minimize noise on the power supply. A low-ESR decoupling capacitor of 0.1 µF is recommended for filtering this power-supply path. Place this capacitor (C_2 in Figure 58) as close as possible to the AVDD pin of the AMC1305-Q1 for best performance. If better filtering is required, an additional 10-µF capacitor can be used. The floating ground reference (AGND) is derived from the end of the shunt resistor, which is connected to the negative input (AINN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, while AGND is connected to one of the outer leads of the shunt.

For decoupling of the digital power supply on controller side, TI recommends using a 0.1-µF capacitor assembled as close to the DVDD pin of the AMC1305-Q1 as possible, followed by an additional capacitor in the range of 1 µF to 10 µF.

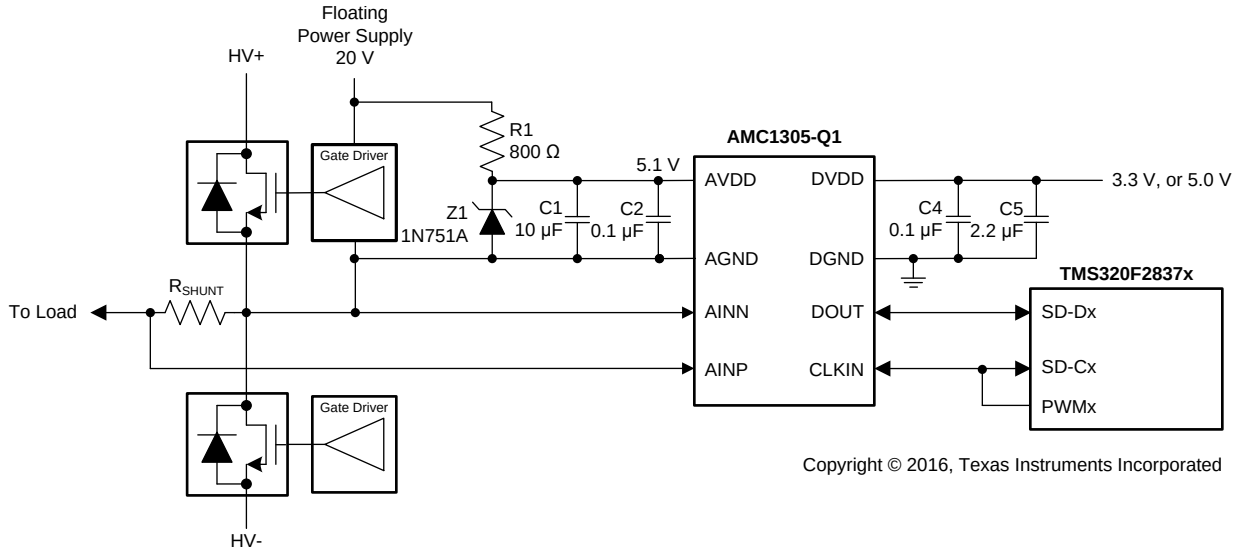

Figure 58. Zener-Diode-Based High-Side Power Supply

11 Layout

11.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors (as close as possible to the AMC1305-Q1) and placement of the other components required by the device is shown in Figure 59.

For the AMC1305L25-Q1 version, place the 100-Ω termination resistor as close as possible to the CLKIN, CLKIN_N inputs of the device to achieve highest signal integrity. If not integrated, an additional termination resistor is required as close as possible to the LVDS data inputs of the MCU or filter device; see Figure 60.

11.2 Layout Examples

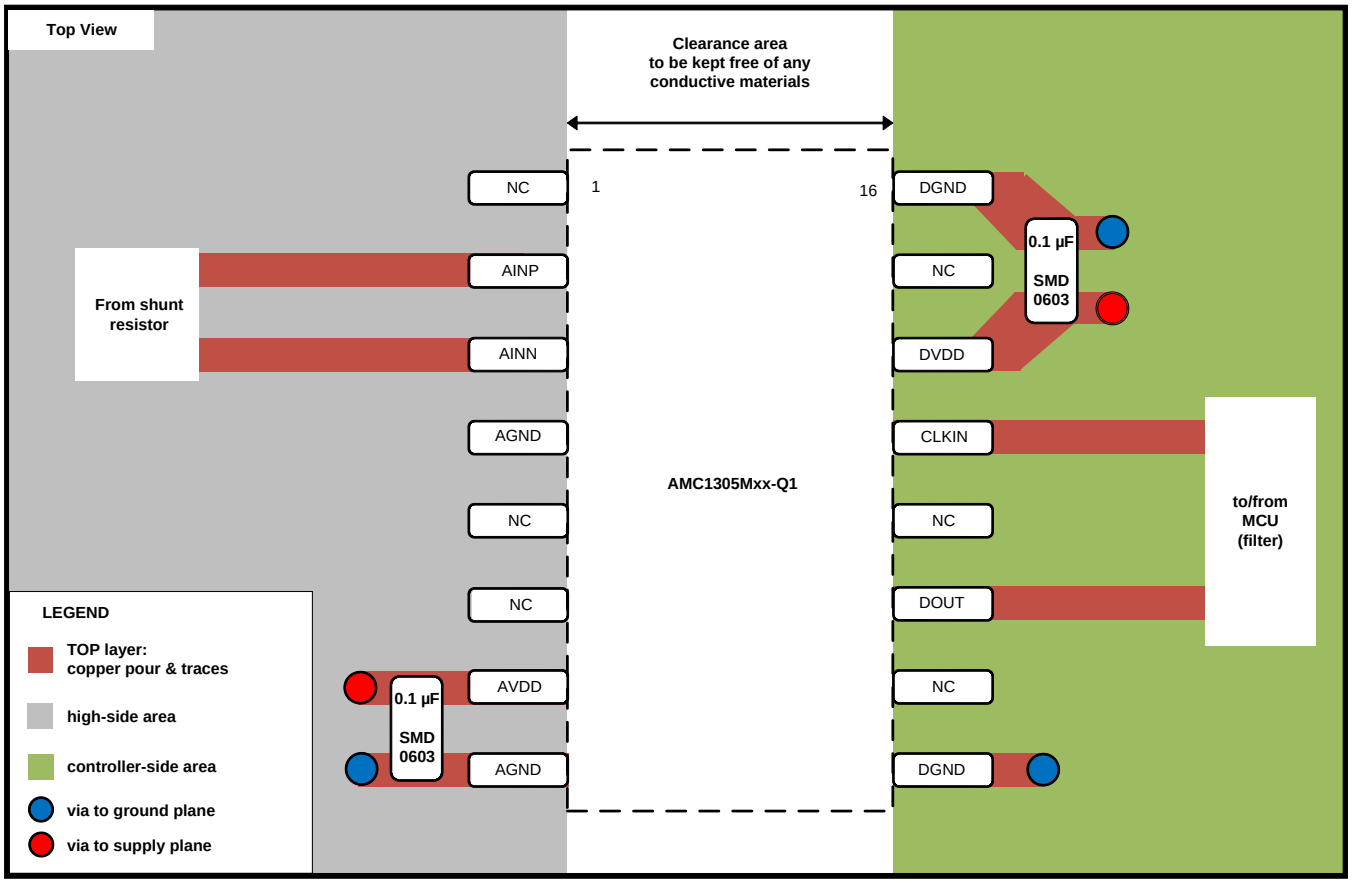

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Figure 59. Recommended Layout of the AMC1305Mx-Q1

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Layout Examples (continued)

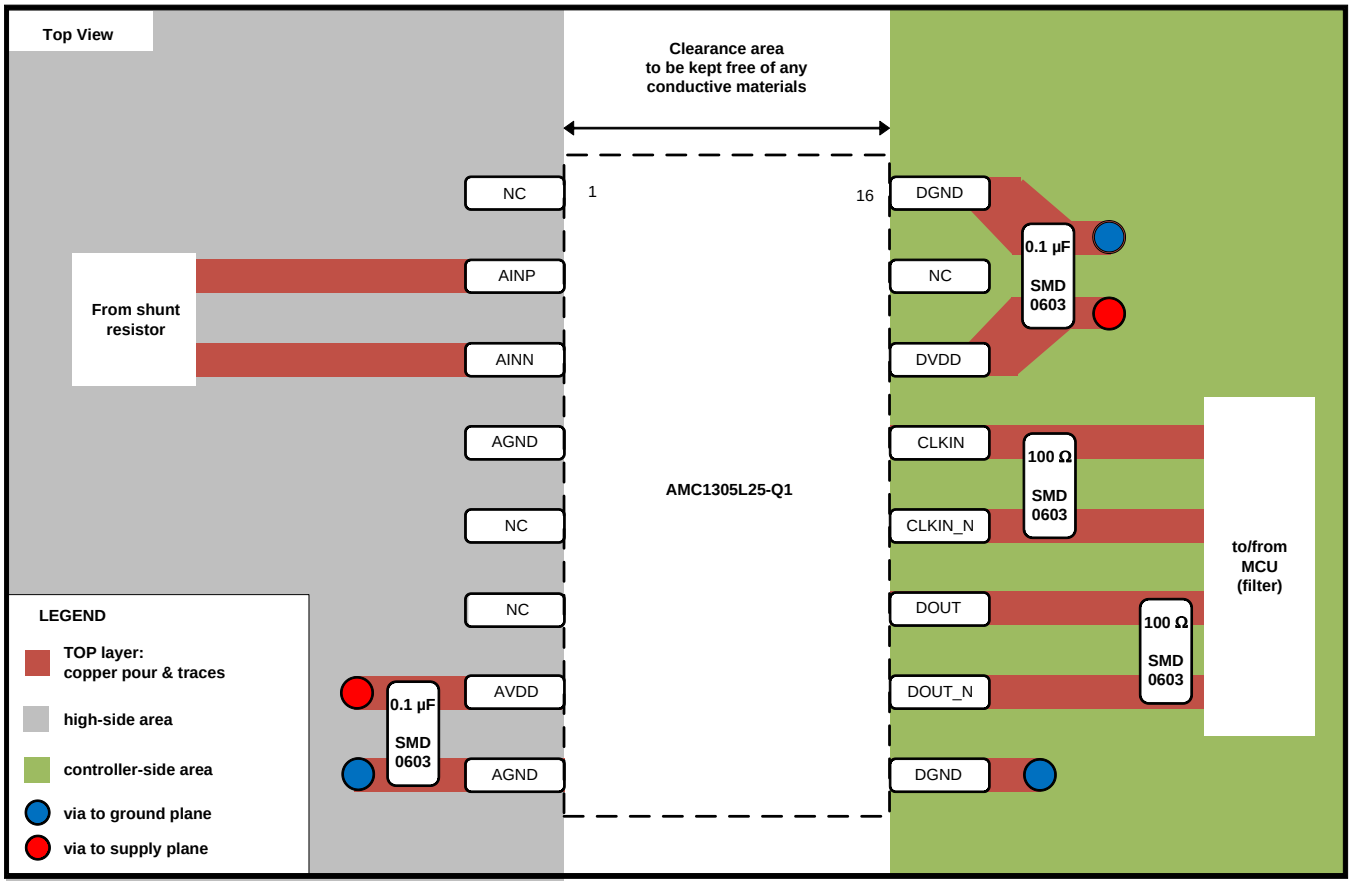

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Figure 60. Recommended Layout of the AMC1305L25-Q1

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary*
- *ISO72x Digital Isolator Magnetic-Field Immunity*
- *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications*
- *LP2951-xx-Q1 Adjustable Micropower Voltage Regulators With Shutdown*
- *TMS320F2837xD Dual-Core Delfino™ Microcontrollers*

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
AMC1305L25-Q1	Click here	Click here	Click here	Click here	Click here
AMC1305M05-Q1	Click here	Click here	Click here	Click here	Click here
AMC1305M25-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1305L25QDWQ1	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305L25Q1
AMC1305L25QDWQ1.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305L25Q1
AMC1305L25QDWQ1.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305L25Q1
AMC1305L25QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 125	1305L25Q1
AMC1305L25QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305L25Q1
AMC1305L25QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305L25Q1
AMC1305M05QDWQ1	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M05Q1
AMC1305M05QDWQ1.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M05Q1
AMC1305M05QDWQ1.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M05Q1
AMC1305M05QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M05Q1
AMC1305M05QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M05Q1
AMC1305M05QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M05Q1
AMC1305M25QDWQ1	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M25Q1
AMC1305M25QDWQ1.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M25Q1
AMC1305M25QDWQ1.B	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M25Q1
AMC1305M25QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M25Q1
AMC1305M25QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M25Q1
AMC1305M25QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1305M25Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AMC1305L25-Q1, AMC1305M05-Q1, AMC1305M25-Q1 :

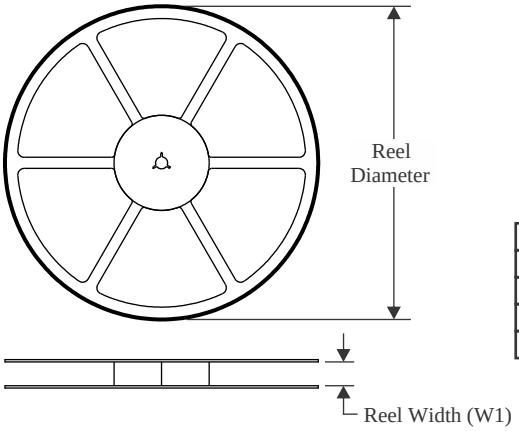
- Catalog : AMC1305L25, AMC1305M05, AMC1305M25

NOTE: Qualified Version Definitions:

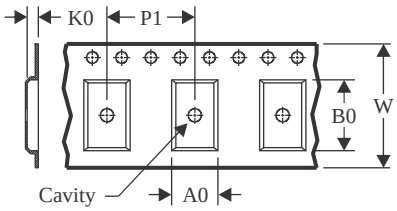
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

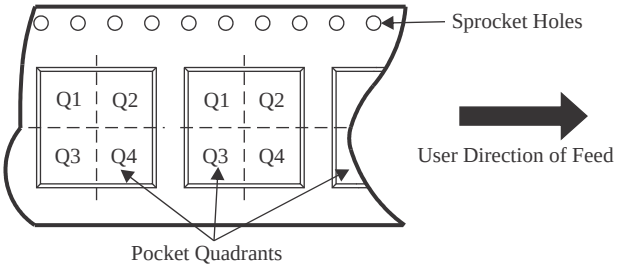


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

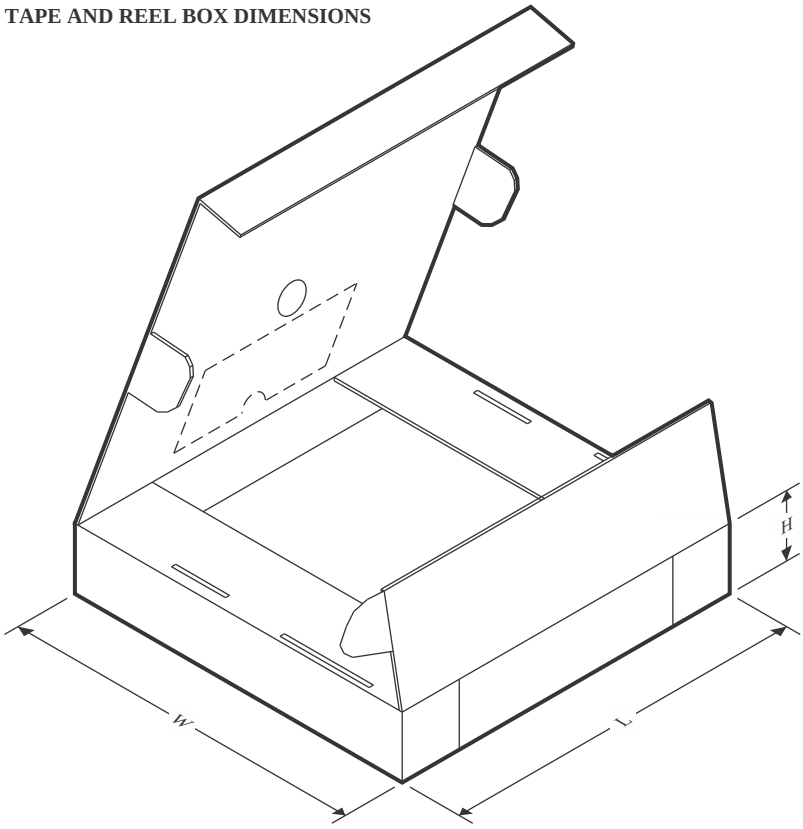
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1305L25QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
AMC1305M05QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
AMC1305M25QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

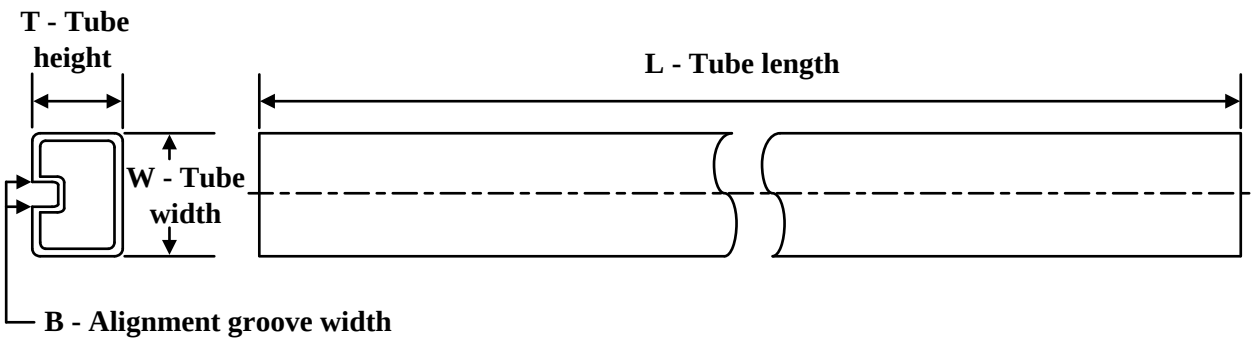
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1305L25QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
AMC1305M05QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
AMC1305M25QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1305L25QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305L25QDWQ1.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305L25QDWQ1.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305M05QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305M05QDWQ1	DW	SOIC	16	40	507	12.83	5080	6.6
AMC1305M05QDWQ1.A	DW	SOIC	16	40	507	12.83	5080	6.6
AMC1305M05QDWQ1.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305M05QDWQ1.B	DW	SOIC	16	40	507	12.83	5080	6.6
AMC1305M05QDWQ1.B	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305M25QDWQ1	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305M25QDWQ1.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
AMC1305M25QDWQ1.B	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

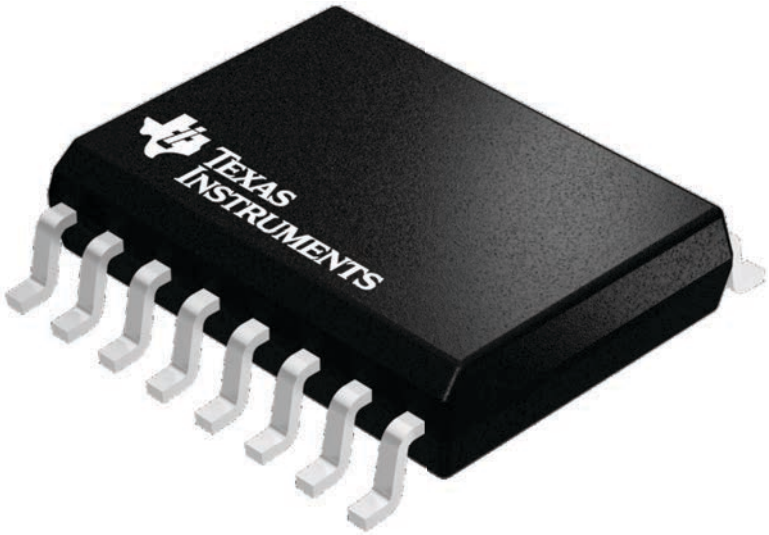
DW 16

SOIC - 2.65 mm max height

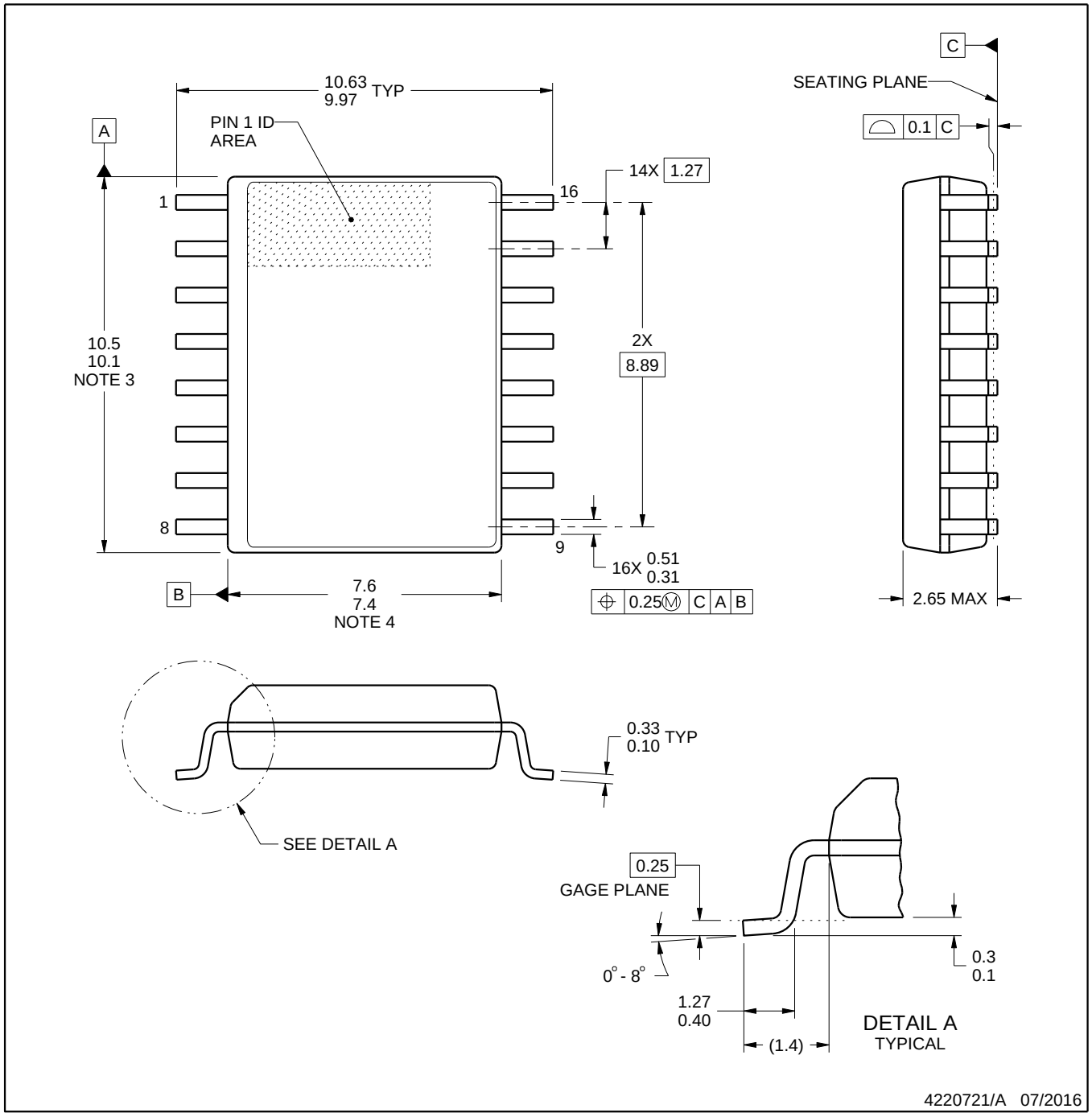
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

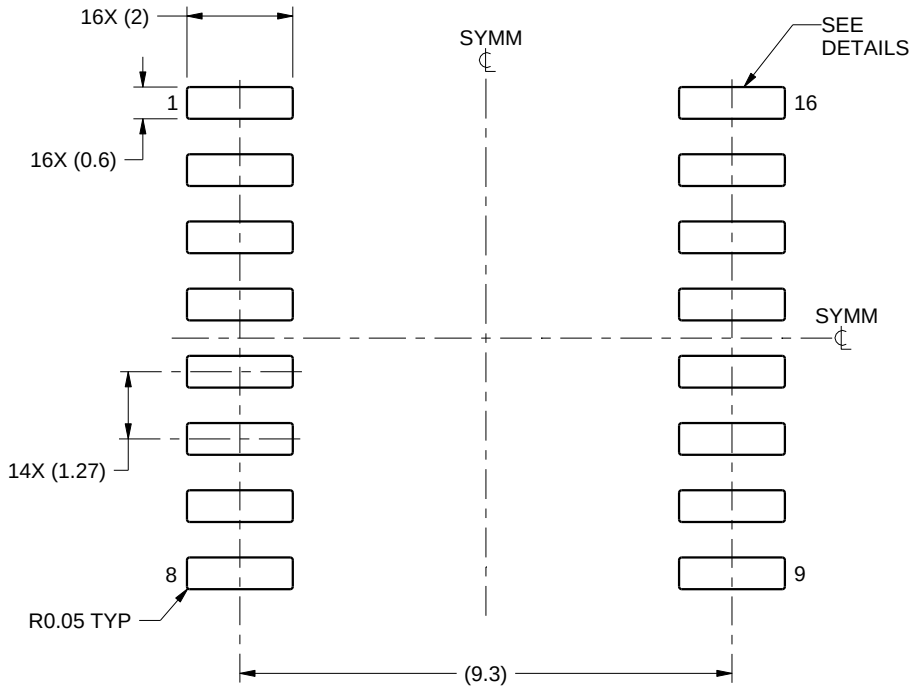


4224780/A

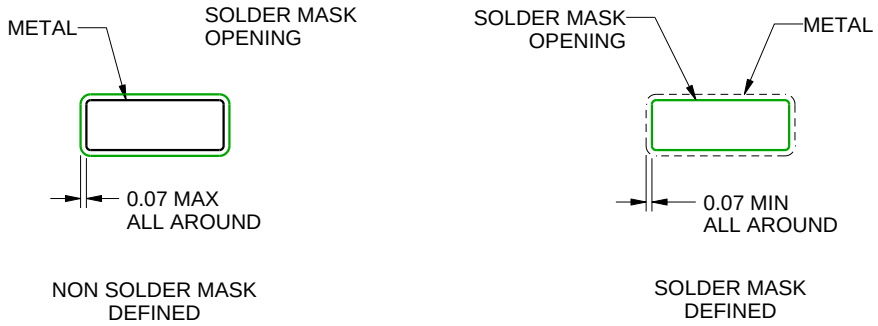


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

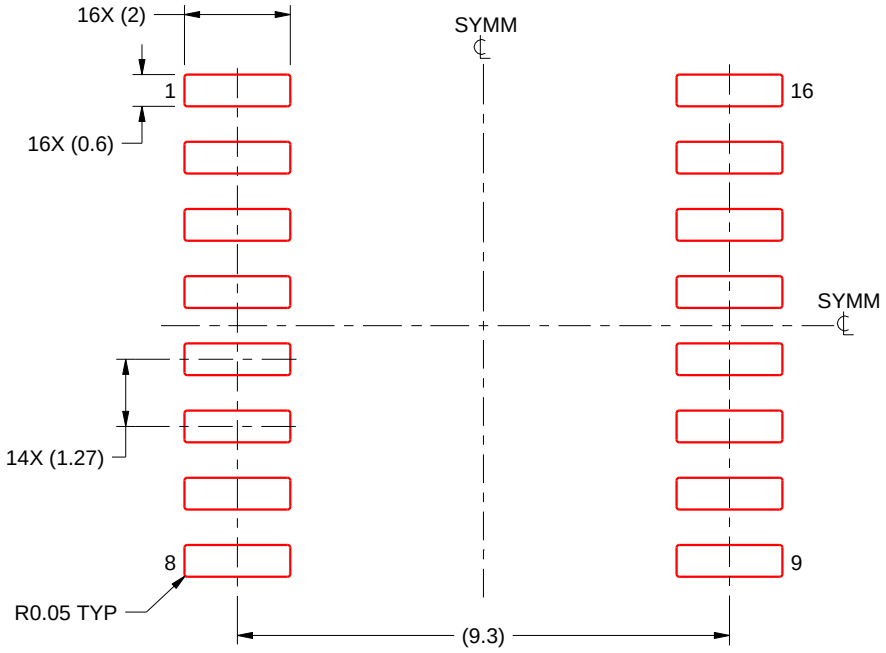


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

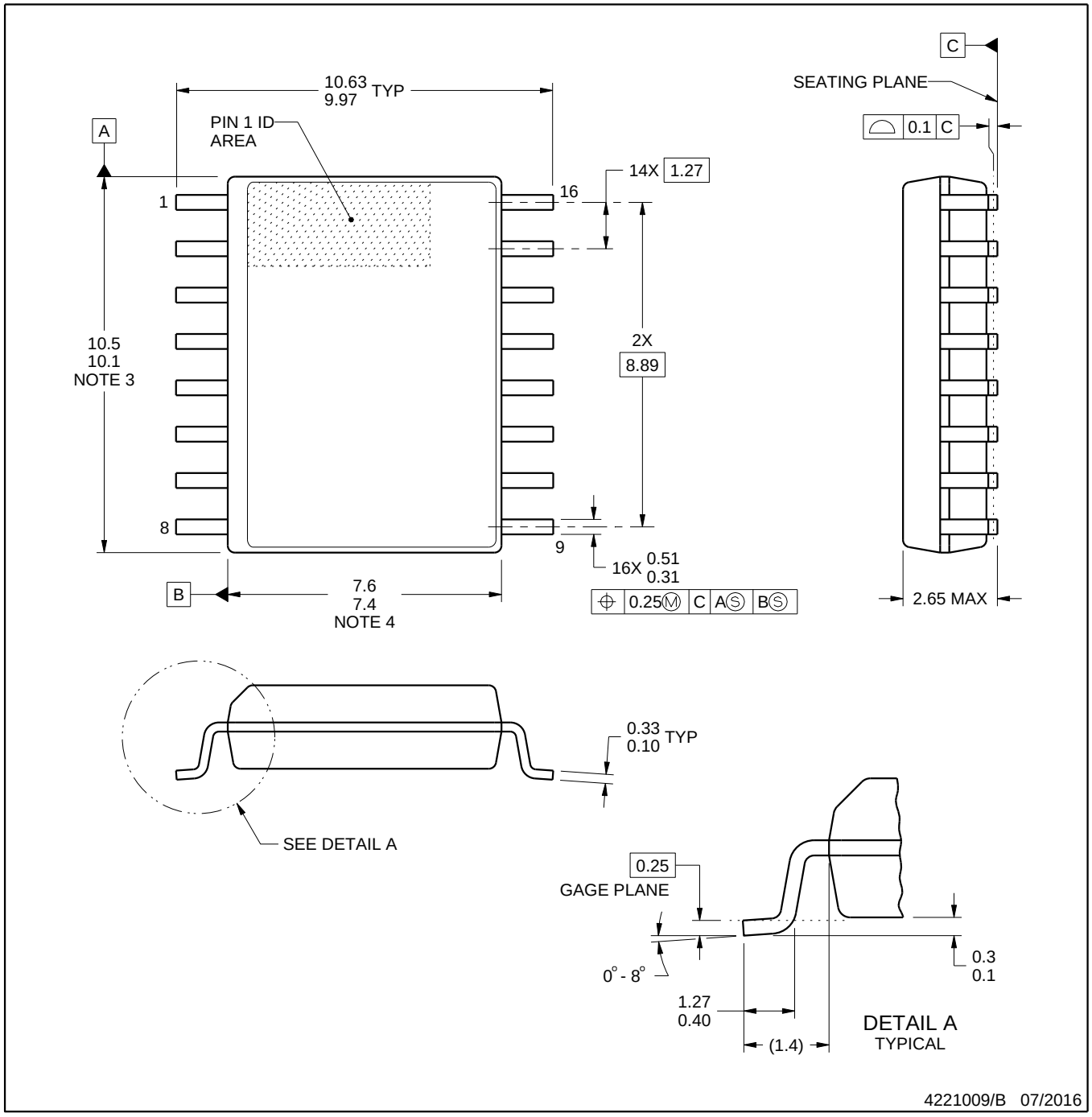


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

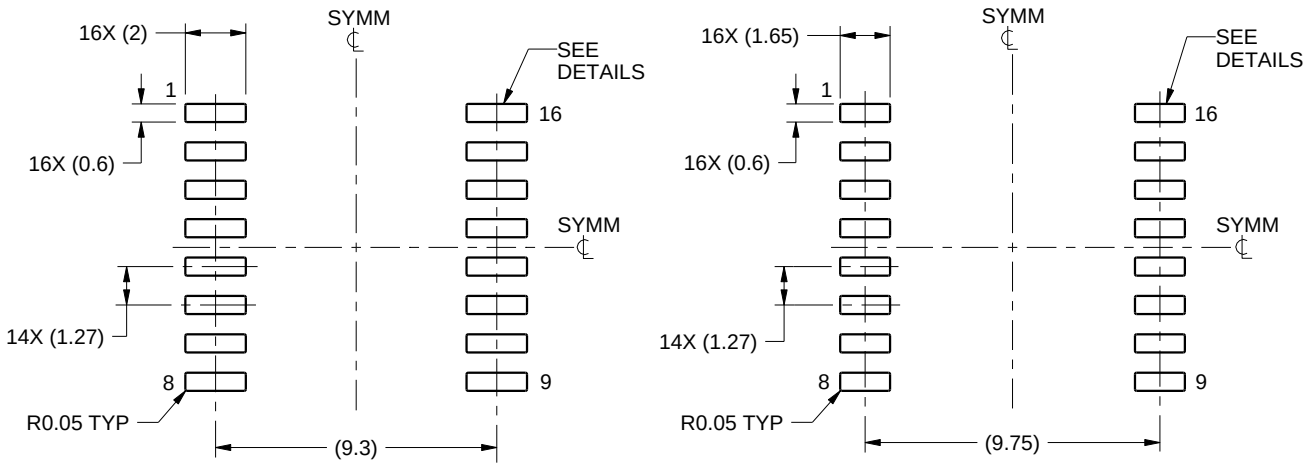
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



NOTES:

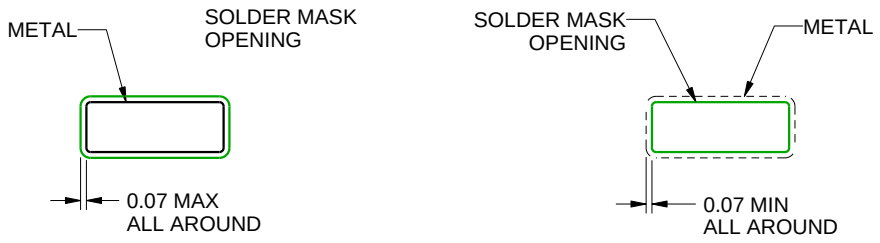
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

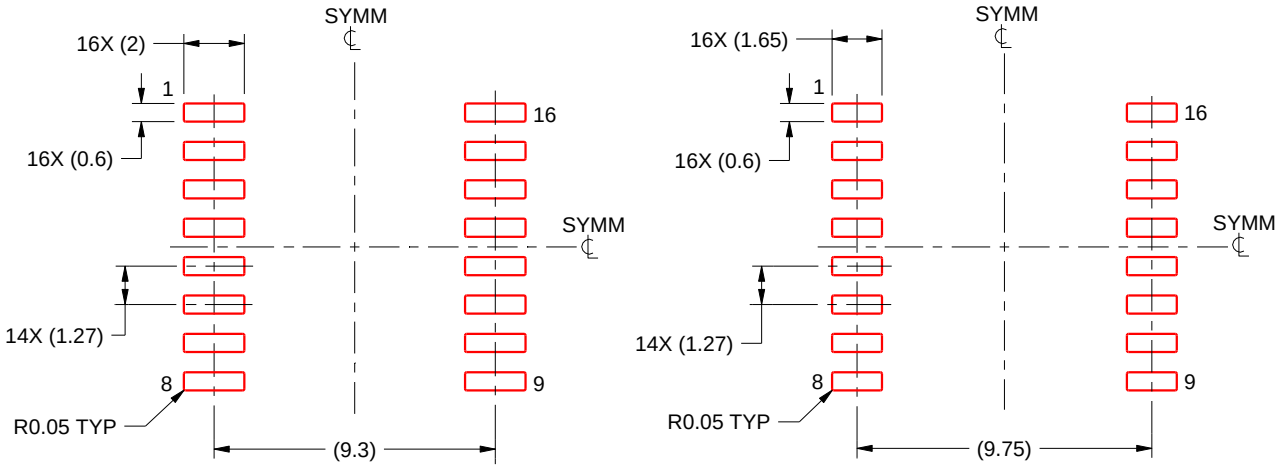
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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