

LT1004-1.2, LT1004-2.5 MICROPOWER INTEGRATED VOLTAGE REFERENCES

SLVS022M – JANUARY 1989 – REVISED MAY 2008

- **Initial Accuracy**
 - ± 4 mV for LT1004-1.2
 - ± 20 mV for LT1004-2.5
- **Micropower Operation**
- **Operates up to 20 mA**
- **Very Low Reference Impedance**
- **Applications:**
 - Portable Meter Reference
 - Portable Test Instruments
 - Battery-Operated Systems
 - Current-Loop Instrumentation

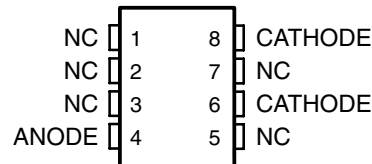
description/ordering information

The LT1004 micropower voltage reference is a two-terminal band-gap reference diode designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimizing the key parameters in the design, processing, and testing of the device results in specifications previously attainable only with selected units.

The LT1004 is a pin-for-pin replacement for the LM285 and LM385 series of references, with improved specifications. It is an excellent device for use in systems in which accuracy previously was attained at the expense of power consumption and trimming.

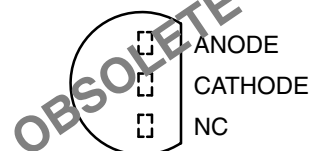
The LT1004C is characterized for operation from 0°C to 70°C. The LT1004I is characterized for operation from –40°C to 85°C.

D OR PW PACKAGE (TOP VIEW)



NC – No internal connection
Terminals 6 and 8 are internally connected.

LP PACKAGE (TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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LT1004-1.2, LT1004-2.5

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description/ordering information (continued)

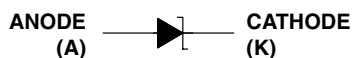
ORDERING INFORMATION[†]

T _A	V _Z TYP	PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	1.2 V	SOIC (D)	Tube of 75	LT1004CD-1-2	4C-12
			Reel of 2500	LT1004CDR-1-2	
		TSSOP (PW)	Tube of 150	LT1004CPW-1-2	4C-12
			Reel of 2000	LT1004CPWR-1-2	
	2.5 V	SOIC (D)	Tube of 75	LT1004CD-2-5	4C-25
			Reel of 2500	LT1004CDR-2-5	
		TSSOP (PW)	Tube of 150	LT1004CPW-2-5	4C-25
			Reel of 2000	LT1004CPWR-2-5	
–40°C to 85°C	1.2 V	SOIC (D)	Tube of 75	LT1004ID-1-2	4I-12
			Reel of 2500	LT1004IDR-1-2	
		TSSOP (PW)	Tube of 150	LT1004IPW-1-2	4I-12
			Reel of 2000	LT1004IPWR-1-2	
	2.5 V	SOIC (D)	Tube of 75	LT1004ID-2-5	4I-25
			Reel of 2500	LT1004IDR-2-5	
		TSSOP (PW)	Tube of 150	LT1004IPW-2-5	4I-25
			Reel of 2000	LT1004IPWR-2-5	

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

[‡] Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

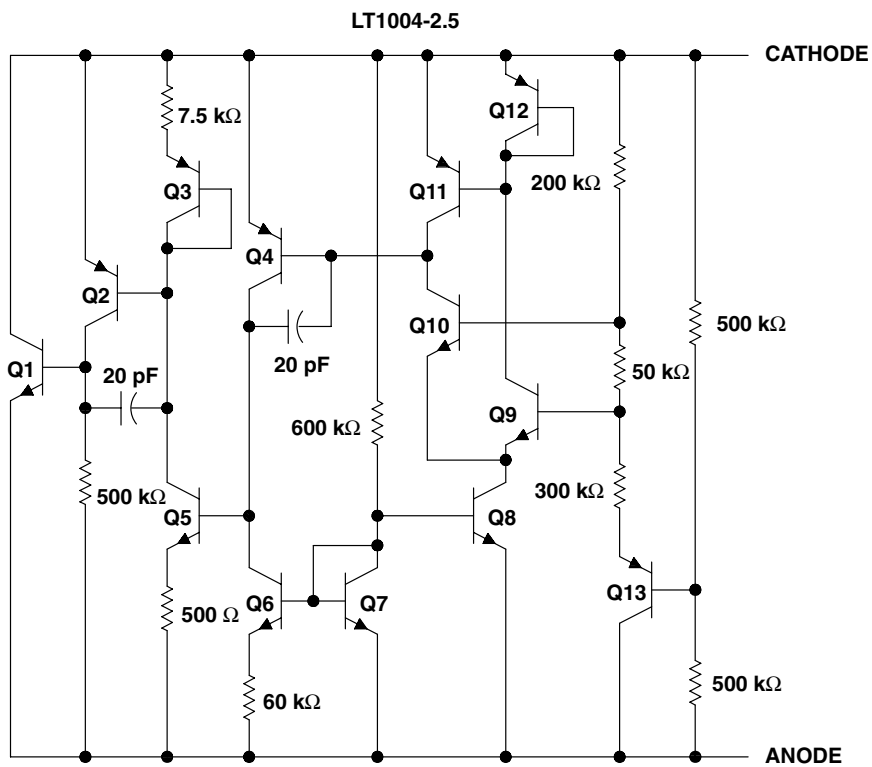
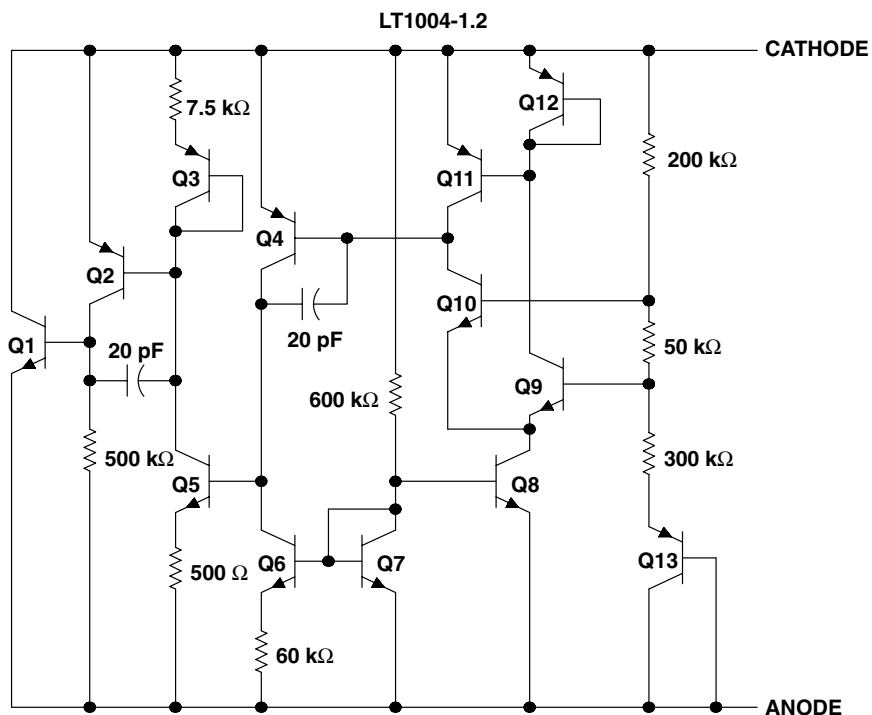
symbol



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schematic



NOTE A: All component values shown are nominal.

LT1004-1.2, LT1004-2.5

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Reverse current, I_R	30 mA
Forward current, I_F	10 mA
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package	97°C/W
PW package	149°C/W
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
T_A Operating free-air temperature	LT1004C	0	70	°C
	LT1004I	–40	85	

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T _A [‡]		LT1004-1.2			LT1004-2.5			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
V _Z	Reference voltage	I _Z = 100 μA	25°C		1.231	1.235	1.239	2.48	2.5	2.52	V	
			Full range	LT1004C	1.225		1.245		2.47	2.53		
				LT1004I	1.225		1.245		2.47	2.53		
α _{V_Z}	Average temperature coefficient of reference voltage [§]	I _Z = 10 μA	25°C		20						ppm/°C	
		I _Z = 20 μA			20							
ΔV _Z	Change in reference voltage with current	I _Z = I _Z (min) to 1 mA	25°C		1			1			mV	
			Full range		1.5			1.5				
		I _Z = 1 mA to 20 mA	25°C		10			10				
			Full range		20			20				
ΔV _Z /Δt	Long-term change in reference voltage	I _Z = 100 μA	25°C		20			20			ppm/khr	
I _Z (min)	Minimum reference current		Full range		8 10			12 20			μA	
z _Z	Reference impedance	I _Z = 100 μA	25°C		0.2 0.6			0.2 0.6			Ω	
			Full range		1.5			1.5				
V _n	Broadband noise voltage	I _Z = 100 μA, f = 10 Hz to 10 kHz	25°C		60			120			μV	

[‡] Full range is 0°C to 70°C for the LT1004C and –40°C to 85°C for the LT1004I.

[§] The average temperature coefficient of reference voltage is defined as the total change in reference voltage divided by the specified temperature range.



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TYPICAL CHARACTERISTICS

Table of Graphs

GRAPH TITLE	FIGURE
LT1004x-1.2	
Reverse current vs Reverse voltage	1
Reference-voltage change vs Reverse current	2
Forward voltage vs Forward current	3
Reference voltage vs Free-air temperature	4
Reference impedance vs Reference current	5
Noise voltage vs Frequency	6
Filtered output noise voltage vs Cutoff frequency	7
LT1004x-2.5	
Transient response	8
Reverse current vs Reverse voltage	9
Forward voltage vs Forward current	10
Reference voltage vs Free-air temperature	11
Reference impedance vs Reference current	12
Noise voltage vs Frequency	13
Filtered output noise voltage vs Cutoff frequency	14
Transient response	15

LT1004-1.2, LT1004-2.5
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TYPICAL CHARACTERISTICS†

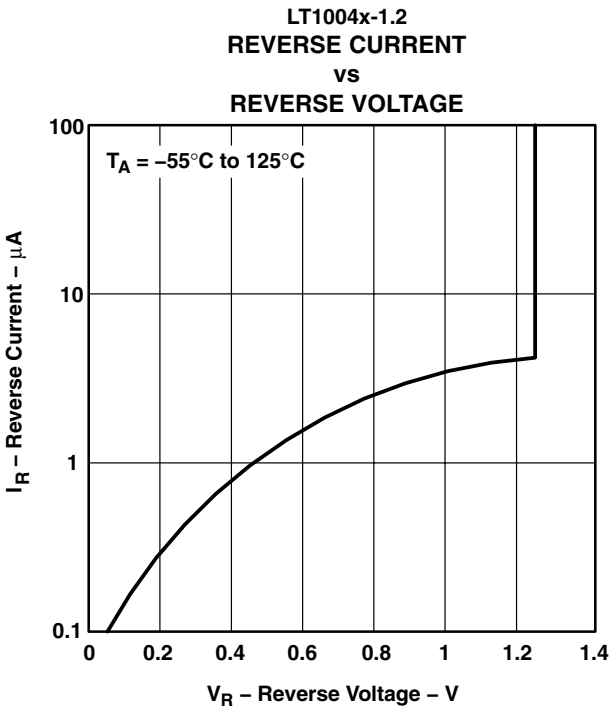


Figure 1

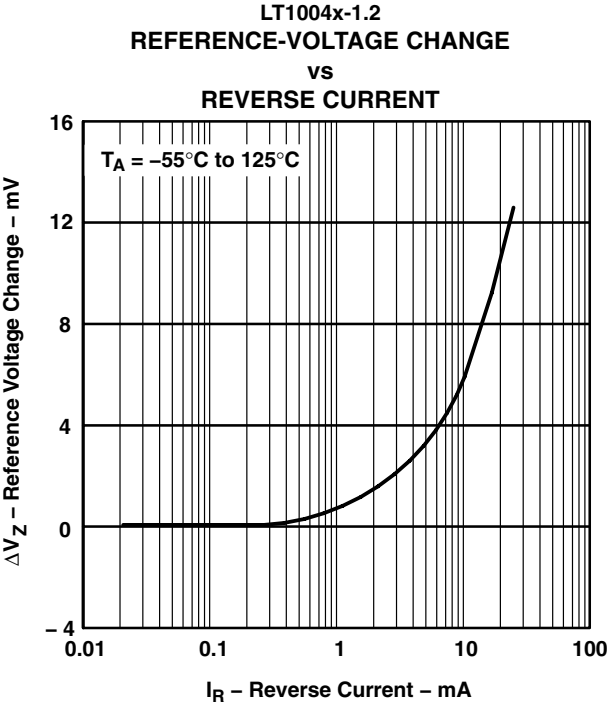


Figure 2

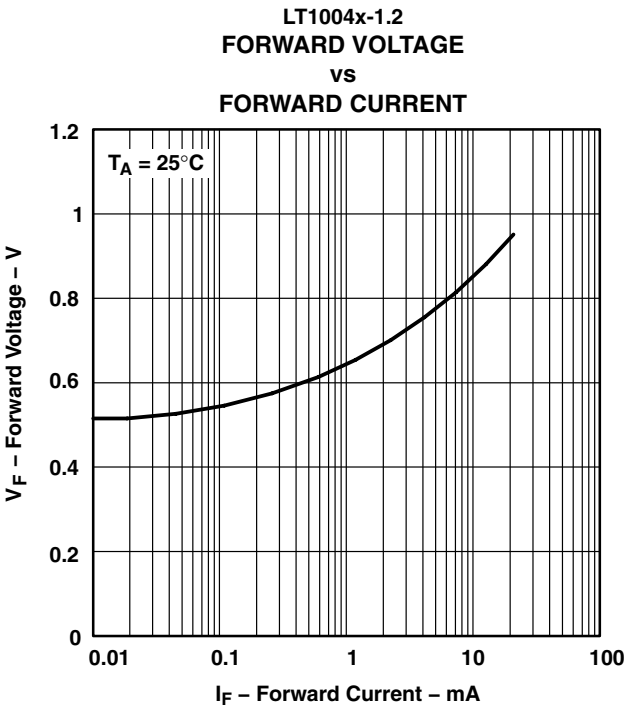


Figure 3

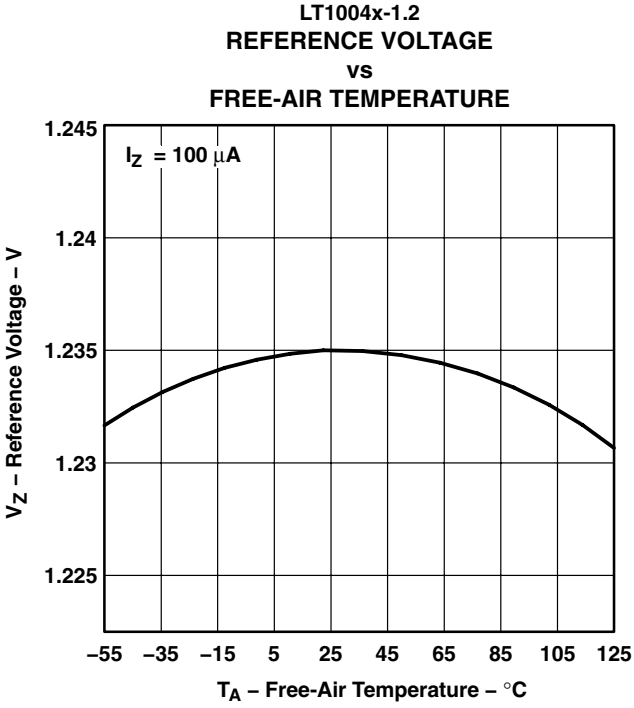


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

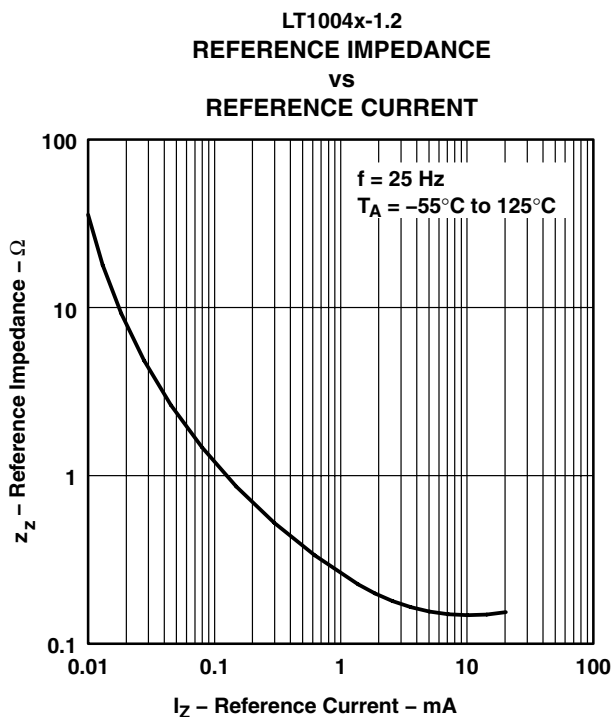


Figure 5

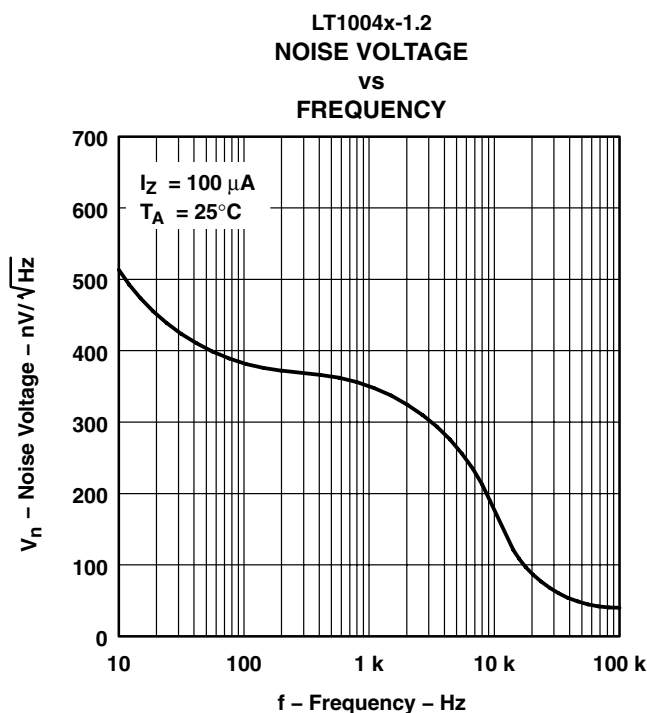


Figure 6

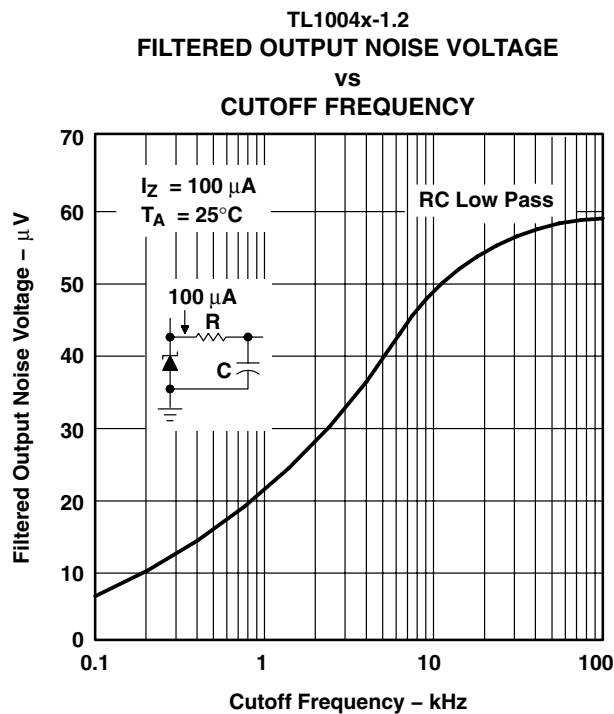


Figure 7

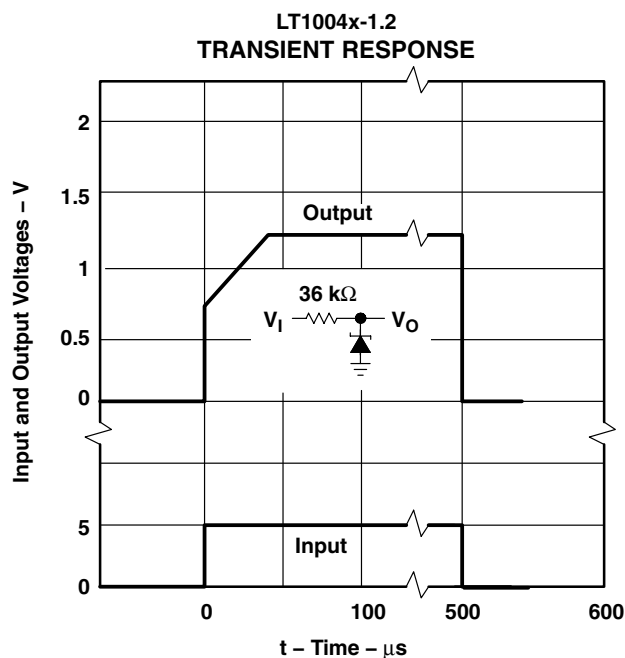


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

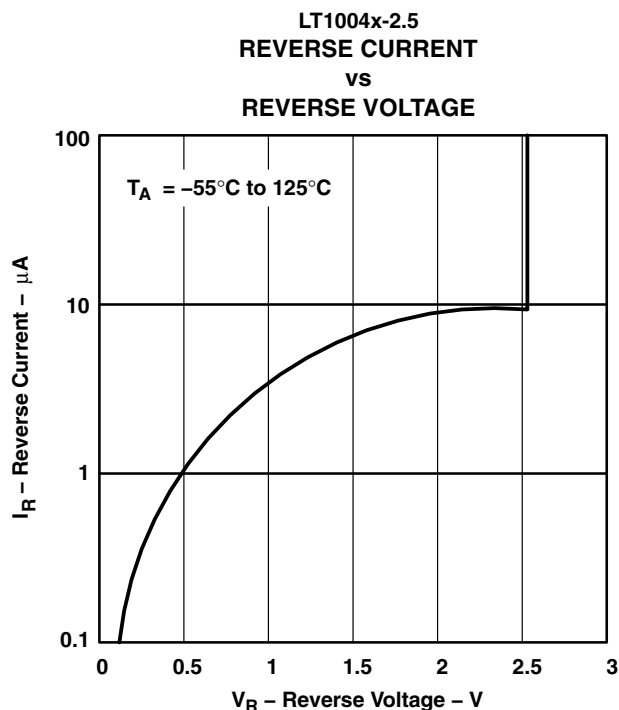


Figure 9

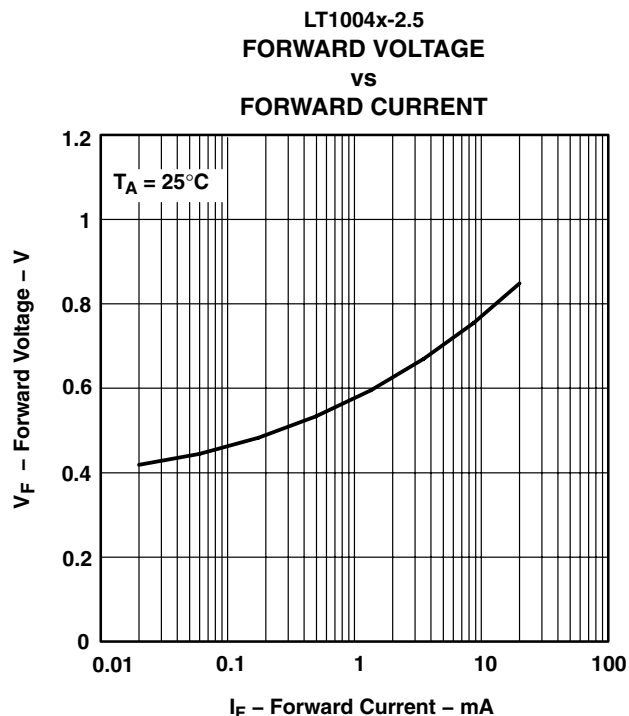


Figure 10

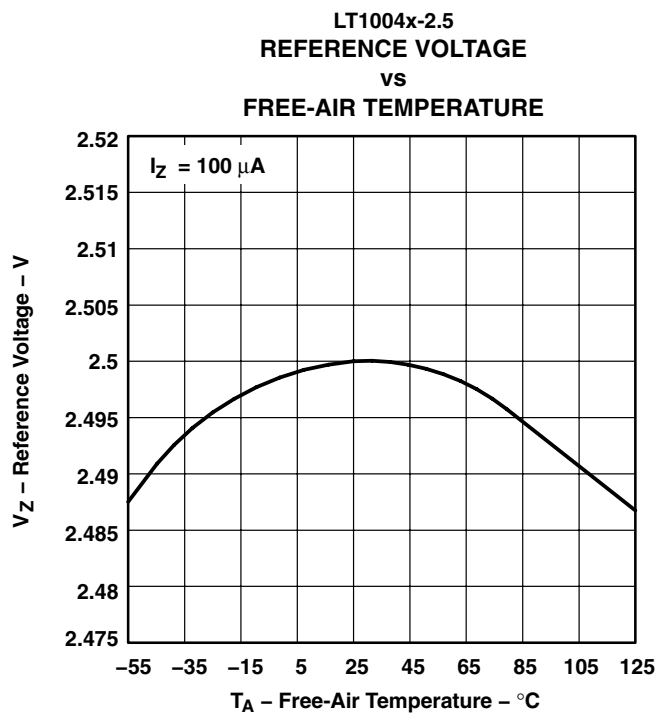


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

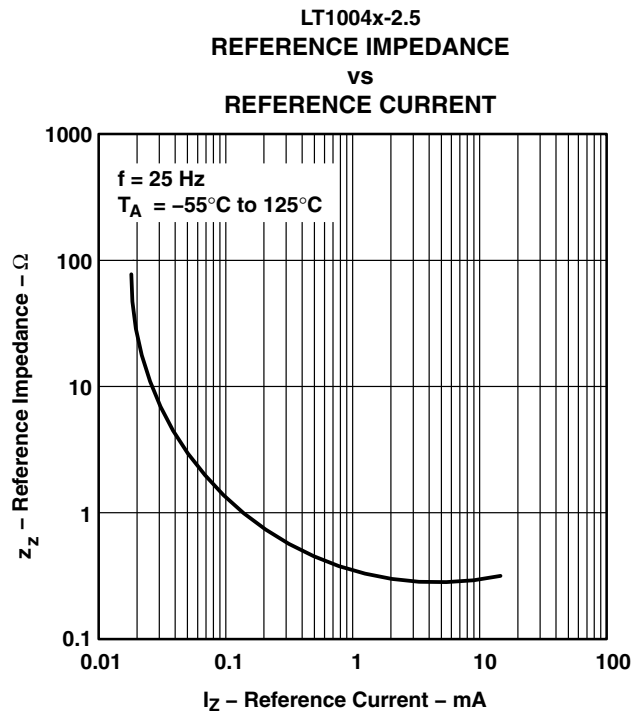


Figure 12

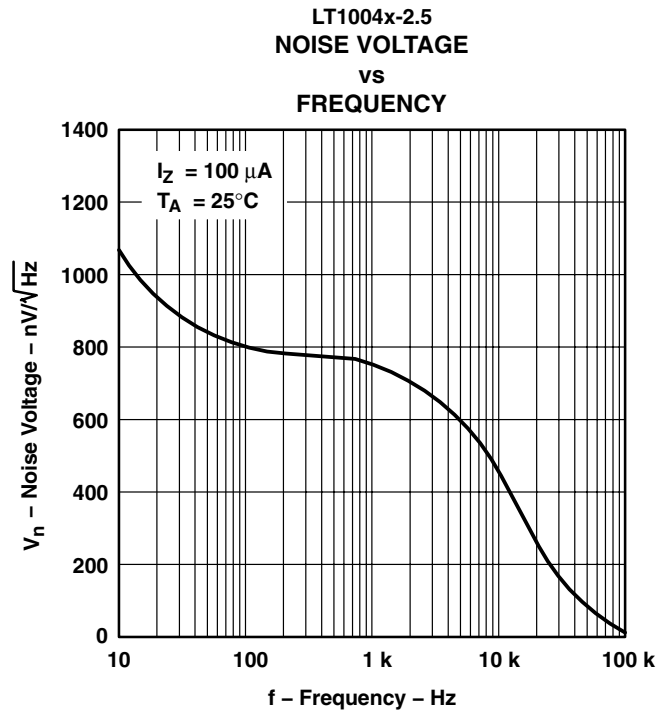


Figure 13

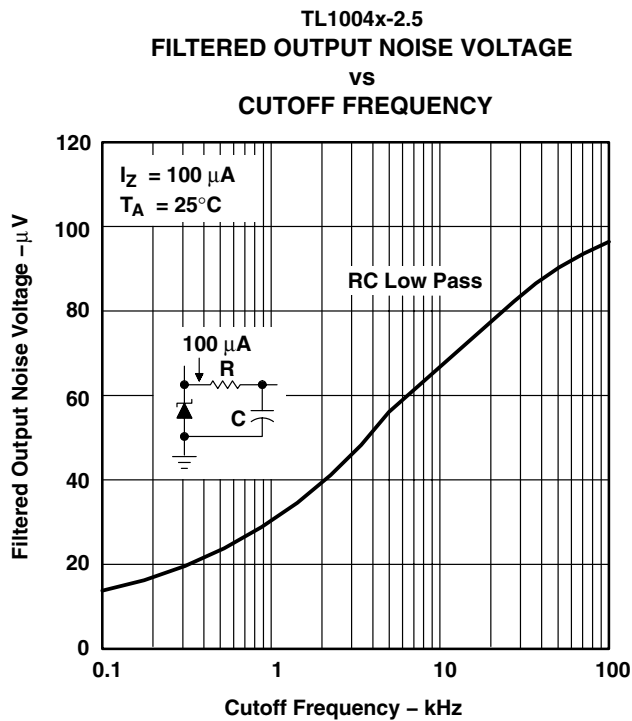


Figure 14

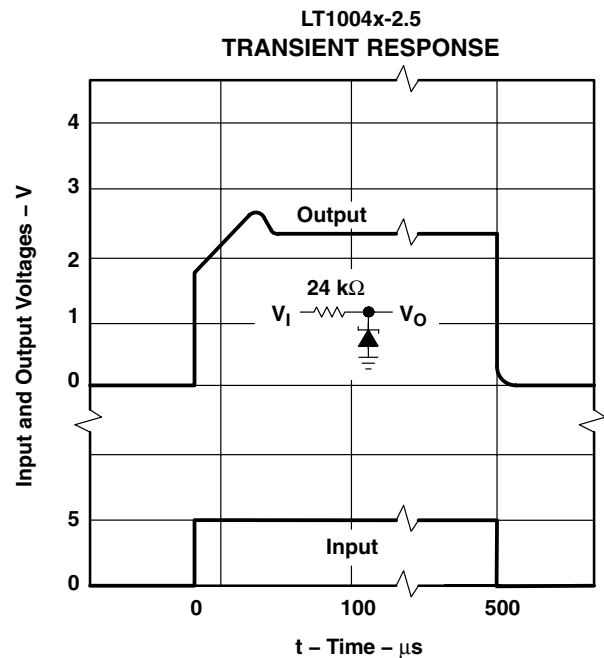


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

LT1004-1.2, LT1004-2.5 MICROPOWER INTEGRATED VOLTAGE REFERENCES

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APPLICATION INFORMATION

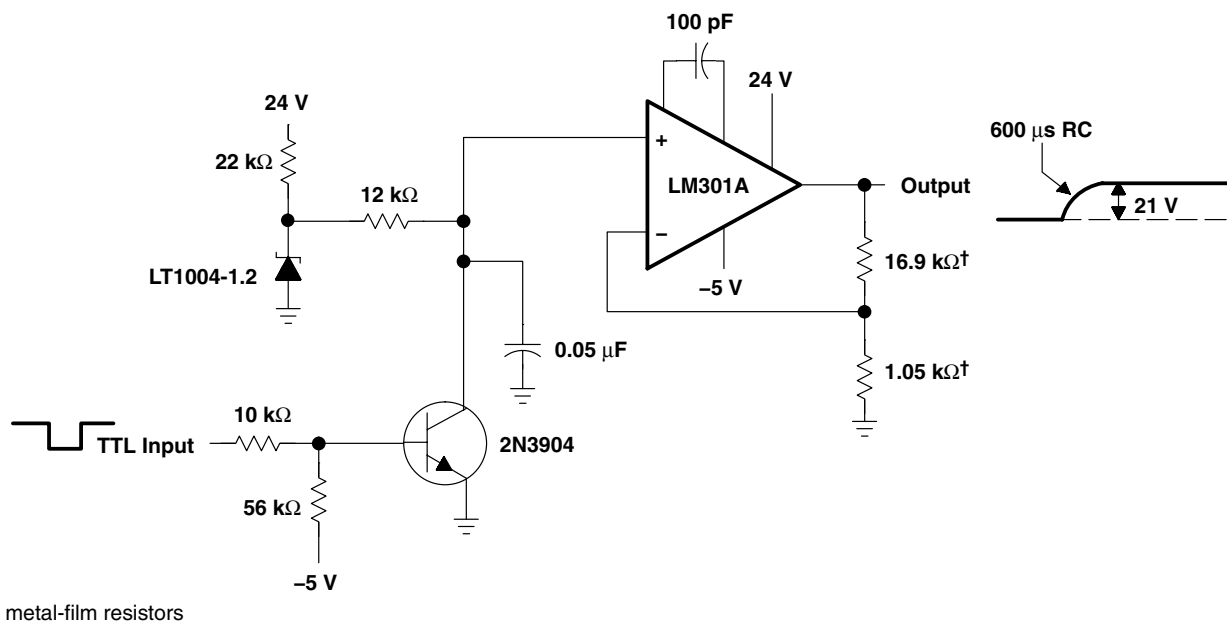


Figure 16. $V_{I(PP)}$ Generator for EPROMs (No Trim Required)

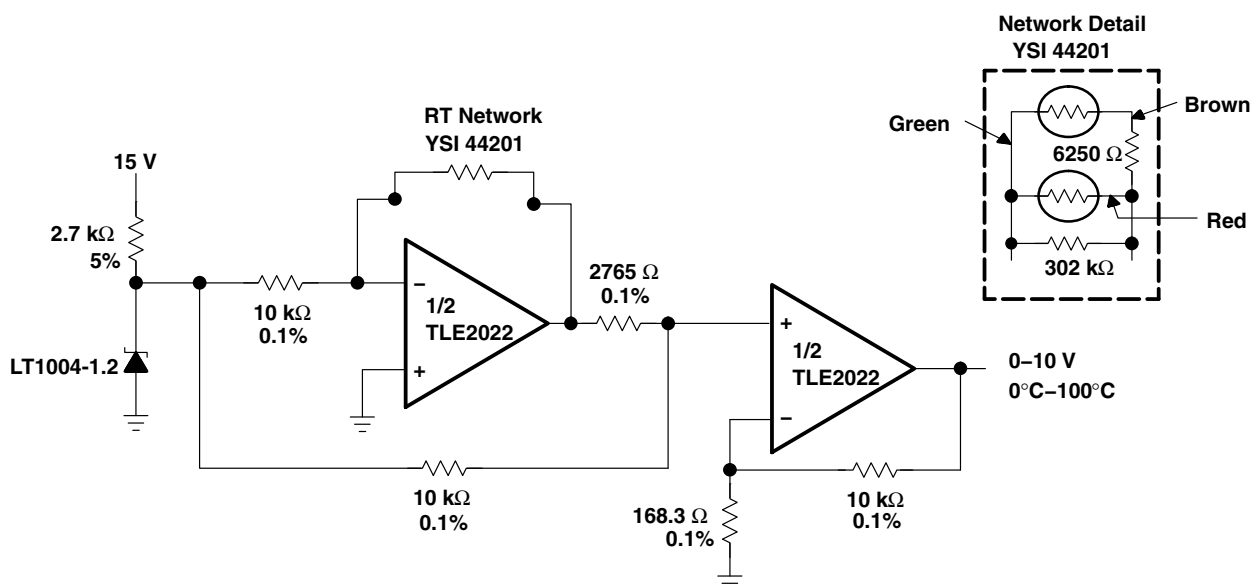


Figure 17. 0°C-to-100°C Linear-Output Thermometer

APPLICATION INFORMATION

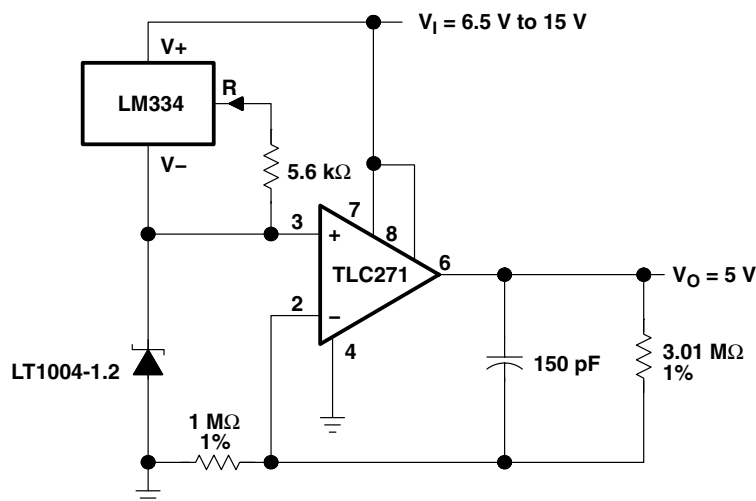


Figure 18. Micropower 5-V Reference

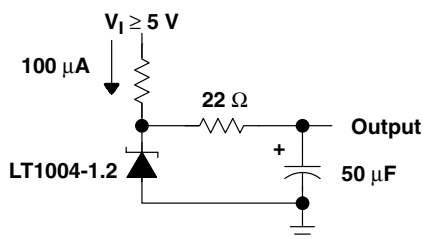


Figure 19. Low-Noise Reference

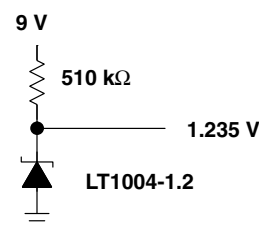
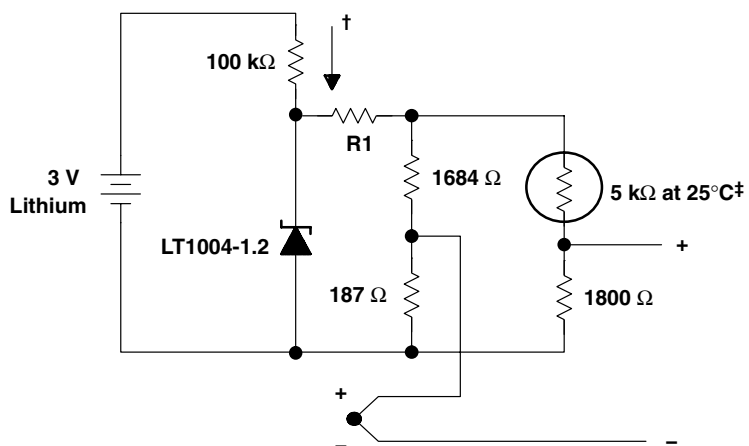


Figure 20. Micropower Reference From 9-V Battery



THERMOCOUPLE TYPE	R1
J	232 kΩ
K	298 kΩ
T	301 kΩ
S	2.1 MΩ

† Quiescent current $\cong 15 \mu\text{A}$

‡ Yellow Springs Inst. Co., Part #44007

NOTE A: This application compensates within $\pm 1^\circ\text{C}$ from 0°C to 60°C .

Figure 21. Micropower Cold-Junction Compensation for Thermocouples

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APPLICATION INFORMATION

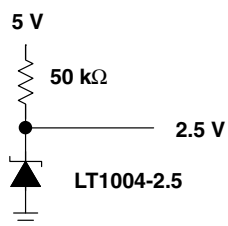


Figure 22. 2.5-V Reference

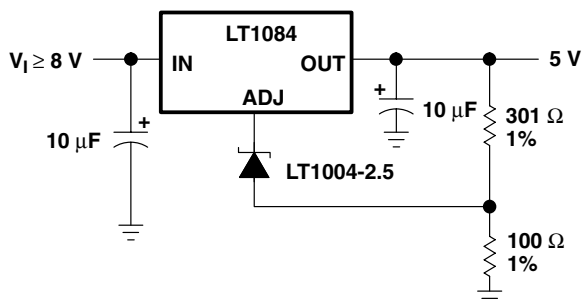
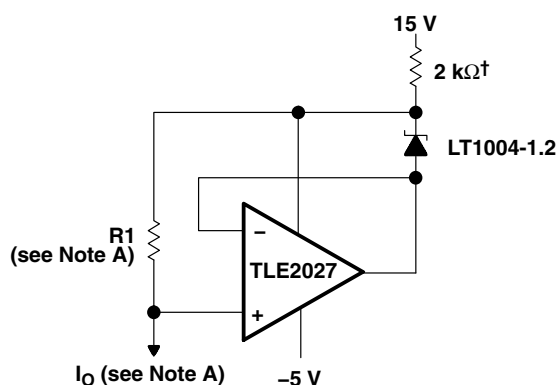


Figure 23. High-Stability 5-V Regulator



† May be increased for small output currents
NOTE A: $R1 \approx \frac{2V}{I_O + 10\mu A}$, $I_O = \frac{1.235V}{R1}$

Figure 24. Ground-Referenced Current Source

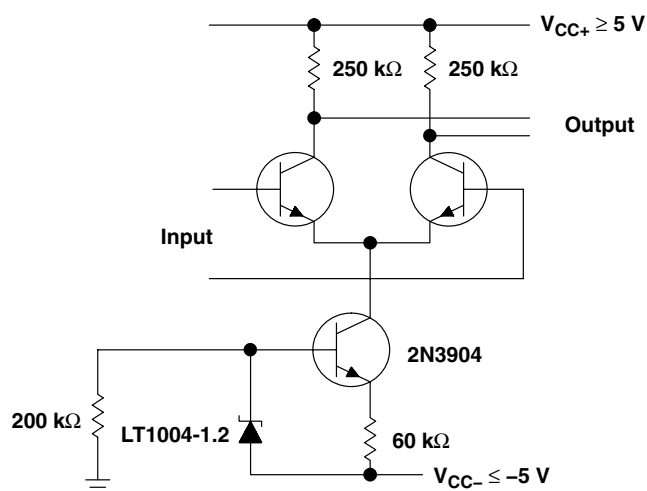
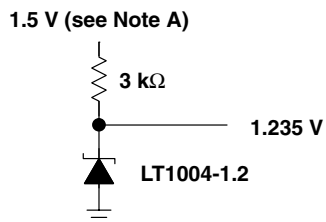


Figure 25. Amplifier With Constant Gain Over Temperature



NOTE A: Output regulates down to 1.285 V for $I_O = 0$.

Figure 26. 1.2-V Reference From 1.5-V Battery

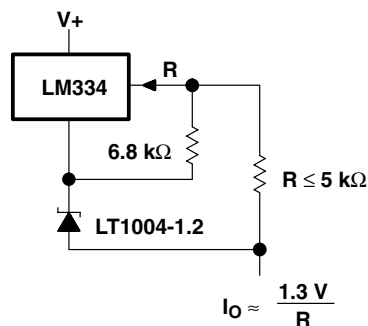
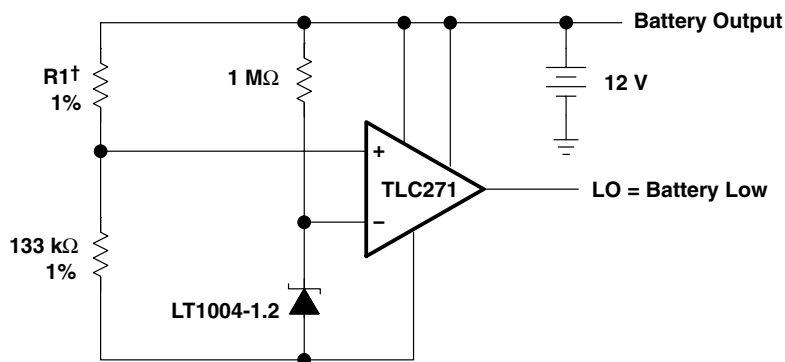


Figure 27. Terminal Current Source With Low Temperature Coefficient

APPLICATION INFORMATION



† R1 sets trip point, 60.4 kΩ per cell for 1.8 V per cell.

Figure 28. Lead-Acid Low-Battery-Voltage Detector

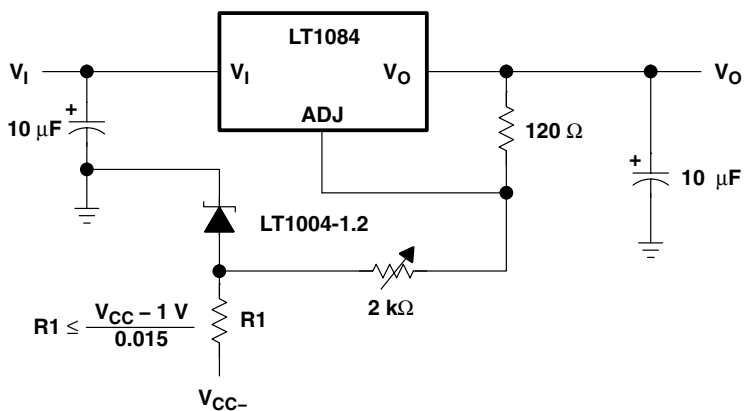


Figure 29. Variable-Voltage Supply

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LT1004CD-1-2	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	4C-12
LT1004CD-1-2.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4C-12
LT1004CD-2-5	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	4C-25
LT1004CD-2-5.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4C-25
LT1004CDR-1-2	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	4C-12
LT1004CDR-1-2.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4C-12
LT1004CDR-2-5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	4C-25
LT1004CDR-2-5.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4C-25
LT1004CPW-1-2	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4C-12
LT1004CPW-1-2.A	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4C-12
LT1004CPWR-1-2	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4C-12
LT1004CPWR-1-2.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4C-12
LT1004CPWR-2-5	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4C-25
LT1004CPWR-2-5.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4C-25
LT1004ID-1-2	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	4I-12
LT1004ID-1-2.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-12
LT1004ID-2-5	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	4I-25
LT1004ID-2-5.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-25
LT1004IDR-1-2	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-12
LT1004IDR-1-2.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-12
LT1004IDR-2-5	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	4I-25
LT1004IDR-2-5.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-25
LT1004IPW-1-2	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-12
LT1004IPW-1-2.A	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-12
LT1004IPW-2-5	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-25
LT1004IPW-2-5.A	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-25
LT1004IPWR-1-2	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-12
LT1004IPWR-1-2.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-12
LT1004IPWR-2-5	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-25

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LT1004IPWR-2-5.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4I-25

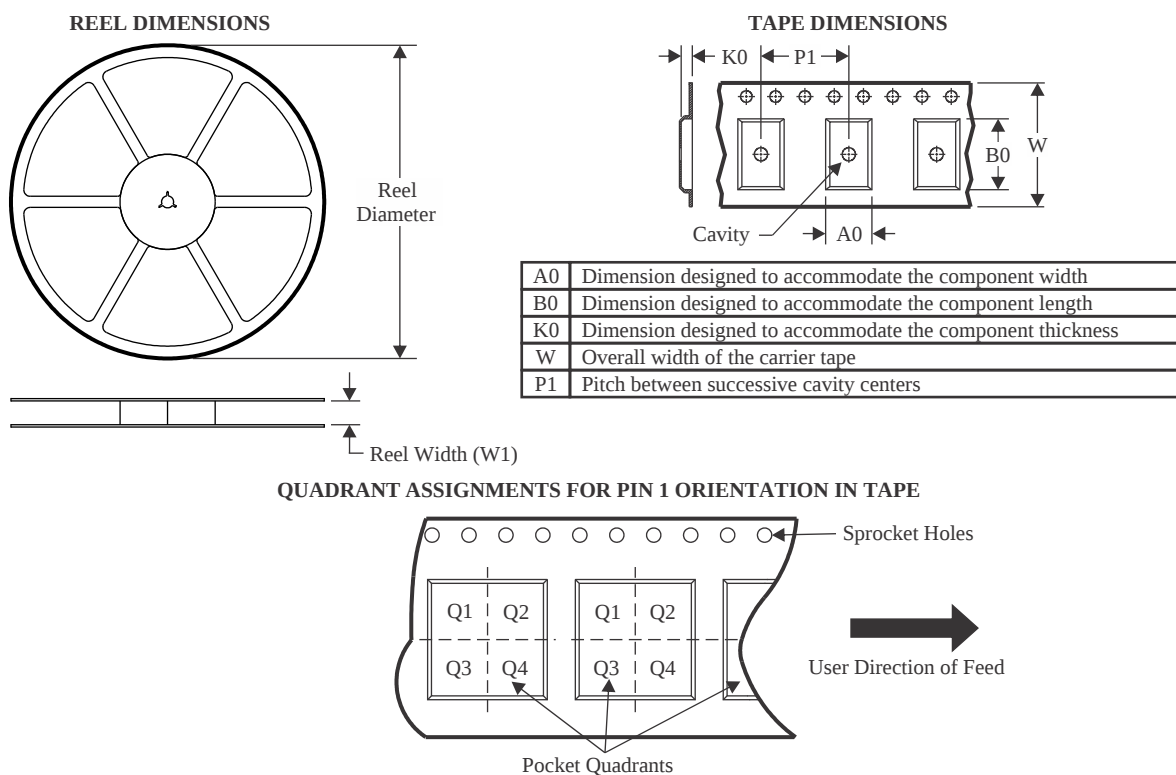
- (1) Status:** For more details on status, see our [product life cycle](#).
- (2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1004CDR-1-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1004CDR-2-5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1004CPWR-1-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LT1004CPWR-2-5	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LT1004IDR-1-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1004IDR-2-5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1004IPWR-1-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LT1004IPWR-2-5	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

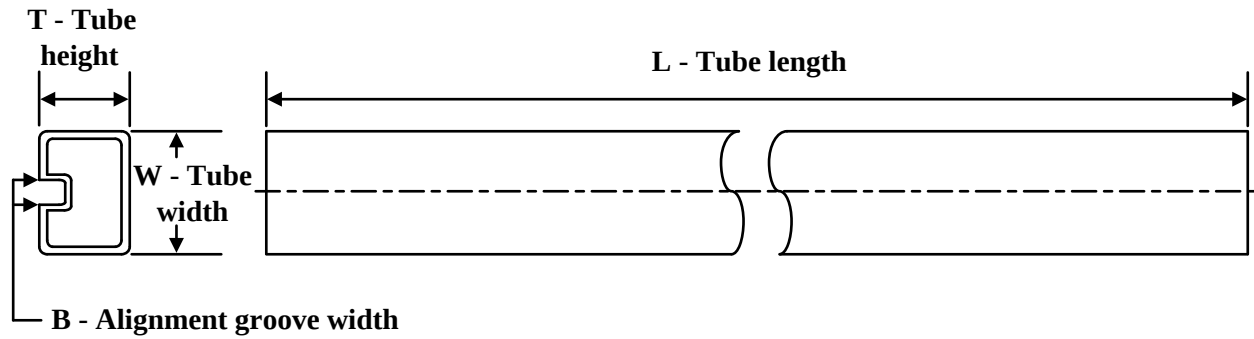
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

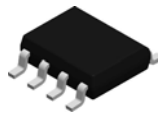
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1004CDR-1-2	SOIC	D	8	2500	353.0	353.0	32.0
LT1004CDR-2-5	SOIC	D	8	2500	353.0	353.0	32.0
LT1004CPWR-1-2	TSSOP	PW	8	2000	367.0	367.0	35.0
LT1004CPWR-2-5	TSSOP	PW	8	2000	367.0	367.0	35.0
LT1004IDR-1-2	SOIC	D	8	2500	353.0	353.0	32.0
LT1004IDR-2-5	SOIC	D	8	2500	353.0	353.0	32.0
LT1004IPWR-1-2	TSSOP	PW	8	2000	367.0	367.0	35.0
LT1004IPWR-2-5	TSSOP	PW	8	2000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LT1004CD-1-2	D	SOIC	8	75	506.6	8	3940	4.32
LT1004CD-1-2	D	SOIC	8	75	507	8	3940	4.32
LT1004CD-1-2.A	D	SOIC	8	75	506.6	8	3940	4.32
LT1004CD-1-2.A	D	SOIC	8	75	507	8	3940	4.32
LT1004CD-2-5	D	SOIC	8	75	507	8	3940	4.32
LT1004CD-2-5.A	D	SOIC	8	75	507	8	3940	4.32
LT1004CPW-1-2	PW	TSSOP	8	150	530	10.2	3600	3.5
LT1004CPW-1-2.A	PW	TSSOP	8	150	530	10.2	3600	3.5
LT1004ID-1-2	D	SOIC	8	75	507	8	3940	4.32
LT1004ID-1-2.A	D	SOIC	8	75	507	8	3940	4.32
LT1004ID-2-5	D	SOIC	8	75	507	8	3940	4.32
LT1004ID-2-5.A	D	SOIC	8	75	507	8	3940	4.32
LT1004IPW-1-2	PW	TSSOP	8	150	530	10.2	3600	3.5
LT1004IPW-1-2.A	PW	TSSOP	8	150	530	10.2	3600	3.5
LT1004IPW-2-5	PW	TSSOP	8	150	530	10.2	3600	3.5
LT1004IPW-2-5.A	PW	TSSOP	8	150	530	10.2	3600	3.5

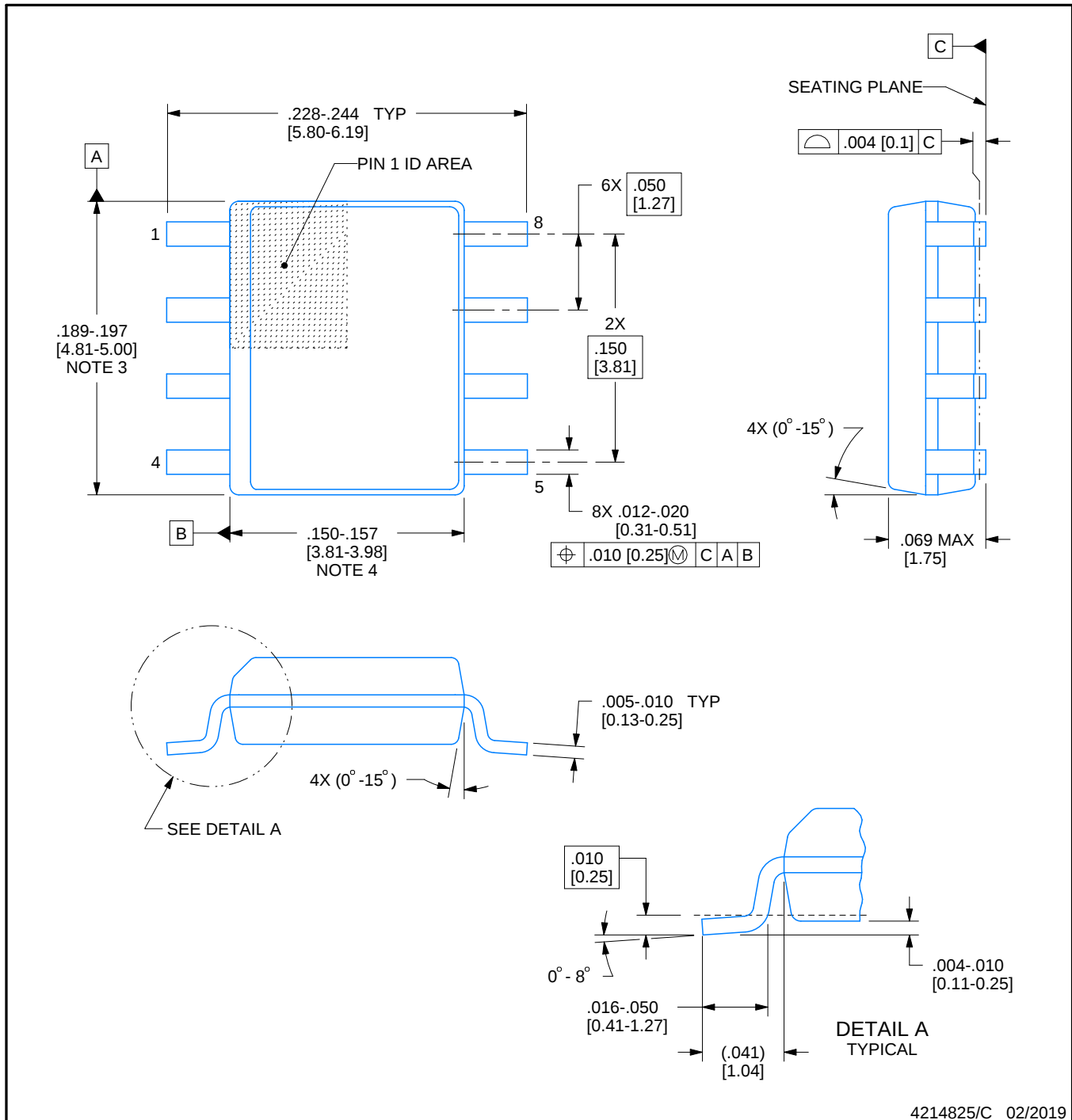


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

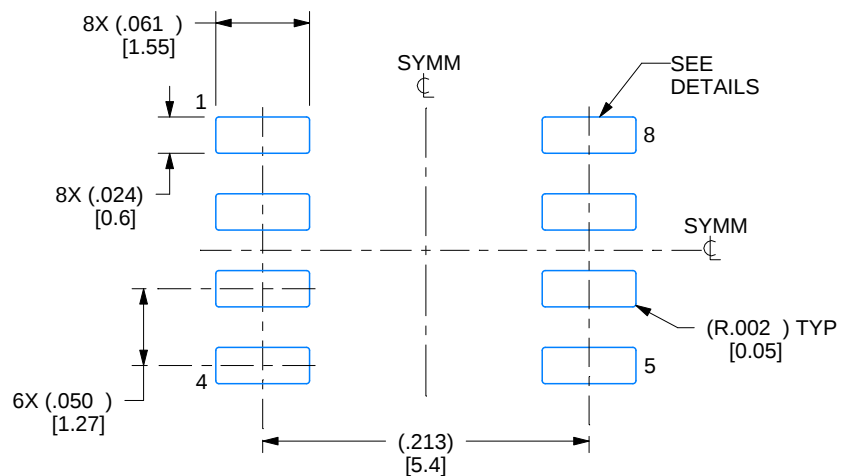
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

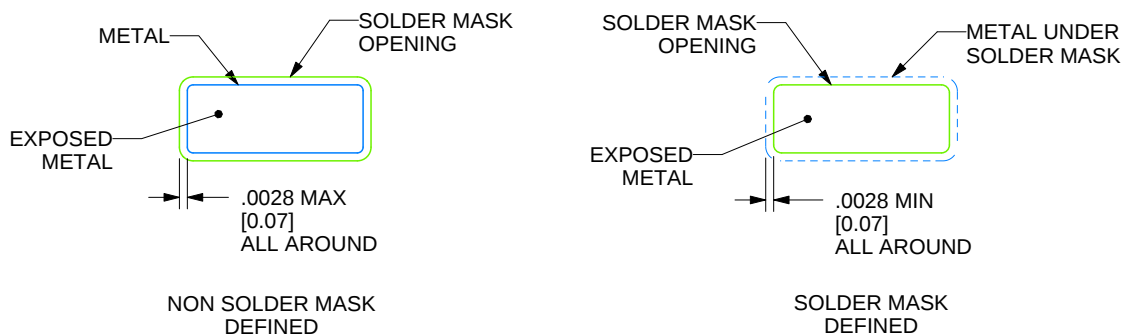
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

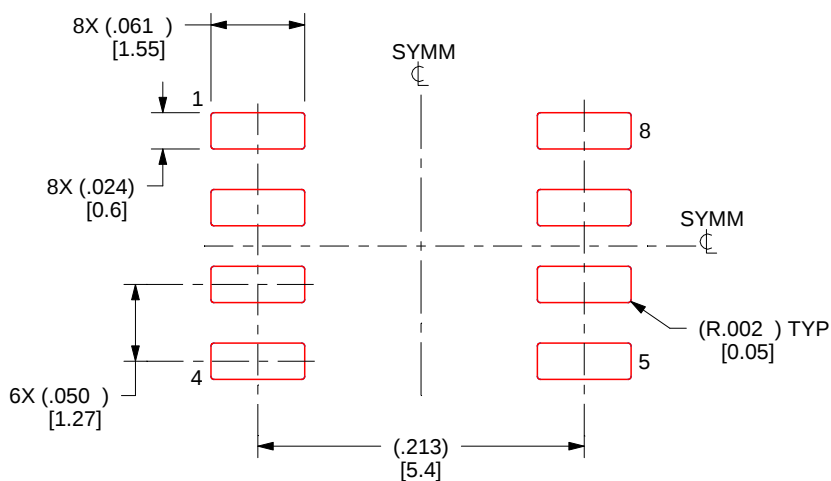
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

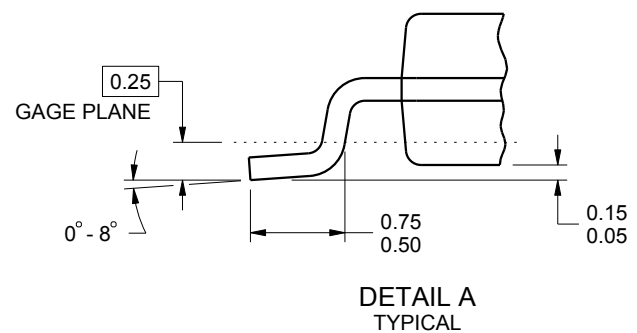
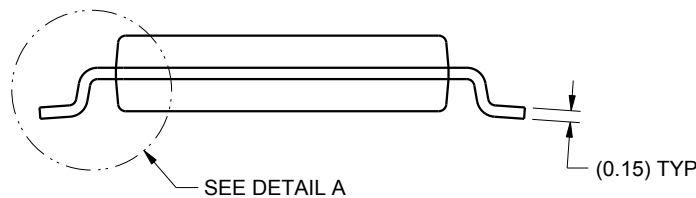
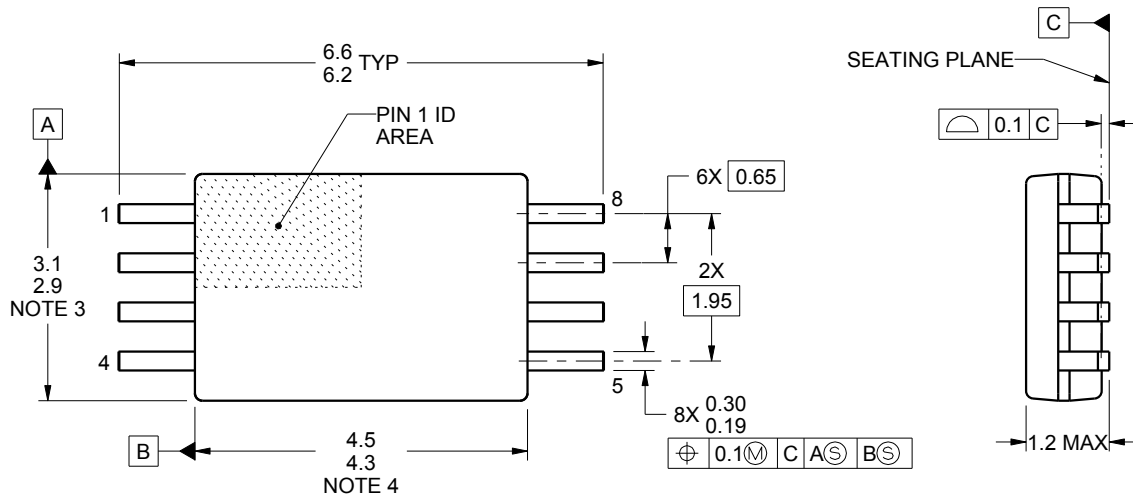
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

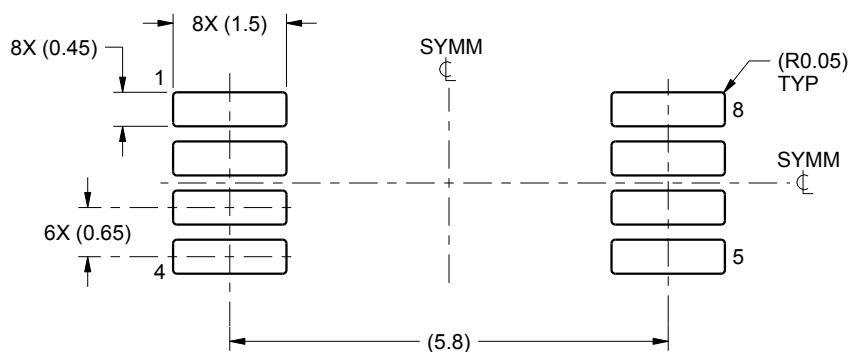
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

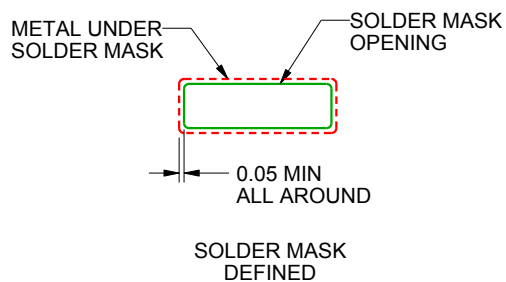
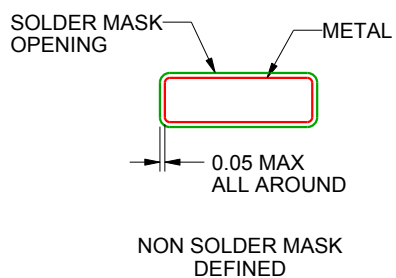
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

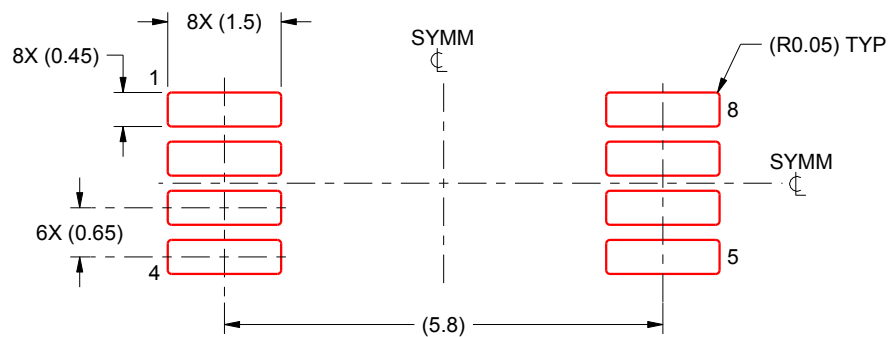
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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