

## LMH6572 Triple 2:1 High Speed Video Multiplexer

### 1 Features

- 350-MHz, 250-mV, –3-dB Bandwidth
- 290-MHz, 2-V<sub>PP</sub>, –3-dB Bandwidth
- 10-ns Channel Switching Time
- 90-dB Channel to Channel Isolation at 5 MHz
- 0.02%, 0.02° Diff. Gain, Phase
- 0.1-dB Gain Flatness to 140 MHz
- 1400-V/μs Slew Rate
- Wide Supply Voltage Range:  
6 V (±3 V) to 12 V (±6 V)
- –78-dB HD2 at 10 MHz
- –75-dB HD3 at 10 MHz

### 2 Applications

- RGB Video Router
- Multi Input Video Monitor
- Fault Tolerant Data Switch

### 3 Description

The LMH6572 is a high performance analog multiplexer optimized for professional grade video and other high fidelity, high bandwidth analog applications. The LMH6572 provides a 290-MHz bandwidth at 2-V<sub>PP</sub> output signal levels. The 140 MHz of 0.1-dB bandwidth and a 1500-V/μs slew rate make this part suitable for high definition television (HDTV) and high resolution multimedia video applications.

The LMH6572 supports composite video applications with its 0.02% and 0.02° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75-Ω load. The LM6572 can deliver 80-mA linear output current for driving multiple video load applications.

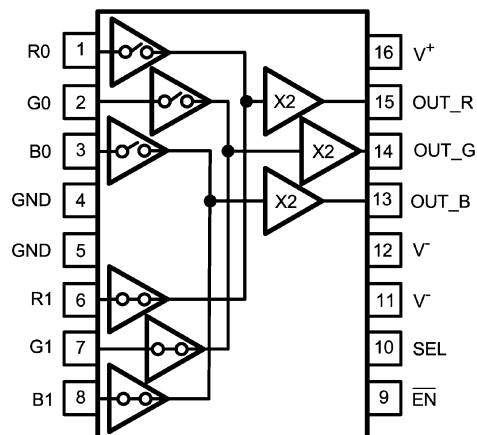
The LMH6572 has an internal gain of 2 V/V (+6 dBv) for driving back terminated transmission lines at a net gain of 1 V/V (0 dBv).

The LMH6572 is available in the SSOP package.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE (NOM)   |
|-------------|-----------|-------------------|
| LMH6572     | SSOP (16) | 4.90 mm × 3.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

|                                                 |           |                                                                  |           |
|-------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                         | <b>1</b>  | 7.1 Overview .....                                               | <b>11</b> |
| <b>2 Applications</b> .....                     | <b>1</b>  | 7.2 Feature Description .....                                    | <b>11</b> |
| <b>3 Description</b> .....                      | <b>1</b>  | <b>8 Power Supply Recommendations</b> .....                      | <b>15</b> |
| <b>4 Revision History</b> .....                 | <b>2</b>  | 8.1 Power Dissipation .....                                      | <b>15</b> |
| <b>5 Pin Configuration and Functions</b> .....  | <b>3</b>  | 8.2 ESD Protection .....                                         | <b>15</b> |
| <b>6 Specifications</b> .....                   | <b>4</b>  | <b>9 Layout</b> .....                                            | <b>16</b> |
| 6.1 Absolute Maximum Ratings .....              | <b>4</b>  | 9.1 Layout Guidelines .....                                      | <b>16</b> |
| 6.2 ESD Ratings .....                           | <b>4</b>  | <b>10 Device and Documentation Support</b> .....                 | <b>17</b> |
| 6.3 Recommended Operating Conditions .....      | <b>4</b>  | 10.1 Receiving Notification of Documentation Updates .....       | <b>17</b> |
| 6.4 Thermal Information .....                   | <b>4</b>  | 10.2 Community Resources .....                                   | <b>17</b> |
| 6.5 $\pm 5V$ Electrical Characteristics .....   | <b>5</b>  | 10.3 Trademarks .....                                            | <b>17</b> |
| 6.6 $\pm 3.3V$ Electrical Characteristics ..... | <b>7</b>  | 10.4 Electrostatic Discharge Caution .....                       | <b>17</b> |
| 6.7 Typical Characteristics .....               | <b>8</b>  | 10.5 Glossary .....                                              | <b>17</b> |
| <b>7 Detailed Description</b> .....             | <b>11</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>17</b> |

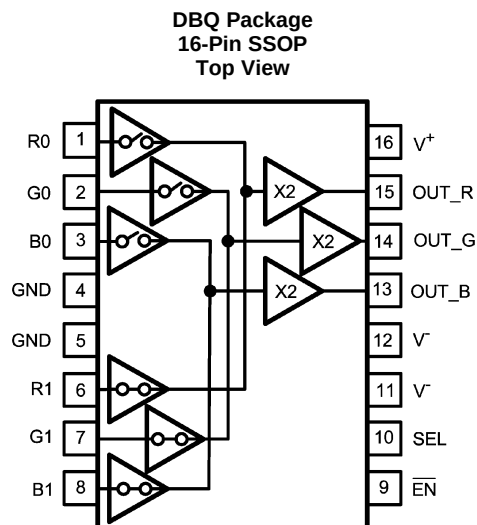
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (May 2013) to Revision G                                                                                                                                                                                                                                                                                                      | Page      |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| • Deleted preview watermark .....                                                                                                                                                                                                                                                                                                                     | <b>1</b>  |
| • Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>1</b>  |
| • Deleted bolding from Electrical Characteristics specifications, added temperature range to test conditions for clarification .....                                                                                                                                                                                                                  | <b>5</b>  |
| • Changed <i>Overview</i> title from <i>General Information</i> .....                                                                                                                                                                                                                                                                                 | <b>11</b> |
| • Changed <i>Layout Considerations</i> title to <i>Layout Guidelines</i> .....                                                                                                                                                                                                                                                                        | <b>16</b> |

| Changes from Revision E (April 2013) to Revision F                       | Page      |
|--------------------------------------------------------------------------|-----------|
| • Changed layout of National Semiconductor Data Sheet to TI format ..... | <b>16</b> |

## 5 Pin Configuration and Functions



**Truth Table**

| SEL | $\overline{\text{EN}}$ | OUT     |
|-----|------------------------|---------|
| 0   | 0                      | CH 1    |
| 1   | 0                      | CH 0    |
| X   | 1                      | Disable |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

see <sup>(1)(2)</sup>

|                                             | MIN | MAX        | UNIT |
|---------------------------------------------|-----|------------|------|
| Supply Voltage ( $V^+ - V^-$ )              |     | 13.2       | V    |
| $I_{OUT}^{(3)}$                             |     | 130        | mA   |
| Input Voltage Range                         |     | $\pm(V_S)$ | V    |
| Maximum Junction Temperature <sup>(4)</sup> |     | +150       | °C   |
| Storage temperature, $T_{stg}$              | –65 | +150       | °C   |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) The maximum output current ( $I_{OUT}$ ) is determined by the device power dissipation limitations. See the [Power Dissipation](#) section for more details. A short circuit condition should be limited to 5 seconds or less.
- (4) Human Body Model, 1.5 k $\Omega$  in series with 100 pF. Machine Model 0  $\Omega$  in series with 200 pF.

### 6.2 ESD Ratings

|             |                         |                                                                   | VALUE      | UNIT |
|-------------|-------------------------|-------------------------------------------------------------------|------------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup> | $\pm 2000$ | V    |
|             |                         | Machine model (MM)                                                | $\pm 200$  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

see <sup>(1)</sup>

|  |                       | MIN | NOM | MAX | UNIT |
|--|-----------------------|-----|-----|-----|------|
|  | Operating Temperature | –40 |     | 85  | °C   |
|  | Supply Voltage Range  | 6   |     | 12  | V    |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                           | LMH6572    | UNIT |
|-------------------------------|-------------------------------------------|------------|------|
|                               |                                           | DBQ (SSOP) |      |
|                               |                                           | 16 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance    | 125        | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance | 36         | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 ±5V Electrical Characteristics

 $V_S = \pm 5\text{ V}$  and  $R_L = 100\ \Omega$ , (unless otherwise noted)

| PARAMETER                           |                                                | TEST CONDITIONS <sup>(1)</sup>                                                                      | MIN  | TYP   | MAX   | UNIT                         |
|-------------------------------------|------------------------------------------------|-----------------------------------------------------------------------------------------------------|------|-------|-------|------------------------------|
| <b>FREQUENCY DOMAIN PERFORMANCE</b> |                                                |                                                                                                     |      |       |       |                              |
| SSBW                                | –3 dB Bandwidth                                | $V_{OUT} = 0.25\ V_{PP}$                                                                            |      | 350   |       | MHz                          |
| LSBW                                | –3 dB Bandwidth <sup>(2)</sup>                 | $V_{OUT} = 2\ V_{PP}$                                                                               | 250  | 290   |       | MHz                          |
| .1 dBBW                             | 0.1 dB Bandwidth                               | $V_{OUT} = 0.25\ V_{PP}$                                                                            |      | 140   |       | MHz                          |
| DG                                  | Differential Gain                              | $R_L = 150\ \Omega$ , $f = 4.43\text{ MHz}$                                                         |      | 0.02% |       |                              |
| DP                                  | Differential Phase                             | $R_L = 150\ \Omega$ , $f = 4.43\text{ MHz}$                                                         |      | 0.02  |       | deg                          |
| <b>TIME DOMAIN RESPONSE</b>         |                                                |                                                                                                     |      |       |       |                              |
| TRS                                 | Channel to Channel Switching Time              | Logic Transition to 90% Output                                                                      |      | 10    |       | ns                           |
|                                     | Enable and Disable Times                       | Logic Transition to 90% or 10% Output                                                               |      | 11    |       | ns                           |
| TRL                                 | Rise and Fall Time                             | 2-V Step                                                                                            |      | 1.5   |       | ns                           |
| TSS                                 | Settling Time to 0.05%                         | 2-V Step                                                                                            |      | 17    |       | ns                           |
| OS                                  | Overshoot                                      | 4-V Step                                                                                            |      | 5%    |       |                              |
| SR                                  | Slew Rate <sup>(2)</sup>                       | 4-V Step                                                                                            | 1200 | 1400  |       | V/ $\mu$ s                   |
| <b>DISTORTION</b>                   |                                                |                                                                                                     |      |       |       |                              |
| HD2                                 | 2 <sup>nd</sup> Harmonic Distortion            | $2\ V_{PP}$ , 10 MHz                                                                                |      | –78   |       | dBc                          |
| HD3                                 | 3 <sup>rd</sup> Harmonic Distortion            | $2\ V_{PP}$ , 10 MHz                                                                                |      | –75   |       | dBc                          |
| IMD                                 | 3 <sup>rd</sup> Order Intermodulation Products | 10 MHz, Two tones $2\ V_{PP}$ at Output                                                             |      | –80   |       | dBc                          |
| <b>EQUIVALENT INPUT NOISE</b>       |                                                |                                                                                                     |      |       |       |                              |
| VN                                  | Voltage                                        | >1 MHz, Input Referred                                                                              |      | 5     |       | nV/ $\sqrt{\text{Hz}}$       |
| ICN                                 | Current                                        | >1 MHz, Input Referred                                                                              |      | 5     |       | pA/ $\sqrt{\text{Hz}}$       |
| <b>STATIC, DC PERFORMANCE</b>       |                                                |                                                                                                     |      |       |       |                              |
| GAIN                                | Voltage Gain                                   |                                                                                                     |      | 2.0   |       | V/V                          |
|                                     | Gain Error <sup>(3)</sup>                      | No load, with respect to nominal gain of 2.00 V/V                                                   |      | ±0.3% | ±0.5% |                              |
|                                     |                                                | No load, with respect to nominal gain of 2.00 V/V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ |      | ±0.3% | ±0.7% |                              |
|                                     | Gain Error                                     | $R_L = 50\ \Omega$ , with respect to nominal gain of 2.00 V/V                                       |      | 0.3%  |       |                              |
| VIO                                 | Output Offset Voltage <sup>(3)</sup>           | $V_{IN} = 0\text{ V}$                                                                               |      | 1     | ±14   | mV                           |
|                                     |                                                | $V_{IN} = 0\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$                            |      | 1     | ±17.5 |                              |
| DVIO                                | Average Drift                                  |                                                                                                     |      | 27    |       | $\mu\text{V}/^\circ\text{C}$ |
| IBN                                 | Input Bias Current <sup>(3)(4)</sup>           | $V_{IN} = 0\text{ V}$                                                                               |      | –1.4  | ±5.0  | $\mu\text{A}$                |
|                                     |                                                | $V_{IN} = 0\text{ V}$ , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$                            |      | –1.4  | ±5.6  |                              |
| DIBN                                | Average Drift                                  |                                                                                                     |      | 7     |       | nA/ $^\circ\text{C}$         |
| PSRR                                | Power Supply Rejection Ratio <sup>(3)</sup>    | DC, Input referred                                                                                  | 50   | 54    |       | dB                           |
|                                     |                                                | DC, Input referred, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$                                | 48   | 54    |       |                              |
| ICC                                 | Supply Current <sup>(3)</sup>                  | No load                                                                                             | 20   | 23    | 25    | mA                           |
|                                     |                                                | No load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$                                           | 20   | 23    | 28.5  |                              |
|                                     | Supply Current Disabled <sup>(3)</sup>         | No load                                                                                             |      | 2.0   | 2.2   | mA                           |
|                                     |                                                | No load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$                                           |      | 2.0   | 2.3   |                              |
| VIH                                 | Logic High Threshold <sup>(3)</sup>            | Select and Enable Pins                                                                              | 2.0  |       |       | V                            |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where  $T_J > T_A$ . See the [Power Dissipation](#) section for information on temperature de-rating of this device. Minimum and maximum ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Parameters ensured by design.

(3) Parameters ensured by electrical testing at  $25^\circ\text{C}$ .

(4) Positive Value is current into device.

## ±5V Electrical Characteristics (continued)

 $V_S = \pm 5\text{ V}$  and  $R_L = 100\ \Omega$ , (unless otherwise noted)

| PARAMETER                 |                                                | TEST CONDITIONS <sup>(1)</sup>                               | MIN   | TYP   | MAX  | UNIT |
|---------------------------|------------------------------------------------|--------------------------------------------------------------|-------|-------|------|------|
| VIL                       | Logic Low Threshold <sup>(3)</sup>             | Select and Enable Pins                                       |       |       | 0.8  | V    |
| IiL                       | Logic Pin Input Current Low <sup>(4)</sup>     | Logic Input = 0 V                                            |       | -1    | ±5.0 | μA   |
|                           |                                                | Logic Input = 0 V, T <sub>A</sub> = -40°C to +85°C           |       | -1    | ±15  |      |
| IiH                       | Logic Pin Input Current High <sup>(4)</sup>    | Logic Input = 2.0 V                                          | 112   | 150   | 200  | μA   |
|                           |                                                | Logic Input = 2.0 V, T <sub>A</sub> = -40°C to +85°C         | 100   | 150   | 210  |      |
| MISCELLANEOUS PERFORMANCE |                                                |                                                              |       |       |      |      |
| RF                        | Internal Feedback and Gain Set Resistor Values |                                                              | 650   | 800   | 940  | Ω    |
|                           |                                                | T <sub>A</sub> = -40°C to +85°C                              | 620   | 800   | 1010 |      |
| RODIS                     | Disabled Output Resistance                     | Internal Feedback and Gain Set Resistors in Series to Ground | 1.3   | 1.6   | 1.88 | kΩ   |
| RIN+                      | Input Resistance                               |                                                              |       | 100   |      | kΩ   |
| CIN                       | Input Capacitance                              |                                                              |       | 0.9   |      | pF   |
| ROUT                      | Output Resistance                              |                                                              |       | 0.26  |      | Ω    |
| VO                        | Output Voltage Range                           | No Load                                                      | ±3.83 | ±3.9  |      | V    |
|                           |                                                | No Load, T <sub>A</sub> = -40°C to +85°C                     | ±3.80 | ±3.9  |      |      |
| VOL                       |                                                | R <sub>L</sub> = 100 Ω                                       | ±3.52 | ±3.53 |      | V    |
|                           |                                                | R <sub>L</sub> = 100 Ω, T <sub>A</sub> = -40°C to +85°C      | ±3.5  | ±3.53 |      |      |
| CMIR                      | Input Voltage Range                            |                                                              | ±2    | ±2.5  |      | V    |
| IO                        | Linear Output Current <sup>(3)(4)</sup>        | V <sub>IN</sub> = 0 V                                        | +70   | ±80   |      | mA   |
|                           |                                                | V <sub>IN</sub> = 0 V, T <sub>A</sub> = -40°C to +85°C       | 40    | ±80   |      |      |
| ISC                       | Short Circuit Current <sup>(5)</sup>           | V <sub>IN</sub> = ±2 V, Output Shorted to Ground             |       | ±230  |      | mA   |
| XTLK                      | Channel to Channel Crosstalk                   | V <sub>IN</sub> = 2 V <sub>PP</sub> at 5 MHz                 |       | -90   |      | dBc  |
| XTLK                      | Channel to Channel Crosstalk                   | V <sub>IN</sub> = 2 V <sub>PP</sub> at 100 MHz               |       | -54   |      | dBc  |
| XTLK                      | All Hostile Crosstalk                          | In A, C, Out B, V <sub>IN</sub> = 2 V <sub>PP</sub> at 5 MHz |       | -95   |      | dBc  |

(5) The maximum output current ( $I_{OUT}$ ) is determined by the device power dissipation limitations. See the [Power Dissipation](#) section for more details. A short circuit condition should be limited to 5 seconds or less.

## 6.6 ±3.3V Electrical Characteristics

 $V_S = \pm 3.3\text{ V}$ ,  $R_L = 100\ \Omega$  (unless otherwise noted)

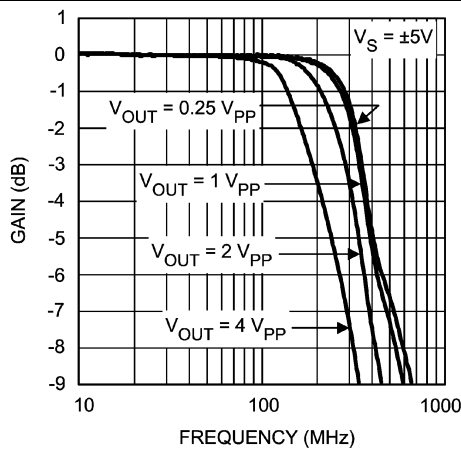
| PARAMETER                           |                                                | TEST CONDITIONS <sup>(1)</sup>                       | MIN | TYP       | MAX | UNIT                  |
|-------------------------------------|------------------------------------------------|------------------------------------------------------|-----|-----------|-----|-----------------------|
| <b>FREQUENCY DOMAIN PERFORMANCE</b> |                                                |                                                      |     |           |     |                       |
| SSBW                                | –3 dB Bandwidth                                | $V_{OUT} = 0.25\ V_{PP}$                             |     | 360       |     | MHz                   |
| LSBW                                | –3 dB Bandwidth                                | $V_{OUT} = 2.0\ V_{PP}$                              |     | 270       |     | MHz                   |
| 0.1 dBBW                            | 0.1 dB Bandwidth                               | $V_{OUT} = 0.5\ V_{PP}$                              |     | 80        |     | MHz                   |
| GFP                                 | Peaking                                        | DC to 200 MHz                                        |     | 0.3       |     | dB                    |
| DG                                  | Differential Gain                              | $R_L = 150\ \Omega$ , $f = 4.43\text{ MHz}$          |     | 0.02%     |     |                       |
| DP                                  | Differential Phase                             | $R_L = 150\ \Omega$ , $f = 4.43\text{ MHz}$          |     | 0.03      |     | deg                   |
| <b>TIME DOMAIN RESPONSE</b>         |                                                |                                                      |     |           |     |                       |
| TRL                                 | Rise and Fall Time                             | 2-V Step                                             |     | 2.0       |     | ns                    |
| TSS                                 | Settling Time to 0.05%                         | 2-V Step                                             |     | 15        |     | ns                    |
| OS                                  | Overshoot                                      | 2-V Step                                             |     | 5%        |     |                       |
| SR                                  | Slew Rate                                      | 2-V Step                                             |     | 1000      |     | V/ $\mu$ s            |
| <b>DISTORTION</b>                   |                                                |                                                      |     |           |     |                       |
| HD2                                 | 2 <sup>nd</sup> Harmonic Distortion            | 2 $V_{PP}$ , 10 MHz                                  |     | –70       |     | dBc                   |
| HD3                                 | 3 <sup>rd</sup> Harmonic Distortion            | 2 $V_{PP}$ , 10 MHz                                  |     | –74       |     | dBc                   |
| IMD                                 | 3 <sup>rd</sup> Order Intermodulation Products | 10 MHz, Two tones 2 $V_{PP}$ at Output               |     | –79       |     | dBc                   |
| <b>STATIC, DC PERFORMANCE</b>       |                                                |                                                      |     |           |     |                       |
| GAIN                                | Voltage Gain                                   |                                                      |     | 2.0       |     | V/V                   |
| VIO                                 | Output Offset Voltage                          | $V_{IN} = 0\text{ V}$                                |     | 1         |     | mV                    |
| DVIO                                | Average Drift                                  |                                                      |     | 36        |     | $\mu$ V/ $^{\circ}$ C |
| IBN                                 | Input Bias Current <sup>(2)</sup>              | $V_{IN} = 0\text{ V}$                                |     | 2         |     | $\mu$ A               |
| DIBN                                | Average Drift                                  |                                                      |     | 24        |     | nA/ $^{\circ}$ C      |
| PSRR                                | Power Supply Rejection Ratio                   | DC, Input Referred                                   |     | 54        |     | dB                    |
| ICC                                 | Supply Current                                 | $R_L = \infty$                                       |     | 20        |     | mA                    |
| VIH                                 | Logic High Threshold                           | Select and Enable Pins                               |     |           | 1.3 | V                     |
| VIL                                 | Logic Low Threshold                            | Select and Enable Pins                               | 0.4 |           |     | V                     |
| <b>MISCELLANEOUS PERFORMANCE</b>    |                                                |                                                      |     |           |     |                       |
| RIN+                                | Input Resistance                               |                                                      |     | 100       |     | k $\Omega$            |
| CIN                                 | Input Capacitance                              |                                                      |     | 0.9       |     | pF                    |
| ROUT                                | Output Resistance                              |                                                      |     | 0.27      |     | $\Omega$              |
| VO                                  | Output Voltage Range                           | No Load                                              |     | $\pm 2.5$ |     | V                     |
| VOL                                 |                                                | $R_L = 100\ \Omega$                                  |     | $\pm 2.2$ |     | V                     |
| CMIR                                | Input Voltage Range                            |                                                      |     | $\pm 1.2$ |     | V                     |
| IO                                  | Linear Output Current                          | $V_{IN} = 0\text{ V}$                                |     | $\pm 60$  |     | mA                    |
| ISC                                 | Short Circuit Current                          | $V_{IN} = \pm 1\text{ V}$ , Output Shorted to Ground |     | $\pm 150$ |     | mA                    |
| XTLK                                | Channel to Channel Crosstalk                   | 5 MHz                                                |     | –90       |     | dBc                   |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self heating where  $T_J > T_A$ . See the [Power Dissipation](#) section for information on temperature de-rating of this device. Minimum and maximum ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

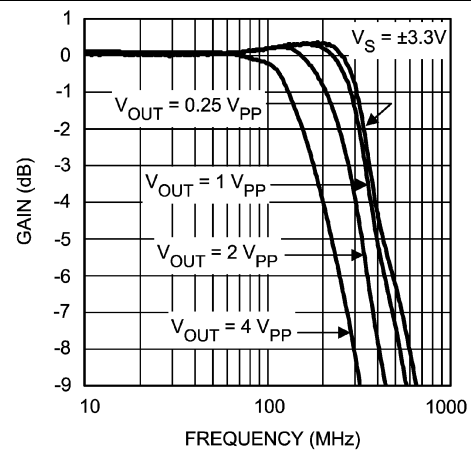
(2) Positive Value is current into device.

## 6.7 Typical Characteristics

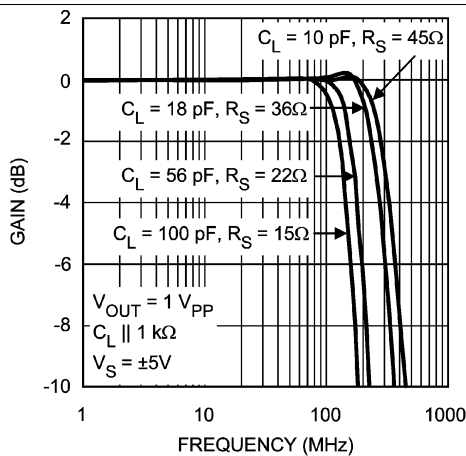
$V_S = \pm 5\text{ V}$  and  $R_L = 100\ \Omega$  (unless otherwise noted)



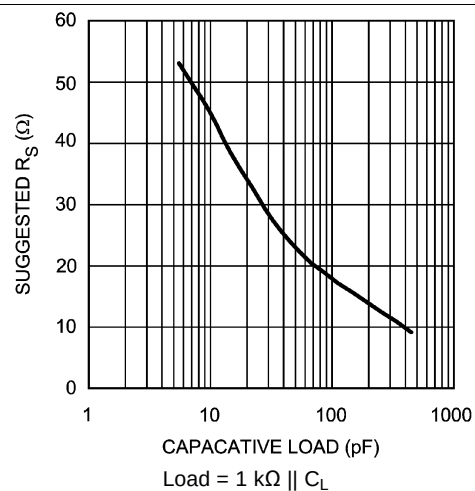
**Figure 1. Frequency Response vs  $V_{OUT}$**



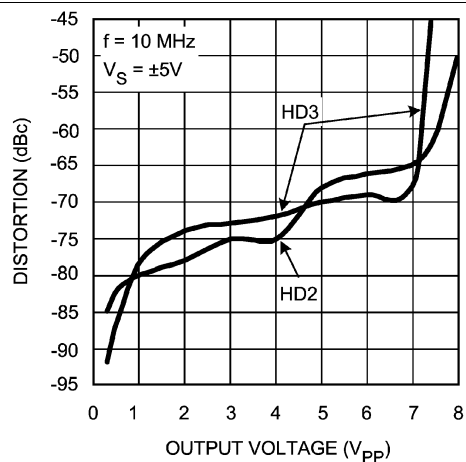
**Figure 2. Frequency Response vs  $V_{OUT}$**



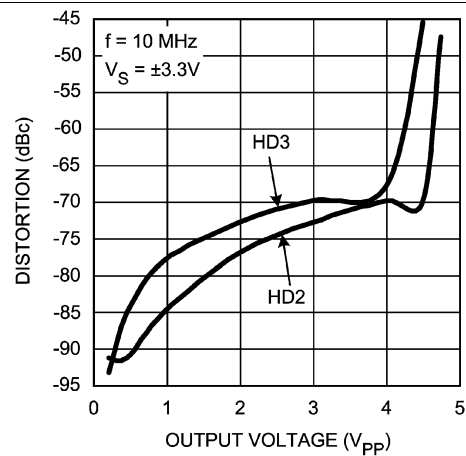
**Figure 3. Frequency Response vs Capacitive Load**



**Figure 4. Suggested  $R_S$  vs Capacitive Load**



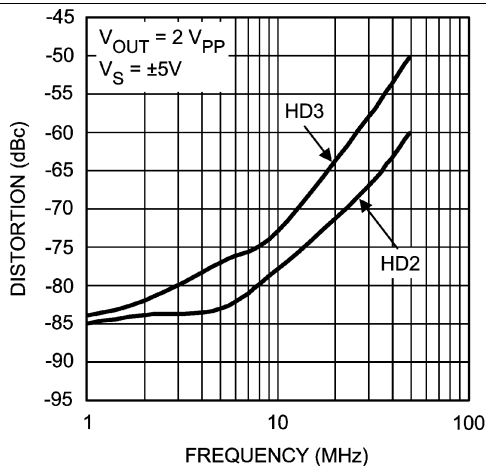
**Figure 5. Harmonic Distortion vs Output Voltage**



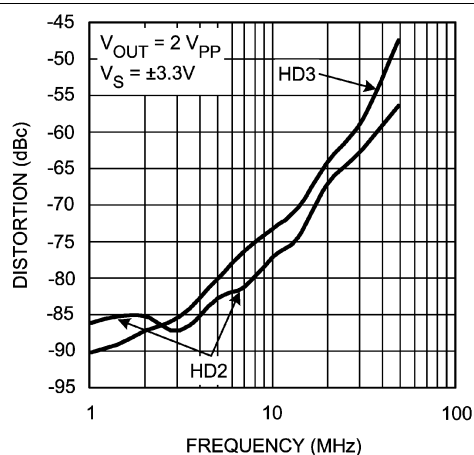
**Figure 6. Harmonic Distortion vs Output Voltage**

## Typical Characteristics (continued)

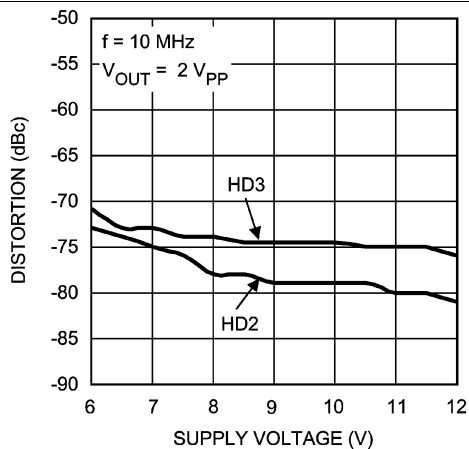
$V_S = \pm 5\text{ V}$  and  $R_L = 100\ \Omega$  (unless otherwise noted)



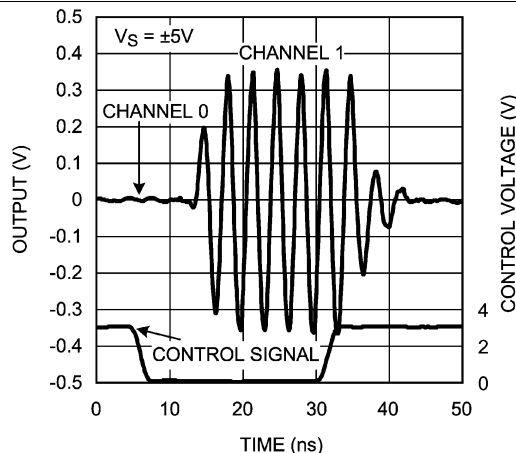
**Figure 7. Harmonic Distortion vs Frequency**



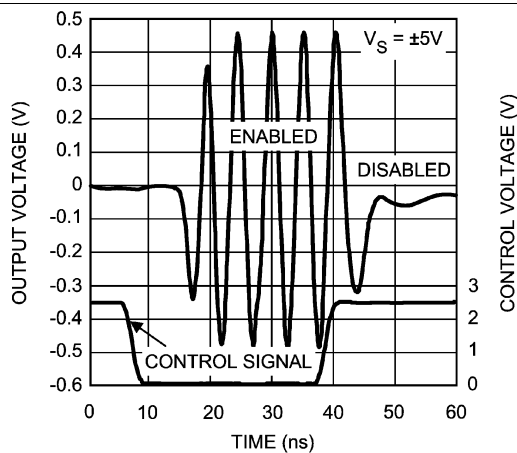
**Figure 8. Harmonic Distortion vs Frequency**



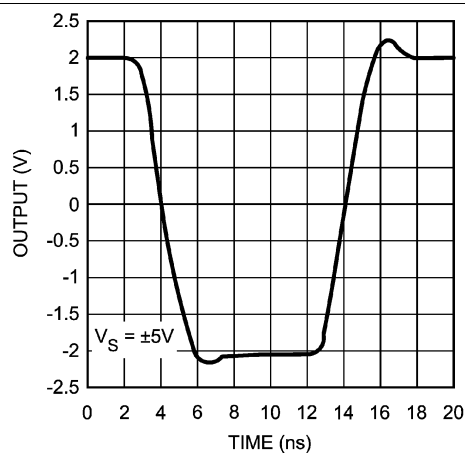
**Figure 9. Harmonic Distortion vs Supply Voltage**



**Figure 10. Channel Switching Time**



**Figure 11. Disable Time**



**Figure 12. Pulse Response**

## Typical Characteristics (continued)

$V_S = \pm 5\text{ V}$  and  $R_L = 100\ \Omega$  (unless otherwise noted)

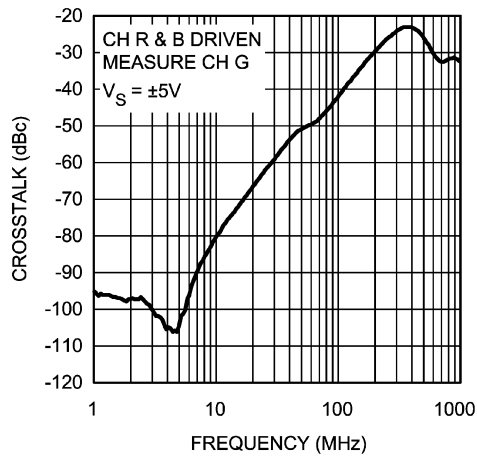


Figure 13. Crosstalk

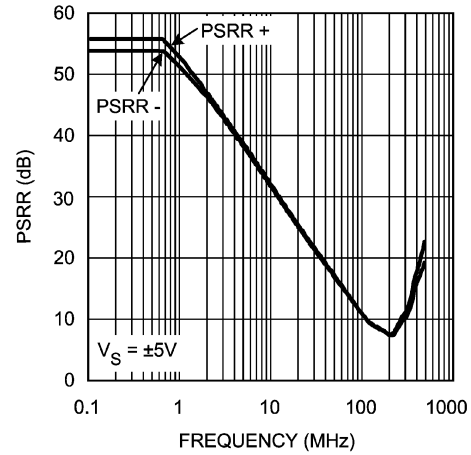


Figure 14. PSRR

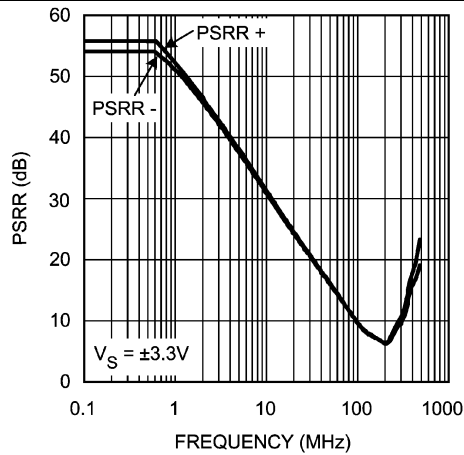


Figure 15. PSRR

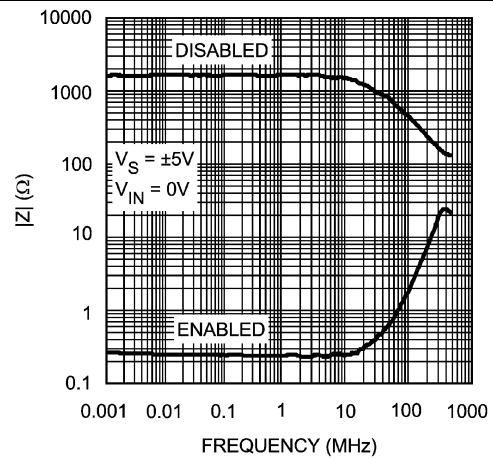


Figure 16. Closed-Loop Output Impedance

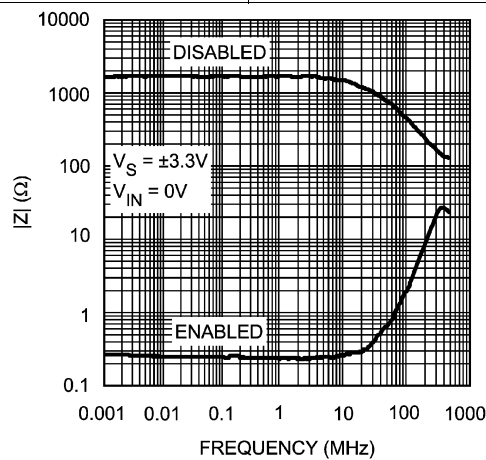


Figure 17. Closed-Loop Output Impedance

## 7 Detailed Description

### 7.1 Overview

The LMH6572 is a high-speed triple 2:1 analog multiplexer, optimized for very high speed and low distortion. With a fixed gain of 2 and excellent AC performance, the LMH6572 is ideally suited for switching high resolution, presentation grade video signals. The LMH6572 has no internal ground reference. Single or split supply configurations are both possible. The LMH6572 features very high speed channel switching and disable times. When disabled the LMH6572 output is high impedance, making multiplexer expansion possible by combining multiple devices.

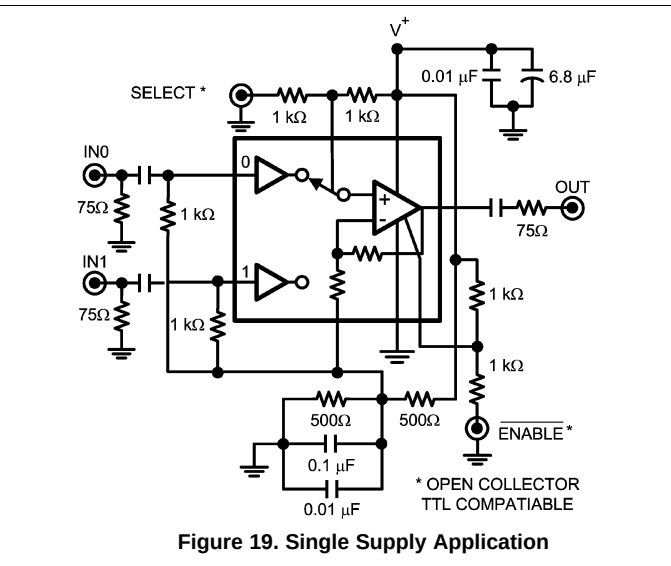
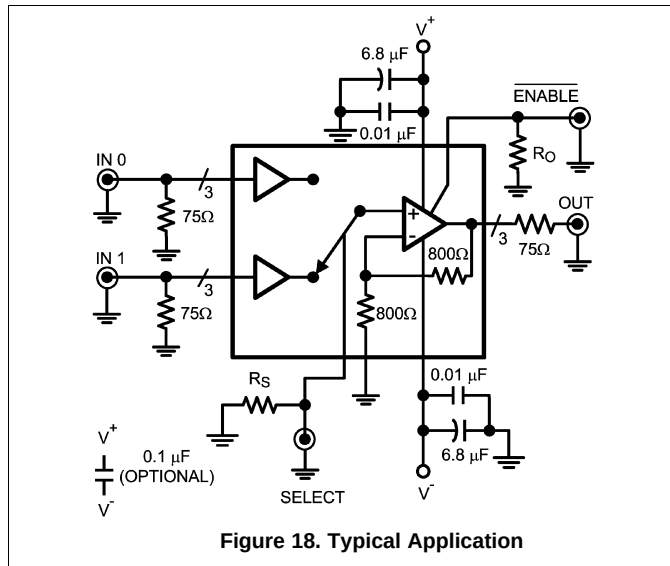
### 7.2 Feature Description

#### 7.2.1 Single Supply Operation

The LMH6572 uses mid-supply referenced circuits for the select and disable pins. In order to use the LMH6572 in single supply configuration, it is necessary to use a circuit similar to [Figure 19](#). In this configuration the logical inputs are compatible with high breakdown open collector TTL, or open drain CMOS logic. In addition, the default logic state is reversed since there is a pull-up resistor on those pins. Single supply operation also requires the input to be biased to within the common mode input range of roughly  $\pm 2V$  from the mid-supply point.

#### 7.2.2 Video Performance

The LMH6572 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. [Figure 18](#) shows a typical configuration for driving a 75- $\Omega$  cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.



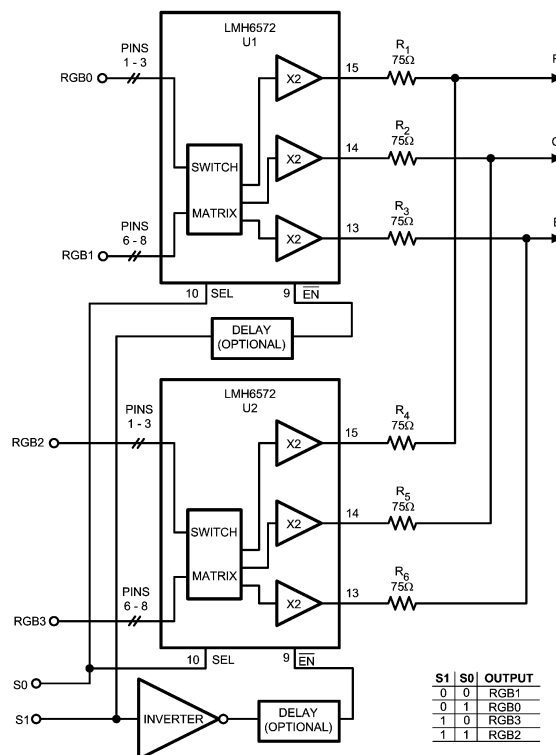
#### 7.2.3 Gain Accuracy

The gain accuracy of the LMH6572 is accurate to  $\pm 0.5\%$  (0.3% typical) and stable over temperature. The internal gain setting resistors, RF and RG, match very well; however, over process and temperature their absolute value will change.

## Feature Description (continued)

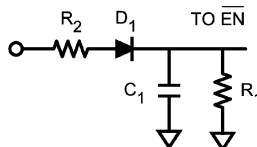
### 7.2.4 Expanding the Multiplexer

It is possible to build higher density multiplexers by paralleling several LMH6572s. Figure 20 shows a 4:1 RGB MUX using two LMH6572s:



**Figure 20. RGB MUX Using Two LMH6572's**

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added prior to the  $\overline{\text{ENABLE}}(\text{EN})$  pin of each device, as shown. Figure 21 shows one possible approach to this delay circuit. The delay circuit shown will delay  $\text{ENABLE}$ 's H to L transitions ( $R_1$  and  $C_1$  decay) but will not delay its L to H transition.

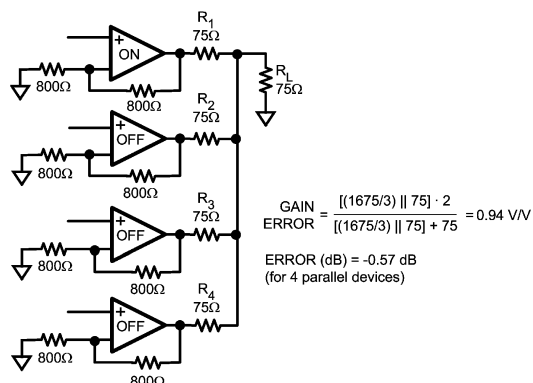


**Figure 21. Delay Circuit Implementation**

$R_2$  should be kept small compared to  $R_1$  in order to not reduce the  $\overline{\text{ENABLE}}$  voltage and to produce little or no delay to the  $\text{ENABLE}$  L to H transition.

With the  $\overline{\text{ENABLE}}$  pin putting the output stage into a high impedance state, several LMH6572's can be tied together to form a larger input MUX. However, there is a slight loading effect on the active output caused by the off-channel feedback and gain set resistors, as shown in Figure 21. Figure 22 is assuming there are four LMH6572 devices tied together to form a triple 8:1 MUX. With the internal resistors valued at approximately 800Ω, the gain error is about -0.57 dB, or about -6%.

## Feature Description (continued)



**Figure 22. Multiplexer Input Expansion by Combining Outputs**

An alternate approach would be to tie the outputs directly together and let all devices share a common back termination resistor in order to alleviate the gain error issue above.

The drawback in this case is the increased capacitive load presented to the output of each LMH6572 due to the offstate capacitance of the LMH6572.

## Feature Description (continued)

### 7.2.5 Other Applications

The LMH6572 may be utilized in systems that involve a single RGB channel as well whenever there is a need to switch between different “flavors” of a single RGB input.

Here are some examples:

1. RGB positive polarity, negative polarity switch
2. RGB full resolution, high-pass filter switch

In each of these applications, the same RGB input occupies one set of inputs to the LMH6572 and the other “flavor” would be tied to the other input set.

#### 7.2.5.1 Driving Capacitive Loads

Capacitive output loading applications will benefit from the use of a series output resistor. Figure 23 shows the use of a series output resistor,  $R_{OUT}$ , to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Figure 24 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of  $R_{OUT}$  can be reduced slightly from the recommended values.

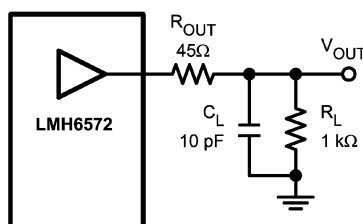


Figure 23. Decoupling Capacitive Loads

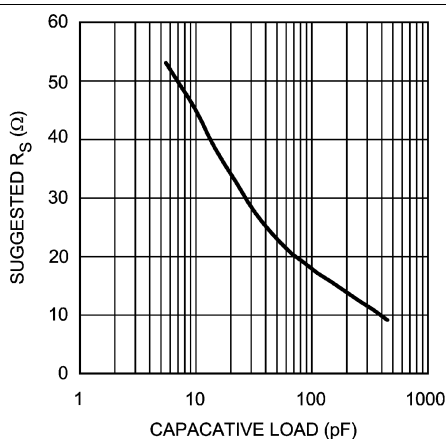


Figure 24. Recommended  $R_{OUT}$  vs Capacitive Load

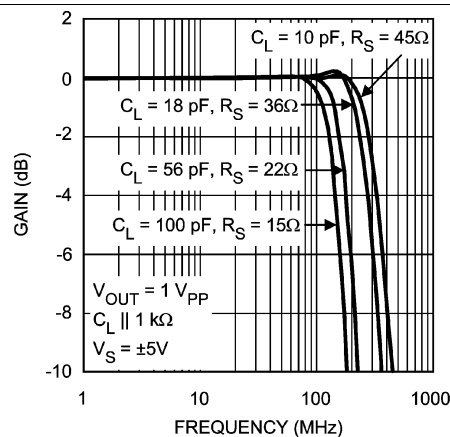


Figure 25. Frequency Response vs Capacitive Load

## 8 Power Supply Recommendations

### 8.1 Power Dissipation

The LMH6572 is optimized for maximum speed and performance in the small form factor of the standard SSOP package. To achieve its high level of performance, the LMH6572 consumes 23 mA of quiescent current, which cannot be neglected when considering the total package power dissipation limit. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the  $T_{JMAX}$  is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6572:

1. Calculate the quiescent (no-load) power:

$$P_{AMP} = I_{CC} * (V_S)$$

where

- $V_S = V^+ - V^-$  (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D (rms) = rms [(V_S - V_{OUT}) * I_{OUT}]$$

where

- $V_{OUT}$  and  $I_{OUT}$  are the voltage across and the current through the external load
- $V_S$  is the total supply voltage (2)

3. Calculate the total RMS power:

$$P_T = P_{AMP} + P_D \quad (3)$$

The maximum power that the LMH6572 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150^\circ\text{C} - T_{AMB}) / \theta_{JA}$$

where

- $T_{AMB}$  = Ambient temperature ( $^\circ\text{C}$ )
- $\theta_{JA}$  = Thermal resistance, from junction to ambient, for a given package ( $^\circ\text{C}/\text{W}$ )
- For the SSOP package  $\theta_{JA}$  is 125  $^\circ\text{C}/\text{W}$  (4)

### 8.2 ESD Protection

The LMH6572 is protected against electrostatic discharge (ESD) on all pins. The LMH6572 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6572 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

## 9 Layout

### 9.1 Layout Guidelines

Whenever questions about layout arise, use the LMH730151 evaluation board as a guide. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device; however, the smaller ceramic capacitors should be placed as close to the device as possible. In [Figure 18](#) and [Figure 19](#), the capacitor between  $V^+$  and  $V^-$  is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$  ceramic capacitors for each supply bypass.

#### 9.1.1 Evaluation Boards

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

| DEVICE  | PACKAGE | EVALUATION BOARD PART NUMBER |
|---------|---------|------------------------------|
| LMH6572 | SSOP    | LMH730151                    |

An evaluation board can be shipped when a device sample request is placed with Texas Instruments.

## 10 Device and Documentation Support

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 10.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LMH6572MQ/NOPB</a>  | Active        | Production           | SSOP (DBQ)   16 | 95   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LH65<br>72MQ        |
| LMH6572MQ/NOPB.A                | Active        | Production           | SSOP (DBQ)   16 | 95   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LH65<br>72MQ        |
| <a href="#">LMH6572MQX/NOPB</a> | Active        | Production           | SSOP (DBQ)   16 | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LH65<br>72MQ        |
| LMH6572MQX/NOPB.A               | Active        | Production           | SSOP (DBQ)   16 | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | LH65<br>72MQ        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

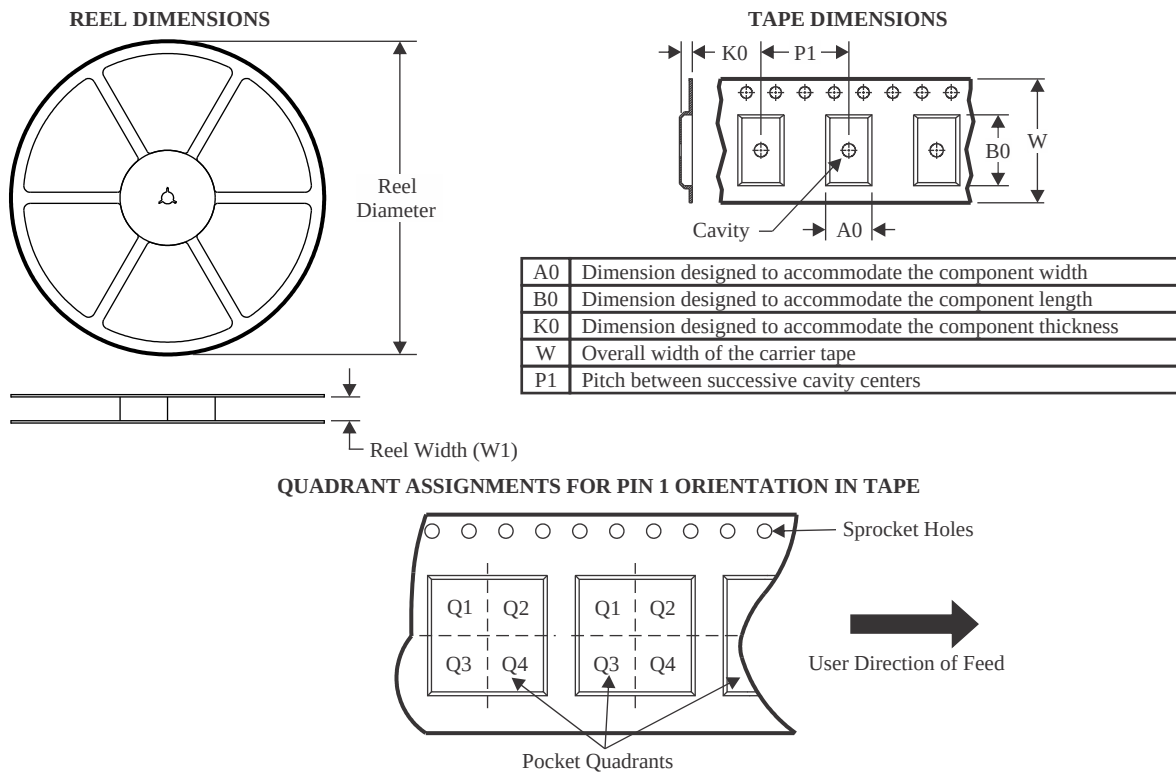
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



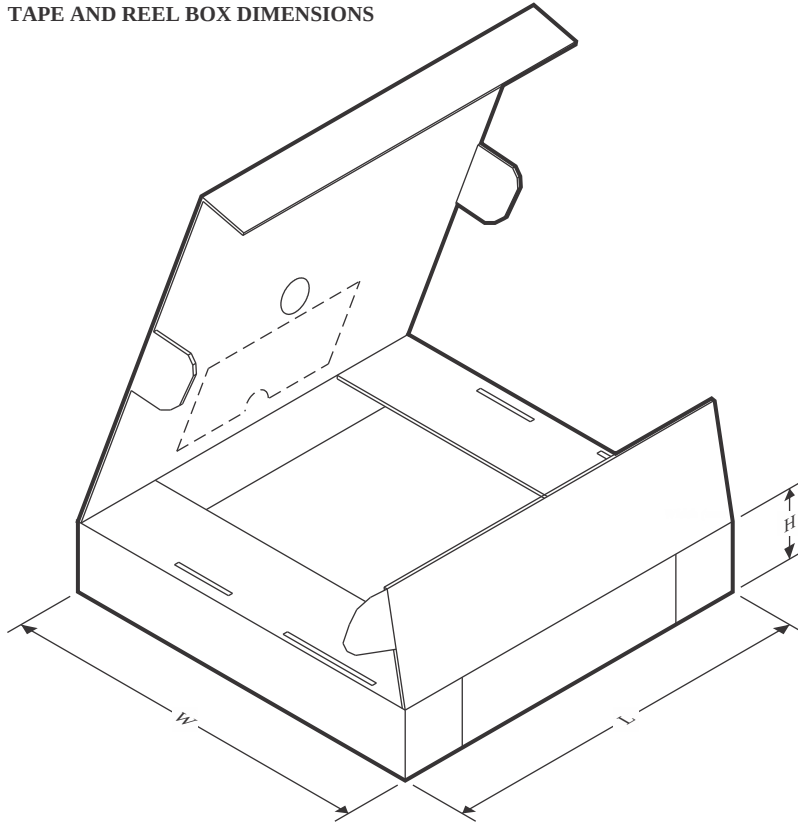
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMH6572MQX/NOPB | SSOP         | DBQ             | 16   | 2500 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |

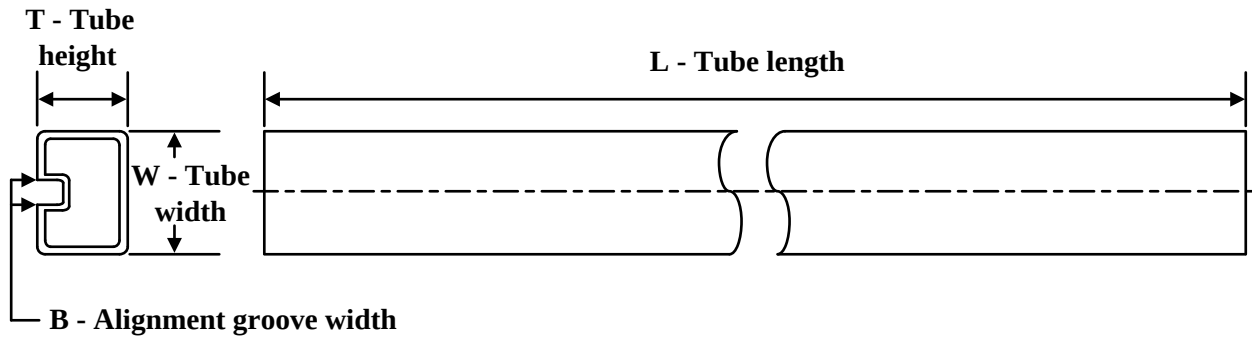
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

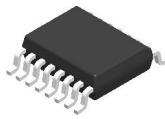
| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMH6572MQX/NOPB | SSOP         | DBQ             | 16   | 2500 | 367.0       | 367.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device           | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LMH6572MQ/NOPB   | DBQ          | SSOP         | 16   | 95  | 495    | 8      | 4064   | 3.05   |
| LMH6572MQ/NOPB.A | DBQ          | SSOP         | 16   | 95  | 495    | 8      | 4064   | 3.05   |

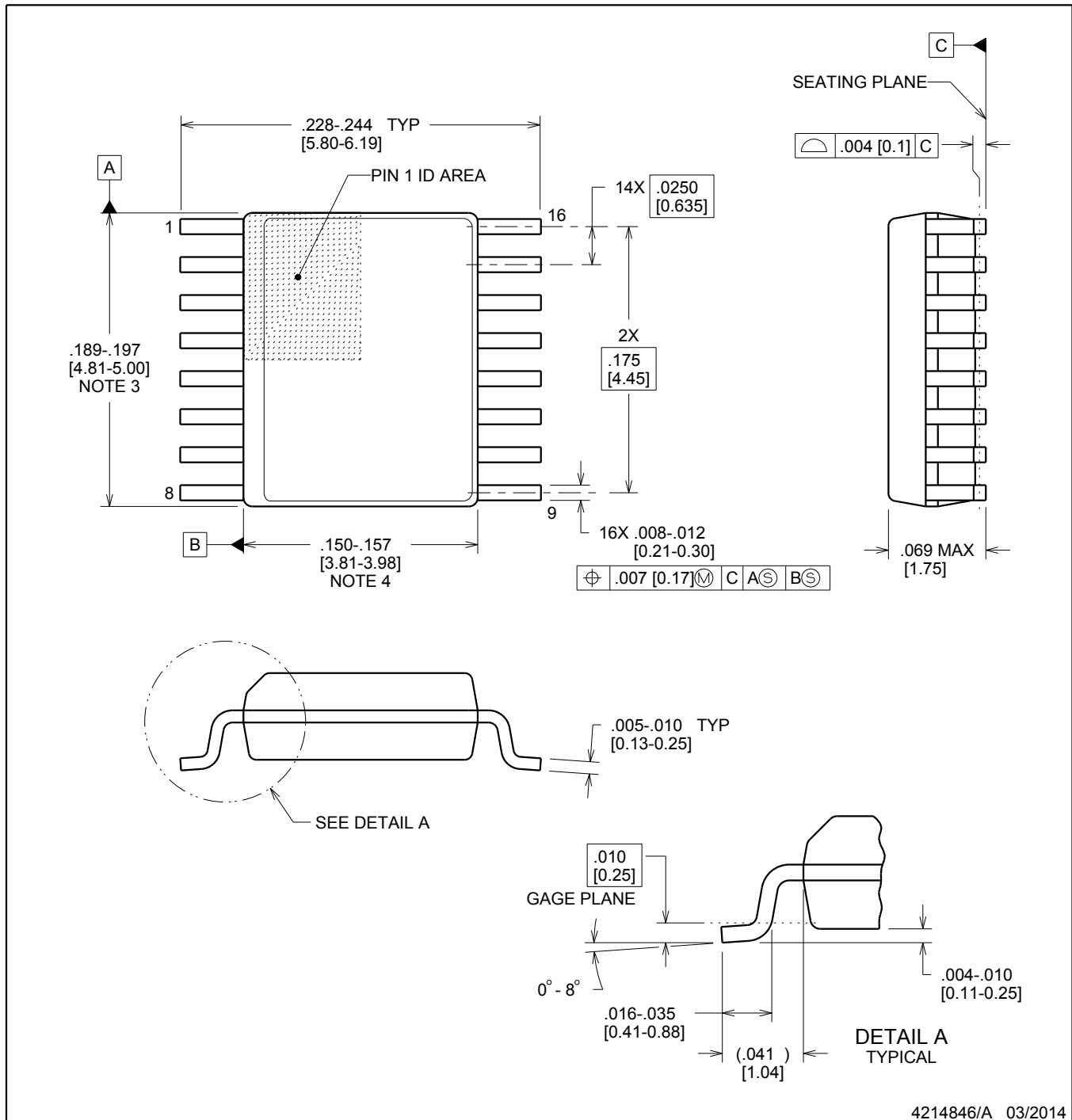


**DBQ0016A**

# PACKAGE OUTLINE

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

## NOTES:

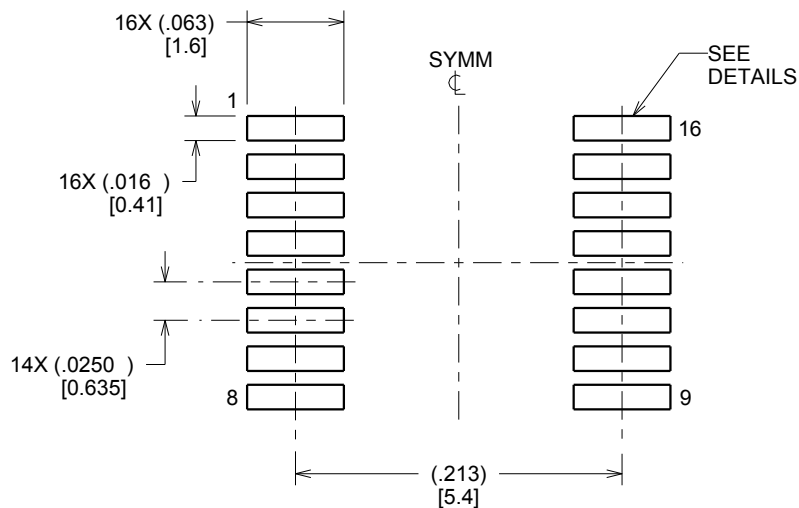
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

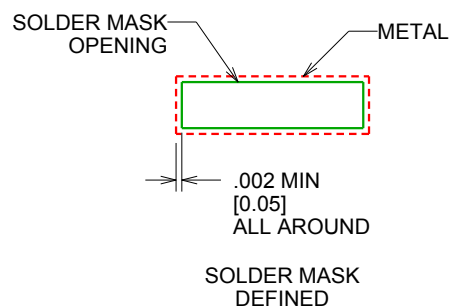
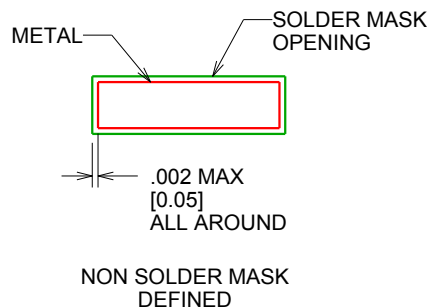
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

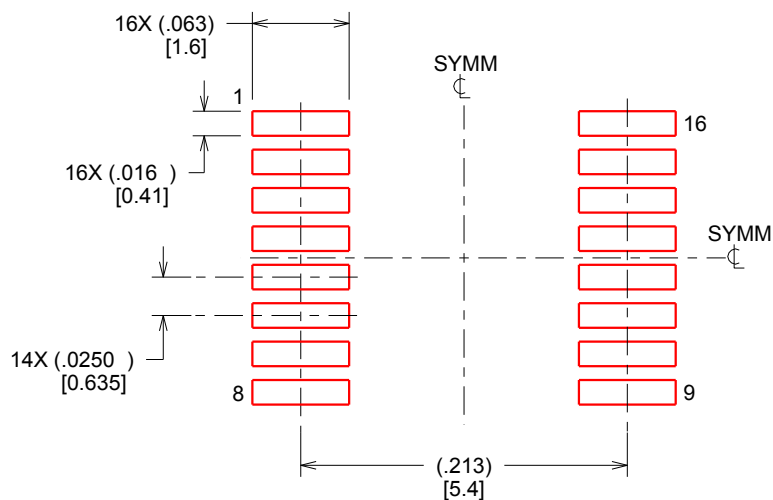
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated