SN74HCT08 Quadruple 2-Input Positive-AND Gates

1 Features

- Operating voltage range of 4.5V to 5.5V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 20μA max I_{CC}
- Typical t_{pd} = 13ns
- ±4mA output drive at 5V
- Low input current of 1μA max
- Inputs are TTL-voltage compatible

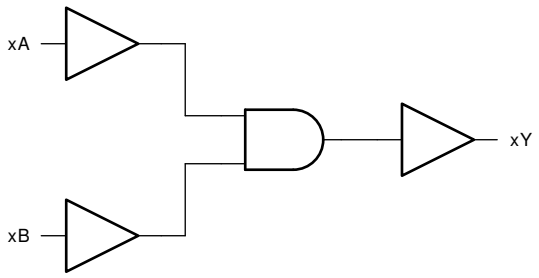
2 Description

These devices contain four independent 2-input AND gates. They perform the Boolean function Y = A • B in positive logic.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(2)
SN74HCT08	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	DB (SSOP, 14)	6.20mm × 7.8mm	6.20mm × 5.30 mm
	N (PDIP, 14)	19.30mm × 9.4mm	19.30mm × 6.35mm
	NS (SO, 4)	10.20mm × 7.8mm	10.20mm × 5.30mm
	PW (TSSOP, 14)	5.00mm × 6.4mm	5.00mm × 4.40mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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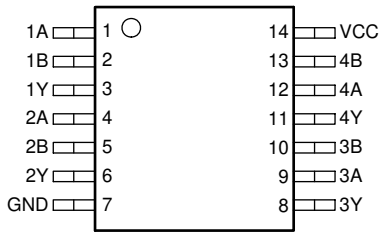
3 Pin Configuration and Functions



D, DB, J, N, NS, PW or W Package
14-Pin SOIC, SSOP, PDIP, SO or TSSOP
Top View

Table 3-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V_{CC}	14	—	Positive Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input clamp current [2]	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current [2]	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
V_{CC} or GND	Continuous current through			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			SN74HCT08			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
Δt/Δv	Input transition rise/fall time				500	ns
T_A	Operating free-air temperature		– 40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating SMOS Inputs, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC		D (SOIC) 14 PINS	DB (SSOP) 14 PINS	N (PDIP) 14 PINS	NS (SO) 14 PINS	PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [1]	138.7	114.8	103.8	129.3	157.6	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	93.8	60	91.6	85.7	84.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	63.8	83.5	89.9	100.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	49.1	19.7	71.1	48.2	27.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.3	63.1	83.4	89.4	100.2	°C/W
$R_{\theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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4.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V_{CC} (V)	T_A = 25°C			SN74HCT08		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –20 µA	4.5	4.4	4.499		4.4		V
		I_{OH} = –4 mA		3.98	4.3		3.84		
V_{OL}	Low-level output voltage	I_{OL} = 20 µA	4.5		0.001	0.1		0.1	V
		I_{OL} = 4 mA			0.17	0.26		0.33	
I_I	Input hold current	V_I = V_{CC} or 0	5.5		±0.1	±100		±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0. I_O = 0	5.5			2		20	µA
ΔI_{CC} [2]	Supply-current change	One input at 0.5V or 2.4 V, Other inputs at 0 or V_{CC}	5.5		1.4	2.4		2.9	mA
C_i	Input capacitance		4.5 to 5.5		3	10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

4.5 Switching Characteristics

C_L = 50 pF. See Parameter Measurement Information

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	T_A = 25°C			SN74HCT08		
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	Propagation delay	A or B	Y	4.5		15	24		30	ns
				5.5		13	22		27	
t_t	Transition time		Y	4.5		9	15		19	ns
				5.5		8	14		17	

4.6 Operating Characteristics

T_A = 25°C

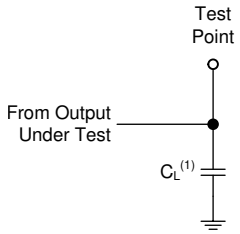
		Test Conditions	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

5 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 6ns.

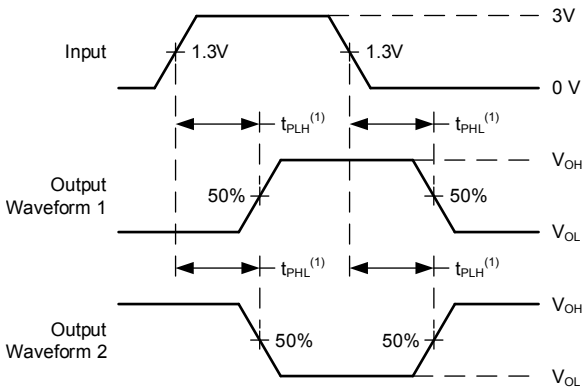
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 5-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 5-2. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

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6 Detailed Description

6.1 Overview

This device contains four independent 2-input AND Gates. Each gate performs the Boolean function Y = A ● B in positive logic.

6.2 Functional Block Diagram

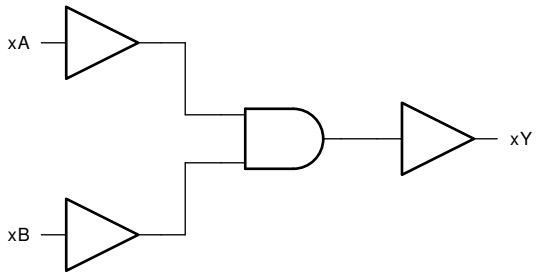

Figure 6-1. Functional Block Diagram

6.3 Device Functional Modes

Table 6-1 lists the functional modes of the SN74HCT08.

Table 6-1. Function Table

INPUTS[(1)]		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

7.2.2 Layout Example

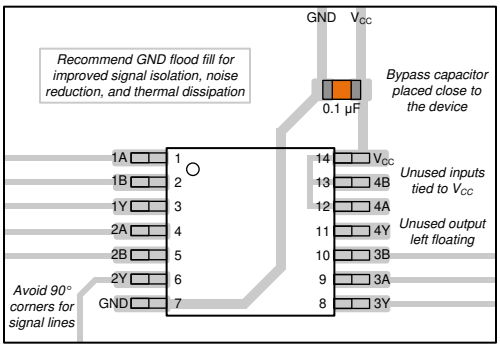

Figure 7-1. Example Layout for the SN74HCT08

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October 2022) to Revision G (August 2024)	Page
• Added package size to *Package Information* table	1
• Deleted references to preview-only GPN throughout data sheet	1
• Added *Pin Functions* table	3
• Updated RθJA values: N = 67 to 103.8, NS = 93.3 to 129.3, PW = 159.8 to 157.6; Updated N, NS, and PW packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W	4
• Added *Application and Implementation* section	8

Changes from Revision E (February 2022) to Revision F (October 2022)	Page
• Increased RθJA for packages: D (86 to 138.7); DB (96 to 114.8); N (80 to 67); NS (76 to 93.3); PW (113 to 159.8)	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCT08D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	HCT08
SN74HCT08DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT08
SN74HCT08DBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT08
SN74HCT08DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08DRE4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08DRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT08N
SN74HCT08N.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT08N
SN74HCT08NE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT08N
SN74HCT08NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08NSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT08
SN74HCT08PW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	HT08
SN74HCT08PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HT08
SN74HCT08PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT08
SN74HCT08PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT08
SN74HCT08PWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT08
SN74HCT08PWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 85	HT08

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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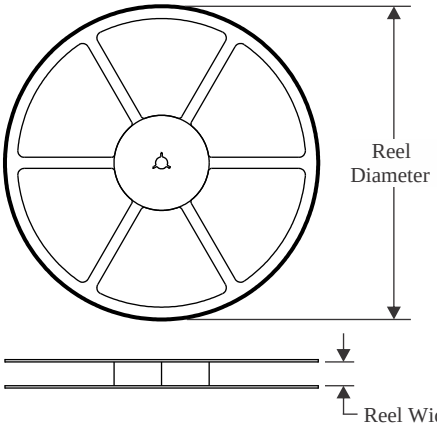
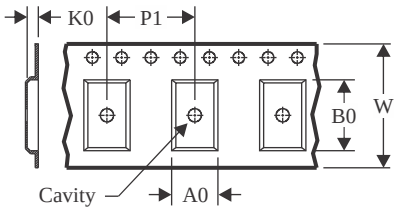
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

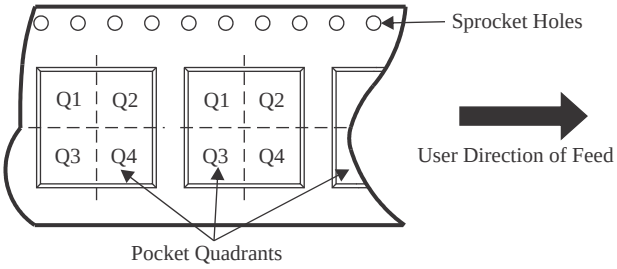


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

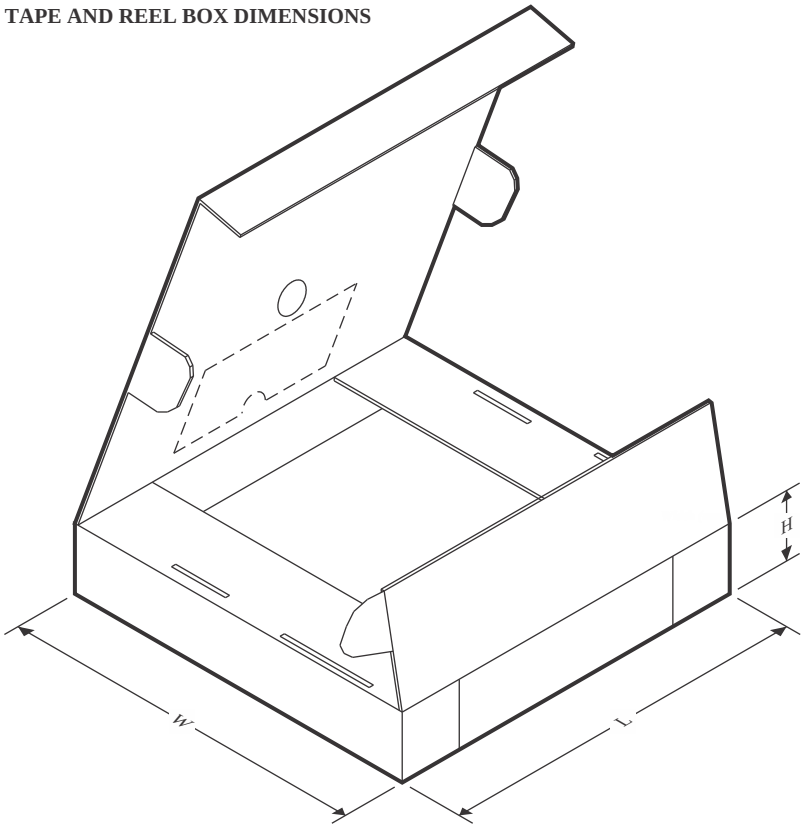
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HCT08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT08DRE4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT08DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT08NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HCT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74HCT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

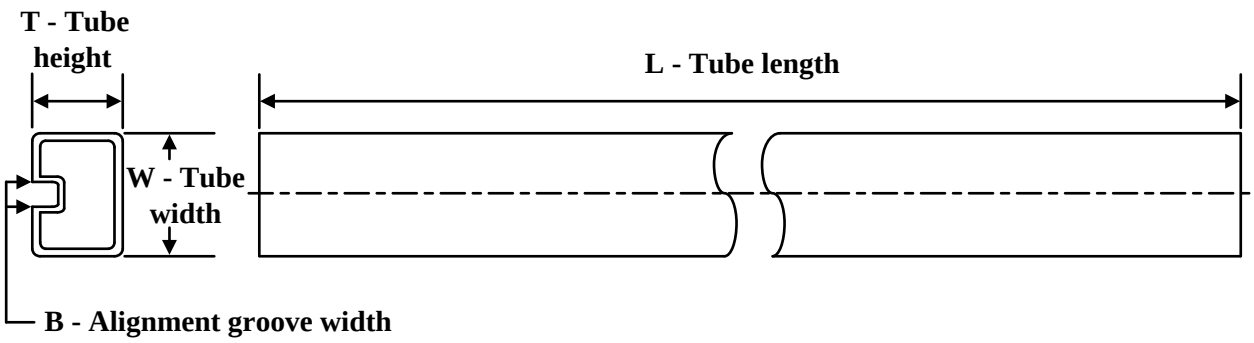
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

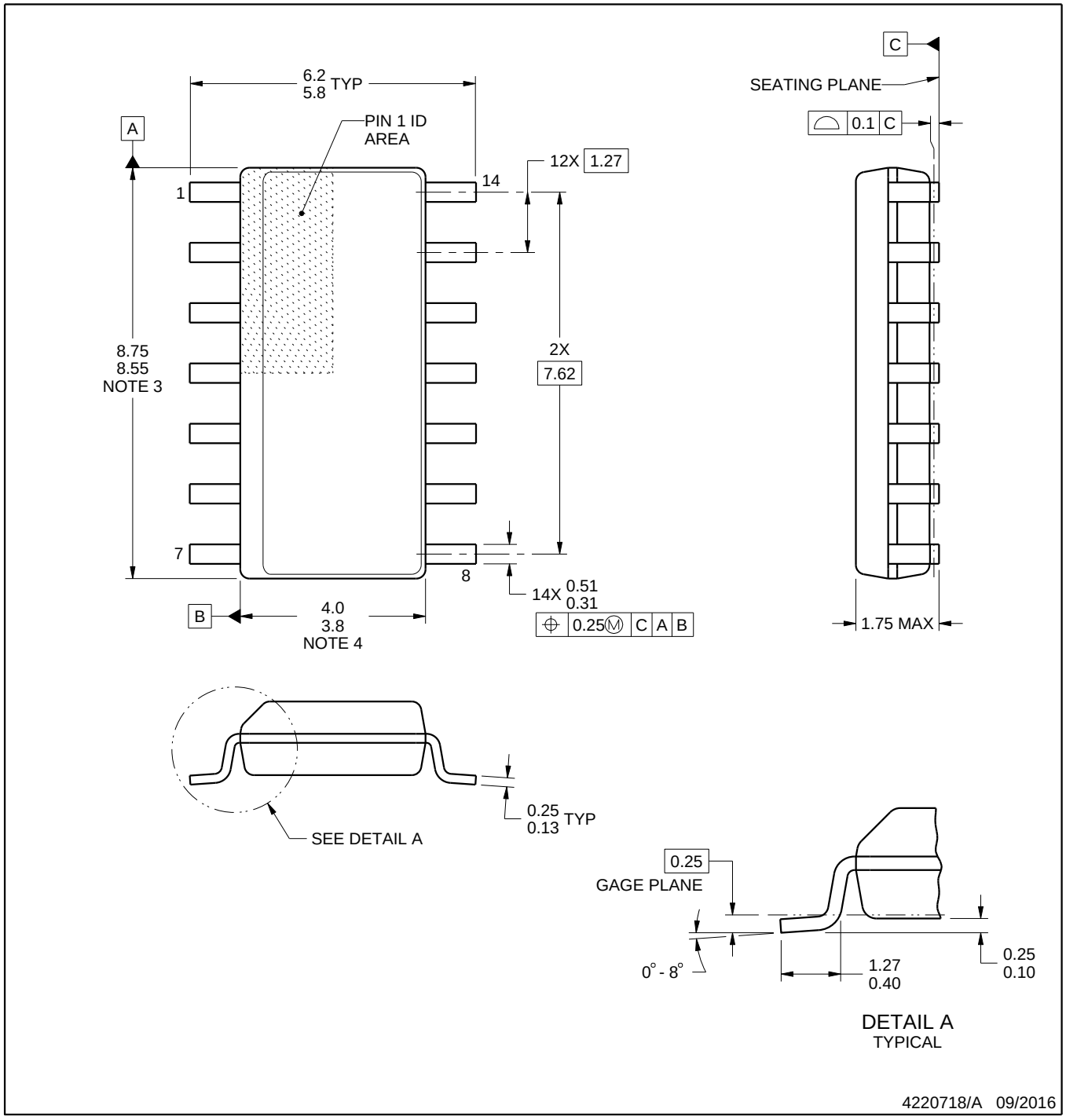
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT08DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74HCT08DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74HCT08DRE4	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCT08DRG4	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCT08NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74HCT08PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74HCT08PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT08PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT08PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT08PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



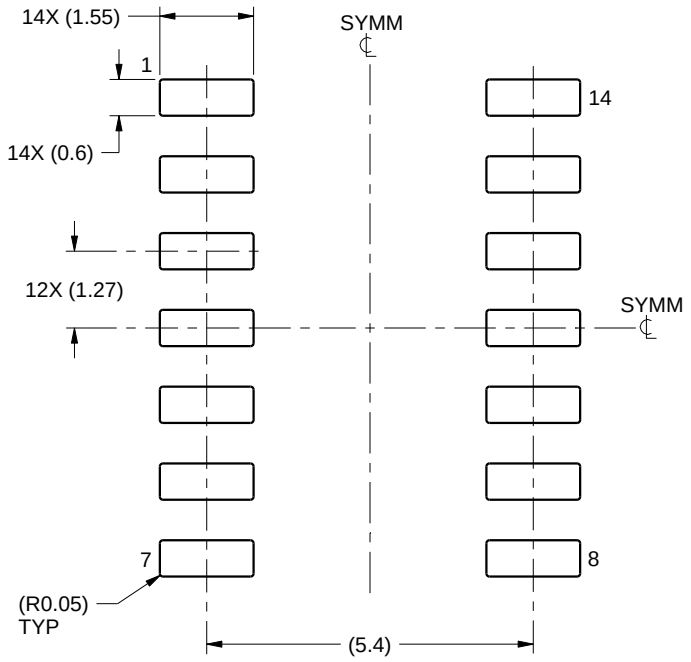
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HCT08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT08N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT08N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT08NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT08NE4	N	PDIP	14	25	506	13.97	11230	4.32

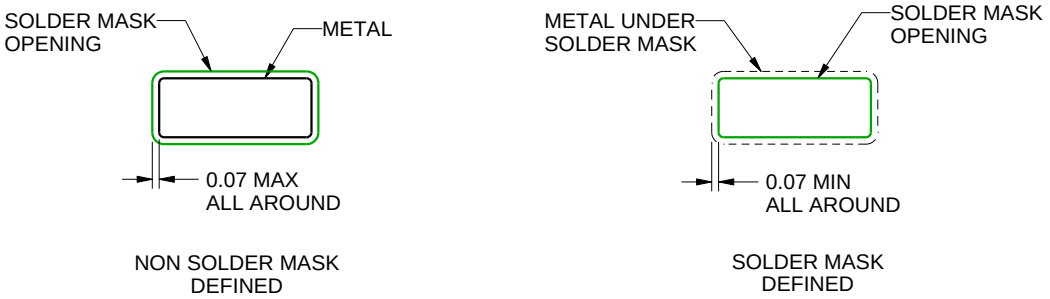


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

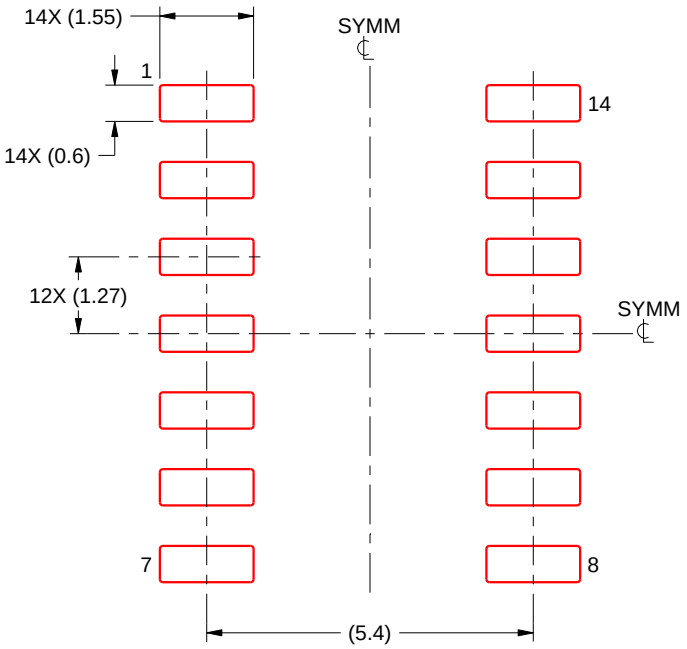


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

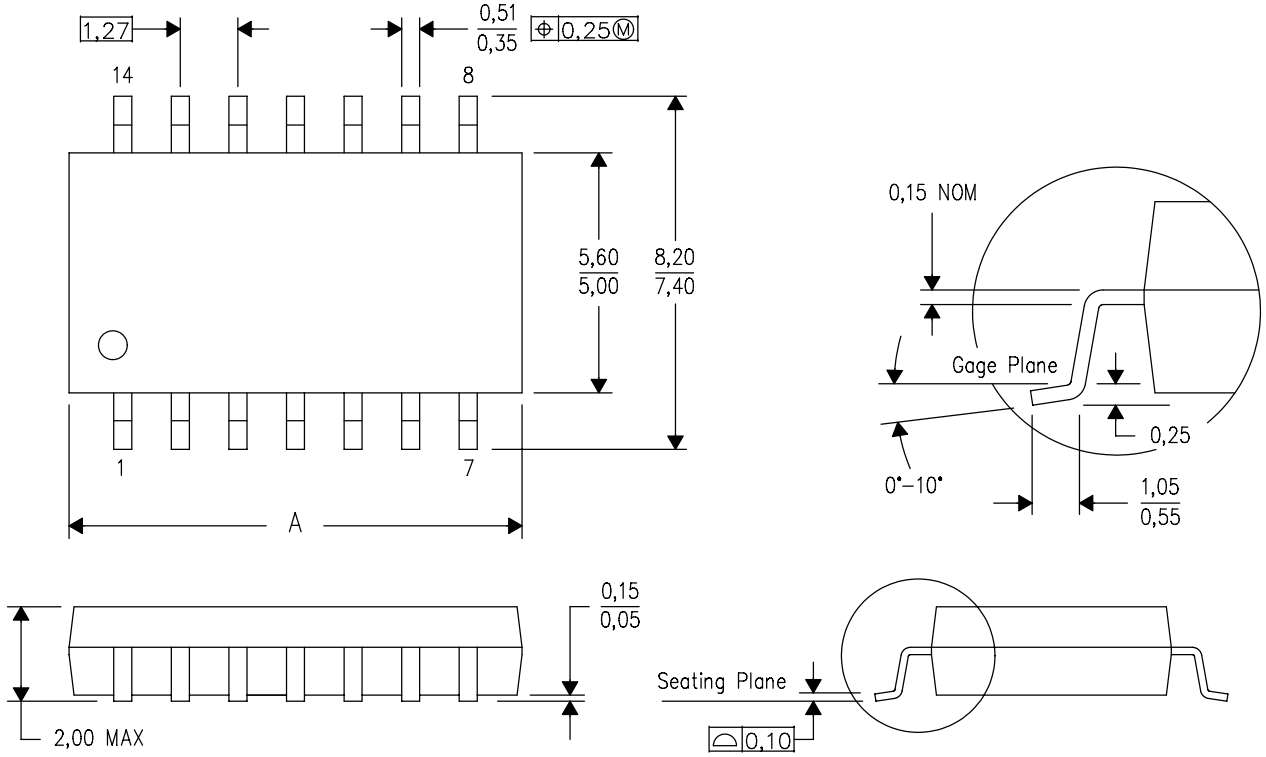
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

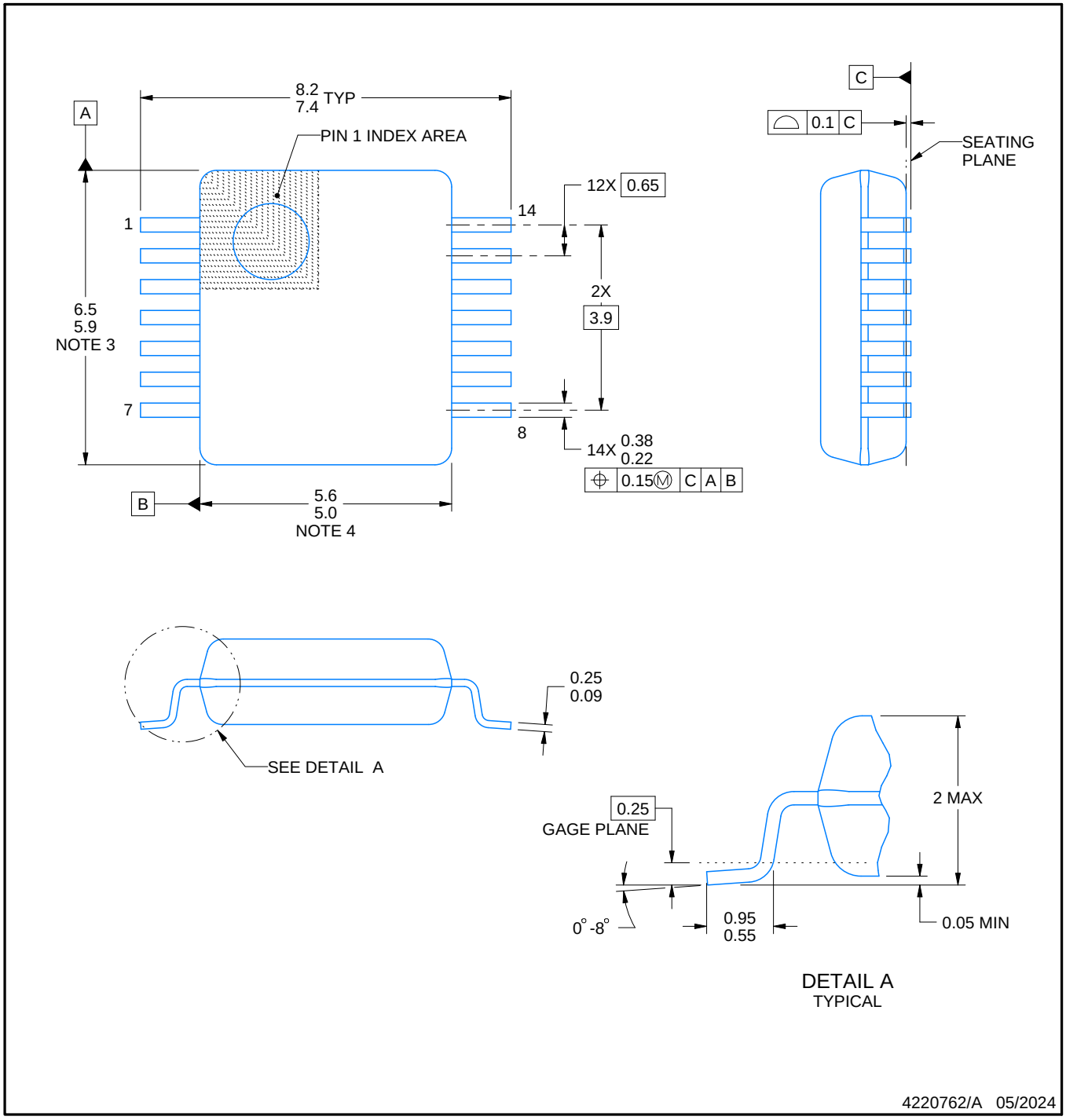
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

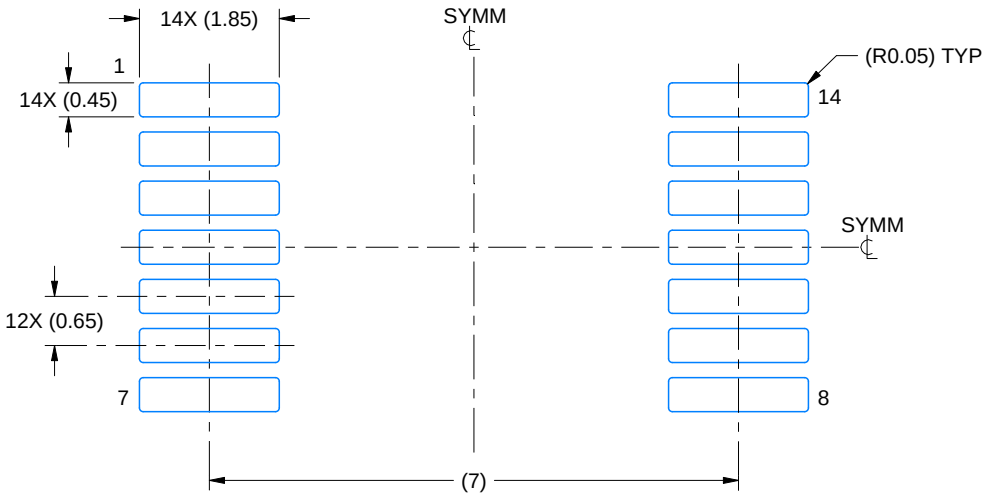
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

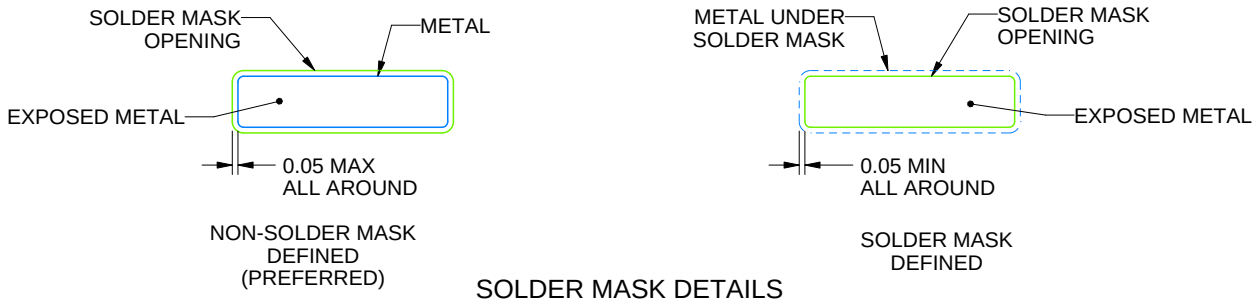


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

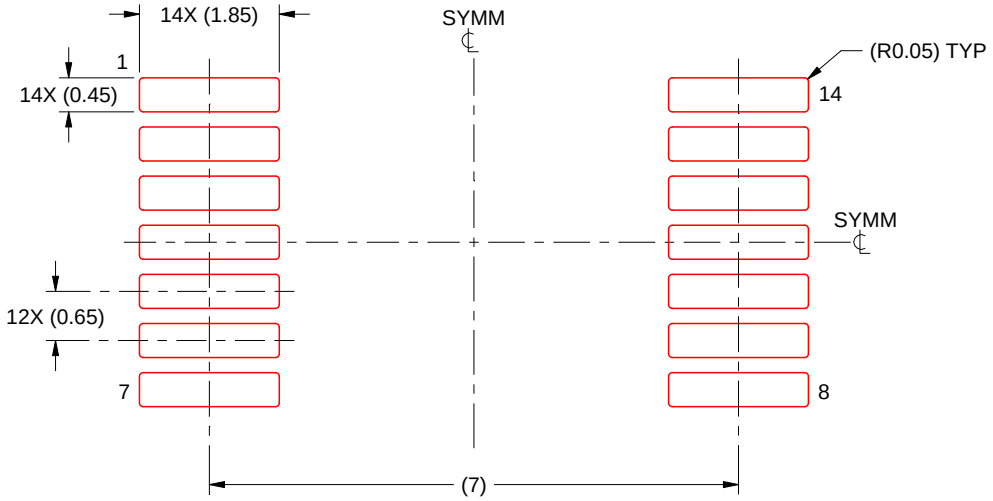


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

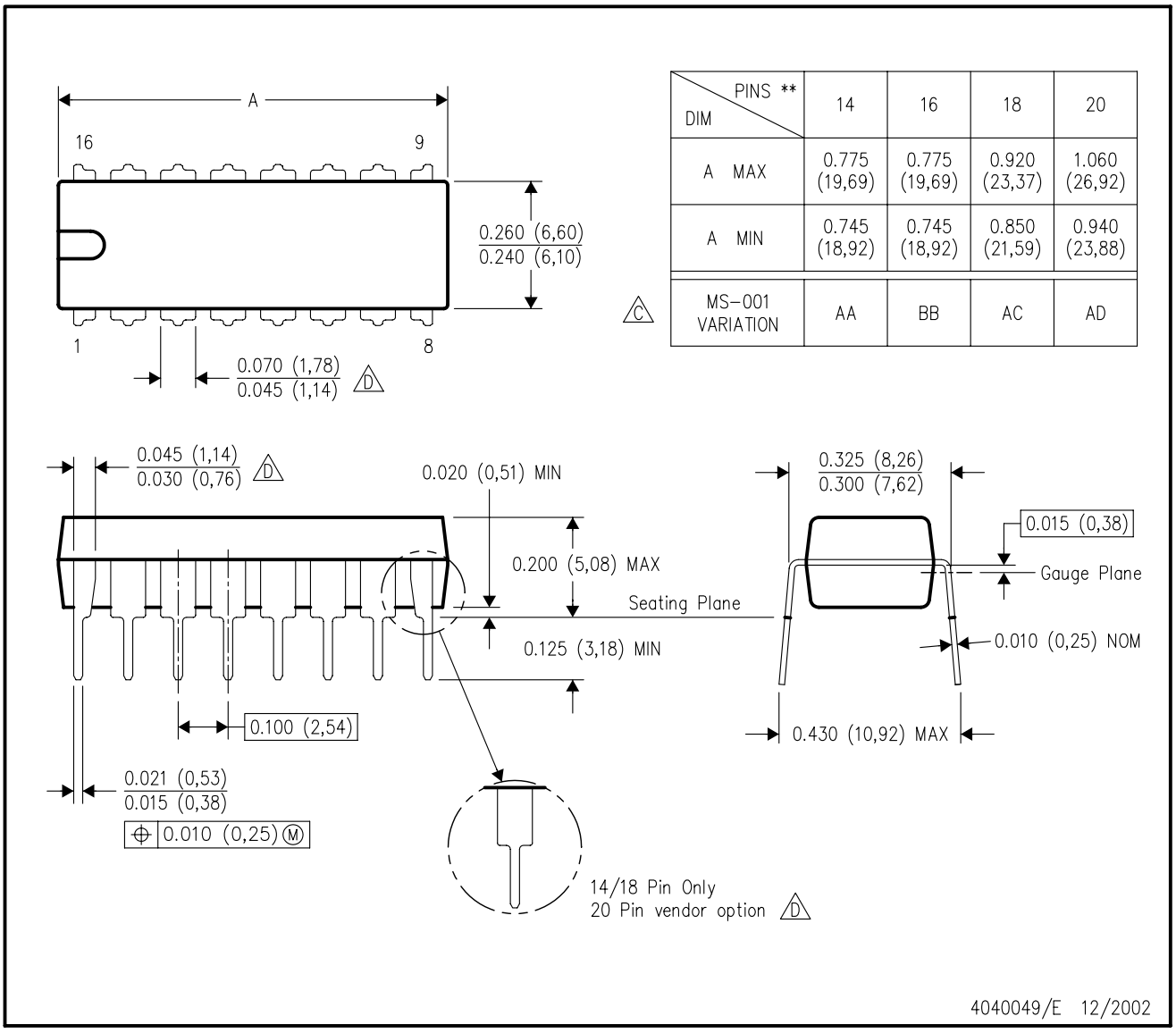
4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

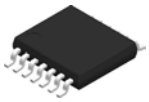
16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

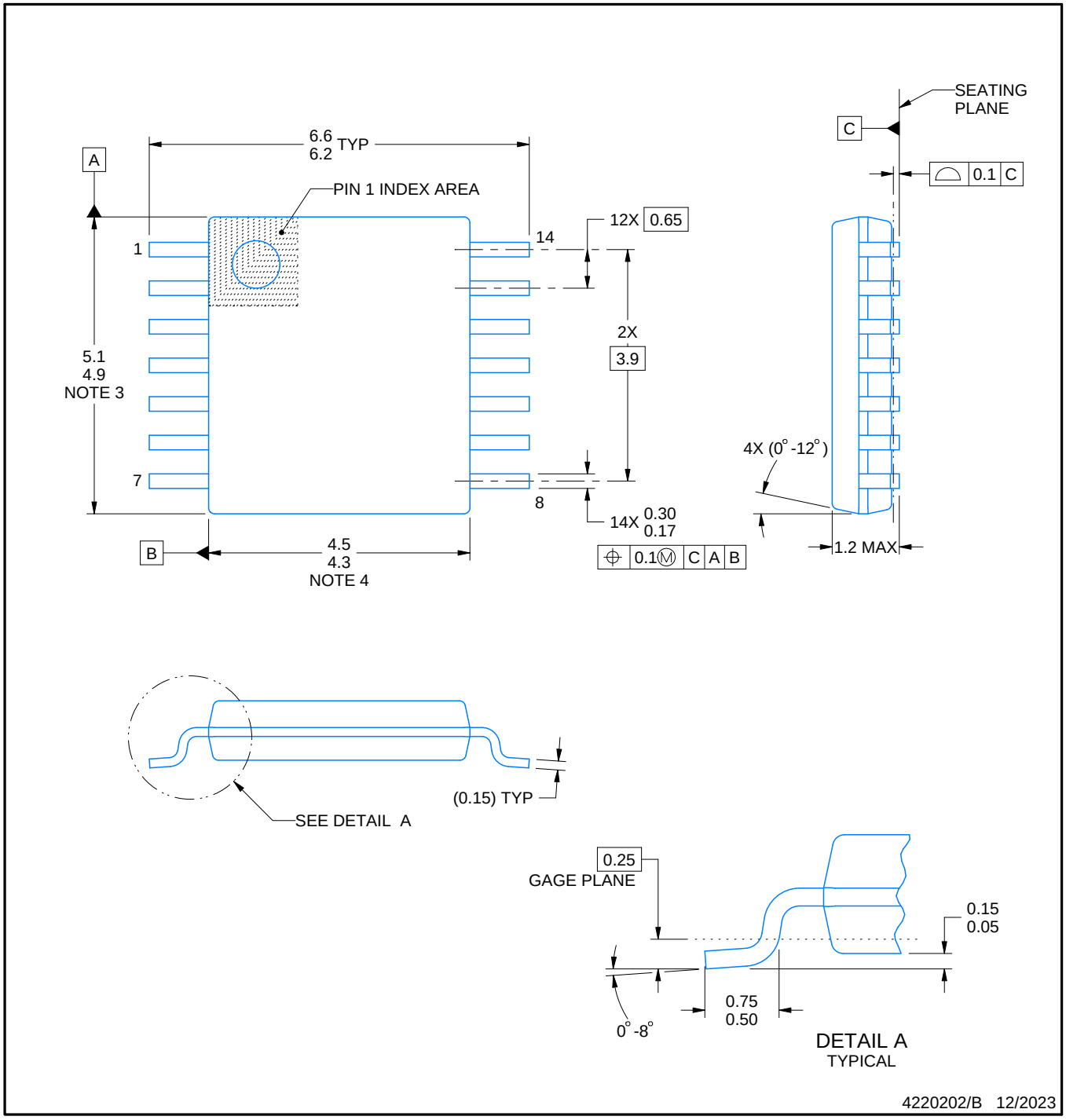
PW0014A



PACKAGE OUTLINE

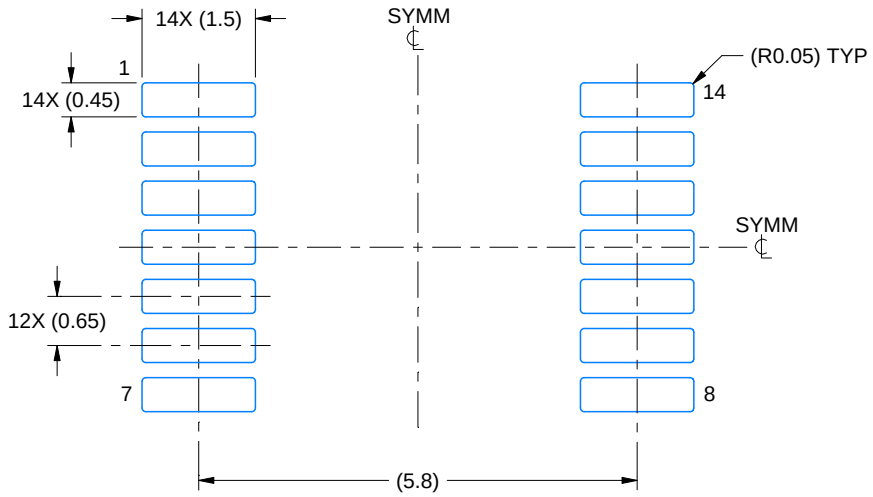
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

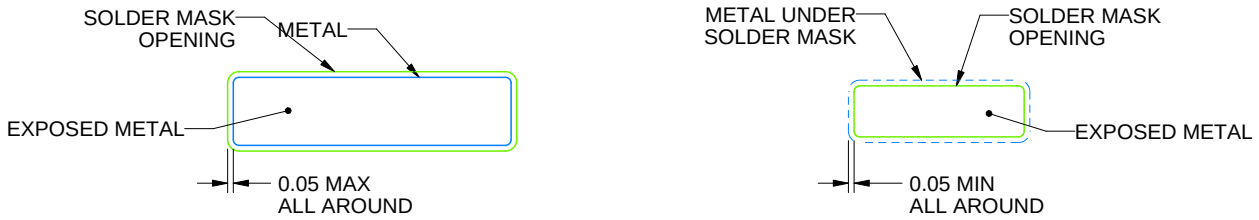


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

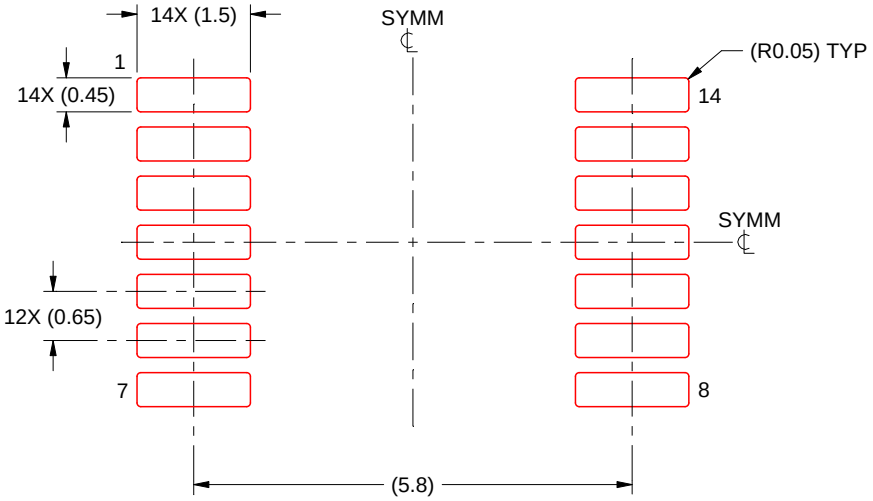
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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