LM5032 High-Voltage Dual Interleaved Current Mode Controller

1 Features

- Two Independent PWM Current Mode Controllers
- Integrated High-Voltage Startup Regulator
- Compound 2.5-A Main Output Gate Drivers
- Single Resistor Oscillator Setting to 2 MHz
- Synchronizable Oscillator
- Programmable Maximum Duty Cycle
- Maximum Duty Cycle Fold-Back at High-Line Voltage
- Adjustable Timer for Hiccup Mode Current Limiting
- Integrated Slope Compensation
- Adjustable Line Undervoltage Lockout
- Independently Adjustable Soft-Start (Each Regulator)
- Direct Interface with Opto-Coupler Transistor
- Thermal Shutdown
- TSSOP 16-Pin Package

2 Applications

- Telecommunication Power Converters
- Industrial Power Converters
- 42-V Automotive Systems

3 Description

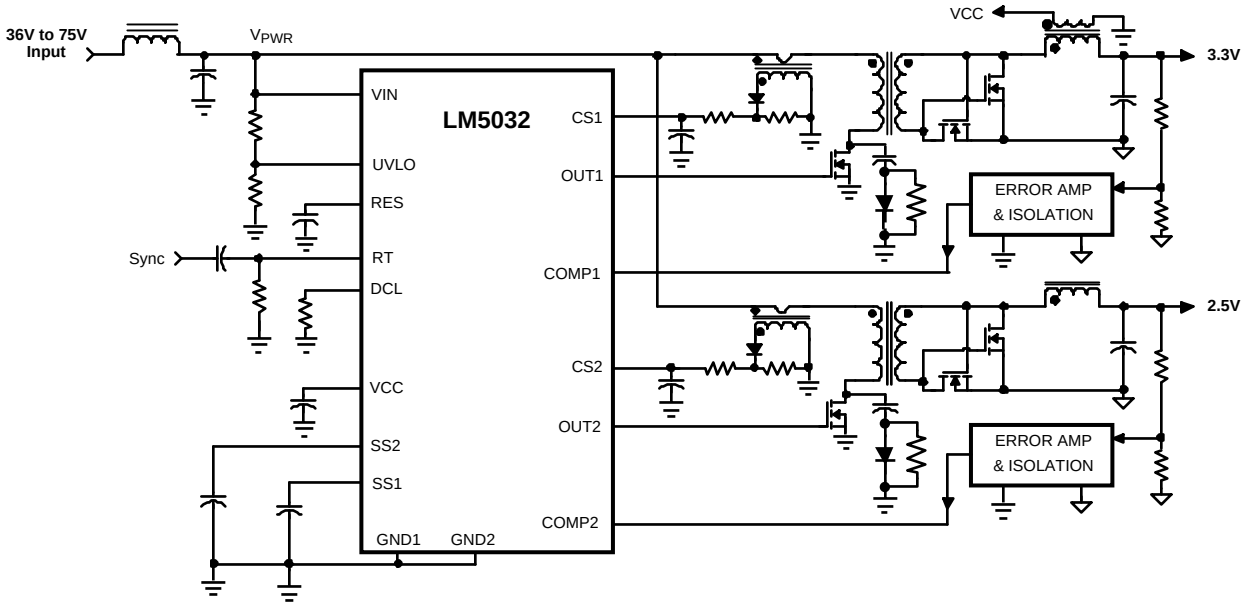
The LM5032 dual current mode PWM controller contains all the features needed to control either two independent forward dc/dc converters or a single high current converter comprised of two interleaved power stages. The two controller channels operate 180° out of phase thereby reducing input ripple current. The LM5032 includes a startup regulator that operates over a wide input range up to 100 V and compound (bipolar + CMOS) gate drivers that provide a robust 2.5-A peak sink current. The adjustable maximum PWM duty cycle reduce stress on the primary side MOSFET switches. Additional features include programmable line undervoltage lockout, cycle-by-cycle current limit, hiccup mode fault operation with adjustable response time, PWM slope compensation, soft-start, and a 2-MHz capable oscillator with synchronization capability.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5032	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2013) to Revision B — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (April 2013) to Revision A — **Page**

- Changed layout of National Data Sheet to TI format ... 27

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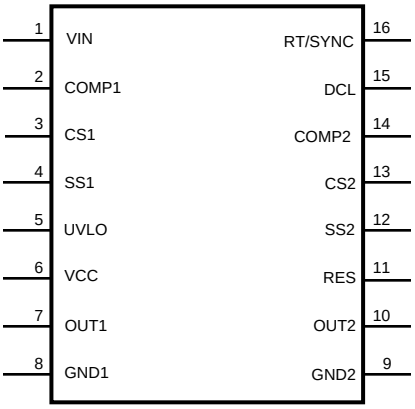
5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION	APPLICATIONS INFORMATION
NO.	NAME			
1	VIN	P	Input Supply	Input to the startup regulator. The operating input range is 13 V to 100 V with transient capability to 105 V.
2	COMP1	I	PWM Control, Controller 1	The COMP1 input provides voltage feedback to the PWM comparator inverting input of Controller 1 through a 3:1 divider. The OUT1 duty cycle increases as the COMP1 voltage increases. An internal 5-KΩ pull-up resistor to 5.0-V provides bias current to an opto-coupler transistor.
3	CS1	I	Current Sense Input, Controller 1	Input for current mode control and the current limit sensing. If the CS1 pin exceeds 0.5V the OUT1 pulse is terminated producing cycle-by-cycle current limiting. External resistance connected to CS1 will adjust (increase) PWM slope compensation. This pin's voltage must not exceed 1.25V.
4	SS1	I	Soft-start, Controller 1	An internal 50-µA current source charges an external capacitor to set the soft-start rate. During a current limit restart sequence, the internal current source is reduced to 1 µA to increase the delay before retry. Forcing SS1 below 0.5 V shuts off Controller 1.
5	UVLO	I	VIN Under-Voltage Lockout	An external resistor divider sets the input voltage threshold to enable the LM5032. The UVLO comparator reference voltage is 1.25 V. A switched 20-µA current source provides adjustable UVLO hysteresis. The UVLO pin voltage also controls the maximum duty cycle as described in the *Feature Description* section.
6	VCC	P	Start-up regulator output	Output of the 7.7-V high-voltage start-up regulator. Current limit is a minimum of 19 mA.
7	OUT1	O	Main Gate Driver, Controller 1	Gate driver output to the primary side switch for Controller 1. OUT1 swings between VCC and GND1 at a frequency equal to half the oscillator frequency.
8	GND1	G	Ground, Controller 1	Ground connection for Controller 1 including gate driver, PWM controller, soft-start and support functions.
9	GND2	G	Ground, Controller 2	Ground connection for Controller 2 including the gate driver, PWM controller and soft-start.
10	OUT2	O	Main Gate Driver, Controller 2	Gate driver output to the primary side switch for Controller 2. OUT2 swings between VCC and GND2 at a frequency equal to half the oscillator frequency.
11	RES	I	Hiccup mode restart adjust	An external capacitor sets the time delay before forced restart during a sustained period of cycle-by-cycle current limiting. The hiccup mode comparator threshold is 2.55 V.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION	APPLICATIONS INFORMATION
NO.	NAME			
12	SS2	I	Soft-start, Controller 2	An internal 50-µA current source charges an external capacitor to set the soft-start rate. During a current limit restart sequence, the internal current source is reduced to 1 µA to increase the delay before retry. Forcing SS2 below 0.5 V shuts off Controller 2.
13	CS2	I	Current Sense Input, Controller 2	Input for current mode control and the current limit sensing. If the CS2 pin exceeds 0.5 V the OUT2 pulse is terminated producing cycle-by-cycle current limiting. External resistance connected to CS2 will adjust (increase) PWM slope compensation. This pin's voltage must not exceed 1.25V.
14	COMP2	I	PWM Control, Controller 2	The COMP2 input provides voltage feedback to the PWM comparator inverting input of Controller 2 through a 3:1 divider. The OUT2 duty cycle increases as the COMP2 voltage increases. An internal 5kΩ pull-up resistor to 5.0 V provides bias current to the opto-coupler transistor.
15	DCL	I	Duty Cycle Limit	An external resistor sets the maximum allowed duty cycle at OUT1 and OUT2.
16	RT/SYNC	I	Oscillator Adjust and Synchronizing input	An external resistor sets the oscillator frequency. This pin also accepts ac-coupled synchronization pulses from an external source.

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

	MIN	MAX	UNIT
VIN to GND	–0.3	105	V
VCC to GND	–0.3	16	V
RT/SYNC, RES and DCL to GND	–0.3	5.5	V
CS Pins to GND	–0.3	1.25	V
All other inputs to GND	–0.3	7	V
Junction temperature		150	°C
Lead Temperature (Soldering 4 sec),[3]		260	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. *Recommended Operating Conditions* are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the *Electrical Characteristics*.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For detailed information on soldering plastic TSSOP packages, refer to the Packaging Data Book available from Texas Instruments.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN Voltage	13	100	V
External Voltage Applied to VCC	8	15	V
Operating Junction Temperature	–40	125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		LM5032 PW 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	42.4	
ψ_{JT}	Junction-to-top characterization parameter	1.7	
ψ_{JB}	Junction-to-board characterization parameter	41.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

MIN and MAX limits apply –40°C ≤ T_J ≤ 125°C. VIN = 48 V, VCC = 10 V externally applied, R_T = R_{DCL} = 42.2kΩ, UVLO = 1.5 V, T_J = 25°C, unless otherwise stated, see(1)and see(2).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STARTUP REGULATOR (VIN, VCC Pins)						
V_{CC}Reg	V_{CC} voltage	Ext. supply disconnected.	7.4	7.7	8	V
$I_{CC(Lim)}$	V_{CC} current limit	VCC = 0V.	19	22		mA
V_{CC} UVT	V_{CC} Under-voltage threshold (V_{CC} increasing)	Ext. supply disconnected, VIN =11V.	VCC - 300 mV	VCC - 100 mV		V
	V_{CC} decreasing		5.5	6.2	6.9	V
I_{IN}	Startup regulator current	VIN = 90V, UVLO = 0V		500	600	µA
I_{CC}In	Supply current into VCC from external source	Output loads = open, V_{CC} = 10V		4.3	7	mA
UVLO						
UVLO	Under-voltage threshold		1.22	1.25	1.28	V
I_{HYST}	Hysteresis current		16	20	24	µA
CURRENT SENSE INPUT (CS1, CS2 Pins)						
CS	Current Limit Threshold		0.45	0.5	0.55	V
	CS delay to output	CS1 (CS2) taken from zero to 1.0V. Time for OUT1 (OUT2) to fall to 90% of VCC. Output load = 0 pF.		40		ns
	Leading edge blanking time at CS1 (CS2)			50		ns
	CS1 (CS2) sink impedance (clocked)	Internal pull-down FET on.		30	55	Ω
R_{CS}	Equivalent input resistance at CS	CS taken from 0.2V to 0.5V, internal FET off.		42		kΩ
CURRENT LIMIT RESTART (RES Pin)						
ResTh	Threshold		2.4	2.55	2.7	V
	Charge source current		15	20	25	µA
	Discharge sink current		7.5	10	12.5	µA
SOFT-START (SS1, SS2 Pins)						
I_{SS}	Current source (normal operation)		35	50	65	µA
	Current source during a current limit restart		0.7	1	1.3	µA
V_{SS}	Open circuit voltage			5		V
OSCILLATOR (RT/SYNC Pin)						
F_{S1}	Frequency 1 (at OUT1, OUT2)	R_T = 42.2 kΩ	183	200	217	kHz
F_{S2}	Frequency 2 (at OUT1, OUT2)	R_T = 13.7 kΩ	530	600	670	kHz

(1) All electrical characteristics having room temperature limits are tested during production with T_A = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Typical specifications represent the most likely parametric norm at 25°C operation

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Electrical Characteristics (continued)

MIN and MAX limits apply –40°C ≤ T_J ≤ 125°C. VIN = 48 V, VCC = 10 V externally applied, R_T = R_{DCL} = 42.2kΩ, UVLO = 1.5 V, T_J = 25°C, unless otherwise stated, see(1)and see(2).

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DC voltage			2		V
	Input Sync threshold		2.6	3.3	3.7	V
PWM CONTROLLER (COMP1, COMP2, Duty Cycle Limit Pins)						
	Delay to output	COMP1 (COMP2) set to 2V. CS1 (CS2) stepped from 0 to 0.4V. Time for OUT1 (OUT2) to fall to 90% of VCC. Output load = 0 pF.		50		ns
V_{COMP}	COMP1 (COMP2) open circuit voltage			5		V
I_{COMP}	COMP1 (COMP2) short circuit current	COMP1 (COMP2) = 0V	0.6	1	1.4	mA
	COMP1 (COMP2) to PWM1 (PWM2) gain			0.33		V/V
	Minimum duty cycle	SS1 (SS2) = 0V			0%	
	Maximum duty cycle 1	UVLO pin = 1.30V, R_{DCL} = R_T, COMP1 (COMP2) = open		76%		
	Maximum duty cycle 2	UVLO pin = 3.75V, R_{DCL} = R_T, COMP1 (COMP2) = open		20%		
	Maximum duty cycle 3	UVLO pin = 1.30V, R_{DCL} = R_T/4, COMP1 (COMP2) = open		20%		
	Maximum duty cycle 4	UVLO pin = 2.50V, R_{DCL} = R_T, COMP1 (COMP2) = open		50%		
	Maximum duty cycle 5	UVLO pin = 1.30V, R_{DCL} = R_T/2, COMP1 (COMP2) = open		40%		
	Slope compensation	Delta increase at PWM comparator to CS1 (CS2)		90		mV
	Channel mismatch	CS1 (CS2) = 0.25V			7%	
	Soft-start to COMP offset	SS1 (SS2) = 0.8V		0		V
MAIN OUTPUT DRIVERS (OUT1, OUT2)						
	Output high voltage	I_{OUT} = 50mA (source)	VCC-1	VCC-0.2		V
	Output low voltage	I_{OUT} = 100 mA (sink)		0.3	1	V
	Rise time	C_{LOAD} = 1 nF		12		ns
	Fall time	C_{LOAD} = 1 nF		10		ns
	Peak source current			1.5		A
	Peak sink current			2.5		A
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature			165		°C
	Hysteresis			20		°C

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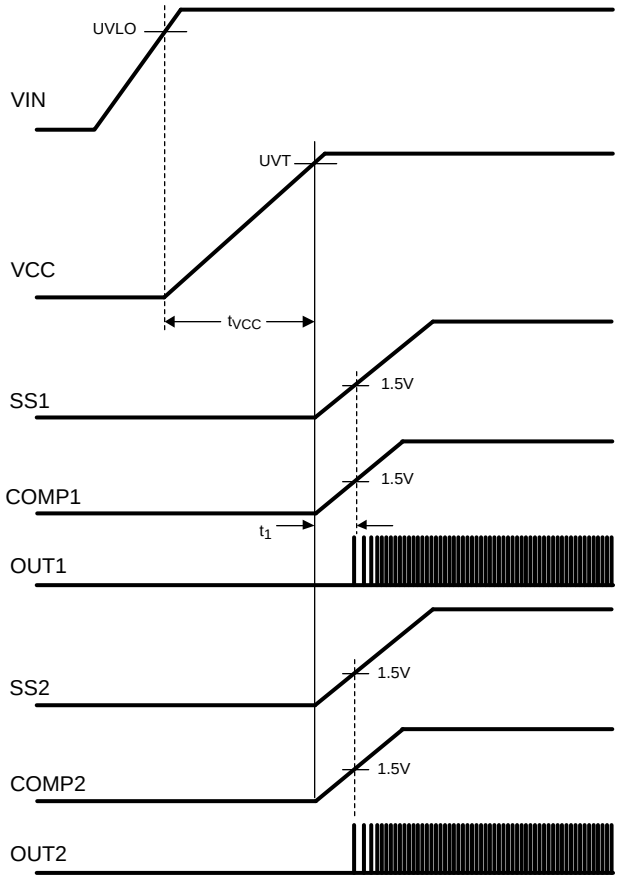

Figure 1. Startup Sequence

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6.6 Typical Characteristics

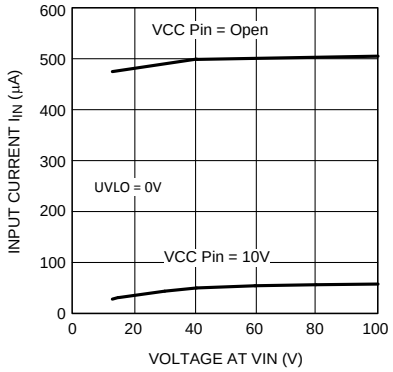

Figure 2. I_{IN} vs VIN

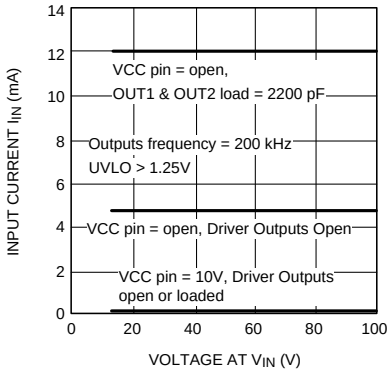

Figure 3. I_{IN} vs VIN

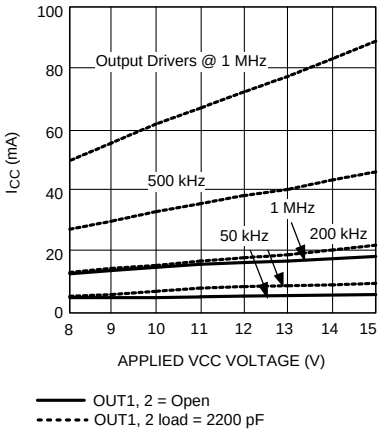

Figure 4. I_{CC} vs Externally Applied VCC

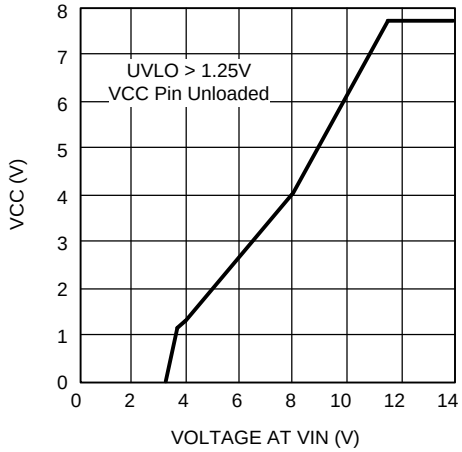

Figure 5. VCC vs VIN

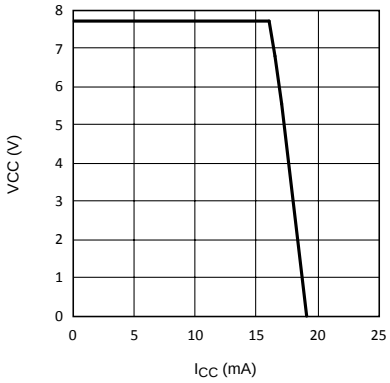

Figure 6. VCC vs I_{CC} (Externally Loaded)

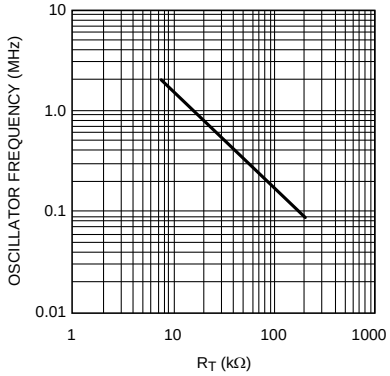

Figure 7. Oscillator Frequency vs R_T Resistor

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Typical Characteristics (continued)

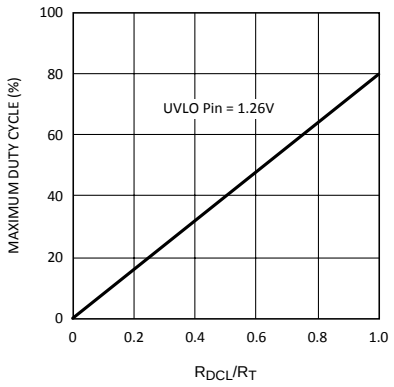

Figure 8. User Defined Maximum Duty Cycle vs R_{DCL} Resistor

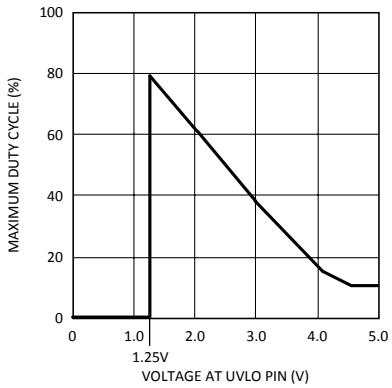

Figure 9. Maximum Duty Cycle vs. UVLO Voltage

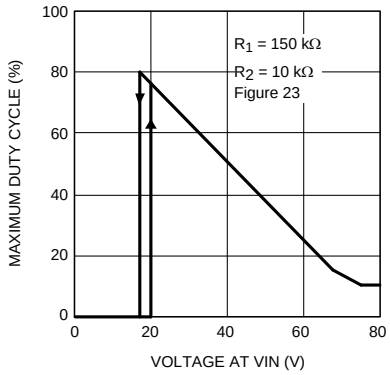

Figure 10. Maximum Duty Cycle vs. VIN (Figure 24)

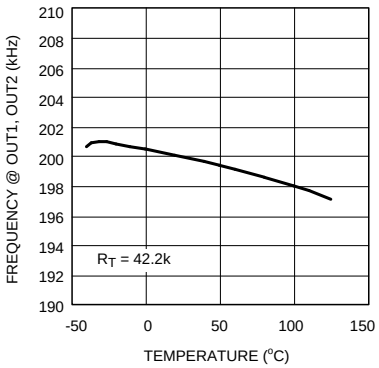

Figure 11. Frequency vs. Temperature

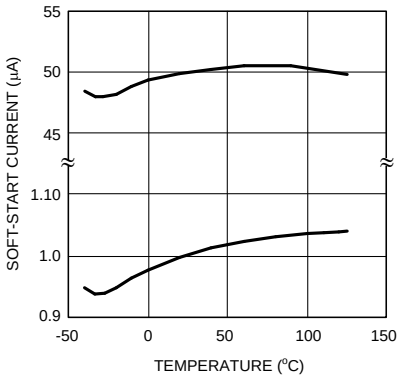

Figure 12. Soft-Start Pin Current vs Temperature

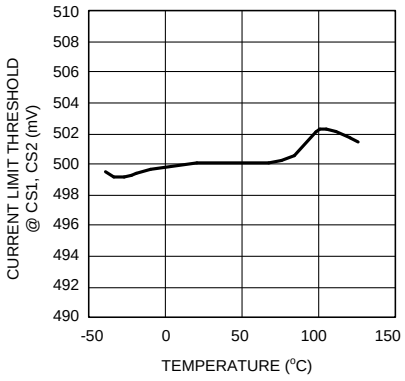

Figure 13. Current Limit Threshold at CS1, CS2 vs Temperature

7 Detailed Description

7.1 Overview

The LM5032 contains all the features necessary to implement two independently regulated current mode dc/dc converters, or a single high current converter comprised of two parallel interleaved channels using the Forward converter topology. The two controllers operate 180° out of phase from a common oscillator, thereby reducing input ripple current. Each regulator channel contains a complete PWM controller, current sense input, soft-start circuit, and gate driver output. Common to both channels are the startup and V_{CC} regulator, line under-voltage lockout, 2 MHz capable oscillator, maximum duty cycle control, and the hiccup mode fault protection circuit.

The gate driver outputs (OUT1, OUT2) are designed to drive N-channel MOSFETs. Their compound configuration reduces the turn-off-time, thereby reducing switching losses. Additional features include thermal shutdown, slope compensation, and the oscillator synchronization capability.

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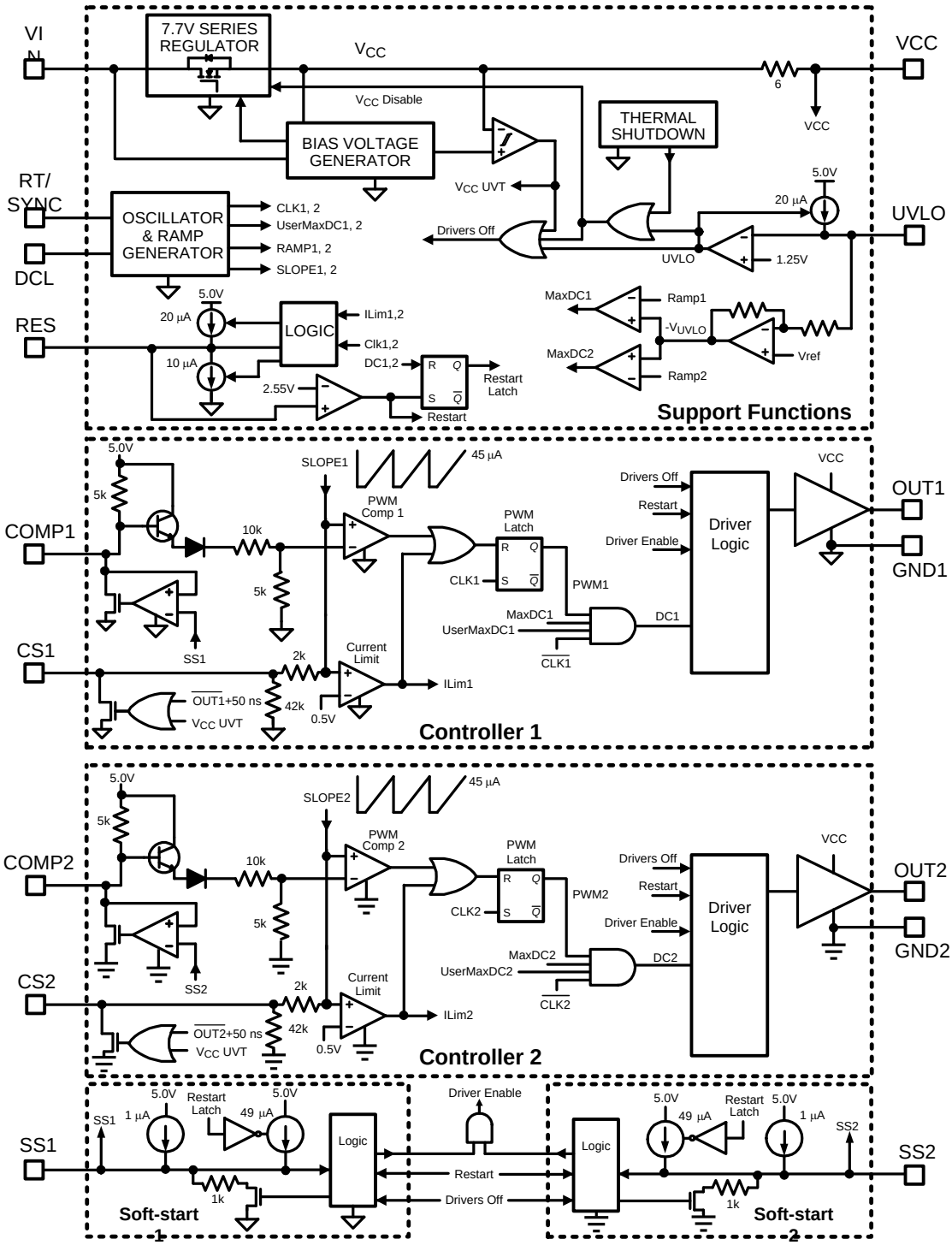
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Line Undervoltage Lock Out, UVLO, Shutdown

The LM5032 contains a line under-voltage lockout circuit (UVLO) designed to enable the V_{CC} regulator and output drivers when the system voltage (V_{PWR}) exceeds the desired level (see Figure 14). V_{PWR} is the voltage normally applied to the transformer primary, and usually connected to the VIN pin (see the schematic on Page 1). The threshold at the UVLO comparator is 1.25V. An external resistor divider connected from V_{PWR} to ground provides 1.25V at the UVLO pin when V_{PWR} is increased to the desired turn-on threshold. When V_{PWR} is below the threshold the V_{CC} regulator and output drivers are disabled, and the internal 20 µA current source is off. When V_{PWR} reaches the threshold, the comparator output switches low to enable the internal circuits and the 20 µA current source. The 20 µA flows into the external divider's junction, raising the voltage at UVLO, thereby providing hysteresis. Internally the voltage at UVLO also drives the Maximum Duty Cycle Limiter circuit (described below), which may influence the values chosen for the UVLO pin resistors. At maximum V_{PWR}, the voltage at UVLO should not exceed 6V. Refer to the Applications Information section for a procedure to calculate the resistors values.

The LM5032 controller can be shutdown by forcing the UVLO pin below 1.25V with an external switch. When the UVLO pin is low, the outputs and the V_{CC} regulator are disabled, and the LM5032 enters a low power mode. If VCC pin is not powered from an external source, the current into VIN drops to a nominal 500 µA. If the VCC pin is powered from an external source, the current into VIN is nominally 50 µA, and the current into the VCC pin is approximately 4.3 mA. To disable one regulator without affecting the other, see the description of the Soft-start section.

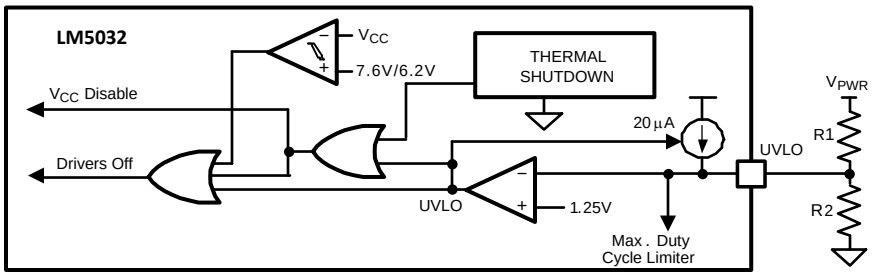


Figure 14. Drivers Off and V_{CC} Disable

7.3.2 Startup Regulator, VIN, VCC

The high voltage startup regulator is integral to the LM5032. The input pin VIN can be connected directly to a voltage between 13V and 100V, with transient capability to 105V. The startup regulator provides bias voltages to the series pass V_{CC} regulator and the UVLO circuit. The V_{CC} regulator is disabled until the voltage at the UVLO pin (described above) exceeds 1.25V. For applications where V_{PWR} exceeds 100V the internal startup regulator can be powered from an external startup regulator or other available low voltage source. See the Applications Information section for details.

The V_{CC} under-voltage threshold circuit (UVT) monitors the VCC regulator output. When the series pass regulator is enabled and the internal V_{CC} voltage increases to > 7.6V, the UVT comparator activates the PWM controller and output drivers via the Drivers Off signal. The UVT comparator has built-in hysteresis, with the lower threshold nominally set to 6.2V. See Figure 1 and Figure 14.

When enabled, the V_{CC} regulated output is 7.7V ±4% with current limited to a minimum of 19 mA (typically 22 mA). The regulator's output impedance is ≅ 6Ω.

The VCC pin requires a capacitor to ground for stability, as well as to provide the surge currents to the external MOSFETs via the gate driver outputs. The capacitor should be physically close to the VCC and GND pins.

In most applications it is necessary to power V_{CC} from an external source as the average current required at the output drivers may exceed the current capability of the internal regulator and/or the thermal capability of the LM5032 package (see Figure 4). Normally the external source is derived from the converter's power stage once the LM5032 outputs are active. Refer to the Applications Information section for more information.

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Feature Description (continued)

7.3.3 Drivers Off, V_{CC} Disable

Referring to Figure 14, Drivers Off and V_{CC} Disable are internal signals which, when active disable portions of the LM5032. If the UVLO pin is below 1.25V, or if the thermal shutdown activates, the V_{CC} Disable line switches high to disable the V_{CC} regulator. UVLO also activates the Drivers Off signal to disable the output drivers, connect the SS1, SS2, COMP1, COMP2 and RES pins to ground, and enable the 50 µA Soft-start current sources.

If the V_{CC} voltage falls below the under-voltage threshold of 6.2V , the UVT comparator activates only the Drivers Off signal. The output drivers are disabled but the V_{CC} regulator is not disabled. Additionally, the CS1, CS2, SS1, SS2, COMP1, COMP2 and RES pins are internally grounded, and the 50 µA Soft-start current sources are enabled.

7.3.4 Oscillator

The oscillator frequency is set with an external resistor R_T connected between the RT/SYNC and GND1 pins. The resistor value is calculated from:

$$R_T = \frac{17100}{F_S} - 0.001(F_S - 400) \quad (1)$$

where F_S is the desired oscillator frequency in kHz (maximum of 2 MHz), and R_T is in kΩ. See Figure 7. The two gate driver outputs (OUT1 and OUT2) switch at half the oscillator frequency and 180° out of phase with each other. The voltage at the R_T/SYNC pin is internally regulated at 2.0V. The R_T resistor should be located as close as possible to the LM5032 with short direct connections to the pins.

The LM5032 can be synchronized to an external clock by applying a narrow clock pulse to the R_T/SYNC pin. See the Applications Information section for details on this procedure. The R_T resistor is always required, whether the oscillator is free running or externally synchronized.

7.3.5 PWM Comparator/Slope Compensation

The PWM comparator of each controller compares a slope compensated current ramp signal with the loop error voltage derived from the COMP pin. The COMP voltage is typically controlled by an external error amplifier/optocoupler feedback circuit to regulate the converter output voltage. Internally, the voltage at the COMP pin passes through two level shifting diodes and a gain reducing 3:1 resistor divider (see Figure 15). The compensated current ramp signal is a combination of the current waveform at the CS pin, and an internally generated ramp derived from the internal clock. At duty cycles greater than 50% current mode control circuits are prone to subharmonic oscillation. By adding a small fixed ramp to the external current sense signal oscillations can be avoided. The internal ramp has an amplitude of 45 µA and is sourced into an internal 2kΩ resistor, and a 42 kΩ resistor in parallel with the external impedance at the CS pin. The ramp current also flows through the external impedance connected to the CS pin and thus, the amount of slope compensation can be adjusted by varying the external circuit at the CS pin.

The output of the PWM comparator provides the pulse width information to the output drivers. This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The comparator's output duty cycle is 0% for V_{COMP} ≤1.5V, and increases as V_{COMP} increases.

If either Soft-start pin is pulled low (internally or externally) the corresponding COMP pin is pulled down with it, forcing the output duty cycle to zero. When the Soft-start pin voltage increases, the COMP pin is allowed to increase. An internal 5 kΩ resistor connected from COMP to an internal 5.0V supply provides a pull-up for the COMP pin and bias current to the collector of the opto-coupler transistor.

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Feature Description (continued)

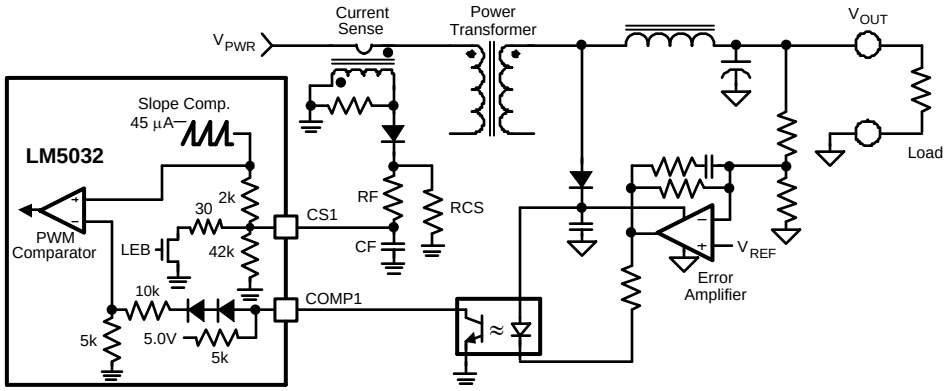

Figure 15. Typical Feedback Network

7.3.6 Cycle-by-Cycle Current Limit

Each CS pin is designed to accept a signal representative of its transformer primary current. If the voltage at CS exceeds 0.5V the current sense comparator terminates the present main output driver (OUT pin) pulse. If the high current fault persists, the controller operates with constant peak switch current in a cycle-by-cycle current limit mode, and a Hiccup Mode Current Limit Restart cycle begins (see below).

Each CS pin is internally connect to ground through a 30Ω resistor during the main output off time to discharge external filter capacitance. The discharge device remains on for an additional 50 ns after the main output driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filter requirement which improves the current sense response time.

The current sense comparators are fast and respond to short duration noise pulses. The external circuitry at each CS pin should include an R-C filter to suppress noise. Layout considerations are critical for the current sense filter and the sense resistor. Refer to the Applications Information section for PC board layout guidelines.

7.3.7 Hiccup Mode Current Limit Restart

If cycle-by-cycle current limiting continues in either or both controllers for a sufficient period of time, the Current Limit Restart circuit disables both regulators and initiates a soft-start sequence after a programmable delay. The duration of cycle-by-cycle current limiting before turn-off occurs is programmed by the value of the external capacitor at the RES pin. The dwell time before output switching resumes is programmed by the value of the Soft-start capacitor(s). The circuit is detailed in Figure 16 and the timing is shown in Figure 17. A description of this circuit's operation is as follows:

a) No current limit detected:

The 10 µA discharge current source at RES is enabled pulling the RES pin to ground.

b) Current limit repeatedly detected at both CS inputs:

The 20 µA current source at RES is enabled continuously to charge the RES pin capacitor as shown in Figure 17. The current limit comparators also terminate the PWM output pulses to provide a cycle-by-cycle current limiting. When the voltage on the RES capacitor reaches the 2.55V restart comparator threshold, the comparator sets the Restart Latch which produces the following restart sequence:

- The SS1 and SS2 pin charging currents are reduced from 50µA to 1 µA.
- An internal MOSFET is turned on to discharge the RES pin capacitor.
- The internal MOSFETs at SS1 and SS2 are turned on to discharge the Soft-start capacitors.
- COMP1 and COMP2 follow SS1 and SS2 respectively and reduce the PWM duty cycles to zero.
- When the voltages at the SS pins fall below 200mV, the internal MOSFETs at the SS pins are turned off allowing the SS pins to be charged by the 1µA current sources.
- When either SS pin reaches ≅1.5V its PWM controller produces the first pulse of a soft-start sequence which

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Feature Description (continued)

resets the Restart Latch. The SS charging currents are increased to 50 µA and the soft-start sequence continues at the normal rate.

If the overload condition still exists, the voltage at RES begins to increase again and repeat the restart cycle as shown in Figure 17. If the overload condition has been cleared, the RES pin is held at ground by the 10 µA current source.

c) Current limit repeatedly detected at one of the two CS inputs:

In this condition the RES pin capacitor is charged by the 20 µA current source once each clock cycle of the current limited regulator, and discharged by the 10 µA current source once each clock cycle of the unaffected regulator. The voltage at the RES pin increases one fourth as fast as in case b) described above. The current limited regulator operates in a cycle-by-cycle current limit mode until the voltage at RES reaches the 2.55V threshold. When the Restart Comparator output switches high the Restart Latch is set, both SS pin capacitors are discharged to disable the regulator channels, and a restart sequence begins as described in case b) above.

To determine the value of the RES pin capacitor, see the Applications Information section.

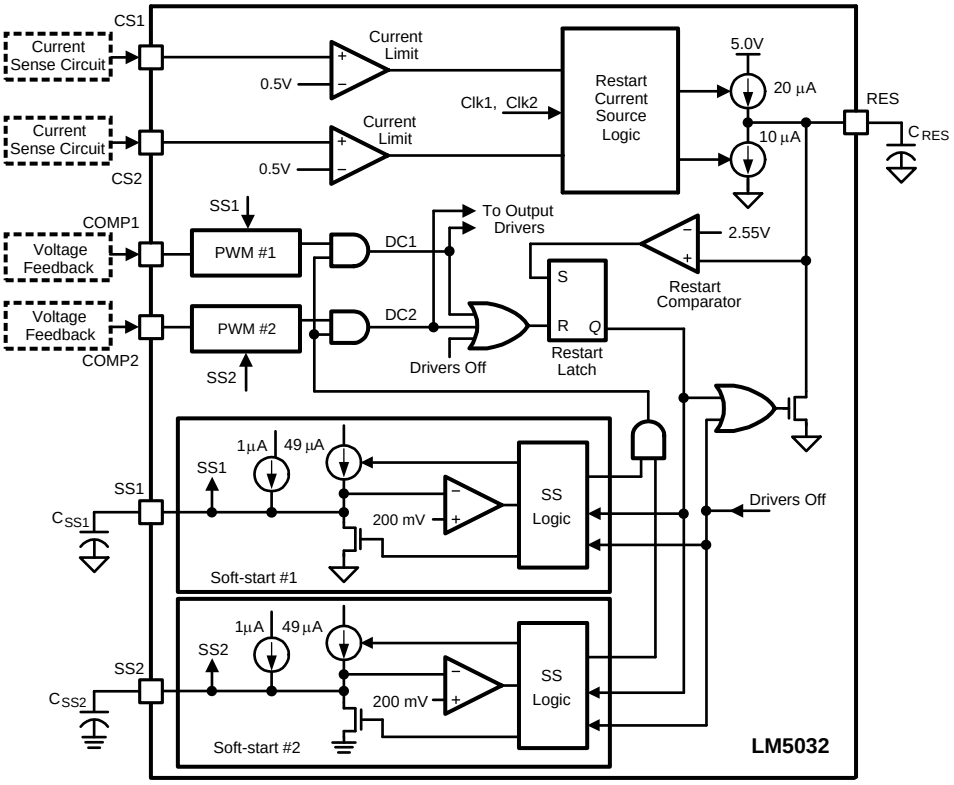

Figure 16. Current Limit Restart Circuit

Feature Description (continued)

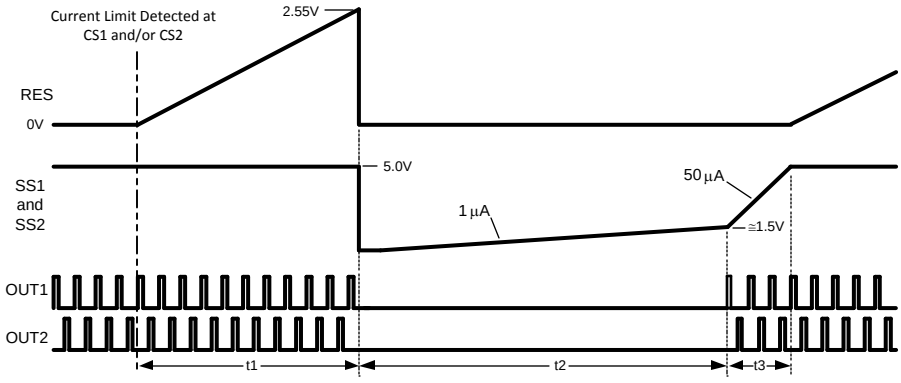

Figure 17. Current Limit Restart Timing

7.3.8 Soft-Start

Each soft-start circuit allows the corresponding regulator to gradually reach a steady state operating point, thereby reducing startup current surges and output overshoot. Upon turn-on, both SS pins are internally held at ground. When VCC increases past its under-voltage threshold (UVT), the SS pins are released and internal 50 µA current sources charge the external capacitors. The voltage at each COMP pin follows the SS pin, and when COMP reaches ≅1.5V, the output pulses commence at a low duty cycle. The voltage at the SS pins continues to increase and saturates at ≅5.0V, The voltage at each COMP pin increases to the value required for regulation where it is controlled by its voltage feedback loop (see Figure 1).

If the internal Drivers Off line is activated (see *Drivers Off, V_{CC} Disable*), both SS pins are internally grounded. The SS pins pull the COMP pins to ground while the Driver Off signal disables the output drivers. When the event which activated the Drivers Off line is cleared and Vcc exceeds its under-voltage threshold, the SS pins are released. The internal 50 µA current sources then charge the external soft-start capacitors allowing each regulator's output duty cycle to increase.

If the Current Limit Restart threshold is reached due to repeated over-current detections, both SS pins (and the COMP pins) are pulled to ground. The output drivers are disabled, and the 50 µA SS pin current sources are reduced to 1 µA. After a short propagation delay the SS pins and the COMP pins are released, and the external capacitors are charged up at a slow rate. When the COMP voltage reaches ≅ 1.5V, the output drivers are enabled, and the current sources at the SS pins are increased to 50 µA. The output duty cycle then increases to the value required for regulation.

To shutdown one regulator without affecting the other, ground the appropriate SS pin. This forces the COMP pin to ground, reducing the output duty cycle to zero for that regulator. Releasing the SS pin allows normal operation to resume.

7.3.9 Output Duty Cycle

The output driver's duty cycle for each controller is normally controlled by comparing the voltage provided to the COMP input by the external voltage feedback circuit with the current information at the CS pin. However, the maximum duty cycle during transient or fault conditions may be intentionally limited by two other circuits, both of which are common to the two controller channels.

User Defined Maximum Duty Cycle. The maximum allowed duty cycle can be set with the R_{DCL} resistor connected from the DCL pin to GND1, according to the following equation:

$$\text{Maximum User Duty Cycle} = 80\% \times R_{DCL}/R_T \quad (2)$$

R_T is the oscillator frequency programming resistor connected to the R_T/SYNC pin. The value of the R_{DCL} resistor must be calculated after the R_T resistor is selected. See Figure 8. Referring to the block diagram of the voltage at the DCL pin is compared to the Ramp1 and Ramp2 signals, creating the UserMaxDC1 and UserMaxDC2 timing signals. These signal are provided to the two 4-input AND gates to limit the PWM duty cycle of both channels.

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Feature Description (continued)

Line Voltage Maximum Duty Cycle. The voltage at the UVLO pin, normally proportional to the voltage at V_{PWR}, further limits the maximum duty cycle at high input voltages. Referring to Figure 10, when the UVLO pin is below 1.25V, the outputs are disabled. At UVLO = 1.25V the maximum allowed duty cycle is 80% (or less if limited by the DCL resistor). As the UVLO pin voltage increases with V_{PWR}, the maximum duty cycle decreases, reaching a minimum of 10% at ≅4.5V. Referring to the UVLO voltage, after passing through an inverting gain stage, is compared to the Ramp1 and Ramp2 signals generated by the oscillator. The output of these comparators are the MaxDC1 and MaxDC2 timing signals. These signals are provided to the two 4-input AND gates which limit the PWM pulses delivered to the output drivers.

Resulting Output Duty Cycle. The controller duty cycle is determined by the four signals into the 4-input AND gates in (UserMaxDC, MaxDC, PWM and CLK). The output driver pulsewidth is equal to the least of these four pulses. Whichever input of the AND gate transitions high-to-low first terminates the output driver's on-time.

7.3.10 Driver Outputs

OUT1, the primary switch driver for Controller 1 is designed to drive the gate of an N-channel MOSFET with 1.5A sourcing current and 2.5A sinking current. The peak output levels are VCC and GND1. The ground return path for Controller 1 is GND1. The corresponding pins for Controller 2 are OUT2 and GND2.

OUT1 and OUT2 are compound gate drivers with CMOS and Bipolar output transistors as shown in Figure 18. The parallel MOS and Bipolar devices provide a faster turn-off of the primary switch thereby reducing switching losses. The outputs switch at one-half the oscillator frequency with the rising edges at OUT1 and OUT2 180° out of phase with each other. The on-time of OUT1 and OUT2 is determined by their respective duty cycle control.

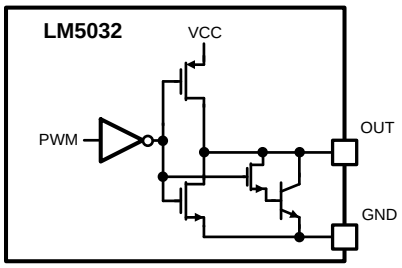

Figure 18. Compound Gate Driver

7.3.11 Thermal Shutdown

The LM5032 should be operated so the junction temperature does not exceed 125°C. If a junction temperature transient reaches 165°C (typical), the Thermal Shutdown circuit activates the V_{CC} Disable and Drivers Off lines (see Figure 14). The V_{CC} regulator and the four output drivers are disabled, the SS1, SS2, and RES pins are grounded, and the soft-start current is set to 50 µA. This puts the LM5032 in a low power state helping to prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled and a startup sequence is initiated (Figure 1).

7.4 Device Functional Modes

Normal device operating mode is described above in sections *Line Undervoltage Lock Out, UVLO, Shutdown* through *Cycle-by-Cycle Current Limit*, and sections *Soft-Start* to *Thermal Shutdown*. Under overcurrent fault conditions, the device operate in Hiccup Mode, as detailed above in the *Hiccup Mode Current Limit Restart* section.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 VIN

The voltage applied to the VIN pin, normally the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary in the range of 13 to 100V with transient capability to 105V. The current into VIN depends primarily on the output driver capacitive loads, the switching frequency, and any external load at VCC. If the power dissipation associated with the VIN current exceeds the package capability, an external voltage should be applied to VCC (see Figure 2 & Figure 3) to reduce power in the internal start-up regulator. It is recommended the circuit of Figure 19 be used to suppress transients which may occur at the input supply, in particular where VIN is operated close to the maximum operating rating of the LM5032.

When all internal bias currents for the LM5032 and output driver currents are supplied through VIN and the internal V_{CC} regulator, the required input current (I_{IN}) is shown in Figure 2 & Figure 3. In most applications, upon turn-on, I_{IN} increases with V_{IN} as shown in Figure 2 until the UVLO threshold is reached. After the outputs are enabled and the external VCC supply voltage is active, the current into VIN then drops to a nominal 120 µA.

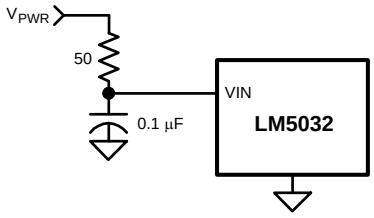

Figure 19. Input Transient Protection

8.1.2 For Applications > 100 V

For applications where the system input voltage (V_{PWR}) exceeds 100V, VIN can be powered from an external start-up regulator as shown in Figure 20, or from any other low voltage source as shown in Figure 21. Connecting VIN and VCC together allows the LM5032 to be operated with VIN below 13V. The voltage at VCC must not exceed 15V. The voltage source at the right side of Figure 20 is typically derived from the power stage, and becomes active once the LM5032's outputs are active.

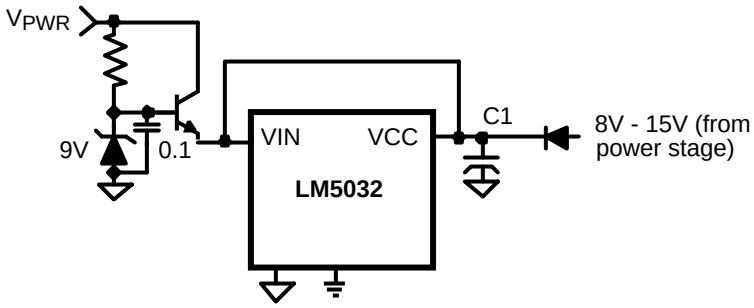

Figure 20. Start-up Regulator for V_{PWR} >100V

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Application Information (continued)

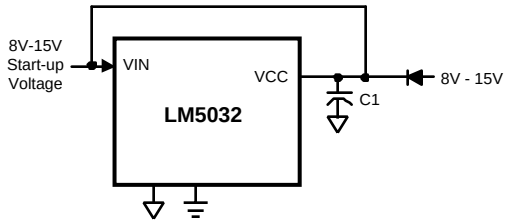

Figure 21. Bypassing the Internal Start-up Regulator

8.1.3 UVLO

The under-voltage lockout threshold (UVLO) is internally set at 1.25V at the UVLO pin. With two external resistors as shown in Figure 22, the LM5032 is enabled when V_{PWR} exceeds the programmed threshold voltage. When V_{PWR} is above the threshold, the internal 20 µA current source is enabled to raise the voltage at the UVLO pin, providing hysteresis. R1 and R2 are determined from the following equations:

$$R1 = V_{HYS}/20\ \mu A \quad (3)$$

$$R2 = \frac{1.25 \times R1}{V_{PWR} - 1.25} \quad (4)$$

where V_{HYS} is the desired UVLO hysteresis at V_{PWR}, and V_{PWR} in the second equation is the turn-on voltage. For example, if the LM5032 is to be enabled when V_{PWR} reaches 20V, and disabled when V_{PWR} is decreased to 17V, R1 calculates to 150 kΩ, and R2 calculates to 10 kΩ. The voltage at UVLO should not exceed 6V at any time.

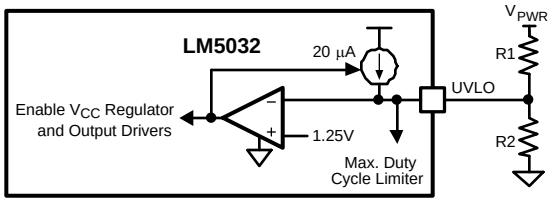

Figure 22. UVLO Circuit

The LM5032 can be remotely shutdown by taking the UVLO pin below 1.25V with an external open collector or open drain device, as shown in Figure 23. The outputs, and the V_{CC} regulator, are disabled, and the LM5032 enters a low power mode. To shut down one regulator without affecting the other, see the Soft-start section.

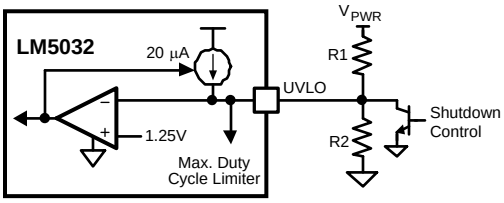

Figure 23. Shutdown Control

Application Information (continued)

8.1.4 VCC

The capacitor at VCC provides not only regulator noise filtering and stability, but also prevents VCC from dropping to the lower under-voltage threshold level (UVT = 6.2V) when the output drivers source current surges to the external MOSFET gates. Additionally, the capacitor provides a necessary time delay during startup. The time delay allows the internal circuitry of the LM5032 and associated external circuitry to stabilize before VCC reaches the upper UVT threshold level (7.6V), at which time the outputs are enabled and the soft-start sequence begins. VCC is nominally regulated at 7.7V. The delay to the UVT level (Figure 1) is calculated from the following:

$$t_{VCC} = \frac{C1 \times 7.6V}{I_{CC(Lim)}} \quad (5)$$

where C1 is the capacitor at VCC and $I_{CC(Lim)}$ is the V_{CC} regulator's current limit. If the capacitor is 0.1 µF, the nominal $I_{CC(Lim)}$ of 22 mA provides a delay of approximately 35 µs. The capacitor value should range between 0.1 µF and 25 µF. Experimentation with the final design may be necessary to determine the optimum value for the VCC capacitor.

The average V_{CC} regulator current required to drive the external MOSFETs is a function of the MOSFET gate capacitance and the switching frequency (see Figure 4). To ensure VCC does not droop below the lower UVT threshold, an external supply should be diode connected to VCC to provide the required current, as shown in Figure 24. The applied V_{CC} voltage must be between 8V and 15V. Providing the V_{CC} voltage higher than the 7.7V regulation level with an external supply shuts off the internal regulator, reducing power dissipation within the IC. Internally there is a diode from the V_{CC} regulator output to VIN. Typically the applied voltage is derived from an auxiliary winding on the power transformer, or on the output inductor.

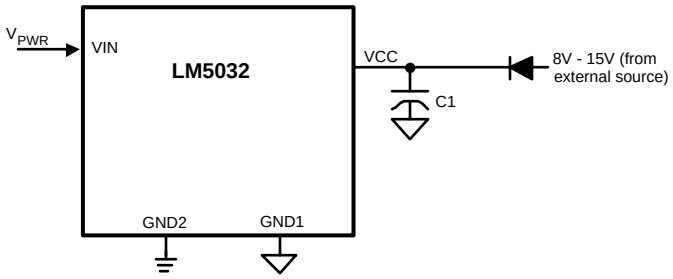

Figure 24. External Power to V_{CC}

8.1.5 Oscillator, Sync Input

The oscillator frequency is generally selected in conjunction with the system magnetic components, and any other aspects of the system which may be affected by the frequency. The R_T resistor at the RT/SYNC pin sets the frequency according to Equation 1. Each output (OUT1 and OUT2) switches at one-half the oscillator frequency. If the required frequency tolerance is critical in a particular application, the tolerance of the external resistor and the frequency tolerance specified in the Electrical Characteristics table must be considered when selecting the R_T resistor.

If the LM5032 is to be synchronized to an external clock, that signal must be coupled into the RT/SYNC pin through a 100 pF capacitor. The external synchronizing frequency must be at least 4% higher than the free running frequency set by the R_T resistor and no higher than twice the free running frequency. The RT/SYNC pin voltage is nominally regulated at 2.0V and the external pulse amplitude should lift the pin to between 3.8V and 5.0V on the low-to-high transition. The synchronization pulse width should be between 15 and 150 ns. The R_T resistor is always required, whether the oscillator is free running or externally synchronized.

8.1.6 Voltage Feedback, COMP1, COMP2

Each COMP pin is designed to accept a voltage feedback signal from the respective regulated output via an error amplifier and (typically) an opto-coupler. A typical configuration is shown in Figure 15. V_{OUT} is compared to a reference by the error amplifier which has an appropriate frequency compensation network. The amplifier's output drives the opto-coupler, which in turn drives the COMP pin.

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Application Information (continued)

When the LM5032's two controller channels are configured to provide a single high current output, COMP1 and COMP2 are typically connected together, and to the feedback signal from the optocoupler.

8.1.7 Current Sense, CS1, CS2

Each CS pin receives an input signal representative of its transformer's primary current, either from a current sense transformer or from a resistor in series with the source of the primary switch, as shown in Figure 25 and Figure 26. In both cases the sensed current creates a ramping voltage across R1, and the R_F/C_F filter suppresses noise and transients. R1, R_F and C_F should be as physically close to the LM5032 as possible, and the ground connection from the current sense transformer, or R1, should be a dedicated track to the appropriate GND pin. The current sense components must provide >0.5V at the CS pin when an over-current condition exists.

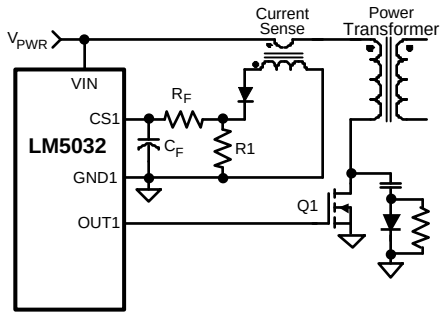

Figure 25. Current Sense Using a Current Sense Transformer

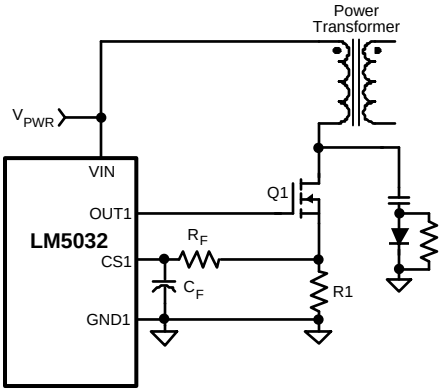

Figure 26. Current Sense Using a Source Sense Resistor (R1)

8.1.8 Hiccup Mode Current Limit Restart

This circuit's operation is described in the Functional Description. Also see Figure 16 and Figure 17. In the case of continuous current limit detection at both CS pins, the time required to reach the 2.55V RES pin threshold is:

$$t1 = \frac{C_{RES} \times 2.55V}{20\ \mu A} = 1.275 \times 10^5 \times C_{RES} \quad (6)$$

For example, if C_{RES} = 0.1 µF the time t1 in Figure 18 is approximately 12.75 ms.

In the case of continuous current limit detection at one CS pin only, the time to reach the 2.55V threshold is increased by a factor of four, or:

$$t1 = 5.1 \times 10^5 \times C_{RES} \quad (7)$$

The time t2 in Figure 17 is set by the capacitor at each SS pin and the internal 1 µA current source, and is equal to:

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Application Information (continued)

$$t2 = \frac{C_{SS} \times 1.5V}{1\ \mu A} = 1.5 \times 10^6 \times C_{SS} \quad (8)$$

If C_{SS} = 0.1 µF t2 is ≅150 ms. Time t3 is set by the internal 50 µA current source, and is equal to:

$$t3 = \frac{C_{SS} \times 3.5V}{50\ \mu A} = 7 \times 10^4 \times C_{SS} \quad (9)$$

The time t2 provides a periodic dwell time for the converter in the event of a sustained overload or short circuit. This results in lower average input current and lower power dissipated within the circuit components. It is recommended that the ratio of t2/(t1 + t3) be in the range of 5 to 10 to make good use of this feature.

If the application requires no delay from the first detection of a current limit condition, so that t1 is effectively zero, the RES pin can be left open (no external capacitor). If it is desired to disable the hiccup mode current limit operation then the RES pin should be connected to ground.

8.1.9 Soft-Start

The capacitors at SS1 and SS2 determine the time required for each regulator's output duty cycle to increase from zero to its final value for regulation. The minimum acceptable time is dependent on the output capacitance and the response of each feedback loop to the COMP pin. If the Soft-start time is too quick, the output could significantly overshoot its intended voltage before the feedback loop has a chance to regulate the PWM controller.

After power is applied and V_{CC} has passed its upper UVT threshold (≅7.6V), the voltage at each SS pin ramps up as its external capacitor is charged up by an internal 50 µA current source (see Figure 1). The voltage at the COMP pins follow the SS pins. When both have reached ≅1.5V, PWM pulses appear at the driver outputs with very low duty cycle. The voltage at each SS pin continues to increase to ≅5.0V. The voltage at each COMP pin, and the PWM duty cycle, increase to the value required for regulation as determined by its feedback loop. The time t1 in Figure 1 is calculated from:

$$t1 = \frac{C_{SS} \times 1.5V}{50\ \mu A} = 3 \times 10^4 \times C_{SS} \quad (10)$$

With a 0.1 µF capacitor at SS, t1 is ≅3 ms.

If the Hiccup Mode Current Limit Restart circuit activates due to repeated current limit detections at CS1 and/or CS2, both SS1 and SS2 are internally grounded (see the section on Hiccup Mode Current Limit Restart). After a short propagation delay, the SS pins are released and the external SS pin capacitors are charged by internal 1 µA current sources. The slow charge rate provides a rest or dwell time for the converter power stage (t2 in Figure 17), reducing the average input current and component temperature rise while in an overload condition. When the voltage at the SS and COMP pins reach ≅1.5V, the first pulse out of either PWM comparator switches the internal SS pin current sources to 50 µA. The voltages at the SS and COMP pins then increase more quickly, increasing the duty cycle at the output drivers. The rest time t2 is the time required for SS to reach 1.5V:

$$t2 = \frac{C_{SS} \times 1.5V}{1\ \mu A} = 1.5 \times 10^6 \times C_{SS} \quad (11)$$

With a 0.1 µF capacitor at SS, t2 is ≅150 ms.

Experimentation with the startup sequence and over-current restart condition is usually necessary to determine the appropriate value for the SS capacitors.

To shutdown one regulator without affecting the other, ground the appropriate SS pin with an open collector or open drain device as shown in Figure 27. The SS pin forces the COMP pin to ground which reduces the PWM duty cycle to zero for that regulator. Releasing the SS pin allows normal operation to resume.

When the LM5032's two controller channels are configured to provide a single high current output, SS1 and SS2 are typically connected together, requiring a single capacitor for the two pins.

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Application Information (continued)

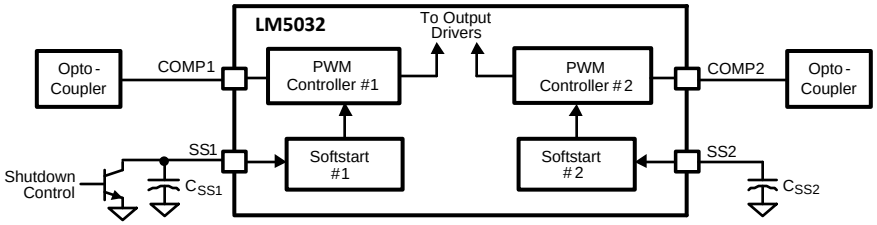

Figure 27. Shutting Down One Regulator Channel

8.1.10 Line Voltage Dependent Maximum Duty Cycle

As V_{PWR} increases and the voltage at UVLO follows, the maximum allowed duty cycle decreases according to the graph of Figure 9. Using values from the example above (R1 = 150 kΩ, R2 = 10 kΩ in Figure 22), the maximum duty cycle varies as shown in Figure 10. If it is desired to increase the slope of the ramp in Figure 10, Figure 28 shows a suggested configuration. After the LM5032 is enabled, Z1 clamps the voltage across R1B, and UVLO increases with V_{PWR} at a rate determined by the ratio R2/(R1A + R2).

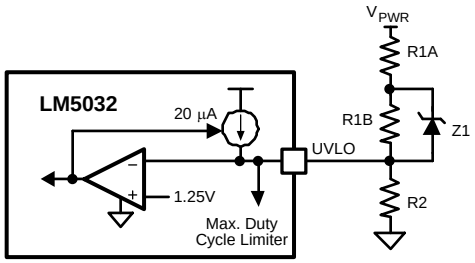

Figure 28. Altering the Slope of Duty Cycle vs. V_{PWR}

8.1.11 User Defined Max Duty Cycle

The maximum allowed duty cycle at OUT1 and OUT2 can be set with a resistor from DCL to GND1. See Figure 8 and Equation 2. The default maximum duty cycle (80%) determined by the internal clock signals can be selected by setting $R_{DCL} = R_T$. The oscillator frequency setting resistor (R_T) must be determined before R_{DCL} is selected. The DCL pin should not be left open.

8.2 Typical Application

Figure 29 shows an example of an LM5032-controlled 200-W interleaved regulator which provides a single regulated 48-V output. The interleaving of two power stages to a single output reduces the ripple voltage across both input and output capacitors, and improves the power stage efficiency compared to a single-stage design. Since the two interleaved control blocks are used to regulate a single combined output, the two soft-start pins SS1 and SS2 are connected to a single soft-start capacitor, and the two COMP1 and COMP2 pins are connected together to a single error amplifier.

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Typical Application (continued)

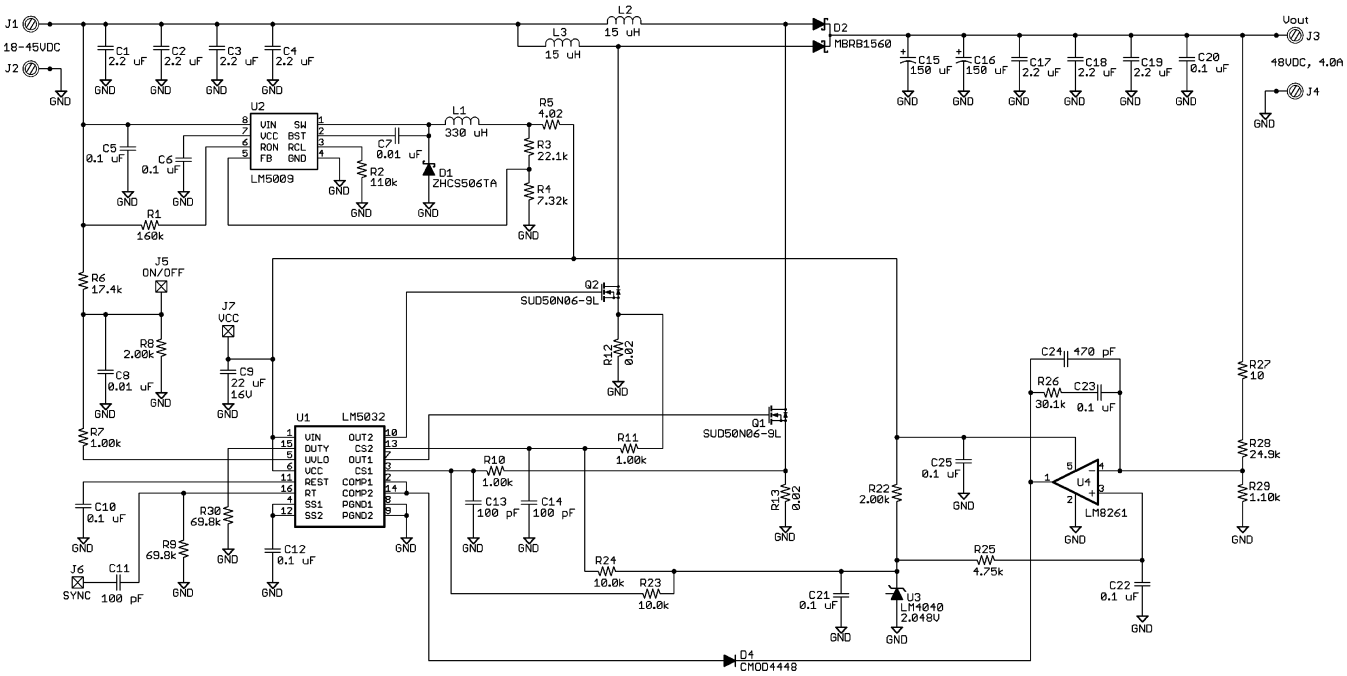

Figure 29. Evaluation Module Schematic

8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input voltage range, V_{IN}	18 V to 45 V
Output voltage, V_{OUT}	48 V
Output current, I_{OUT}	4 A
Output ripple voltage, $V_{RIPPLE(OUT)}$	< 2% (960 mV_{pp})
Switching frequency, F_{SW} (per phase)	123 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Oscillator Frequency and Maximum Duty Cycle

The LM5032 oscillator frequency should be set at twice the target switching frequency of each interleaved power stage, for example, F_{osc} = 2 x F_{sw}.

From Equation 1, the required value of resistor on the RT pin (R9 in Figure 29) is calculated as follows:

$$R_T = \frac{17100}{F_{osc}} - 0.001 \times (F_{osc} - 400) = \frac{17100}{246} - 0.001 \times (246 - 400) = 69.67\,k\Omega \quad (12)$$

The nearest E96 value of 69.8 kΩ is used.

The maximum duty cycle is set to 80% (see the *Output Duty Cycle* section) by choosing the same value resistor on the DCL pin, so R30 is also set to 69.8 kΩ.

8.2.2.2 Power Stage Design

8.2.2.2.1 Boost Inductor Selection

Maximum and minimum operating duty cycles are calculated at maximum and minimum input voltage, where V_d is the boost diode forward voltage drop, and $V_{sw(on)}$ is the voltage drop across the boost MOSFET plus current sense element:

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$$D_{max} = \frac{V_{OUT} + V_d - V_{IN(MIN)}}{V_{OUT} + V_d - V_{sw(on)}} = \frac{48 + 0.7 - 18}{48 + 0.7 - 0.5} = 63.7\% \quad (13)$$

$$D_{min} = \frac{V_{OUT} + V_d - V_{IN(max)}}{V_{OUT} + V_d - V_{sw(on)}} = \frac{48 + 0.7 - 45}{48 + 0.7 - 0.5} = 7.7\% \quad (14)$$

The highest average inductor current in each phase is calculated at highest load and minimum input voltage, where each phase is assumed to carry 50% of the total load current:

$$I_{L(avg)} = \frac{50\% \times I_{out}}{1 - D_{max}} = \frac{0.5 \times 4}{1 - 0.637} = 5.51A \quad (15)$$

Allowing the peak-to-peak inductor current ripple to be 100% of the average:

$$\Delta I_{L(pk-pk)} = I_{L(avg)} = 5.51A \quad (16)$$

And the peak inductor current $I_{L(peak)}$ will be:

$$I_{L(peak)} = I_{L(avg)} + \frac{\Delta I_{L(pk-pk)}}{2} = 8.26A \quad (17)$$

Knowing the switching frequency, maximum duty cycle and target peak-peak ripple current, the required inductance can be calculated:

$$L_{min} = \frac{(V_{IN(min)} - V_{SW(on)}) \times D_{max}}{f_{SW} \times \Delta I_{L(pk-pk)}} = \frac{(18 - 0.5) \times 0.637}{123kHz \times 5.51} = 16.4\mu H \quad (18)$$

Off-the-shelf available inductors of 15 µH were used, resulting in slightly higher peak-peak inductor ripple current, and slightly higher inductor peak current.

8.2.2.2.2 Output Capacitor Selection

The output ripple across the boost output capacitor can be approximated from the following equation, where C_{OUT} is the value of output capacitance, and ESR is the equivalent-series-resistance of the output capacitance. For this design, the chosen electrolytic output capacitors are 150 µF with 160-mΩ ESR, so the net capacitance is 300 µF and net ESR is 80 mΩ.

$$\Delta V_{OUT} = \left[\frac{I_{OUT(max)} \times (1 - D_{min})}{2 \times f_{SW} \times C_{OUT}}\right] + \left[I_{L(peak)} \times ESR\right] = \left[\frac{4 \times (1 - 0.077)}{2 \times 123k \times 300\mu}\right] + \left[8.26 \times 0.08\right] = 711mV \quad (19)$$

This meets the target 2% specification. However, the extra ceramic output capacitors will also absorb a significant percentage of the switching frequency ripple, so the resulting output peak-to-peak ripple voltage should be lower than the value calculated above, and should be comfortably less than the 2% specification.

8.2.2.2.3 Boost MOSFET Selection

The boost MOSFET should be rated for at least the rated output voltage plus some margin for voltage ringing. A 60-V device was selected. Since the boost inductor value was chosen to achieve peak-to-peak ripple current equal to 100% of the average current, the RMS MOSFET current at maximum load and minimum Vin is:

$$I_{SW(rms)} = \sqrt{\frac{D_{max}}{3}} \times \sqrt{\Delta I_{L(pk-pk)}{}^2 + 3 \times I_{peak}{}^2 - 3 \times I_{peak} \times \Delta I_{L(pk-pk)}} = \sqrt{\frac{0.637}{3}} \times \sqrt{5.51^2 + 3 \times 8.26^2 - 3 \times 8.26 \times 5.51} = 4.57A \quad (20)$$

The chosen 60-V rated MOSFET SUD50N06-9L has 9.3-mΩ Rds(on), resulting in approximately 200-mW conduction loss.

8.2.2.2.4 Boost Diode Selection

The boost diode must have a reverse voltage rating of at least V_{OUT}, plus some margin for ringing. Thus a 60-V rated part was selected. Since fast reverse recovery is important, a Schottky device can be used at this voltage rating. A common-cathode dual-diode MBR1560 was selected, with each diode connected to one or other of the interleaved phases.

8.2.2.3 UVLO Setting

To ensure start-up below the required minimum system input voltage of 18 V, the UVLO divider resistors R6 and R8 are set to 17.4 kΩ and 2 kΩ, respectively. This sets the input UVLO turn-on level to:

$$V_{in(on)} = \frac{R6 + R8}{R8} \times V_{UVLO} = \frac{17.4 + 2}{2} \times 1.25 = 12.125V \quad (21)$$

This gives plenty margin to the required 16-V minimum. Resistor R7 in series with the UVLO pin increases the effective UVLO hysteresis.

8.2.2.4 VIN, VCC, Startup

To reduce the power dissipation in the internal startup regulator on the VIN pin, a separate external switching regulator is used. This consists of U2 (LM5009) plus associated circuitry C5, C6, R1, R2, C7, D1, L1, R3 and R4. This buck regulator is designed to generate a 10-V regulated supply voltage for the VCC of U1 LM5032. See the LM5009 device datasheet, SNVS402, for detailed design information.

Since the LM5032 internal VIN regulator is not used in this design, the LM5032 VIN and VCC pins are shorted together.

8.2.2.5 Soft-Start and Overload

Since the two soft-start pins SS1 and SS2 are connected to a single soft-start capacitor, C12, the combined charging current of both soft-start pins charges the single soft-start capacitor. The soft-start delay to commencement of first PWM switching can be calculated from:

$$t_{ss_delay} = \frac{1.5V \times C_{SS}}{100\mu A} = \frac{1.5 \times 0.1\mu F}{100\mu A} = 1.5ms \quad (22)$$

Thereafter, the soft-start ramp time will depend on the power stage design and the operating conditions (input voltage and output load).

8.2.2.6 Current Sense

In order to improve the efficiency, a lower value current sense shunt resistance is used. To enable this lower value, the normal operating range of the CS1/CS2 pins is reduced by adding an external DC offset to the CS1/CS2 pins, as shown in Figure 30.

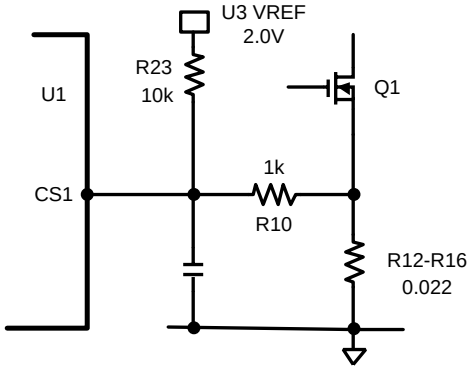

Figure 30. Current Sense DC Offset Circuit

This circuit uses the 2.048-V reference U3 to add a typical offset of 185 mV to both current-sense pins. This reduces the active range of the internal cycle-by-cycle current-limit comparator to 315 mV, allowing the current-sense shunt to be decreased to 66% of the value that would be otherwise required.

From the power stage design calculations, the peak inductor current in each power stage was approximately 9 A at max load and minimum Vin. Allowing for tolerances, and providing some margin for output overload, the current-sense shunt resistors are chosen for a peak current limit of approximately 15 A:

$$R12 / R13 = \frac{(0.5 - 0.185)V}{15A} = 21m\Omega \quad (23)$$

A standard value of 20 mΩ was used.

8.2.3 Application Curves

Figure 31 shows the measured efficiency as a function of load current and input voltage.

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Figure 32 illustrates the switching nodes of the two interleaved phases, and the resulting output ripple at twice the switching frequency. This was measured at Vin of 24 V, where duty cycle is approx. 50% and maximum ripple-cancellation occurs.

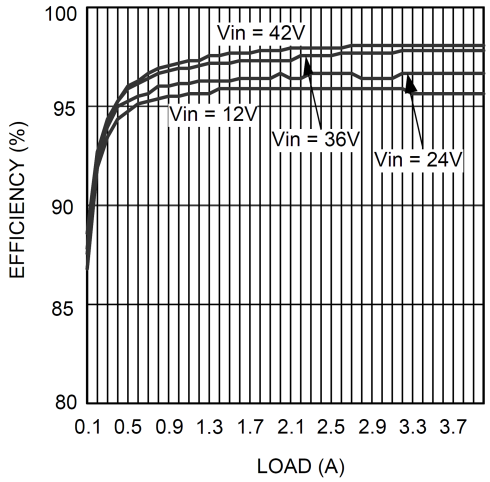

Figure 31. Efficiency vs. Load and Vin

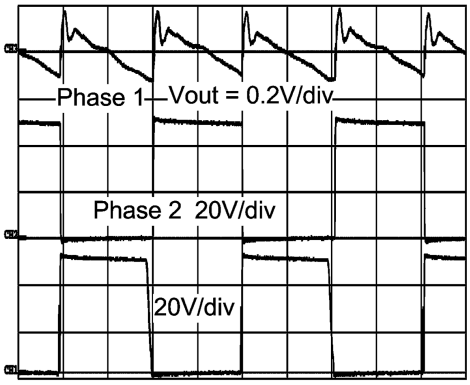

Figure 32. Output Ripple at 24-V Vin

9 Power Supply Recommendations

The VCC pin requires a local decoupling capacitor to ground for stability of the internal regulator from the VIN pin. This decoupling capacitor also provides the current pulses to drive the gates of the external MOSFETs through the driver output pins. The decoupling capacitor should be placed close to the VCC and GND1/GNS2 pins, and should be tracked directly to the pins.

The two ground pins (GND1 and GND2) must be connected together with a short direct connection.

10 Layout

10.1 Layout Guidelines

The LM5032 Current Sense and PWM comparators are very fast, and respond to short duration noise pulses. The components at the CS, COMP, SS, DCL, UVLO, and the RT/SYNC pins should be as physically close as possible to the IC, thereby minimizing noise pickup in the PC board tracks.

Layout considerations are critical for the current sense filter. If current sense transformers are used, both leads of each transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of each transformer should be connected via a dedicated PC board track to its appropriate GND pin, rather than through the ground plane.

If the current sense circuits employ sense resistors in the drive transistor sources, low inductance resistors should be used. In this case, all the noise sensitive low current ground tracks should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point). The outputs of the LM5032 should have short direct paths to the power MOSFETs in order to minimize inductance in the PC board traces.

The two ground pins (GND1, GND2) must be connected together with a short direct connection to avoid jitter due to relative ground bounce in the operation of the two regulators.

If the internal dissipation of the LM5032 produces high junction temperatures during normal operation, the use of wide PC board traces can help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

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10.2 Layout Example

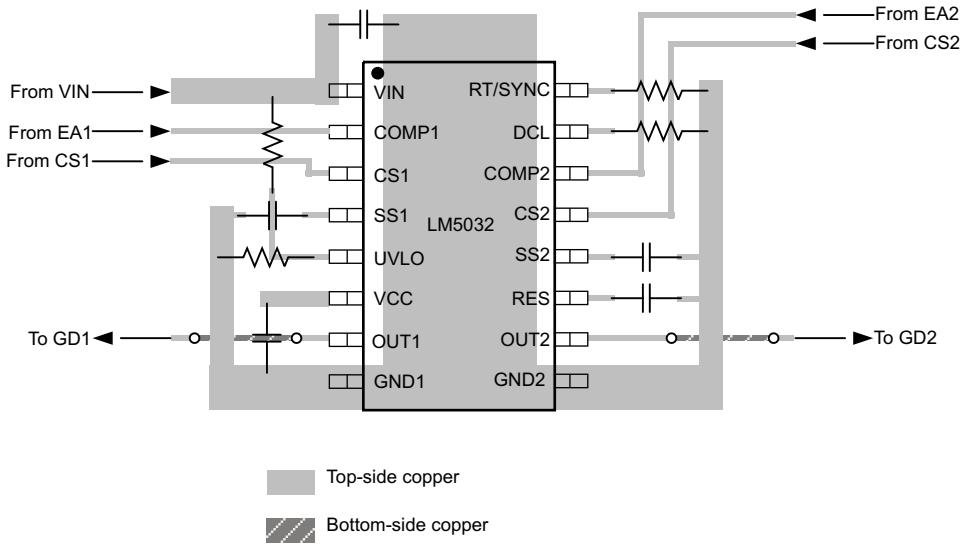

Figure 33. Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM5032MTC/NOPB	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 125	LM5032 MTC
LM5032MTCX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5032 MTC
LM5032MTCX/NOPB.A	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5032 MTC
LM5032MTCX/NOPB.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LM5032 MTC

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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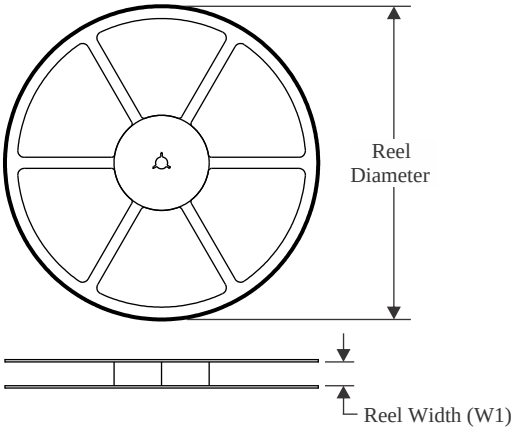
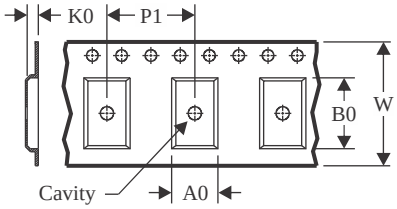
TAPE AND REEL INFORMATION

REEL DIMENSIONS

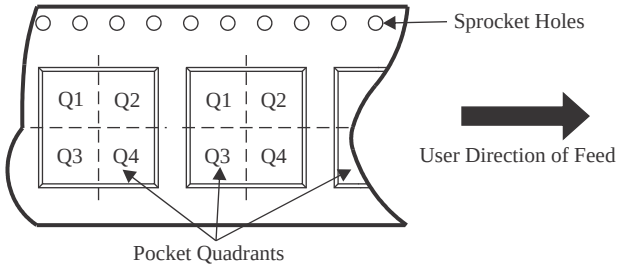


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

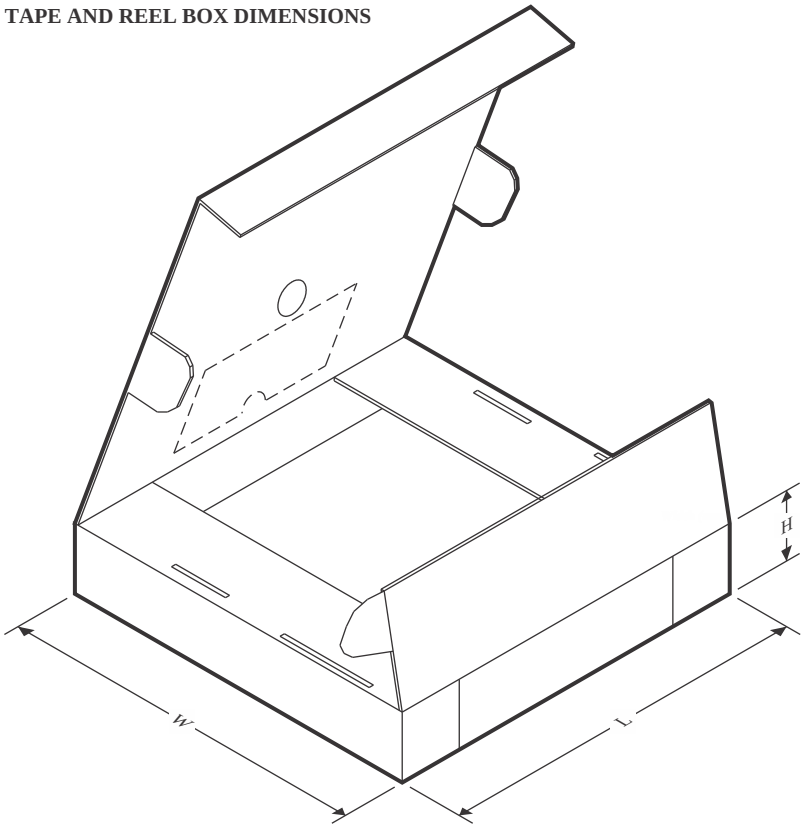
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5032MTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

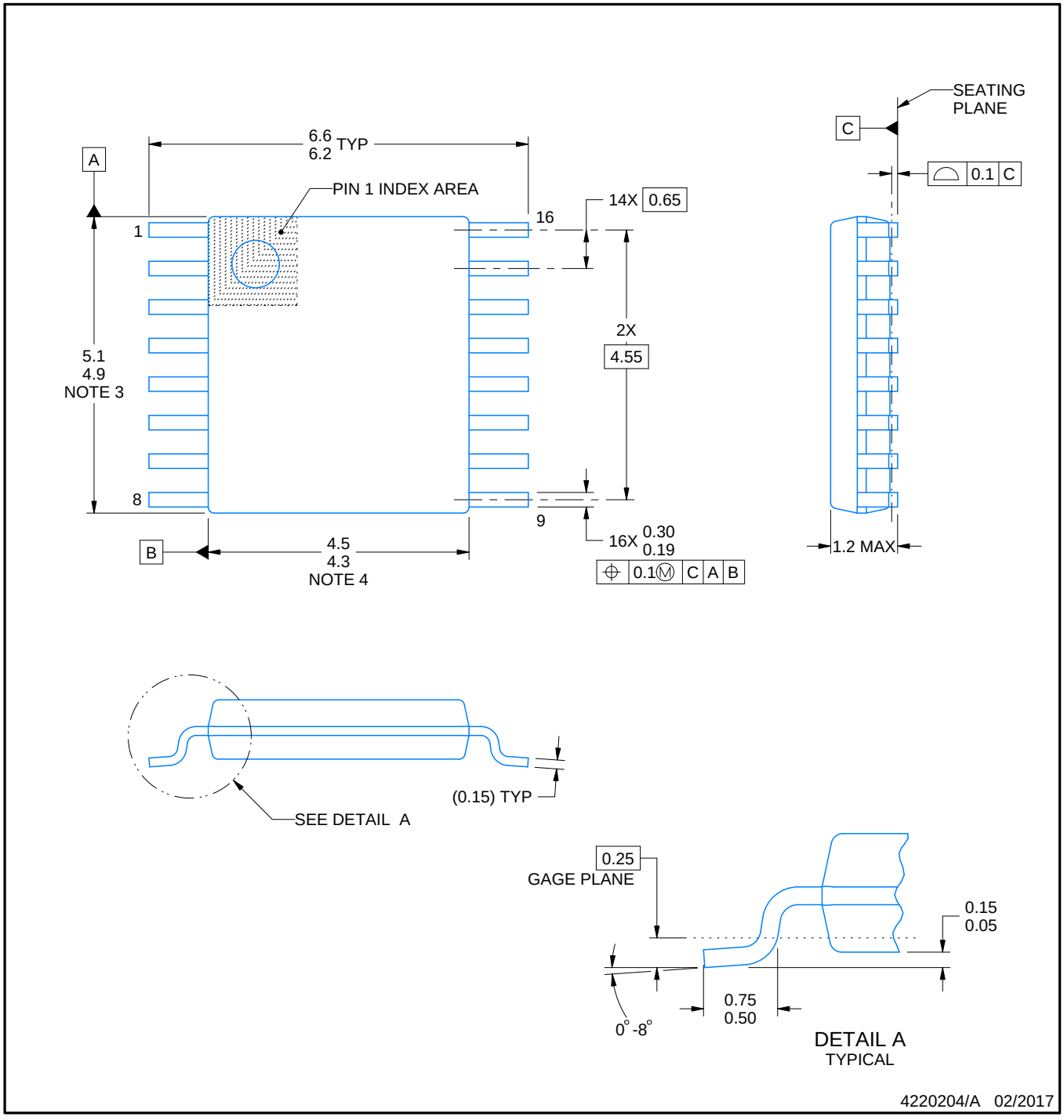
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5032MTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

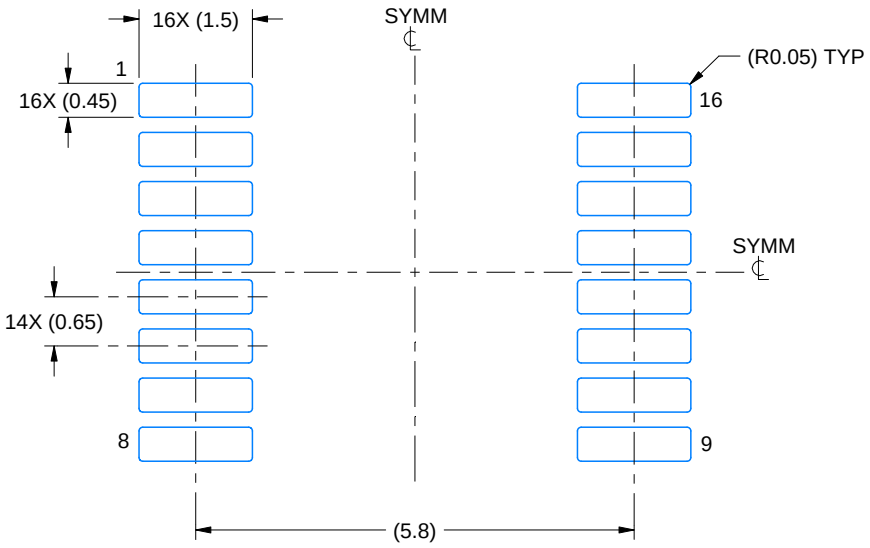
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



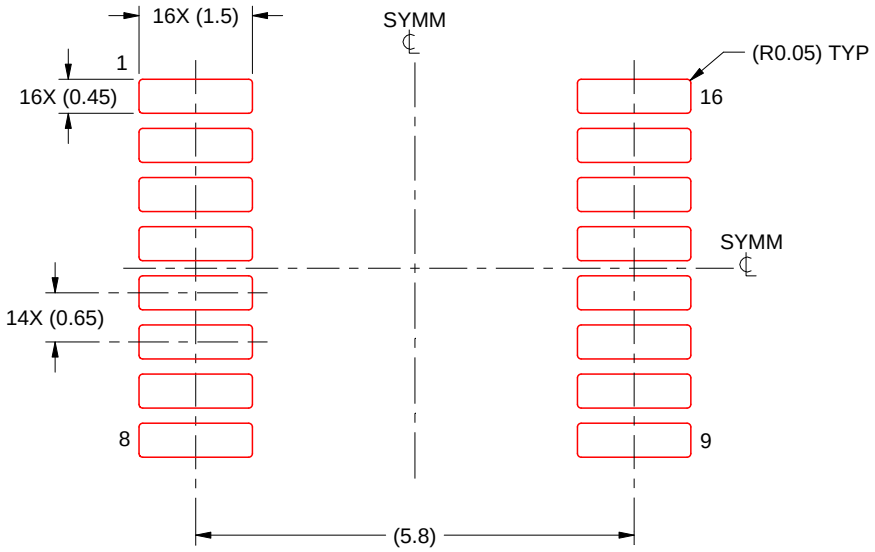
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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