SN74AC595-Q1 Automotive 8-Bit Shift Register With 3-State Output Registers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Maximum t_{pd} of 12ns at 5V, 50pF load

2 Applications

- Output expansion
- LED matrix control
- 7-segment display control

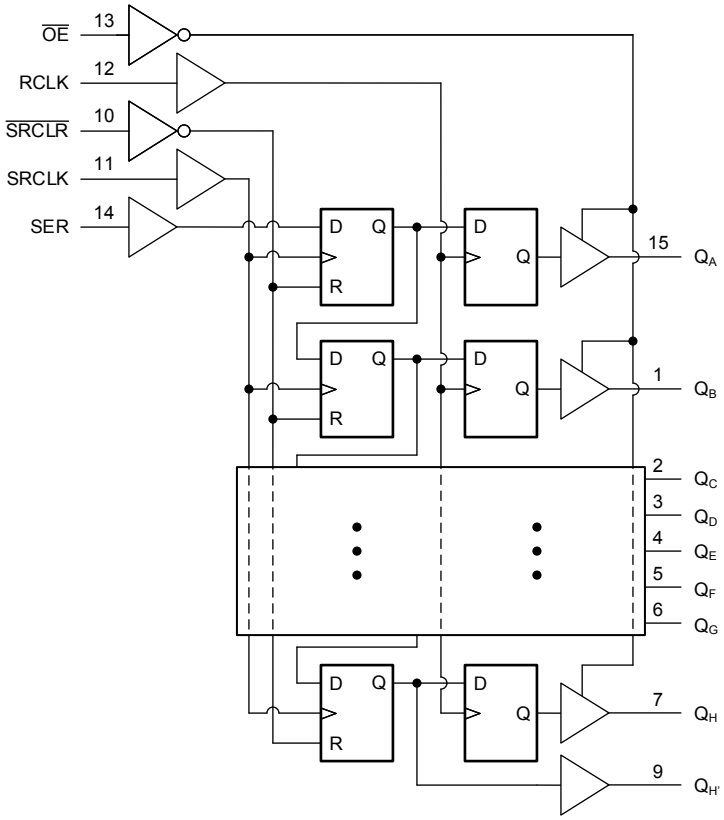
3 Description

The SN74AC595-Q1 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. This configuration allows data to be loaded into the shift register while the outputs remain static. The device includes 3-state outputs to allow for disabling the outputs. The device has a separate shift register output ($Q_{H'}$) for connecting shift registers in series.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AC595-Q1	PW (TSSOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm

(1) For more information, see Section 11.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

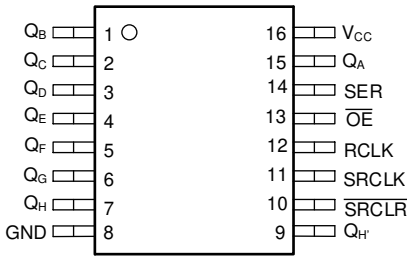

Figure 4-1. PW Package, 16-PIN TSSOP (Top View)

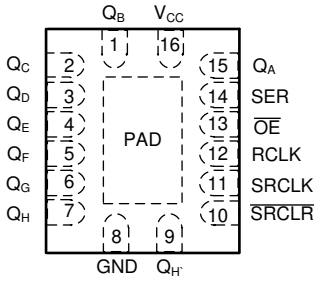

Figure 4-2. BQB Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Q_B	1	O	Storage register B output
Q_C	2	O	Storage register C output
Q_D	3	O	Storage register D output
Q_E	4	O	Storage register E output
Q_F	5	O	Storage register F output
Q_G	6	O	Storage register G output
Q_H	7	O	Storage register H output
GND	8	G	Ground
$Q_{H'}$	9	O	Shift register H output
$\overline{SRCLR}$	10	I	Shift register clear input, active low
SRCLK	11	I	Shift register clock input
RCLK	12	I	Output register clock input
$\overline{OE}$	13	I	Output enable for Q_A — Q_H outputs, active low
SER	14	I	Shift register serial data input
Q_A	15	O	Storage register A output
V_{CC}	16	P	Positive supply
Thermal pad[2]		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, G = Ground, P = Power
(2) BQB package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range[2]		-0.5	V_{CC} + 0.5 V	V
V_O	Output voltage range[2]		-0.5	V_{CC} + 0.5 V	V
I_{IK}	Input clamp current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output clamp current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous output current through V_{CC} or GND			±200	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2[1]	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordrance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage	Supply voltage	1.5	6	V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	1.2		V
		V_{CC} = 1.8 V	1.26		V
		V_{CC} = 2.5 V	1.75		V
		V_{CC} = 3 V	2.1		V
		V_{CC} = 4.5 V	3.15		V
		V_{CC} = 5.5 V	3.85		V
V_{IL}	Low-Level input voltage	V_{CC} = 1.5 V		0.3	V
		V_{CC} = 1.8 V		0.54	V
		V_{CC} = 2.5 V		0.75	
		V_{CC} = 3 V		0.9	V
		V_{CC} = 4.5 V		1.35	V
		V_{CC} = 5.5 V		1.65	V
V_I	Input Voltage	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	Output Voltage	0	V_{CC}	V

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Spec	Description	Condition	MIN	MAX	UNIT
I_{OH}	High-level output current	V_{CC} = 1.8 V		-1	mA
		V_{CC} = 2.5 V		-2	mA
		V_{CC} = 3 V		-12	mA
		V_{CC} = 4.5 V to 5.5 V		-24	mA
I_{OL}	Low-level output current	V_{CC} = 1.8 V		1	mA
		V_{CC} = 2.5 V		2	mA
		V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V to 5.5 V		24	mA
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.5 V to 3 V		50	ns/V
		V_{CC} = 3.6 V to 5.5 V		20	ns/V
T_A	Operating free-air temperature	Operating free-air temperature	-40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		BQB (WQFN)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.9	126.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.6	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.6	84.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.6	7.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.5	83.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	31.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = -50 µA	1.5 V	1.4	1.49		1.4			1.4			V
		1.8 V	1.7	1.79		1.7			1.7			
		2.5 V	2.4	2.49		2.4			2.4			
		3 V	2.9	2.99		2.9			2.9			
		4.5 V	4.4	4.49		4.4			4.4			
		5.5 V	5.4	5.49		5.4			5.4			
	I_{OH} = -1 mA	1.8 V	1.53			1.5			1.44			
	I_{OH} = -2 mA	2.5 V	2.13			2.1			2			
	I_{OH} = -4 mA	3 V	2.58			2.48			2.4			
	I_{OH} = -12 mA	3 V	2.58			2.48			2.4			
	I_{OH} = -24 mA	4.5 V	3.94			3.8			3.7			
	I_{OH} = -24 mA	5.5 V	4.94			4.8			4.7			
	I_{OH} = -50 mA[1]	5.5 V				3.85						
	I_{OH} = -75 mA[1]	5.5 V							3.85			

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5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	I_{OL} = 50 µA	1.5 V		0.01	0.1			0.1			0.1	V
		1.8 V		0.01	0.1			0.1			0.1	
		2.5 V		0.01	0.1			0.1			0.1	
		3 V		0.01	0.1			0.1			0.1	
		4.5 V		0.01	0.1			0.1			0.1	
		5.5 V		0.01	0.1			0.1			0.1	
	I_{OL} = 1 mA	1.8 V			0.2			0.3			0.36	
	I_{OL} = 2 mA	2.5 V			0.36			0.44			0.5	
	I_{OL} = 4 mA	3 V			0.36			0.44			0.5	
	I_{OL} = 12 mA	3 V			0.36			0.44			0.5	
	I_{OL} = 24 mA	4.5 V			0.36			0.44			0.5	
	I_{OL} = 24 mA	5.5 V			0.36			0.44			0.5	
	I_{OL} = 50 mA(1)	5.5 V						1.65				
	I_{OL} = 75 mA(1)	5.5 V									1.65	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1			±1			±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.25			±2.5			±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			2			20			20	µA
C_I	V_I = V_{CC} or GND	5 V		9			9			9		pF
C_O	V_O = V_{CC} or GND	5 V		15			15			15		pF
C_{PD}	C_L = 50 pF, F = 1 MHz	5 V		60			60			60		pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{CLOCK}	Clock frequency		1.5 V						20	MHz
			1.8 V						25	MHz
			2.5 V						50	MHz
			3.3 V						55	MHz
			5 V						90	MHz

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5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	T_A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	RCLK or SRCLK high or low	1.5 V					13		ns
			1.8 V					8		ns
			2.5 V					6		ns
			3.3 V					4		ns
			5 V					2		ns
		$\overline{SRCLR}$ low	1.5 V					7		ns
			1.8 V					6		ns
			2.5 V					4		ns
			3.3 V					3		ns
			5 V					2		ns
t_{SU}	Setup time	SER before SRCLK↑	1.5 V					8		ns
			1.8 V					5		ns
			2.5 V					3		ns
			3.3 V					2		ns
			5 V					1		ns
		SRCLK↑ before RCLK↑	1.5 V					25		ns
			1.8 V					15		ns
			2.5 V					9		ns
			3.3 V					6		ns
			5 V					4		ns
		$\overline{SRCLR}$ low before RCLK↑	1.5 V					17		ns
			1.8 V					11		ns
			2.5 V					7		ns
			3.3 V					5		ns
			5 V					3		ns
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	1.5 V					2		ns
			1.8 V					1		ns
			2.5 V					1		ns
			3.3 V					1		ns
			5 V					1		ns
t_H	Hold time	SER after SRCLK↑	1.5 V					7		ns
			1.8 V					4		ns
			2.5 V					3		ns
			3.3 V					2		ns
			5 V					2		ns

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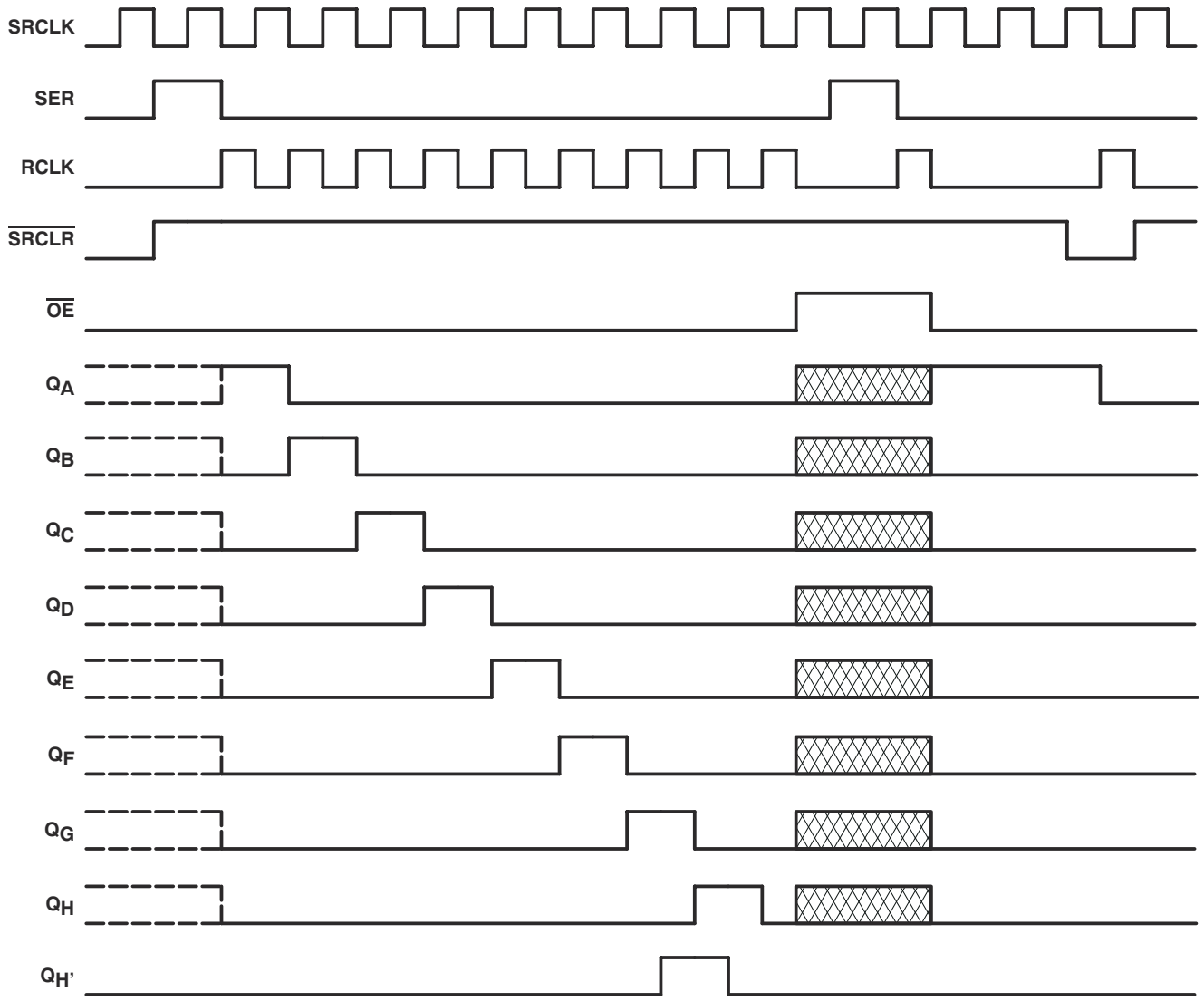
5.7 Timing Diagrams



NOTE: implies that the output is in 3-State mode.

5.8 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZL}	$\overline{OE}$	Q	1.5 V									58	ns
t_{PZH}	$\overline{OE}$	Q	1.5 V									54	ns
t_{PLZ}	$\overline{OE}$	Q	1.5 V									42	ns
t_{PHZ}	$\overline{OE}$	Q	1.5 V									50	ns
t_{PLH}	RCLK	Q_A-Q_H	1.5 V									60	ns
t_{PHL}	RCLK	Q_A-Q_H	1.5 V									60	ns
t_{PLH}	SRCLK	$Q_{H'}$	1.5 V									64	ns
t_{PHL}	SRCLK	$Q_{H'}$	1.5 V									63	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	1.5 V									51	ns
t_{PZL}	$\overline{OE}$	Q	1.8 V									38	ns

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5.8 Switching Characteristics (continued)

C_L = 50 pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PZH}	$\overline{OE}$	Q	1.8 V									35	ns
t_{PLZ}	$\overline{OE}$	Q	1.8 V									27	ns
t_{PHZ}	$\overline{OE}$	Q	1.8 V									32	ns
t_{PLH}	RCLK	Q_A-Q_H	1.8 V									37	ns
t_{PHL}	RCLK	Q_A-Q_H	1.8 V									38	ns
t_{PLH}	SRCLK	$Q_{H'}$	1.8 V									39	ns
t_{PHL}	SRCLK	$Q_{H'}$	1.8 V									39	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	1.8 V									34	ns
t_{PZL}	$\overline{OE}$	Q	2.5 V									24	ns
t_{PZH}	$\overline{OE}$	Q	2.5 V									22	ns
t_{PLZ}	$\overline{OE}$	Q	2.5 V									13	ns
t_{PHZ}	$\overline{OE}$	Q	2.5 V									16	ns
t_{PLH}	RCLK	Q_A-Q_H	2.5 V									21	ns
t_{PHL}	RCLK	Q_A-Q_H	2.5 V									21	ns
t_{PLH}	SRCLK	$Q_{H'}$	2.5 V									22	ns
t_{PHL}	SRCLK	$Q_{H'}$	2.5 V									22	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	2.5 V									20	ns
t_{PZL}	$\overline{OE}$	Q	3.3 V									19	ns
t_{PZH}	$\overline{OE}$	Q	3.3 V									17	ns
t_{PLZ}	$\overline{OE}$	Q	3.3 V									10	ns
t_{PHZ}	$\overline{OE}$	Q	3.3 V									12	ns
t_{PLH}	RCLK	Q_A-Q_H	3.3 V									17	ns
t_{PHL}	RCLK	Q_A-Q_H	3.3 V									17	ns
t_{PLH}	SRCLK	$Q_{H'}$	3.3 V									18	ns
t_{PHL}	SRCLK	$Q_{H'}$	3.3 V									18	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	3.3 V									16	ns
t_{PZL}	$\overline{OE}$	Q	5 V									13	ns
t_{PZH}	$\overline{OE}$	Q	5 V									12	ns
t_{PLZ}	$\overline{OE}$	Q	5 V									6	ns
t_{PHZ}	$\overline{OE}$	Q	5 V									8	ns
t_{PLH}	RCLK	Q_A-Q_H	5 V									12	ns
t_{PHL}	RCLK	Q_A-Q_H	5 V									11	ns
t_{PLH}	SRCLK	$Q_{H'}$	5 V									12	ns
t_{PHL}	SRCLK	$Q_{H'}$	5 V									12	ns
t_{PHL}	$\overline{SRCLR}$	$Q_{H'}$	5 V									11	ns

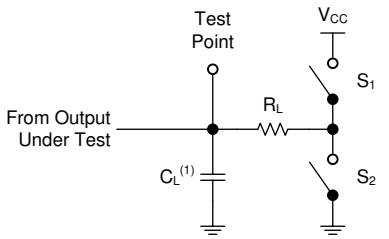
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

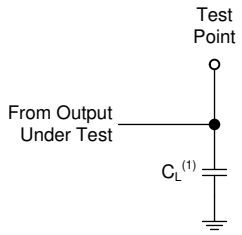
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH}, t_{PHL}	OPEN	OPEN	—	2.5ns	—	ALL
t_{PLZ}, t_{PZL}	CLOSED	OPEN	500Ω	2.5ns	0.15V	≤ 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	500Ω	2.5ns	0.15V	≤ 2.5V
t_{PLZ}, t_{PZL}	CLOSED	OPEN	500Ω	2.5ns	0.3V	> 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	500Ω	2.5ns	0.3V	> 2.5V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

Figure 6-2. Load Circuit for Push-Pull Outputs

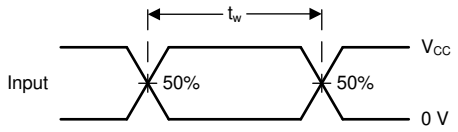


Figure 6-3. Voltage Waveforms, Pulse Duration

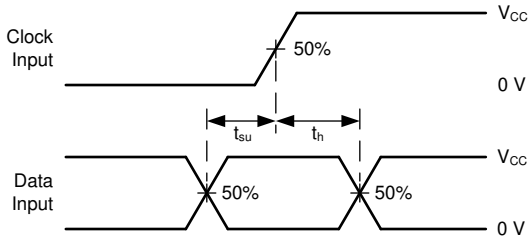
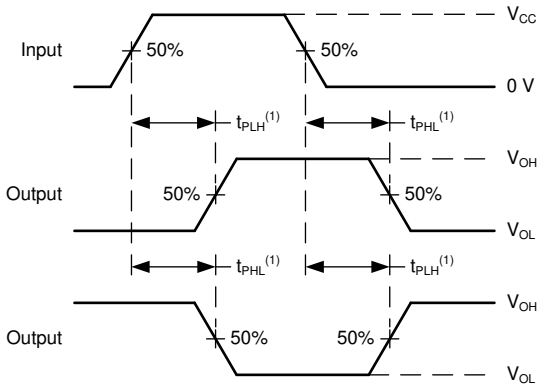
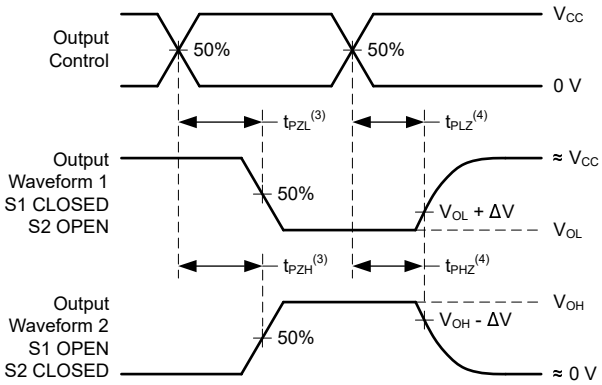


Figure 6-4. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-5. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-6. Voltage Waveforms Propagation Delays

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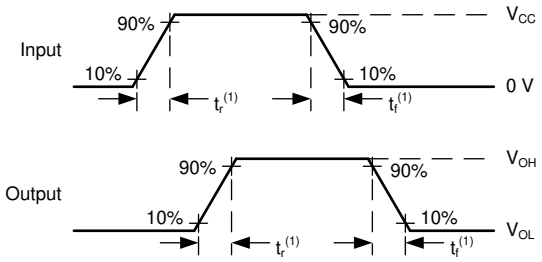

(1) The greater between t_r and t_f is the same as t_t.

Figure 6-7. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74AC595-Q1 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 parallel 3-state outputs. Separate clocks are provided for both the shift (SRCLK) and storage (RCLK) registers.

The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and a serial output ($Q_{H'}$) for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs, except $Q_{H'}$, are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered.

If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register. In this configuration, it takes 8 clock pulses to load data into all 8 registers, and 9 clock pulses for the outputs to display that data.

7.2 Functional Block Diagram

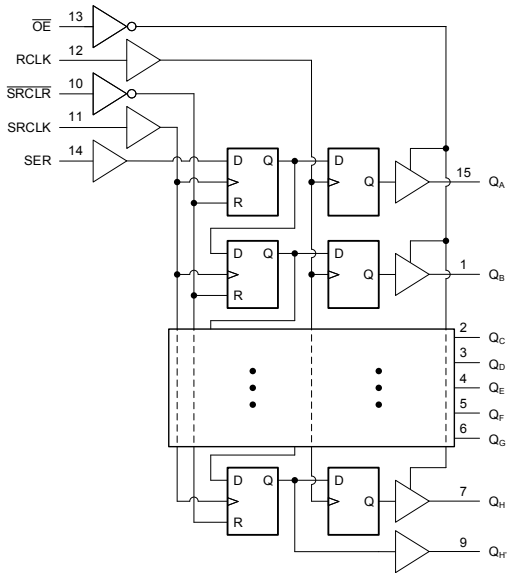

Figure 7-1. Logic Diagram (Positive Logic)

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7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	L, H, ↓	H	X	X	Shift register data remains constant.
X	X	X	L, H, ↓	X	Storage register data remains constant.
X	X	X	X	H	Outputs Q_A–Q_H are disabled.
X	X	X	X	L	Outputs Q_A–Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Each subsequent stage stores the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Each subsequent stage stores the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74AC595-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74AC595-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The OE pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74AC595-Q1 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74AC595-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register. An RC circuit can be connected to the $\overline{\text{SRCLR}}$ pin as shown in the Figure 8-1 to initialize the shift register to all zeros. With the $\overline{\text{OE}}$ pin pulled up with a resistor, this process can be performed while the outputs are in a high impedance state eliminating any erroneous data causing issues with the displays.

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8.2 Typical Application

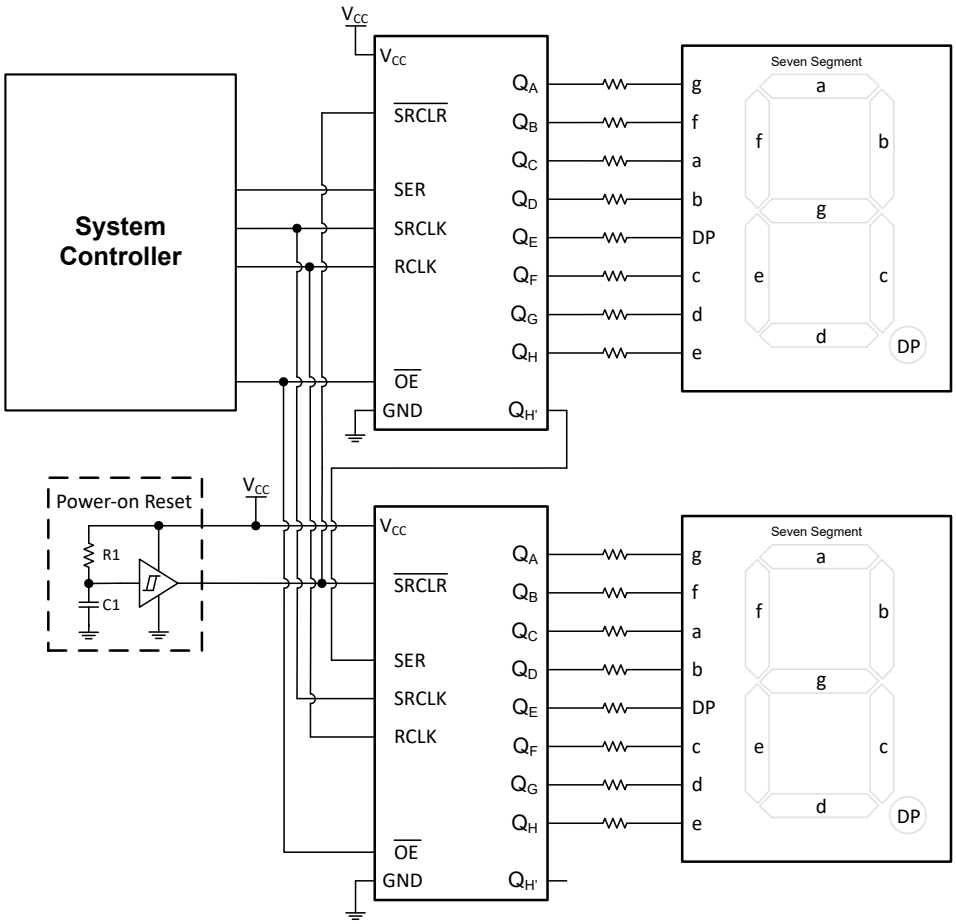

Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC595-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC595-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC595-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AC595-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC595-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74AC595-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AC595-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.3 Application Curves

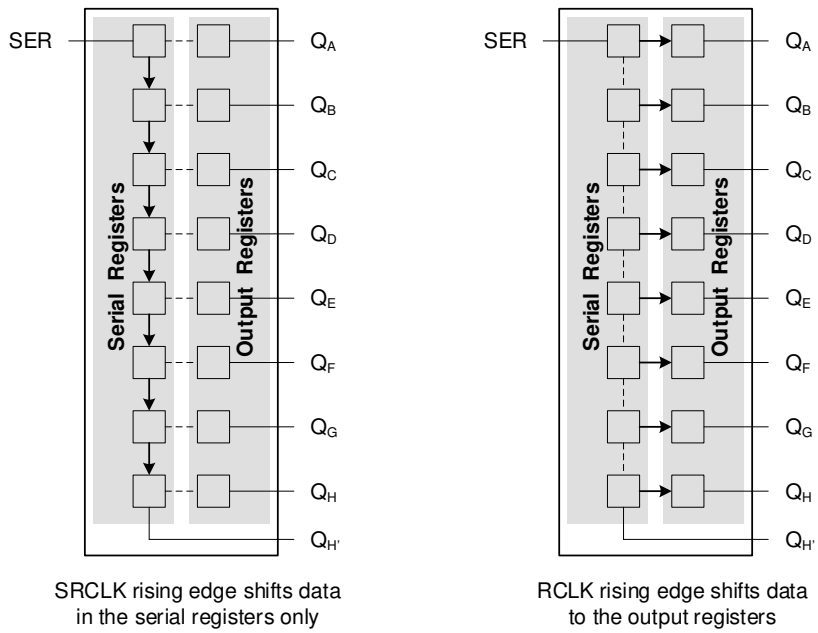

Figure 8-2. Simplified Functional Diagram Showing Clock Operation

8.4 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

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8.5 Layout

8.5.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.5.2 Layout Example

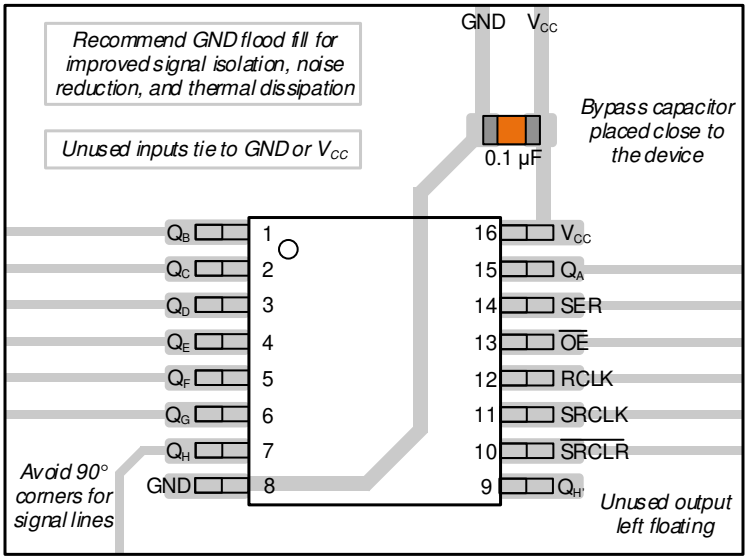

Figure 8-3. Example Layout for the SN74AC595-Q1

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9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2024) to Revision A (April 2024)	Page
• Changed the status from: *Advanced Information* to: *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN74AC595PWRQ1.A	Active	Preproduction	TSSOP (PW) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
SN74AC595PWRQ1	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC595Q
SN74AC595PWRQ1.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC595Q
SN74AC595WBQBRQ1	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC595Q
SN74AC595WBQBRQ1.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC595Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AC595-Q1 :

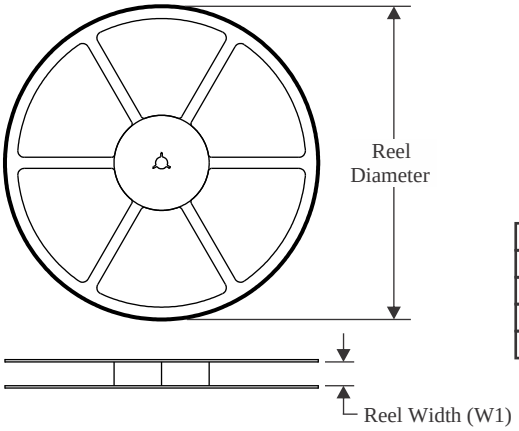
- Catalog : SN74AC595

NOTE: Qualified Version Definitions:

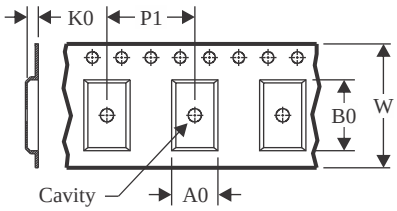
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

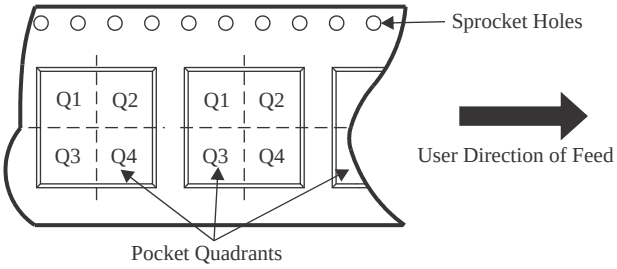


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

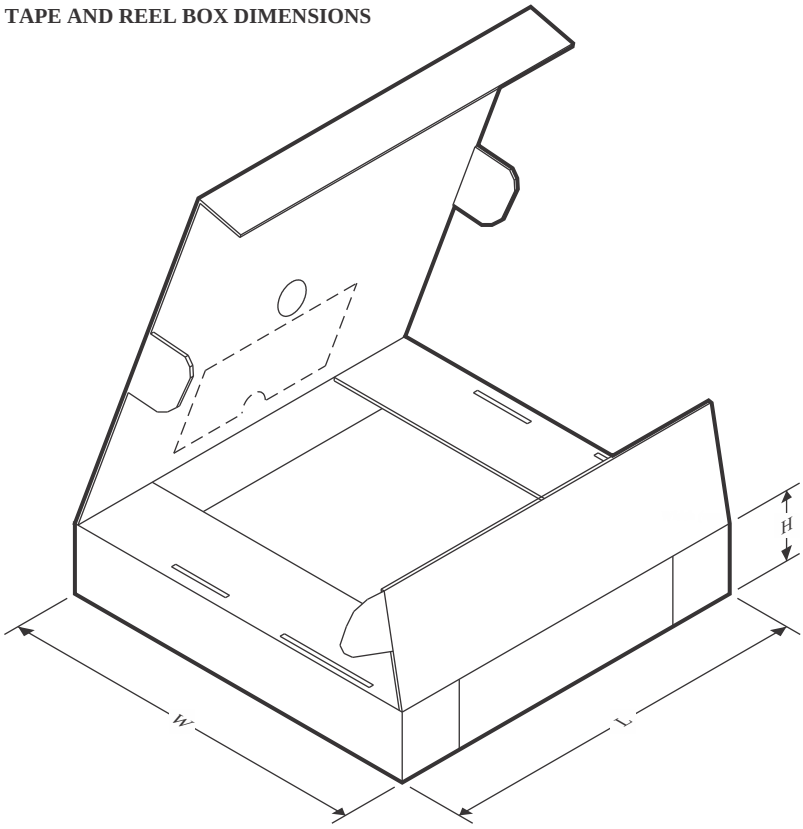
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC595PWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC595WBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC595PWRQ1	TSSOP	PW	16	3000	353.0	353.0	32.0
SN74AC595WBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

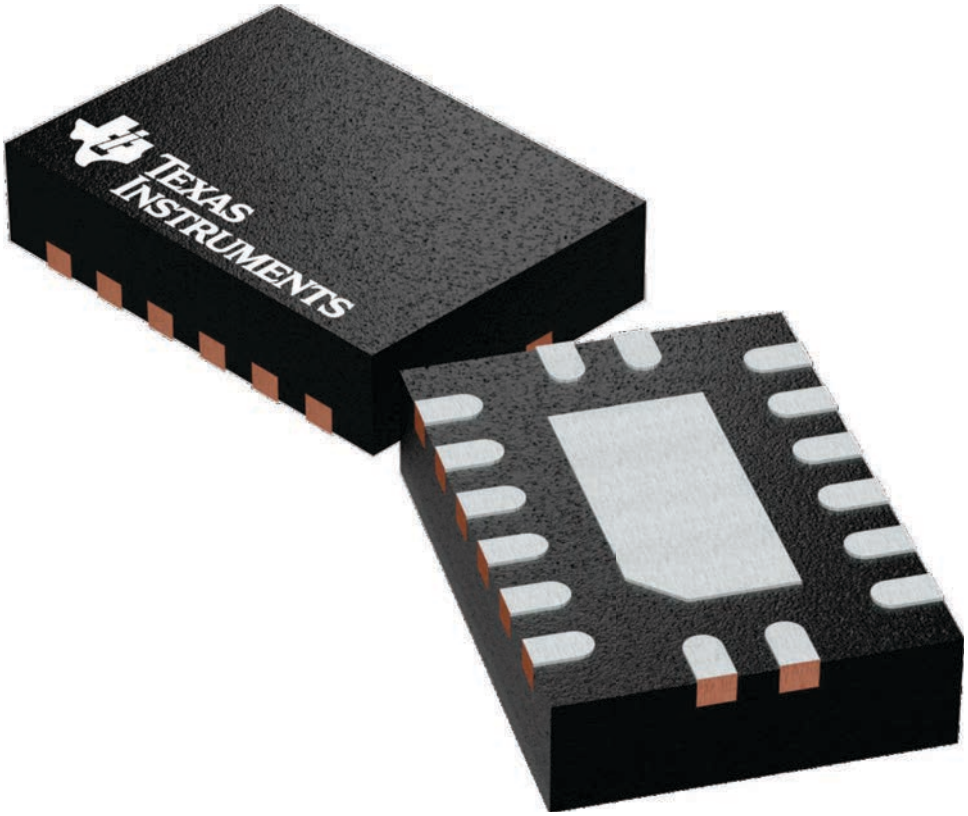
BQB 16

WQFN - 0.8 mm max height

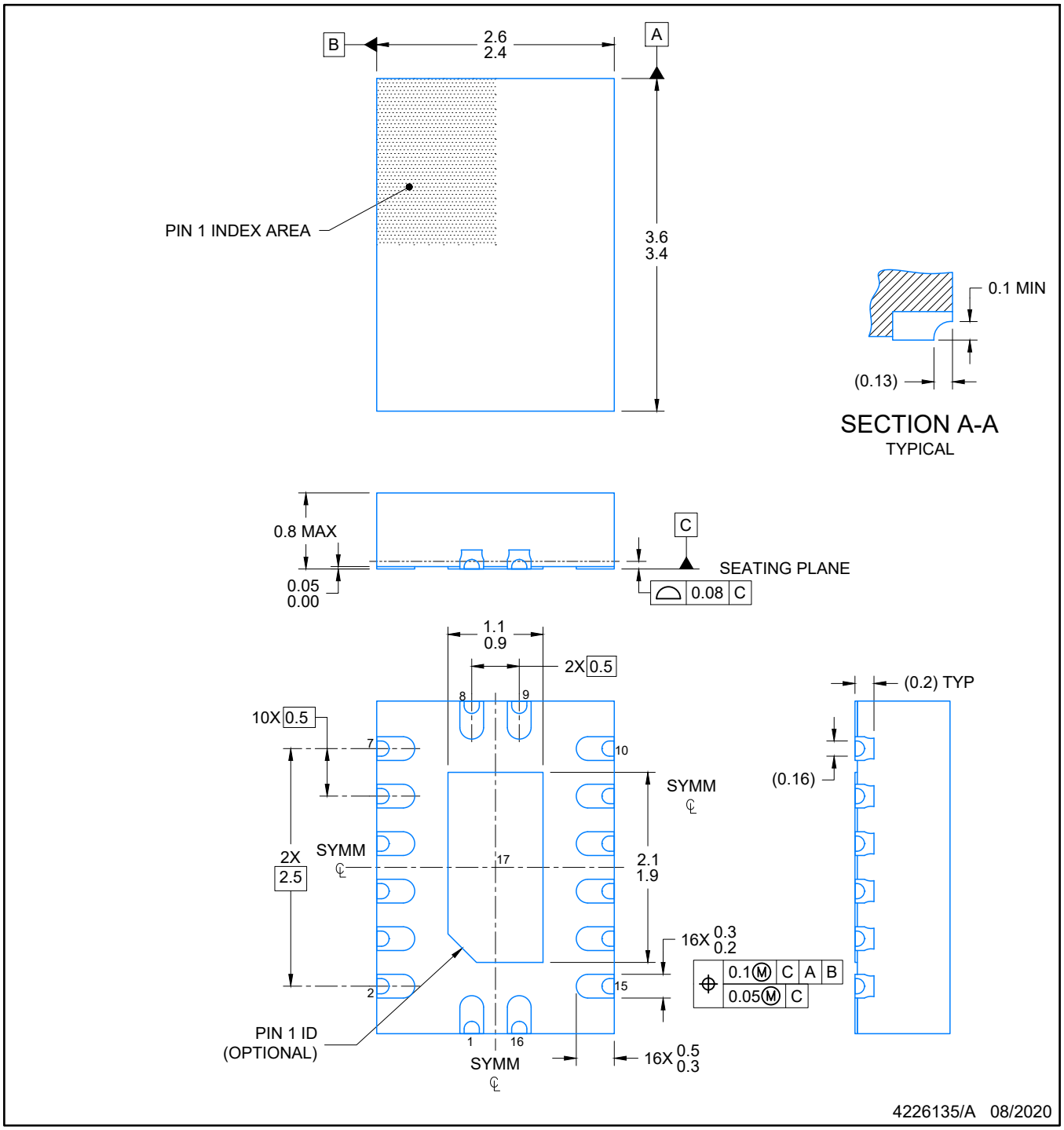
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

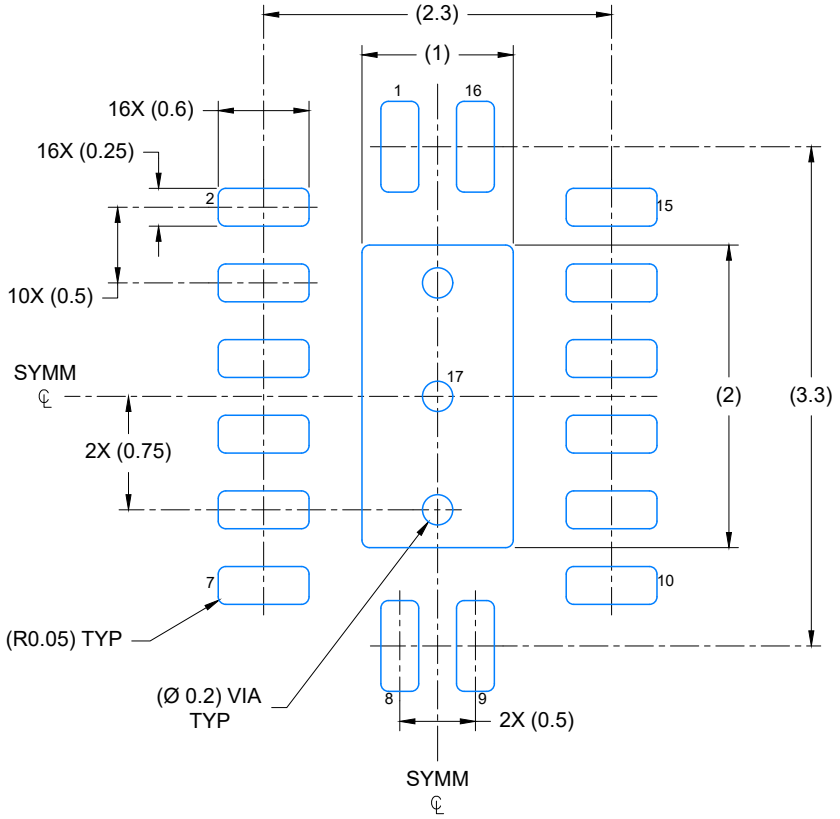


4226161/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

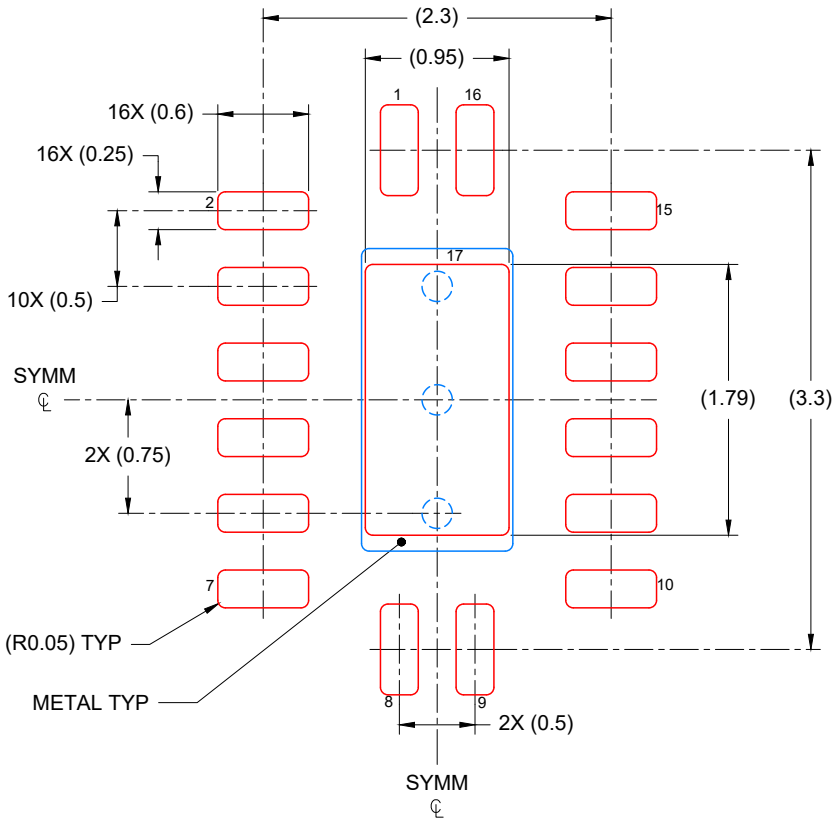


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

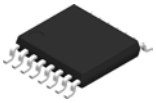
EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

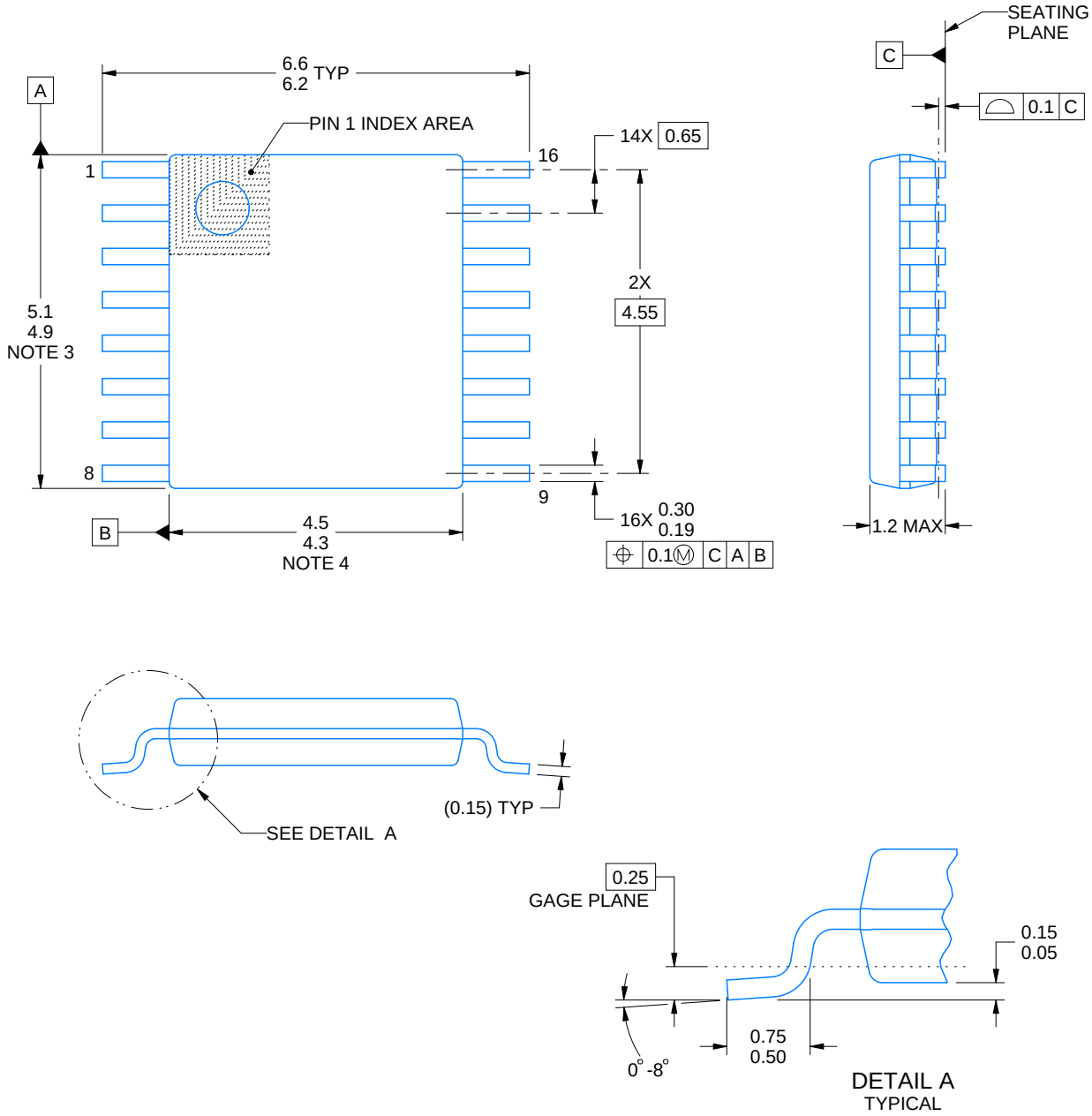
PW0016A



PACKAGE OUTLINE

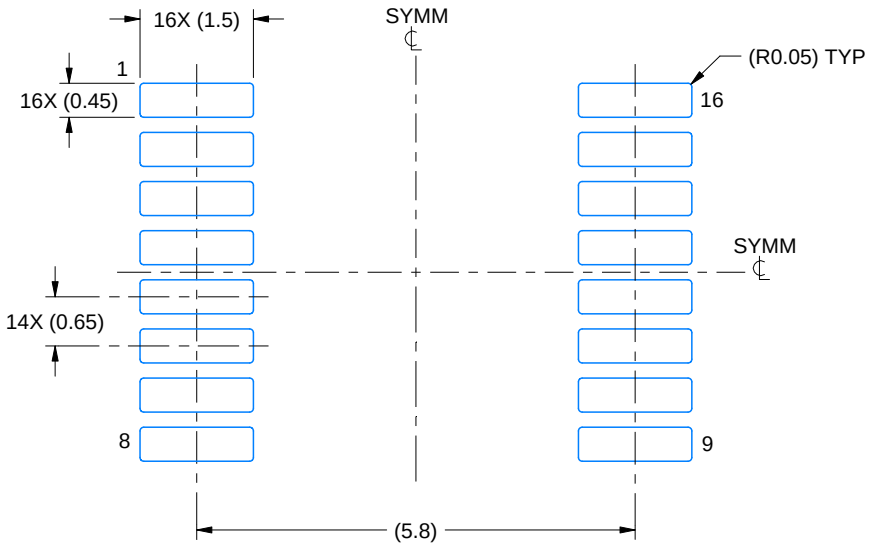
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

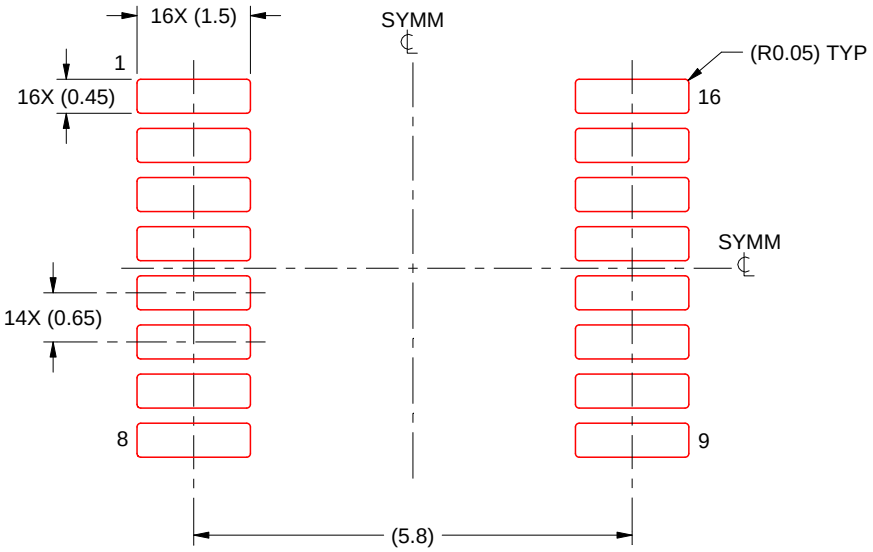
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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