16-Bit, 400-kSPS, Serial Interface, microPower, Miniature, True-Differential Input, SAR Analog-to-Digital Converter

Check for Samples: ADS8865

FEATURES

- **Sample Rate: 400 kHz**
- **No Latency Output**
- **Unipolar, True-Differential Input Range: $-V_{REF}$ to $+V_{REF}$**
- **Wide Common-Mode Voltage Range: 0 V to V_{REF} with 90-dB CMRR (min)**
- **SPI™-Compatible Serial Interface with Daisy-Chain Option**
- **Excellent AC and DC Performance:**
  - **SNR: 96 dB, THD: –115 dB**
  - **INL: ±1.0 LSB (max)**
  - **DNL: ±1.0 LSB (max), 16-Bit NMC**
- **Wide Operating Range:**
  - **AVDD: 2.7 V to 3.6 V**
  - **DVDD: 1.65 V to 3.6 V (Independent of AVDD)**
  - **REF: 2.5 V to 5 V (Independent of AVDD)**
  - **Operating Temperature: –40°C to +85°C**
- **Low-Power Dissipation:**
  - **2.6 mW at 400 kSPS**
  - **0.65 mW at 100 kSPS**
  - **65 µW at 10 kSPS**
- **Power-Down Current (AVDD): 50 nA**
- **Full-Scale Step Settling to 16 Bits: 1200 ns**
- **Packages: MSOP-10 and SON-10**

APPLICATIONS

- **Automatic Test Equipment (ATE)**
- **Instrumentation and Process Controls**
- **Precision Medical Equipment**
- **Low-Power, Battery-Operated Instruments**

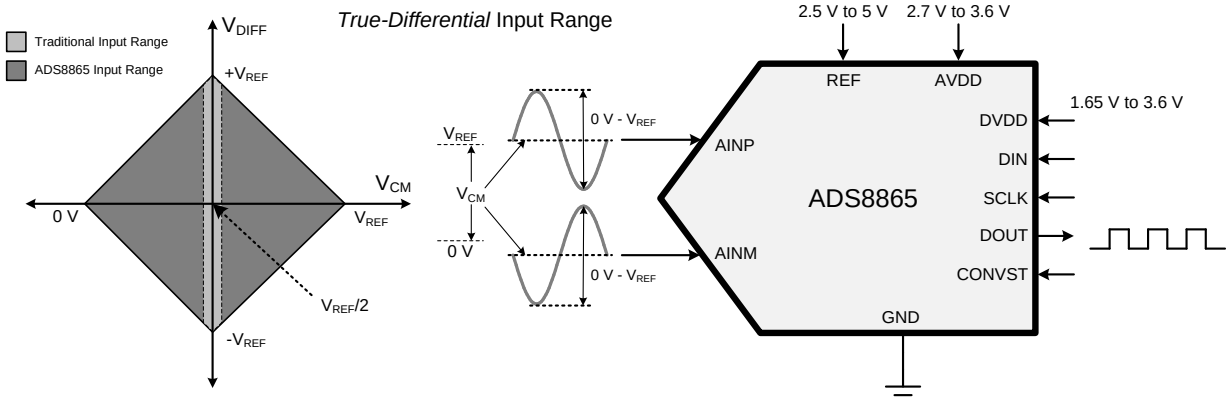
DESCRIPTION

The ADS8865 is a 16-bit, 400-kSPS, true-differential input, analog-to-digital converter (ADC). The device operates with a 2.5-V to 5-V external reference, offering a wide selection of signal ranges without additional input signal scaling. The reference voltage setting is independent of, and can exceed, the analog supply voltage (AVDD).

The device offers an SPI-compatible serial interface that also supports daisy-chain operation for cascading multiple devices. An optional busy-indicator bit makes synchronizing with the digital host easy.

The device supports unipolar, true-differential analog input signals with a differential input swing of $-V_{REF}$ to $+V_{REF}$. This true-differential analog input structure allows for a common-mode voltage of any value in the range of 0 V to $+V_{REF}$ (when both inputs are within the operating input range of –0.1 V to V_{REF} + 0.1 V).

Device operation is optimized for very low-power operation. Power consumption directly scales with speed. This feature makes the ADS8865 excellent for lower-speed applications.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FAMILY INFORMATION(1)

THROUGHPUT	18-BIT, TRUE-DIFFERENTIAL	16-BIT, SINGLE-ENDED	16-BIT, TRUE-DIFFERENTIAL
100 kSPS	ADS8887	ADS8866	ADS8867
250 kSPS	—	—	—
400 kSPS	ADS8885	ADS8864	ADS8865
500 kSPS	—	ADS8319(2)	ADS8318(2)
680 kSPS	ADS8883	ADS8862	ADS8863
1 MSPS	ADS8881	ADS8860	ADS8861

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Pin-to-pin compatible device with AVDD = 5 V.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VALUE		UNIT
	MIN	MAX	
AINP to GND or AINN to GND	–0.3	REF + 0.3	V
AVDD to GND or DVDD to GND	–0.3	4	V
REF to GND	–0.3	5.7	V
Digital input voltage to GND	–0.3	DVDD + 0.3	V
Digital output to GND	–0.3	DVDD + 0.3	V
Operating temperature range, T_A	–40	+85	°C
Storage temperature range, T_{stg}	–65	+150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *electrical characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS8865		UNITS
		DGS	DRC	
		10 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	151.9	111.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	45.4	46.4	
θ_{JB}	Junction-to-board thermal resistance	72.2	45.9	
ψ_{JT}	Junction-to-top characterization parameter	3.3	3.5	
ψ_{JB}	Junction-to-board characterization parameter	70.9	45.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

All minimum and maximum specifications are at T_A = –40°C to +85°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, V_{CM} = V_{REF} / 2 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.
Typical specifications are at T_A = +25°C, AVDD = 3 V, and DVDD = 3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input span (1) (2)	AINP – AINN	$–V_{REF}$		V_{REF}	V
	Operating input range (1) (2)	AINP	–0.1		V_{REF} + 0.1	V
		AINN	–0.1		V_{REF} + 0.1	V
V_{CM}	Input common-mode range		0	V_{REF} / 2	V_{REF}	V
C_I	Input capacitance	AINP and AINN terminal to GND		59		pF
	Input leakage current	During acquisition for dc input		5		nA
SYSTEM PERFORMANCE						
	Resolution			16		Bits
NMC	No missing codes		16			Bits
DNL	Differential linearity		–0.99	±0.5	1	LSB (3)
INL	Integral linearity (4)		–1	±0.5	1	LSB (3)
E_O	Offset error (5)		–4	±1	4	mV
	Offset error drift with temperature			±1.5		µV/°C
E_G	Gain error		–0.01	±0.005	0.01	%FSR
	Gain error drift with temperature			±0.15		ppm/°C
CMRR	Common-mode rejection ratio	With common-mode input signal = 5 V_{PP} at dc	90	100		dB
PSRR	Power-supply rejection ratio	At mid-code		80		dB
	Transition noise			0.35		LSB
SAMPLING DYNAMICS						
t_{conv}	Conversion time		500		1300	ns
t_{ACQ}	Acquisition time		1200			ns
	Maximum throughput rate with or without latency				400	kHz
	Aperture delay			4		ns
	Aperture jitter, RMS			5		ps
	Step response	Settling to 16-bit accuracy		1200		ns
	Overvoltage recovery	Settling to 16-bit accuracy		1200		ns

(1) Ideal input span, does not include gain or offset error.
(2) Specified for V_{CM} = V_{REF} / 2. Refer to the *Analog Input* section for the effect of V_{CM} on the full-scale input range.
(3) LSB = least significant bit.
(4) This parameter is the endpoint INL, not best-fit.
(5) Measured relative to actual measured reference.

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ELECTRICAL CHARACTERISTICS (continued)

All minimum and maximum specifications are at T_A = –40°C to +85°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, V_{CM} = V_{REF} / 2 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.
Typical specifications are at T_A = +25°C, AVDD = 3 V, and DVDD = 3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
SINAD	Signal-to-noise + distortion(6)		At 1 kHz, V_{REF} = 5 V	95	96.4		dB
			At 10 kHz, V_{REF} = 5 V		95.4		dB
			At 100 kHz, V_{REF} = 5 V		91.6		dB
SNR	Signal-to-noise ratio(6)		At 1 kHz, V_{REF} = 5 V	95.1	96.5		dB
			At 10 kHz, V_{REF} = 5 V		95.5		dB
			At 100 kHz, V_{REF} = 5 V		92		dB
THD	Total harmonic distortion(6)(7)		At 1 kHz, V_{REF} = 5 V		–112		dB
			At 10 kHz, V_{REF} = 5 V		–112		dB
			At , V_{REF} = 5 V		-102		dB
SFDR	Spurious-free dynamic range(6)		At 1 kHz, V_{REF} = 5 V		112		dB
			At 10 kHz, V_{REF} = 5 V		112		dB
			At 100 kHz, V_{REF} = 5 V		102		dB
BW_{-3dB}	–3-dB small-signal bandwidth				30		MHz
EXTERNAL REFERENCE INPUT							
V_{REF}	Input range			2.5		5	V
	Reference input current		During conversion, 400-kHz sample rate, mid-code		100		µA
	Reference leakage current				250		nA
C_{REF}	Decoupling capacitor at the REF input			10	22		µF
POWER-SUPPLY REQUIREMENTS							
	Power-supply voltage	AVDD	Analog supply	2.7	3	3.6	V
		DVDD	Digital supply range	1.65	1.8	3.6	V
	Supply current	AVDD	400-kHz sample rate, AVDD = 3 V		0.85	1.2	mA
P_{VA}	Power dissipation		400-kHz sample rate, AVDD = 3 V		2.6	3.6	mW
			100-kHz sample rate, AVDD = 3 V		0.65		mW
			10-kHz sample rate, AVDD = 3 V		65		µW
IA_{PD}	Device power-down current(8)				50		nA
DIGITAL INPUTS: LOGIC FAMILY (CMOS)							
V_{IH}	High-level input voltage		1.65 V < DVDD < 2.3 V	0.8 × DVDD		DVDD + 0.3	V
			2.3 V < DVDD < 3.6 V	0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		1.65 V < DVDD < 2.3 V	–0.3		0.2 × DVDD	V
			2.3 V < DVDD < 3.6 V	–0.3		0.3 × DVDD	V
I_{LK}	Digital input leakage current				±10	±100	nA
DIGITAL OUTPUTS: LOGIC FAMILY (CMOS)							
V_{OH}	High-level output voltage		I_O = 500-µA source, C_{LOAD} = 20 pF	0.8 × DVDD		DVDD	V
V_{OL}	Low-level output voltage		I_O = 500-µA sink, C_{LOAD} = 20 pF	0		0.2 × DVDD	V
TEMPERATURE RANGE							
T_A	Operating free-air temperature			–40		+85	°C

(6) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(7) Calculated on the first nine harmonics of the input frequency.
(8) The device automatically enters a power-down state at the end of every conversion, and remains in power-down during the acquisition phase.

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TIMING CHARACTERISTICS

3-WIRE OPERATION

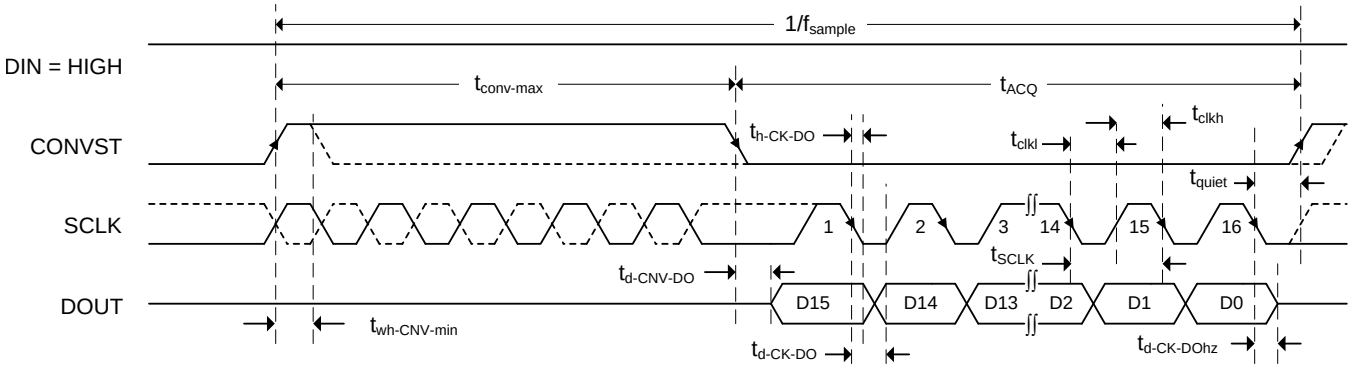

Figure 1. 3-Wire Operation: CONVST Functions as Chip Select

NOTE

Figure 1 shows the timing diagram for the *3-Wire CS Mode Without a Busy Indicator* interface option. However, the timing parameters specified in Table 1 are also applicable for the *3-Wire CS Mode With a Busy Indicator* interface option, unless otherwise specified. Refer to the *Digital Interface* section for specific details for each interface option.

Table 1. TIMING REQUIREMENTS: 3-Wire Operation(1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	1200			ns
t_{conv}	Conversion time	500		1300	ns
$1/f_{sample}$	Time between conversions	2500			ns
$t_{wh\text{-}CNV}$	Pulse duration: CONVST high	10			ns
f_{SCLK}	SCLK frequency			16	MHz
t_{SCLK}	SCLK period	62.5			ns
t_{clkl}	SCLK low time	0.45		0.55	t_{SCLK}
t_{clkh}	SCLK high time	0.45		0.55	t_{SCLK}
$t_{h\text{-}CK\text{-}DO}$	SCLK falling edge to current data invalid	3			ns
$t_{d\text{-}CK\text{-}DO}$	SCLK falling edge to next data valid delay			13.4	ns
$t_{d\text{-}CNV\text{-}DO}$	Enable time: CONVST low to MSB valid			12.3	ns
$t_{d\text{-}CNV\text{-}DOhz}$	Disable time: CONVST high or last SCLK falling edge to DOUT 3-state ($\overline{CS}$ mode)			13.2	ns
t_{quiet}	Quiet time	20			ns

(1) All specifications are at T_A = –40°C to +85°C, AVDD = 3 V, and DVDD = 3 V, unless otherwise noted.

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4-WIRE OPERATION

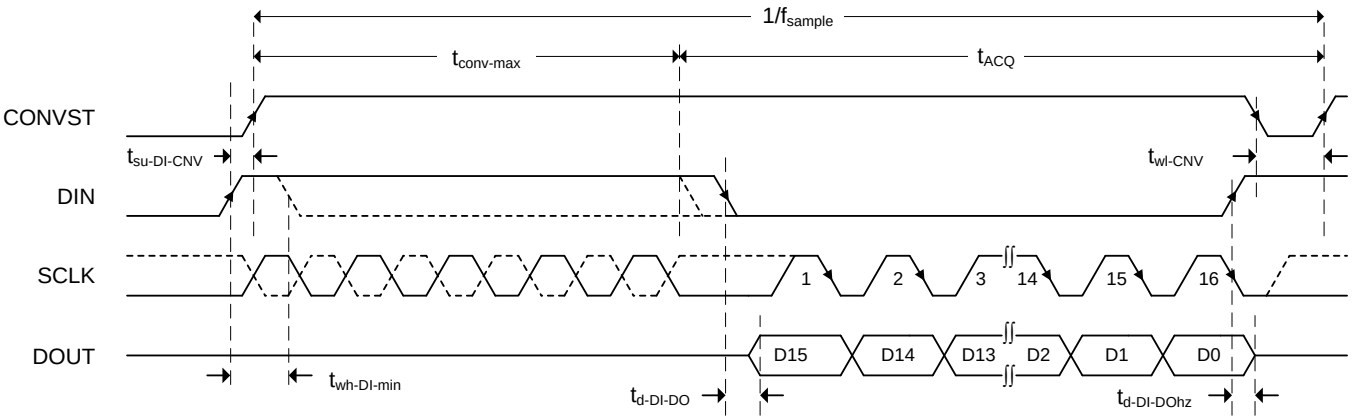

Figure 2. 4-Wire Operation: DIN Functions as Chip Select

NOTE

Figure 2 shows the timing diagram for the *4-Wire CS Mode Without a Busy Indicator* interface option. However, the timing parameters specified in Table 2 are also applicable for the *4-Wire CS Mode With a Busy Indicator* interface option, unless otherwise specified. Refer to the *Digital Interface* section for specific details for each interface option.

Table 2. TIMING REQUIREMENTS: 4-Wire Operation(1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	1200			ns
t_{conv}	Conversion time	500		1300	ns
$1/f_{sample}$	Time between conversions	2500			ns
$t_{wh\text{-}DI}$	Pulse duration: DIN high	10			ns
$t_{wl\text{-}CNV}$	Pulse width: CONVST low	20			ns
$t_{d\text{-}DI\text{-}DO}$	Delay time: DIN low to MSB valid			12.3	ns
$t_{d\text{-}DI\text{-}DOhz}$	Delay time: DIN high or last SCLK falling edge to DOUT 3-state			13.2	ns
$t_{su\text{-}DI\text{-}CNV}$	Setup time: DIN high to CONVST rising edge	7.5			ns
$t_{h\text{-}DI\text{-}CNV}$	Hold time: DIN high from CONVST rising edge (see Figure 63)	0			ns

(1) All specifications are at T_A = –40°C to +85°C, AVDD = 3 V, and DVDD = 3 V, unless otherwise noted.

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DAISY-CHAIN OPERATION

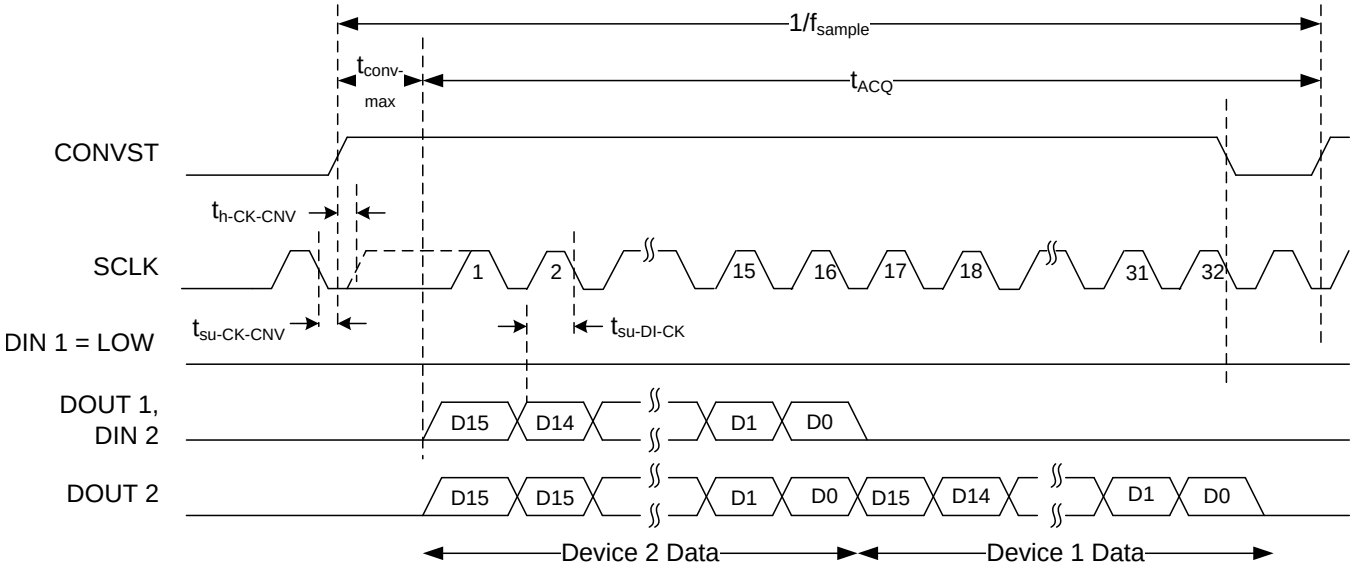

Figure 3. Daisy-Chain Operation: Two Devices

NOTE

Figure 3 shows the timing diagram for the *Daisy-Chain Mode Without a Busy Indicator* interface option. However, the timing parameters specified in Table 3 are also applicable for the *Daisy-Chain Mode With a Busy Indicator* interface option, unless otherwise specified. Refer to the *Digital Interface* section for specific details for each interface option.

Table 3. TIMING REQUIREMENTS: Daisy-Chain(1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	1200			ns
t_{conv}	Conversion time	500		1300	ns
$1/f_{sample}$	Time between conversions	2500			ns
$t_{su\text{-}CK\text{-}CNV}$	Setup time: SCLK valid to CONVST rising edge	5			ns
$t_{h\text{-}CK\text{-}CNV}$	Hold time: SCLK valid from CONVST rising edge	5			ns
$t_{su\text{-}DI\text{-}CNV}$	Setup time: DIN low to CONVST rising edge (see)	7.5			ns
$t_{h\text{-}DI\text{-}CNV}$	Hold time: DIN low from CONVST rising edge (see Figure 63)	0			ns
$t_{su\text{-}DI\text{-}CK}$	Setup time: DIN valid to SCLK falling edge	1.5			ns

(1) All specifications are at T_A = –40°C to +85°C, AVDD = 3 V, and DVDD = 3 V, unless otherwise noted.

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EQUIVALENT CIRCUITS

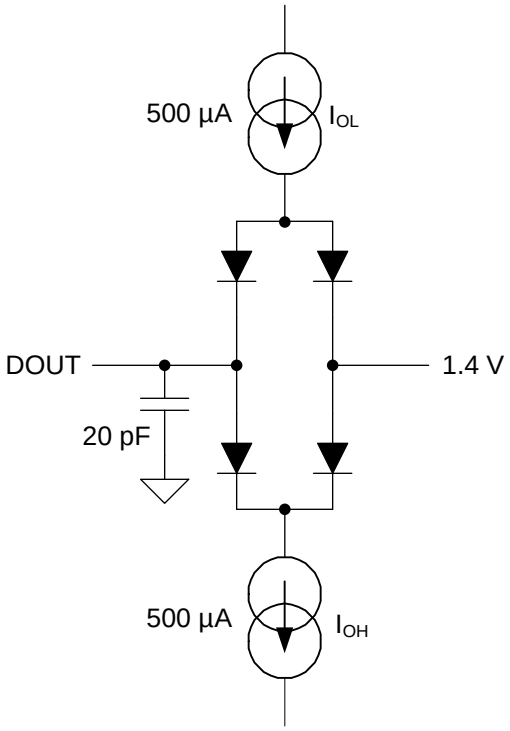

Figure 4. Load Circuit for Digital Interface Timing

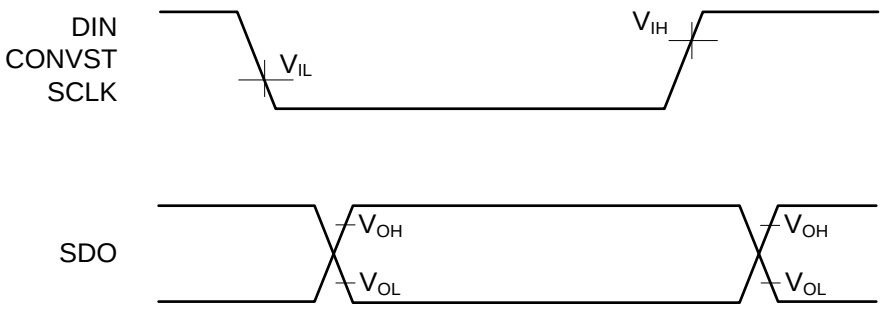

Figure 5. Voltage Levels for Timing

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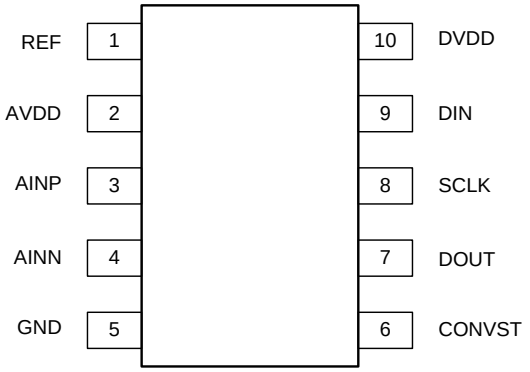
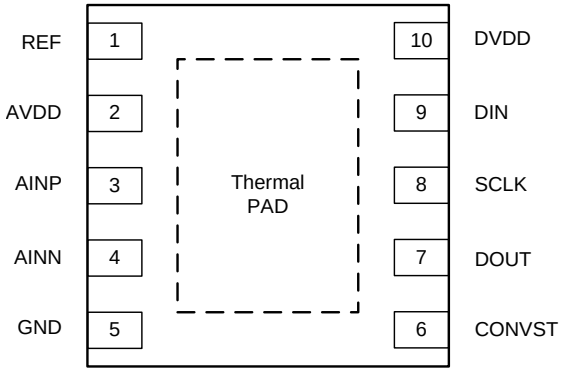
PIN CONFIGURATIONS

DGS PACKAGE
VSSOP-10
(TOP VIEW, Not to Scale)



DRC PACKAGE
SON-10
(TOP VIEW, Not to Scale)



PIN ASSIGNMENTS

PIN NAME	PIN NUMBER	FUNCTION	DESCRIPTION
AINN	4	Analog input	Inverting analog signal input
AINP	3	Analog input	Noninverting analog signal input
AVDD	2	Analog	Analog power supply. This pin must be decoupled to GND with a 1-µF capacitor.
CONVST	6	Digital input	Convert input. This pin also functions as the $\overline{CS}$ input in 3-wire interface mode. Refer to the *Description* and *Timing Characteristics* sections for more details.
DIN	9	Digital input	Serial data input. The DIN level at the start of a conversion selects the mode of operation (such as $\overline{CS}$ or daisy-chain mode). This pin also serves as the $\overline{CS}$ input in 4-wire interface mode. Refer to the *Description* and *Timing Characteristics* sections for more details.
DOUT	7	Digital output	Serial data output
DVDD	10	Power supply	Digital interface power supply. This pin must be decoupled to GND with a 1-µF capacitor.
GND	5	Analog, digital	Device ground. Note that this pin is a common ground pin for both the analog power supply (AVDD) and digital I/O supply (DVDD). The reference return line is also internally connected to this pin.
REF	1	Analog	Positive reference input. This pin must be decoupled with a 10-µF or larger capacitor.
SCLK	8	Digital input	Clock input for serial interface. Data output (on DOUT) are synchronized with this clock.
Thermal pad	—	Thermal pad	Exposed thermal pad. Texas Instruments recommends connecting the thermal pad to the printed circuit board (PCB) ground.

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TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.

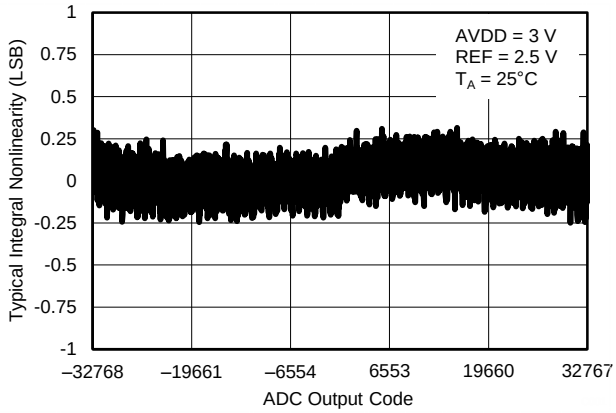

Figure 6. TYPICAL INL (V_{REF} = 2.5 V)

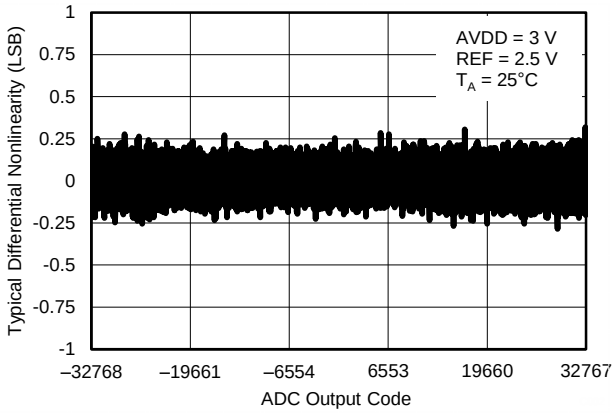

Figure 7. TYPICAL DNL (V_{REF} = 2.5 V)

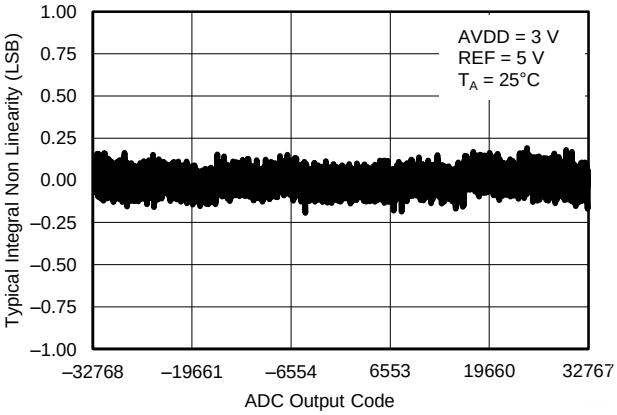

Figure 8. TYPICAL INL (V_{REF} = 5 V)

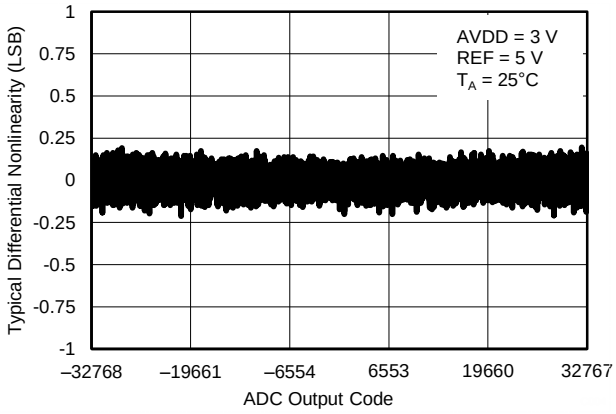

Figure 9. TYPICAL DNL (V_{REF} = 5 V)

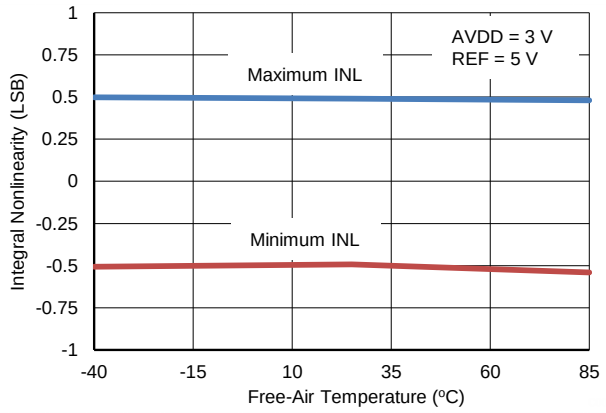

Figure 10. INL vs TEMPERATURE

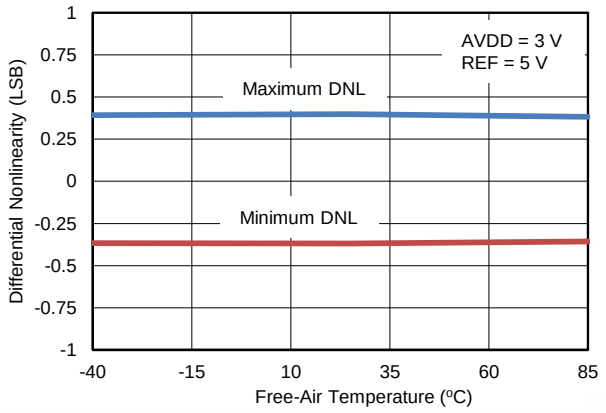

Figure 11. DNL vs TEMPERATURE

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.

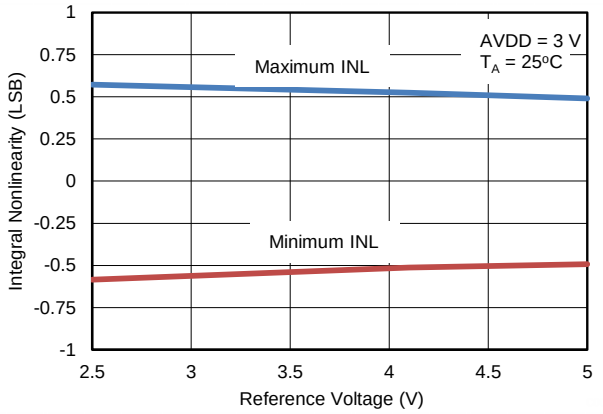

Figure 12. INL vs REFERENCE VOLTAGE

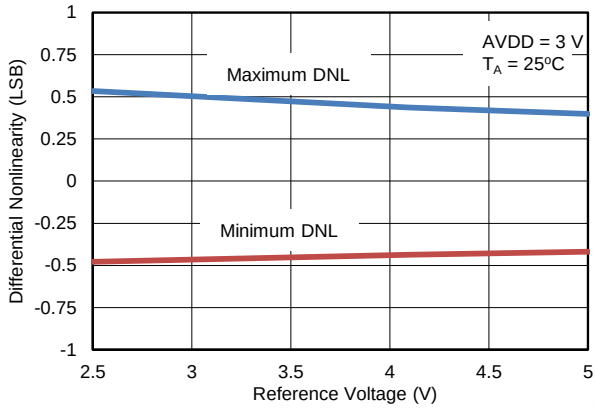

Figure 13. DNL vs REFERENCE VOLTAGE

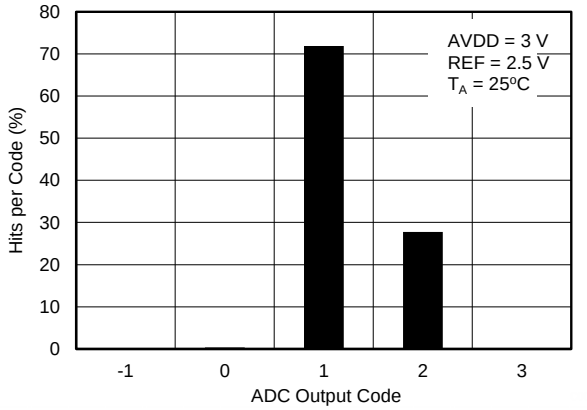

Figure 14. DC INPUT HISTOGRAM (V_{REF} = 2.5 V)

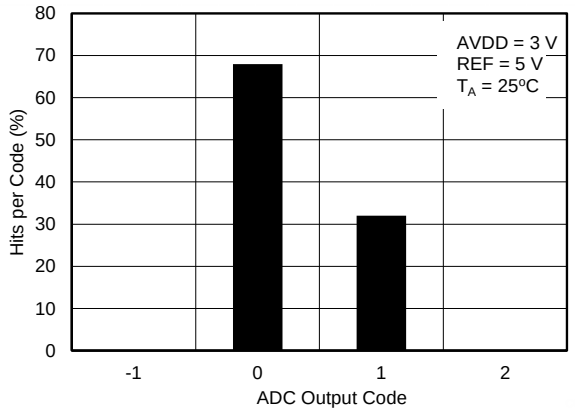

Figure 15. DC INPUT HISTOGRAM (V_{REF} = 5 V)

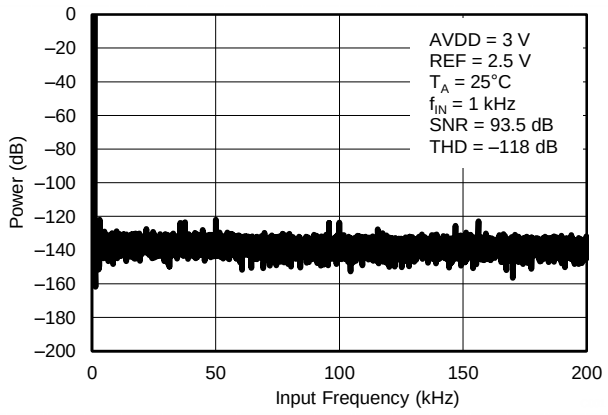

Figure 16. TYPICAL FFT (V_{REF} = 2.5 V)

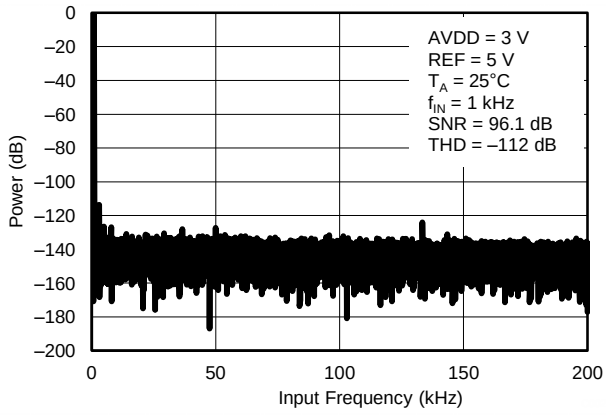

Figure 17. TYPICAL FFT (V_{REF} = 5 V)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.

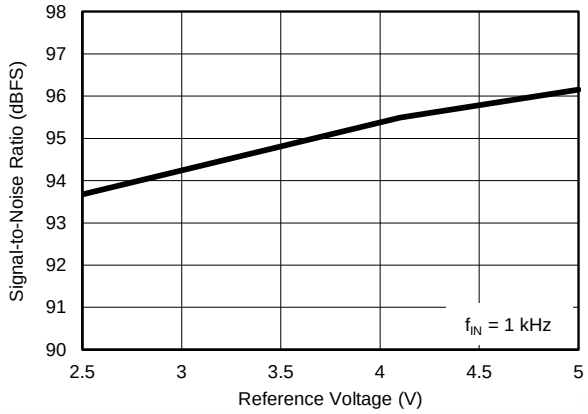

Figure 18. SNR vs REFERENCE VOLTAGE

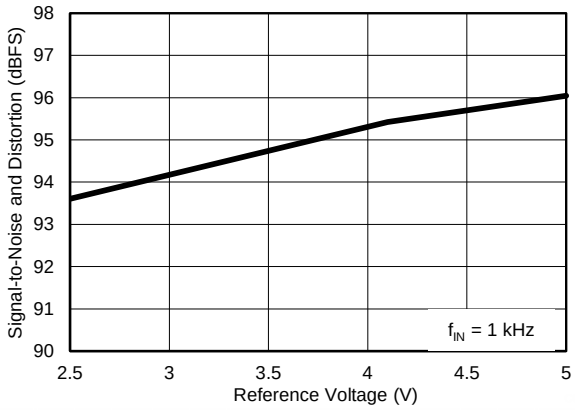

Figure 19. SINAD vs REFERENCE VOLTAGE

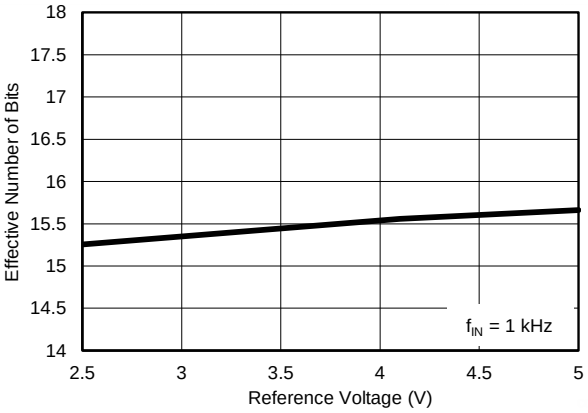

Figure 20. ENOB vs REFERENCE VOLTAGE

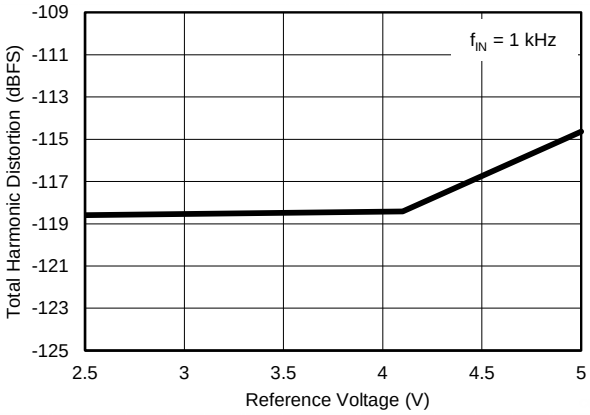

Figure 21. THD vs REFERENCE VOLTAGE

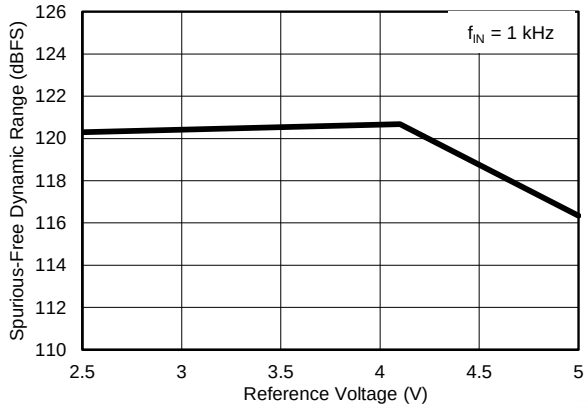

Figure 22. SFDR vs REFERENCE VOLTAGE

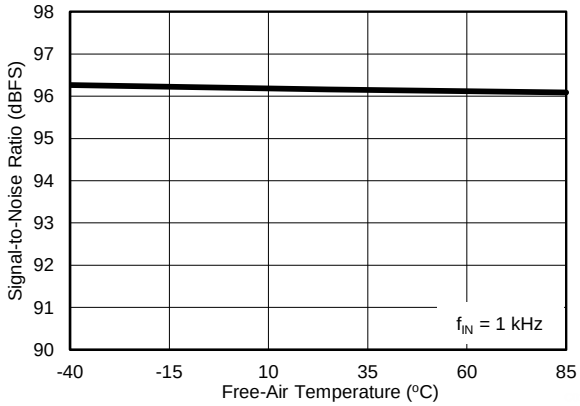

Figure 23. SNR vs TEMPERATURE

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.

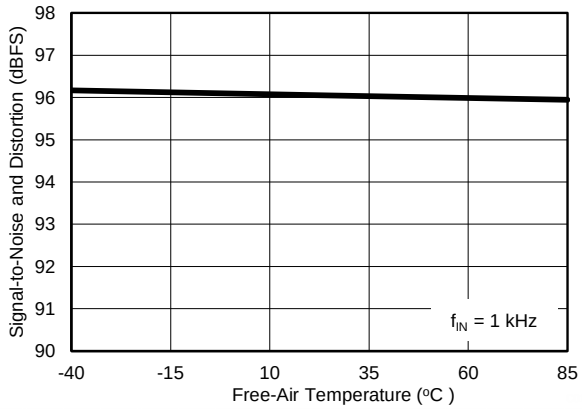

Figure 24. SINAD vs TEMPERATURE

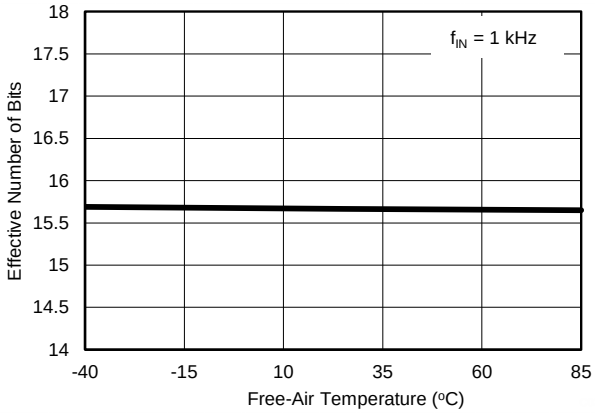

Figure 25. ENOB vs TEMPERATURE

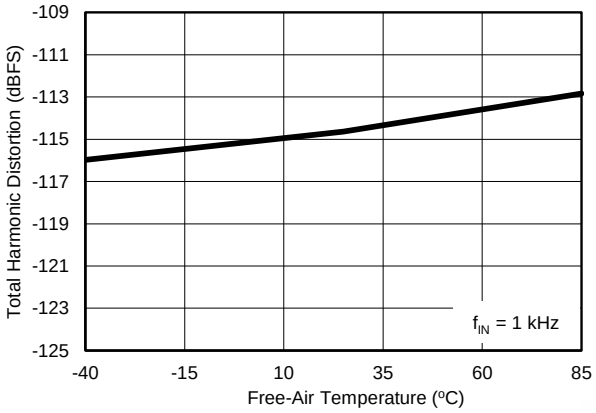

Figure 26. THD vs TEMPERATURE

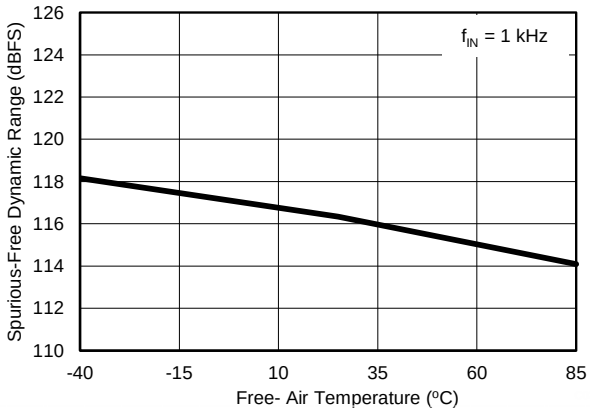

Figure 27. SFDR vs TEMPERATURE

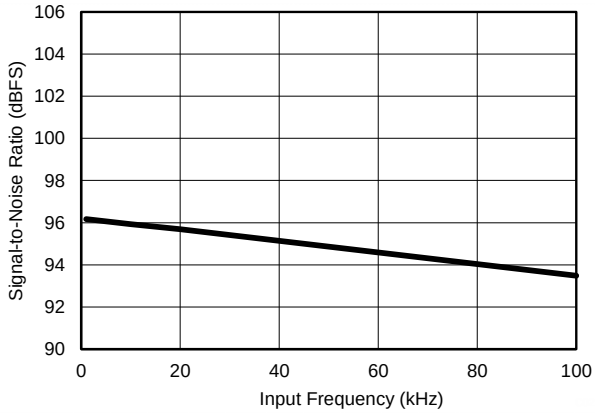

Figure 28. SNR vs INPUT FREQUENCY

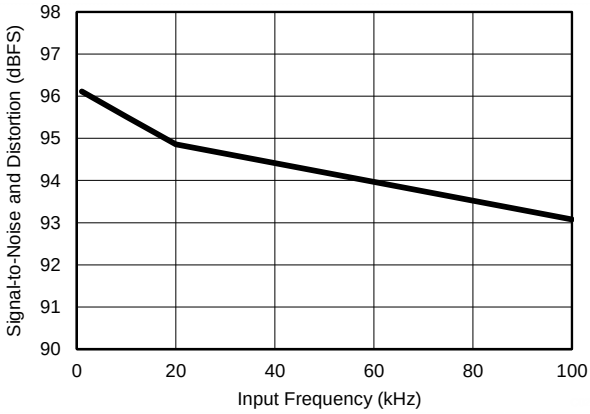

Figure 29. SINAD vs INPUT FREQUENCY

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.

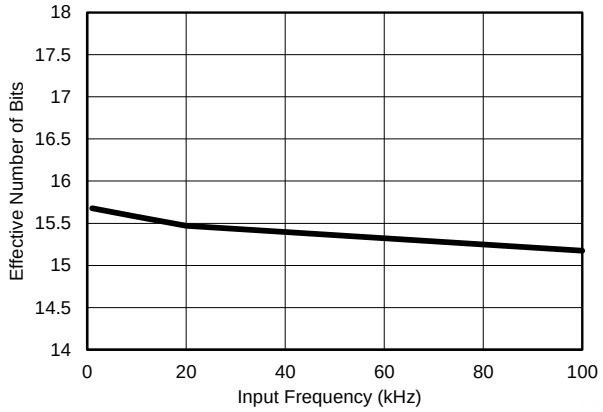

Figure 30. ENOB vs INPUT FREQUENCY

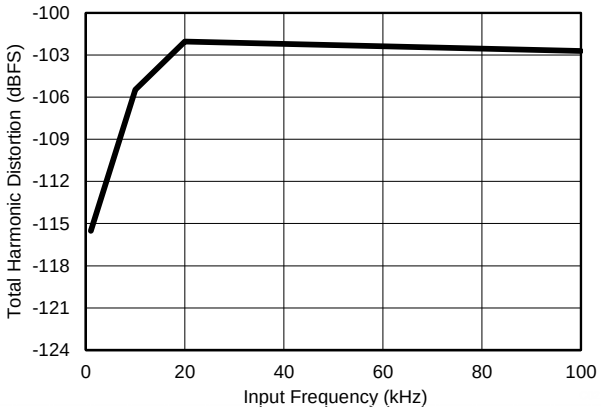

Figure 31. THD vs INPUT FREQUENCY

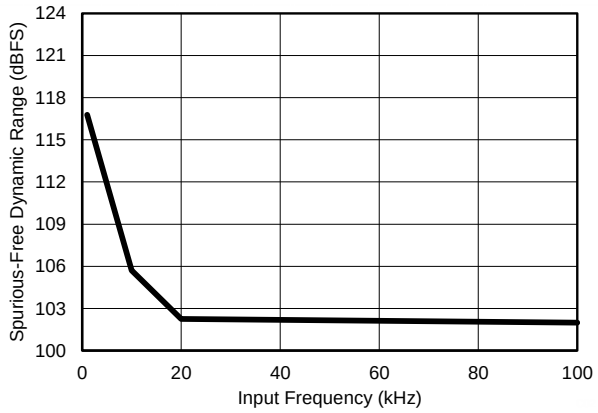

Figure 32. SFDR vs INPUT FREQUENCY

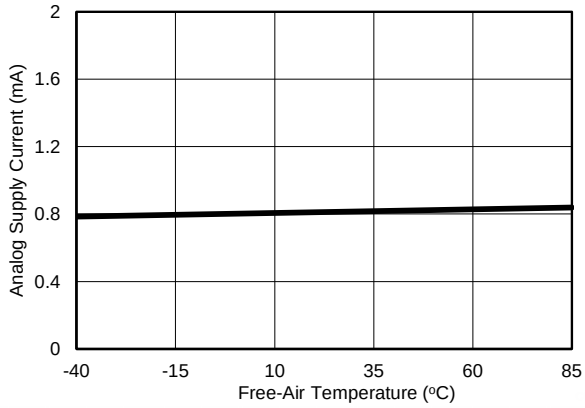

Figure 33. SUPPLY CURRENT vs TEMPERATURE

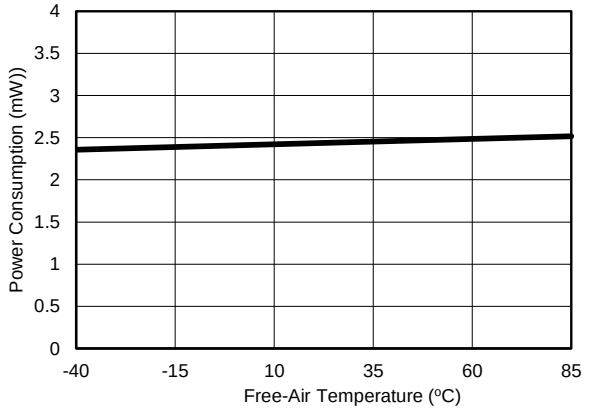

Figure 34. POWER CONSUMPTION vs TEMPERATURE

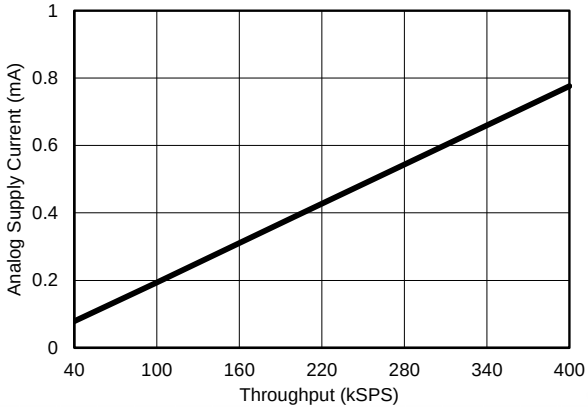

Figure 35. SUPPLY CURRENT vs THROUGHPUT

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.

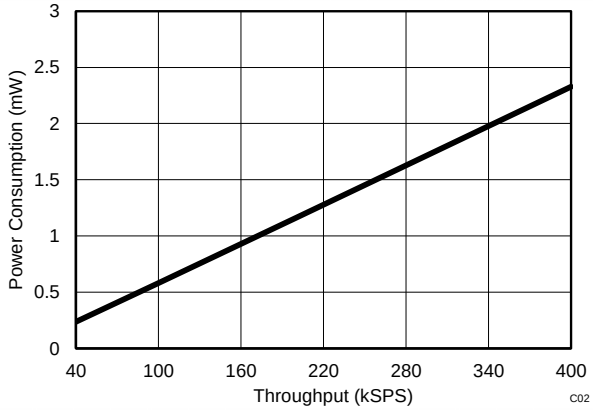

Figure 36. POWER CONSUMPTION vs THROUGHPUT

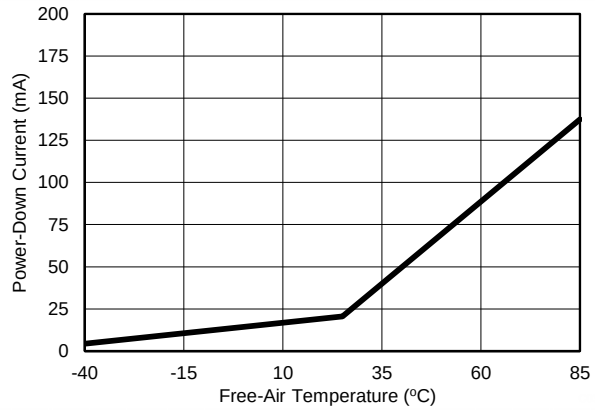

Figure 37. POWER-DOWN CURRENT vs TEMPERATURE

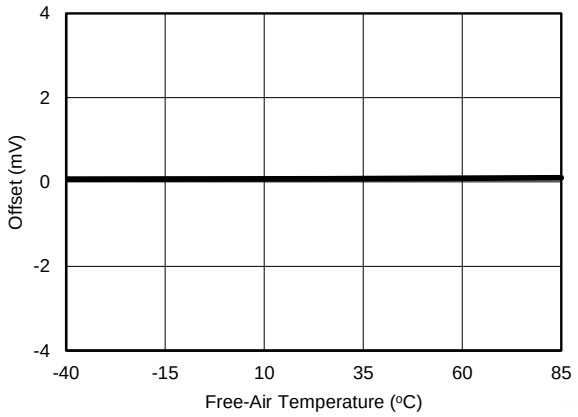

Figure 38. OFFSET vs TEMPERATURE

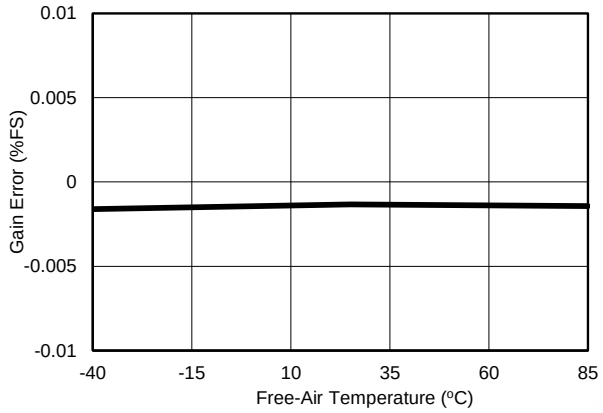

Figure 39. GAIN ERROR vs TEMPERATURE

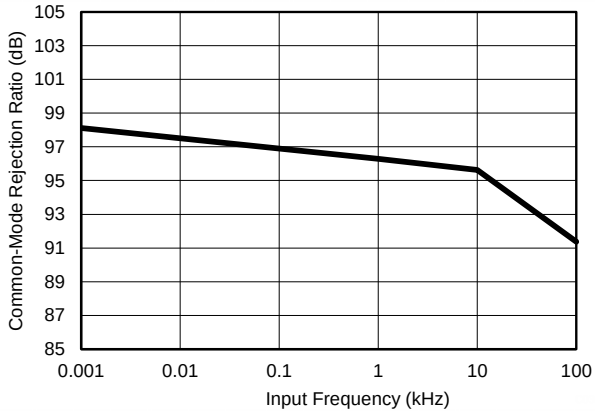

Figure 40. CMRR vs INPUT FREQUENCY

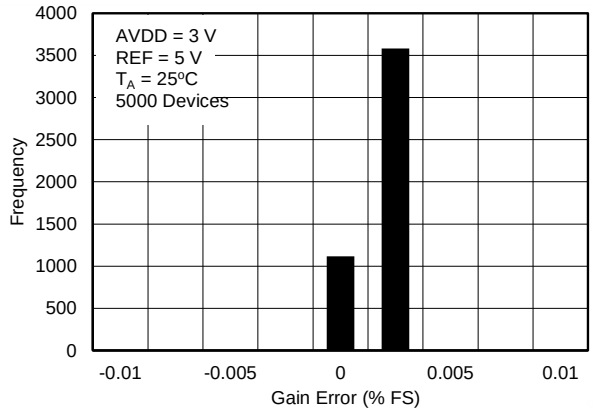

Figure 41. TYPICAL DISTRIBUTION OF GAIN ERROR

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3 V, DVDD = 3 V, V_{REF} = 5 V, and f_{SAMPLE} = 400 kSPS, unless otherwise noted.

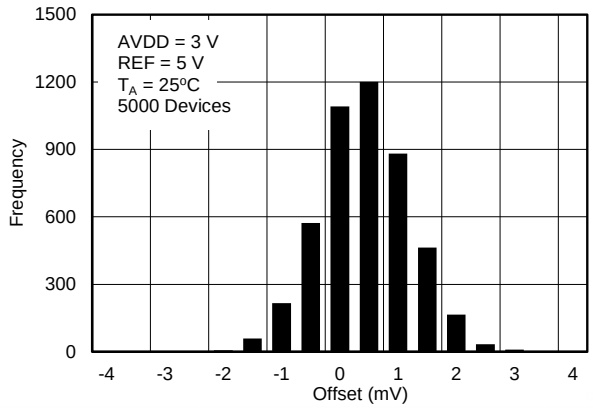

Figure 42. TYPICAL DISTRIBUTION OF OFFSET ERROR

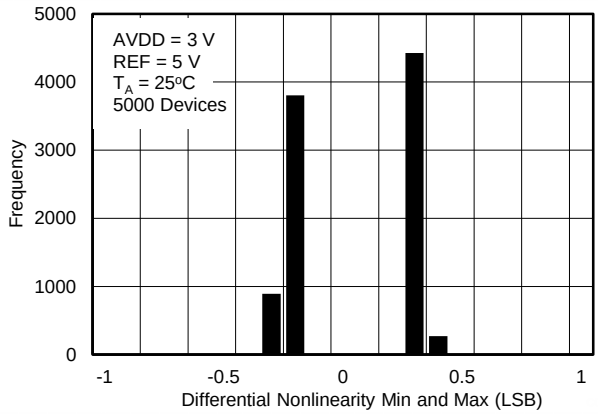

Figure 43. TYPICAL DISTRIBUTION OF DIFFERENTIAL NONLINEARITY (Minimum and Maximum)

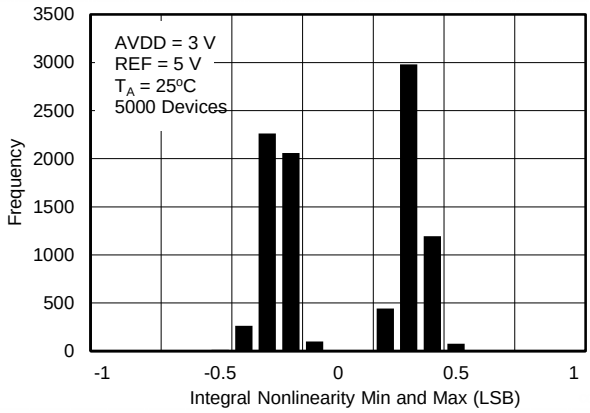

Figure 44. TYPICAL DISTRIBUTION OF INTEGRAL NONLINEARITY (Minimum and Maximum)

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OVERVIEW

The ADS8865 is a high-speed, successive approximation register (SAR), analog-to-digital converter (ADC) from a 16- and 18-bit product family. This compact device features high performance. Power consumption is inherently low and scales linearly with sampling speed. The architecture is based on charge redistribution, which inherently includes a sample-and-hold (S/H) function.

The ADS8865 supports a true-differential analog input across two pins (INP and INN). When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both the INP and INN inputs are disconnected from the internal circuit.

The ADS8865 uses an internal clock to perform conversions. The device reconnects the sampling capacitors to the INP and INN pins after conversion and then enters an acquisition phase. During the acquisition phase, the device is powered down and the conversion result can be read.

The device digital output is available in SPI-compatible format, which makes interfacing with microprocessors, digital signal processors (DSPs), or field-programmable gate arrays (FPGAs) easy.

ANALOG INPUT

As shown in Figure 45, the device features a differential analog input. Both positive and negative inputs are individually sampled on 55-pF sampling capacitors and the device converts for the voltage difference between the two sampled values: $V_{INP} – V_{INN}$.

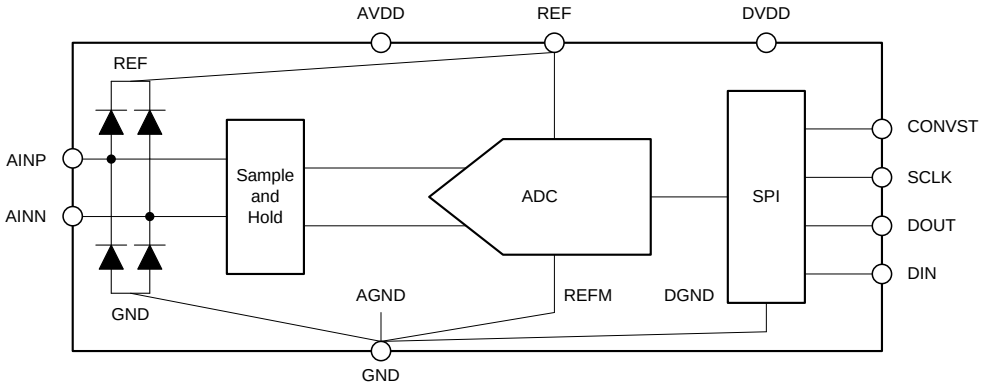

Figure 45. Detailed Block Diagram

Most differential input SAR ADCs prohibit the input common-mode voltage, V_{CM} (that is, the average voltage between the inputs), at AINP or AINM from varying more than approximately 10% beyond the mid-scale input value. As shown in Figure 46, the device has a unique common-mode voltage detection and rejection block that does not have this restriction and thus allows V_{CM} to be set to any value between 0 V and V_{REF} without degrading device performance.

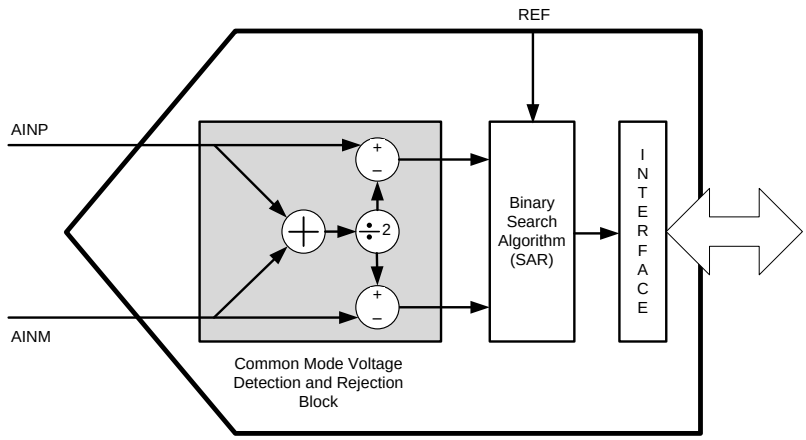

Figure 46. Conceptual Diagram: True Differential Input Structure

Table 4 shows the full-scale input range of the device as a function of input common-mode voltage. The device offers a maximum dynamic range for $V_{CM} = V_{REF} / 2$. The differential input with wide common-mode range allows connecting differential signals from sensors without any signal conditioning.

Table 4. Full-Scale Input Range

V_{CM}	ABSOLUTE INPUT RANGE		FULL SCALE INPUT RANGE (V_{FS})
	V_{AINP}	V_{AINN}	
$V_{CM} < V_{REF} / 2$	0 to 2 × V_{CM}	0 to 2 x V_{CM}	(–2 x V_{CM}) to (2 x V_{CM})
$V_{CM} = V_{REF} / 2$	0 to V_{REF}	0 to V_{REF}	(–V_{REF}) to (V_{REF})
$V_{CM} > V_{REF} / 2$	(2 × V_{CM} – V_{REF}) to V_{REF}	(2 × V_{CM} – V_{REF}) to V_{REF}	(–2 × (V_{CM} – V_{REF})) to (2 × (V_{CM} – V_{REF}))

Figure 47 shows an equivalent circuit of the input sampling stage. The sampling switch is represented by a 96-Ω resistance in series with the ideal switch. Refer to the *ADC Input Driver* section for more details on the recommended driving circuits.

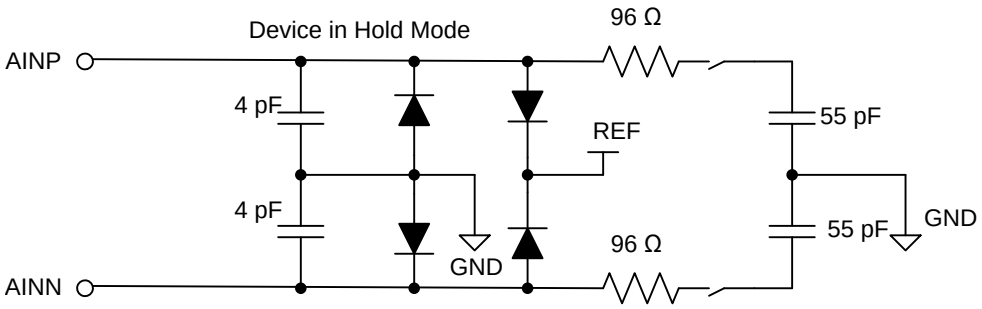

Figure 47. Input Sampling Stage Equivalent Circuit

Figure 45 and Figure 47 illustrate electrostatic discharge (ESD) protection diodes to REF and GND from both analog inputs. Make sure that these diodes do not turn on by keeping the analog inputs within the specified range.

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REFERENCE

The device operates with an external reference voltage and switches binary-weighted capacitors onto the reference terminal (REF pin) during the conversion process. The switching frequency is proportional to the internal conversion clock frequency but the dynamic charge requirements are a function of the absolute value of the input voltage and reference voltage. This dynamic load must be supported by a reference driver circuit without degrading the noise and linearity performance of the device. During the acquisition process, the device automatically powers down and does not take any dynamic current from the external reference source. The basic circuit diagram for such a reference driver circuit for precision ADCs is shown in Figure 48. Refer to the *ADC Reference Driver* section for more details on the application circuits.

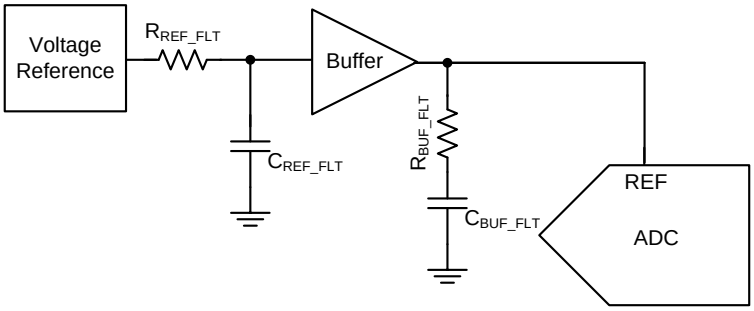

Figure 48. Reference Driver Schematic

CLOCK

The device uses an internal clock for conversion. Conversion duration may vary but is bounded by the minimum and maximum value of t_{conv}, as specified in the Timing Characteristics section. An external SCLK is only used for a serial data read operation. Data are read after a conversion completes and when the device is in acquisition phase for the next sample.

ADC TRANSFER FUNCTION

The ADS8865 is a unipolar, differential input device. The device output is in twos compliment format.

Figure 49 shows ideal characteristics for the device. The full-scale range for the ADC input (AINP – AINN) is equal to twice the reference input voltage to the ADC ($2 \times V_{REF}$). The LSB for the ADC is given by Equation 1.

$$1\ LSB = [2 \times (V_{REF} / 2^{16})] \quad (1)$$

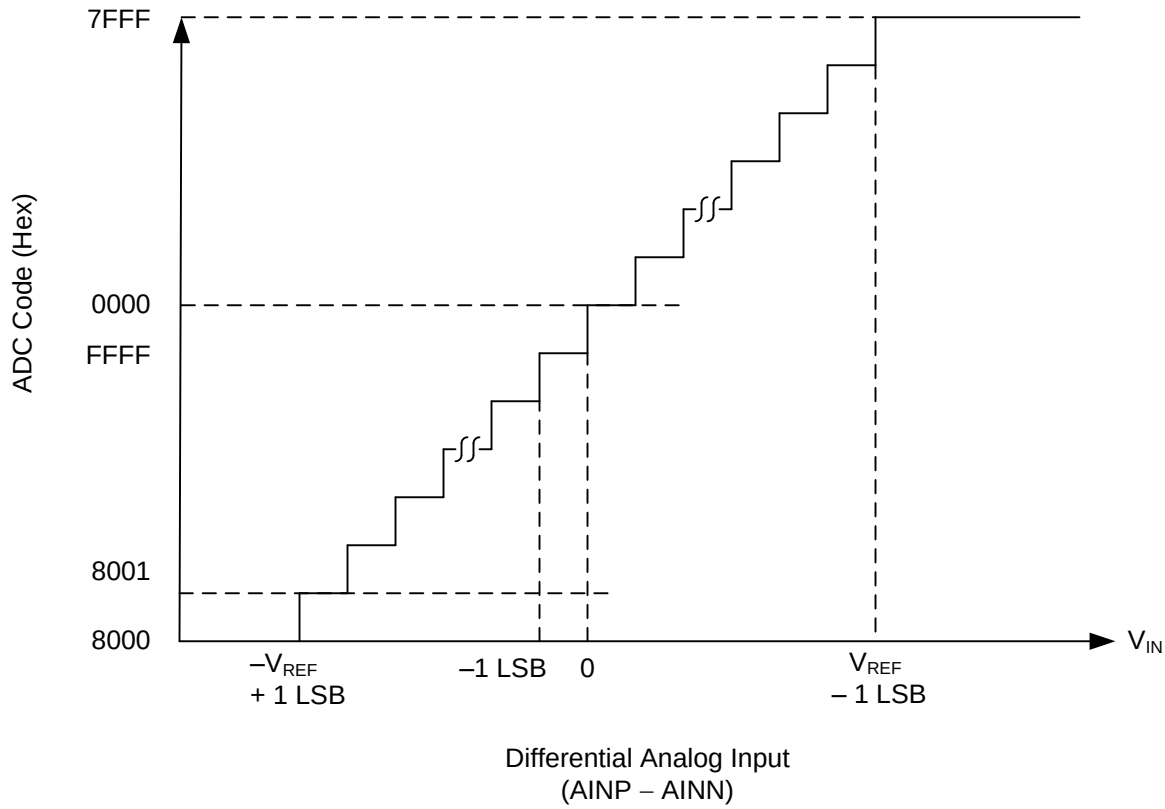

Figure 49. Transfer Characteristics

DIGITAL INTERFACE

The ADS8865 is a low pin-count device. However, the device offers six different options for interfacing with the digital host.

These options can be broadly classified as being either *$\overline{CS}$ mode* (in either a 3- or 4-wire interface) or *daisy-chain mode*. The device operates in $\overline{CS}$ mode if DIN is high at the CONVST rising edge. If DIN is low at the CONVST rising edge, or if DIN and CONVST are connected together, the device operates in daisy-chain mode. In both modes, the device can either operate with or without a *busy indicator*, where the busy indicator is a bit preceding the output data bits that can be used to interrupt the digital host and trigger the data transfer.

The 3-wire interface in $\overline{CS}$ mode is useful for applications that need galvanic isolation on-board. The 4-wire interface in $\overline{CS}$ mode allows the user to sample the analog input independent of the serial interface timing and, therefore, allows easier control of an individual device while having multiple, similar devices on-board. The daisy-chain mode is provided to hook multiple devices in a chain similar to a shift register and is useful in reducing component count and the number of signal traces on the board.

$\overline{CS}$ Mode

$\overline{CS}$ mode is selected if DIN is high at the CONVST rising edge. There are four different interface options available in this mode: 3-wire $\overline{CS}$ mode without a busy indicator, 3-wire $\overline{CS}$ mode with a busy indicator, 4-wire $\overline{CS}$ mode without a busy indicator, and 4-wire $\overline{CS}$ mode with a busy indicator. The following sections discuss these interface options in detail.

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3-Wire $\overline{CS}$ Mode Without a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host. In this interface option, DIN can be connected to DVDD and CONVST functions as $\overline{CS}$ (as shown in Figure 50). As shown in Figure 51, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must return high before the minimum conversion time ($t_{conv\text{-}min}$) elapses and is held high until the maximum possible conversion time ($t_{conv\text{-}max}$) elapses. A high level on CONVST at the end of the conversion ensures the device does not generate a busy indicator.

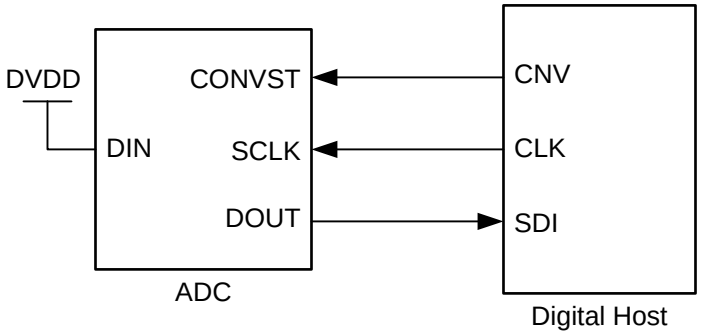

Figure 50. Connection Diagram: 3-Wire $\overline{CS}$ Mode Without a Busy Indicator (DIN = 1)

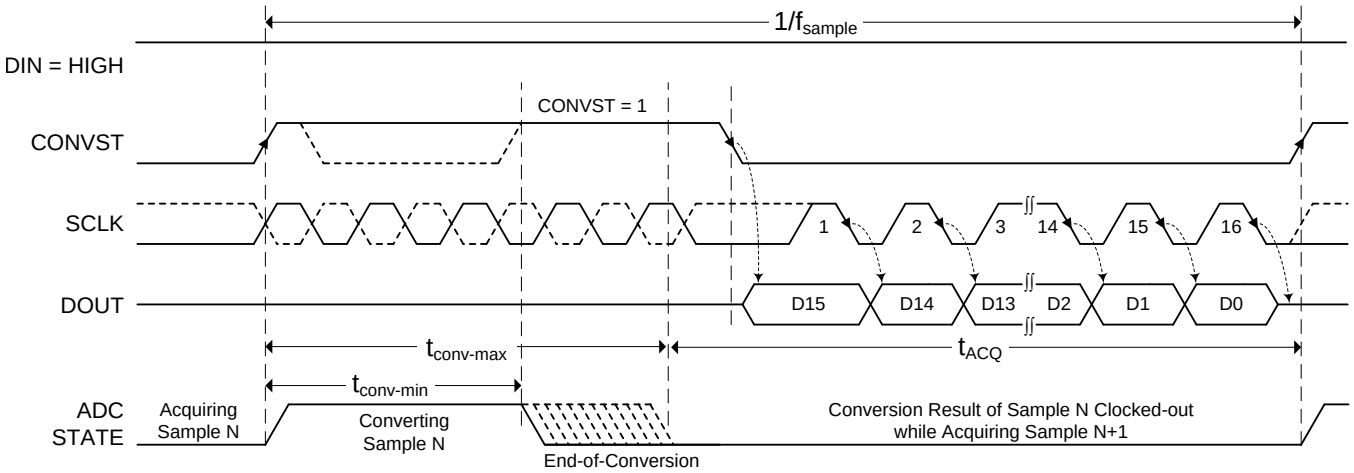

Figure 51. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode Without a Busy Indicator (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down. CONVST (functioning as $\overline{CS}$) can be brought low after the maximum conversion time ($t_{conv\text{-}max}$) elapses. On the CONVST falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided $t_{h_CK_DO}$ is acceptable). DOUT goes to 3-state after the 16th SCLK falling edge or when CONVST goes high, whichever occurs first.

3-Wire $\overline{CS}$ Mode With a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, DIN can be connected to DVDD and CONVST functions as $\overline{CS}$ (as shown in Figure 52). The pull-up resistor on the DOUT pin ensures that the $\overline{IRQ}$ pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 53, a CONVST rising edge forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. Conversion is done with the internal clock and continues regardless of the state of CONVST. As a result, CONVST (functioning as $\overline{CS}$) can be pulled low after the start of the conversion to select other devices on the board. However, CONVST must be pulled low before the minimum conversion time ($t_{conv\text{-}min}$) elapses and must remain low until the maximum possible conversion time ($t_{conv\text{-}max}$) elapses. A low level on the CONVST input at the end of a conversion ensures the device generates a busy indicator.

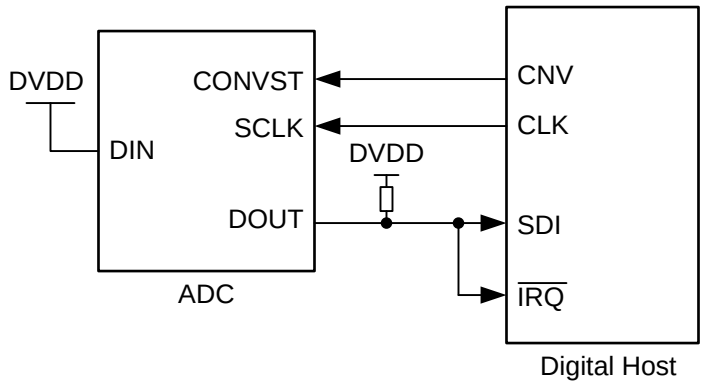

Figure 52. Connection Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator

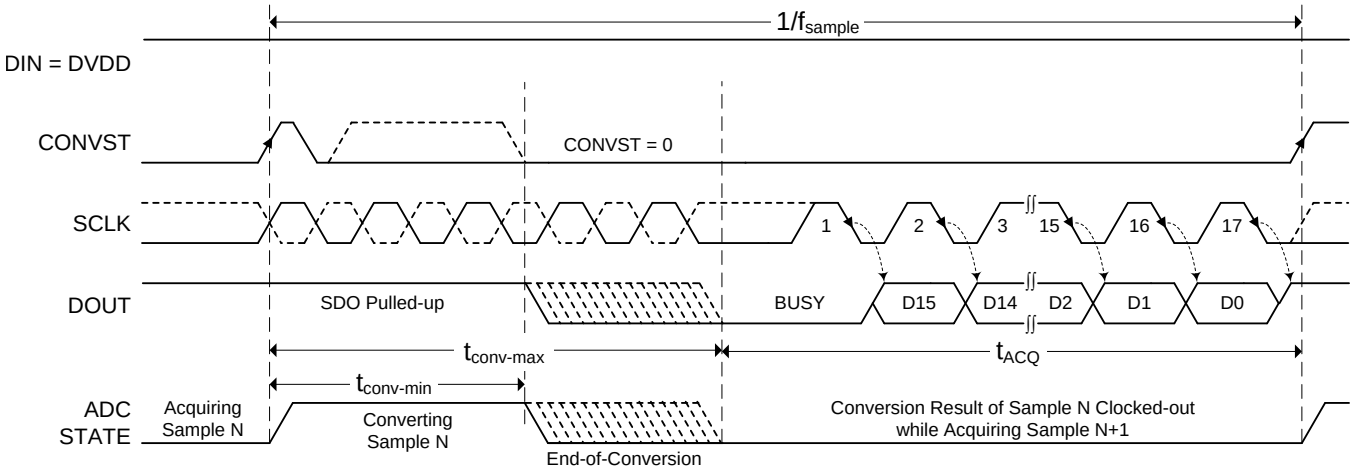

Figure 53. Interface Timing Diagram: 3-Wire $\overline{CS}$ Mode With a Busy Indicator (DIN = 1)

When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided $t_{h_CK_DO}$ is acceptable). DOUT goes to 3-state after the 17th SCLK falling edge or when CONVST goes high, whichever occurs first.

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4-Wire $\overline{CS}$ Mode Without a Busy Indicator

This interface option is useful when one or more ADCs are connected to an SPI-compatible digital host. Figure 54 shows the connection diagram for single ADC, Figure 56 shows the connection diagram for two ADCs.

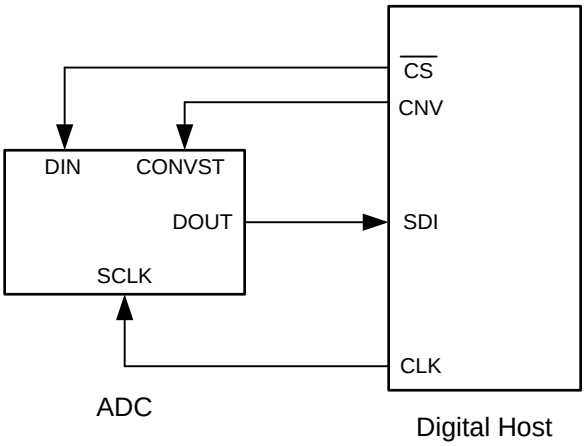

Figure 54. Connection Diagram: Single ADC with 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

In this interface option, DIN is controlled by the digital host and functions as $\overline{CS}$. As shown in Figure 55, with DIN high, a CONVST rising edge selects $\overline{CS}$ mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held at a high level from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (functioning as $\overline{CS}$) can be pulled low to select other devices on the board. However, DIN must be pulled high before the minimum conversion time ($t_{conv\text{-}min}$) elapses and remains high until the maximum possible conversion time ($t_{conv\text{-}max}$) elapses. A high level on DIN at the end of the conversion ensures the device does not generate a busy indicator.

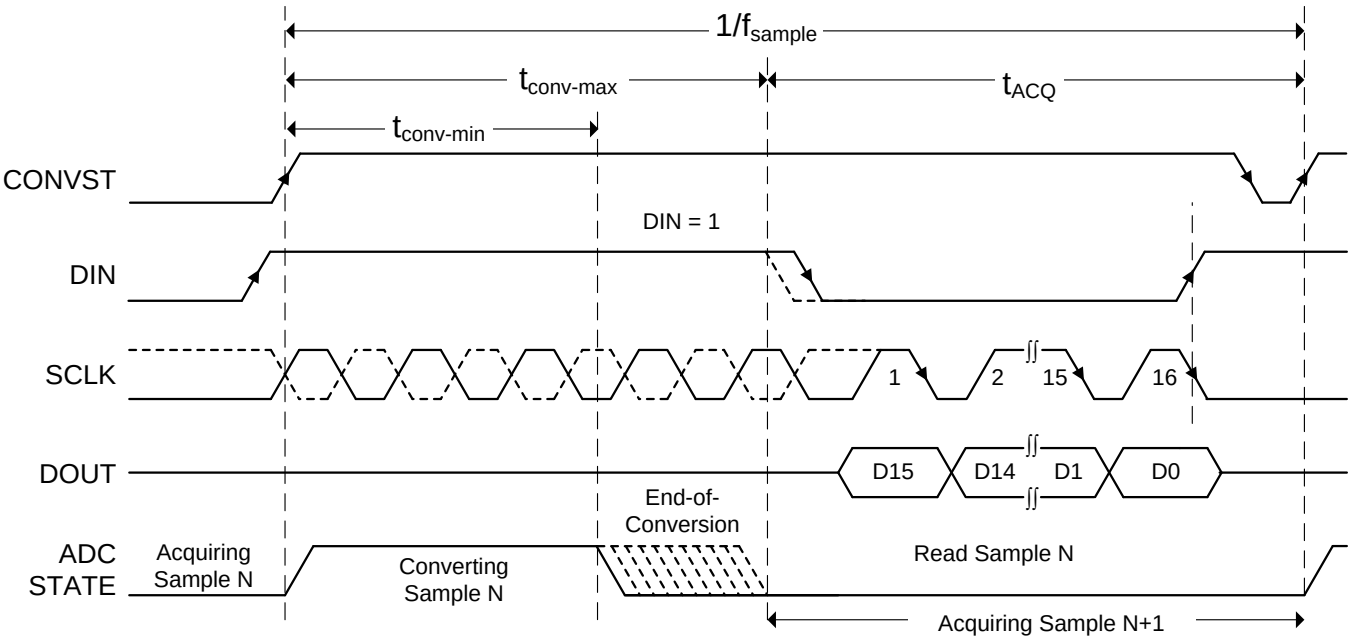

Figure 55. Interface Timing Diagram: Single ADC with 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

When conversion is complete, the device enters acquisition phase and powers down. DIN (functioning as $\overline{CS}$) can be brought low after the maximum conversion time ($t_{conv-max}$) elapses. On the DIN falling edge, DOUT comes out of 3-state and the device outputs the MSB of the data. The lower data bits are output on subsequent SCLK falling edges. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided $t_{h_CK_DO}$ is acceptable). DOUT goes to 3-state after the 16th SCLK falling edge or when DIN goes high, whichever occurs first.

As shown in Figure 56, multiple devices can be hooked together on the same data bus. In this case, as shown in Figure 57, the DIN of the second device (functioning as $\overline{CS}$ for the second device) can go low after the first device data are read and the DOUT of the first device is in 3-state.

Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

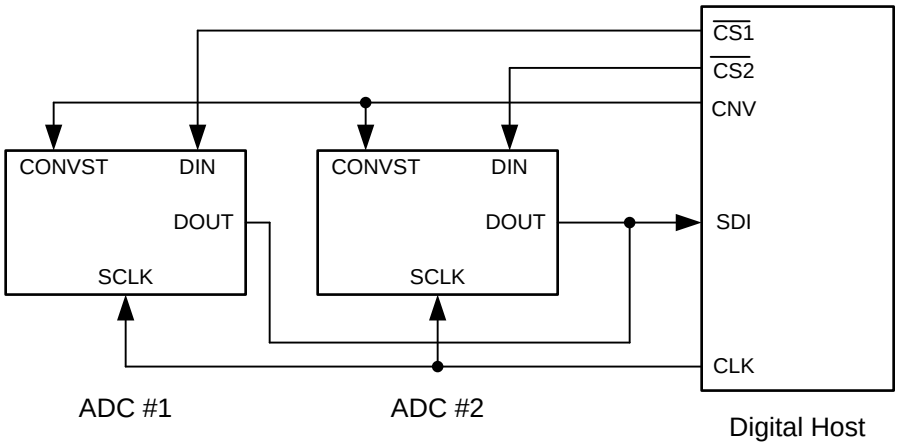

Figure 56. Connection Diagram: Two ADCs with 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

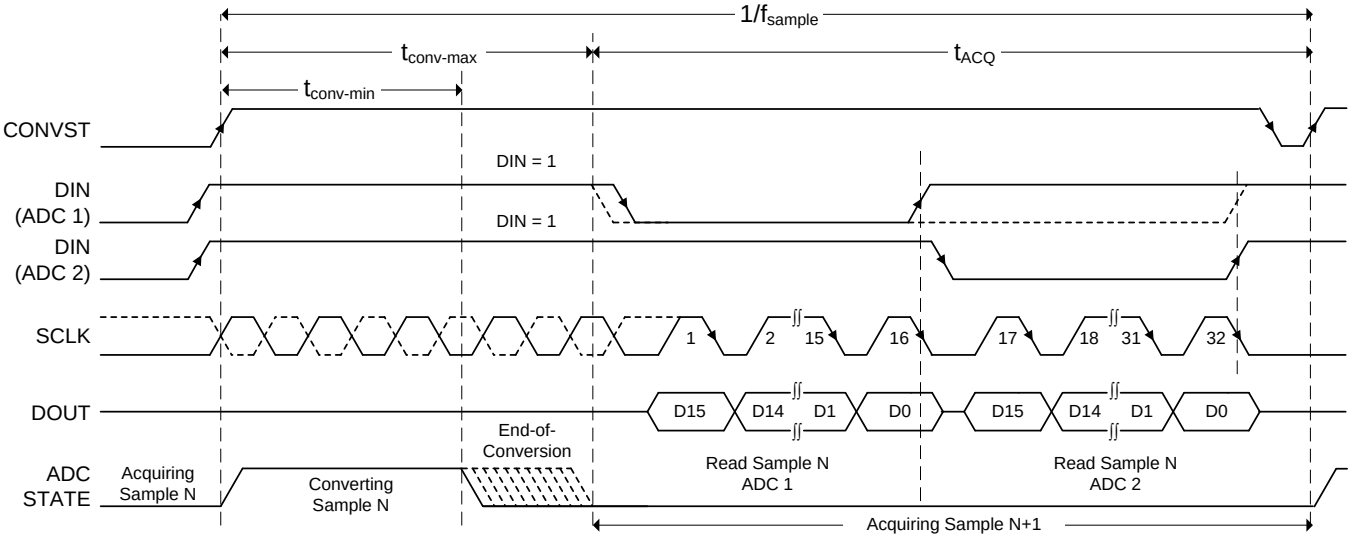

Figure 57. Interface Timing Diagram: Two ADCs with 4-Wire $\overline{CS}$ Mode Without a Busy Indicator

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4-Wire $\overline{CS}$ Mode With a Busy Indicator

This interface option is most useful when a single ADC is connected to an SPI-compatible digital host and an interrupt-driven data transfer is desired. In this interface option, the analog sample is least affected by clock jitter because the CONVST signal (used to sample the input) is independent of the data read operation. In this interface option, DIN is controlled by the digital host and functions as $\overline{CS}$ (as shown in Figure 58). The pull-up resistor on the DOUT pin ensures that the $\overline{IRQ}$ pin of the digital host is held high when DOUT goes to 3-state. As shown in Figure 59, when DIN is high, a CONVST rising edge selects $\overline{CS}$ mode, forces DOUT to 3-state, samples the input signal, and causes the device to enter a conversion phase. In this interface option, CONVST must be held high from the start of the conversion until all data bits are read. Conversion is done with the internal clock and continues regardless of the state of DIN. As a result, DIN (acting as $\overline{CS}$) can be pulled low to select other devices on the board. However, DIN must be pulled low before the minimum conversion time ($t_{conv\text{-}min}$) elapses and remains low until the maximum possible conversion time ($t_{conv\text{-}max}$) elapses. A low level on the DIN input at the end of a conversion ensures the device generates a busy indicator.

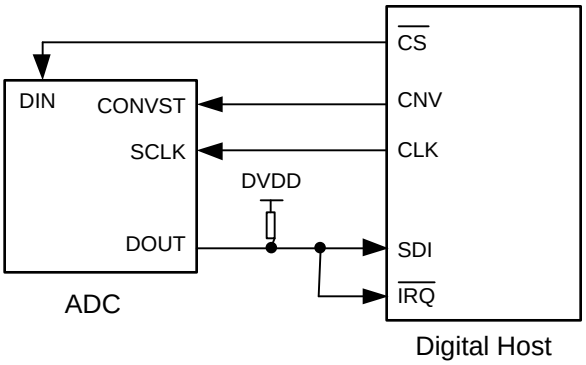

Figure 58. Connection Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

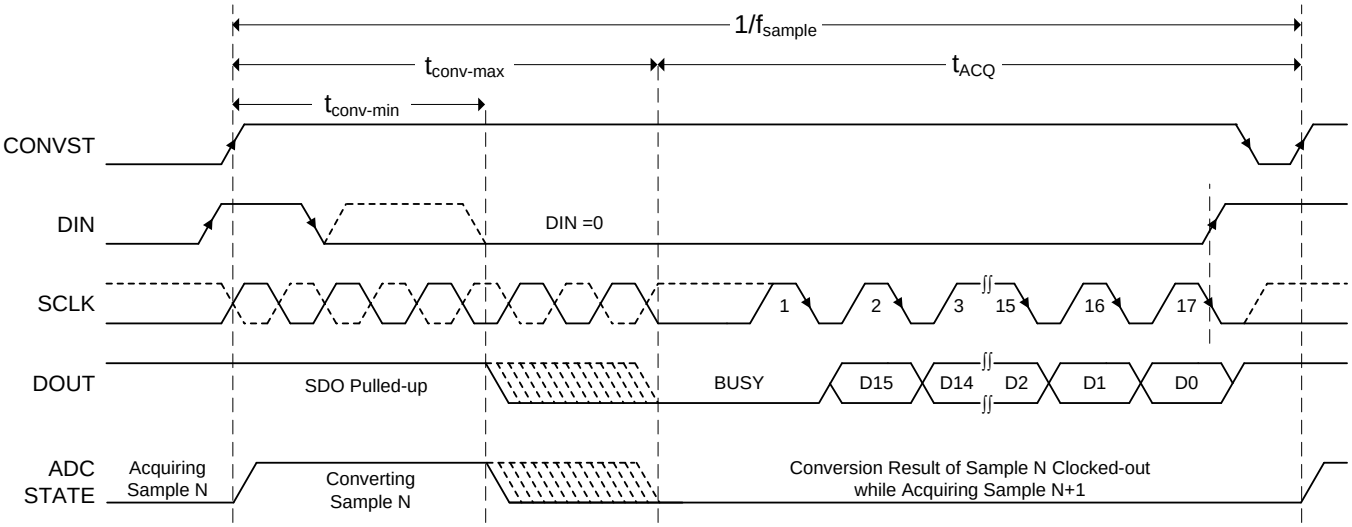

Figure 59. Interface Timing Diagram: 4-Wire $\overline{CS}$ Mode With a Busy Indicator

When conversion is complete, the device enters an acquisition phase and powers down, DOUT comes out of 3-state, and the device outputs a busy indicator bit (low level) on the DOUT pin. This configuration provides a high-to-low transition on the $\overline{IRQ}$ pin of the digital host. The data bits are clocked out, MSB first, on the subsequent SCLK falling edges. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided $t_{h_CK_DO}$ is acceptable). DOUT goes to 3-state after the 17th SCLK falling edge or when DIN goes high, whichever occurs first. Care must be taken so that CONVST and DIN are not both low together at any time during the cycle.

DAISY-CHAIN MODE

Daisy-chain mode is selected if DIN is low at the time of a CONVST rising edge or if DIN and CONVST are connected together. Similar to $\overline{CS}$ mode, this mode features operation with or without a busy indicator. The following sections discuss these interface modes in detail.

Daisy-Chain Mode Without a Busy Indicator

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability. Figure 60 shows a connection diagram with *N* ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 is connected to GND. The DOUT pin of ADC 1 is connected to the DIN pin of ADC 2, and so on. The DOUT pin of the last ADC in the chain (ADC N) is connected to the SDI pin of the digital host.

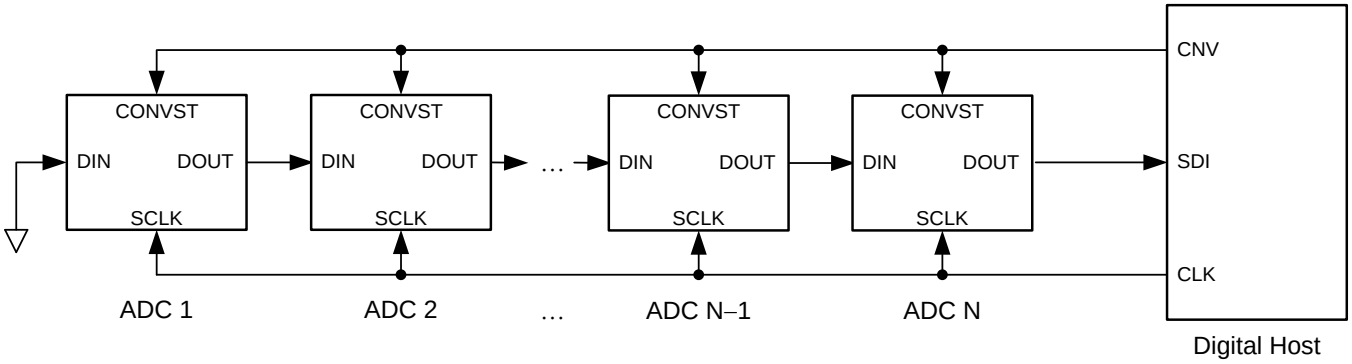

Figure 60. Connection Diagram: Daisy-Chain Mode Without a Busy Indicator (DIN = 0)

As shown in Figure 61, the device DOUT pin is driven low when DIN and CONVST are low together. With DIN low, a CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be low at the CONVST rising edge so that the device does not generate a busy indicator at the end of the conversion.

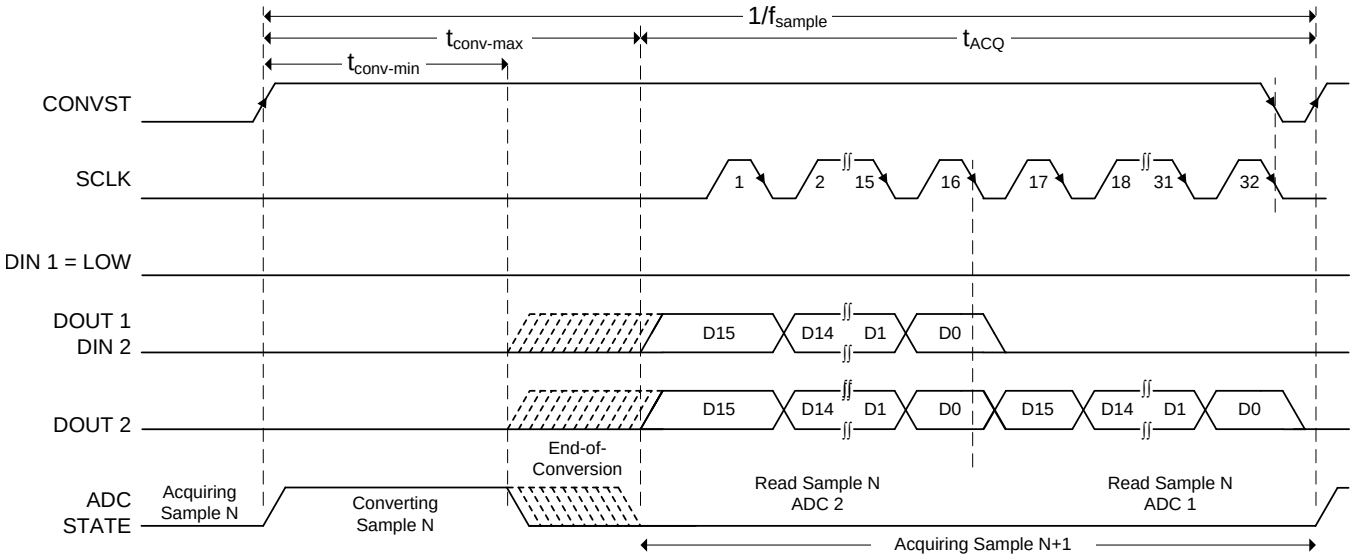

Figure 61. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode Without a Busy Indicator

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At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 16-bit, shift register and also outputs the MSB bit of this conversion result on its own DOUT pin. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the data of ADC N, followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of 16 x *N* SCLK falling edges are required to capture the outputs of all *N* devices in the chain. Data are valid on both SCLK edges. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided $t_{h_CK_DO}$ is acceptable).

Daisy-Chain Mode With a Busy Indicator

This interface option is most useful in applications where multiple ADC devices are used but the digital host has limited interfacing capability and an interrupt-driven data transfer is desired. Figure 62 shows a connection diagram with *N* ADCs connected in the daisy-chain. The CONVST pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. Similarly, the SCLK pins of all ADCs in the chain are connected together and are controlled by a single pin of the digital host. The DIN pin for ADC 1 is connected to its CONVST. The DOUT pin of ADC 1 is connected to the DIN pin of ADC 2, and so on. The DOUT pin of the last ADC in the chain (ADC N) is connected to the SDI and IRQ pins of the digital host.

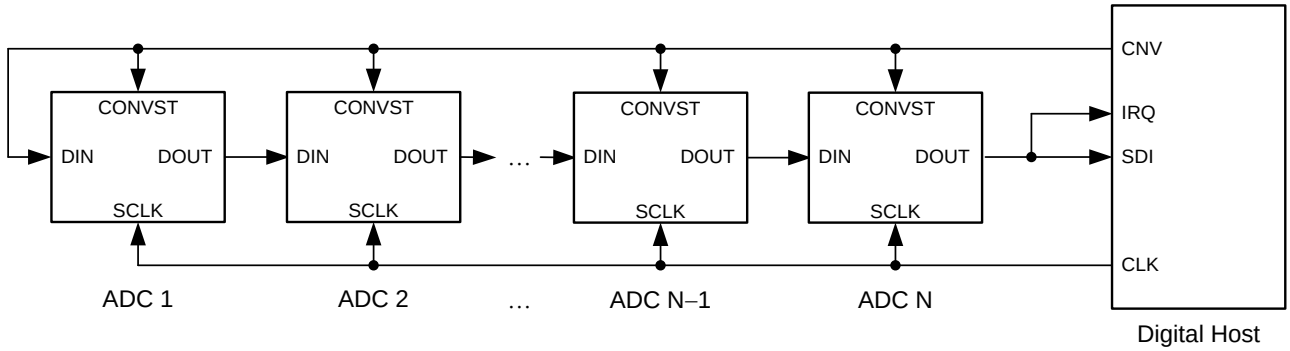

Figure 62. Connection Diagram: Daisy-Chain Mode With a Busy Indicator (DIN = 0)

As shown in Figure 63, the device DOUT pin is driven low when DIN and CONVST are low together. A CONVST rising edge selects daisy-chain mode, samples the analog input, and causes the device to enter a conversion phase. In this interface option, CONVST must remain high from the start of the conversion until all data bits are read. When started, the conversion continues regardless of the state of SCLK, however SCLK must be high at the CONVST rising edge so that the device generates a busy indicator at the end of the conversion.

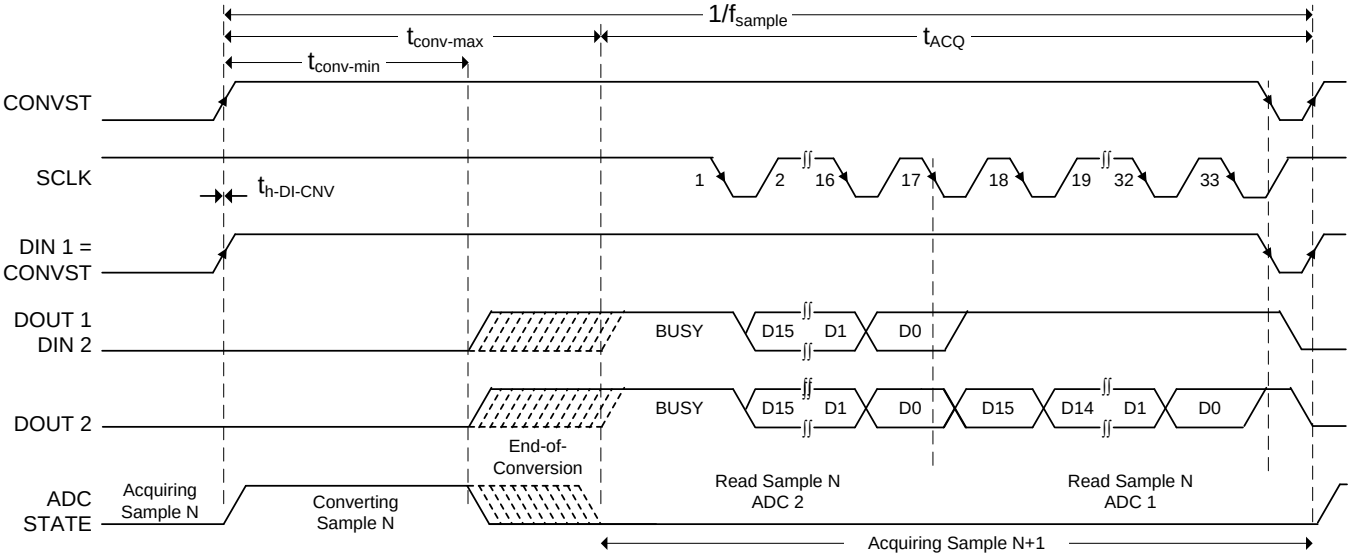

Figure 63. Interface Timing Diagram: For Two Devices in Daisy-Chain Mode With a Busy Indicator

At the end of conversion, every ADC in the chain loads its own conversion result into the internal, 16-bit, shift register and also forces its DOUT pin high, thereby providing a low-to-high transition on the IRQ pin of the digital host. All ADCs enter an acquisition phase and power-down. On every subsequent SCLK falling edge, the internal shift register of each ADC latches the data available on its DIN pin and shifts out the next bit of data on its DOUT pin. Therefore, the digital host receives the interrupt signal followed by the data of ADC N followed by the data of ADC N–1, and so on (in MSB-first fashion). A total of (16 x N) + 1 SCLK falling edges are required to capture the outputs of all *N* devices in the chain. Data are valid on both edges of SCLK and can be captured on either edge. However, a digital host capturing data on the SCLK falling edge can achieve a faster reading rate (provided $t_{h_CK_DO}$ is acceptable). Note that the busy indicator bits of ADC 1 to ADC N–1 do not propagate to the next device in the chain.

POWER SUPPLY

The device has two separate power supplies: AVDD and DVDD. The internal circuits of the device operate on AVDD; DVDD is used for the digital interface. AVDD and DVDD can be independently set to any value within the permissible range.

Decouple the AVDD and DVDD pins with GND, using individual 1-µF decoupling capacitors placed in close proximity to the pin, as shown in Figure 64.

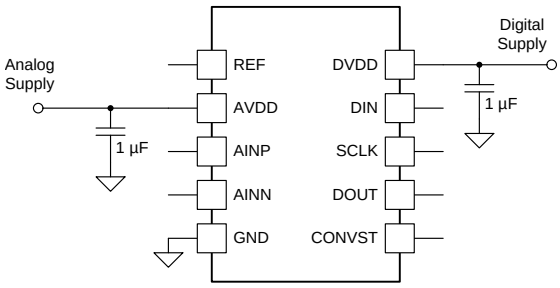

Figure 64. Supply Decoupling

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POWER SAVING

The device has an auto power-down feature that powers down the internal circuitry at the end of every conversion. Referring to Figure 65, the input signal is acquired on the sampling capacitors when the device is in a power-down state (t_{acq}); at the same time, the result for the previous conversion is available for reading. The device powers up on the start of the next conversion. During conversion phase (t_{conv}), the device also consumes current from the reference source (connected to pin REF).

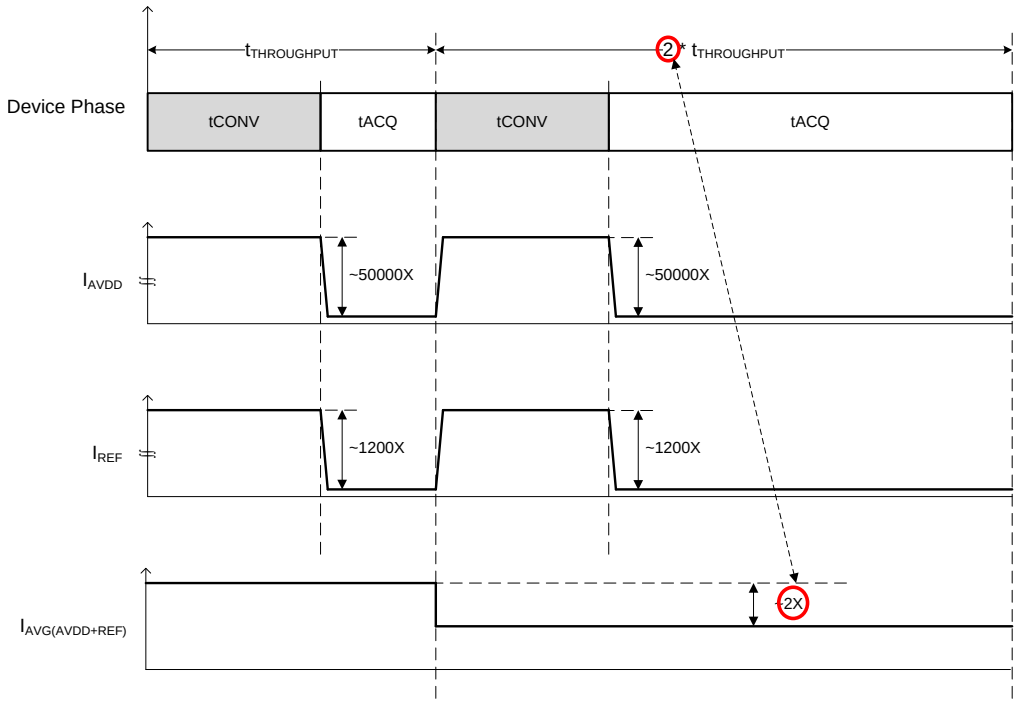

Figure 65. Power Scaling with Throughput

The conversion time, t_{conv}, is independent of the SCLK frequency. When operating the device at speeds lower than the maximum rated throughput, the conversion time, t_{conv}, does not change; the device spends more time in power-down state. Therefore, as shown in Figure 66, the device power consumption from the AVDD supply and the external reference source is directly proportional to the speed of operation. Extremely low AVDD power-down current (50 nA, typical) and extremely low external reference leakage current (250 nA, typical), make this device ideal for very low throughput applications (such as pulsed measurements).

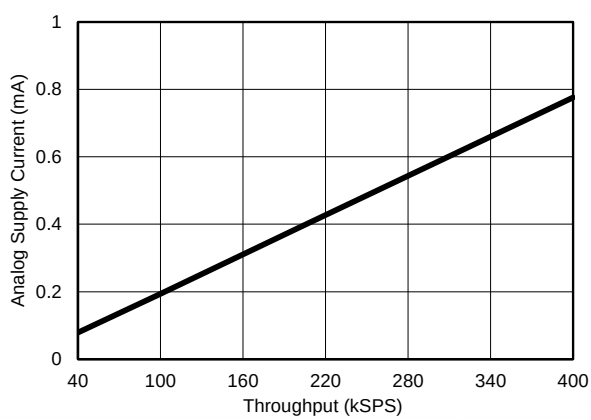

Figure 66. Power Scaling with Throughput

APPLICATION INFORMATION

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits, followed by some application circuits designed using the ADS8865.

ADC REFERENCE DRIVER

The external reference source to the ADS8865 must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few 100 μV_{RMS}. Therefore, to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred Hertz.

After band-limiting the noise of the reference circuit, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. The reference buffer must regulate the voltage at the reference pin such that the value of V_{REF} stays within the 1-LSB error at the start of each conversion. This condition necessitates the use of a large capacitor, C_{BUF_FLT} (refer to Figure 48) for regulating the voltage at the reference input of the ADC. The amplifier selected to drive the reference pin should have an extremely low offset and temperature drift with a low output impedance to drive the capacitor at the ADC reference pin without any stability issues.

Reference Driver Circuit for V_{REF} = 4.5 V

The application circuit in Figure 67 shows the schematic of a complete reference driver circuit that generates a voltage of 4.5 V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8865 at higher sampling rates up to 400 kSPS. The 4.5-V reference voltage in this design is generated by the high-precision, low-noise REF5045 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz.

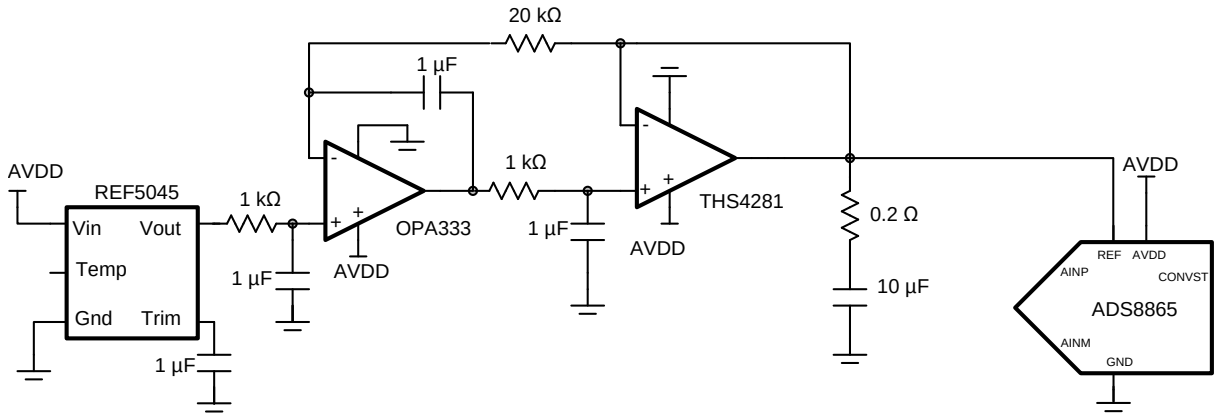

Figure 67. Schematic of Reference Driver Circuit with V_{REF} = 4.5 V

The reference buffer is designed with the THS4281 and OPA333 in a composite architecture to achieve superior dc and ac performance at a reduced power consumption, compared to using a single high-performance amplifier. The THS4281 is a high-bandwidth amplifier with a very low output impedance of 1 Ω at a frequency of 1 MHz. The low output impedance makes the THS4281 a good choice for driving a high capacitive load to regulate the voltage at the reference input of the ADC. The high offset and drift specifications of the THS4281 are corrected by using a dc-correcting amplifier (OPA333) inside the feedback loop. The composite scheme inherits the extremely low offset and temperature drift specifications of the OPA333.

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to *18-Bit Data Acquisition (DAQ) Block Optimized for 1-µs Full-Scale Step Response* (SLAU512).

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Reference Driver Circuit for V_{REF} = 2.5 V in Ultralow Power, Lower Throughput Applications

The application circuit in Figure 68 shows the schematic of a complete reference driver circuit that generates a voltage of 2.5 V dc using a single 3.3-V supply. This ultralow power reference block is suitable to drive the ADS8865 for power-sensitive applications at a relatively lower throughput. This design uses the high-precision REF3325 circuit that provides an accurate 2.5-V reference voltage at an extremely low quiescent current of 5 µA. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

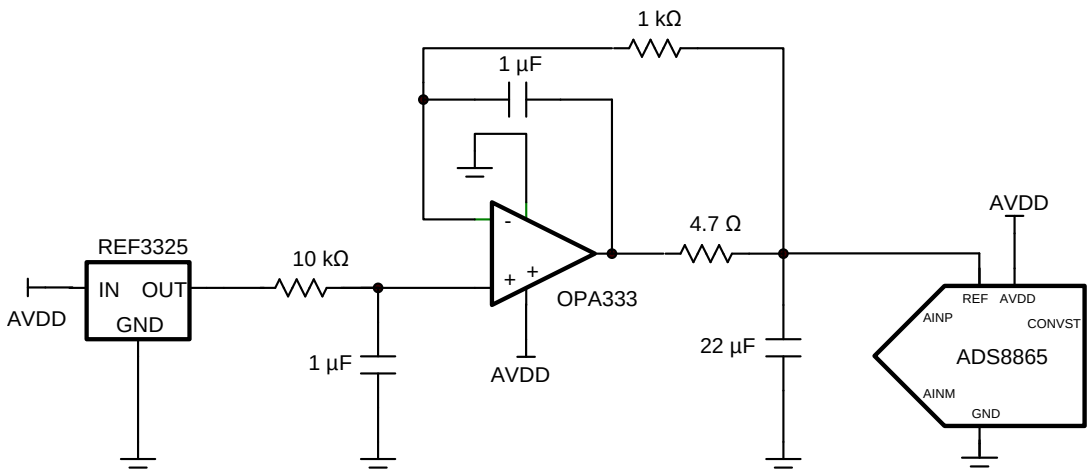

Figure 68. Schematic of Reference Driver Circuit with V_{REF} = 2.5 V DC

The reference buffer is designed using the low-power OPA333 that can operate from a 3.3-V supply at an extremely low quiescent current of 28 µA. The wideband noise contribution from the amplifier is limited by a low-pass filter of a cutoff frequency equal to 1.5 kHz, formed by a 4.7-Ω resistor in combination with a 22-µF capacitor. The 4.7-Ω series resistor creates an additional drop in the reference voltage, which is corrected by a dual-feedback configuration.

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to *18-Bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power < 1mW* (SLAU514).

ADC INPUT DRIVER

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision, 16-bit ADC such as the ADS8865.

Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- *Small-signal bandwidth.* Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter (refer to the *Antialiasing Filter* section) at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in Equation 2:

$$\text{Unity} - \text{Gain Bandwidth} \geq 4 \times \left(\frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \tag{2}$$

- *Noise.* Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in Equation 3.

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6} \right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)}$$

where:

- V_{1/f_AMP_PP} is the peak-to-peak flicker noise in μV_{RMS},
- e_{n_RMS} is the amplifier broadband noise density in $nV/\sqrt{Hz}$,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to '1' in a buffer configuration. (3)

- *Distortion.* Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in Equation 4.

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \tag{4}$$

- *Settling Time.* For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within a 16-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 16-bit accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

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Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the inputs of the ADC during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the input of the ADC, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A differential capacitor, C_{FLT}, is connected across the inputs of the ADC (as shown in Figure 69). This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For the ADS8865, the input sampling capacitance is equal to 59 pF, thus the value of C_{FLT} should be greater than 590 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}}$$

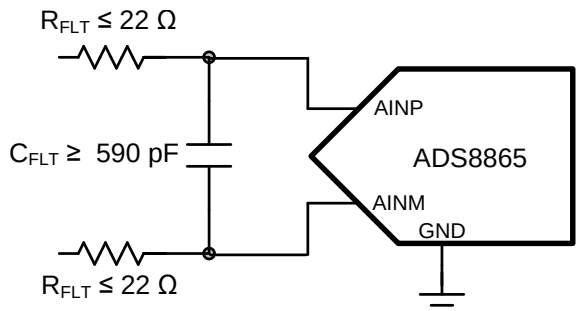

Figure 69. Antialiasing Filter

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For the ADS8865, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22-Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

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APPLICATION CIRCUIT EXAMPLES

This section describes some common application circuits using the ADS8865. These data acquisition (DAQ) blocks are optimized for specific input types and performance requirements of the system. For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; refer to the *Power Supply* section for suggested guidelines.

DAQ Circuit for a 2.5-µs, Full-Scale Step Response

The application circuit shown in Figure 70 is optimized for using the ADS8865 at the maximum-specified throughput of 400 kSPS for a full-scale step input voltage. Such step input signals are common in multiplexed applications when switching between different channels. In a worst-case scenario, one channel is at the negative full-scale (NFS) and the other channel is at the positive full-scale (PFS) voltage, in which case the step size is the full-scale range (FSR) of the ADC when the MUX channel is switched.

In such applications, the primary design requirement is to ensure that the full-scale step input signal settles to 16-bit accuracy at the ADC inputs. This condition is critical to achieve the excellent linearity specifications of the ADC. Therefore, the bandwidth of the antialiasing RC filter should be large enough to allow optimal settling of the input signal during the ADC acquisition time. The filter capacitor helps reduce the sampling charge injection at the ADC inputs, but degrades the phase margin of the driving amplifier, thereby leading to stability issues. Amplifier stability is maintained by the series isolation resistor. Therefore, the component values of the antialiasing filter should be carefully selected to meet the settling requirements of the system as well as to maintain the stability of the input driving amplifiers.

For the input driving amplifiers, key specifications include rail-to-rail input and output swing, high bandwidth, high slew rate, and fast settling time. The OPA350 CMOS amplifier meets all these specification requirements for this circuit with a single-supply and low quiescent current.

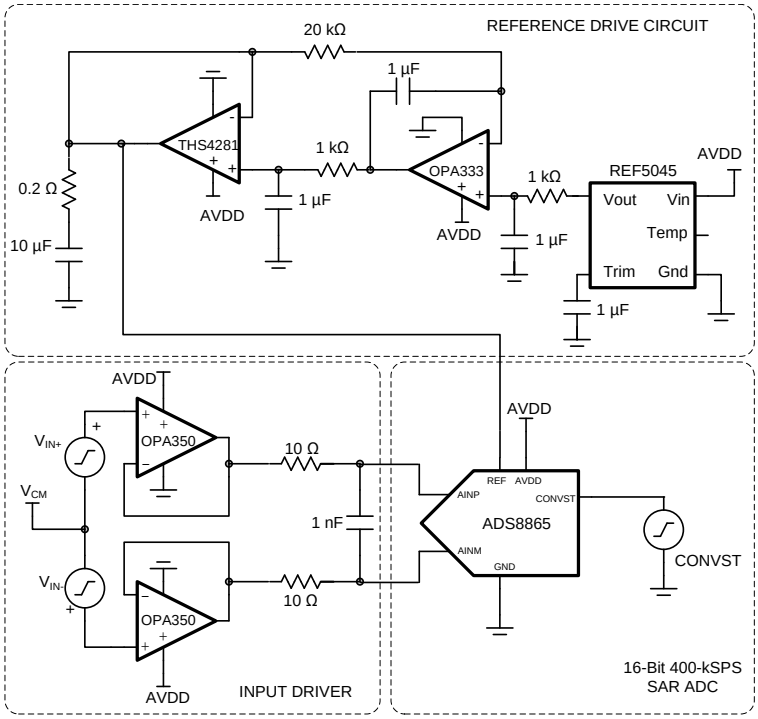

Figure 70. DAQ Circuit for 2.5-µs, Full-Scale Step Response

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to *18-Bit Data Acquisition (DAQ) Block Optimized for 1-µs Full-Scale Step Response* (SLAU512).

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Low-Power DAQ Circuit for Excellent Dynamic Performance at 400 kSPS

The application circuit shown in Figure 71 is optimized for using the ADS8865 at the maximum specified throughput of 400 kSPS for a full-scale sinusoidal signal of 10-kHz frequency. This circuit achieves excellent dynamic performance for the lowest power consumption. The differential ac input signal is processed through low-noise and low-power amplifiers configured as unity-gain buffers and a low-pass, RC filter before being fed into the ADC.

In such applications, the input driver must be low in power and noise as well as able to support rail-to-rail input and output swing with a single supply. A high amplifier bandwidth is also preferred to help attenuate high-frequency distortion. However, oftentimes bandwidth and noise are traded off with the power consumption of the amplifier. This circuit uses the OPA320 as the front-end driving amplifier because this device has a relatively low noise density of 7 nV/√Hz for a maximum-specified quiescent current of 1.45 mA per channel.

The noise contribution from the front-end amplifier is band-limited by the 3-dB bandwidth of the RC filter, which is designed to be 165 kHz in this application. Again, the component values of the antialiasing filter are carefully selected to maintain the stability of the input driving amplifiers.

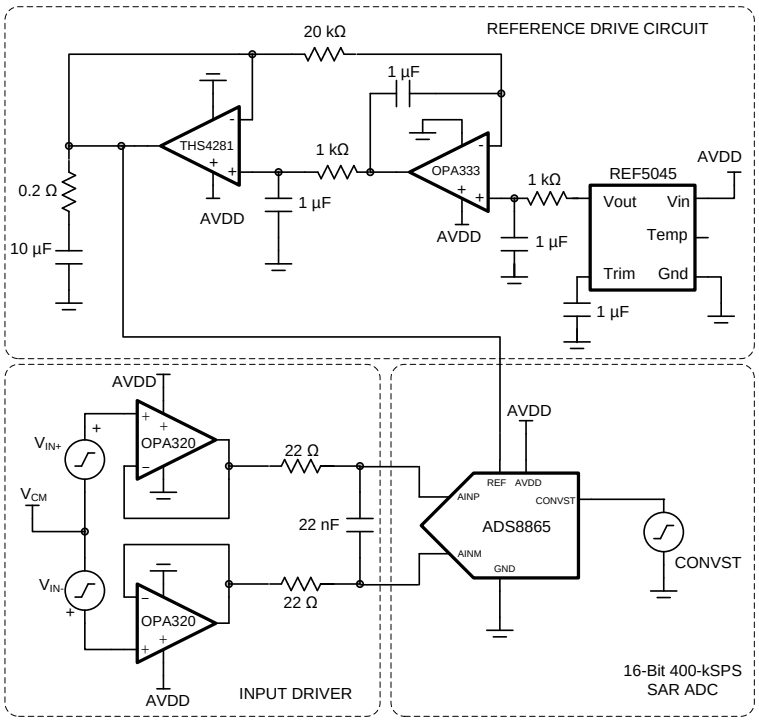

Figure 71. DAQ Circuit for Lowest Power and Excellent Dynamic Performance at 400 kSPS

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Power* (SLAU513).

DAQ Circuit for Lowest Distortion and Noise Performance at 400 kSPS

This section describes two application circuits (Figure 72 and Figure 73) that are optimized for using the ADS8865 with lowest distortion and noise performance at a throughput of 400 kSPS. In both applications, the input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier (FDA) designed in an inverting gain configuration and a low-pass RC filter before being fed into the ADC.

As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the FDA in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the amplifier input. Therefore, these circuits use the low-power THS4521 as an input driver, which provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications.

In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

Differential Input Configuration

The circuit in Figure 72 shows a fully-differential DAQ block optimized for low distortion and noise using the THS4521 and ADS8865. This front-end circuit configuration requires a differential signal at the input of the FDA and provides a differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the V_{OCM} pin of the THS4521 (not shown in Figure 72). To use the complete dynamic range of the ADC, V_{OCM} can be set to V_{REF} / 2 by using a simple resistive divider. However, note that the ADS8865 allows the common-mode input voltage (V_{CM}) to be set to any value in the range of 0 V to V_{REF}.

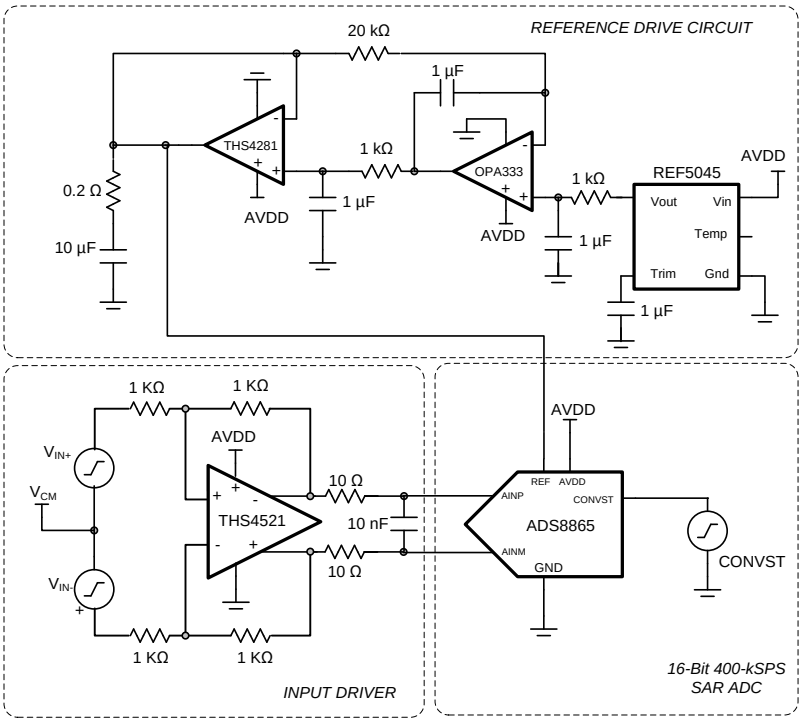

Figure 72. Differential Input DAQ Circuit for Lowest Distortion and Noise at 400 kSPS

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Distortion and Noise* (SLAU515).

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Single-Ended to Differential Configuration

The circuit in Figure 73 shows a single-ended to differential DAQ block optimized for low distortion and noise using the THS4521 and the ADS8865. This front-end circuit configuration requires a single-ended ac signal at the input of the FDA and provides a fully-differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the V_{OCM} pin of the THS4521 (not shown in Figure 73). To use the complete dynamic range of the ADC, V_{OCM} can be set to V_{REF} / 2 by using a simple resistive divider. However, note that the ADS8865 allows the common-mode input voltage (V_{CM}) to be set to any value in the range of 0 V to V_{REF}.

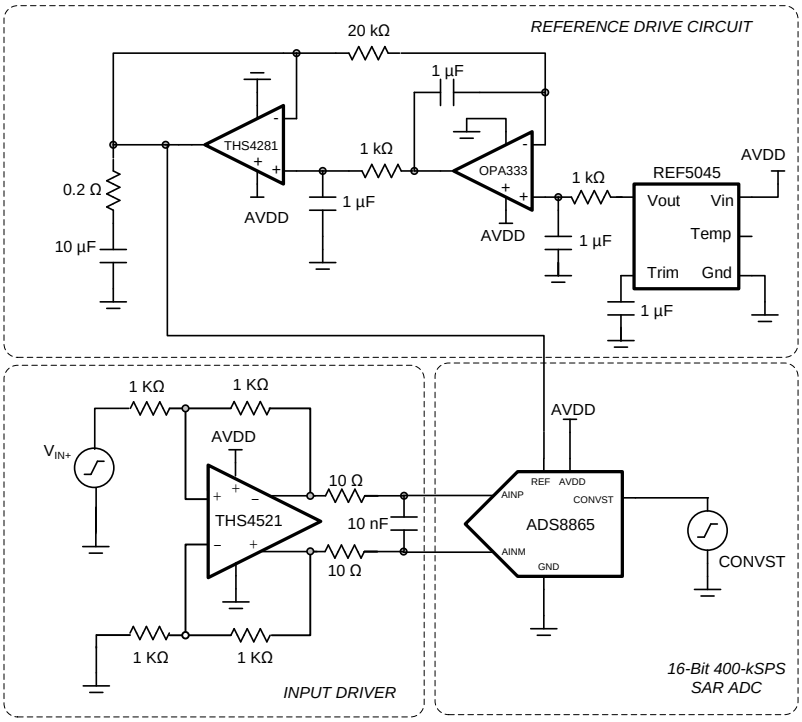

Figure 73. Single-Ended to Differential DAQ Circuit for Lowest Distortion and Noise at 400 kSPS

Ultralow-Power DAQ Circuit at 10 kSPS

The data acquisition circuit shown in Figure 74 is optimized for using the ADS8865 at a reduced throughput of 10 kSPS with ultralow-power consumption (< 1 mW) targeted at portable and battery-powered applications.

In order to save power, this circuit is operated on a single 3.3-V supply. The circuit uses extremely low-power, dual amplifiers (such as the OPA2333) with a maximum quiescent current of 28 µA per channel to drive the ADC inputs. The input amplifiers are configured in a modified unity-gain buffer configuration. The filter capacitor at the ADC inputs attenuates the sampling charge-injection noise from the ADC but effects the stability of the input amplifiers by degrading the phase margin. This attenuation requires a series isolation resistor to maintain amplifier stability. The value of the series resistor is directly proportional to the open-loop output impedance of the driving amplifier to maintain stability, which is high (in the order of kΩ) in the case of low-power amplifiers such as the OPA333. Therefore, a high value of 1 kΩ is selected for the series resistor at the ADC inputs. However, this series resistor creates an additional voltage drop in the signal path, thereby leading to linearity and distortion issues. The dual-feedback configuration used in Figure 74 corrects for this additional voltage drop and maintains system performance at ultralow-power consumption.

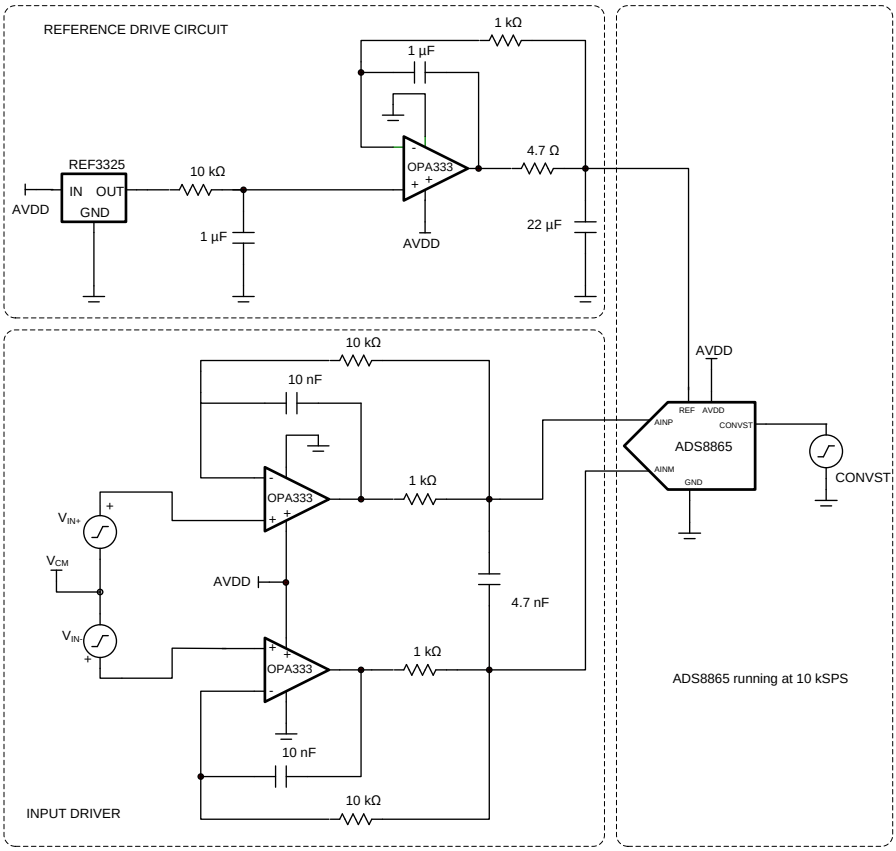

Figure 74. Ultralow-Power DAQ Circuit at 10 kSPS

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, using a similar device, refer to *18-Bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power < 1mW* (SLAU514).

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2013) to Revision A	Page
• Changed *Wide Common-Mode Voltage Range* Features bullet	1
• Changed sub-bullets of *AC and DC Performance* Features bullet	1
• Changed *Full-Scale Step Settling* Features bullet	1
• Deleted last two Applications bullets	1
• Changed *Description* section	1
• Changed front page graphic	1
• Added Family Information, Absolute Maximum Ratings, and Thermal Information tables	2
• Added Electrical Characteristics table	3
• Added *Timing Characteristics* section	5
• Added *Pin Configurations* section	9
• Added *Typical Characteristics* section	10
• Added *Overview* section	17
• Added *Application Information* section	30

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8865IDGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDGS.A	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDGS.B	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCR.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCRG4.B	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865
ADS8865IDRCT.B	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8865

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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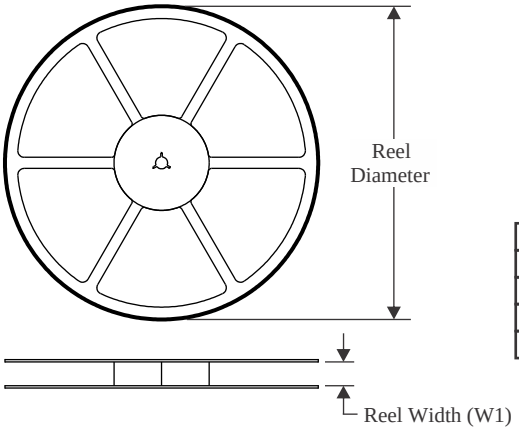
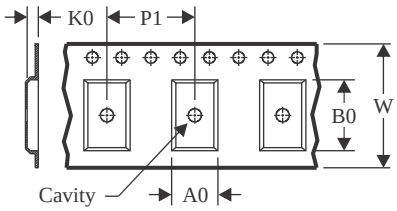
TAPE AND REEL INFORMATION

REEL DIMENSIONS

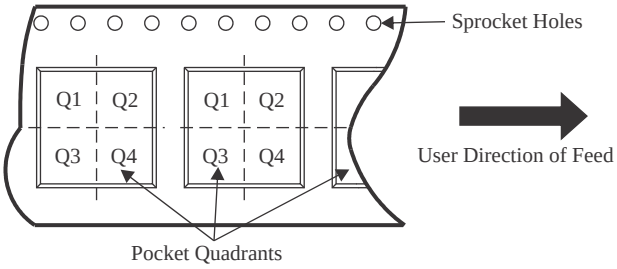


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

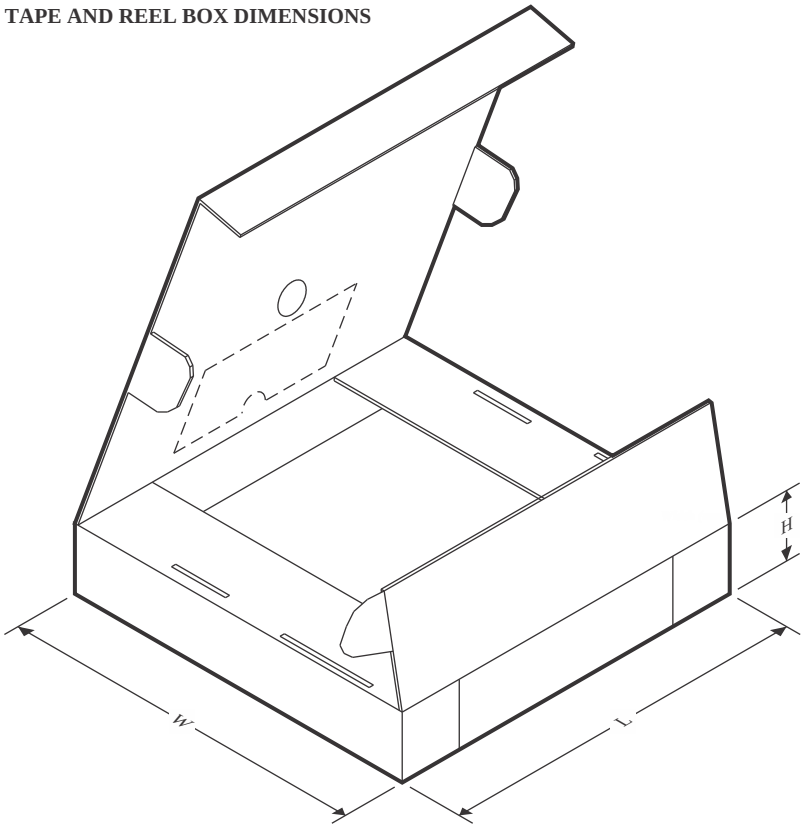
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8865IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8865IDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8865IDRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8865IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

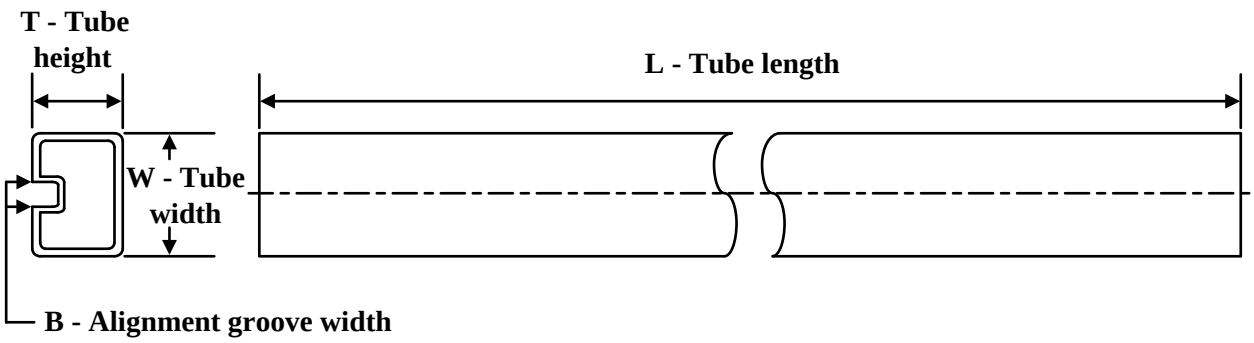
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

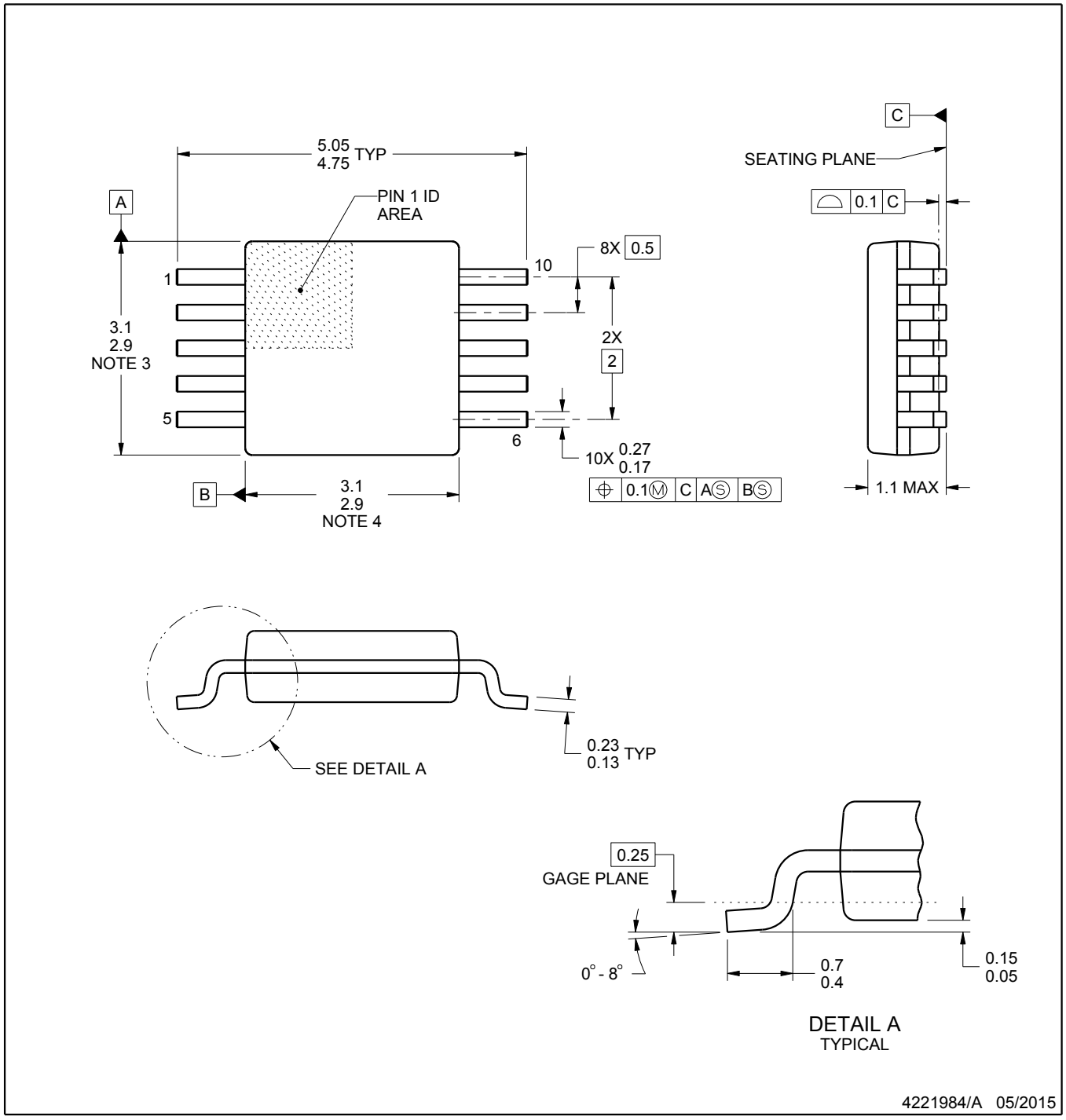
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8865IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS8865IDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8865IDRCRG4	VSON	DRC	10	3000	367.0	367.0	35.0
ADS8865IDRCT	VSON	DRC	10	250	213.0	191.0	35.0

TUBE



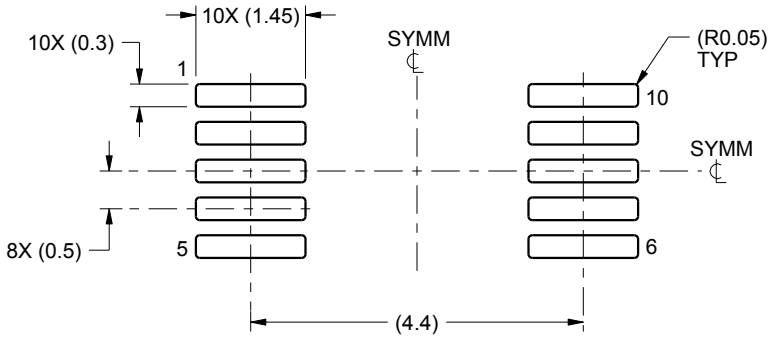
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS8865IDGS	DGS	VSSOP	10	80	330.2	6.6	3005	1.88
ADS8865IDGS.A	DGS	VSSOP	10	80	330.2	6.6	3005	1.88
ADS8865IDGS.B	DGS	VSSOP	10	80	330.2	6.6	3005	1.88

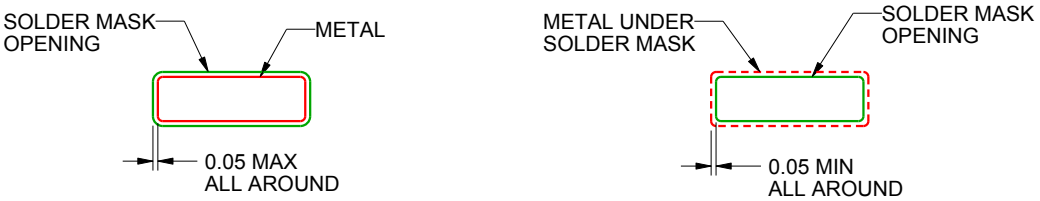


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

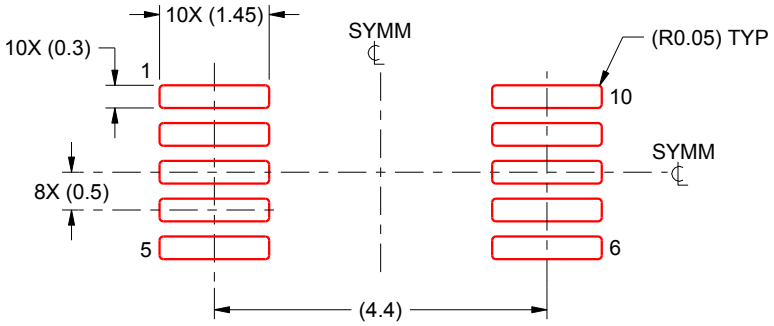
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

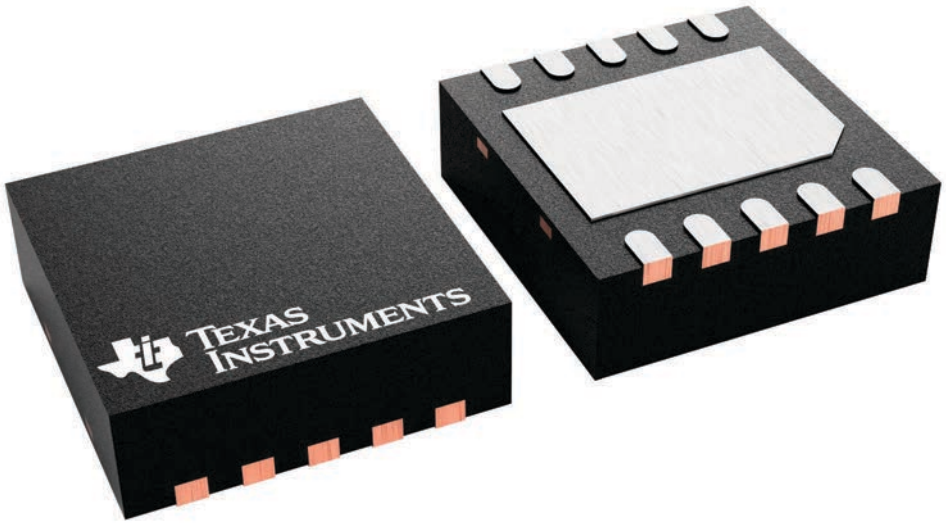
DRC 10

VSON - 1 mm max height

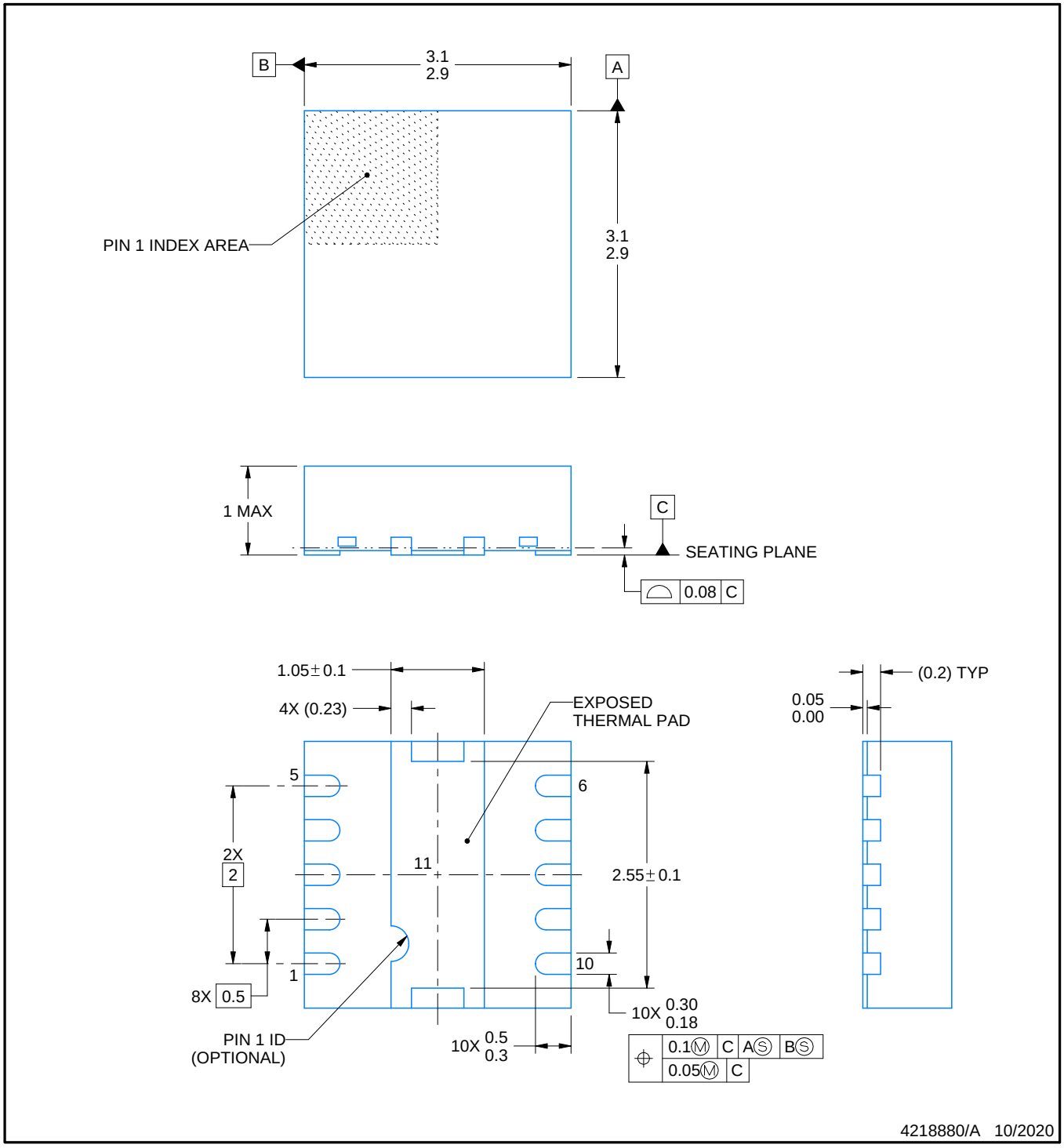
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

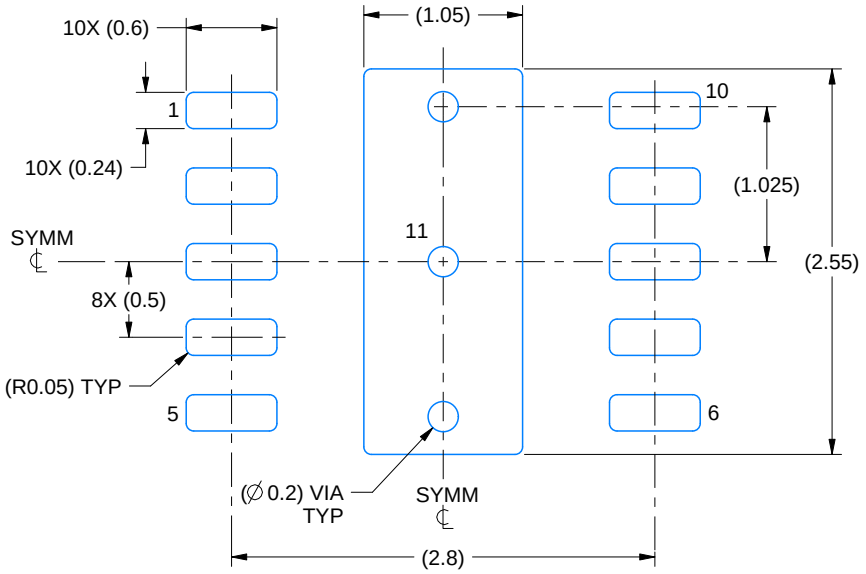


4226193/A

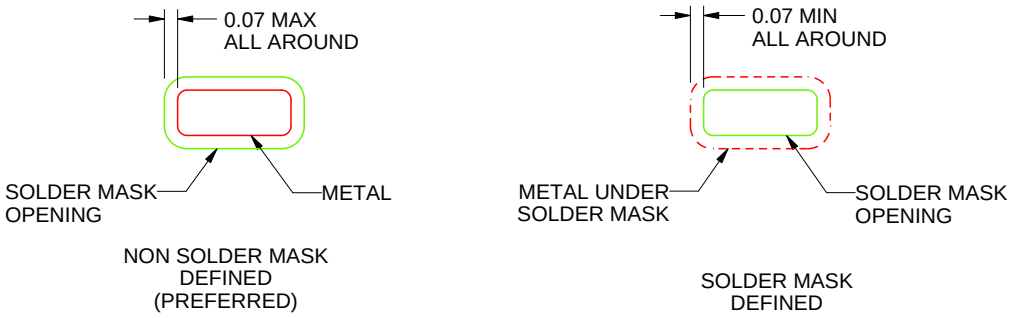


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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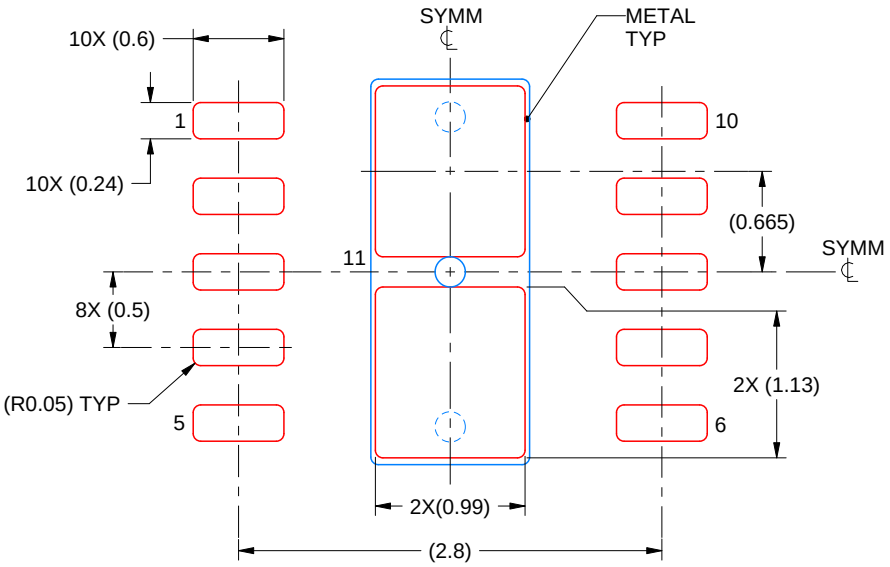
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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