LM25085A 42V Constant On-Time PFET Buck Switching Controller with 0.9V Reference

Check for Samples: LM25085A

FEATURES

- **Wide 4.5V to 42V Input Voltage Range**
- **Adjustable Current Limit using $R_{DS(ON)}$ or a Current Sense Resistor**
- **Programmable Switching Frequency to 1MHz**
- **No Loop Compensation Required**
- **Ultra-Fast Transient Response**
- **Nearly Constant Operating Frequency with Line and Load Variations**
- **Adjustable Output Voltage from 0.9V**
- **Precision ±2% Feedback Reference**
- **Capable of 100% Duty Cycle Operation**
- **Internal Soft-Start Timer**
- **Integrated High Voltage Bias Regulator**
- **Thermal Shutdown**

PACKAGE

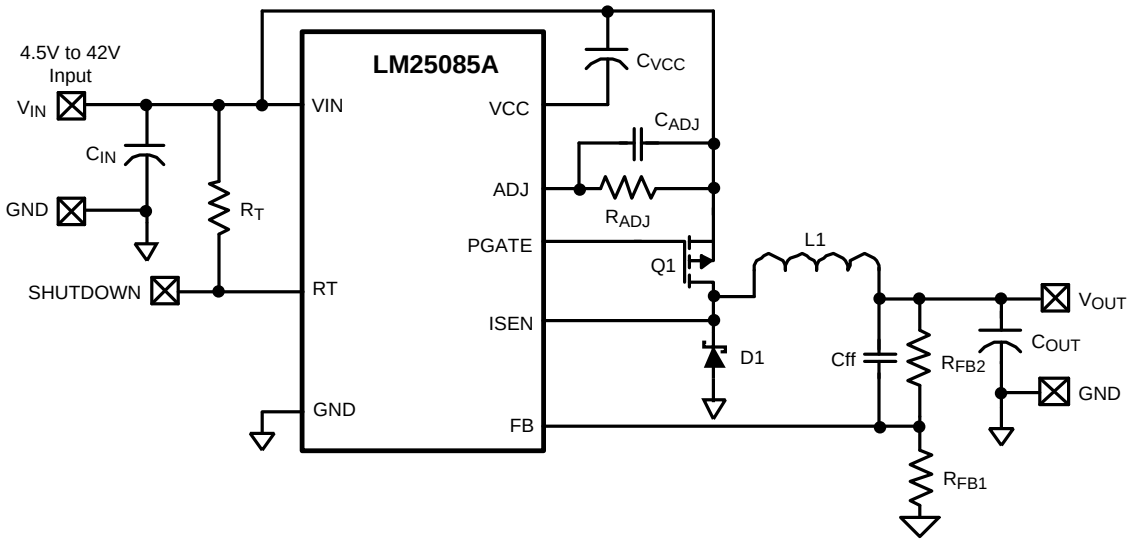
- **HVSSOP-PowerPAD-8**
- **VSSOP-8**
- **WSON-8 (3 mm x 3 mm)**

DESCRIPTION

The LM25085A is a functional variant of the LM25085 COT PFET Buck Switching Controller. The functional differences of the LM25085A are: The feedback reference voltage is 0.9V, the forced off-time after current limit detection is longer, and the soft-start time is shorter (1.8 ms).

The LM25085A is a high efficiency PFET switching regulator controller that can be used to quickly and easily develop a small, efficient buck regulator for a wide range of applications. This high voltage controller contains a PFET gate driver and a high voltage bias regulator which operates over a wide 4.5V to 42V input range. The constant on-time regulation principle requires no loop compensation, simplifies circuit implementation, and results in ultra-fast load transient response. The operating frequency remains nearly constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The PFET architecture allows 100% duty cycle operation for a low dropout voltage. Either the $R_{DS(ON)}$ of the PFET or an external sense resistor can be used to sense current for over-current detection.

Typical Application, Basic Step Down Controller



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009–2013, Texas Instruments Incorporated

Connection Diagram

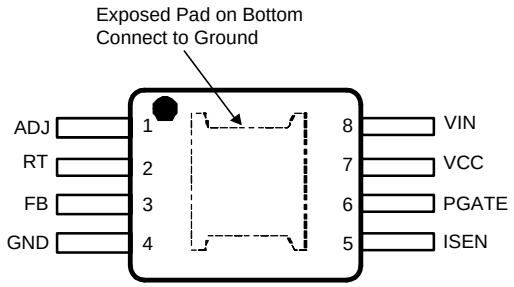


Figure 1. Top View
8-Lead HVSSOP

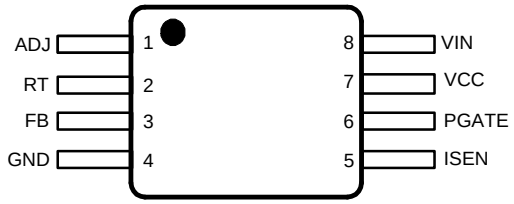


Figure 2. Top View
8-Lead VSSOP

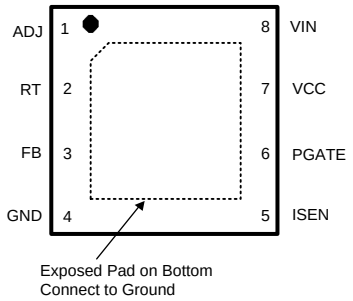


Figure 3. Top View
8-Lead WSON

PIN DESCRIPTIONS

Pin No.	Name	Description	Application Information
1	ADJ	Current Limit Adjust	The current limit threshold is set by an external resistor from VIN to ADJ in conjunction with the external sense resistor or the PFET's $R_{DS(ON)}$.
2	RT	On-time control and shutdown	An external resistor from VIN to RT sets the buck switch on-time and switching frequency. Grounding this pin shuts down the controller.
3	FB	Voltage Feedback from the regulated output	Input to the regulation and over-voltage comparators. The regulation level is 0.9V.
4	GND	Circuit Ground	Ground reference for all internal circuitry
5	ISEN	Current sense input for current limit detection.	Connect to the PFET drain when using $R_{DS(ON)}$ current sense. Connect to the PFET source and the sense resistor when using a current sense resistor.
6	PGATE	Gate Driver Output	Connect to the gate of the external PFET.
7	VCC	Output of the gate driver bias regulator	Output of the negative voltage regulator (relative to VIN) that biases the PFET gate driver. A low ESR capacitor is required from VIN to VCC, located as close as possible to the pins.
8	VIN	Input supply voltage	The operating input range is from 4.5V to 42V. A low ESR bypass capacitor must be located as close as possible to the VIN and GND pins.
	EP	Exposed Pad	Exposed pad on the underside of the package (HVSSOP-PowerPAD-8 and WSON only). This pad is to be soldered to the PC board ground plane to aid in heat dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2009–2013, Texas Instruments Incorporated

Absolute Maximum Ratings [1][2]

VIN to GND	-0.3V to 45V
ISEN to GND	-0.3V to V_{IN} + 0.3V
ADJ to GND	-0.3V to V_{IN} + 0.3V
RT, FB to GND	-0.3V to 7V
VIN to VCC, VIN to PGATE	-0.3V to 10V
ESD Rating [3] Human Body Model	 2kV
Storage Temperature Range	-65°C to +150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings [1]

VIN Voltage	4.5V to 42V
Junction Temperature	−40°C to + 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface** type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 24V, R_T = 100 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN Pin						
I_{IN}	Operating current	Non-switching, FB = 1.05V [1]		1.25	**1.75**	mA
I_Q	Shutdown current	RT = 0V [1]		175	**300**	µA
VCC Regulator [2]						
$V_{CC(reg)}$	VIN - VCC	Vin = 9V, FB = 1.05V, ICC = 0 mA	**6.9**	7.7	**8.5**	V
		Vin = 9V, FB = 1.05V, ICC = 20 mA		7.7		V
		Vin = 42V, FB = 1.05V, ICC = 0 mA		7.7		V
$UVLO_{Vcc}$	VCC under-voltage lock-out threshold	V_{CC} increasing		3.8		V
	$UVLO_{Vcc}$ hysteresis	V_{CC} decreasing		260		mV
$V_{CC(CL)}$	VCC Current Limit	FB = 1.05V	**20**	40		mA
PGATE Pin						
$V_{PGATE(HI)}$	PGATE High voltage	PGATE Pin = Open	**V_{IN} -0.1**	V_{IN}		V
$V_{PGATE(LO)}$	PGATE Low voltage	PGATE Pin = Open		V_{CC}	**V_{CC}+0.1**	V
$V_{PGATE(HI)4.5}$	PGATE High Voltage at Vin = 4.5V	PGATE Pin = Open	**V_{IN} -0.1**	V_{IN}		V
$V_{PGATE(LO)4.5}$	PGATE Low Voltage at Vin = 4.5V	PGATE Pin = Open		V_{CC}	**V_{CC}+0.1**	V
I_{PGATE}	Driver Output Source Current	VIN = 12V, PGATE = VIN - 3.5V		1.75		A
	Driver Output Sink Current	VIN = 12V, PGATE = VIN - 3.5V		1.5		A
R_{PGATE}	Driver Output Resistance	Source current = 500 mA		2.3		Ω
		Sink current = 500 mA		2.3		Ω
Current Limit Detection						
I_{ADJ}	ADJUST pin current source	V_{ADJ} = 22.5V	**32**	40	**48**	µA
$V_{CL\ OFFSET}$	Current limit comparator offset	V_{ADJ} = 22.5V, V_{ADJ} - V_{ISEN}	**-9**	0	**9**	mV

(1) Operating current and shutdown current do not include the current in the R_T resistor.
(2) V_{CC} provides self bias for the internal gate drive.

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface** type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 24V, R_T = 100 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RT Pin						
RT_{SD}	Shutdown threshold	RT Pin voltage rising		0.73		V
RT_{HYS}	Shutdown threshold hysteresis			50		mV
On-Time						
t_{ON-1}	On-time	VIN = 4.5V, R_T = 100 kΩ	**3.5**	5	**7.15**	µs
t_{ON-2}		VIN = 24V, R_T = 100 kΩ	**560**	720	**870**	ns
t_{ON-3}		VIN = 42V, R_T = 100 kΩ	**329**	415	**500**	ns
t_{ON-4}	Minimum on-time in current limit (3)	VIN = 24V, 25 mV overdrive at ISEN	**55**	140	**235**	ns
Off-Time						
$t_{OFF(CL1)}$	Off-time (current limit) (3)	VIN = 12V, V_{FB} = 0V	**5.56**	8	**10.96**	µs
$t_{OFF(CL2)}$		VIN = 12V, V_{FB} = 0.75V	**2.59**	3.7	**5.16**	µs
$t_{OFF(CL3)}$		VIN = 24V, V_{FB} = 0V	**9.03**	13.2	**18.1**	µs
$t_{OFF(CL4)}$		VIN = 24V, V_{FB} = 0.75V	**4.29**	6	**8.54**	µs
Regulation and Over-Voltage Comparators (FB Pin)						
V_{REF}	FB regulation threshold		**0.882**	0.9	**0.918**	V
V_{OV}	FB over-voltage threshold	Measured with respect to V_{REF}		350		mV
I_{FB}	FB bias current			10		nA
Soft-Start Function						
t_{SS}	Soft-start time		**1.16**	1.8	**3.15**	ms
Thermal Shutdown						
T_{SD}	Junction shutdown temperature	Junction temperature rising		170		°C
T_{HYS}	Junction shutdown hysteresis			20		°C
Thermal Resistance (4)						
θ_{JA}	Junction to ambient, 0 LFPM air flow (5)	VSSOP-8 package		126		°C/W
		HVSSOP-PowerPAD-8 package		46		
		WSON-8 package		54		
θ_{JC}	Junction to case, 0 LFPM air flow (5)	VSSOP-8 package		29		°C/W
		HVSSOP-PowerPAD-8 package		5.5		
		WSON-8 package		9.1		

(3) The tolerance of the minimum on-time (t_{ON}-4) and the current limit off-times ($t_{OFF(CL1)}$ through ($t_{OFF(CL4)}$) track each other over process and temperature variations. A device which has an on-time at the high end of the range will have an off-time that is at the high end of its range.
(4) For detailed information on soldering plastic VSSOP and WSON packages visit www.ti.com/packaging.
(5) Tested on a 4 layer JEDEC board. Four vias provided under the exposed pad. See JEDEC standards JESD51-5 and JESD51-7.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 24V.

Efficiency (Circuit of Figure 28)

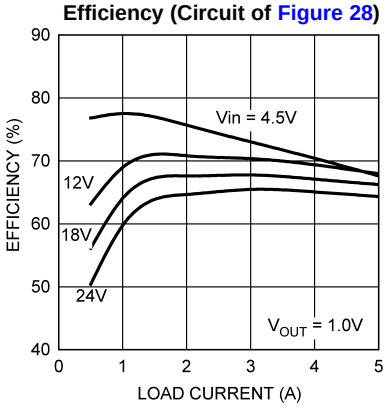


Figure 4.

Input Operating Current vs. V_{IN}

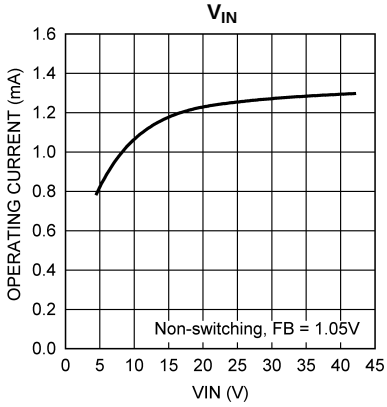


Figure 5.

Shutdown Current vs. V_{IN}

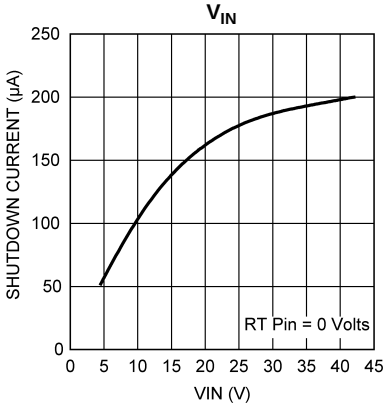


Figure 6.

V_{CC} vs. V_{IN}

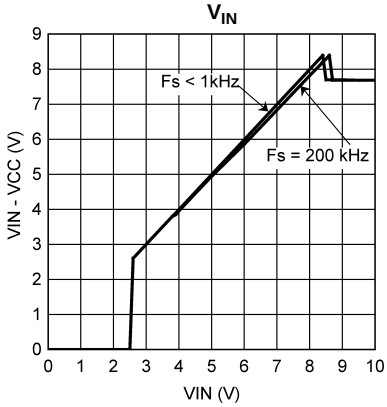


Figure 7.

V_{CC} vs. I_{CC}

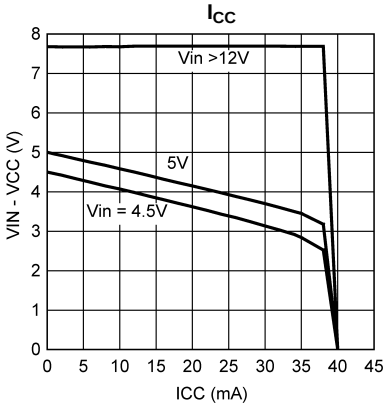


Figure 8.

On-Time vs. R_T and V_{IN}

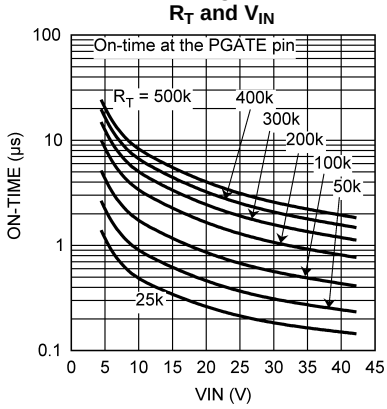


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 24V.

Off-Time vs. V_{IN} and V_{FB}

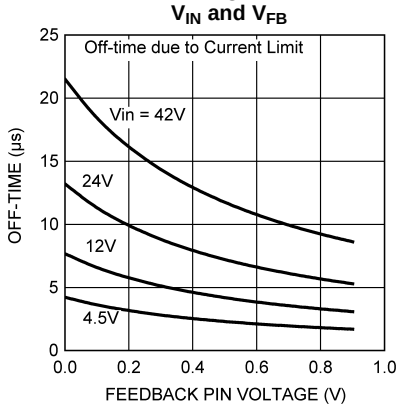


Figure 10.

Voltage at the RT Pin

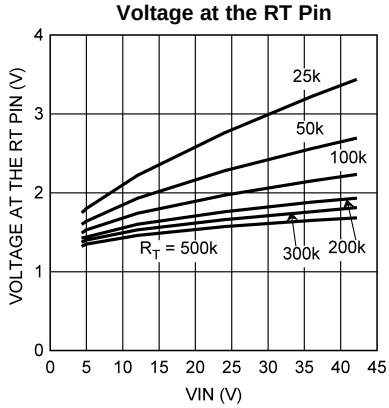


Figure 11.

ADJ Pin Current vs. V_{IN}

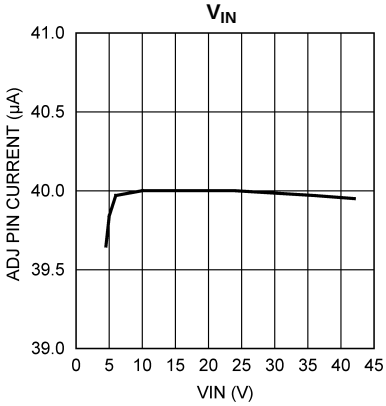


Figure 12.

Input Operating Current vs. Temperature

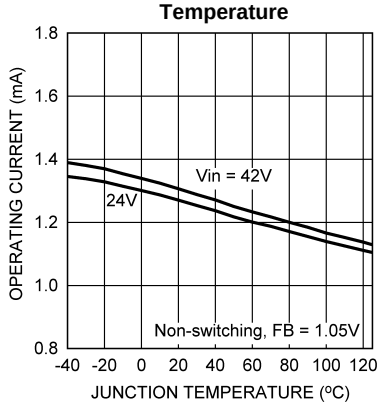


Figure 13.

Shutdown Current vs. Temperature

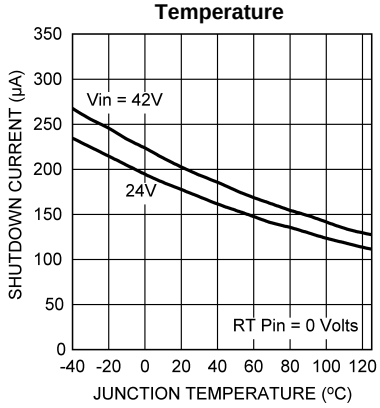


Figure 14.

VCC vs. Temperature

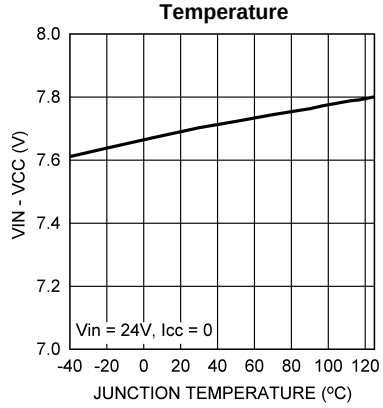


Figure 15.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 24V.

On-Time vs. Temperature

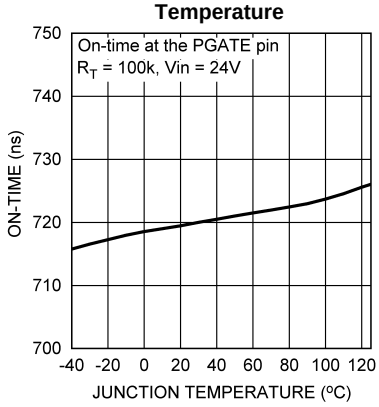


Figure 16.

Minimum On-Time vs. Temperature

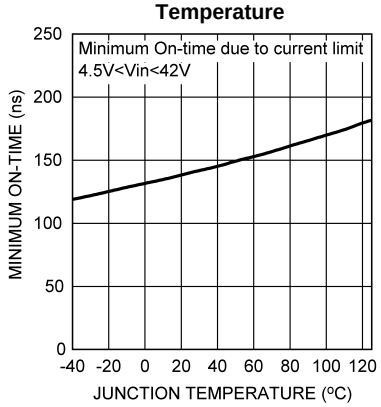


Figure 17.

Off-Time vs. Temperature

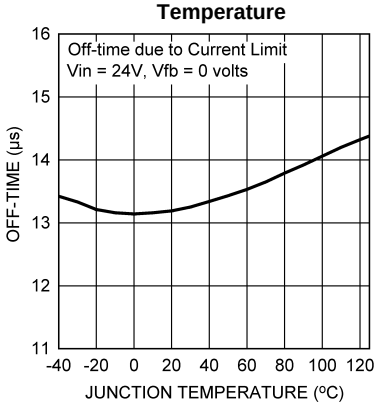


Figure 18.

Current Limit Comparator Offset vs. Temperature

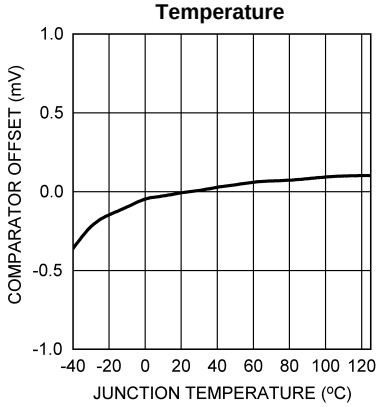


Figure 19.

ADJ Pin Current vs. Temperature

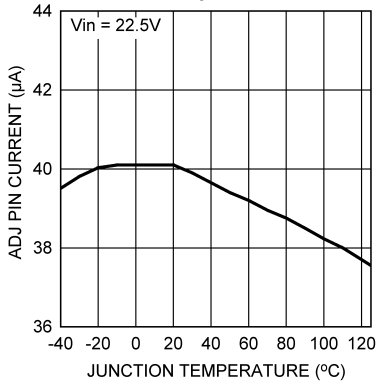


Figure 20.

PGATE Driver Output Resistance vs. Temperature

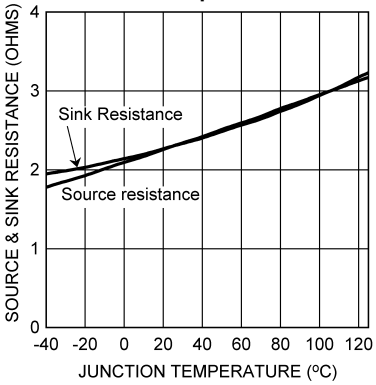


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 24V.

Feedback Reference Voltage vs. Temperature

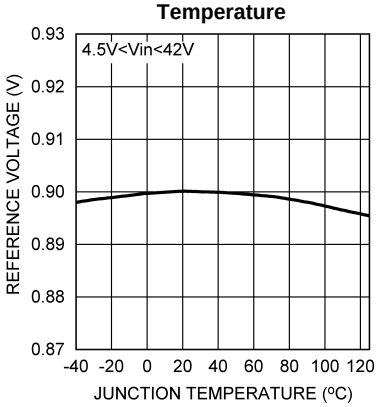


Figure 22.

Soft-Start Time vs. Temperature

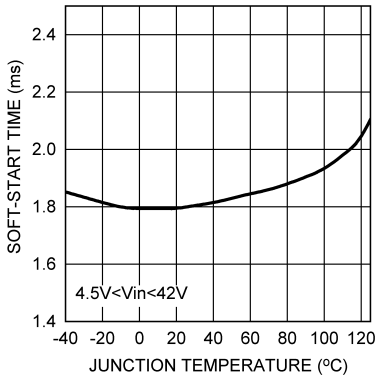


Figure 23.

RT Pin Shutdown Threshold vs. Temperature

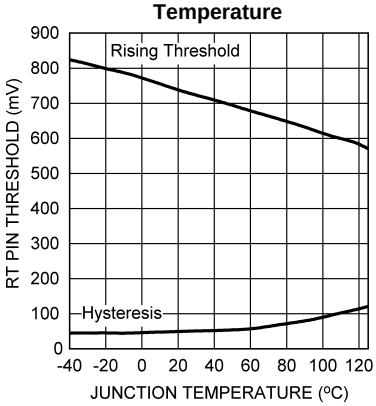
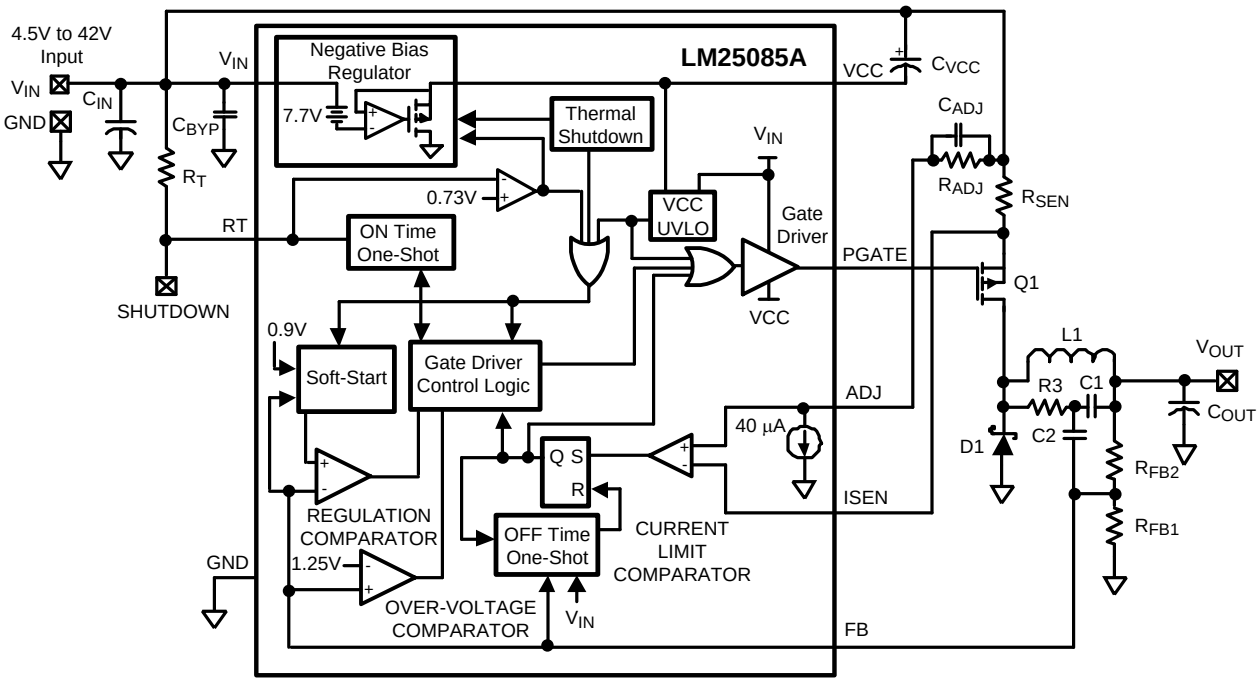


Figure 24.

Copyright © 2009–2013, Texas Instruments Incorporated

Block Diagram



Sense resistor method shown for current limit detection.
Minimum output ripple configuration shown.

FUNCTIONAL DESCRIPTION

OVERVIEW

The LM25085A is a PFET buck (step-down) DC-DC controller using the constant on-time (COT) control principle. The input operating voltage range of the LM25085A is 4.5V to 42V. The use of a PFET in a buck regulator greatly simplifies the gate drive requirements and allows for 100% duty cycle operation to extend the regulation range when operating at low input voltage. However, PFET transistors typically have higher on-resistance and gate charge when compared to similarly rated NFET transistors. Consideration of available PFETs, input voltage range, gate drive capability of the LM25085A, and thermal resistances indicate an upper limit of 10A for the load current for LM25085A applications. Constant on-time control is implemented using an on-time one-shot that is triggered by the feedback signal. During the off-time, when the PFET (Q1) is off, the load current is supplied by the inductor and the output capacitor. As the output voltage falls, the voltage at the feedback comparator input (FB) falls below the regulation threshold. When this occurs Q1 is turned on for the one-shot period which is determined by the input voltage (V_{IN}) and the R_T resistor. During the on-time the increasing inductor current increases the voltage at FB above the feedback comparator threshold. For a buck regulator the basic relationship between the on-time, off-time, input voltage and output voltage is:

$$\text{Duty Cycle} = \frac{V_{OUT}}{V_{IN}} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times F_S \tag{1}$$

where Fs is the switching frequency. Equation 1 is valid only in continuous conduction mode (inductor current does not reach zero). Since the LM25085A controls the on-time inversely proportional to V_{IN}, the switching frequency remains relatively constant as V_{IN} is varied. If the input voltage falls to a level that is equal to or less than the regulated output voltage Q1 is held on continuously (100% duty cycle) and V_{OUT} is approximately equal to V_{IN}.

The COT control scheme, with the feedback signal applied to a comparator rather than an error amplifier, requires no loop compensation, resulting in very fast load transient response.

The LM25085A is available in both an 8 pin HVSSOP-PowerPAD package and an 8 pin WSON package with an exposed pad to aid in heat dissipation. An 8 pin VSSOP package without an exposed pad is also available.

REGULATION CONTROL CIRCUIT

The LM25085A buck DC-DC controller employs a control scheme based on a comparator and a one-shot on-timer, with the output voltage feedback compared to an internal reference voltage (0.9V). When the FB pin voltage falls below the feedback reference, Q1 is switched on for a time period determined by the input voltage and a programming resistor (R_T). Following the on-time Q1 remains off until the FB voltage falls below the reference. Q1 is then switched on for another on-time period. The output voltage is set by the feedback resistors (R_{FB1}, R_{FB2} in Block Diagram). The regulated output voltage is calculated as follows:

$$V_{OUT} = 0.9V \times (R_{FB2} + R_{FB1}) / R_{FB1} \tag{2}$$

The feedback voltage supplied to the FB pin is applied to a comparator rather than a linear amplifier. For proper operation sufficient ripple amplitude is necessary at the FB pin to switch the comparator at regular intervals with minimum delay and noise susceptibility. This ripple is normally obtained from the output voltage ripple attenuated through the feedback resistors. The output voltage ripple is a result of the inductor's ripple current passing through the output capacitor's ESR, or through a resistor in series with the output capacitor. Multiple methods are available to ensure sufficient ripple is supplied to the FB pin, and three different configurations are discussed in Applications Information.

When in regulation, the LM25085A operates in continuous conduction mode at medium to heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode the inductor's current is always greater than zero, and the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. In discontinuous conduction mode, where the inductor's current reaches zero during the off-time, the operating frequency is lower than in continuous conduction mode and varies with load current. Conversion efficiency is maintained at light loads since the switching losses are reduced with the reduction in load and frequency.

If the voltage at the FB pin exceeds 1.25V due to a transient overshoot or excessive ripple at V_{OUT} the internal over-voltage comparator immediately switches off Q1. The next on-time period starts when the voltage at FB falls below the feedback reference voltage.

Copyright © 2009–2013, Texas Instruments Incorporated

ON-TIME TIMER

The on-time of the PFET gate drive output (PGATE pin) is determined by the resistor (R_T) and the input voltage (V_{IN}), and is calculated from:

$$t_{ON} = \frac{1.45 \times 10^{-7} \times (R_T + 1.4)}{(V_{IN} - 1.56V + R_T/3167)} + 50\ ns \tag{3}$$

where R_T is in kΩ. The minimum on-time, which occurs at maximum V_{IN}, should not be set less than 150 ns (see CURRENT LIMITING). The buck regulator effective on-time, measured at the SW node (junction of Q1, L1, and D1) is typically longer than that calculated in Equation 3 due to the asymmetric delay of the PFET. The on-time difference caused by the PFET switching delay can be estimated as the difference of the turn-off and turn-on delays listed in the PFET data sheet. Measuring the difference between the on-time at the PGATE pin versus the SW node in the actual application circuit is also recommended.

In continuous conduction mode, the inverse relationship of t_{ON} with V_{IN} results in a nearly constant switching frequency as V_{IN} is varied. The operating frequency can be calculated from:

$$F_S = \frac{V_{OUT} \times (V_{IN} - 1.56V + R_T/3167)}{V_{IN} \times [(1.45 \times 10^{-7} \times (R_T + 1.4)) + (t_D \times (V_{IN} - 1.56V + R_T/3167))]} \tag{4}$$

where R_T is in kΩ, and t_D is equal to 50 ns plus the PFET's delay difference. To set a specific continuous conduction mode switching frequency (F_S), the R_T resistor is determined from the following:

$$R_T = \frac{V_{OUT} \times (V_{IN} - 1.56V)}{1.45 \times 10^{-7} \times V_{IN} \times F_S} - \frac{t_D \times (V_{IN} - 1.56V)}{1.45 \times 10^{-7}} - 1.4 \tag{5}$$

where R_T is in kΩ. A simplified version of Equation 6 at V_{IN} = 12V, and t_D = 100 ns, is:

$$R_T = \frac{V_{OUT} \times 6 \times 10^6}{F_S} - 8.6$$

For V_{IN} = 42V and t_D = 100 ns, the simplified equation is:

$$R_T = \frac{V_{OUT} \times 6.64 \times 10^6}{F_S} - 29.3$$

SHUTDOWN

The LM25085A can be shutdown by grounding the RT pin (see Figure 25). In this mode the PFET is held off, and the VCC regulator is disabled. The internal operating current is reduced to the value shown in the graph "Shutdown current vs. VIN". The shutdown threshold at the RT pin is ≅0.73V, with ≅50 mV of hysteresis. Releasing the pin enables normal operation. The RT pin must not be forced high during normal operation.

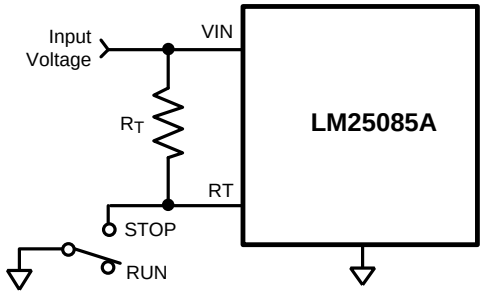


Figure 25. Shutdown Implementation

CURRENT LIMITING

The LM25085A current limiting operates by sensing the voltage across either the $R_{DS(ON)}$ of Q1, or a sense resistor, during the on-time and comparing it to the voltage across the resistor R_{ADJ} (see Figure 26). The current limit function is much more accurate and stable over temperature when a sense resistor is used. The $R_{DS(ON)}$ of a MOSFET has a wide process variation and a large temperature coefficient.

If the voltage across $R_{DS(ON)}$ of Q1, or the sense resistor, is greater than the voltage across R_{ADJ}, the current limit comparator switches to turn off Q1. Current sensing is disabled for a blanking time of ≅100 ns at the beginning of the on-time to prevent false triggering of the current limit comparator due to leading edge current spikes. Because of the blanking time and the turn-on and turn-off delays created by the PFET, the on-time at the PGATE pin should not be set less than 150 ns. An on-time shorter than that may prevent the current limit detection circuit from properly detecting an over-current condition. The duration of the subsequent forced off-time is a function of the input voltage and the voltage at the FB pin, as shown in Figure 10. The longer-than-normal forced off-time allows the inductor current to decrease to a low level before the next on-time. This cycle-by-cycle monitoring, followed by a forced off-time, provides effective protection from output load faults over a wide range of operating conditions.

The voltage across the R_{ADJ} resistor is set by an internal 40 µA current sink at the ADJ pin. When using Q1's $R_{DS(ON)}$ for sensing, the current at which the current limit comparator switches is calculated from:

$$I_{CL} = 40\ \mu A \times R_{ADJ}/R_{DS(ON)} \tag{6}$$

When using a sense resistor (R_{SEN}) the thrshold of the current limit comparator is calculated from:

$$I_{CL} = 40\ \mu A \times R_{ADJ}/R_{SEN} \tag{7}$$

When using Equation 6 or Equation 7, the tolerances for the ADJ pin current sink and the offset of the current limit comparator should be included to ensure the resulting minimum current limit is not less than the required maximum switch current. Simultaneously increasing the values of R_{ADJ} and R_{SEN} decreases the effects of the current limit comparator offset, but at the expense of higher power dissipation. When using a sense resistor, the R_{SEN} resistor value should be chosen within the practical limitations of power dissipation and physical size. For example, for a 10A current limit, setting R_{SEN} = 0.005Ω results in a power dissipation as high as 0.5W. Current sense connections to the R_{SEN} resistor, or to Q1, must be Kelvin connections to ensure accuracy.

The C_{ADJ} capacitor filters noise from the ADJ pin, and helps prevent unintended switching of the current limit comparator due to input voltage transients. The recommended value for C_{ADJ} is 1000 pF.

CURRENT LIMIT OFF-TIME

When the current through Q1 exceeds the current limit threshold, the LM25085A forces an off-time longer than the normal off-time defined by Equation 1. See Figure 10, or calculate the current limit off-time from the following equation:

$$t_{OFF(CL)} = \frac{8 \times 10^{-6} \times ((V_{IN}/31) + 0.15)}{(V_{FB} \times 0.93) + 0.56V} \tag{8}$$

where V_{IN} is the input voltage, and V_{FB} is the voltage at the FB pin at the time current limit was detected. This feature is necessary to allow the inductor current to decrease sufficiently to offset the current increase which occurred during the on-time. During the on-time, the inductor current increases an amount equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L} \tag{9}$$

During the off-time the inductor current decreases due to the reverse voltage applied across the inductor by the output voltage, the freewheeling diode's forward voltage (V_{FD}), and the voltage drop due to the inductor's series resistance (V_{ESR}). The current decrease is equal to:

$$\Delta I = \frac{(V_{OUT} + V_{FD} + V_{ESR}) \times t_{OFF}}{L} \tag{10}$$

Copyright © 2009–2013, Texas Instruments Incorporated

The on-time in Equation 9 is shorter than the normal on-time since the PFET is shut off when the current limit threshold is crossed. If the off-time is not long enough, such that the current decrease (Equation 10) is less than the current increase (Equation 9), the current levels are higher at the start of the next on-time. This results in a further decrease in on-time, since the current limit threshold is crossed sooner. A balance is reached when the current changes in Equation 9 and Equation 10 are equal. The worst case situation is that of a direct short circuit at the output terminals, where V_{OUT} = 0 volts, as that results in the largest current increase during the on-time, and the smallest decrease during the off-time. The sum of the diode's forward voltage and the inductor's ESR voltage must be sufficient to ensure current runaway does not occur. Using Equation 9 and Equation 10, this requirement can be stated as:

$$V_{FD} + V_{ESR} \geq \frac{V_{IN} \times t_{ON}}{t_{OFF}} \tag{11}$$

For t_{ON} in Equation 11 use the minimum on-time at the SW node. To determine this time period add the "Minimum on-time in current limit" specified in Electrical Characteristics (t_{ON}-4) to the difference of the turn-off and turn-on delays of the PFET. For t_{OFF} use the value in Figure 10, or use Equation 8, where V_{FB} is equal to zero volts. When using the minimum or maximum limits of those specifications to determine worst case situations, the tolerance of the minimum on-time (t_{ON}-4) and the current limit off-times ($t_{OFF(CL1)}$ through $t_{OFF(CL4)}$) track each other over the process and temperature variations. A device which has an on-time at the high end of the range will have an off-time that is at the high end of its range.

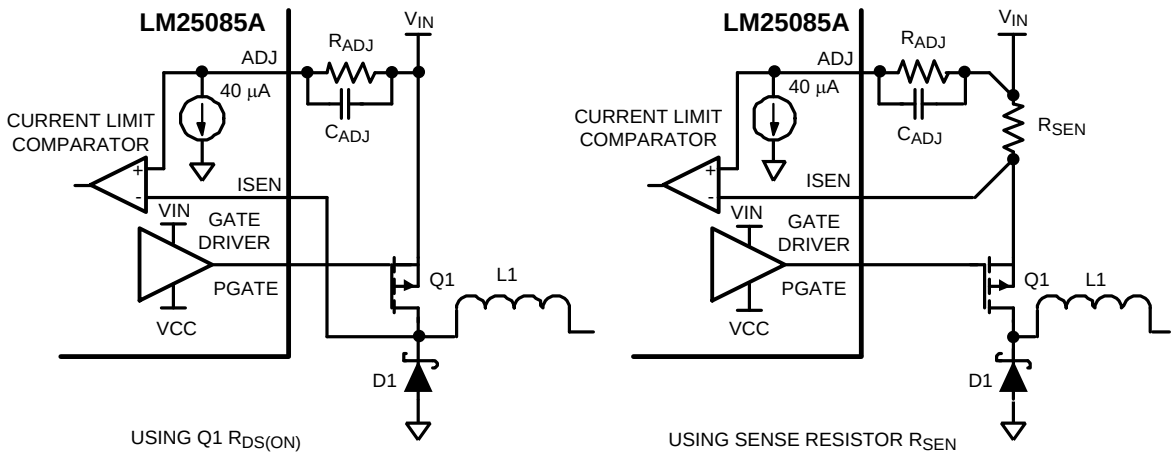


Figure 26. Current Limit Sensing

VCC REGULATOR

The VCC regulator provides a regulated voltage between the VIN and the VCC pins to provide the bias and gate current for the PFET gate driver. The 0.47 µF capacitor at the VCC pin must be a low ESR capacitor, preferably ceramic as it provides the high surge current for the PFET's gate at each turn-on. The capacitor must be located as close as possible to the VIN and VCC pins to minimize inductance in the PC board traces.

Referring to the Figure 7, the voltage across the VCC regulator (VIN – VCC) is equal to VIN until VIN reaches approximately 8.5V. At higher values of VIN, the voltage at the VCC pin is regulated at approximately 7.7V below VIN. The VCC regulator has a maximum current capability of at least 20 mA. The regulator is disabled when the LM25085A is shutdown using the RT pin, or when the thermal shutdown is activated.

PGATE DRIVER OUTPUT

The PGATE pin output swings between V_{IN} (Q1 off) and the VCC pin voltage (Q1 on). The rise and fall times depend on the PFET gate capacitance and the source and sink currents provided by the internal gate driver. See Electrical Characteristics for the current capability of the driver.

Copyright © 2009–2013, Texas Instruments Incorporated

P-CHANNEL MOSFET SELECTION

The PFET must be rated for the maximum input voltage, with some margin above that to allow for transients and ringing which can occur on the supply line and the switching node. The gate-to-source voltage (V_{GS}) normally provided to the PFET is 7.7 volts for VIN greater than 8.5V. However, if the circuit is to be operated at lower values of VIN, the selected PFET must be able to fully turn-on with a V_{GS} voltage equal to VIN. The minimum input operating voltage for the LM25085A is 4.5V.

Similar to NFETs, the case or exposed thermal pad for a PFET is electrically connected to the drain terminal. When designing a PFET buck regulator the drain terminal is connected to the switching node. This situation requires a trade-off between thermal and EMI performance since increasing the PC board area of the switching node to aid the PFET power dissipation also increases radiated noise, possibly disrupting the circuit operation. Typically the switching node area is kept to a reasonable minimum and the PFET peak current is derated to stay within the recommended temperature rating of the PFET. The $R_{DS(ON)}$ of the PFET determines a portion of the power dissipation in the PFET. However, PFETs with very low $R_{DS(ON)}$ usually have large values of gate charge. A PFET with a higher gate charge has a corresponding slower switching speed, leading to higher switching losses and affecting the PFET power dissipation.

If the PFET $R_{DS(ON)}$ is used for current limit detection, note that it typically has a positive temperature coefficient. At 100°C the $R_{DS(ON)}$ may be as much as 50% higher than the value at 25°C which could result in incorrect current limiting if not accounted for when determining the value of the R_{ADJ} resistor. The PFET Total Gate Charge determines most of the power dissipation in the LM25085A due to the repetitive charge and discharge of the PFET's gate capacitance by the gate driver (powered from the VCC regulator). The LM25085A's internal power dissipation can be calculated from the following:

$$P_{DISS} = V_{IN} \times ((Q_G \times F_S) + I_{IN}) \quad (12)$$

where Q_G is the PFET's Total Gate Charge obtained from its datasheet, F_S is the switching frequency, and I_{IN} is the LM25085A's operating current obtained from Figure 5. Using the Thermal Resistance specifications in the Electrical Characteristics, the approximate junction temperature can be determined. If the calculated junction temperature is near the maximum operating temperature of 125°C, either the switching frequency must be reduced, or a PFET with a smaller Total Gate Charge must be used.

SOFT-START

The internal soft-start feature of the LM25085A allows the regulator to gradually reach a steady state operating point at power up, thereby reducing startup stresses and current surges. Upon turn-on, when Vcc reaches its under-voltage lockout threshold, the internal soft-start circuit ramps the feedback reference voltage from 0V to 0.9V, causing V_{OUT} to ramp up in a proportional manner. The soft-start ramp time is typically 1.8 ms.

In addition to controlling the initial power up cycle, the soft-start circuit also activates when the LM25085A is enabled by releasing the RT pin, and when the circuit is shutdown and restarted by the internal Thermal Shutdown circuit.

If the voltage at FB is below the regulation threshold value due to an over-current condition or a short circuit at Vout, the internal reference voltage provided by the soft-start circuit to the regulation comparator is reduced along with FB. When the over-current or short circuit condition is removed, V_{OUT} returns to the regulated value at a rate determined by the soft-start ramp. This feature helps prevent the output voltage from over-shooting following an overload event.

THERMAL SHUTDOWN

The LM25085A should be operated such that the junction temperature does not exceed 125°C. If the junction temperature increases above that, an internal Thermal Shutdown circuit activates at 170°C (typical) to disable the VCC regulator and the gate driver, and discharge the soft-start capacitor. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature falls below 150°C (typical hysteresis = 20°C), the gate driver is enabled, the soft-start circuit is released, and normal operation resumes.

 Copyright © 2009–2013, Texas Instruments Incorporated

Applications Information

EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with the following design example. Referring to Block Diagram, the circuit is to be configured for the following specifications:

- V_{OUT} = 1.0V
- V_{IN} = 4.5V to 24V, 12V Nominal
- Maximum load current ($I_{OUT(max)}$) = 5A
- Minimum load current ($I_{OUT(min)}$) = 500 mA (for continuous conduction mode)
- Switching Frequency (F_{SW}) = 200 kHz
- Maximum allowable output ripple (V_{OS}) = 10 mVp-p
- Selected PFET: Vishay Si7465
- **R_{FB1} and R_{FB2}:** These resistors set the output voltage. The ratio of these resistors is calculated from:

  $R_{FB2}/R_{FB1} = (V_{OUT}/0.9V) - 1$

  For this example, R_{FB2} / R_{FB1} = 0.111. Typically, R_{FB1} and R_{FB2} should be chosen from standard value resistors in the range of 1 kΩ to 20 kΩ which satisfy the above ratio. For this example, R_{FB2} = 1.1 kΩ, and R_{FB1} = 10 kΩ.

  R_T, PFET: Before selecting the R_T resistor, the PFET must be selected as its turn-on and turn-off delays affect the calculated value of R_T. For the Vishay Si7465 PFET, the difference of its typical turn-off and turn-on delays is 57 ns. Using Equation 5 at nominal input voltage, R_T calculates to be:

  $$R_T = \frac{1 \times (12 - 1.56V)}{1.45 \times 10^{-7} \times 12 \times 200\ kHz} - \frac{(50\ ns + 57\ ns) \times (12 - 1.56V)}{1.45 \times 10^{-7}} - 1.4 = 20.9$$

  A standard value 21 kΩ resistor is selected. Using Equation 3 the minimum on-time at the PGATE pin, which occurs at maximum input voltage (24V), is calculated to be 195 ns. This minimum one-shot period is sufficiently longer than the minimum recommended value of 150 ns. The minimum on-time at the SW node is longer due to the delay added by the PFET (57 ns). Therefore the minimum SW node on-time is 252 ns at 24V. At the SW node the maximum on-time is calculated to be 1.21 µs at 4.5V.
- **L1:** The main parameter controlled by the inductor value is the current ripple amplitude (I_{OR}). See Figure 27. The minimum load current for continuous conduction mode is used to determine the maximum allowable ripple such that the inductor current's lower peak does not fall below 0 mA. Continuous conduction mode operation at minimum load current is not a requirement of the LM25085A, but serves as a guideline for selecting L1. For this example, the maximum ripple current is:

  $$I_{OR(max)} = 2 \times I_{OUT(min)} = 1.0\ Amp \quad (13)$$

  If an application's minimum load current is zero, a good initial estimate for the maximum ripple current ($I_{OR(max)}$) is 20% of the maximum load current. The ripple calculated in Equation 13 is then used in the following equation to calculate L1:

  $$L1 = \frac{t_{ON(min)} \times (V_{IN(max)} - V_{OUT})}{I_{OR(max)}} = 5.79\ \mu H \quad (14)$$

  A standard value 6.8 µH inductor is selected. Using this inductance value, the maximum ripple current amplitude, which occurs at maximum input voltage, calculates to 0.85 Ap-p. The peak current (I_{PK}) at maximum load current is 5.43A. However, the current rating of the selected inductor must be based on the maximum current limit value calculated below.

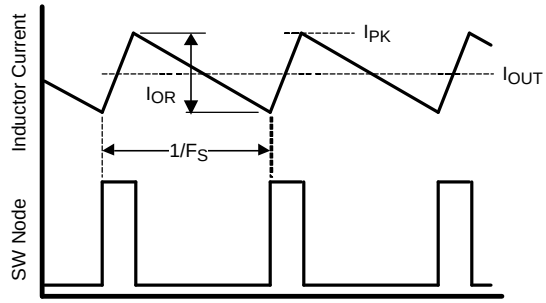


Figure 27. Inductor Current Waveform

- **R_{SEN}, R_{ADJ}:** To achieve good current limit accuracy and avoid over designing the power stage components, the sense resistor method is used for current limiting in this example. A standard value 10 mΩ resistor is selected for R_{SEN}, resulting in a 50 mV drop at maximum load current, and a maximum 0.25W power dissipation in the resistor. Since the LM25085A uses peak current detection, the minimum value for the current limit threshold must be equal to the maximum load current (5A) plus half the maximum ripple amplitude calculated above:

  $I_{CL(min)}$ = 5A + 0.85A/2 = 5.43A

  At this current level the voltage across R_{SEN} is 54.3 mV. Adding the current limit comparator offset of 9 mV (max) increases the required current limit threshold to 6.33A. Using Equation 7 with the minimum value for the ADJ pin current (32 µA), the required R_{ADJ} resistor calculates to:

  $$R_{ADJ} = \frac{6.33A \times 0.01\Omega}{32\ \mu A} = 1.98\ k\Omega$$

  A standard value 2.05 kΩ resistor is selected. The nominal current limit threshold calculates to:

  $$I_{CL(nom)} = \frac{(2.05\ k\Omega \times 40\ \mu A)}{0.01\Omega} = 8.2A$$

  Using the tolerances for the ADJ pin current and the current limit comparator offset, the maximum current limit threshold calculates to:

  $$I_{CL(max)} = \frac{(2.05\ k\Omega \times 48\ \mu A) + 9\ mV}{0.01\Omega} = 10.7A$$

  The minimum current limit thresholds calculate to:

  $$I_{CL(min)} = \frac{(2.05\ k\Omega \times 32\ \mu A) - 9\ mV}{0.01\Omega} = 5.66A$$

  The load current in each case is equal to the current limit threshold minus half the current ripple amplitude. The recommended value of 1000 pF for C_{ADJ} is used in this example.

- **C_{OUT}:** Since the maximum allowed output ripple voltage is very low in this example (10 mVp-p), the minimum ripple configuration (R3, C1, and C2 in the Block Diagram) must be used. The resulting ripple at V_{OUT} is then due to the inductor's ripple current passing through C_{OUT}. This capacitor's value can be selected based on the maximum allowable ripple voltage at V_{OUT}, or based on transient response requirements. The following calculation, based on ripple voltage, provides a first order result for the value of C_{OUT}:

  $$C_{OUT} = \frac{I_{OR(max)}}{8 \times F_S \times V_{RIPPLE}}$$

  where $I_{OR(max)}$ is the maximum ripple current calculated above, and V_{RIPPLE} is the allowable ripple at V_{OUT}.

  $$C_{OUT} = \frac{0.85A}{8 \times 200\ kHz \times 0.01V} = 53.1\ \mu F$$

  A 68 µF capacitor is selected. Typically the ripple amplitude will be higher than the calculations indicate due to the capacitor's ESR.

- **R3, C1, C2:** The minimum ripple configuration uses these three components to generate the ripple voltage required at the FB pin since there is insufficient ripple at V_{OUT}. A minimum of 25 mVp-p must be applied to the FB pin to obtain stable constant frequency operation. R3 and C1 are selected to generate a sawtooth waveform at their junction, and that waveform is AC coupled to the FB pin via C2. The values of the three

Copyright © 2009–2013, Texas Instruments Incorporated

components are determined using the following procedure:

Calculate $V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN(min)})))$

where V_{SW} is the absolute value of the voltage at the SW node during the off-time, typically 0.5V to 1V depending on the diode D1. Using a typical value of 0.65V, V_A calculates to 0.49V. V_A is the nominal DC voltage at the R3/C1 junction, and is used in the next equation:

$$R3 \times C1 = \frac{(V_{IN(min)} - V_A) \times t_{ON}}{\Delta V}$$

where t_{ON} is the maximum on-time (at minimum input voltage), and ΔV is the desired ripple amplitude at the R3/C1 junction, typically 30 mVp-p. For this example

$$R3 \times C1 = \frac{(4.5V - 0.49V) \times 1.21\ \mu s}{0.03V} = 1.62 \times 10^{-4}$$

R3 and C1 are then selected from standard value components to produce the product calculated above. Typical values for C1 are 3000 pF to 10,000 pF, and R3 is typically from 10 kΩ to 300 kΩ. C2 is then chosen large compared to C1, typically 0.1 µF. For this example, 3300 pF is chosen for C1, requiring R3 to be 48.9 kΩ. A standard value 48.7 kΩ resistor is selected.

- **C_{IN}, C_{BYP}:** These capacitors limit the voltage ripple at VIN by supplying most of the switch current during the on-time. At maximum load current, when Q1 is switched on, the current through Q1 suddenly increases to the lower peak of the inductor's ripple current, then ramps up to the upper peak, and then drops to zero at turn-off. The average current during the on-time is the load current. For a worst case calculation, these capacitors must supply this average load current during the maximum on-time, while limiting the voltage drop at VIN. For this example, 0.25V is selected as the maximum allowable droop at VIN. Their minimum value is calculated from:

$$C_{IN} + C_{BYP} = \frac{I_{OUT(max)} \times t_{ON(max)}}{\Delta V} = \frac{5A \times 1.21\ \mu s}{0.25V} = 24.2\ \mu F$$

A 33 µF electrolytic capacitor is selected for C_{IN}, and a 1 µF ceramic capacitor is selected for C_{BYP}. Due to the ESR of C_{IN}, the ripple at VIN will likely be higher than the calculation indicates, and therefore it may be desirable to increase C_{IN} to 47 µF or 68 µF. C_{BYP} must be located as close as possible to the VIN and GND pins of the LM25085A. The voltage rating for both capacitors must be at least 24V. The RMS ripple current rating for the input capacitors must also be considered. A good approximation for the required ripple current rating is $I_{RMS} > I_{OUT}/2$.

- **D1:** A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may affect the regulator's operation due to the diode's reverse recovery transients. The diode must be rated for the maximum input voltage, and the worst case current limit level. The average power dissipation in the diode is calculated from:

  $P_{D1} = V_F \times I_{OUT} \times (1\text{-}D)$

  where V_F is the diode's forward voltage drop, and D is the on-time duty cycle. Using Equation 1, the minimum duty cycle occurs at maximum input voltage, and is calculated to be ≅4.2% in this example. The diode power dissipation calculates to be:

  $P_{D1} = 0.65V \times 5A \times (1\text{-}\ 0.042) = 3.11W$

- **C_{VCC}:** The capacitor at the VCC pin (from VIN to VCC) provides not only noise filtering and stability for the VCC regulator, but also provides the surge current for the PFET gate drive. The typical recommended value for C_{VCC} is 0.47 µF. A good quality, low ESR, ceramic capacitor is recommended. C_{VCC} must be located as close as possible to the VIN and VCC pins. If the selected PFET has a Total Gate Charge specification of 100 nC or larger, or if the circuit is required to operate at input voltages below 7 volts, a larger capacitor may be required. The maximum recommended value for C_{VCC} is 1 µF.

- **IC Power Dissipation:** The maximum power dissipated in the LM25085A package is calculated using Equation 12 at the maximum input voltage. The Total Gate Charge for the Si7465 PFET is specified to be 40 nC (max) in its data sheet. Therefore the total power dissipation within the LM25085A is calculated to be:

  $P_{DISS} = 24V \times ((40\ nC \times 200\ kHz) + 1.25\ mA) = 222\ mW$

  Using an HVSSOP-PowerPAD-8 package with a θ_{JA} of 46°C/W produces a temperature rise of 10°C from junction to ambient.

Final Design Example Circuit

The final circuit is shown in Figure 28, and its performance is presented in Figure 29 through Figure 32. The measured efficiencies shown in Figure 29 are typical for a buck converter producing a low output voltage (1V).

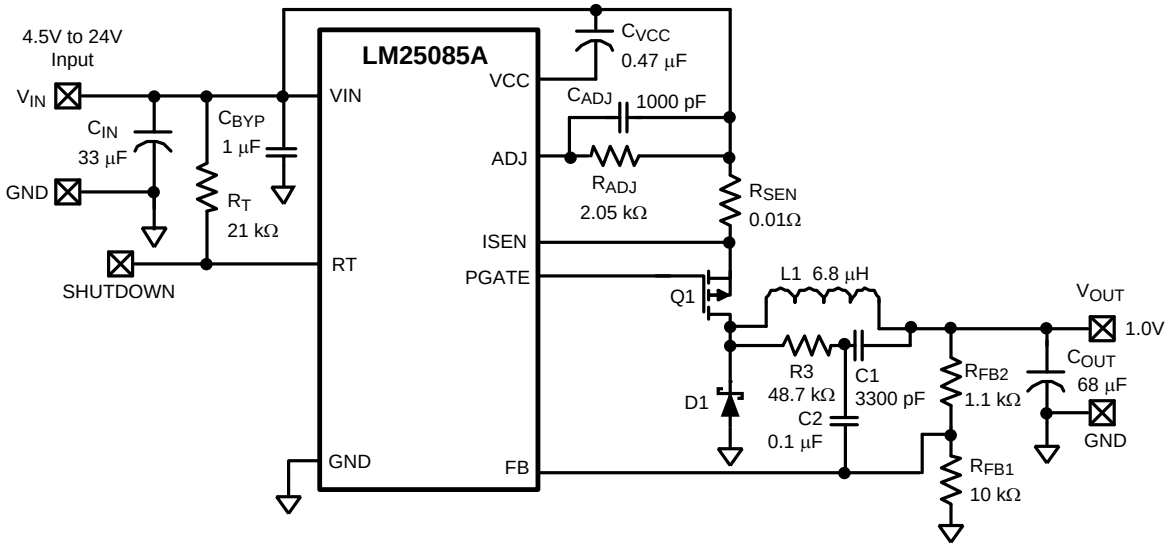


Figure 28. Example Circuit

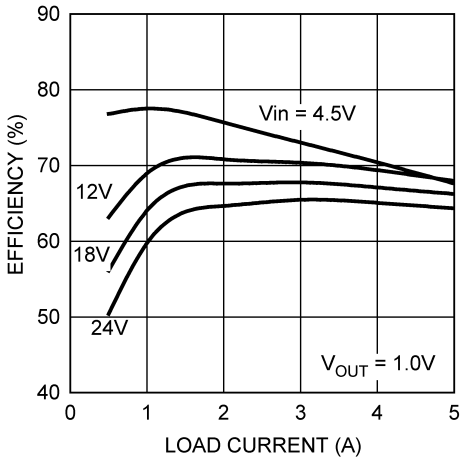


Figure 29. Efficiency vs. Load Current and V_{IN} (Circuit of Figure 28)

Copyright © 2009–2013, Texas Instruments Incorporated

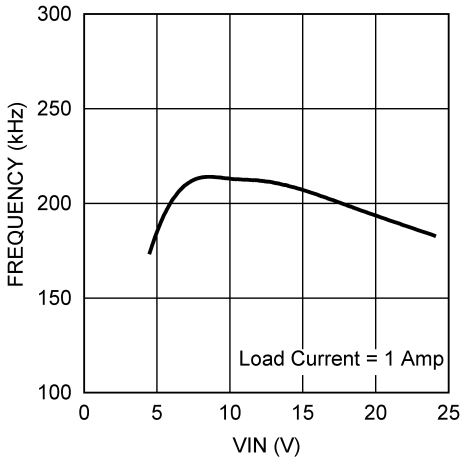


Figure 30. Frequency vs. V_{IN} (Circuit of Figure 28)

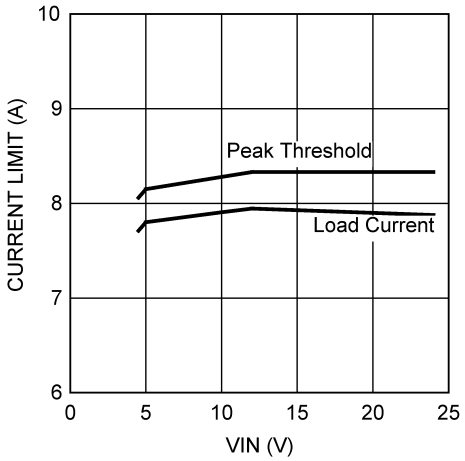


Figure 31. Current Limit vs. V_{IN} (Circuit of Figure 28)

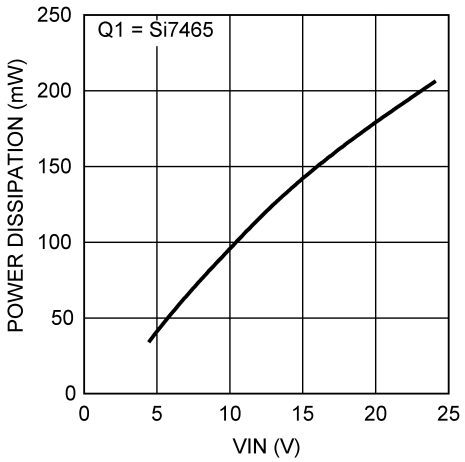


Figure 32. LM25085A Power Dissipation (Circuit of Figure 28)

Alternate Output Ripple Configurations

The minimum ripple configuration, using C1, C2 and R3, used in the example circuit Figure 28, results in a low ripple amplitude at V_{OUT} determined mainly by the characteristics of the output capacitor and the ripple current in L1. This configuration allows multiple ceramic capacitors to be used for V_{OUT} if the output voltage is provided to several places on the PC board. However, if a slightly higher level of ripple at V_{OUT} is acceptable in the application, and distributed capacitance is not used, the ripple required for the FB comparator pin can be generated with fewer external components using the circuits shown below.

Reduced ripple configuration: In Figure 33, R3, C1 and C2 are removed (compared to Figure 28). A low value resistor (R4) is added in series with C_{OUT}, and a capacitor (Cff) is added across R_{FB2}. Ripple is generated at V_{OUT} by the inductor's ripple current flowing through R4, and that ripple voltage is passed to the FB pin via Cff. The ripple at V_{OUT} can be set as low as 25 mVp-p since it is not attenuated by R_{FB2} and R_{FB1}. The minimum value for R4 is calculated from:

$$R4 = \frac{25\ mV}{I_{OR(min)}}$$

where $I_{OR(min)}$ is the minimum ripple current, which occurs at minimum input voltage. The minimum value for Cff is determined from:

$$Cff = \frac{3 \times t_{ON(max)}}{(R_{FB1}//R_{FB2})}$$

where $t_{ON(max)}$ is the maximum on-time, which occurs at minimum VIN. The next larger standard value capacitor should be used for Cff.

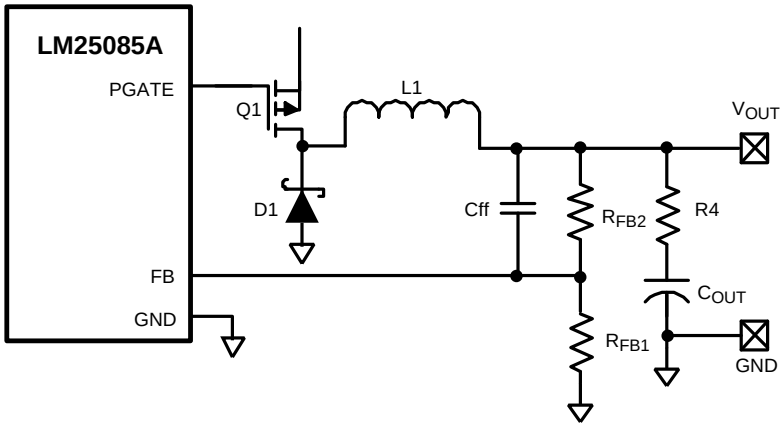


Figure 33. Reduced Ripple Configuration

b) Lowest cost configuration: This configuration, shown in Figure 34, is the same as Figure 33 except Cff is removed. Since the ripple voltage at V_{OUT} is attenuated by R_{FB2} and R_{FB1}, the minimum ripple required at V_{OUT} is equal to:

$$V_{RIP(min)} = 25\ mV \times (R_{FB2} + R_{FB1})/R_{FB1}$$

The minimum value for R4 is calculated from:

$$R4 = \frac{V_{RIP(min)}}{I_{OR(min)}}$$

where $I_{OR(min)}$ is the minimum ripple current, which occurs at minimum input voltage.

Copyright © 2009–2013, Texas Instruments Incorporated

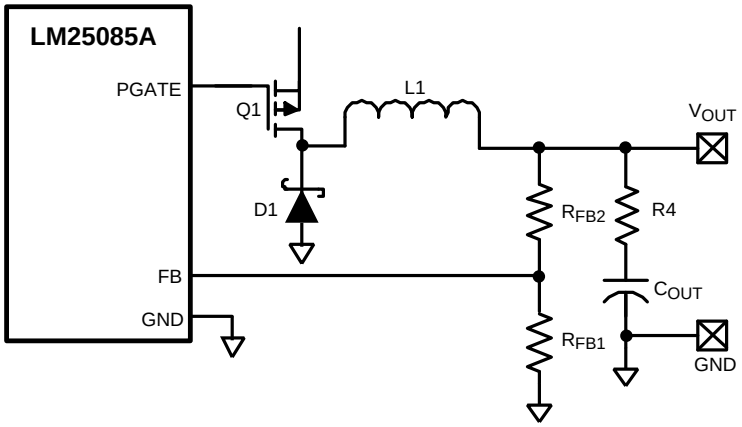


Figure 34. Lowest Cost Ripple Generating Configuration

PC Board Layout

In most applications, the heat sink pad or tab of Q1 is connected to the switch node, i.e. the junction of Q1, L1 and D1. While it is common to extend the PC board pad from under these devices to aid in heat dissipation, the pad size should be limited to minimize EMI radiation from this switching node. If the PC board layout allows, a similarly sized copper pad can be placed on the underside of the PC board, and connected with as many vias as possible to aid in heat dissipation.

The voltage regulation, over-voltage, and current limit comparators are very fast and can respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible with all the components as close as possible to their associated pins. Two major current loops conduct currents which switch very fast, requiring the loops to be as small as possible to minimize conducted and radiated EMI. The first loop is that formed by C_{IN}, Q1, L1, C_{OUT}, and back to C_{IN}. The second loop is that formed by D1, L1, C_{OUT}, and back to D1. The connection from the anode of D1 to the ground end of C_{IN} must be short and direct. C_{IN} must be as close as possible to the VIN and GND pins, and C_{VCC} must be as close as possible to the VIN and VCC pins.

If the anticipated internal power dissipation of the LM25085A will produce excessive junction temperatures during normal operation, a package option with an exposed pad must be used (HVSSOP-PowerPAD-8 or WSON-8). Effective use of the PC board ground plane can help dissipate heat. Additionally, the use of wide PC board traces, where possible, helps conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) also helps reduce the junction temperature.

Copyright © 2009–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	21

Copyright © 2009–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25085AMM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMM/NOPB.B	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMME/NOPB	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMME/NOPB.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMME/NOPB.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMMX/NOPB.B	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVZA
LM25085AMY/NOPB	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMY/NOPB.A	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMY/NOPB.B	Active	Production	HVSSOP (DGN) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMYE/NOPB	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMYE/NOPB.A	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMYE/NOPB.B	Active	Production	HVSSOP (DGN) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMYX/NOPB	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMYX/NOPB.A	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085AMYX/NOPB.B	Active	Production	HVSSOP (DGN) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SVYA
LM25085ASD/NOPB	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASD/NOPB.A	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASD/NOPB.B	Active	Production	WSON (NGQ) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASDE/NOPB	Active	Production	WSON (NGQ) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASDE/NOPB.A	Active	Production	WSON (NGQ) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASDE/NOPB.B	Active	Production	WSON (NGQ) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASDX/NOPB	Active	Production	WSON (NGQ) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASDX/NOPB.A	Active	Production	WSON (NGQ) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A
LM25085ASDX/NOPB.B	Active	Production	WSON (NGQ) | 8	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L246A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

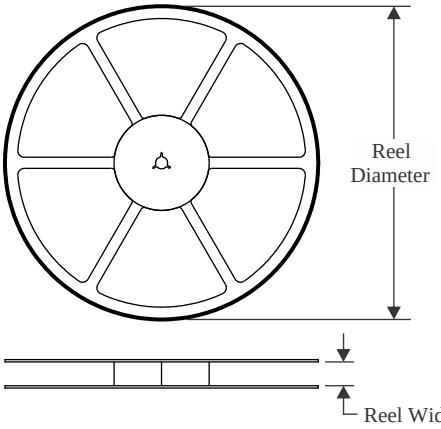
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

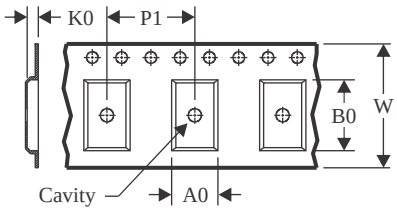
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

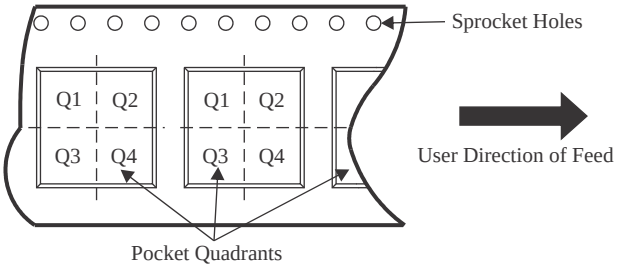


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

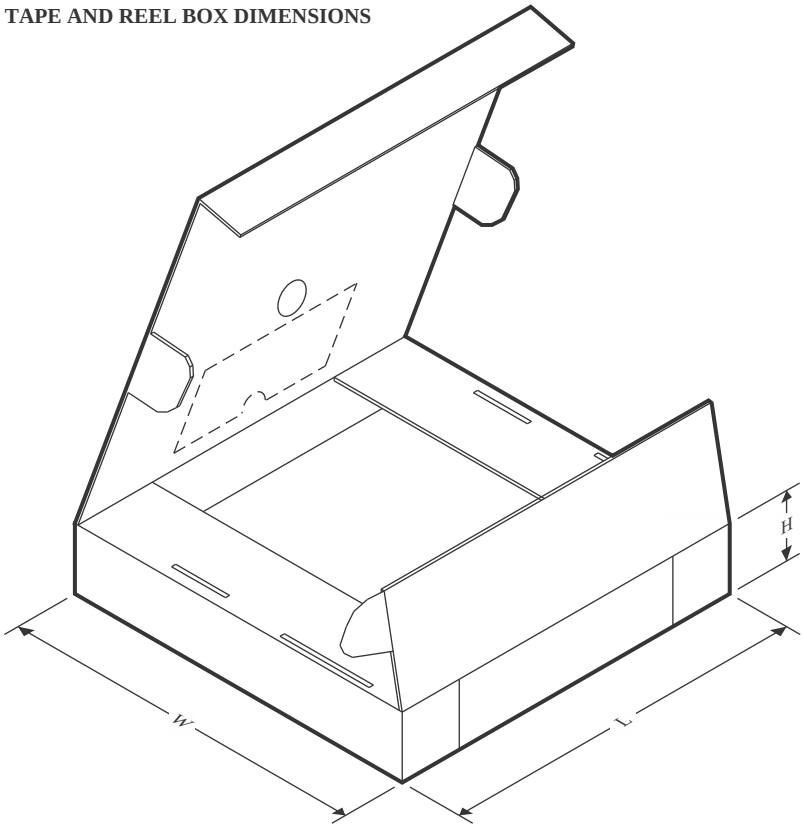
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25085AMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25085AMME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25085AMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25085AMY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25085AMYE/NOPB	HVSSOP	DGN	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25085AMYX/NOPB	HVSSOP	DGN	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM25085ASD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM25085ASDE/NOPB	WSON	NGQ	8	250	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM25085ASDX/NOPB	WSON	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

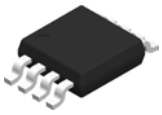


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25085AMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM25085AMME/NOPB	VSSOP	DGK	8	250	210.0	185.0	35.0
LM25085AMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM25085AMY/NOPB	HVSSOP	DGN	8	1000	210.0	185.0	35.0
LM25085AMYE/NOPB	HVSSOP	DGN	8	250	210.0	185.0	35.0
LM25085AMYX/NOPB	HVSSOP	DGN	8	3500	367.0	367.0	35.0
LM25085ASD/NOPB	WSON	NGQ	8	1000	210.0	185.0	35.0
LM25085ASDE/NOPB	WSON	NGQ	8	250	210.0	185.0	35.0
LM25085ASDX/NOPB	WSON	NGQ	8	4500	367.0	367.0	35.0

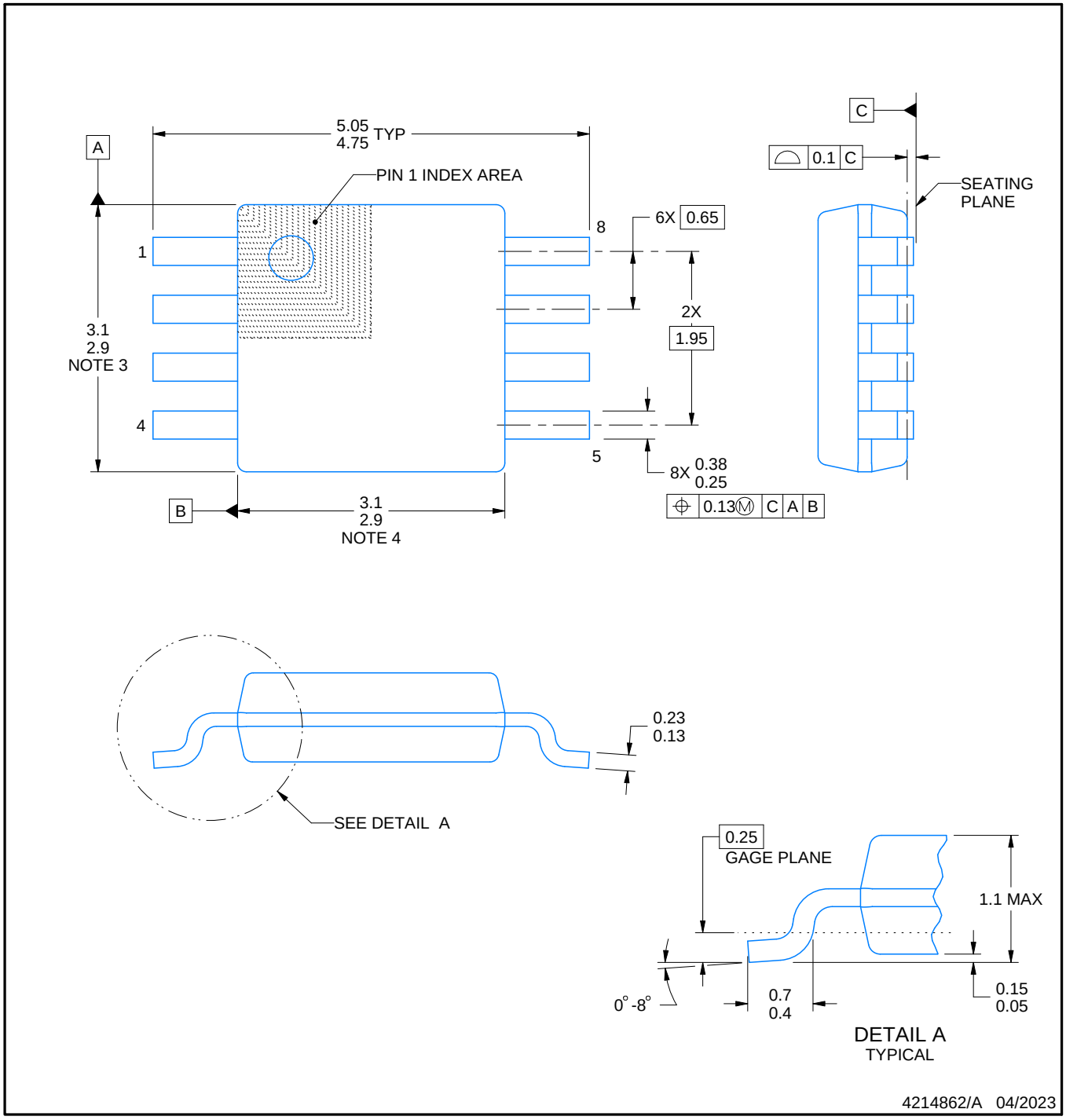
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

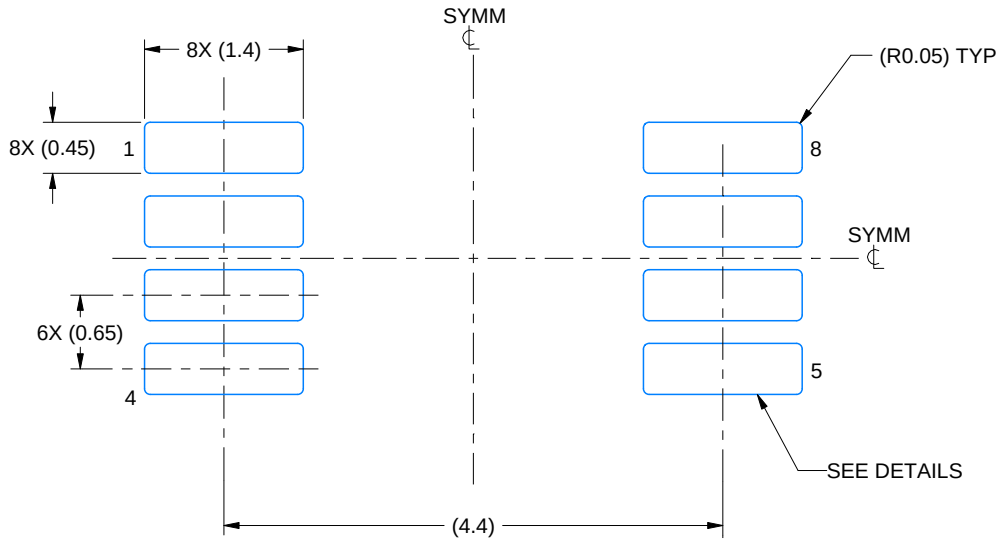
SMALL OUTLINE PACKAGE



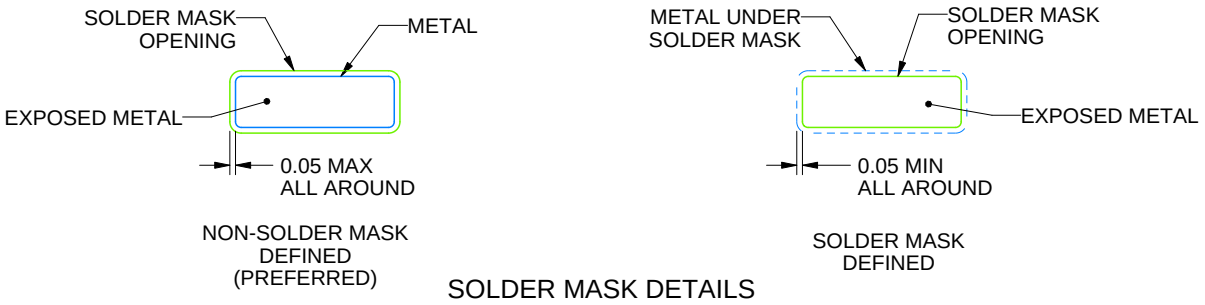
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

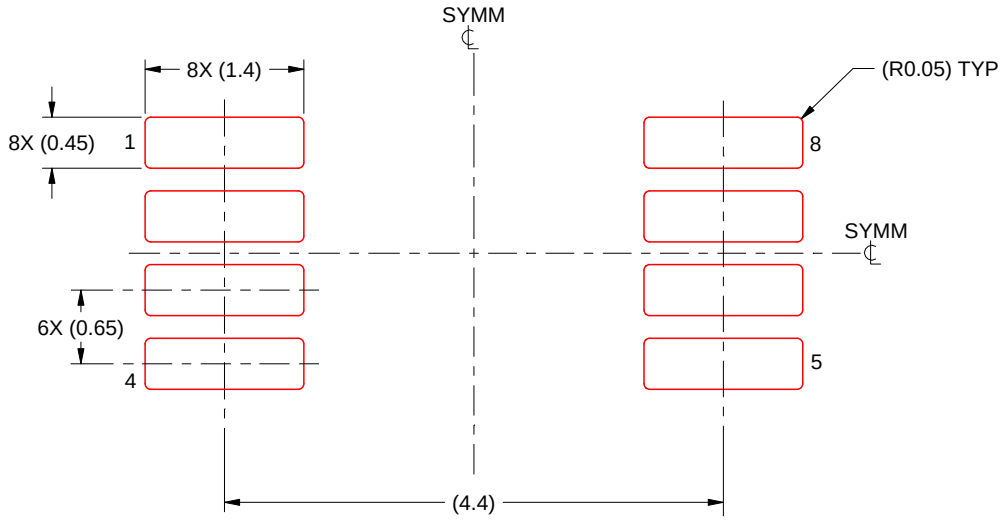


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

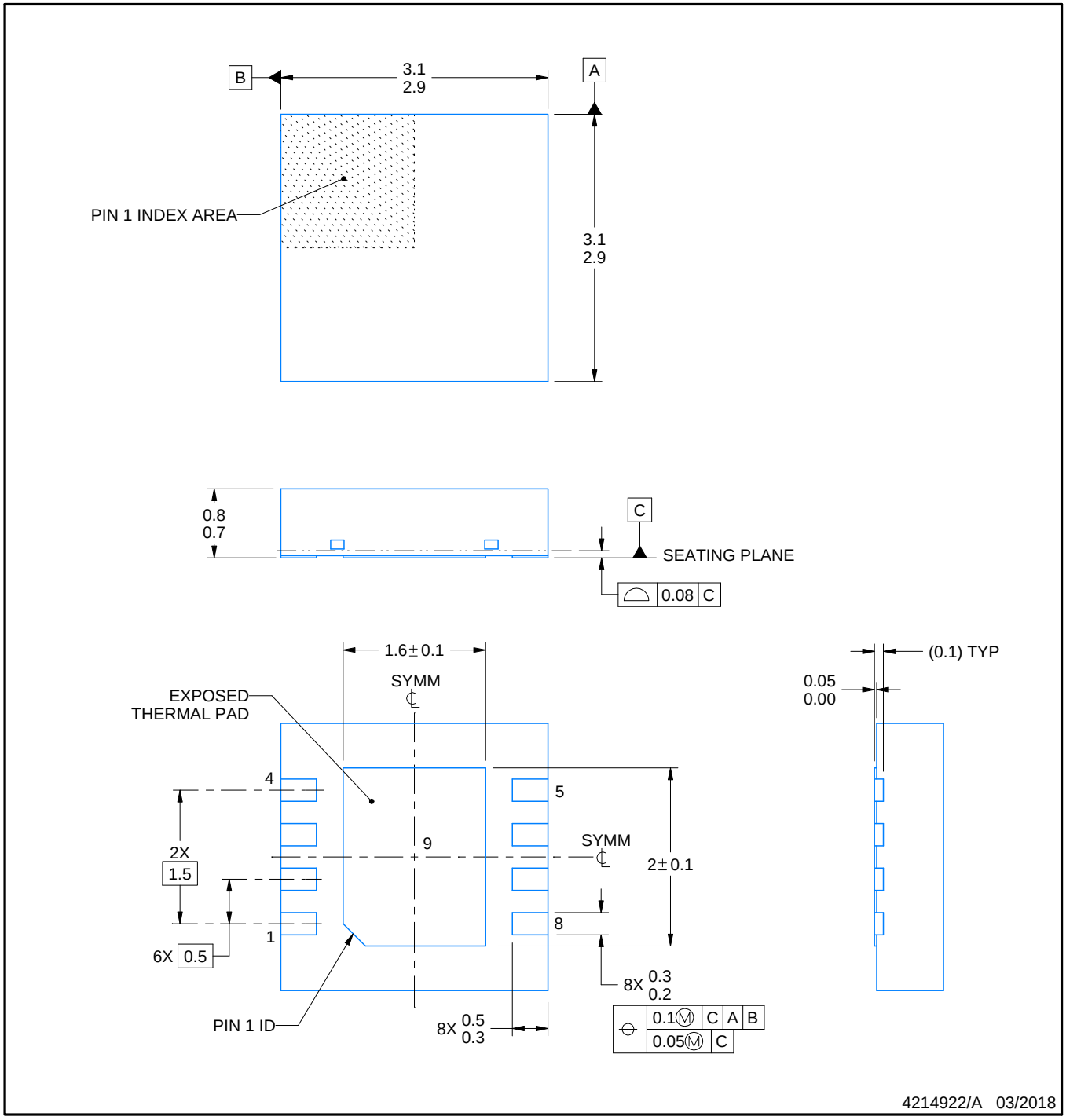


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

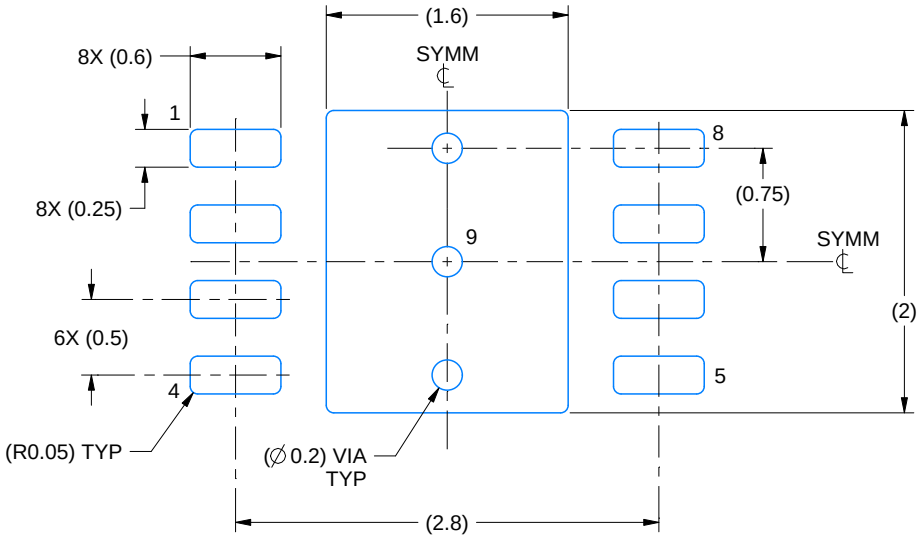
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

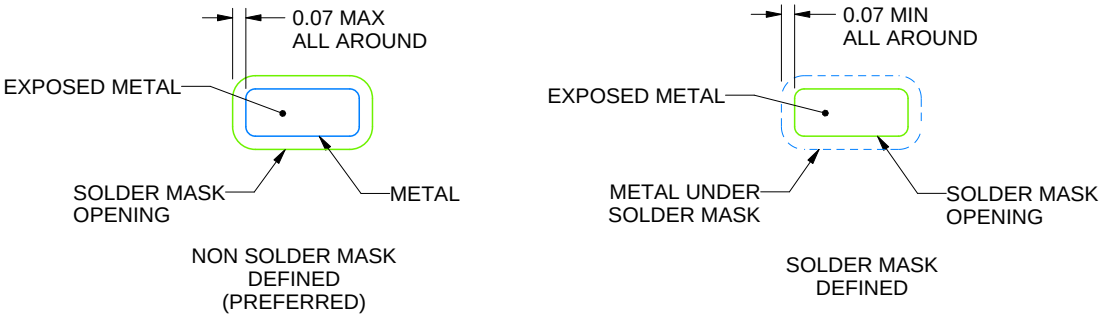


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

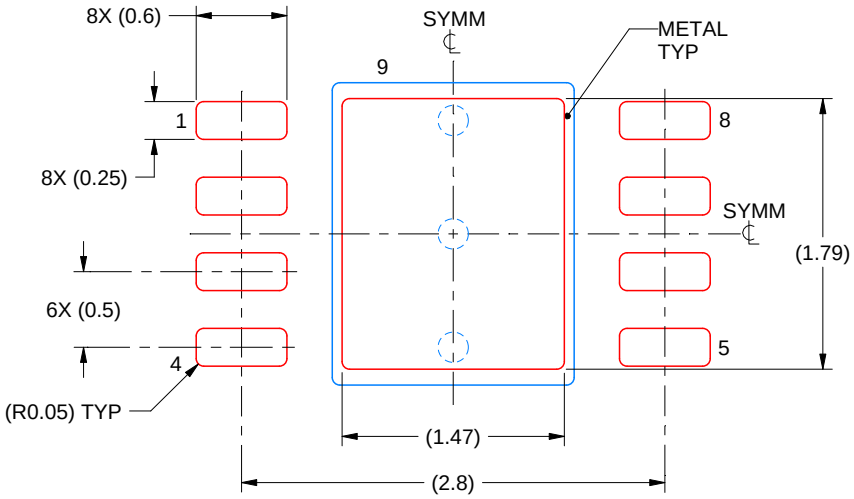


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

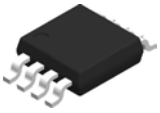
4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

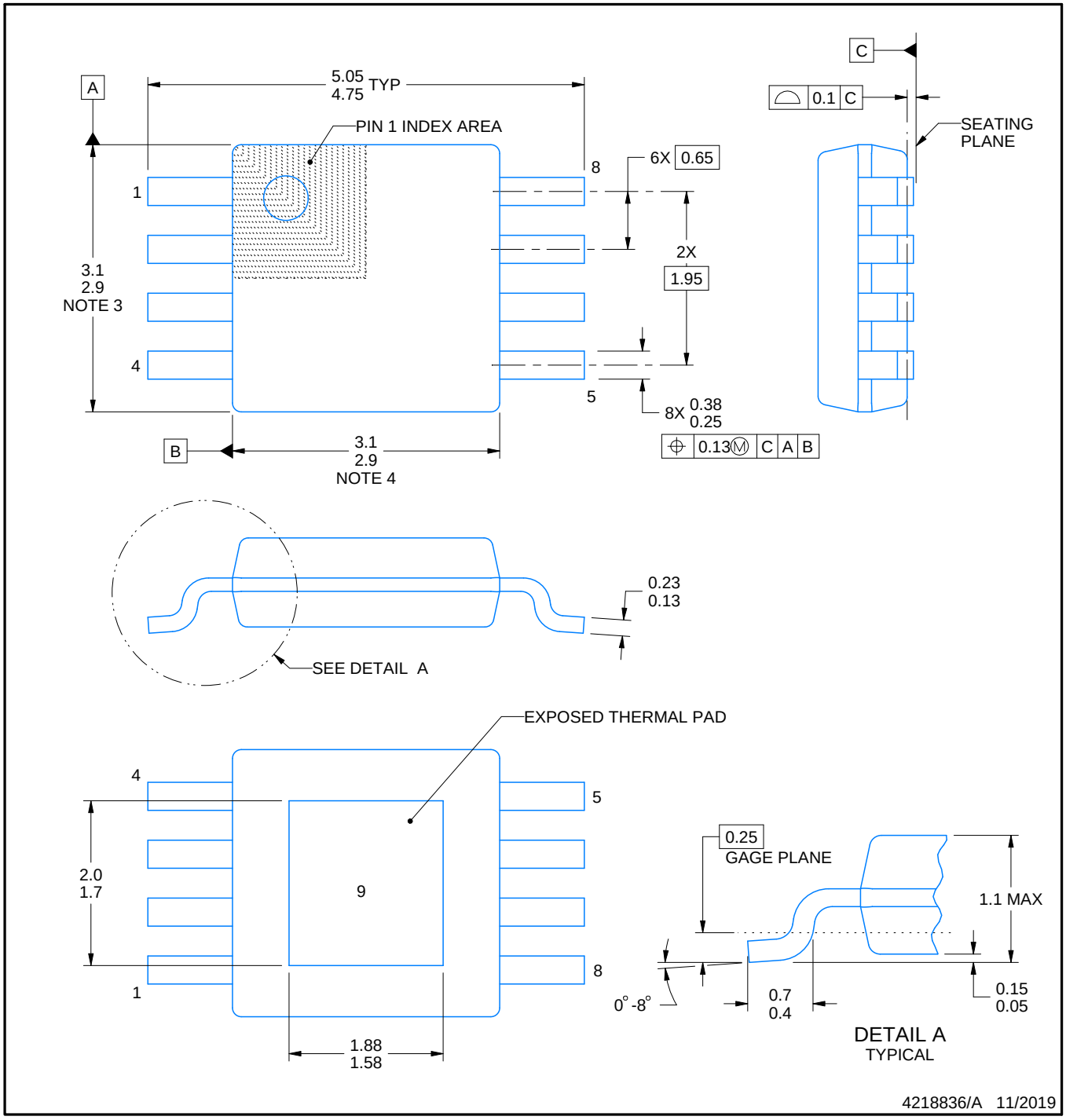
PACKAGE OUTLINE

DGN0008A



PowerPAD™ VSSOP - 1.1 mm max height

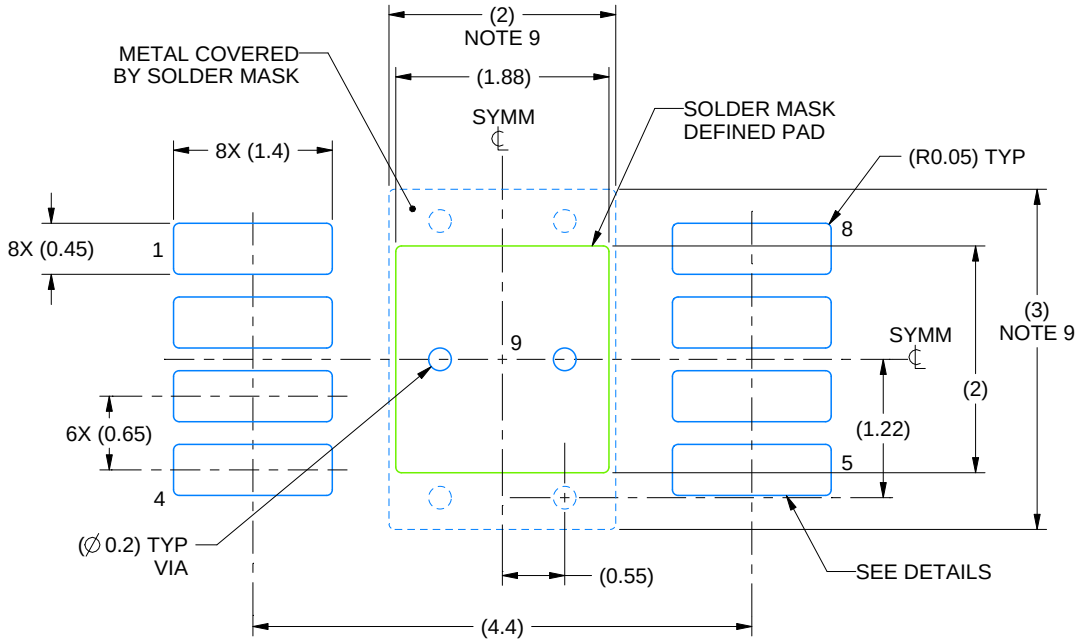
SMALL OUTLINE PACKAGE



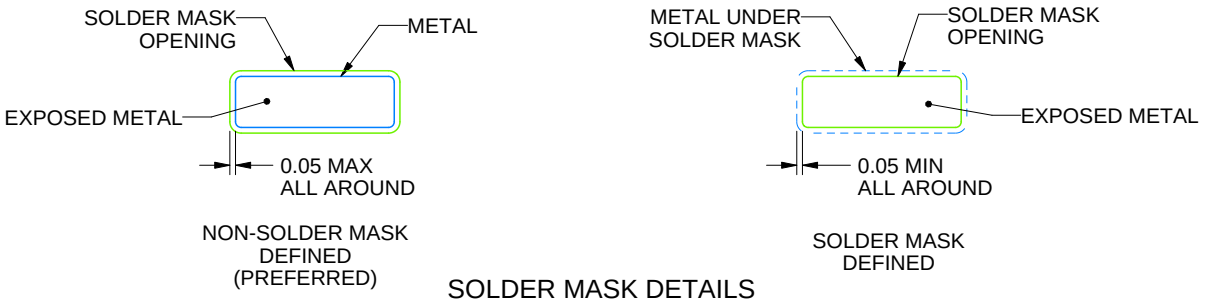
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

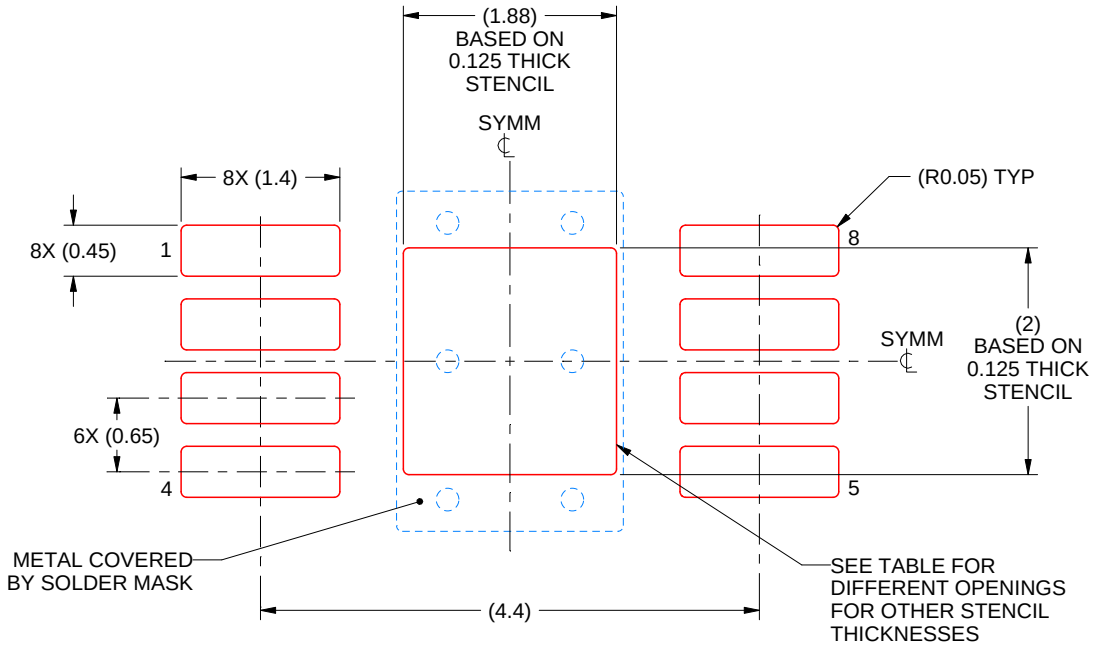


SOLDER MASK DETAILS

4218836/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

4218836/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated