12-Bit, 500-/550-MSPS Analog-to-Digital Converters

FEATURES

- **12-Bit Resolution**
- **On-Chip Analog Buffer**
- **ADS5463: 500 MSPS**
- **ADS5463 SFDR: 77dBc at 300 MHz f_{IN}**
- **ADS54RF63: 550 MSPS**
- **ADS54RF63 SFDR: 70dBc at 900 MHz f_{IN}**
- **2.3-GHz Input Bandwidth**
- **LVDS-Compatible Outputs**
- **Very Low Latency: 3.5 Clock Cycles**
- **High Analog Input Swing without Damage, > 10 V_{pp} Differential-AC Signal**
- **Total Power Dissipation: 2.2 W**
- **80-Pin TQFP PowerPAD™ Package (14-mm × 14-mm footprint)**
- **Industrial Temperature Range: –40°C to 85°C**
- **Pin-Similar/Compatible to 12-, 13-, and 14-Bit Family: ADS5440/ADS5444/ADS5474**

APPLICATIONS

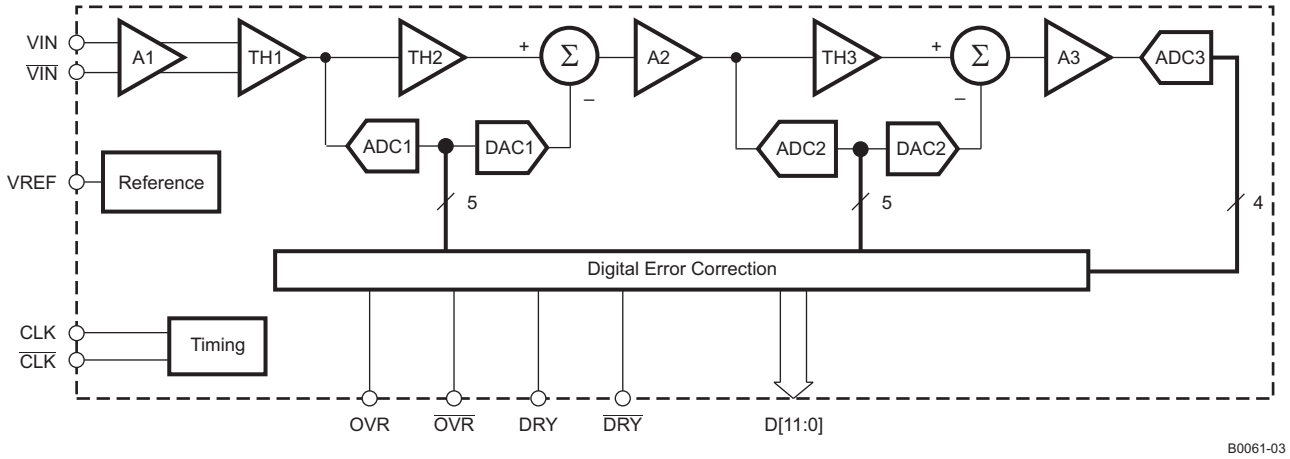
- **Test and Measurement Instrumentation**
- **Software-Defined Radio**
- **Data Acquisition**
- **Power Amplifier Linearization**
- **Communication Instrumentation**
- **Radar**

DESCRIPTION

The ADS5463/ADS54RF63 is a 12-bit, 500-/550-MSPS analog-to-digital converter (ADC) that operates from both a 5-V supply and 3.3-V supply, while providing LVDS-compatible digital outputs. This ADC is one of a family of 12-, 13-, and 14-bit ADCs that operate from 210 MSPS to 550 MSPS. The ADS5463/ADS54RF63 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source while providing a high-impedance input.

The ADS54RF63 provides superior SFDR compared to the ADS5463 when the analog input frequency exceeds ~350 MHz or if operation up to 550 MSPS is required.

The ADS5463/ADS54RF63 is available in a TQFP-80 PowerPAD™ package. The ADS5463/ADS54RF63 is built on the Texas Instrument complementary bipolar process (BiCom3) and specified over the full industrial temperature range (–40°C to 85°C).



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5463	HTQFP-80(2) PowerPAD	PFP	–40°C to 85°C	ADS5463I	ADS5463IPFP	Tray, 96
					ADS5463IPFPR	Tape and reel, 1000
ADS54RF63	HTQFP-80(2) PowerPAD	PFP	–40°C to 85°C	ADS54RF63I	ADS54RF63IPFP	Tray, 96
					ADS54RF63IPFPR	Tape and reel, 1000

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 6.15 mm × 6.15 mm (min), 7.5 mm × 7.5 mm (maximum), see Thermal Pad Addendum located at the end of the data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			ADS5463/ADS54RF63	UNIT
Supply voltage	AVDD5 to GND		6	V
	AVDD3 to GND		5	
	DVDD3 to GND		5	
AIN, $\overline{AIN}$ to GND(2)	Voltage difference between pin and ground	AC Signal	–0.3 to (AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.4 to 4.4	
		DC signal, T_J = 125°C	1.0 to 3.8	
AIN to $\overline{AIN}$(2)	Voltage difference between these pins	AC Signal	-5.2 to 5.2	V
		DC Signal, T_J = 105°C	-4.0 to 4.0	
		DC signal, T_J = 125°C	-2.8 to 2.8	
CLK, $\overline{CLK}$ to GND(2)	Voltage difference between pin and ground	AC signal	–0.3 to (AVDD5 + 0.3)	V
		DC signal, T_J = 105°C	0.1 to 4.7	
		DC signal, T_J = 125°C	1.1 to 3.7	
CLK to $\overline{CLK}$(2)	Voltage difference between these pins	AC Signal	-3.3 to 3.3	V
		DC signal, T_J = 105°C	-3.3 to 3.3	
		DC signal, T_J = 125°C	-2.6 to 2.6	
Data output to GND(2)	LVDS digital outputs		–0.3 to (DVDD3 + 0.3)	V
Operating temperature range			–40 to 85	°C
Maximum junction temperature (max T_J)			150	°C
Storage temperature range			–65 to 150	°C
ESD, human-body model (HBM)			2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. Kirkendall voidings and current density information for calculation of expected lifetime is available upon request.
(2) Valid when supplies are within recommended operating range.

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THERMAL CHARACTERISTICS[1]

PARAMETER	TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$[2]	Soldered thermal pad, no airflow	23.7	°C/W
	Soldered thermal pad, 150-LFM airflow	17.8	
	Soldered thermal pad, 250-LFM airflow	16.4	
$R_{\theta JP}$[3]	Bottom of package (thermal pad)	2.99	°C/W

(1) Using 36 thermal vias (6 × 6 array). See *PowerPAD Package* in the *Application Information* section.
(2) $R_{\theta JA}$ is the thermal resistance from the junction to ambient.
(3) $R_{\theta JP}$ is the thermal resistance from the junction to the thermal pad.

RECOMMENDED OPERATING CONDITIONS

		ADS54RF63			ADS5463			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
T_A	Open free-air temperature	–40		85	–40		85	°C
SUPPLIES								
AVDD5	Analog supply voltage	4.75	5	5.25	4.75	5	5.25	V
AVDD3	Analog supply voltage	3.0	3.3	3.6	3.0	3.3	3.6	V
DVDD3	Output driver supply voltage	3.0	3.3	3.6	3.0	3.3	3.6	V
ANALOG INPUT								
	Differential input range		2.2			2.2		V_{pp}
VCM	Input common mode		2.4			2.4		V
DIGITAL OUTPUT (DRY, DATA, OVR)								
	Maximum differential output load		10			10		pF
CLOCK INPUT (CLK)								
	CLK input sample rate (sine wave)	40		550	20		500	MSPS
	Clock amplitude, differential sine wave, see Figure 59	0.5		3.5	0.5		3.5	V_{pp}
	Clock duty cycle, see Figure 64	40%	50%	60%	40%	50%	60%	

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ELECTRICAL CHARACTERISTICS

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, ADS5463 sampling rate = 500 MSPS, ADS54RF63 sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS54RF63			ADS5463			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				12			12		Bits
ANALOG INPUTS									
	Differential input			2.2			2.2		V_{PP}
VCM	Common-mode voltage	Self-biased		2.4			2.4		V
	Input resistance	To VCM		500			500		Ω
	Input capacitance	To ground (un-soldered package)		2.3			2.3		pF
	Input bandwidth	(–3 dB)		2.3			2.3		GHz
CMRR	Common-mode rejection ratio	Common mode signal = 10 MHz		90			90		dB
CLOCK INPUTS									
	Input resistance	To internal common-mode		1000			1000		Ω
	Input capacitance	To ground (un-soldered package)		1.5			1.5		pF
	Common mode	Internally generated		2.4			2.4		V
INTERNAL REFERENCE VOLTAGE									
V_{REF}	Reference voltage			2.4			2.4		V

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ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, ADS5463 sampling rate = 500 MSPS, ADS54RF63 sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS54RF63			ADS5463			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC ACCURACY									
	No missing codes			Specified			Specified		
DNL	Differential linearity error	f_{IN} = 10 MHz	–0.95	±0.5	0.95	–0.95	±0.25	0.95	LSB
INL	Integral linearity error	500MSPS, f_{IN} = 10 MHz	–2.5	±0.7	2.5	–2.5	+0.8/–0.3	2.5	LSB
		550MSPS, f_{IN} = 10 MHz	–4.5	±1.5	4.5		NA		LSB
	Offset error		–11		11	–11		11	mV
	Offset temperature coefficient			0.0005			0.0005		mV/°C
	Gain error		–5		5	–5		5	%FS
	Gain temperature coefficient			–0.02			–0.02		%FS/°C
POWER SUPPLY									
I_{AVDD5}	5-V analog supply current	V_{IN} = full scale, f_{IN} = 10 MHz		310	340		300	330	mA
I_{AVDD3}	3.3-V analog supply current			140	155		125	138	mA
I_{DVDD3}	3.3-V digital supply current (includes LVDS)			82	88		82	88	mA
	Total power dissipation			2.25	2.5		2.18	2.4	W
	Power-up time			200			200		µs
PSRR	Power-supply rejection ratio	Without 0.1-µF board supply capacitors, with 100-kHz supply noise		85			85		dB

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ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, ADS5463 sampling rate = 500 MSPS, ADS54RF63 sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS54RF63			ADS5463			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC AC CHARACTERISTICS									
CLK	Maximum clock frequency		550			500			MHz
RMS idle-channel noise		Inputs tied to common-mode		0.8			0.7		LSB
SNR, Signal-to-Noise Ratio									
SNR	f_S = 500MSPS	f_{IN} = 10 MHz		64.7			65.4		dBFS
		f_{IN} = 70 MHz		64.6			65.4		
		f_{IN} = 100 MHz		64.6		63.5	65.3		
		f_{IN} = 230 MHz		64.4			65.1		
		f_{IN} = 300 MHz	62.5	64.3		63	65		
		f_{IN} = 450 MHz		64.1			64.6		
		f_{IN} = 650 MHz		63.5			63.9		
		f_{IN} = 900 MHz		62.5			62.6		
		f_{IN} = 1.3 GHz		61			59.3		
	f_S = 550MSPS	f_{IN} = 100 MHz		62.6			NA		
		f_{IN} = 450 MHz	59	61.9			NA		
		f_{IN} = 1.3 GHz		59.3			NA		
SFDR, Spurious-Free Dynamic Range									
SFDR	f_S = 500MSPS	f_{IN} = 10 MHz		85			85		dBc
		f_{IN} = 70 MHz		83			82		
		f_{IN} = 100 MHz		84		70	82		
		f_{IN} = 230 MHz		81			78		
		f_{IN} = 300 MHz	64	78		64	77		
		f_{IN} = 450 MHz		80			75		
		f_{IN} = 650 MHz		75			65		
		f_{IN} = 900 MHz		70			56		
		f_{IN} = 1.3 GHz		58			45		
	f_S = 550MSPS	f_{IN} = 100 MHz		76			NA		
		f_{IN} = 450 MHz	62	75			NA		
		f_{IN} = 1.3 GHz		57			NA		

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ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, ADS5463 sampling rate = 500 MSPS, ADS54RF63 sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS54RF63			ADS5463			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2, Second Harmonic									
HD2	f_S = 500MSPS	f_{IN} = 10 MHz		87			87		dBc
		f_{IN} = 70 MHz		87			82		
		f_{IN} = 100 MHz		85		70	80		
		f_{IN} = 230 MHz		83			81		
		f_{IN} = 300 MHz	64	79		64	77		
		f_{IN} = 450 MHz		81			80		
		f_{IN} = 650 MHz		75			77		
		f_{IN} = 900 MHz		70			66		
		f_{IN} = 1.3 GHz		58			50		
	f_S = 550MSPS	f_{IN} = 100 MHz		84			NA		
		f_{IN} = 450 MHz	62	78			NA		
		f_{IN} = 1.3 GHz		63			NA		
HD3, Third Harmonic									
HD3	f_S = 500MSPS	f_{IN} = 10 MHz		90			85		dBc
		f_{IN} = 70 MHz		92			90		
		f_{IN} = 100 MHz		89		70	87		
		f_{IN} = 230 MHz		85			90		
		f_{IN} = 300 MHz	64	83		64	80		
		f_{IN} = 450 MHz		90			75		
		f_{IN} = 650 MHz		76			65		
		f_{IN} = 900 MHz		78			56		
		f_{IN} = 1.3 GHz		58			45		
	f_S = 550MSPS	f_{IN} = 100 MHz		76			NA		
		f_{IN} = 450 MHz	62	75			NA		
		f_{IN} = 1.3 GHz		57			NA		
Worst Harmonic/Spur (other than HD2 and HD3)									
Worst non-HD2/3	f_S = 500MSPS	f_{IN} = 10 MHz		86			86		dBc
		f_{IN} = 70 MHz		86			86		
		f_{IN} = 100 MHz		86			86		
		f_{IN} = 230 MHz		83			77		
		f_{IN} = 300 MHz		82			81		
		f_{IN} = 450 MHz		86			86		
		f_{IN} = 650 MHz		85			85		
		f_{IN} = 900 MHz		82			78		
		f_{IN} = 1.3 GHz		78			67		
	f_S = 550MSPS	f_{IN} = 100 MHz		82			NA		
		f_{IN} = 450 MHz		81			NA		
		f_{IN} = 1.3 GHz		74			NA		

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ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, ADS5463 sampling rate = 500 MSPS, ADS54RF63 sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS54RF63			ADS5463			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THD, Total Harmonic Distortion									
THD	f_S = 500MSPS	f_{IN} = 10 MHz		82			80		dBc
		f_{IN} = 70 MHz		82			79		
		f_{IN} = 100 MHz		80			77		
		f_{IN} = 230 MHz		78			75		
		f_{IN} = 300 MHz		76			73		
		f_{IN} = 450 MHz		77			73		
		f_{IN} = 650 MHz		69			64		
		f_{IN} = 900 MHz		64			55		
		f_{IN} = 1.3 GHz		56			44		
	f_S = 550MSPS	f_{IN} = 100 MHz		74			NA		
		f_{IN} = 450 MHz		72			NA		
		f_{IN} = 1.3 GHz		56			NA		
SINAD, Signal-to-Noise and Distortion									
SINAD	f_S = 500MSPS	f_{IN} = 10 MHz		63.6			64.2		dBc
		f_{IN} = 70 MHz		63.5			64.2		
		f_{IN} = 100 MHz		63.5		62	64.1		
		f_{IN} = 230 MHz		63.2			63.7		
		f_{IN} = 300 MHz	60	63.1			63.5		
		f_{IN} = 450 MHz		62.9			63.1		
		f_{IN} = 650 MHz		61.5			60.5		
		f_{IN} = 900 MHz		59.6			54.4		
		f_{IN} = 1.3 GHz		54.4			44.1		
	f_S = 550MSPS	f_{IN} = 100 MHz		61.3			NA		
		f_{IN} = 450 MHz	57	60.1			NA		
		f_{IN} = 1.3 GHz		54			NA		
ENOB, Effective Number of Bits (from SINAD in dBc)(1)									
ENOB	f_S = 500MSPS	f_{IN} = 100 MHz		10.3		10	10.4		Bits
		f_{IN} = 300 MHz	9.67	10.2			10.4		
		f_{IN} = 900 MHz		9.6			8.7		
		f_{IN} = 1.3 GHz		8.7			7		
	f_S = 550MSPS	f_{IN} = 450 MHz	9.18	9.7			NA		
		f_{IN} = 1.3 GHz		8.7			NA		

(1) ENOB = [SINAD(dBc) - 1.76] / 6.02

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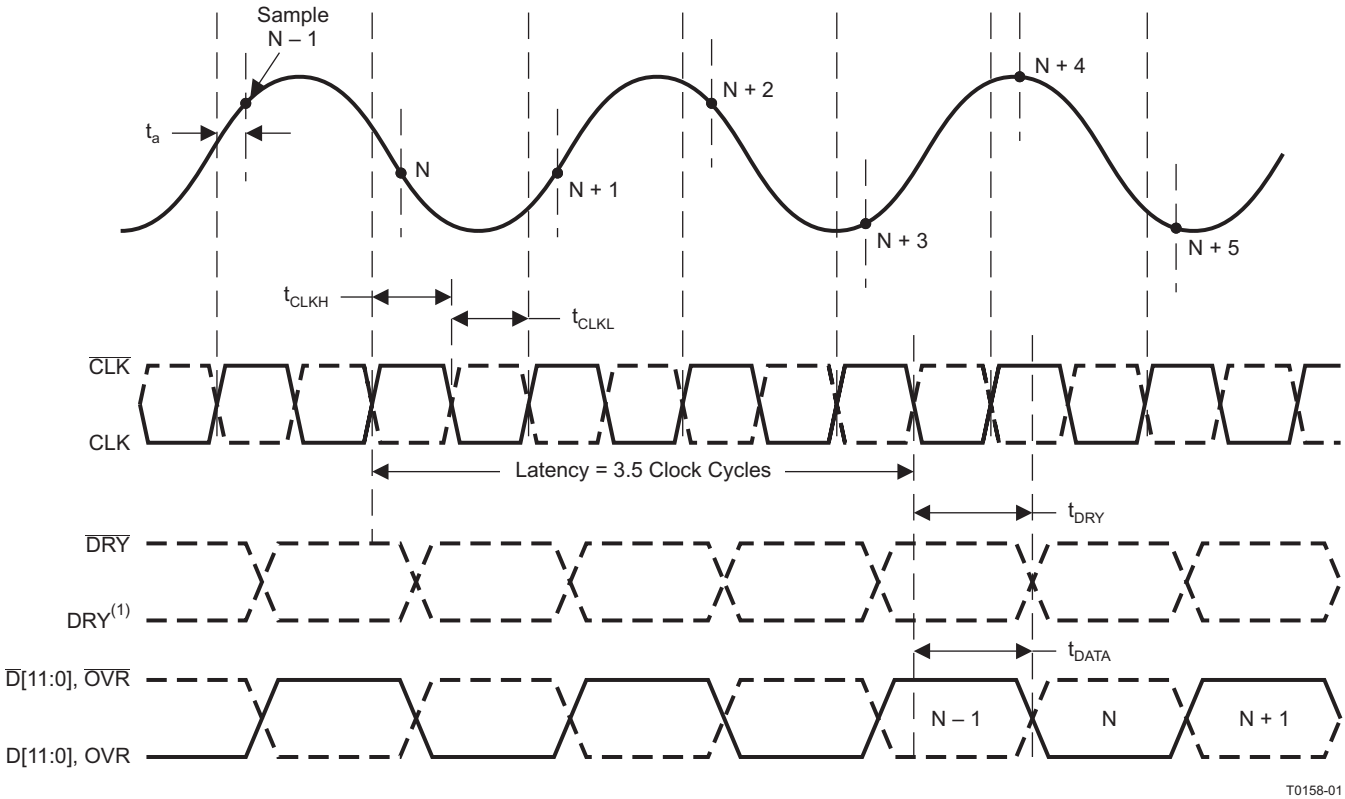
ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, ADS5463 sampling rate = 500 MSPS, ADS54RF63 sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, –1-dBFS differential input, and 3-V_{PP} differential clock, unless otherwise noted

PARAMETER		TEST CONDITIONS	ADS54RF63			ADS5463			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Two-Tone SFDR									
2-tone SFDR	f_S = 500MSPS	f_{IN1} = 65 MHz, f_{IN2} = 70 MHz, each tone at –7 dBFS		90			90		dBFS
		f_{IN1} = 65 MHz, f_{IN2} = 70 MHz, each tone at –16 dBFS		90			89		
		f_{IN1} = 350 MHz, f_{IN2} = 355 MHz, each tone at –7 dBFS		90			82		
		f_{IN1} = 350 MHz, f_{IN2} = 355 MHz, each tone at –16 dBFS		90			89		
	f_S = 550MSPS	f_{IN1} = 397.5 MHz, f_{IN2} = 402.5 MHz, each tone at –7 dBFS		90			NA		
		f_{IN1} = 647.5 MHz, f_{IN2} = 652.5 MHz, each tone at –7 dBFS		84			NA		
LVDS DIGITAL OUTPUTS									
V_{OD}	Differential output voltage (±)		247	350	454	247	350	454	mV
V_{OC}	Common-mode output voltage		1.125		1.375	1.125		1.375	V



(1) Polarity of DRY is undetermined. For further information, see the Digital Outputs section.

Figure 1. Timing Diagram

TIMING CHARACTERISTICS[1]

Typical values at T_A = 25°C, minimum and maximum values over full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, sampling rate = maximum rated, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS54RF63			ADS5463			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_a	Aperture delay			200			200		ps
	Aperture jitter, rms			150			150		fs
	Latency			3.5			3.5		cycles
t_{CLK}	Clock period		1.8181		50	2		50	ns
t_{CLKH}	Clock pulse duration, high	Assumes min 40% duty cycle	0.727			0.8			ns
t_{CLKL}	Clock pulse duration, low		0.727			0.8			ns
t_{DRY}	CLK to DRY delay[2]	Zero crossing	1350		1750	950		1600	ps
t_{DATA}	CLK to DATA/OVR delay[2]	Zero crossing	1100		2000	750		2100	ps
t_{SKEW}	DATA to DRY skew	$t_{DATA} – t_{DRY}$	–250	0	250	–350	0	650	ps
t_{RISE}	DRY/DATA/OVR rise time			500			500		ps
t_{FALL}	DRY/DATA/OVR fall time			500			500		ps

(1) Timing parameters are specified by design or characterization, but not production tested. <10pF load on each output pin.
(2) DRY, DATA, and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the overall propagation delay.

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PIN CONFIGURATION

PFP PACKAGE
(TOP VIEW)

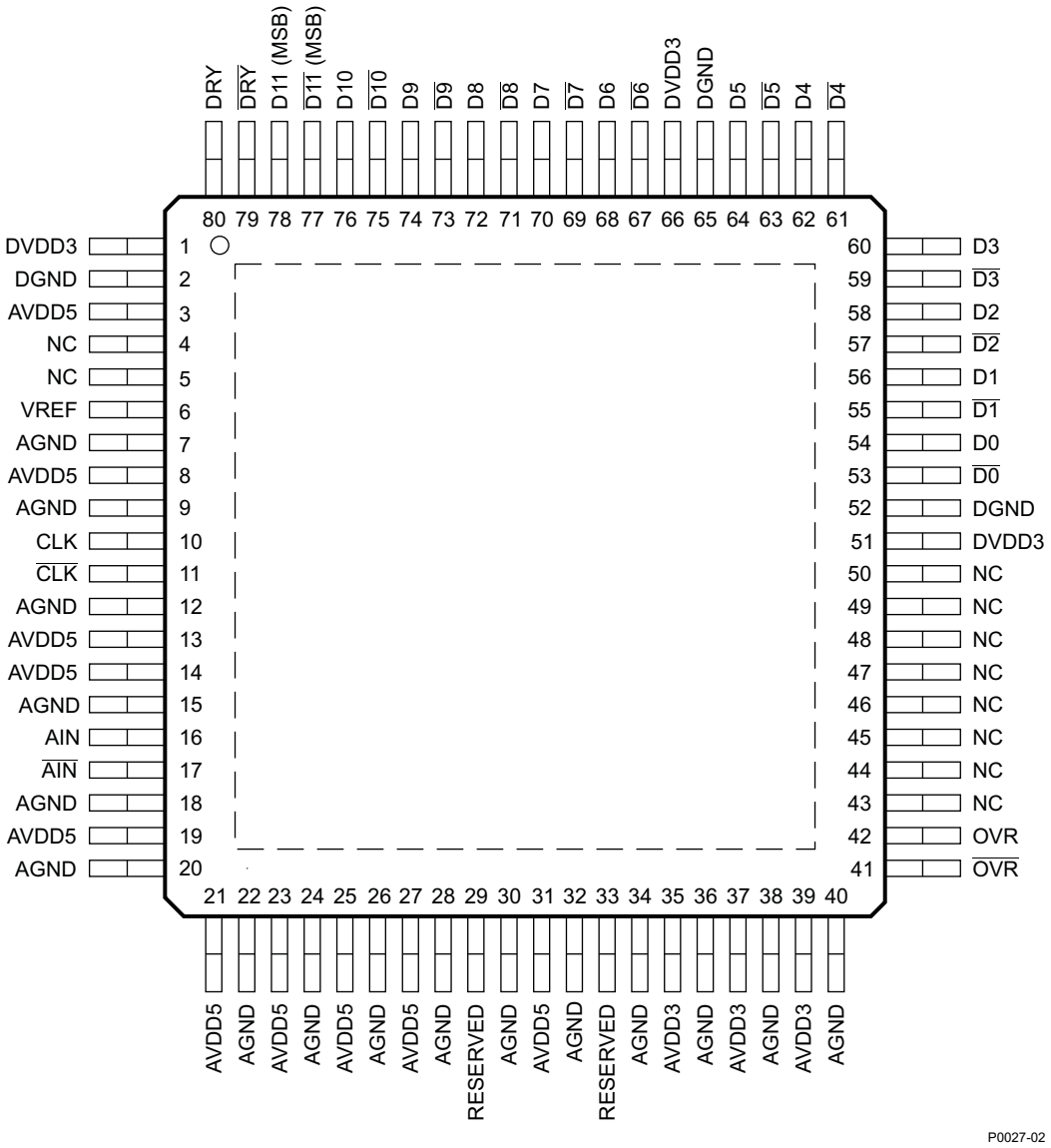

Table 1. PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
AIN	16	Differential input signal (positive)
$\overline{\text{AIN}}$	17	Differential input signal (negative)
AVDD5	3, 8, 13, 14, 19, 21, 23, 25, 27, 31	Analog power supply (5 V)
AVDD3	35, 37, 39	Analog power supply (3.3 V) (Suggestion for ≤250 MSPS: leave option to connect to 5 V for ADS5440/4 13-bit compatibility)
DVDD3	1, 51, 66	Output driver power supply (3.3 V)
AGND	7, 9, 12, 15, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40	Analog ground
(Power Pad)	(81)	Power pad for thermal relief, also analog ground
DGND	2, 52, 65	Digital ground
CLK	10	Differential input clock (positive). Conversion is initiated on rising edge.
$\overline{\text{CLK}}$	11	Differential input clock (negative)
D0–D11	54, 56, 58, 60, 62, 64, 68, 70, 72, 74, 76, 78	LVDS digital output pairs (D0/$\overline{\text{D0}}$ is LSB pair. D11/$\overline{\text{D11}}$ is MSB pair.)
$\overline{\text{D0}}$–$\overline{\text{D11}}$	53, 55, 57, 59, 61, 63, 67, 69, 71, 73, 75, 77	
DRY, $\overline{\text{DRY}}$	80, 79	Data ready LVDS output pair
NC	4, 5, 43–50	No connect (4 and 5 should be left floating, 43–50 are possible future bit additions for this pinout and therefore can be connected to a digital bus or left floating)
OVR, $\overline{\text{OVR}}$	42, 41	Overrange indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
RESERVED	29, 33	Pin 29 is reserved for possible future Vcm output for this pinout, like ADS5474; pin 33 is reserved for possible future power-down control pin for this pinout, like ADS5474.
VREF	6	Reference voltage input/output (2.4 V nominal). Connect 0.1-µF capacitor from VREF to AGND.

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ADS5463 TYPICAL CHARACTERISTICS

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

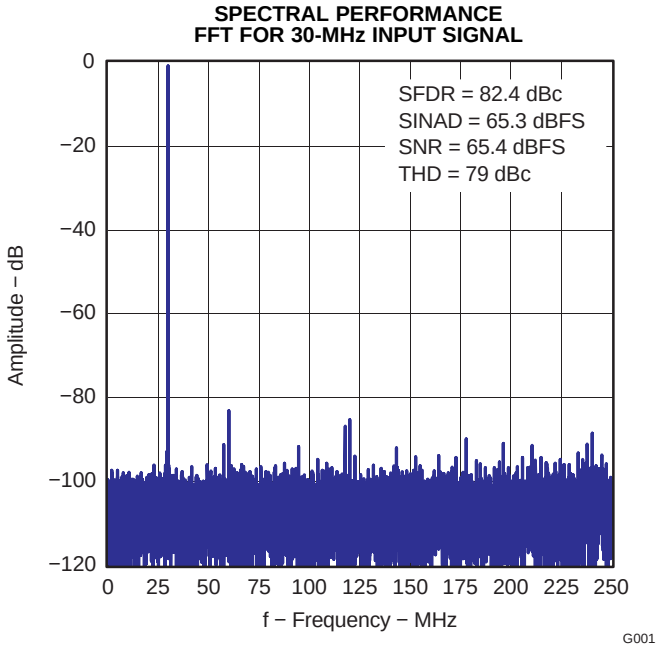
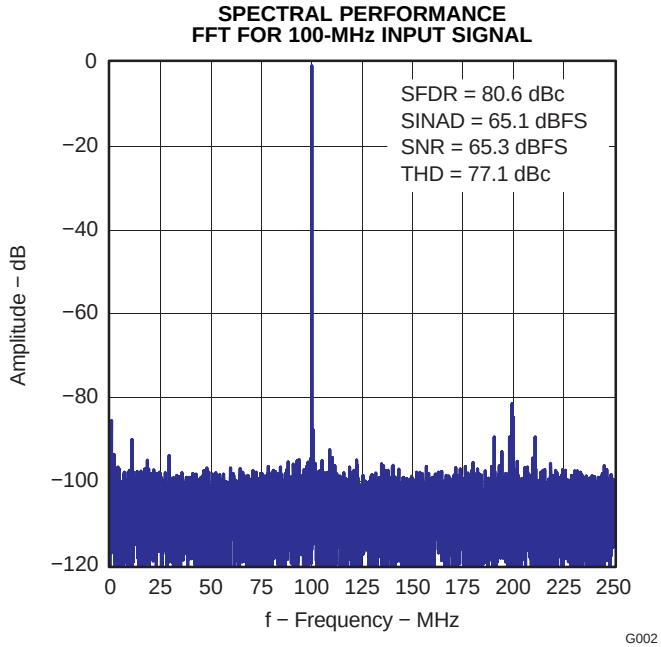


Figure 2.



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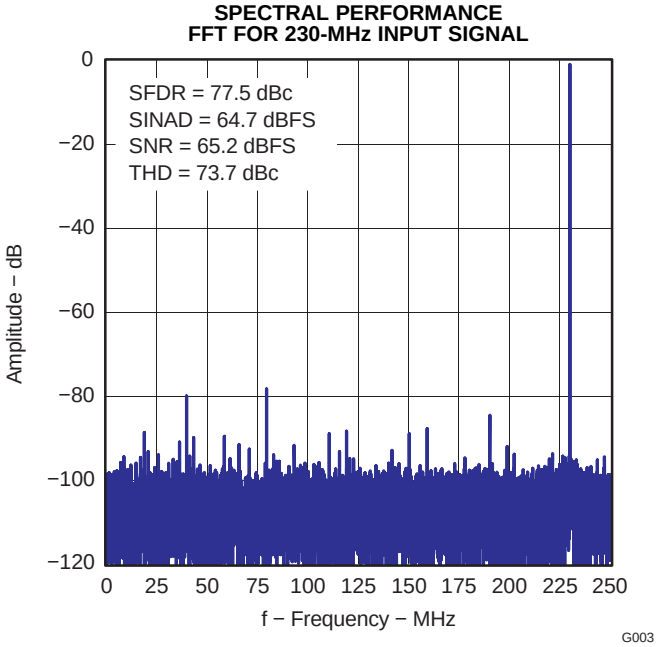

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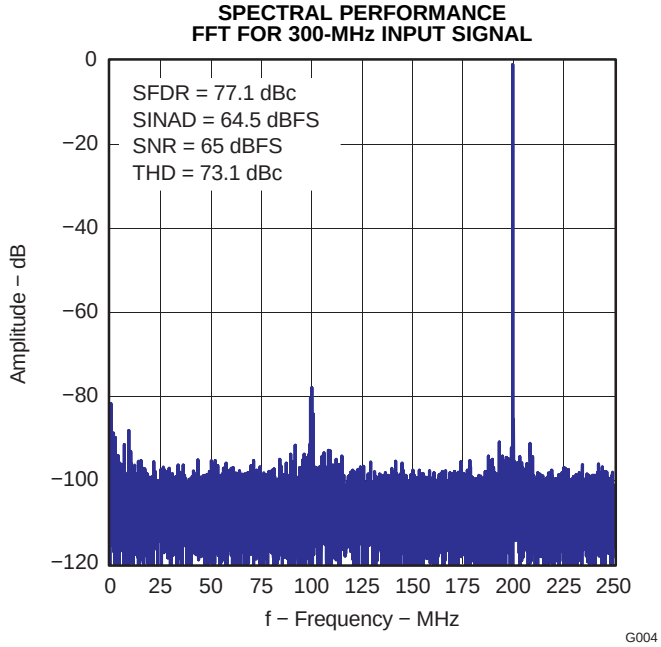

Figure 5.

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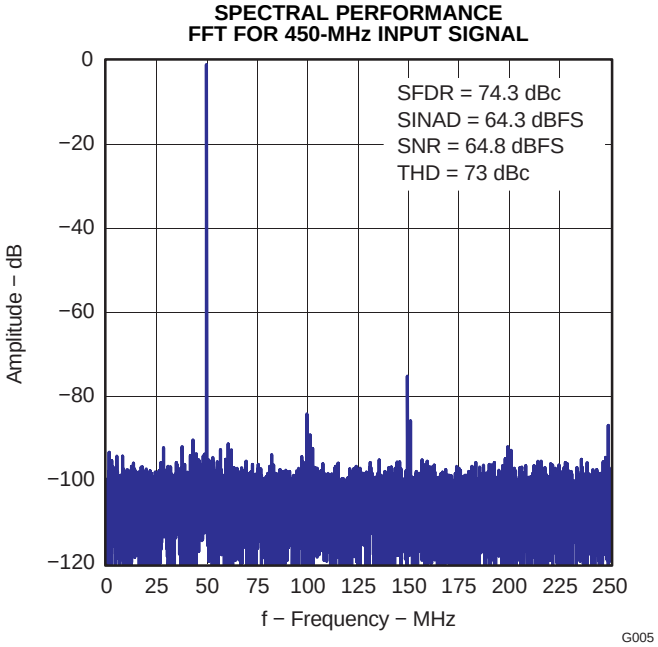
ADS5463 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)



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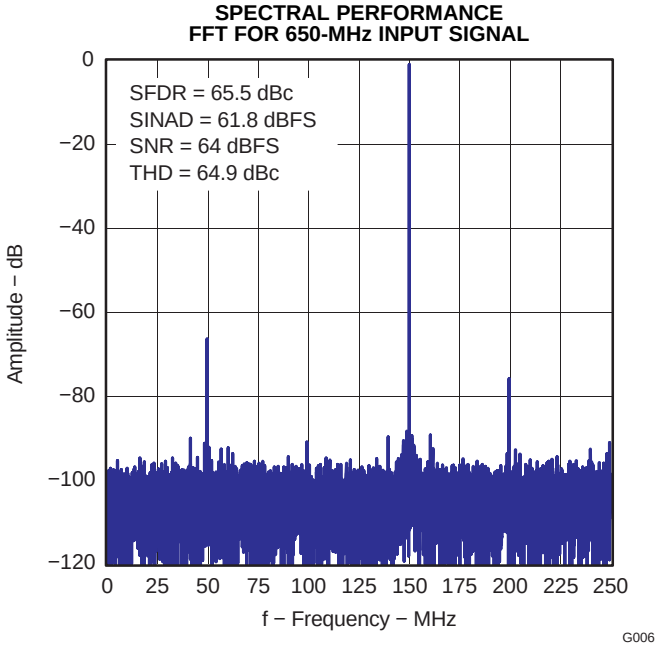

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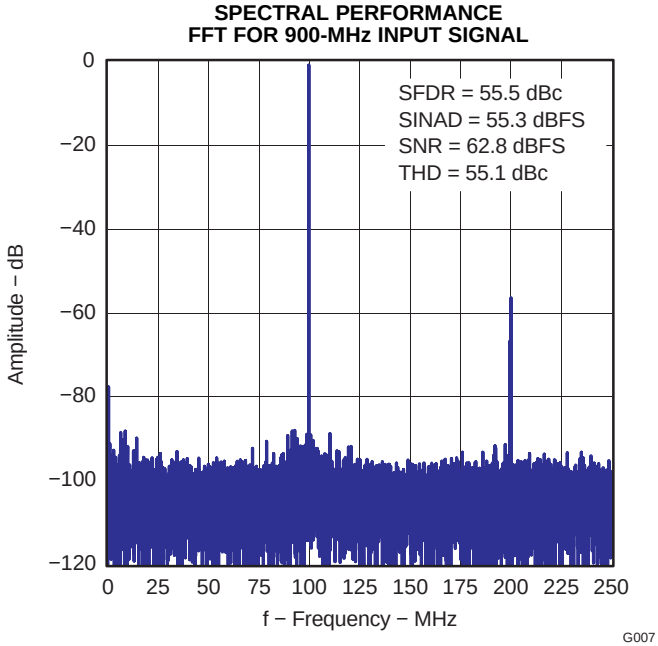

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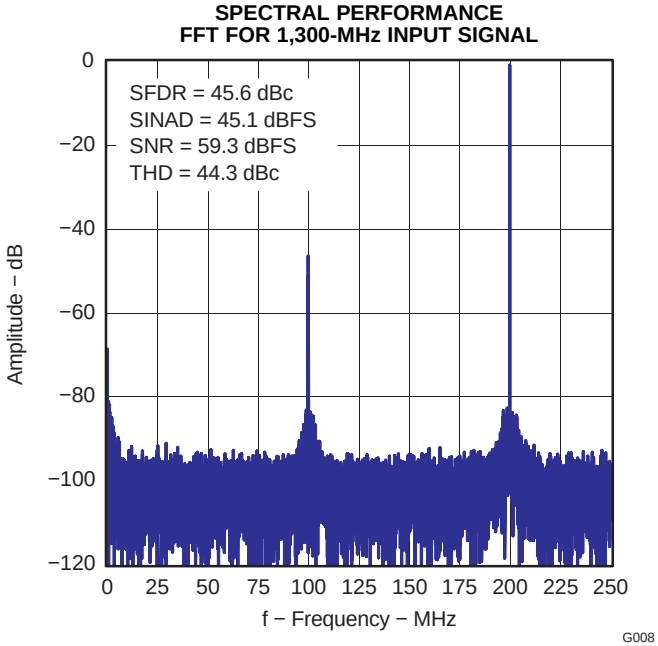

Figure 9.

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ADS5463 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

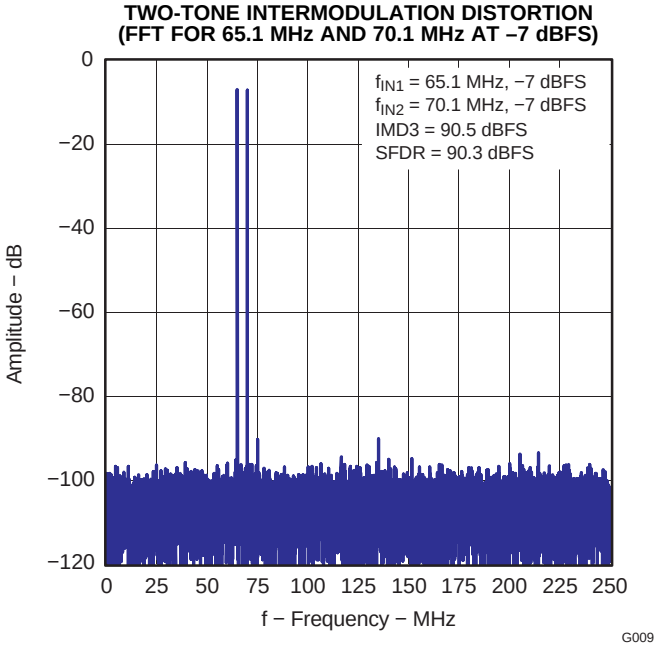


Figure 10.

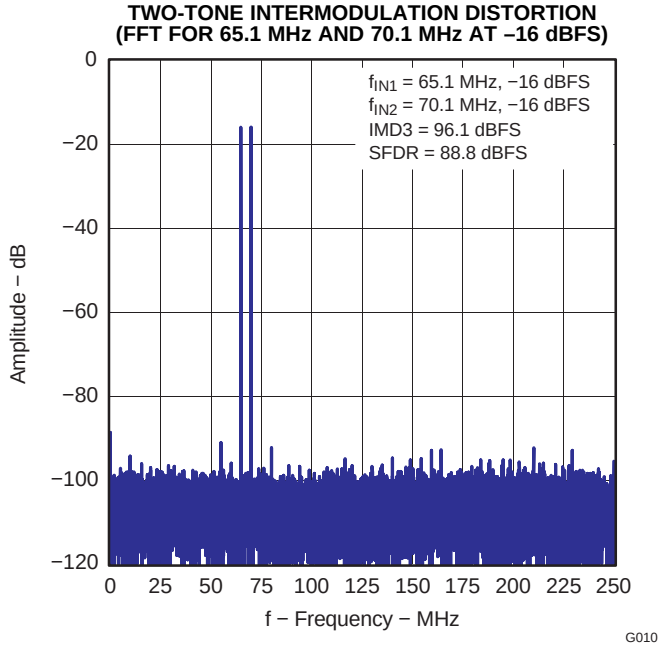
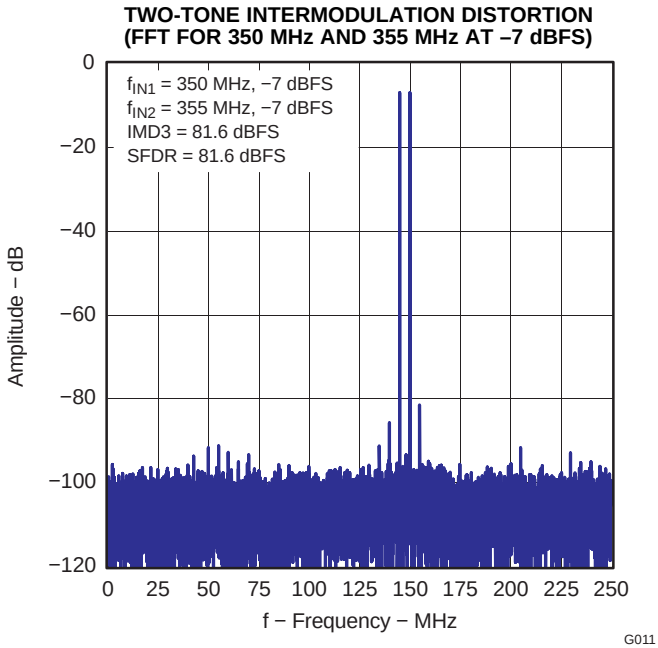


Figure 11.



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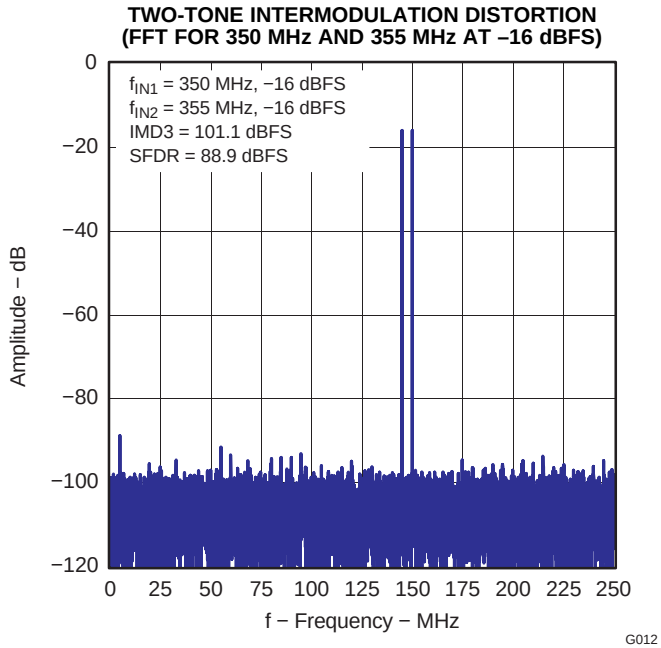
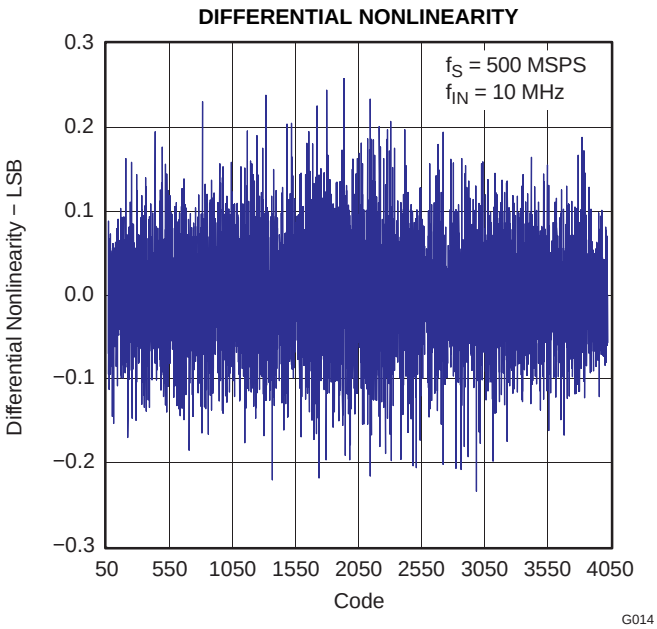


Figure 13.

ADS5463 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)



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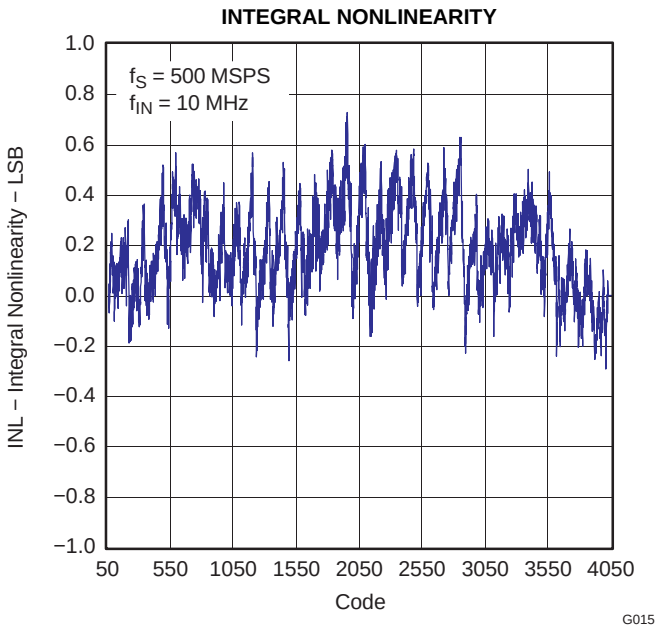

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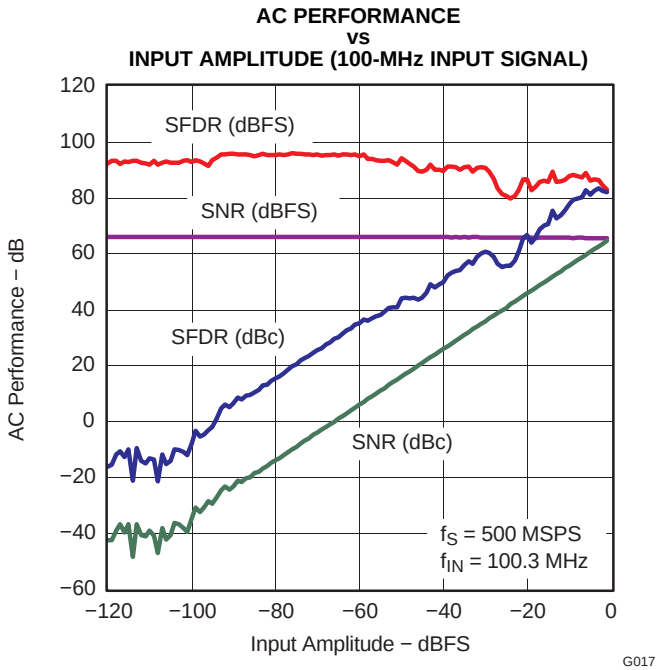

Figure 16.

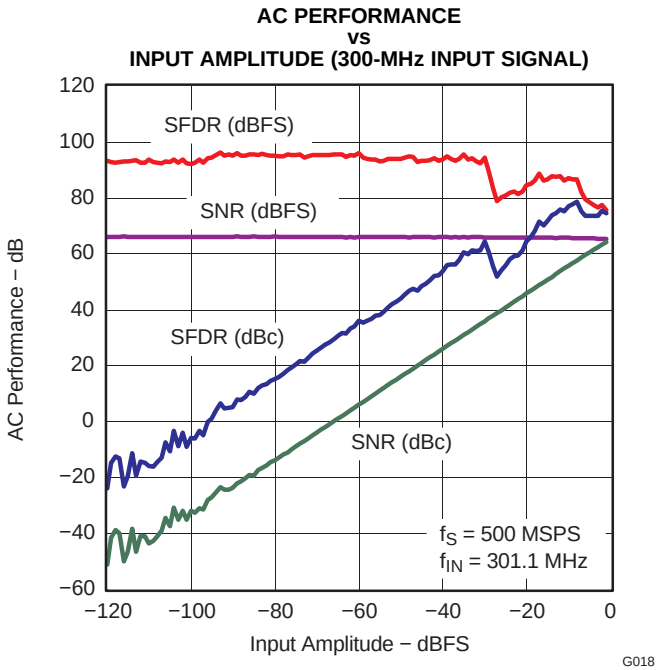

Figure 17.

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ADS5463 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

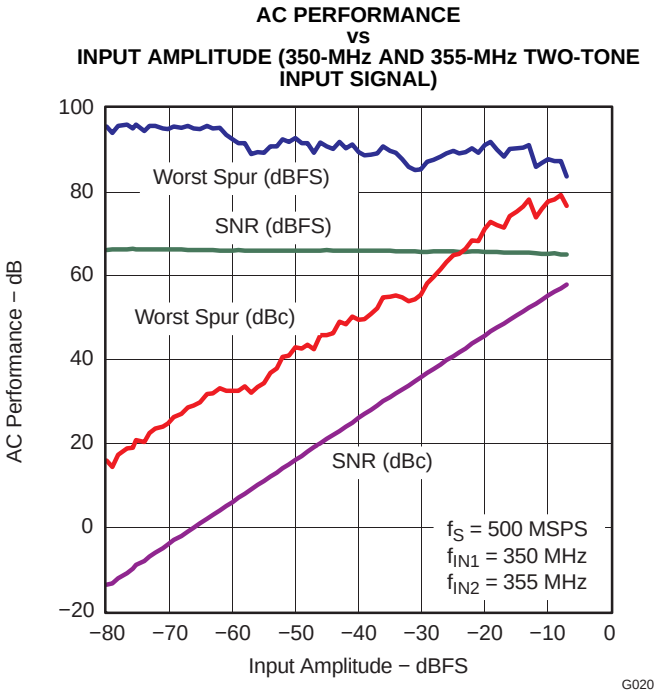
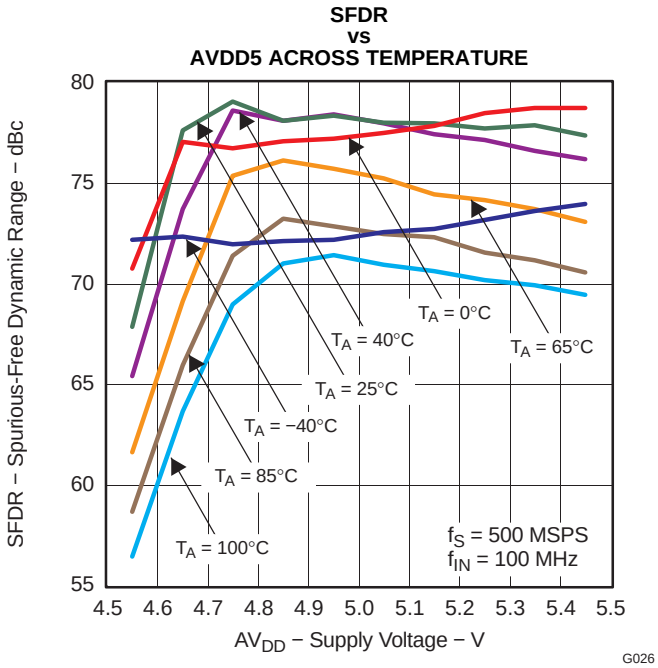


Figure 18.



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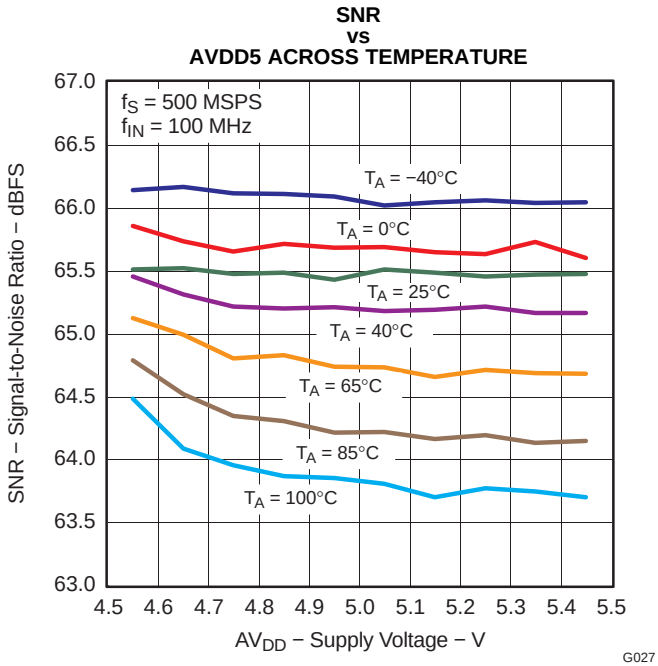

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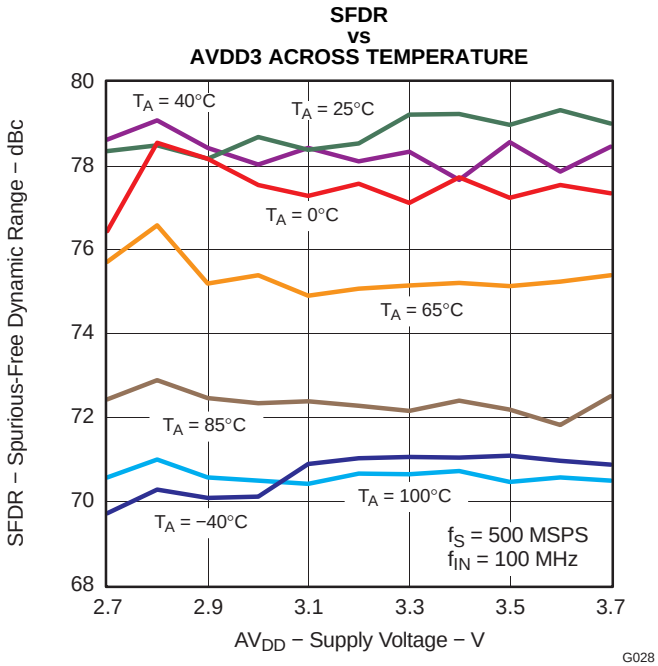
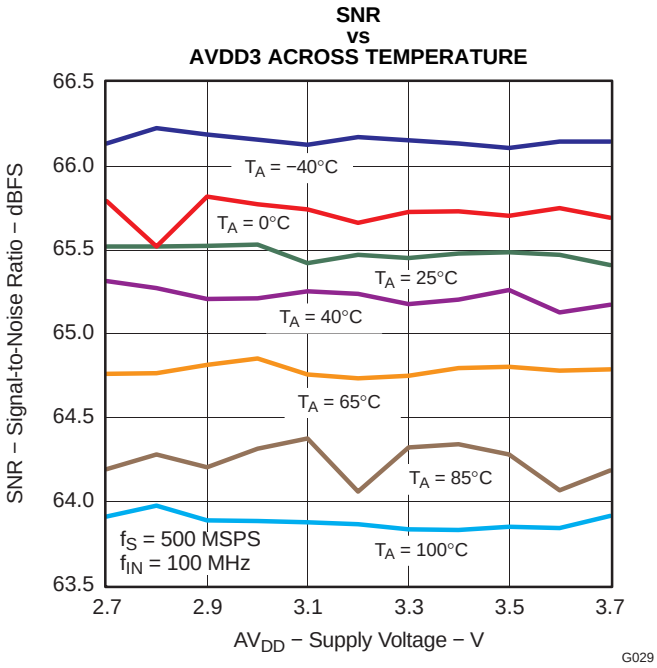


Figure 21.

ADS5463 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)



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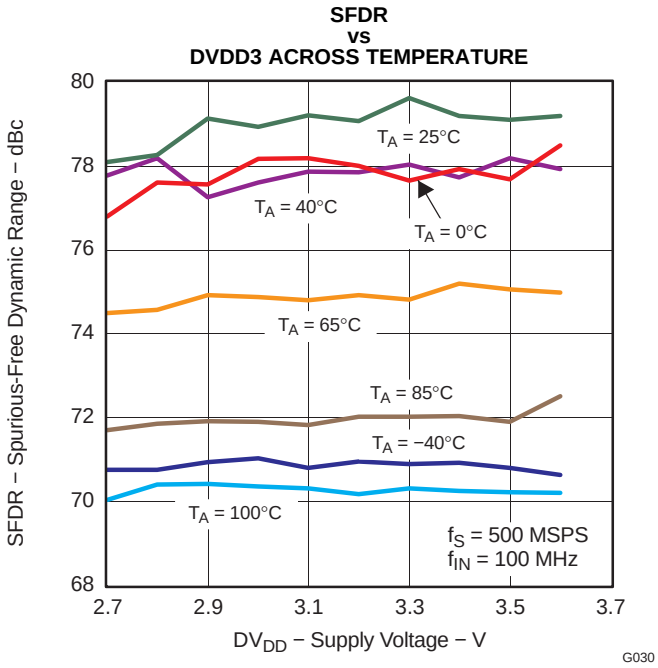

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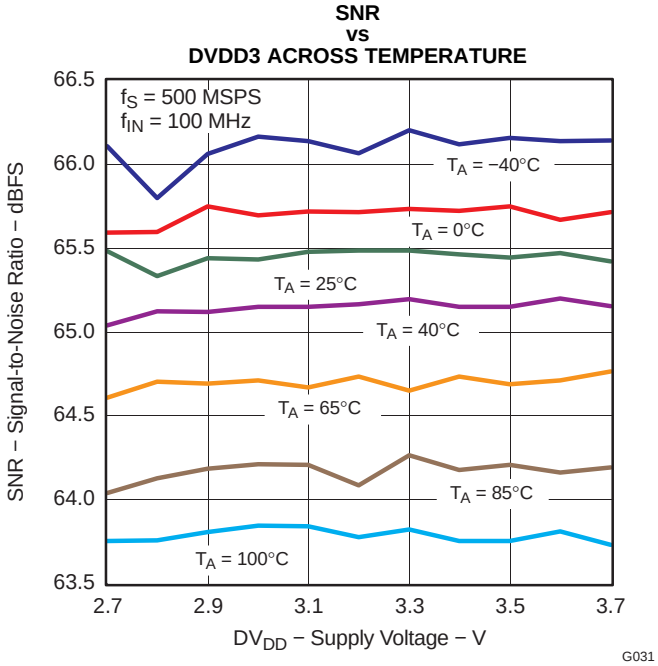

Figure 24.

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ADS5463 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 500 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

SNR vs INPUT FREQUENCY AND SAMPLING FREQUENCY (ADS5463 Only)

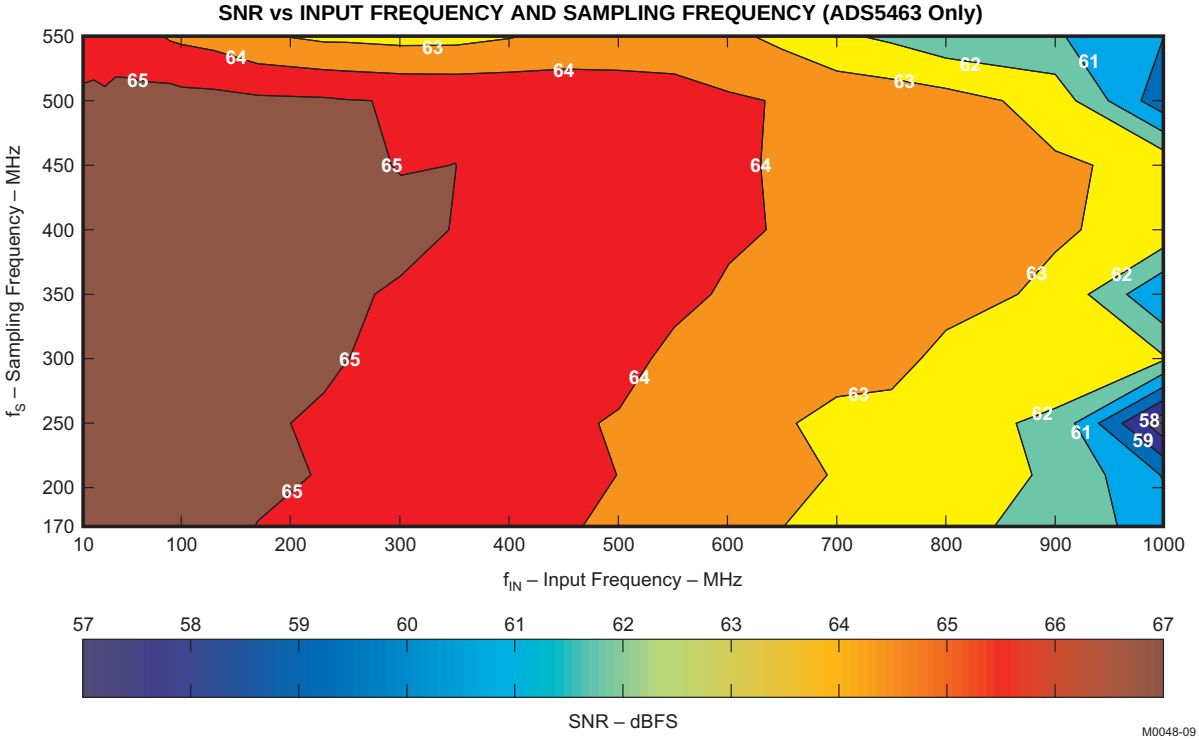


Figure 25.

SFDR vs INPUT FREQUENCY AND SAMPLING FREQUENCY (ADS5463 Only)

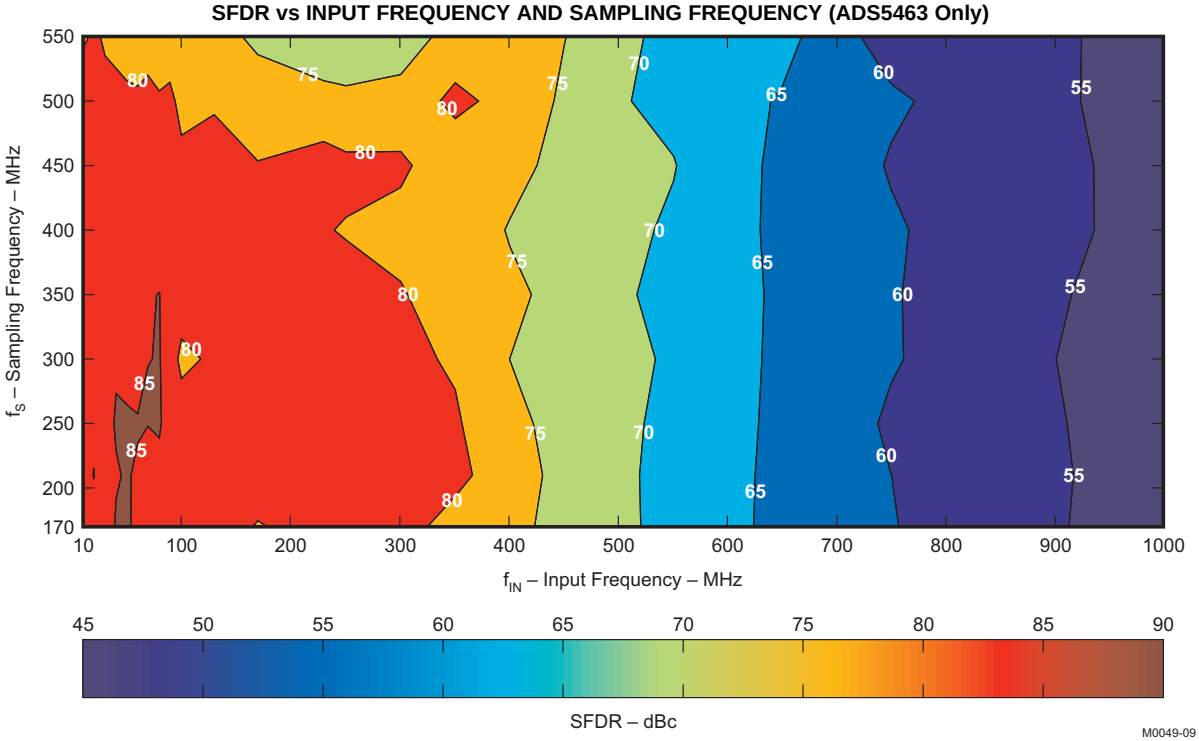


Figure 26.

ADS54RF63 TYPICAL CHARACTERISTICS

Typical plots at T_A = 25°C, sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

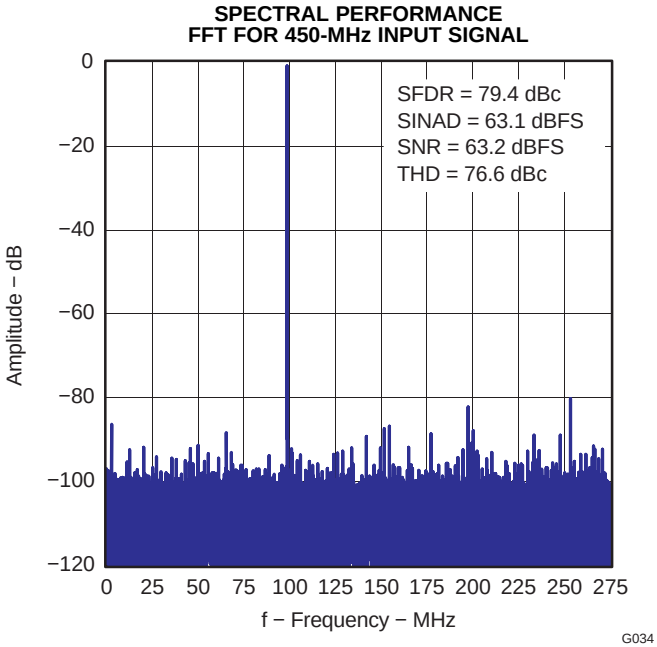


Figure 27.

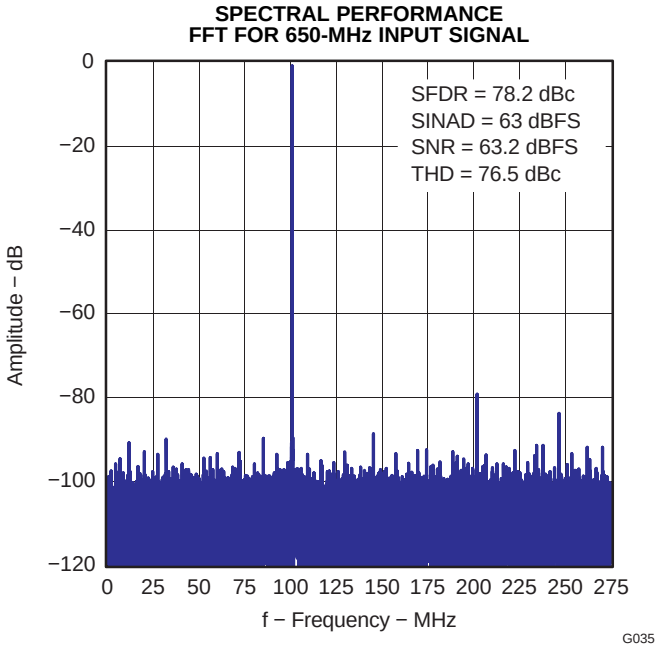
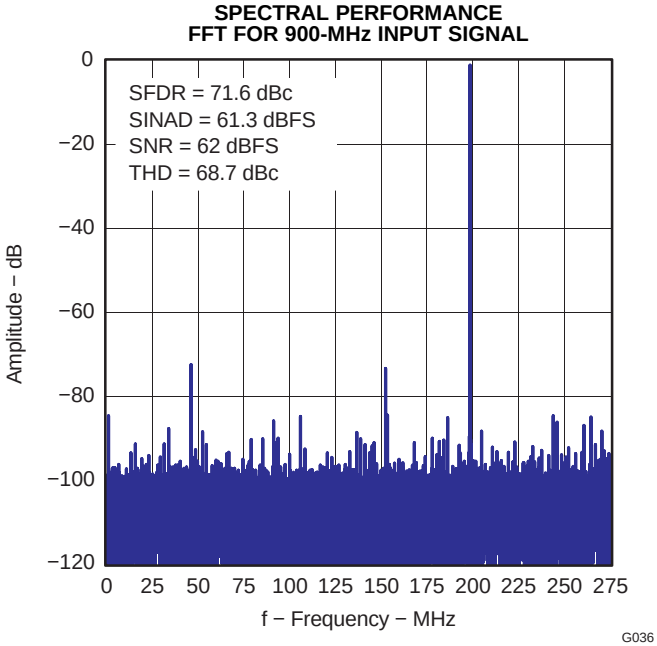


Figure 28.



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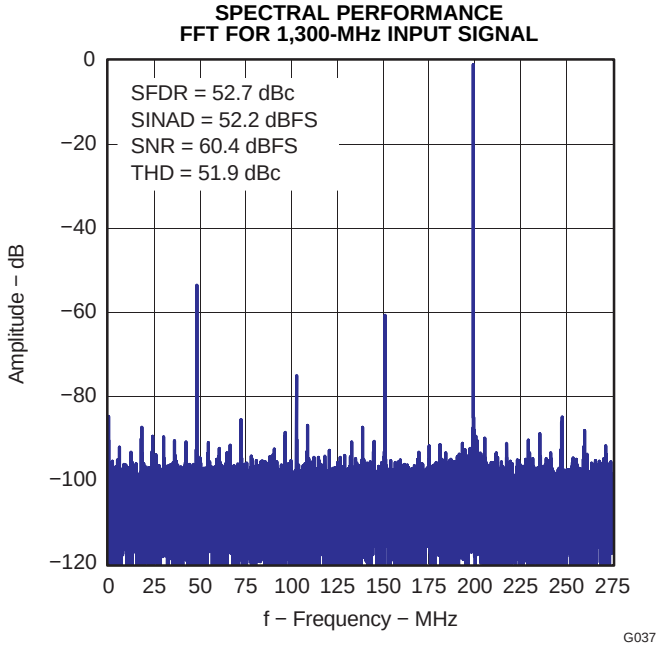

Figure 30.

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ADS54RF63 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

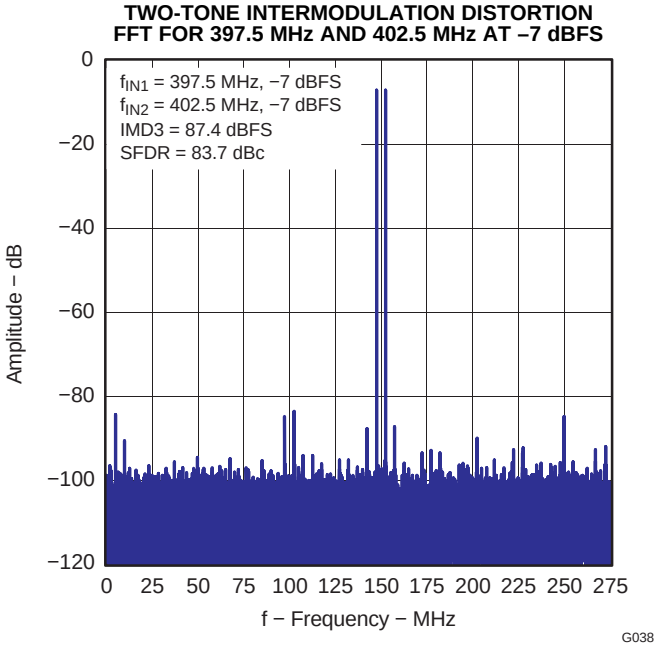
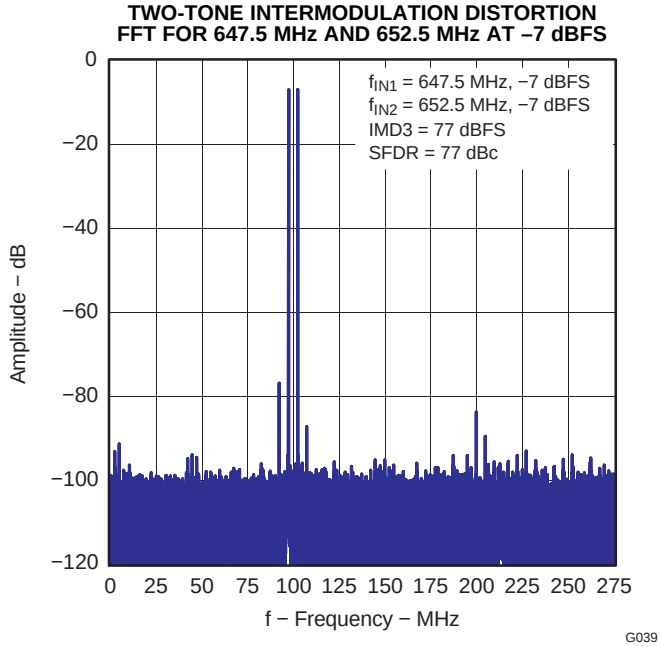


Figure 31.



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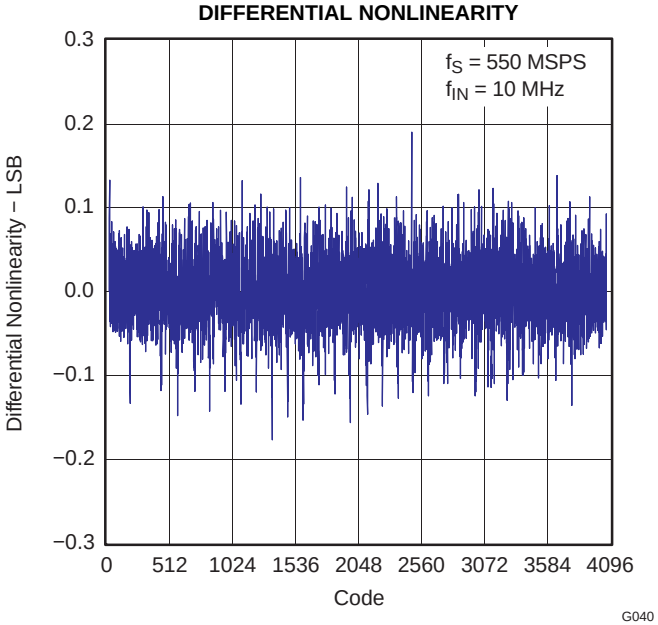

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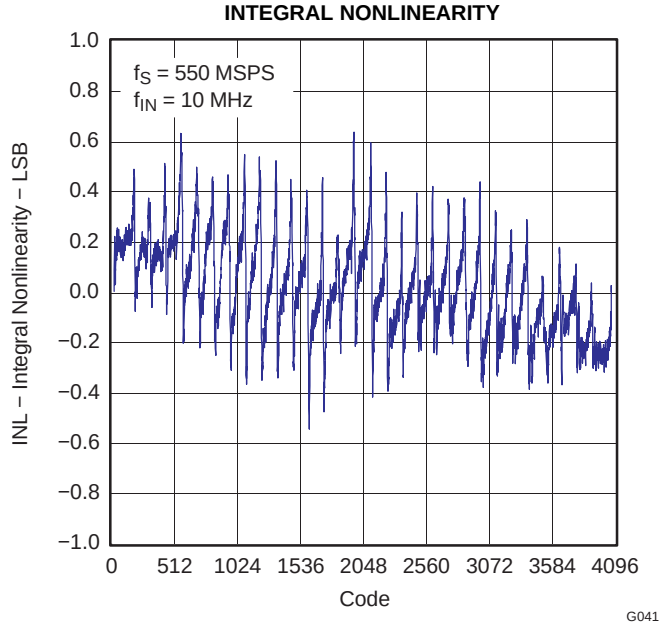

Figure 34.

ADS54RF63 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

AC PERFORMANCE vs INPUT AMPLITUDE (397.5-MHz AND 402.5-MHz TWO-TONE INPUT SIGNAL)

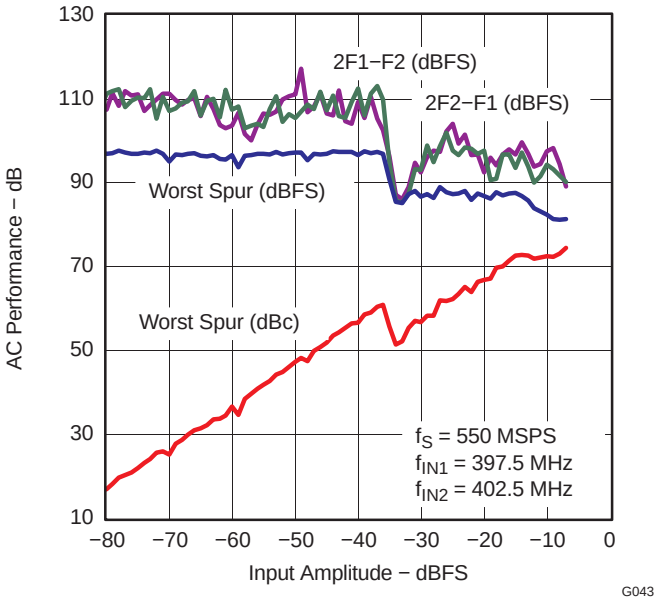

Figure 35.

AC PERFORMANCE vs INPUT AMPLITUDE (647.5-MHz AND 652.5-MHz TWO-TONE INPUT SIGNAL)

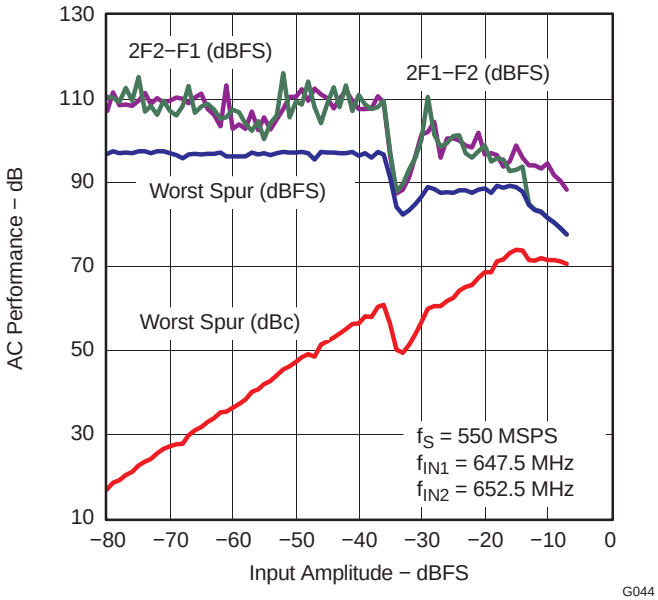

Figure 36.

SFDR vs AVDD5 ACROSS TEMPERATURE

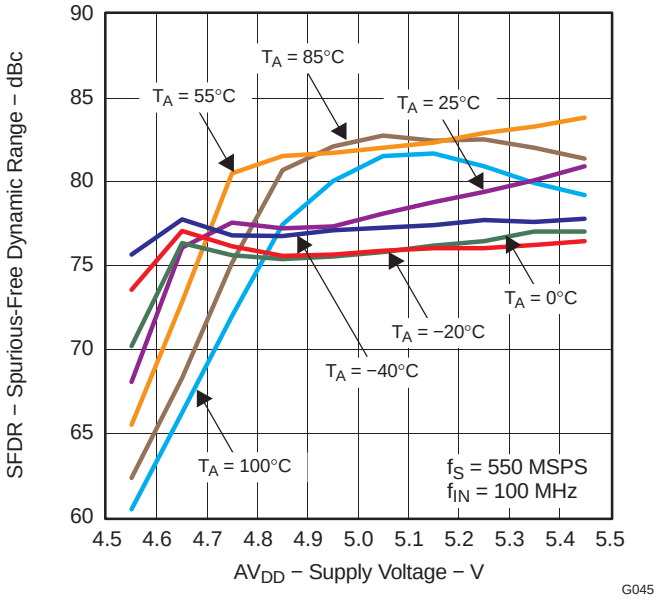

Figure 37.

SNR vs AVDD5 ACROSS TEMPERATURE

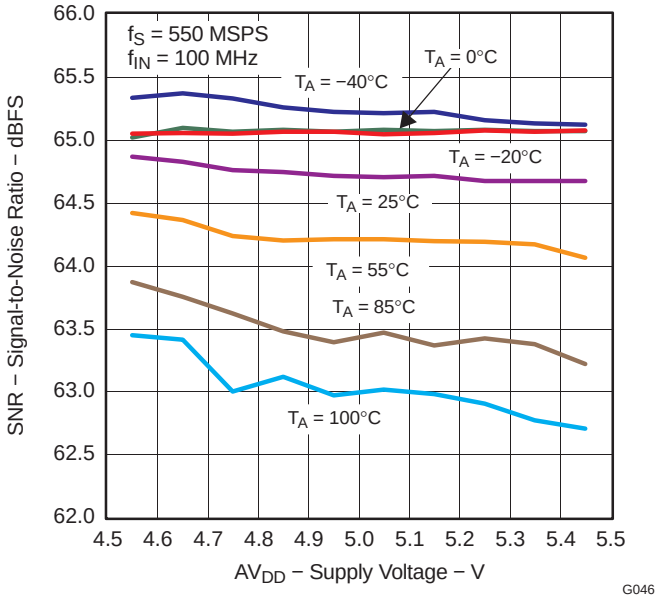

Figure 38.

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ADS54RF63 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

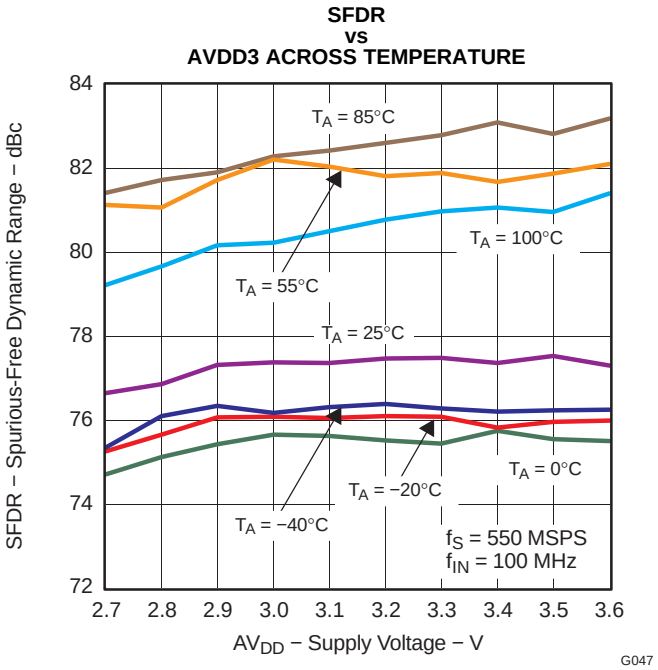

Figure 39.

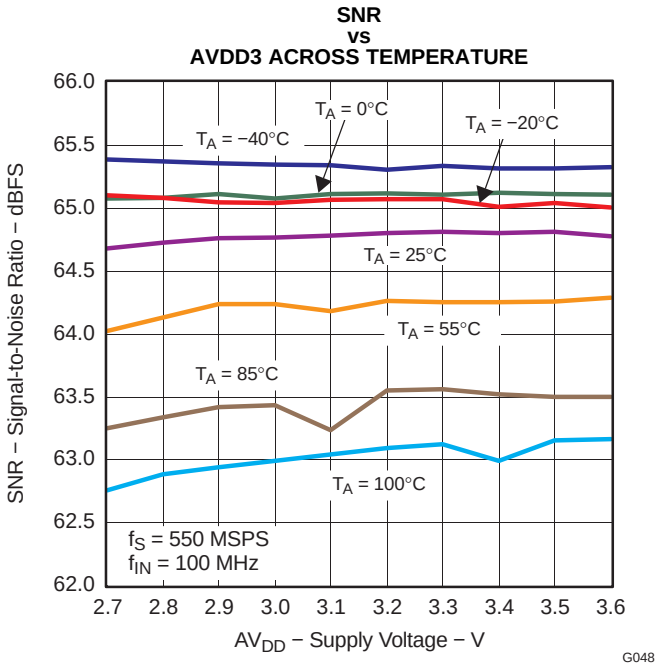

Figure 40.

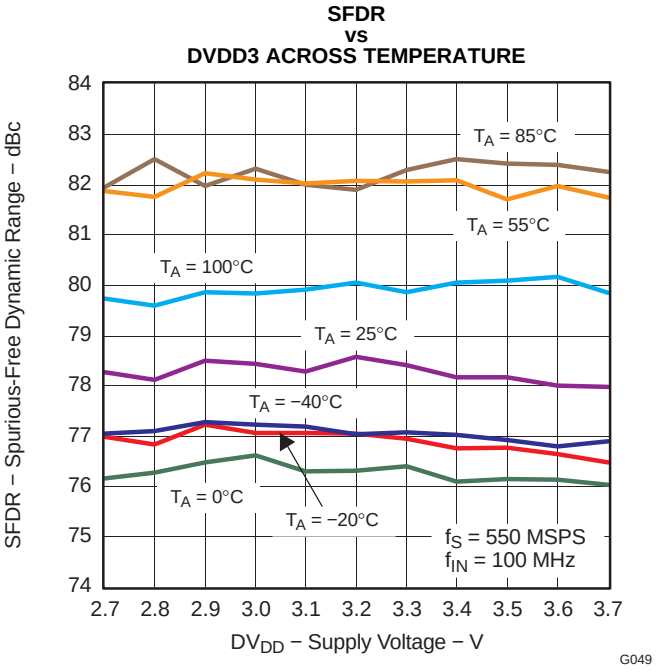

Figure 41.

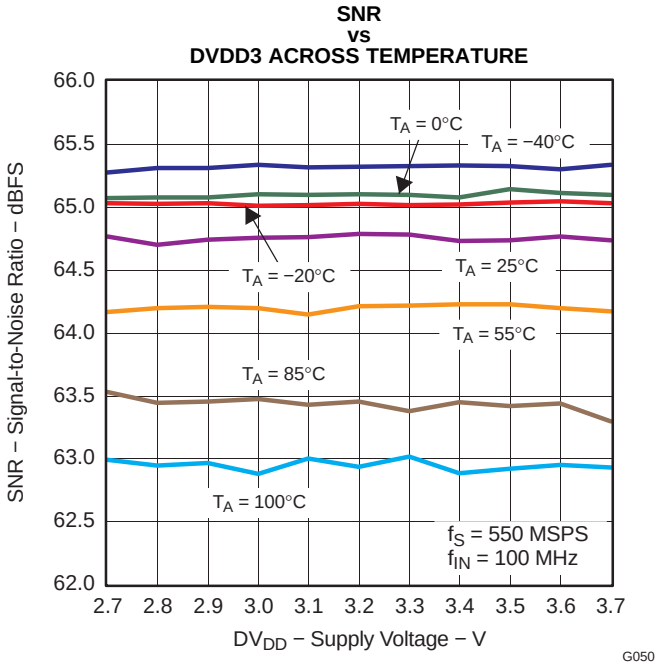

Figure 42.

ADS54RF63 TYPICAL CHARACTERISTICS (continued)

Typical plots at T_A = 25°C, sampling rate = 550 MSPS, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

SNR vs INPUT FREQUENCY AND SAMPLING FREQUENCY (ADS54RF63 Only)

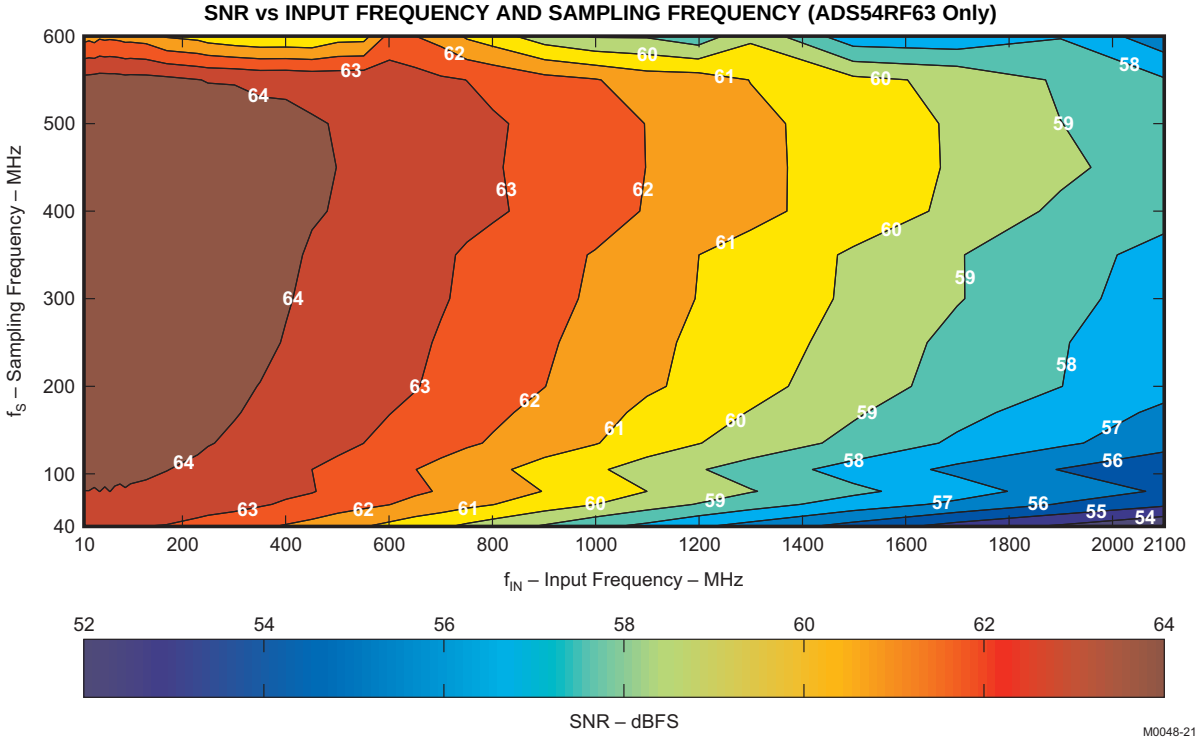

Figure 43.

SFDR vs INPUT FREQUENCY AND SAMPLING FREQUENCY (ADS54RF63 Only)

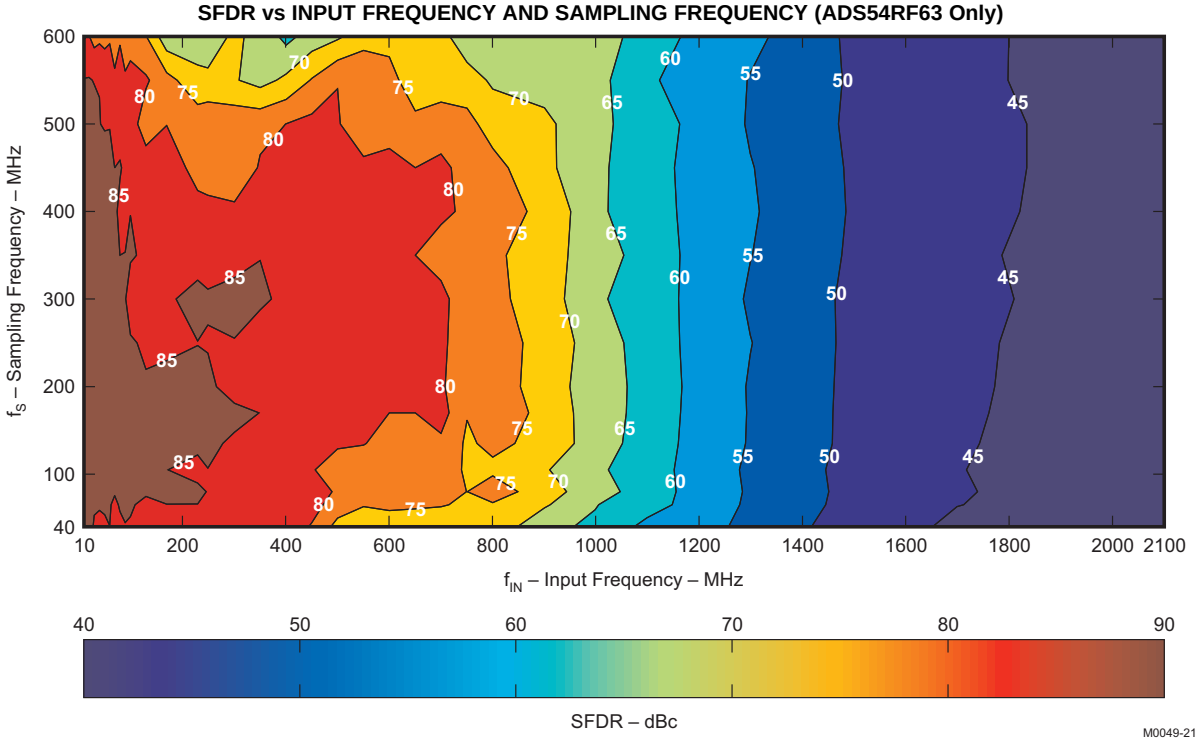

Figure 44.

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ADS5463 AND ADS54RF63 TYPICAL CHARACTERISTICS

Typical plots at T_A = 25°C, 50% clock duty cycle, AVDD5 = 5 V, AVDD3 = 3.3 V, DVDD3 = 3.3 V, and 3-V_{PP} differential clock, (unless otherwise noted)

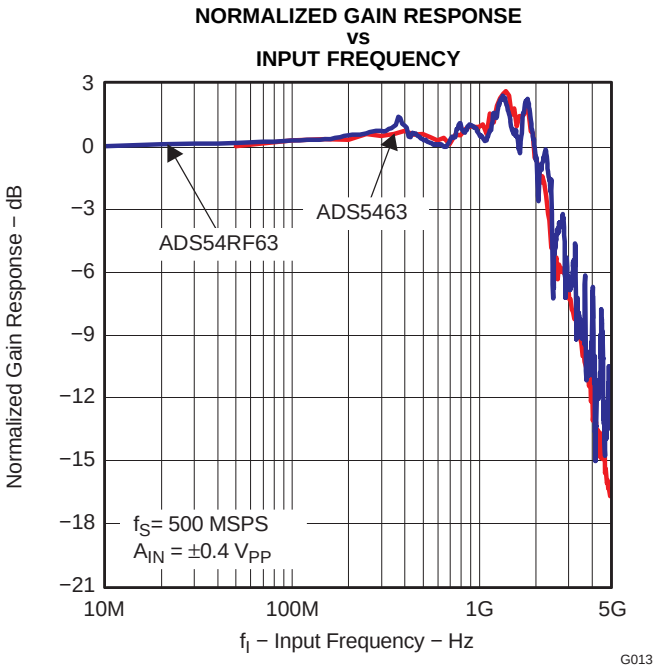

Figure 45.

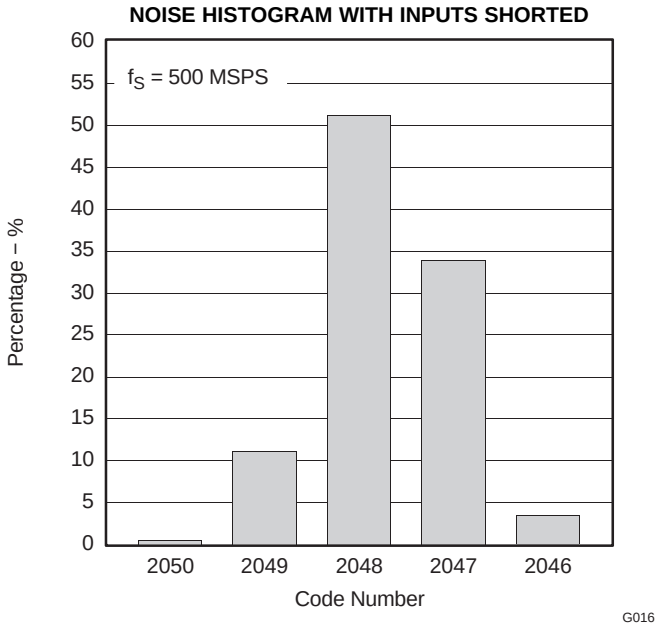

Figure 46.

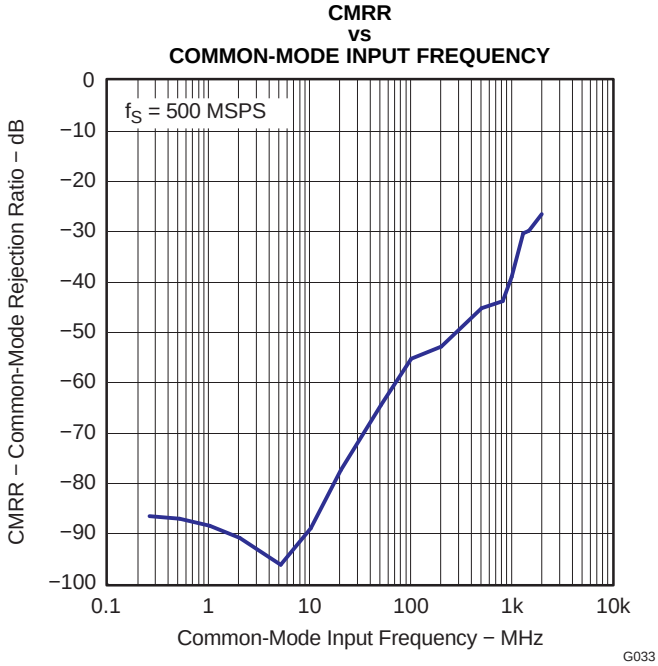

Figure 47.

APPLICATION INFORMATION

Theory of Operation

The ADS5463/ADS54RF63 is a 12-bit, 500/550-MSPS, monolithic pipeline ADC. Its bipolar analog core operates from 5-V and 3.3-V supplies, while the output uses a 3.3-V supply to provide LVDS-compatible outputs. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track-and-hold (T&H), and the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 3.5 clock cycles, after which the output data is available as a 12-bit parallel word, coded in offset binary format.

The ADS5463 and ADS54RF63 are identical in the way they are used on a board. They differ in their maximum sample rate and spectral performance versus frequency. A good study of the contour plots in Figure 25, Figure 26, Figure 43, and Figure 44 demonstrate the spectral differences. The digital output characteristics are the same except the ADS54RF63 has less restrictive timing parameters.

Input Configuration

The analog input for the ADS5463/ADS54RF63 consists of an analog pseudo-differential buffer followed by a bipolar transistor track-and-hold (see Figure 48). The analog buffer isolates the source driving the input of the ADC from any internal switching and presents a high impedance to drive at high input frequencies, as compared to an ADC without a buffered input. The input common mode is set internally through a 500-Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ. The 0.5 pF of parasitic package capacitance is before soldering.

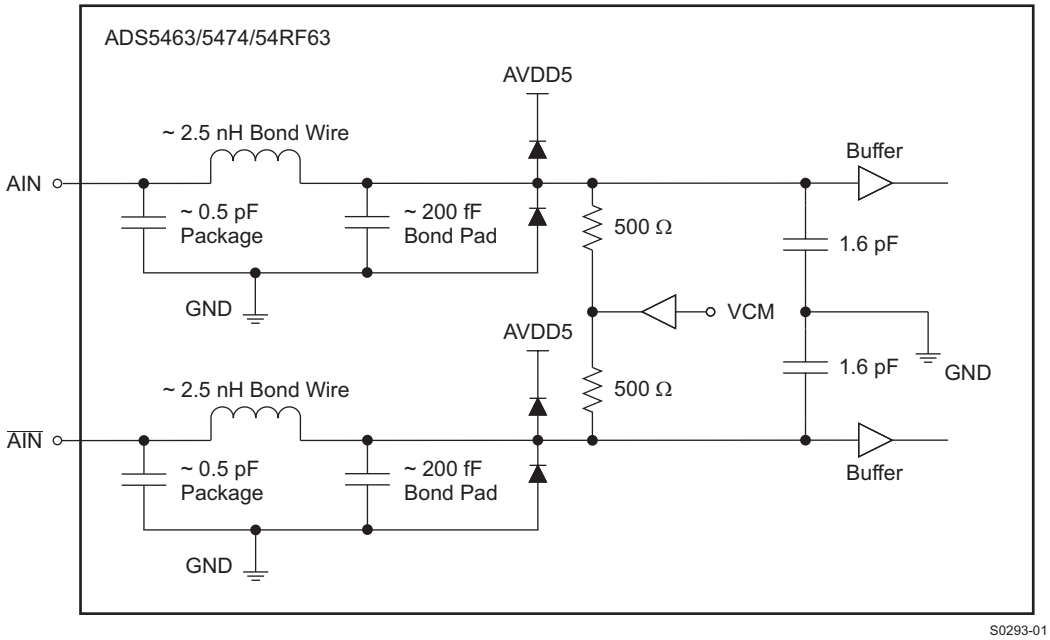

Figure 48. Analog Input Equivalent Circuit (unsoldered)

For a full-scale differential input, each of the differential lines of the input signal (pins 16 and 17) swing symmetrically between 2.4 V + 0.55 V and 2.4 V – 0.55 V. This means that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. Operation below 2.2 V_{PP} is allowable, with the characteristics of performance versus input amplitude demonstrated in Figure 16 and Figure 17. For instance, for performance at 1.1 V_{PP} rather than 2.2 V_{PP}, see the SNR and SFDR at -6 dBFS (0 dBFS = 2.2 V_{PP}). The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose.

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The ADS5463/ADS54RF63 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 49 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. In addition, the evaluation module is configured with two back-to-back transformers, which also demonstrates good performance. If voltage gain is required, a step-up transformer can be used.

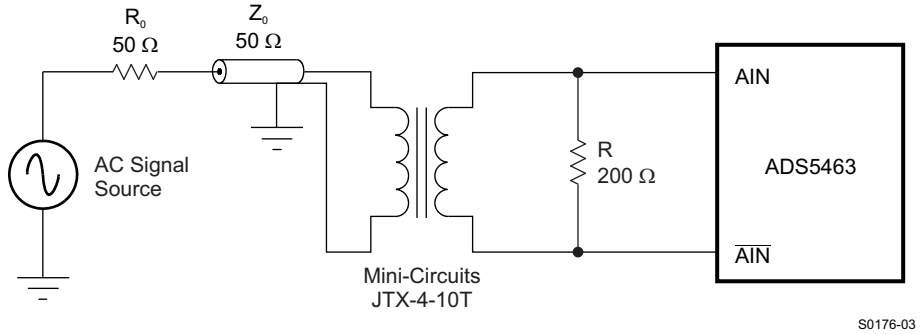

Figure 49. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

In addition to the transformer configurations, an RF gain-block amplifier, such as the Texas Instruments THS9001, can also be used for high-input-frequency applications. For large voltage gains at intermediate frequencies in the 50-MHz – 350-MHz range, the configuration shown in Figure 50 can be used. The component values can be tuned for different intermediate frequencies. The example shown is located on the evaluation module and is tuned for an IF of 170 MHz. More information regarding this configuration can be found in the *ADS5463 EVM User Guide* (SLAU194) and the *THS9001 50 MHz to 350 MHz Cascadeable Amplifier* data sheet (SLOS426).

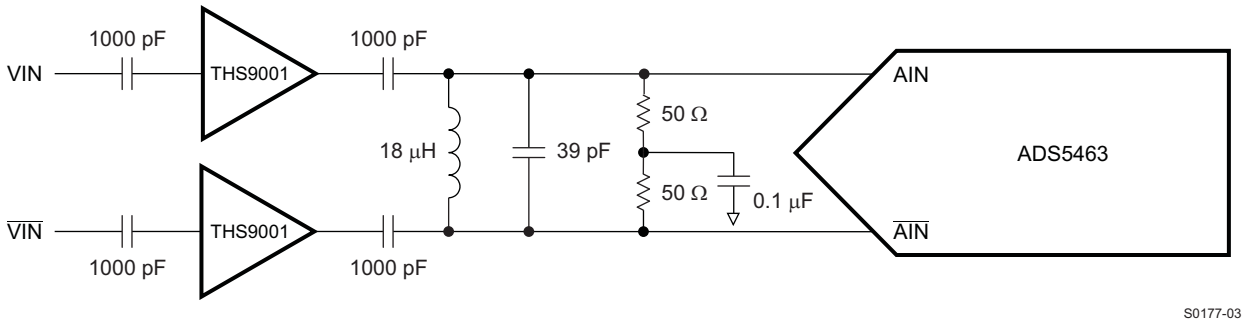

Figure 50. Using the THS9001 IF Amplifier with the ADS5463/ADS54RF63

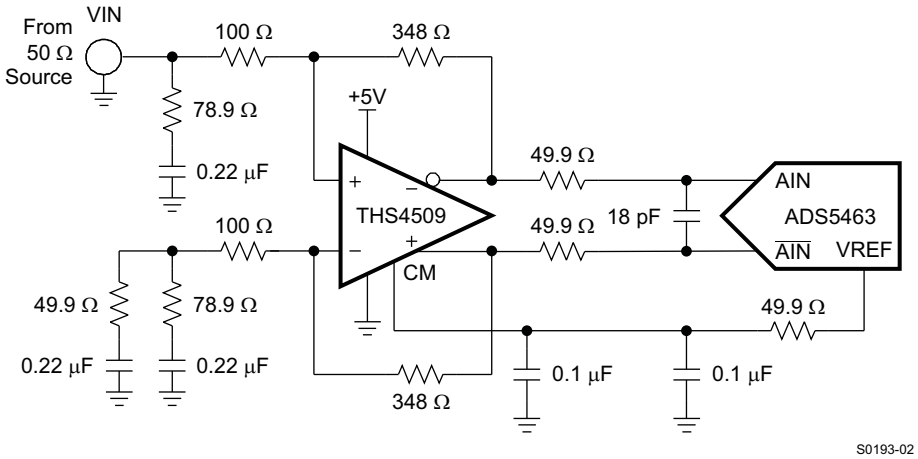

Figure 51. Using the THS4509 with the ADS5463/ADS54RF63

For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier like the THS4509 (see Figure 51) provides good harmonic performance and low noise over a wide range of frequencies. Notice that VREF is used for the common mode with the ADS5463/ADS54RF63 and ADS5444/5440, whereas VCM must be used with the ADS5474.

In this configuration, the THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5463/ADS54RF63 by using the VREF pin from the ADC. The 50-Ω resistors and 18-pF capacitor between the THS4509 outputs and ADS5463/ADS54RF63 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 70 MHz (–3 dB). Input termination is accomplished via the 78.9-Ω resistor and 0.22-µF capacitor to ground, in conjunction with the input impedance of the amplifier circuit. A 0.22-µF capacitor and 49.9-Ω resistor are inserted to ground across the 78.9-Ω resistor and 0.22-µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348-Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50-Ω termination for other common gains. Because the ADS5463/ADS54RF63 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with Vs+ = 5 V and Vs– = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

Over-Range Analog Input Recovery Error

An over-range condition occurs if the analog input voltage exceeds the full-scale range of the converter (0dBFS, nominally 2.2 V_{pp}). To test recovery from an over-range, the ADC analog input is injected with a sinusoidal input frequency exactly at CLKIN/4 (a four-point sinusoid). The four sample points of each period theoretically occur at the top, mid-scale, bottom and mid-scale of the sinusoid. Once the amplitude exceeds 0dBFS, the top and bottom of the sinusoidal input becomes out of range, while the mid-scale points are always in-range and therefore measureable. The graph in Figure 52 indicates the amount of error from the expected mid-scale value of 2048 that occurs after negative over-range (bottom of sinusoid went out of range) and positive over-range (top of sinusoid went out of range). Due to the four point sinusoid, this equates to the amount of error in a valid sample 1 clock cycle after an over-range occurs as a function of amplitude. The errors generally increase as a function of input over-range amplitude, though non-monotonically.

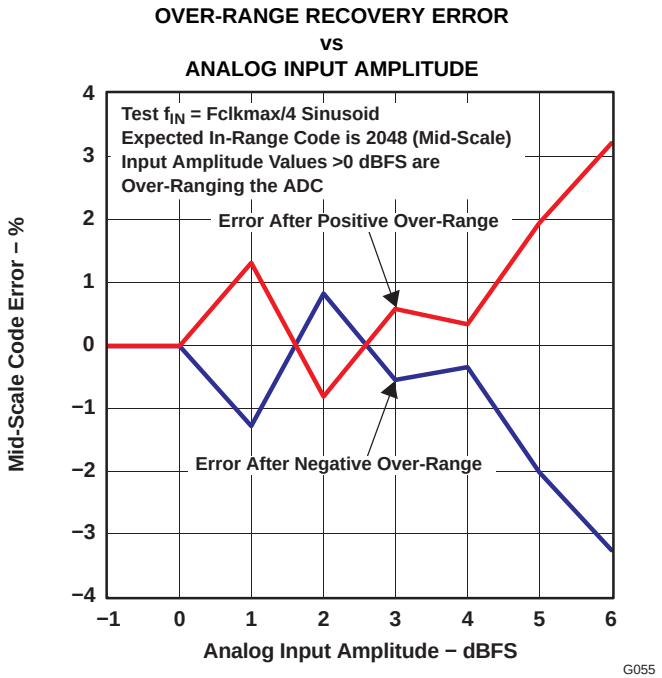

Figure 52.

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External Voltage Reference

For systems that require the analog signal gain to be adjusted or calibrated, this can be performed by using an external reference. The dependency on the signal amplitude to the value of the external reference voltage is characterized typically by Figure 53 (VREF = 2.4 V is normalized to 0 dB as this is the internal reference voltage). (This figure is the average gain adjustment from the data collected from -1dBFS to -6dBFS in 1 dB steps.) As can be seen in the linear fit, this equates to approximately –0.3 dB of signal adjustment per 100 mV of reference adjustment. The range of allowable variation depends on the analog input amplitude that is applied to the inputs and the desired spectral performance, as can be seen in the performance versus external reference graphs in Figure 54 and Figure 55. As the applied analog signal amplitude is reduced, more variation in the reference voltage is allowed in the positive direction (which equates to a reduction in signal amplitude), whereas an adjustment in reference voltage below the nominal 2.4 V (which equates to an increase in signal amplitude) is not recommended below approximately 2.35 V. The power consumption versus reference voltage and operating temperature should also be considered, especially at high ambient temperatures, because the lifetime of the device is affected by internal junction temperature, see Figure 68.

The ADS5463/ADS54RF63 does not have a VCM output pin and uses the VREF pin to provide the common-mode voltage in dc-coupled applications. The ADS5463/ADS54RF63 (VCM = 2.4 V) and ADS5474 (VCM = 3.1 V) do not have the same common-mode voltage, but they do share the same approximate VREF (2.4 V). To create a board layout that may accommodate both devices in dc-coupled applications, route the VCM of the ADS5474 and the VREF of the ADS5463/ADS54RF63 both to a common point that can be selected via a switch, jumper, or a 0-Ω resistor to be used as the common-mode voltage of the driving circuit.

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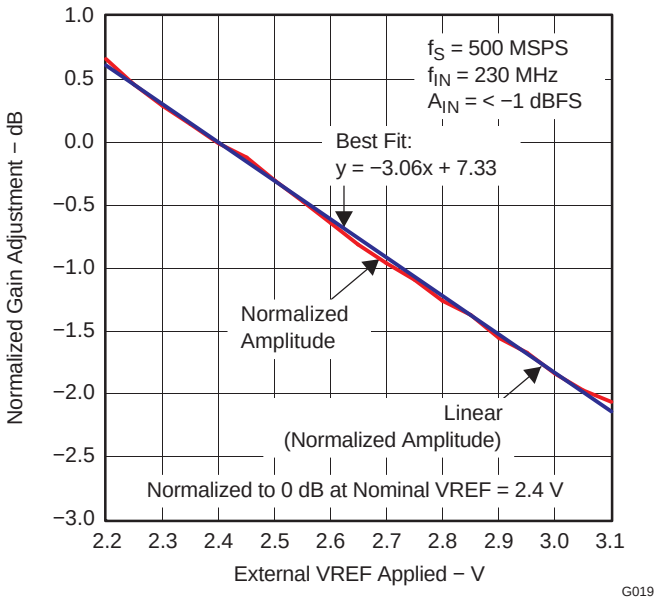

Figure 53. ADS5463 Signal Gain Adjustment versus External Reference (VREF)

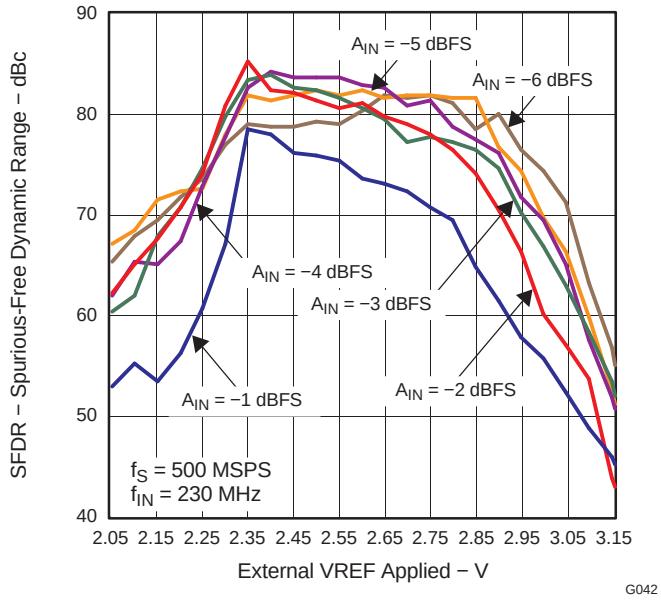

Figure 54. ADS5463 SFDR versus External VREF and A_{IN}

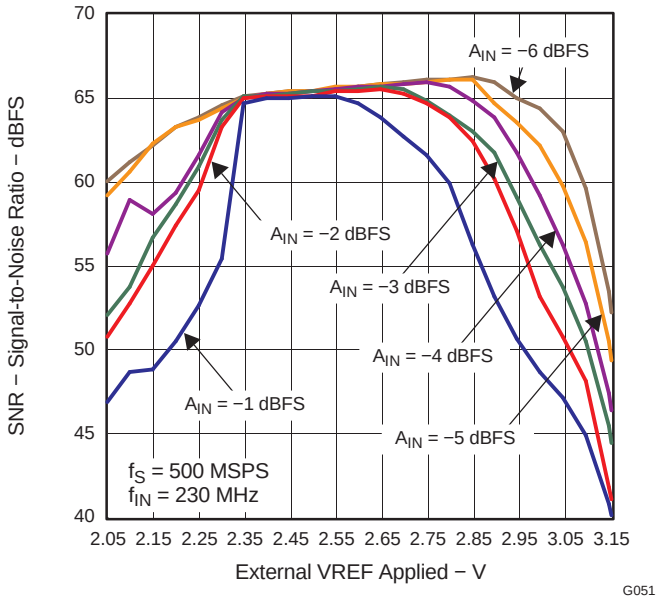

Figure 55. ADS5463 SNR versus External VREF and A_{IN}

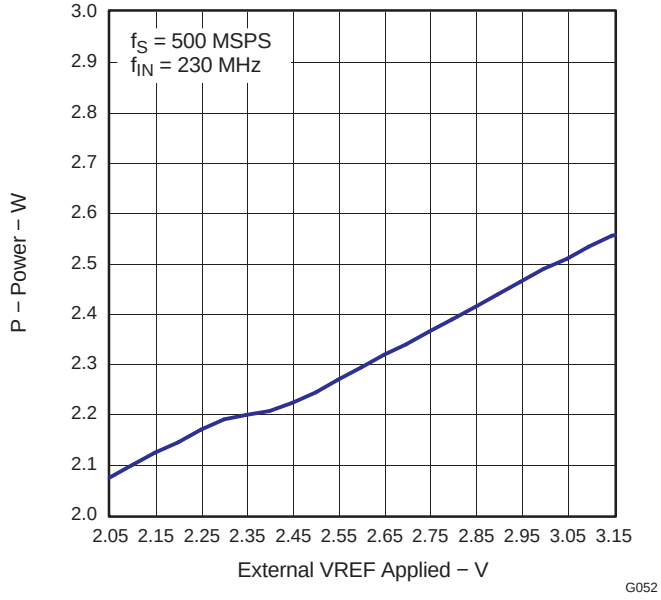

Figure 56. Total Power Consumption versus External VREF

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Clock Inputs

The ADS5463/ADS54RF63 clock input can be driven with either a differential clock signal or a single-ended clock input. The equivalent clock input circuit can be seen in Figure 57. The 0.5 pF of parasitic package capacitance is before soldering. When jitter may not be a big concern, the use of a single-ended clock (as shown in Figure 58) could save cost and board space without much performance tradeoff. When clocked with this configuration, it is best to connect $\overline{CLK}$ to ground with a 0.01-µF capacitor, while CLK is ac-coupled with a 0.01-µF capacitor to the clock source, as shown in Figure 58.

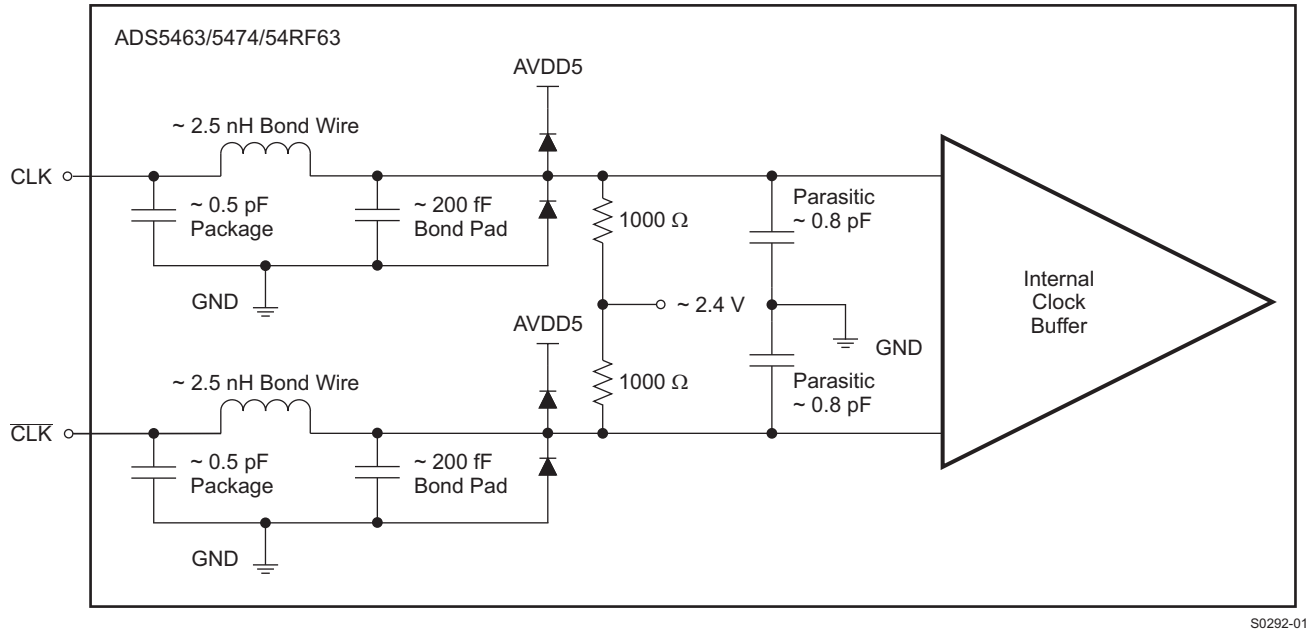

Figure 57. Clock Input Circuit (unsoldered package)

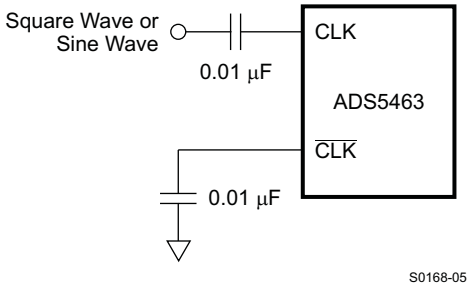

Figure 58. Single-Ended Clock

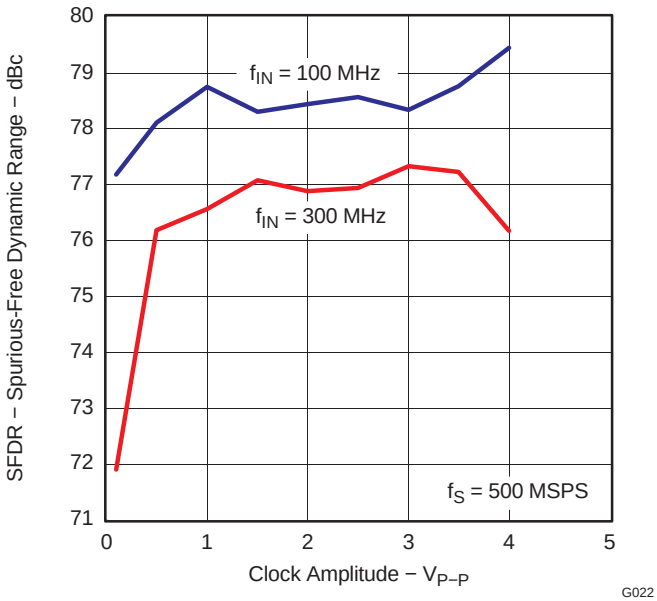

Figure 59. ADS5463 SFDR versus Differential Clock Level

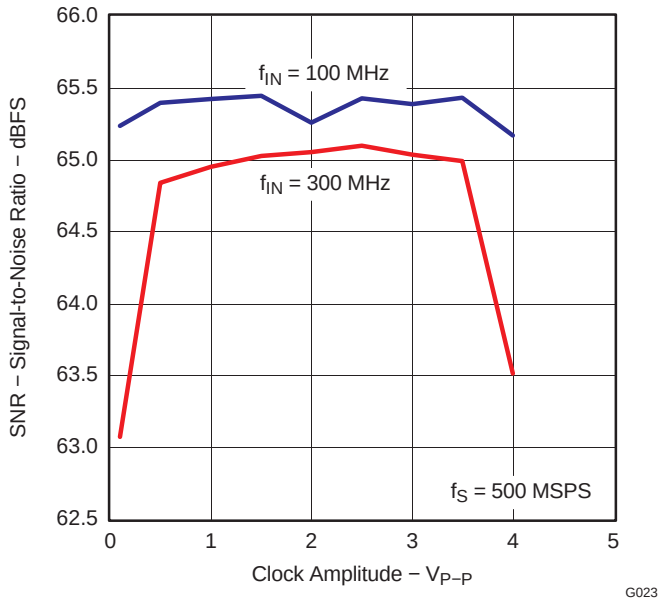

Figure 60. ADS5463 SNR versus Differential Clock Level

The characterization of the ADS5463/ADS54RF63 is typically performed with a 3-V_{PP} differential clock, but the ADC performs well with a differential clock amplitude down to ~0.5 V_{PP} (250-mV swing on both CLK and $\overline{CLK}$), as shown in Figure 59 and Figure 60. For jitter-sensitive applications, the use of a differential clock has some advantages at the system level. The differential clock allows for common-mode noise rejection at the printed circuit board (PCB) level. With a differential clock, the signal-to-noise ratio of the ADC is better for jitter-sensitive, high-frequency applications because the board level clock jitter is superior.

Larger clock amplitude levels are recommended for high analog input frequencies or slow clock frequencies. At high analog input frequencies, the sampling process is sensitive to jitter. At slow clock frequencies, a small amplitude sinusoidal clock has a lower slew rate and can create jitter-related SNR degradation due to the uncertainty in the sampling point associated with a slow slew rate. Figure 61 demonstrates a recommended method for converting a single-ended clock source into a differential clock; it is similar to the configuration found on the evaluation board and was used for much of the characterization. See also *Clocking High Speed Data Converters* (SLYT075) for more details.

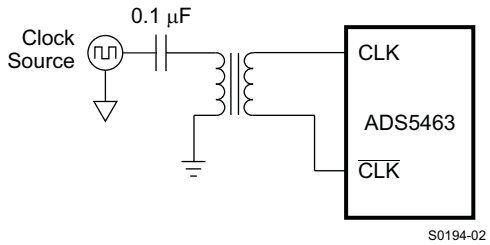

Figure 61. Differential Clock

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1-kΩ resistors (see Figure 57). It is recommended to use ac coupling, but if this scheme is not possible, the ADS5463 features good tolerance to clock common-mode variation, as shown in Figure 62 and Figure 63 (the ADS54RF63 behaves similarly). The internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty-cycle clock signal should be provided, though even 40/60 is good enough for many applications. Performance degradation as a result of duty cycle can be seen in Figure 64.

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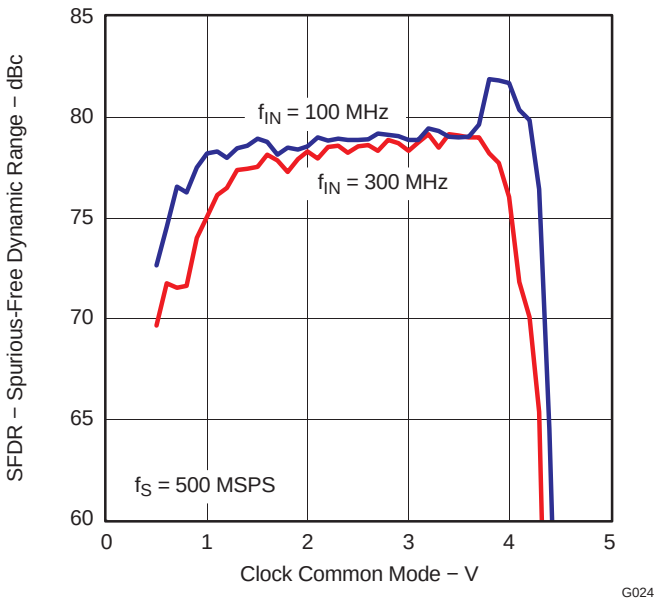

Figure 62. ADS5463 SFDR versus Clock Common Mode

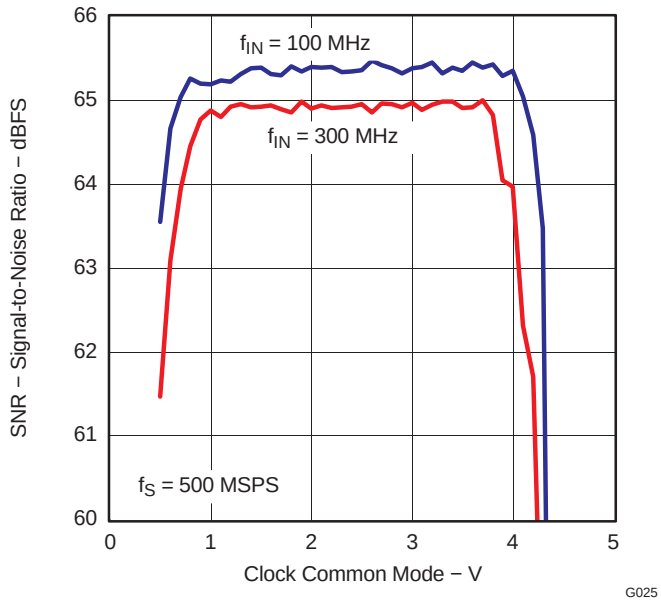

Figure 63. ADS5463 SNR versus Clock Common Mode

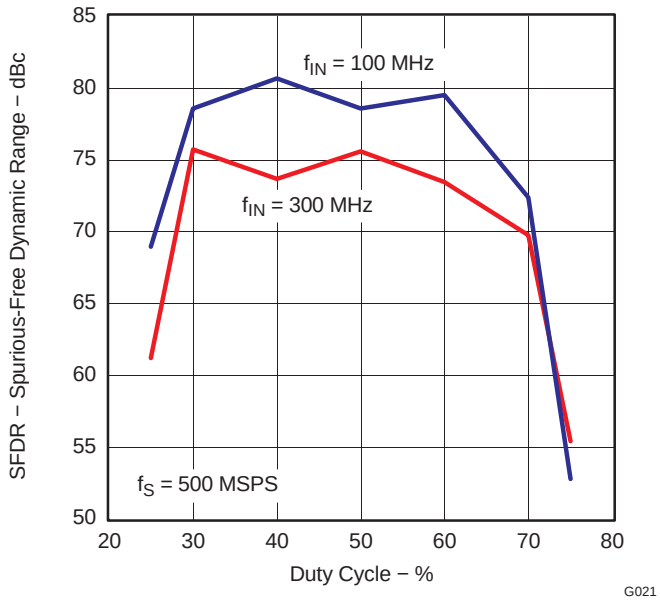

Figure 64. ADS5463 SFDR vs Clock Duty Cycle

To understand how to determine the required clock jitter, an example is useful. The ADS5463 is capable of achieving 63.6 dBFS SNR at 450 MHz of analog input frequency. In order to achieve this SNR at 450 MHz the clock source rms jitter must be at least 181 fsec when combined with the 150 fsec of internal aperture jitter in order for the total rms jitter to be 234 fsec. A summary of maximum recommended rms clock jitter as a function of analog input frequency is provided in Table 2 (using 150 fsec of internal aperture jitter). The equations used to create the table are also presented.

Table 2. Recommended RMS Clock Jitter

INPUT FREQUENCY (MHz)	MEASURED SNR (dBc)	TOTAL JITTER (fsec rms)	MAXIMUM CLOCK JITTER (fsec rms)
10	64.4	9590	9589
70	64.4	1370	1362
100	64.3	970	959
230	64.1	432	405
300	64	335	300
450	63.6	234	181
650	62.9	175	94
1300	58.3	149	16

Equation 1 and Equation 2 are used to estimate the required clock source jitter.

$$\text{SNR (dBc)} = -20 \times \text{LOG10}\,(2 \times \pi \times f_{IN} \times j_{TOTAL}) \quad (1)$$

$$j_{TOTAL} = (j_{ADC}^{2} + j_{CLOCK}^{2})^{1/2} \quad (2)$$

where:

j_{TOTAL} = the rms summation of the clock and ADC aperture jitter;
j_{ADC} = the ADC internal aperture jitter which is located in the data sheet;
j_{CLOCK} = the rms jitter of the clock at the clock input pins to the ADC; and
f_{IN} = the analog input frequency.

Notice that the SNR is a strong function of the analog input frequency, not the clock frequency. The slope of the clock source edges can have a mild impact on SNR as well and is not taken into account for these estimates. For this reason, maximizing clock source amplitudes at the ADC clock inputs is recommended, though not required (faster slope is desirable for jitter-related SNR). For more information on clocking high-speed ADCs, see application note SLWA034, *Implementing a CDC7005 Low Jitter Clock Solution For High-Speed, High-IF ADC Devices*. Recommended clock distribution chips (CDCs) are the TI CDC7005, the CDCM7005, and the CDCE72010. Depending on the jitter requirements, a band pass filter (BPF) is sometimes required between the CDC and the ADC. If the insertion loss of the BPF causes the clock amplitude to be too low for the ADC, or the clock source amplitude is too low to begin with, an inexpensive amplifier can be placed between the CDC and the BPF.

Figure 65 represents a scenario where an LVCMOS single-ended clock output is used from a TI CDCM7005 with the clock signal path optimized for maximum amplitude and minimum jitter. This type of conditioning might generally be well-suited for use with greater than 250 MHz of input frequency. The jitter of this setup is difficult to estimate and requires a careful phase noise analysis of the clock path. The BPF (and possibly a low-cost amplifier because of insertion loss in the BPF) can improve the jitter between the CDC and ADC when the jitter provided by the CDC is still not adequate. The total jitter at the CDCM7005 output depends largely on the phase noise of the VCXO selected, as well as the CDCM7005, and typically has 50 fs – 100 fs of rms jitter. If it is determined that the jitter from the CDCM7005 with a VCXO is sufficient without further conditioning, it is possible to clock the ADS5463/ADS54RF63 directly from the CDCM7005 using differential LVPECL outputs, as illustrated in Figure 66 (see the CDCM7005 data sheet for the exact schematic). This scenario may be more suitable for less than 150 MHz of input frequency where jitter is not as critical. A careful analysis of the required jitter and of the components involved is recommended before determining the proper approach.

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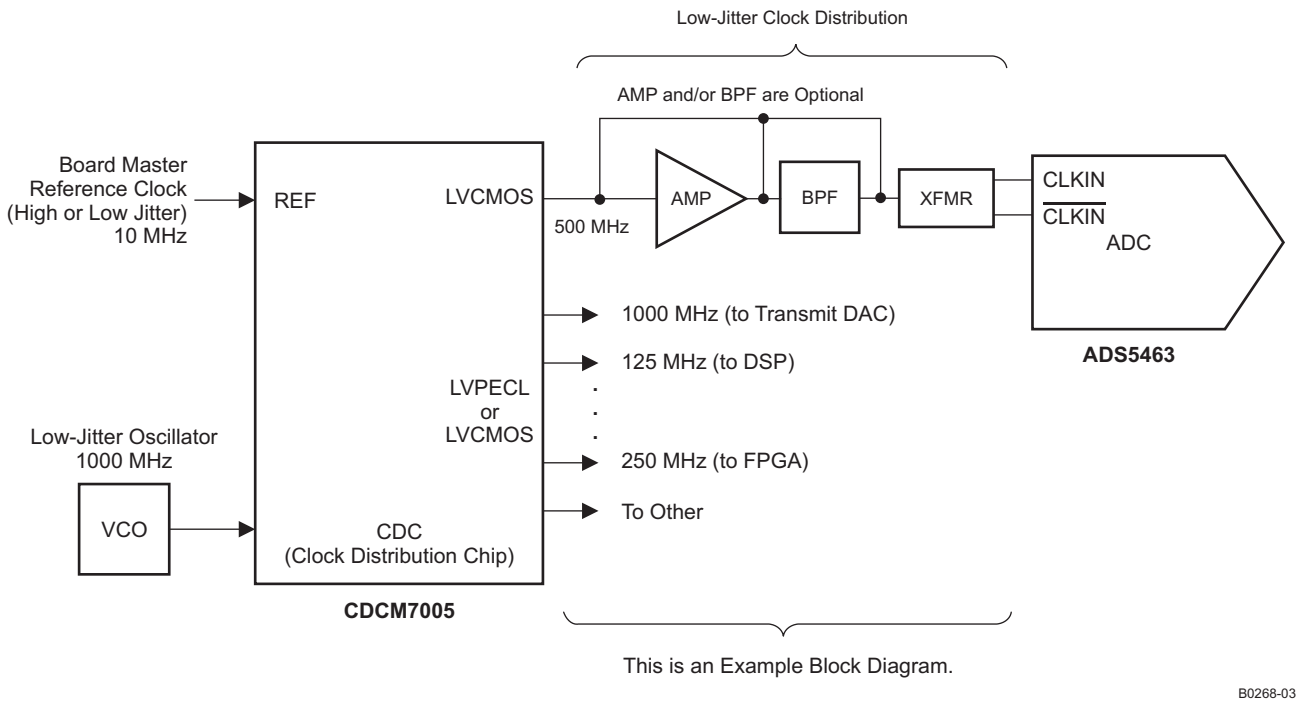
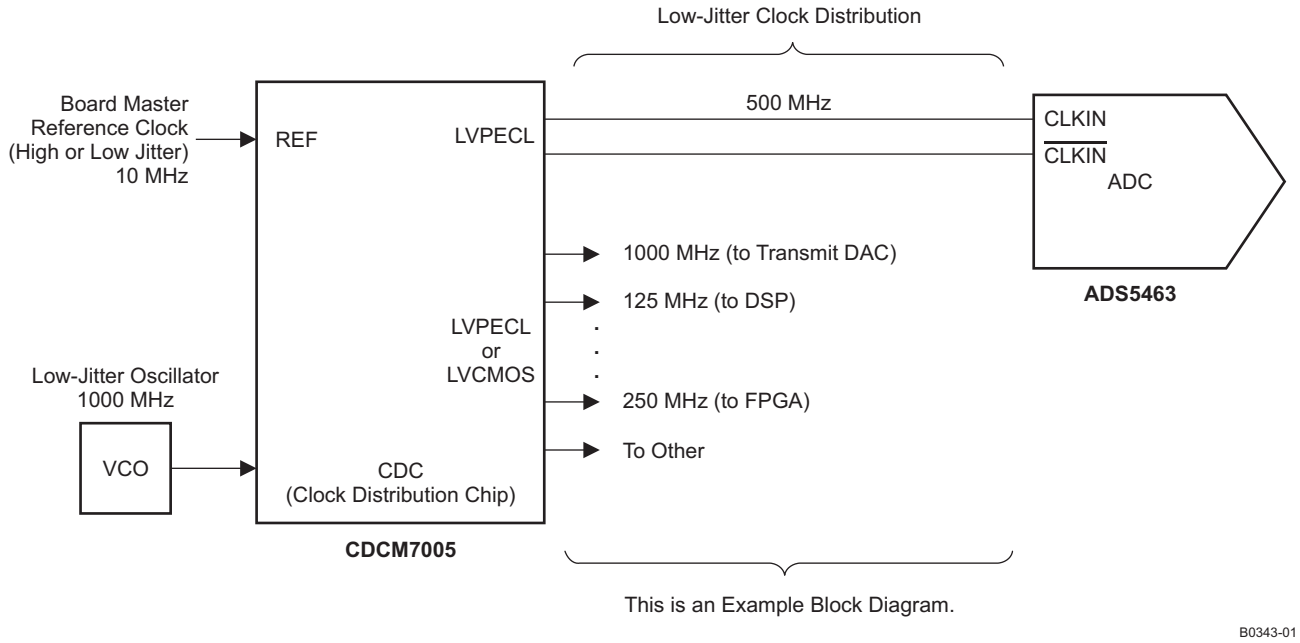


Consult the CDCM7005 data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 65. Optimum Jitter Clock Circuit



Consult the CDCM7005 data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 66. Acceptable Jitter Clock Circuit

Digital Outputs

The ADC provides 12 LVDS-compatible, offset binary data outputs (D11 to D0; D11 is the MSB and D0 is the LSB), a data-ready signal (DRY), and an over-range indicator (OVR). It is recommended to use the DRY signal to capture the output data of the ADS5463/ADS54RF63. DRY is source-synchronous to the DATA/OVR outputs and operates at the same frequency, creating a half-rate DDR interface that updates data on both the rising and falling edges of DRY. It is recommended that the capacitive loading on the digital outputs be minimized. Higher capacitance shortens the data-valid timing window. The values given for timing (see Figure 1) were obtained with a measured 10-pF parasitic board capacitance to ground on each LVDS line (or 5-pF differential parasitic capacitance). When setting the time relationship between DRY and DATA at the receiving device, it is generally recommended that setup time be maximized, but this partially depends on the setup and hold times of the device receiving the digital data (like an FPGA, Field Programmable Gate Array). Since DRY and DATA are coincident, it will likely be necessary to delay either DRY or DATA such that setup time is maximized.

Referencing Figure 1, the polarity of DRY with respect to the sample N data output transition is undetermined because of the unknown startup logic level of the clock divider that generates the DRY signal (DRY is a frequency divide-by-two of CLK). Either the rising or the falling edge of DRY will be coincident with sample N and the polarity of DRY could invert when power is cycled off/on. Data capture from the transition and not the polarity of DRY is recommended, but not required. If the synchronization of multiple ADS5463/ADS54RF63 devices is required, it might be necessary to use a form of the CLKIN signal rather than DRY to capture the data. Studying the timing characteristics, it can be seen that the ADS54RF63 offers more tightly controlled timing parameters than the ADS5463. Depending on the setup/hold requirements of the FPGA in use, it may be possible to use the DRY from a single ADS54RF63 to latch data into the FPGA from multiple ADS54RF63. This would prove much more difficult with the ADS5463 at full clock speed due to more restrictive timing parameters.

The DRY frequency is identical on the ADS5463/ADS54RF63 to the ADS5474 (where DRY equals half of the CLK frequency), but different to the pin-similar ADS5444/ADS5440 (where DRY equals the CLK frequency). The LVDS outputs all require an external 100-Ω load between each output pair in order to meet the expected LVDS voltage levels. For long trace lengths, it may be necessary to place a 100-Ω load on each digital output as close to the ADC as possible and another 100-Ω differential load at the end of the LVDS transmission line to provide matched impedance and avoid signal reflections. The effective load in this case reduces the LVDS voltage levels by half.

The OVR output equals a logic high when the 12-bit output word attempts to exceed either all 0s or all 1s. The digital outputs will clip to all 0s or all 1s if the input is out of range. The OVR signal is provided as an indicator that the analog input signal exceeded the full-scale input limit of approximately 2.2 V_{PP} (± gain error). The OVR indicator is provided for systems that use gain control to keep the analog input signal within acceptable limits.

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Power Supplies

The ADS5463/ADS54RF63 uses three power supplies. For the analog portion of the design, a 5-V and 3.3-V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3-V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies tend to generate more noise components that can be coupled to the ADS5463/ADS54RF63. However, the PSRR value and the plot shown in Figure 67 were obtained without bulk supply decoupling capacitors. When bulk (0.1 µF) decoupling capacitors are used, the board-level PSRR is much higher than the stated value for the ADC. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems. If the noise characteristics of the available supplies are understood, a study of the PSRR data for the ADS5463/ADS54RF63 may provide the user with enough information to select noisy supplies if the performance is still acceptable within the frequency range of interest. The power consumption of the ADS5463/ADS54RF63 does not change substantially over clock rate or input frequency as a result of the architecture and process. The DVDD3 PSRR is superior to both the AVDD5 and AVDD3 so was not graphed.

Because there are two diodes connected in reverse between AVDD3 and DVDD3 internally, a power-up sequence is recommended. When there is a delay in power up between these two supplies, the one that lags could have current sinking through an internal diode before it powers up. The sink current can be large or small depending on the impedance of the external supply and could damage the device or affect the supply source. The best power up sequence is one of the following options (regardless of when AVDD5 powers up):

- Power up both AVDD3 and DVDD3 at the same time (best scenario), OR
- Keep the voltage difference less than 0.8 V between AVDD3 and DVDD3 during the power up (0.8 V is not a hard specification - a smaller delta between supplies is safer).

If the above sequences are not practical then the sink current from the supply needs to be controlled or protection added externally. The max transient current (on the order of µsec) for the DVDD3 or AVDD3 pin is 500 mA to avoid potential damage to the device or reduce its lifetime.

The values for the analog and clock inputs given in the Absolute Maximum Ratings are valid when the supplies are on. When the power supplies are off and the clock or analog inputs are still being actively driven, the input voltage and current need to be limited to avoid device damage. If the ADC supplies are off, max/min continuous dc voltage is ±0.95 V and max dc current is 20 mA for each input pin (clock or analog), relative to ground.

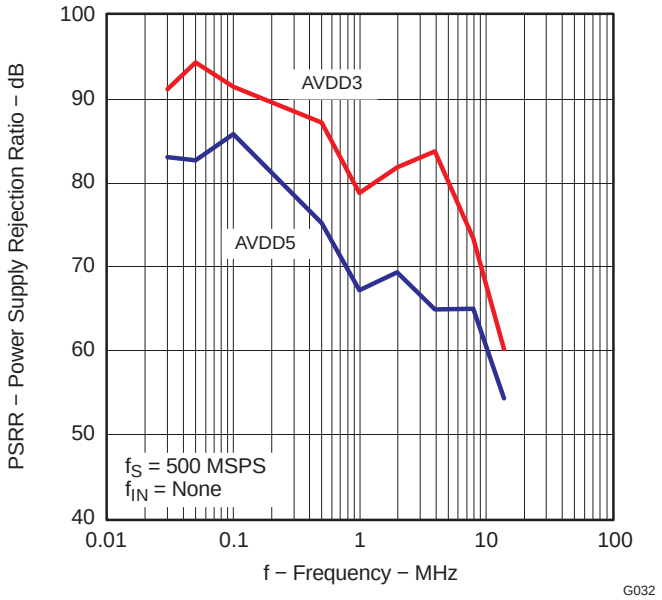

Figure 67. PSRR versus Supply Injected Frequency

Operational Lifetime

It is important for applications that anticipate running continuously for long periods of time near the maximum-rated ambient temperature of +85°C to consider the data shown in Figure 68 and Figure 69. Referring to the Thermal Characteristics table, the worst-case operating condition with no airflow has a thermal rise of 23.7°C/W. At approximately 2.2 W of normal power dissipation, at a maximum ambient of +85°C with no airflow, the junction temperature of the ADS5463 reaches approximately +85°C + 23.7°C/W × 2.2 W = +137°C and therefore the expected lifetime is approximately 8 years due to an electro migration failure and 18 years due to a wirebonding failure. Being even more conservative and accounting for the maximum possible power dissipation that is ensured (2.4 W), the junction temperature becomes nearly +142°C. As Figure 68 and Figure 69 show, this operating condition limits the expected lifetime of the ADS5463 even more. Operation at +85°C continuously may require airflow or an additional heatsink in order to decrease the internal junction temperature and increase the expected lifetime. An airflow of 250 LFM (linear feet per minute) reduces the thermal resistance to 16.4°C/W, the maximum junction temperature to +124°C and the expected lifetime to over 10 years, assuming a worst-case of 2.4 W and +85°C ambient. Of course, operation at lower ambient temperatures greatly increases the expected lifetime.

The ADS5463/ADS54RF63 performance over temperature is quite good and can be seen starting in Figure 19. Although the typical plots show good performance at +100°C, the device is only rated from –40°C to +85°C. For continuous operation at temperatures near or above the maximum, aside from performance degradation, the expected primary negative effect is a shorter device lifetime.

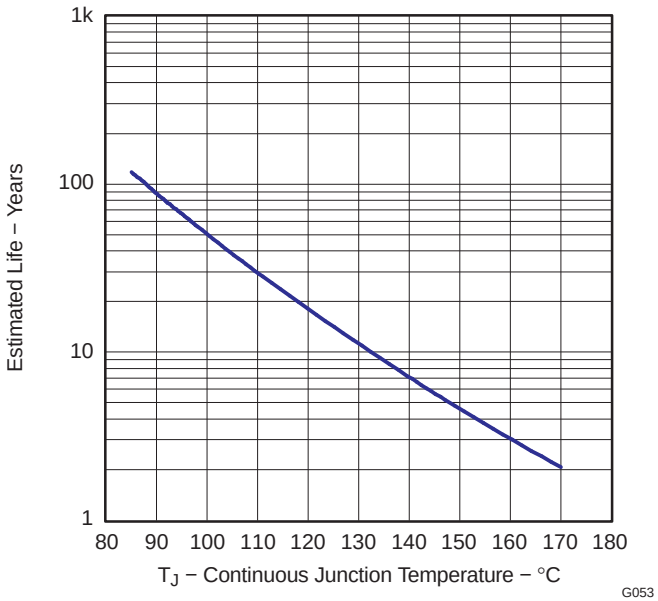

Figure 68. Operating Life Derating Chart, Electro Migration Fail Mode

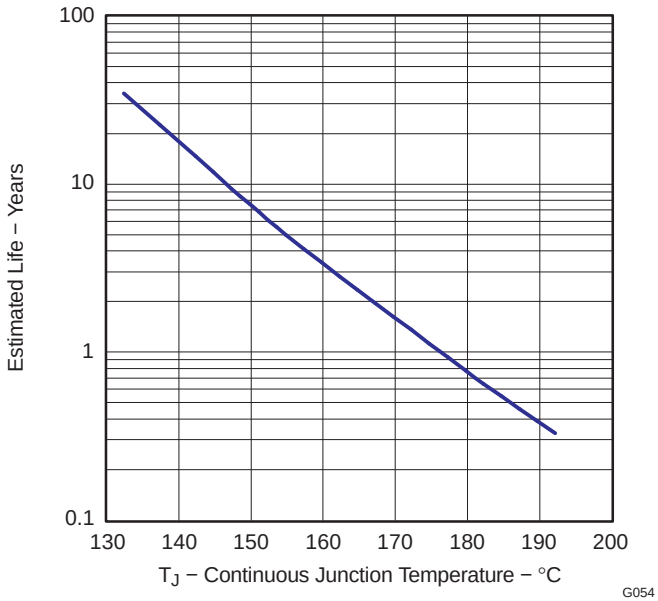

Figure 69. Operating Life Derating Chart, Wirebound Voiding Fail Mode

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Layout Information

The evaluation board represents a good guideline of how to lay out the board to obtain maximum performance from the ADS5463/ADS54RF63. General design rules, such as the use of multilayer boards, single ground plane for ADC ground connections, and local decoupling ceramic chip capacitors, should be applied. The input traces should be isolated from any external source of interference or noise, including the digital outputs as well as the clock traces. The clock signal traces should also be isolated from other signals, especially in applications where low jitter is required like high IF sampling. Besides performance-oriented rules, care must be taken when considering the heat dissipation of the device. The thermal heat sink should be soldered to the board as described in the *PowerPAD Package* section. See *ADS5463 EVM User Guide* (SLAU194) on the TI web site for the evaluation board schematic.

PowerPAD Package

The PowerPAD package is a thermally enhanced standard-size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink.

Assembly Process

1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the Mechanical Data section.
2. Place a 6-by-6 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25-mil-diameter holes under the package, but outside the thermal pad area, to provide an additional heat path.
4. Connect all holes (both inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via-connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the *PowerPAD Made Easy* application brief (SLMA004) or the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

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DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value

Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay

Clock Pulse Duration/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal, expressed as a percentage.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Common-Mode Rejection Ratio (CMRR)

CMRR measures the ability to reject signals that are presented to both analog inputs simultaneously. The injected common-mode frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the CMRR in dB.

Effective Number of Bits (ENOB)

ENOB is a measure in units of bits of a converter's performance as compared to the theoretical limit based on quantization noise

ENOB = (SINAD – 1.76)/6.02

Gain Error

Gain error is the deviation of the ADC actual input full-scale range from its ideal value, given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL)

INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of the ability to reject frequencies present on the power supply. The injected frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the PSRR in dB. The measurement calibrates out the benefit of the board supply decoupling capacitors.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$SNR = 10\log_{10}\frac{P_S}{P_N} \tag{4}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10}\frac{P_S}{P_N + P_D} \tag{5}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Temperature Drift

Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10}\frac{P_S}{P_D} \tag{6}$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3)

IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is given in units of either dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

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REVISION HISTORY

Changes from Revision D (FEBRUARY 2009) to Revision E **Page**

- Added AC to High Analog Input Swing feature description 1
- Changed clock and analog inputs and data outputs in ABSOLUTE MAXIMUM RATINGS table 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5463IPFP	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5463I
ADS5463IPFPG4	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5463I
ADS5463IPFPR	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS5463I
ADS54RF63IPFP	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS54RF63I
ADS54RF63IPFPG4	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS54RF63I
ADS54RF63IPFPR	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 85	ADS54RF63I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ADS5463 :

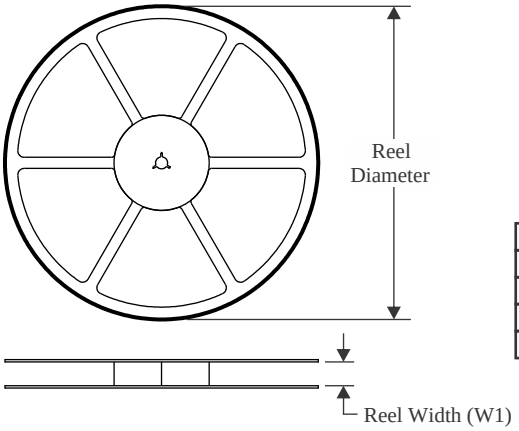
- Enhanced Product : ADS5463-EP
- Space : ADS5463-SP

NOTE: Qualified Version Definitions:

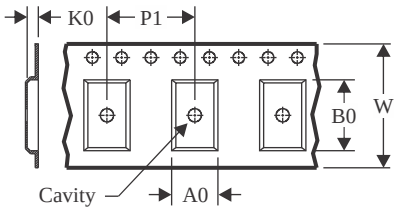
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

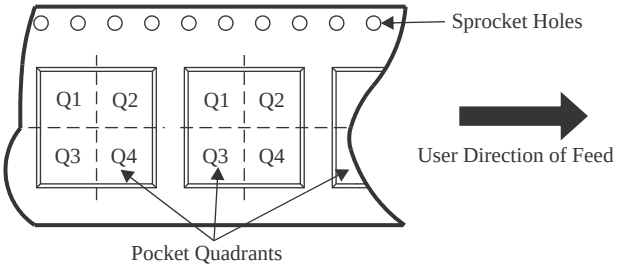


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

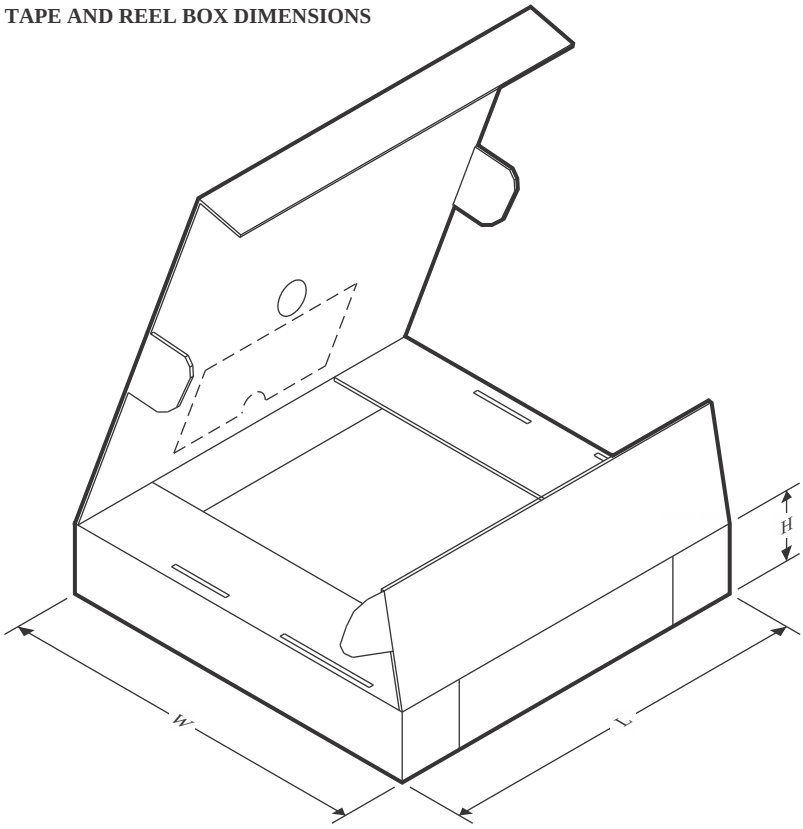
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5463IPFPR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
ADS54RF63IPFPR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

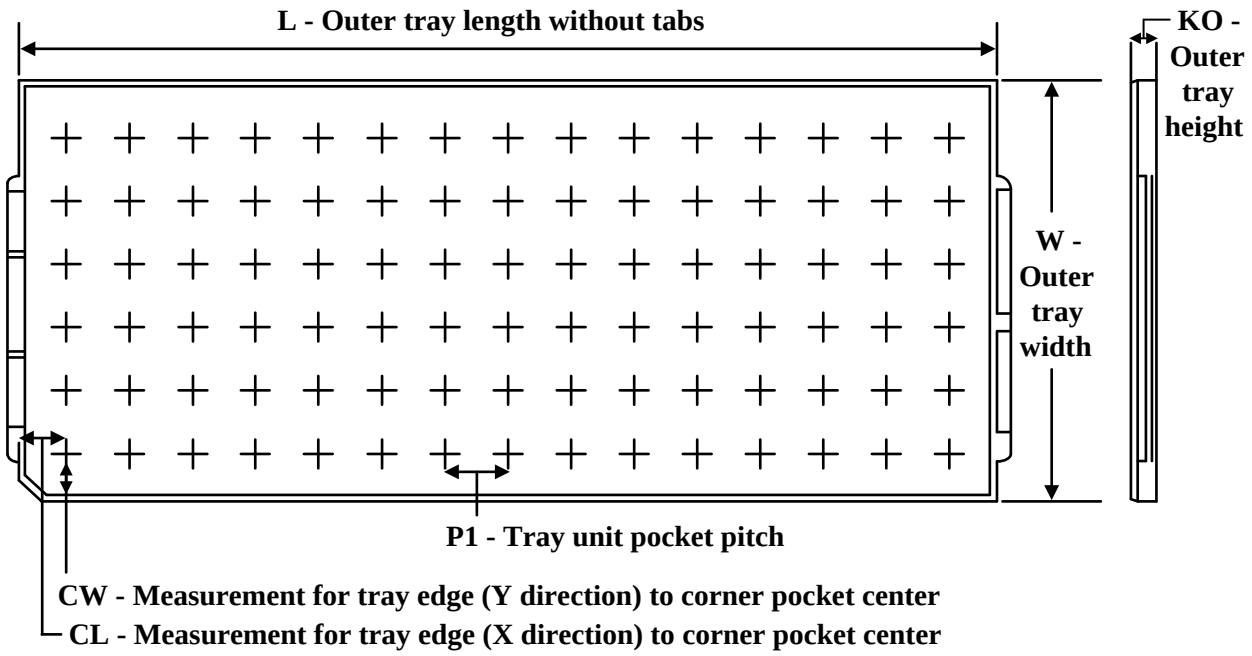
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5463IPFPR	HTQFP	PFP	80	1000	350.0	350.0	43.0
ADS54RF63IPFPR	HTQFP	PFP	80	1000	350.0	350.0	43.0

TRAY

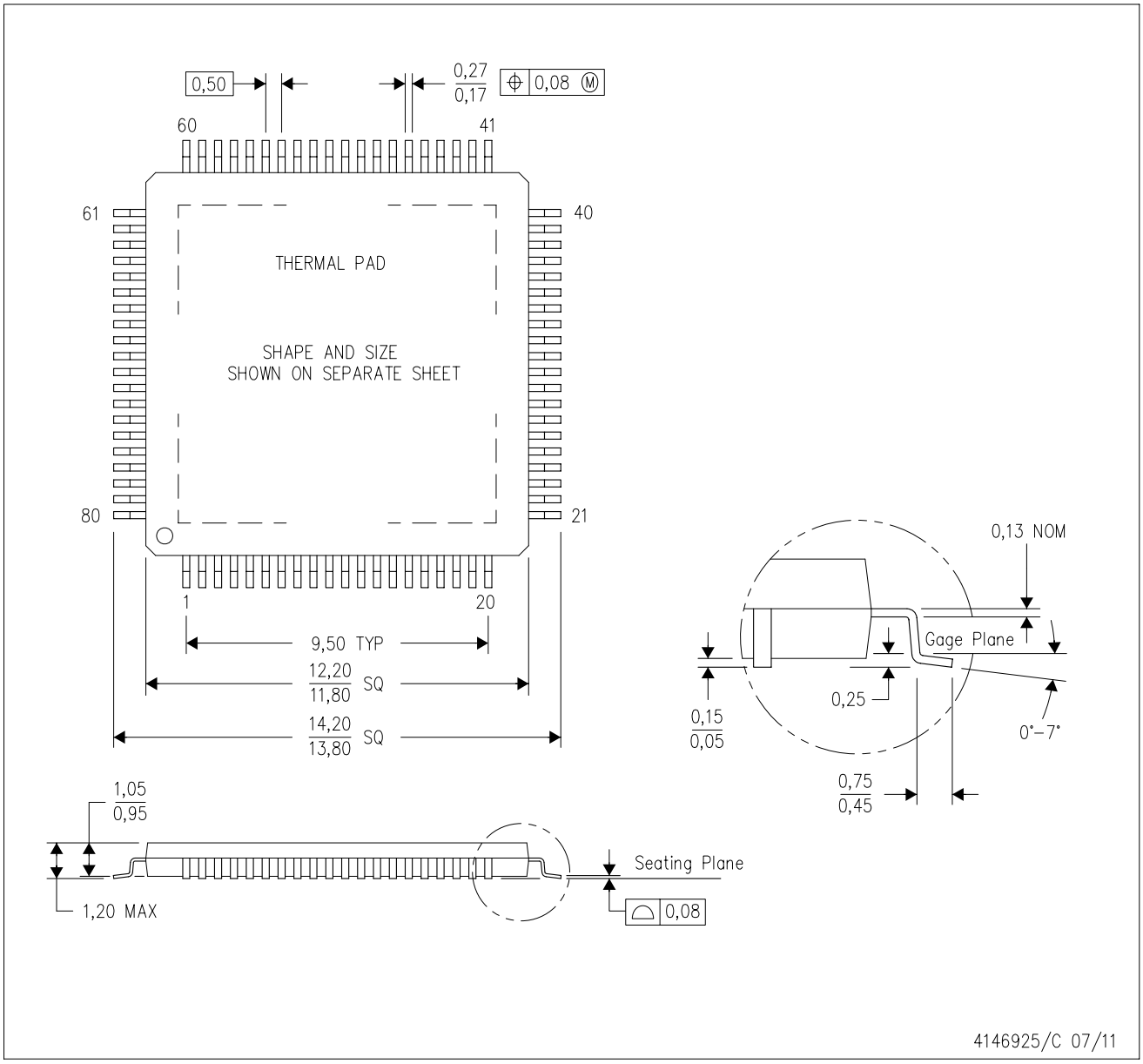


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5463IPFP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
ADS54RF63IPFP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS-026

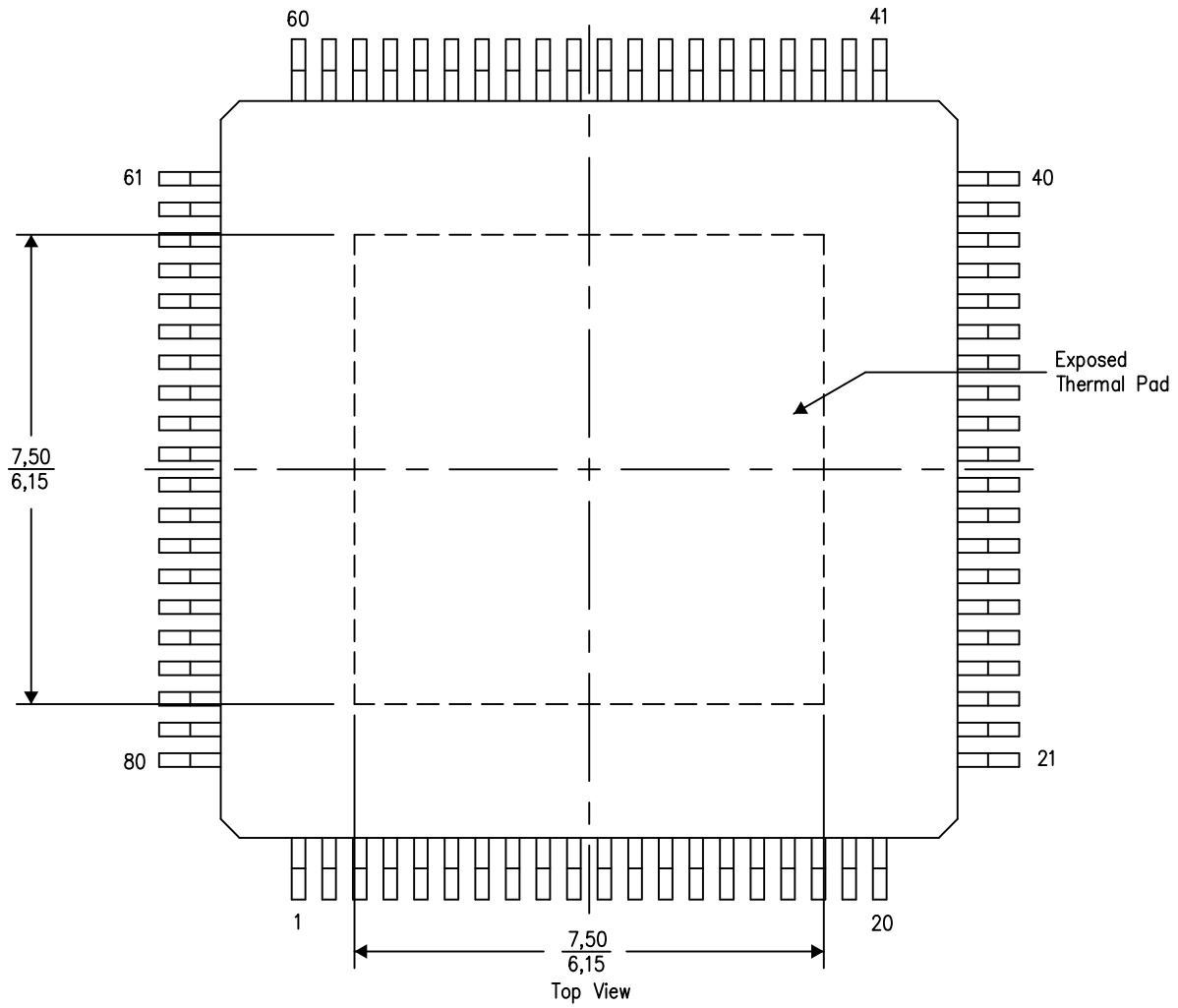
PowerPAD is a trademark of Texas Instruments.

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).
For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



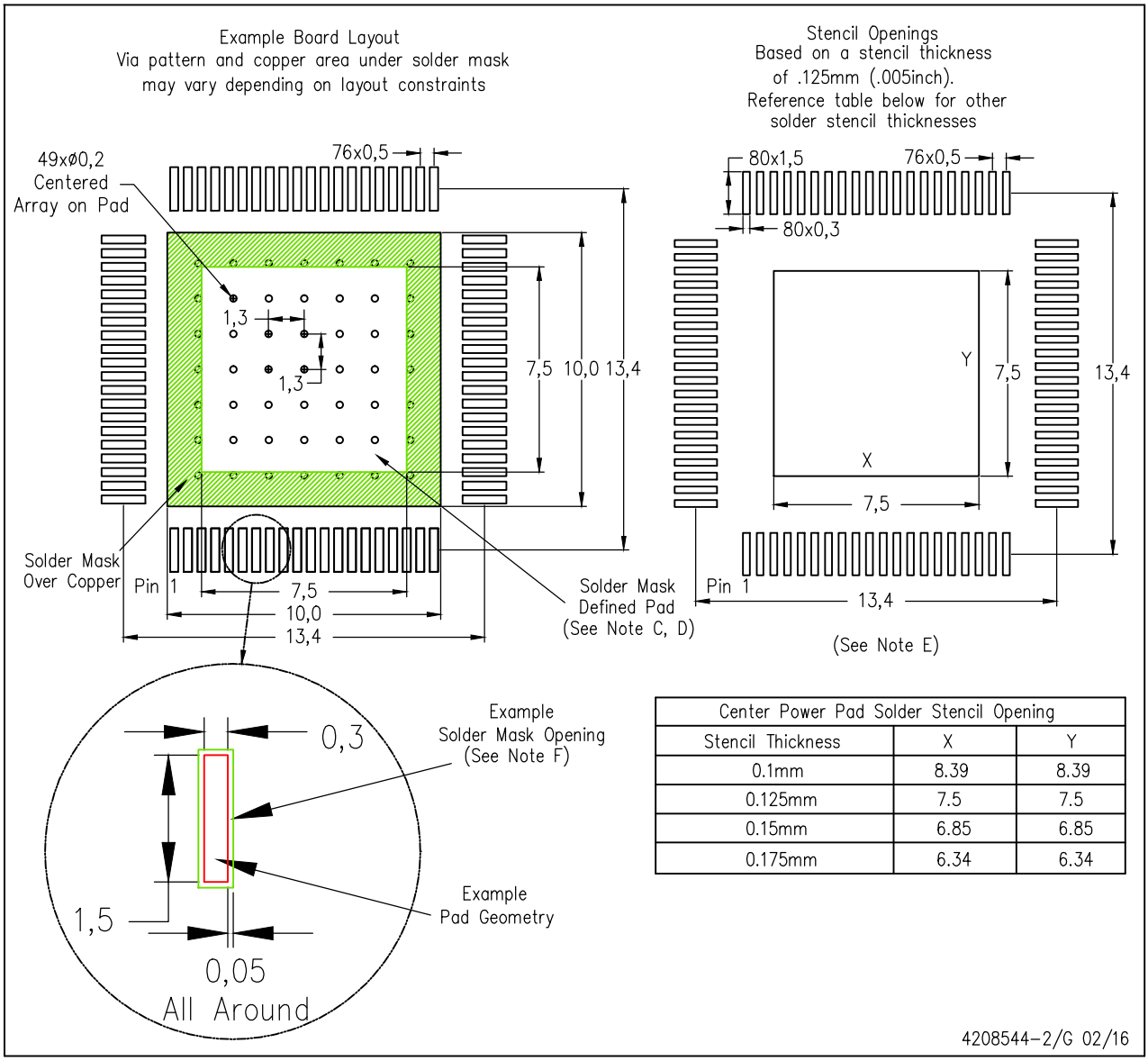
Exposed Thermal Pad Dimensions

4206327-2/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.39	8.39
0.125mm	7.5	7.5
0.15mm	6.85	6.85
0.175mm	6.34	6.34

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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