

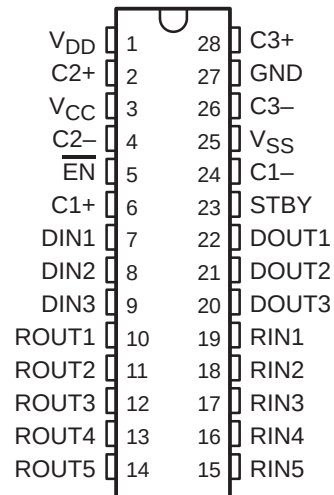
SN75LV4737A

3.3-V/5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

SLLS178D – APRIL 1994 – REVISED FEBRUARY 2000

- Single-Chip and Single-Supply Interface for IBM PC/AT™ Serial Port
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.11 Standards
- Operates With 3.3-V or 5-V Supplies
- One Receiver Remains Active During Standby (Wake-up Mode)
- Designed to Operate at 128 kbit/s Over a 3-m Cable
- Low Standby Current . . . 5 μ A Max
- ESD Protection on RS-232 Pins Meets or Exceeds 4 kV (HBM) and 1.5 kV (HBM) on All Pins Per MIL-STD-883, Method 3015
- External Capacitors . . . 0.1 μ F ($V_{CC} = 3.3$ V . . . Five External Capacitors) ($V_{CC} = 5$ V . . . Four External Capacitors)
- Accepts 5-V Logic Input With 3.3-V Supply
- Applications
 - RS-232 Interface
 - Battery-Powered Systems, PDAs
 - Notebook, Laptop, and Palmtop PCs
 - External Modems and Hand-Held Terminals
- Packaged in Shrink Small-Outline Package

DB PACKAGE†
(TOP VIEW)



† The DB package is only available in left-ended tape and reel (order part number SN75LV4737ADBR).

description

The SN75LV4737A[‡] consists of three line drivers, five line receivers, and a charge-pump circuit. It provides the electrical interface between an asynchronous communication controller and the serial-port connector, and meets the requirements of TIA/EIA-232-F. This combination of drivers and receivers matches those needed for the typical serial port used in an IBM PC/AT or compatibles. The charge pump and five small external capacitors allow operation from a single 3.3-V supply, and four capacitors allow operation from a 5-V supply.

The device has flexible control options for power management when the serial port is inactive. A common disable for all of the drivers and receivers is provided with the active-high STBY input. The active-low $\overline{EN}$ input is an enable for one receiver to implement a wake-up feature for the serial port. All the logic inputs can accept signals from controllers operating from a 5-V supply, even though the SN75LV4737A is operating from 3.3 V.

The SN75LV4737A is characterized for operation over the temperature range of 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[‡] Patent-pending design

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Function Tables

EACH DRIVER

INPUTS		OUTPUT
DIN	STBY	DOUT
X	H	Z
L	L	H
H	L	L
Open	L	L

H = high level, L = low level,
X = irrelevant, Z = high
impedance

EACH RECEIVER

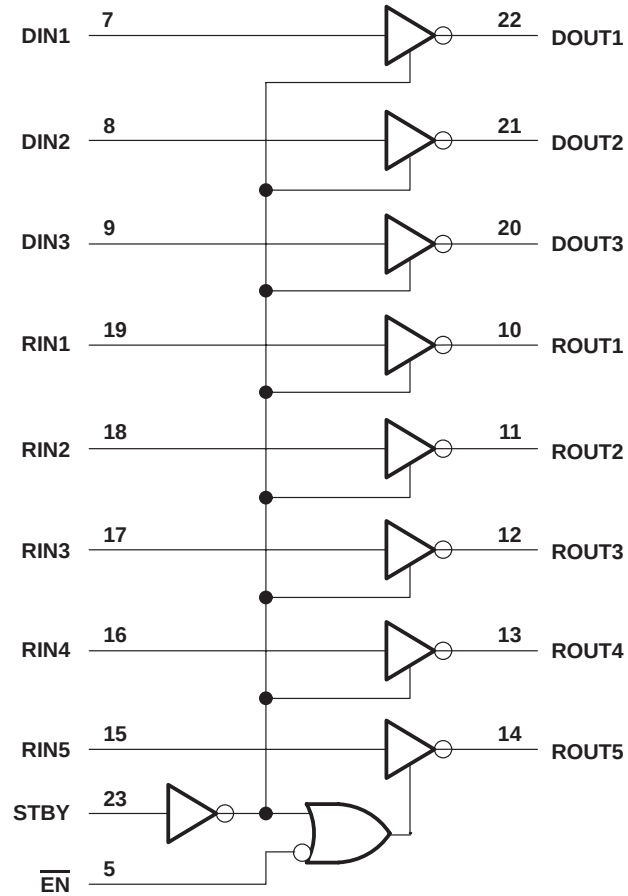
INPUTS				OUTPUTS	
STBY	$\overline{\text{EN}}$	RIN5	RIN1–RIN4	ROUT5	ROUT1–ROUT4
H	H	X	X	Z	Z
H	L	H	X	L	Z
H	L	L	X	H	Z
L	X	L	L	H	H
L	X	H	H	L	L

H = high level, L = low level, X = irrelevant, Z = high impedance

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logic diagram (positive logic)

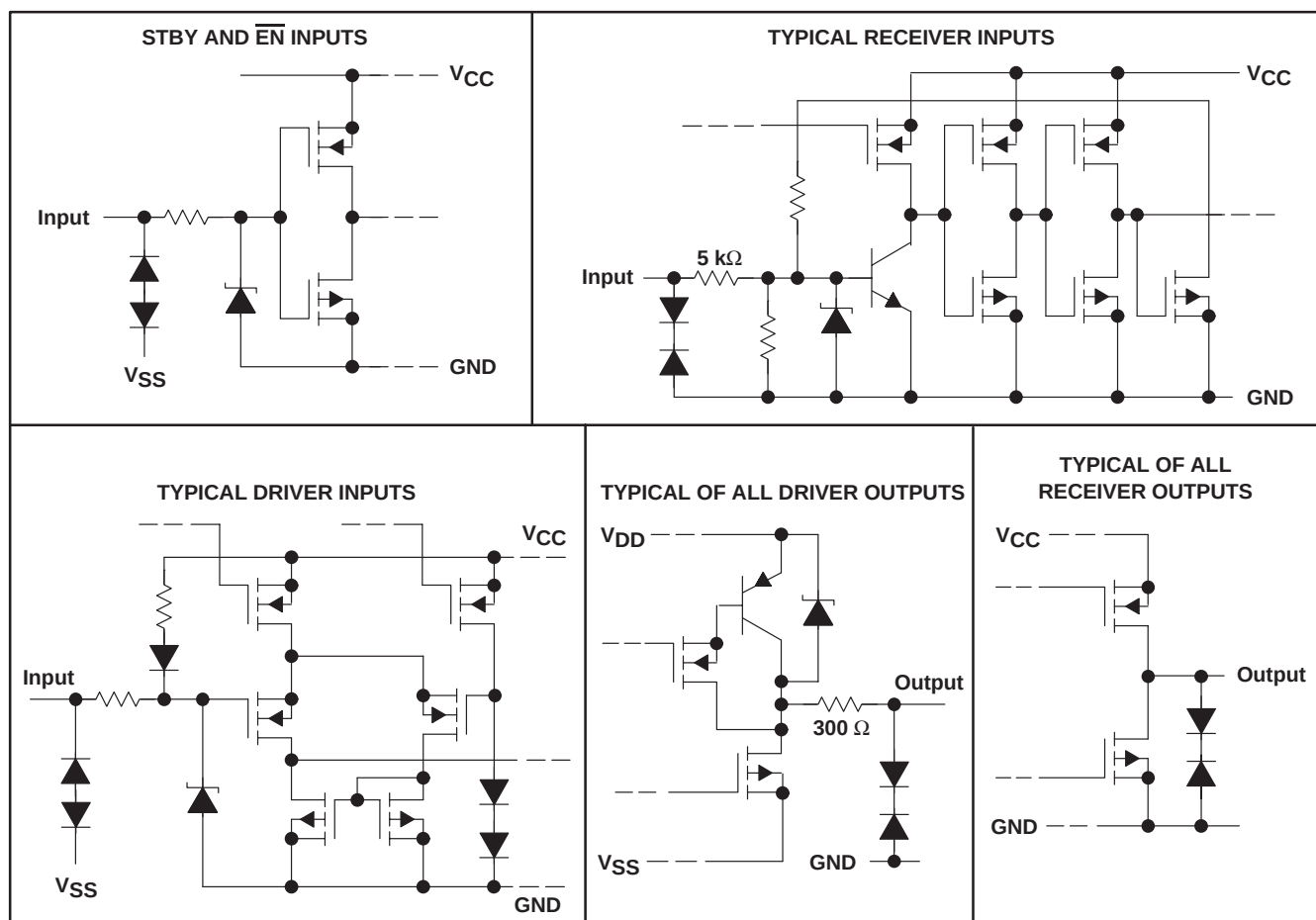


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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Positive output supply voltage, V_{DD} (see Note 1)	15 V
Negative output supply voltage, V_{SS}	-15 V
Input voltage range, V_I : Driver	-3 V to 7 V
Receiver	-30 V to 30 V
Output voltage range, V_O : Driver	$V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V
Receiver	-0.3 V to 7 V
Package thermal impedance, θ_{JA} (see Note 2)	62°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to network GND.
2. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	V
V _{IH}	Driver high-level input voltage	DIN, $\overline{\text{EN}}$, STBY	V _{CC} = 3.3 V			V
		DIN	2			
		$\overline{\text{EN}}$, STBY	V _{CC} = 5 V			
V _{IL}	Driver low-level input voltage	DIN, $\overline{\text{EN}}$, STBY			0.8	V
V _I	Receiver input voltage		±30			V
	External capacitor	3.3-V operation (C1, C2, C3, C4, C5), 5-V operation (C1, C3, C4, C5), See Note 3 and Figures 6 and 7			0.1	μF
T _A	Operating free-air temperature		0			70 °C

NOTE 3: C2 is needed only for 3.3-V operation.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 6 and 7) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC} = 3.3 V			V _{CC} = 5 V			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{DD}	Positive supply voltage	No load	8	10		7	8.7		V
V _{SS}	Negative supply voltage	No load		–9.5	–7		–8	–6	V
I _I	Input current ($\overline{\text{EN}}$, STBY)	See Notes 4 and 5			±2			±2	μA
I _{CC}	Supply current	No load, Inputs open	STBY at GND, $\overline{\text{EN}}$ at V _{CC} or GND			8.4	10	18	mA
	Supply current (standby mode) (see Note 4)		$\overline{\text{EN}}$, STBY at V _{CC}					5	μA
	Supply current (wake-up mode) (see Note 5)		$\overline{\text{EN}}$ at GND, STBY at V _{CC}					10	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTES: 4. When standby mode is not used, STBY input must be taken low.
5. When wake-up mode is not used, $\overline{\text{EN}}$ input must be taken high.



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3.3-V/5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{OH} High-level output voltage	R _L = 3 k Ω	5.5	7		V
V _{OL} Low-level output voltage	R _L = 3 k Ω		–6	–5	V
I _{IH} High-level input current	V _I = V _{CC}			1	μ A
I _{IL} Low-level input current	V _I at GND			–10	μ A
I _{OS} Short-circuit output current (see Note 6)	V _{CC} = 3.6 V, V _O = 0 V		$\pm$ 15	$\pm$ 40	mA
	V _{CC} = 5.5 V, V _O = 0 V				
r _o Output resistance	V _{CC} = V _{DD} = V _{SS} = 0 V, V _O = $\pm$ 2 V	300	500		Ω

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 6: Short-circuit durations should be controlled to prevent exceeding the device absolute maximum power dissipation ratings, and not more than one output should be shorted at a time.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 50 pF, R _L = 3 kΩ to 7 kΩ, See Figure 1	V _{CC} = 3.3 V	100	500	850	ns
			V _{CC} = 5 V	100	500	850	
t _{PHL}	Propagation delay time, high- to low-level output		V _{CC} = 3.3 V	100	500	850	ns
			V _{CC} = 5 V	100	500	850	
t _{PZH}	Output enable time to high level	C _L = 50 pF, See Figure 2	R _L = 3 kΩ to 7 kΩ,		1	5	ms
t _{PZL}	Output enable time to low level				3	7	ms
t _{PHZ}	Output disable time from high level	C _L = 50 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2	V _{CC} = 3.3 V		0.9	3	μs
			V _{CC} = 5 V		0.6	3	
t _{PLZ}	Output disable time from low level		V _{CC} = 3.3 V		0.5	3	μs
			V _{CC} = 5 V		0.3	3	
SR	Slew rate	C _L = 50 pF, See Figure 1	R _L = 3 kΩ to 7 kΩ,	4		30	V/μs
SR(tr)	Slew rate, transition region	C _L = 2500 pF, See Figure 3	R _L = 3 kΩ to 7 kΩ,	3		30	V/μs

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.



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RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = –2 mA	V _{CC} = 3.3 V	2.4	3	V
		V _{CC} = 5 V	3.5	5	
V _{OL} Low-level output voltage	I _{OL} = 2 mA		0.2	0.4	V
V _{IT+} Positive-going input threshold voltage			2.2	2.6	V
V _{IT–} Negative-going input threshold voltage			0.6	1	V
V _{hys} Input hysteresis (V _{IT+} – V _{IT–})			0.5	1.2	1.8
r _i Input resistance	V _I = ±3 V to ±25 V		3	5	7
					kΩ

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF, R_L = 3 kΩ to GND

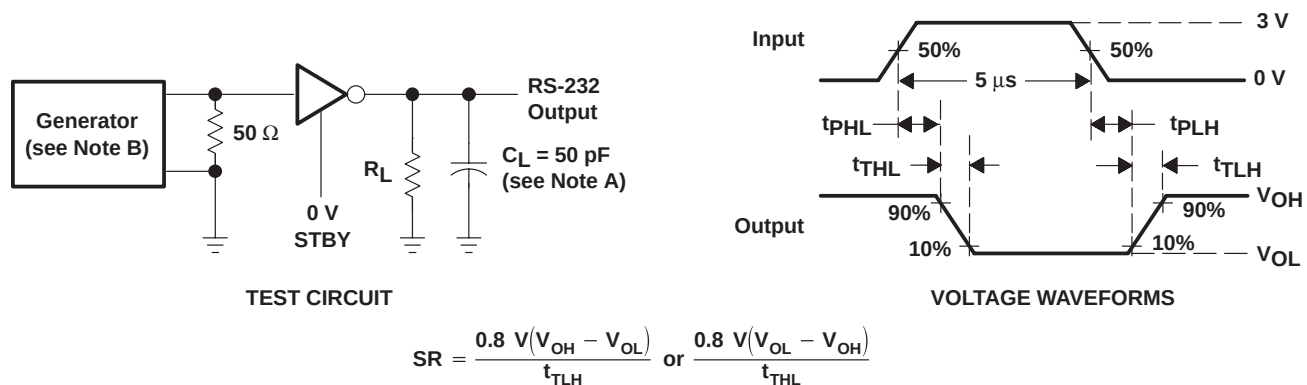
PARAMETER	TEST CONDITIONS	V _{CC} = 3.3 V			V _{CC} = 5 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} Propagation delay time, low- to high-level output	See Figure 4	10	70	200	10	70	200	ns
t _{PHL} Propagation delay time, high- to low-level output		10	60	200	10	55	200	ns
t _{PLH} Propagation delay time, low- to high-level output (wake-up mode)			40	200		40	200	μs
t _{PHL} Propagation delay time, high- to low-level output (wake-up mode)			90	500		70	500	ns
t _{pZH} Output enable time to high level	See Figure 5		3	10		1.2	10	μs
t _{pZL} Output enable time to low level			100	250		60	250	ns
t _{PHZ} Output disable time from high level		100	200	600	100	150	600	ns
t _{PLZ} Output disable time from low level			130	250		60	250	ns

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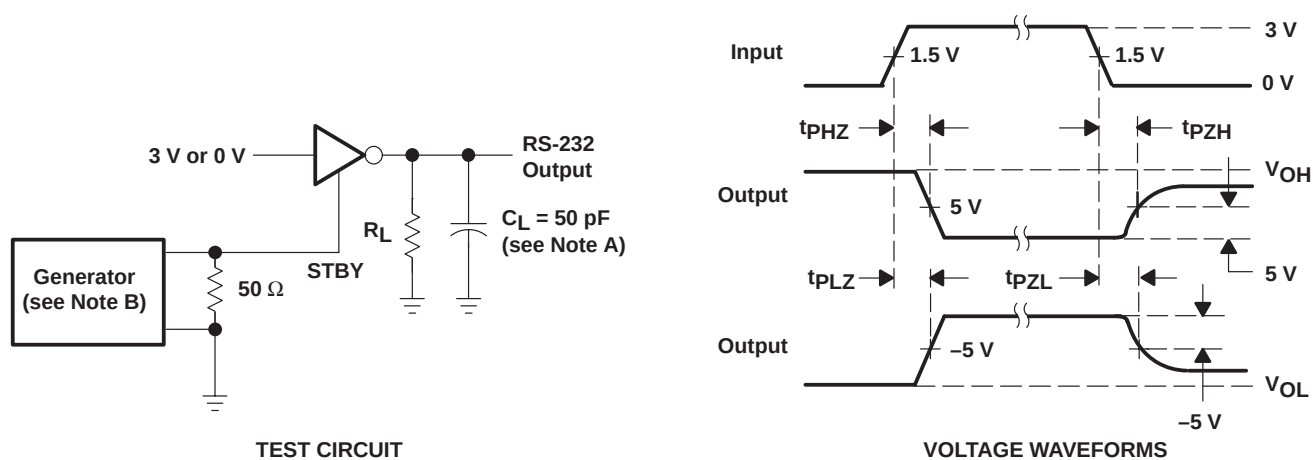
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

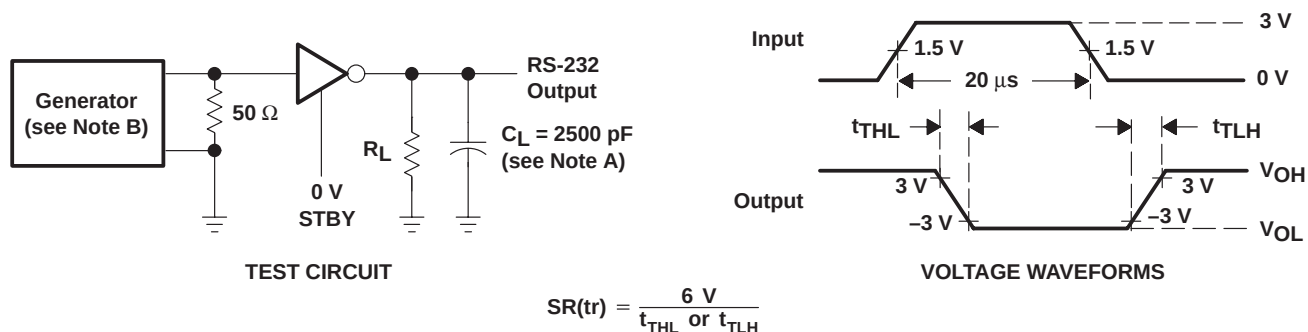
Figure 1. Driver Propagation Delay Times and Slew Rate (5-μs Input)



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

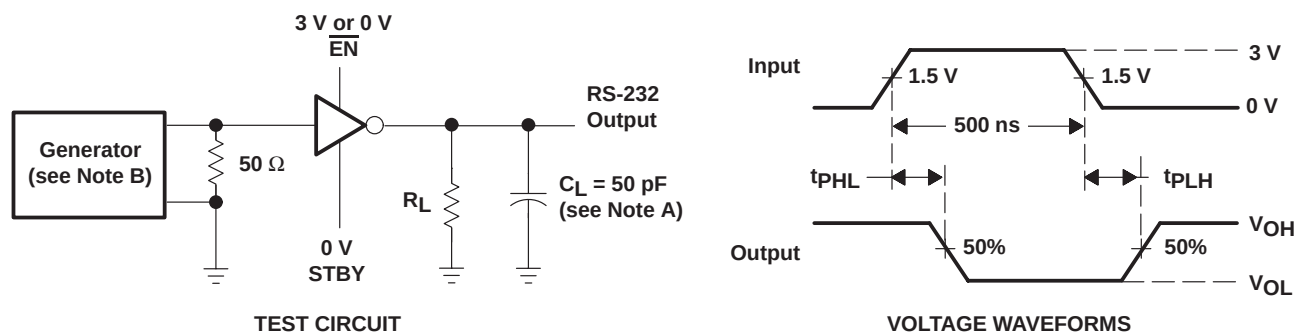
Figure 2. Driver Enable and Disable Test Times

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

Figure 3. Driver Transition Times and Slew Rate (20- μ s Input)



NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

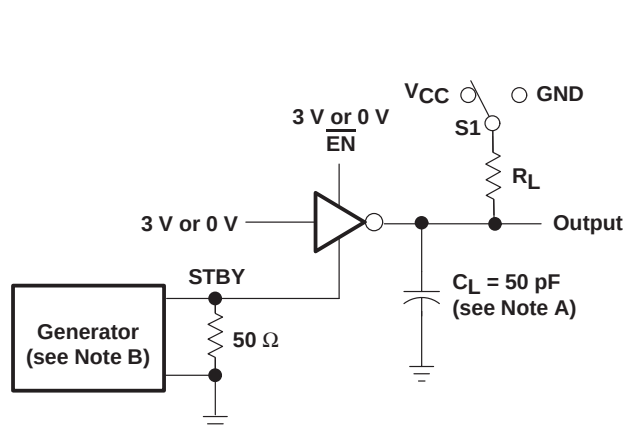
Figure 4. Receiver Propagation Delay Times

SN75LV4737A

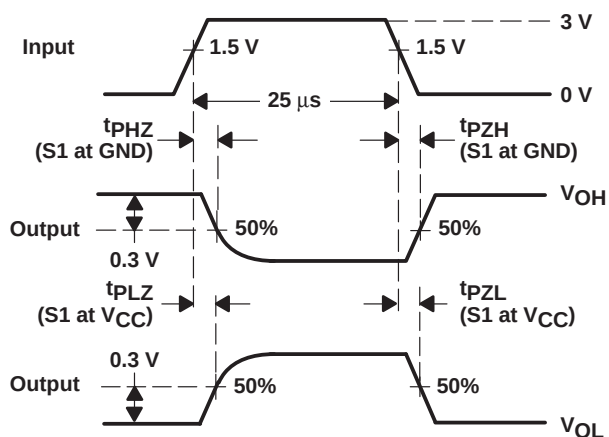
3.3-V/5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. Receiver Enable and Disable Times

Pin Configuration Diagram for RS-232C to TTL Converter

Power and Mode-Control Pins:

- 1: V_{DD}
- 2: C2+
- 3: V_{CC}
- 4: C2-
- 5: EN
- 6: C1+
- 7: V_{CC}
- 23: STBY
- 24: C1-
- 25: V_{SS}
- 26: C3-
- 27: GND
- 28: C3+

Mode-Control Logic: A box labeled "Mode-Control Logic" is connected to pins 1, 2, 3, 4, 5, and 6. Another box labeled "Mode-Control Logic" is connected to pins 23 and 24.

RS-232C Signals:

- Inputs (RIN):** RIN1 (15), RIN2 (16), RIN3 (17), RIN4 (18), RIN5 (19)
- Outputs (DOUT):** DOUT1 (22), DOUT2 (21), DOUT3 (20)

TTL Signals:

- Inputs (DIN):** DIN1 (7), DIN2 (8), DIN3 (9)
- Outputs (ROUT):** ROUT1 (10), ROUT2 (11), ROUT3 (12), ROUT4 (13), ROUT5 (14)

Internal Circuitry: The diagram shows internal buffers and pull-up/pull-down resistors for various signals. For example, DIN1-3 have pull-up resistors to V_{CC}, and ROUT1-5 have pull-down resistors to ground.

Notes:

- Note A:** See Note A (refers to pins 27 and 28).
- Note B:** See Note B (refers to the CBYPASS capacitor connection).

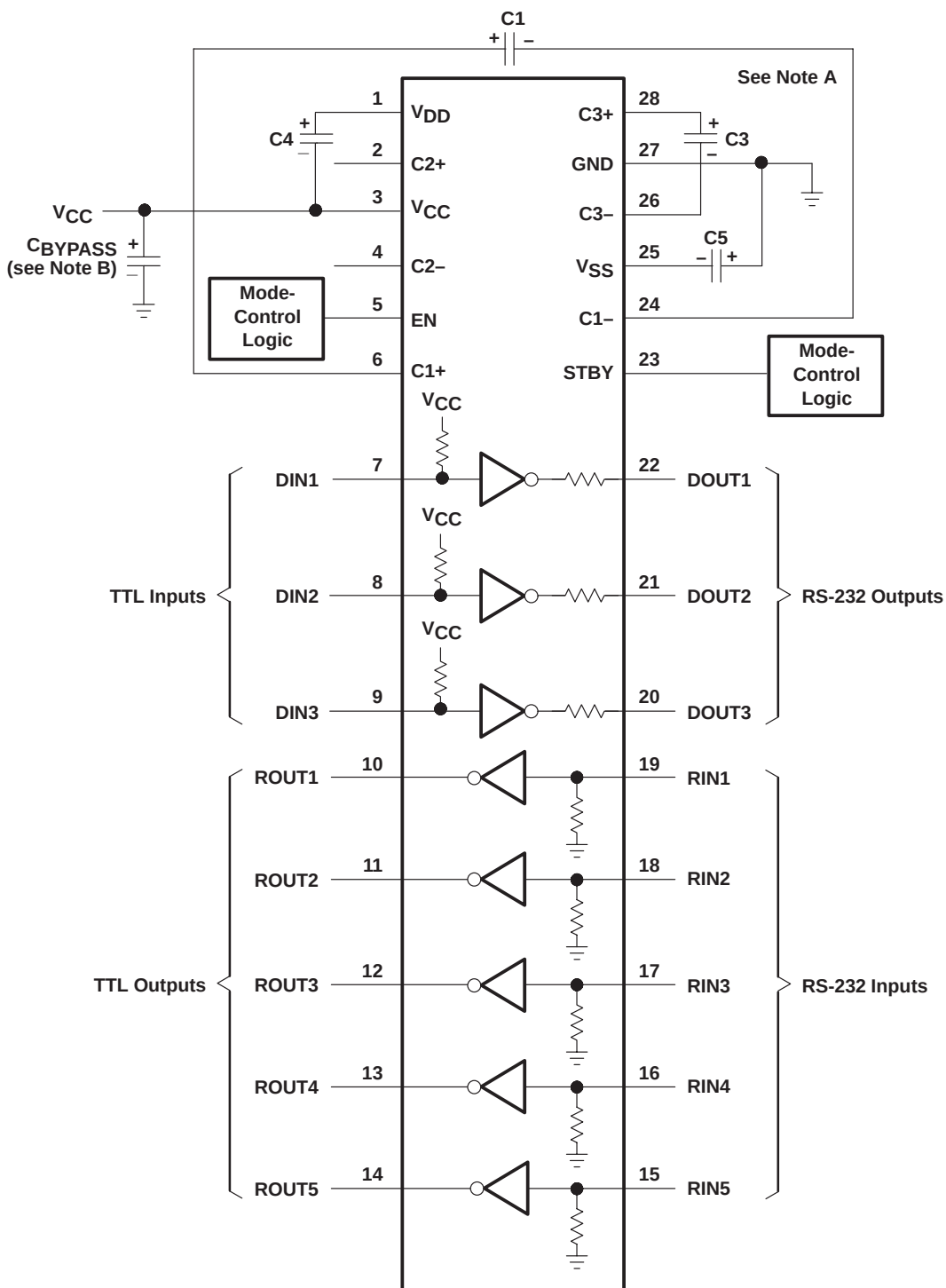
Figure 6. Typical 3.3-V Operating Circuit

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3.3-V/5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

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APPLICATION INFORMATION



NOTES: A. C2 is not used. C1 = C3 = C4 = C5 = CBYPASS = 0.1 μF
B. CBYPASS is used as a decoupling capacitor.

Figure 7. Typical 5-V Operating Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LV4737ADB	Active	Production	SSOP (DB) 28	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A
SN75LV4737ADB.A	Active	Production	SSOP (DB) 28	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A
SN75LV4737ADBR	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A
SN75LV4737ADBR.A	Active	Production	SSOP (DB) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

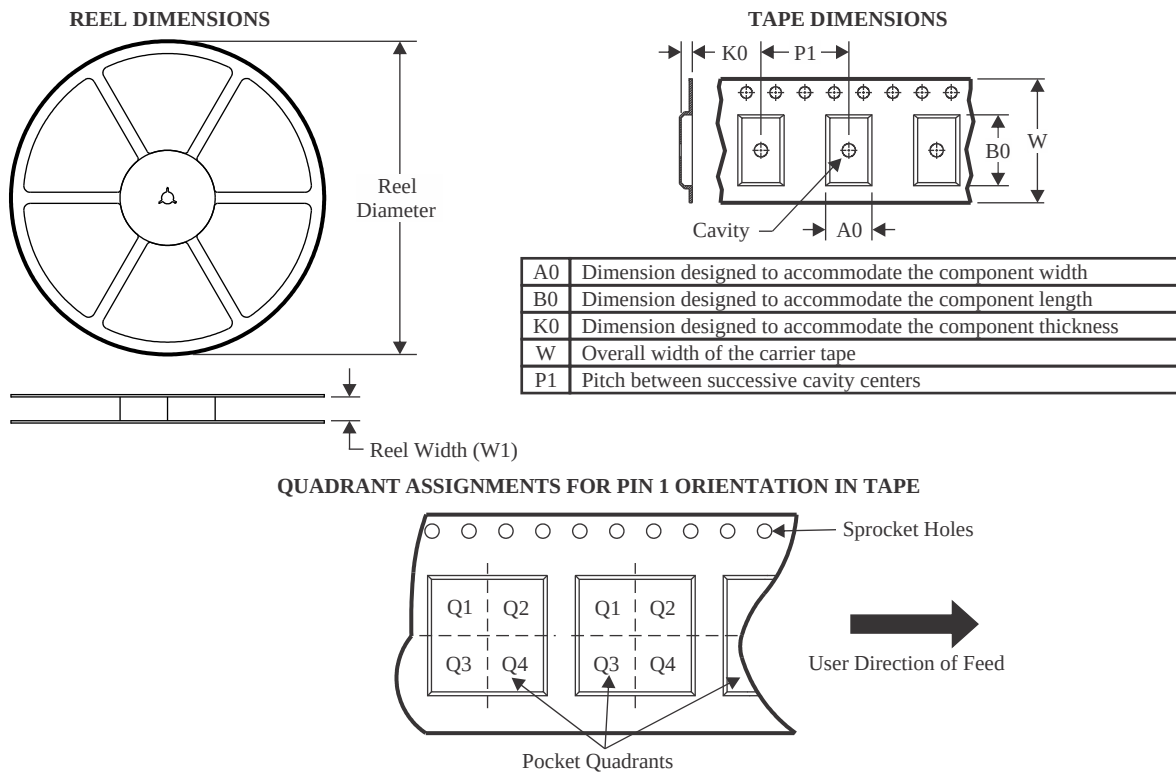
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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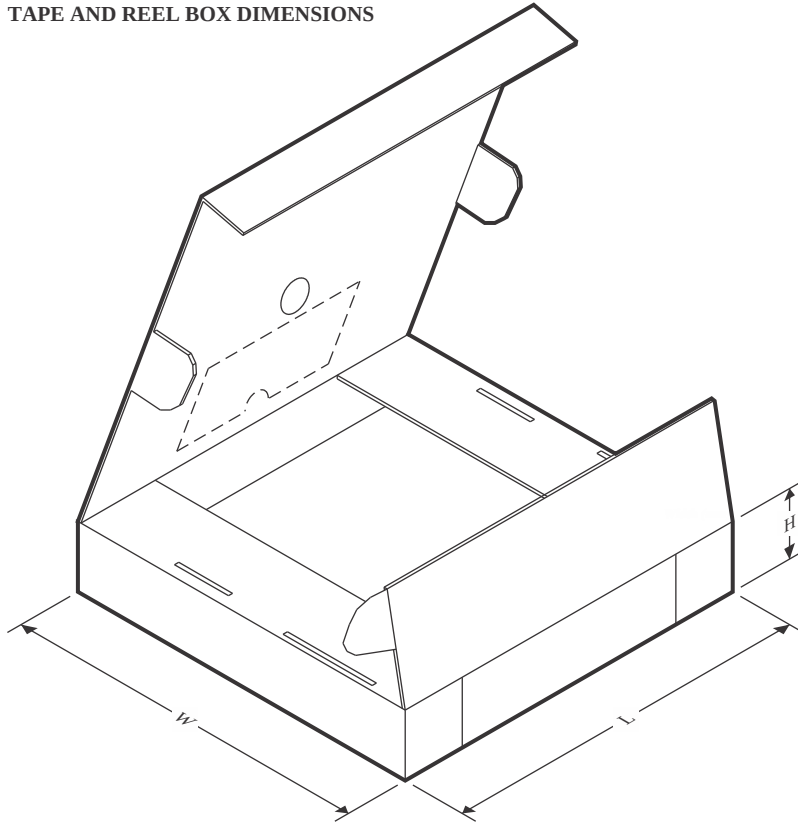
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LV4737ADBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

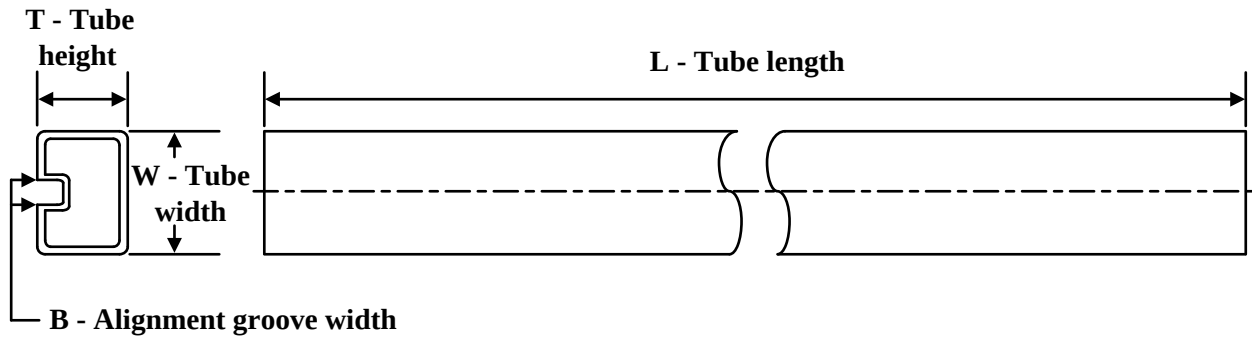
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

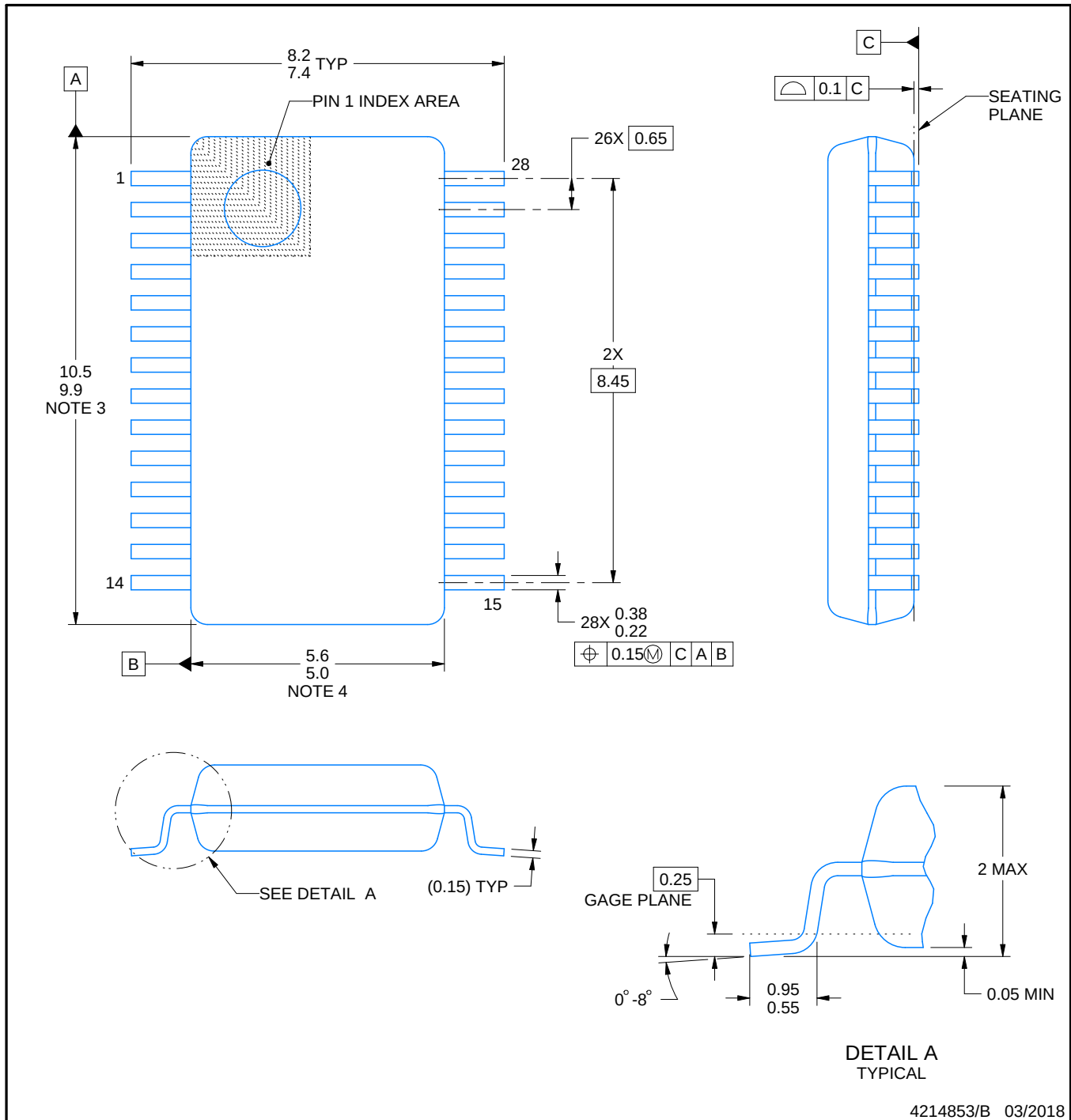
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LV4737ADBR	SSOP	DB	28	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75LV4737ADB	DB	SSOP	28	50	530	10.5	4000	4.1
SN75LV4737ADB.A	DB	SSOP	28	50	530	10.5	4000	4.1



4214853/B 03/2018

NOTES:

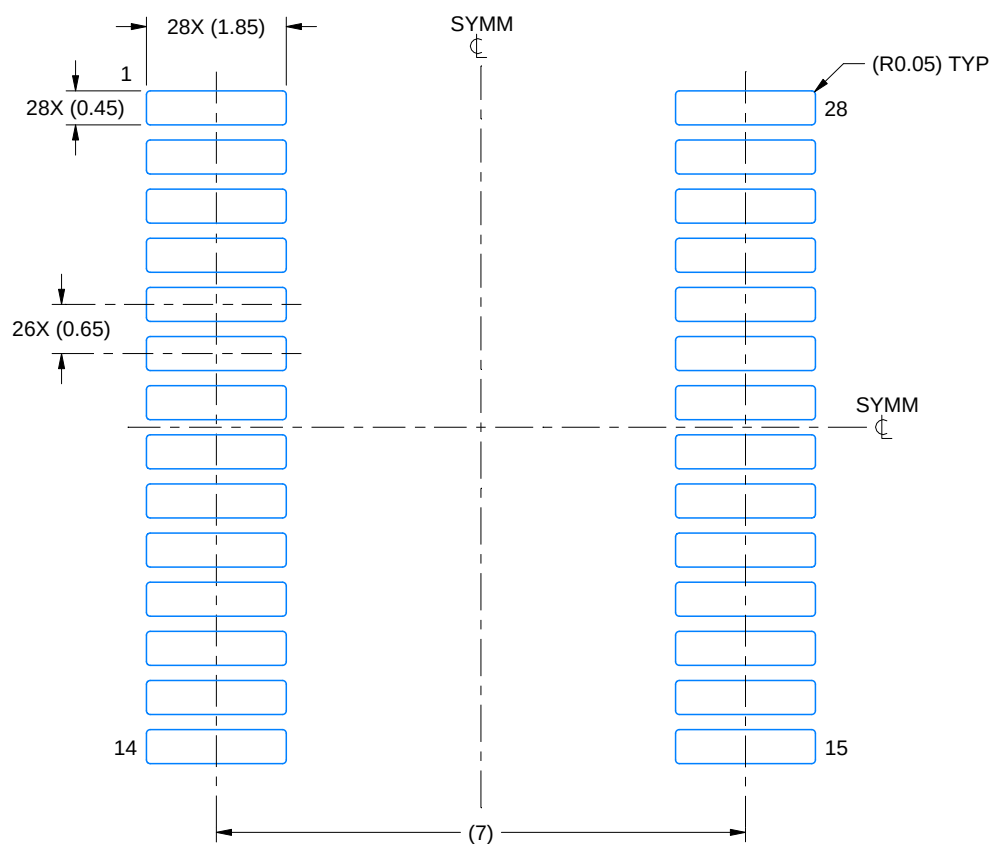
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

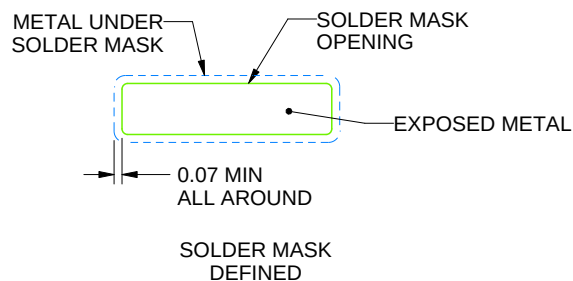
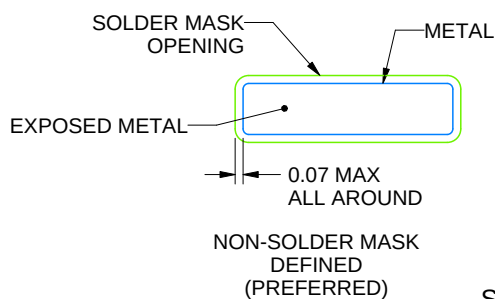
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

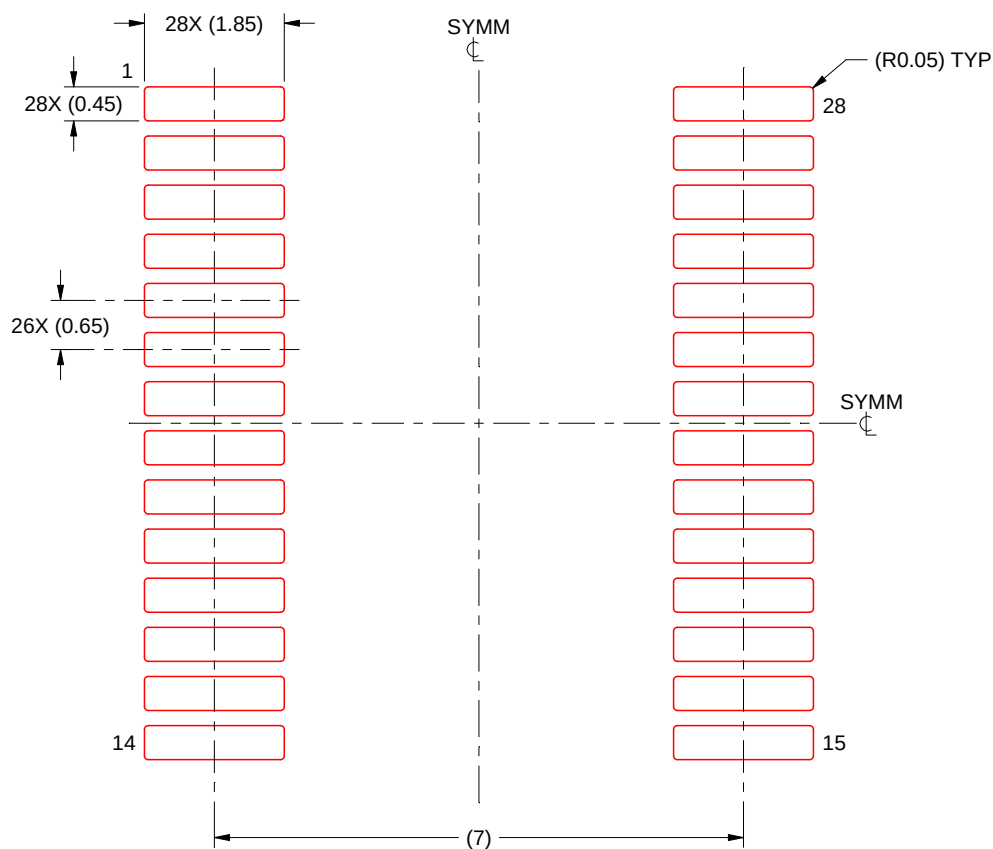
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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