

# TLC139, TLC339, TLC339Q LinCMOS™ MICROPOWER QUAD COMPARATORS

SLCS119B – DECEMBER 1986 – REVISED DECEMBER 2006

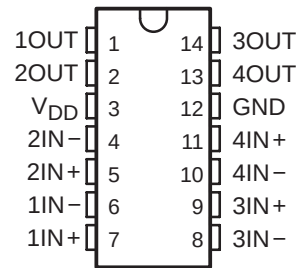
- Very Low Power . . . 200  $\mu$ W Typ at 5 V
- Fast Response Time . . . 2.5  $\mu$ s Typ With 5-mV Overdrive
- Single Supply Operation:  
TLC139M . . . 4 V to 16 V  
TLC339M . . . 4 V to 16 V  
TLC339C . . . 3 V to 16 V  
TLC339I . . . 3 V to 16 V
- High Input Impedance . . .  $10^{12} \Omega$  Typ
- Input Offset Voltage Change at Worst Case Input at Condition Typically 0.23  $\mu$ V/Month Including the First 30 Days
- On-Chip ESD Protection

## description

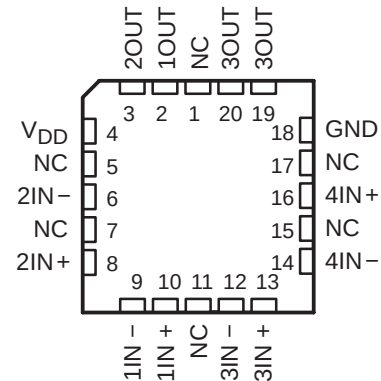
The TLC139/TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM139/LM339 family but uses 1/20th the power for similar response times. The open-drain MOS output stage interfaces to a variety of leads and supplies, as well as wired logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

The Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

D, J, N, OR PW PACKAGE  
(TOP VIEW)



FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## symbol (each comparator)



## AVAILABLE OPTIONS

| T <sub>A</sub> | V <sub>IO</sub><br>max AT<br>25°C | PACKAGE                 |                      |                    |                    |               |
|----------------|-----------------------------------|-------------------------|----------------------|--------------------|--------------------|---------------|
|                |                                   | SMALL<br>OUTLINE<br>(D) | CHIP CARRIER<br>(FK) | CERAMIC DIP<br>(J) | PLASTIC DIP<br>(P) | TSSOP<br>(PW) |
| 0°C to 70°C    | 5 mV                              | TLC339CD                | —                    | —                  | TLC339CN           | TLC339CPW     |
| –40°C to 85°C  | 5 mV                              | TLC339ID                | —                    | —                  | TLC339IN           | TLC339IPW     |
| –40°C to 125°C | 5 mV                              | TLC339QD                | —                    | —                  | TLC339QN           | —             |
| –55°C to 125°C | 5 mV                              | TLC339MD                | TLC139MFK            | TLC139MJ           | TLC339MN           | —             |

The D and PW packages are available taped and reeled. Add the suffix R to the device type (e.g., TLC339CDR or TLC339CPWR).

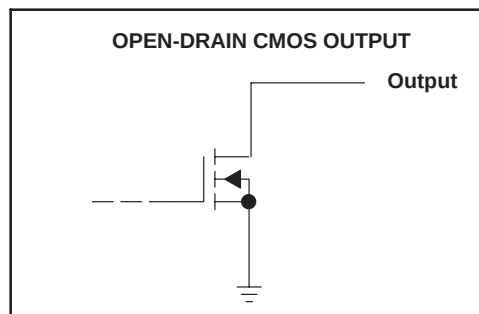
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## description (continued)

The TLC139M and TLC339M are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The TLC339C is characterized for operation over the commercial temperature range of  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ . The TLC339I is characterized for operation over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The TLC339Q is characterized for operation over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## output schematic



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                              |                                              |
|------------------------------------------------------------------------------|----------------------------------------------|
| Supply voltage range, $V_{DD}$ (see Note 1)                                  | $-0.3\text{ V to }18\text{ V}$               |
| Differential input voltage, $V_{ID}$ (see Note 2)                            | $\pm 18\text{ V}$                            |
| Input voltage range, $V_I$                                                   | $-0.3\text{ V to }V_{DD}$                    |
| Output voltage range, $V_O$                                                  | $-0.3\text{ V to }V_{DD}$                    |
| Input current, $I_I$                                                         | $\pm 5\text{ mA}$                            |
| Output current, $I_O$ (each output)                                          | $20\text{ mA}$                               |
| Total supply current into $V_{DD}$                                           | $40\text{ mA}$                               |
| Total current out of GND                                                     | $60\text{ mA}$                               |
| Continuous total dissipation                                                 | See Dissipation Rating Table                 |
| Operating free-air temperature range, $T_A$ : TLC139M                        | $-55^{\circ}\text{C to }125^{\circ}\text{C}$ |
| TLC339C                                                                      | $0^{\circ}\text{C to }70^{\circ}\text{C}$    |
| TLC339I                                                                      | $-40^{\circ}\text{C to }85^{\circ}\text{C}$  |
| TLC339M                                                                      | $-55^{\circ}\text{C to }125^{\circ}\text{C}$ |
| TLC339Q                                                                      | $-40^{\circ}\text{C to }125^{\circ}\text{C}$ |
| Storage temperature range                                                    | $-65^{\circ}\text{C to }150^{\circ}\text{C}$ |
| Case temperature for 60 seconds: FK package                                  | $260^{\circ}\text{C}$                        |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package | $260^{\circ}\text{C}$                        |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package      | $300^{\circ}\text{C}$                        |

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.  
2. Differential voltages are at  $IN+$  with respect to  $IN-$ .

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25^{\circ}\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^{\circ}\text{C}$ | $T_A = 70^{\circ}\text{C}$<br>POWER RATING | $T_A = 85^{\circ}\text{C}$<br>POWER RATING | $T_A = 125^{\circ}\text{C}$<br>POWER RATING |
|---------|-----------------------------------------------|-----------------------------------------------------|--------------------------------------------|--------------------------------------------|---------------------------------------------|
| D       | 950 mW                                        | $7.6\text{ mW}/^{\circ}\text{C}$                    | 608 mW                                     | 494 mW                                     | 190 mW                                      |
| FK      | 1375 mW                                       | $11.0\text{ mW}/^{\circ}\text{C}$                   | 880 mW                                     | 715 mW                                     | 275 mW                                      |
| J       | 1375 mW                                       | $11.0\text{ mW}/^{\circ}\text{C}$                   | 880 mW                                     | 715 mW                                     | 275 mW                                      |
| N       | 1150 mW                                       | $9.2\text{ mW}/^{\circ}\text{C}$                    | 736 mW                                     | 598 mW                                     | 230 mW                                      |
| PW      | 700 mW                                        | $5.6\text{ mW}/^{\circ}\text{C}$                    | 448 mW                                     | 364 mW                                     | 140 mW                                      |

**recommended operating conditions**

|                                       | TLC139M, TLC339M |     |                | UNIT |
|---------------------------------------|------------------|-----|----------------|------|
|                                       | MIN              | NOM | MAX            |      |
| Supply voltage, $V_{DD}$              | 4                | 5   | 16             | V    |
| Common-mode input voltage, $V_{IC}$   | 0                |     | $V_{DD} - 1.5$ | V    |
| Low-level output current, $I_{OL}$    |                  |     | 20             | mA   |
| Operating free-air temperature, $T_A$ | -55              |     | 125            | °C   |

**electrical characteristics at specified operating free-air temperature,  $V_{DD} = 5$  V (unless otherwise noted)**

| PARAMETER |                                   | TEST CONDITIONS†                      | $T_A$          | TLC139M, TLC339M |                     |     | UNIT |
|-----------|-----------------------------------|---------------------------------------|----------------|------------------|---------------------|-----|------|
|           |                                   |                                       |                | MIN              | TYP                 | MAX |      |
| $V_{IO}$  | Input offset voltage              | $V_{IC} = V_{ICRmin}$ ,<br>See Note 3 | 25°C           |                  | 1.4                 | 5   | mV   |
|           |                                   |                                       | -55°C to 125°C |                  |                     | 10  |      |
| $I_{IO}$  | Input offset current              | $V_{IC} = 2.5$ V                      | 25°C           |                  | 1                   |     | pA   |
|           |                                   |                                       | 125°C          |                  |                     | 15  | nA   |
| $I_{IB}$  | Input bias current                | $V_{IC} = 2.5$ V                      | 25°C           |                  | 5                   |     | pA   |
|           |                                   |                                       | 125°C          |                  |                     | 30  | nA   |
| $V_{ICR}$ | Common-mode input voltage range   |                                       | 25°C           |                  | 0 to $V_{DD} - 1$   |     | V    |
|           |                                   |                                       | -55°C to 125°C |                  | 0 to $V_{DD} - 1.5$ |     |      |
| CMRR      | Common-mode rejection ratio       | $V_{IC} = V_{ICRmin}$                 | 25°C           |                  | 84                  |     | dB   |
|           |                                   |                                       | 125°C          |                  | 84                  |     |      |
|           |                                   |                                       | -55°C          |                  | 84                  |     |      |
| $k_{SVR}$ | Supply-voltage rejection ratio    | $V_{DD} = 5$ V to 10 V                | 25°C           |                  | 85                  |     | dB   |
|           |                                   |                                       | 125°C          |                  | 84                  |     |      |
|           |                                   |                                       | -55°C          |                  | 84                  |     |      |
| $V_{OL}$  | Low-level output voltage          | $V_{ID} = -1$ V, $I_{OL} = 6$ mA      | 25°C           |                  | 300                 | 400 | mV   |
|           |                                   |                                       | 125°C          |                  |                     | 800 |      |
| $I_{OH}$  | High-level output current         | $V_{ID} = -1$ V, $V_O = 5$ V          | 25°C           |                  | 0.8                 | 40  | nA   |
|           |                                   |                                       | 125°C          |                  |                     | 1   | μA   |
| $I_{DD}$  | Supply current (four comparators) | Outputs low, No load                  | 25°C           |                  | 44                  | 80  | μA   |
|           |                                   |                                       | -55°C to 125°C |                  |                     | 175 |      |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to  $V_{DD}$ .

# TLC139, TLC339, TLC339Q

## LinCMOS™ MICROPOWER QUAD COMPARATORS

### recommended operating conditions

|                                       | TLC339C |     |              | UNIT |
|---------------------------------------|---------|-----|--------------|------|
|                                       | MIN     | NOM | MAX          |      |
| Supply voltage, $V_{DD}$              | 3       | 5   | 16           | V    |
| Common-mode input voltage, $V_{IC}$   | -0.2    |     | $V_{DD}-1.5$ | V    |
| Low-level output current, $I_{OL}$    |         | 8   | 20           | mA   |
| Operating free-air temperature, $T_A$ | 0       |     | 70           | °C   |

### electrical characteristics at specified operating free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

| PARAMETER |                                   | TEST CONDITIONS†                      | $T_A$       | TLC339C |                   |     | UNIT |
|-----------|-----------------------------------|---------------------------------------|-------------|---------|-------------------|-----|------|
|           |                                   |                                       |             | MIN     | TYP               | MAX |      |
| $V_{IO}$  | Input offset voltage              | $V_{IC} = V_{ICRmin}$ ,<br>See Note 3 | 25°C        |         | 1.4               | 5   | mV   |
|           |                                   |                                       | 0°C to 70°C |         |                   | 6.5 |      |
| $I_{IO}$  | Input offset current              | $V_{IC} = 2.5$ V                      | 25°C        |         | 1                 |     | pA   |
|           |                                   |                                       | 70°C        |         |                   | 0.3 | nA   |
| $I_{IB}$  | Input bias current                | $V_{IC} = 2.5$ V                      | 25°C        |         | 5                 |     | pA   |
|           |                                   |                                       | 70°C        |         |                   | 0.6 | nA   |
| $V_{ICR}$ | Common-mode input voltage range   |                                       | 25°C        |         | 0 to $V_{DD}-1$   |     | V    |
|           |                                   |                                       | 0°C to 70°C |         | 0 to $V_{DD}-1.5$ |     |      |
| CMRR      | Common-mode rejection ratio       | $V_{IC} = V_{ICRmin}$                 | 25°C        |         | 84                |     | dB   |
|           |                                   |                                       | 70°C        |         | 84                |     |      |
|           |                                   |                                       | 0°C         |         | 84                |     |      |
| $k_{SVR}$ | Supply-voltage rejection ratio    | $V_{DD} = 5$ V to 10 V                | 25°C        |         | 85                |     | dB   |
|           |                                   |                                       | 70°C        |         | 85                |     |      |
|           |                                   |                                       | 0°C         |         | 85                |     |      |
| $V_{OL}$  | Low-level output voltage          | $V_{ID} = -1$ V, $I_{OL} = 6$ mA      | 25°C        |         | 300               | 400 | mV   |
|           |                                   |                                       | 70°C        |         |                   | 650 |      |
| $I_{OH}$  | High-level output current         | $V_{ID} = -1$ V, $V_O = 5$ V          | 25°C        |         | 0.8               | 40  | nA   |
|           |                                   |                                       | 70°C        |         |                   | 1   | μA   |
| $I_{DD}$  | Supply current (four comparators) | Outputs low, No load                  | 25°C        |         | 44                | 80  | μA   |
|           |                                   |                                       | 0°C to 70°C |         |                   | 100 |      |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to  $V_{DD}$ .

**recommended operating conditions**

|                                       | TLC339I |     |                | UNIT |
|---------------------------------------|---------|-----|----------------|------|
|                                       | MIN     | NOM | MAX            |      |
| Supply voltage, $V_{DD}$              | 3       | 5   | 16             | V    |
| Common-mode input voltage, $V_{IC}$   | -0.2    |     | $V_{DD} - 1.5$ | V    |
| Low-level output current, $I_{OL}$    |         | 8   | 20             | mA   |
| Operating free-air temperature, $T_A$ | 0       |     | 70             | °C   |

**electrical characteristics at specified operating free-air temperature,  $V_{DD} = 5$  V (unless otherwise noted)**

| PARAMETER |                                   | TEST CONDITIONS†                      | $T_A$         | TLC339I |                     |     | UNIT |
|-----------|-----------------------------------|---------------------------------------|---------------|---------|---------------------|-----|------|
|           |                                   |                                       |               | MIN     | TYP                 | MAX |      |
| $V_{IO}$  | Input offset voltage              | $V_{IC} = V_{ICRmin}$ ,<br>See Note 3 | 25°C          |         | 1.4                 | 5   | mV   |
|           |                                   |                                       | -40°C to 85°C |         |                     | 7   |      |
| $I_{IO}$  | Input offset current              | $V_{IC} = 2.5$ V                      | 25°C          |         | 1                   |     | pA   |
|           |                                   |                                       | 85°C          |         |                     | 1   | nA   |
| $I_{IB}$  | Input bias current                | $V_{IC} = 2.5$ V                      | 25°C          |         | 5                   |     | pA   |
|           |                                   |                                       | 85°C          |         |                     | 2   | nA   |
| $V_{ICR}$ | Common-mode input voltage range   |                                       | 25°C          |         | 0 to $V_{DD} - 1$   |     | V    |
|           |                                   |                                       | -40°C to 85°C |         | 0 to $V_{DD} - 1.5$ |     |      |
| CMRR      | Common-mode rejection ratio       | $V_{IC} = V_{ICRmin}$                 | 25°C          |         | 84                  |     | dB   |
|           |                                   |                                       | 85°C          |         | 84                  |     |      |
|           |                                   |                                       | -40°C         |         | 84                  |     |      |
| $k_{SVR}$ | Supply-voltage rejection ratio    | $V_{DD} = 5$ V to 10 V                | 25°C          |         | 85                  |     | dB   |
|           |                                   |                                       | 85°C          |         | 85                  |     |      |
|           |                                   |                                       | -40°C         |         | 84                  |     |      |
| $V_{OL}$  | Low-level output voltage          | $V_{ID} = -1$ V, $I_{OL} = 6$ mA      | 25°C          |         | 300                 | 400 | mV   |
|           |                                   |                                       | 85°C          |         |                     | 700 |      |
| $I_{OH}$  | High-level output current         | $V_{ID} = -1$ V, $V_O = 5$ V          | 25°C          |         | 0.8                 | 40  | nA   |
|           |                                   |                                       | 85°C          |         |                     | 1   | μA   |
| $I_{DD}$  | Supply current (four comparators) | Outputs low, No load                  | 25°C          |         | 44                  | 80  | μA   |
|           |                                   |                                       | -40°C to 85°C |         |                     | 125 |      |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to  $V_{DD}$ .

# TLC139, TLC339, TLC339Q

## LinCMOS™ MICROPOWER QUAD COMPARATORS

### recommended operating conditions

|                                       | TLC339Q |     |              | UNIT |
|---------------------------------------|---------|-----|--------------|------|
|                                       | MIN     | NOM | MAX          |      |
| Supply voltage, $V_{DD}$              | 4       | 5   | 16           | V    |
| Common-mode input voltage, $V_{IC}$   | 0       |     | $V_{DD}-1.5$ | V    |
| Low-level output current, $I_{OL}$    |         |     | 20           | mA   |
| Operating free-air temperature, $T_A$ | -40     |     | 125          | °C   |

### electrical characteristics at specified operating free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

| PARAMETER |                                   | TEST CONDITIONS†                      | $T_A$          | TLC339Q |                   |     | UNIT |
|-----------|-----------------------------------|---------------------------------------|----------------|---------|-------------------|-----|------|
|           |                                   |                                       |                | MIN     | TYP               | MAX |      |
| $V_{IO}$  | Input offset voltage              | $V_{IC} = V_{ICRmin}$ ,<br>See Note 3 | 25°C           |         | 1.4               | 5   | mV   |
|           |                                   |                                       | -40°C to 125°C |         |                   | 10  |      |
| $I_{IO}$  | Input offset current              | $V_{IC} = 2.5$ V                      | 25°C           |         | 1                 |     | pA   |
|           |                                   |                                       | 125°C          |         |                   | 15  | nA   |
| $I_{IB}$  | Input bias current                | $V_{IC} = 2.5$ V                      | 25°C           |         | 5                 |     | pA   |
|           |                                   |                                       | 125°C          |         |                   | 30  | nA   |
| $V_{ICR}$ | Common-mode input voltage range   |                                       | 25°C           |         | 0 to $V_{DD}-1$   |     | V    |
|           |                                   |                                       | -40°C to 125°C |         | 0 to $V_{DD}-1.5$ |     |      |
| CMRR      | Common-mode rejection ratio       | $V_{IC} = V_{ICRmin}$                 | 25°C           |         | 84                |     | dB   |
|           |                                   |                                       | 125°C          |         | 84                |     |      |
|           |                                   |                                       | -40°C          |         | 84                |     |      |
| $k_{SVR}$ | Supply-voltage rejection ratio    | $V_{DD} = 5$ V to 10 V                | 25°C           |         | 85                |     | dB   |
|           |                                   |                                       | 125°C          |         | 84                |     |      |
|           |                                   |                                       | -40°C          |         | 84                |     |      |
| $V_{OL}$  | Low-level output voltage          | $V_{ID} = -1$ V, $I_{OL} = 6$ mA      | 25°C           |         | 300               | 400 | mV   |
|           |                                   |                                       | 125°C          |         |                   | 800 |      |
| $I_{OH}$  | High-level output current         | $V_{ID} = -1$ V, $V_O = 5$ V          | 25°C           |         | 0.8               | 40  | nA   |
|           |                                   |                                       | 125°C          |         |                   | 1   | μA   |
| $I_{DD}$  | Supply current (four comparators) | Outputs low, No load                  | 25°C           |         | 44                | 80  | μA   |
|           |                                   |                                       | -40°C to 125°C |         |                   | 125 |      |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to  $V_{DD}$ .

switching characteristics,  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 3)

| PARAMETER                                                  | TEST CONDITIONS                               | TLC139M, TLC339C<br>TLC339I, TLC339M<br>TLC339Q |      |     | UNIT          |
|------------------------------------------------------------|-----------------------------------------------|-------------------------------------------------|------|-----|---------------|
|                                                            |                                               | MIN                                             | TYP  | MAX |               |
| $t_{PLH}$ Propagation delay time, low-to-high output       | $f = 10\text{ kHz}$ ,<br>$C_L = 15\text{ pF}$ | Overdrive = 2 mV                                | 4.5  |     | $\mu\text{s}$ |
|                                                            |                                               | Overdrive = 5 mV                                | 2.5  |     |               |
|                                                            |                                               | Overdrive = 10 mV                               | 1.7  |     |               |
|                                                            |                                               | Overdrive = 20 mV                               | 1.2  |     |               |
|                                                            |                                               | Overdrive = 40 mV                               | 1.0  |     |               |
|                                                            | $V_I = 1.4\text{ V}$ step at $IN+$            |                                                 | 1.1  |     |               |
| $t_{PHL}$ Propagation delay time, high-to-low level output | $f = 10\text{ kHz}$ ,<br>$C_L = 15\text{ pF}$ | Overdrive = 2 mV                                | 3.6  |     | $\mu\text{s}$ |
|                                                            |                                               | Overdrive = 5 mV                                | 2.1  |     |               |
|                                                            |                                               | Overdrive = 10 mV                               | 1.3  |     |               |
|                                                            |                                               | Overdrive = 20 mV                               | 0.85 |     |               |
|                                                            |                                               | Overdrive = 40 mV                               | 0.55 |     |               |
|                                                            | $V_I = 1.4\text{ V}$ step at $IN+$            |                                                 | 0.10 |     |               |
| $t_{THL}$ Transition time, high-to-low level output        | $f = 10\text{ kHz}$ ,<br>$C_L = 15\text{ pF}$ | Overdrive = 50 mV                               | 20   |     | ns            |

### PARAMETER MEASUREMENT INFORMATION

The TLC139 and TLC339 contain a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the  $V_{ICR}$  test, rather than changing the input voltages, to provide greater accuracy.

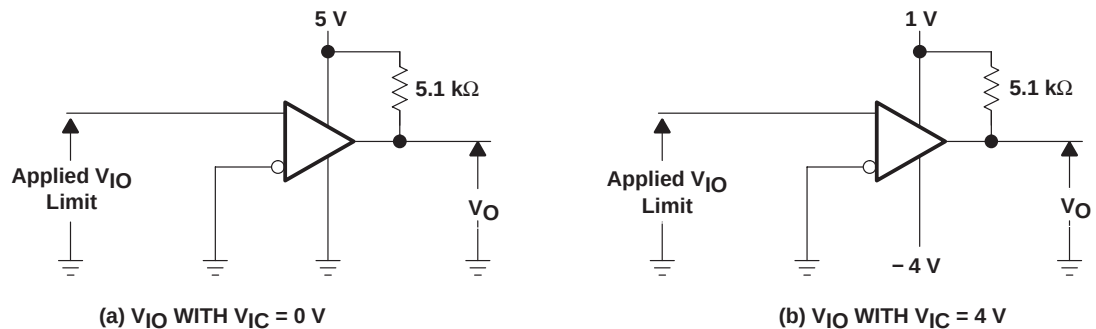


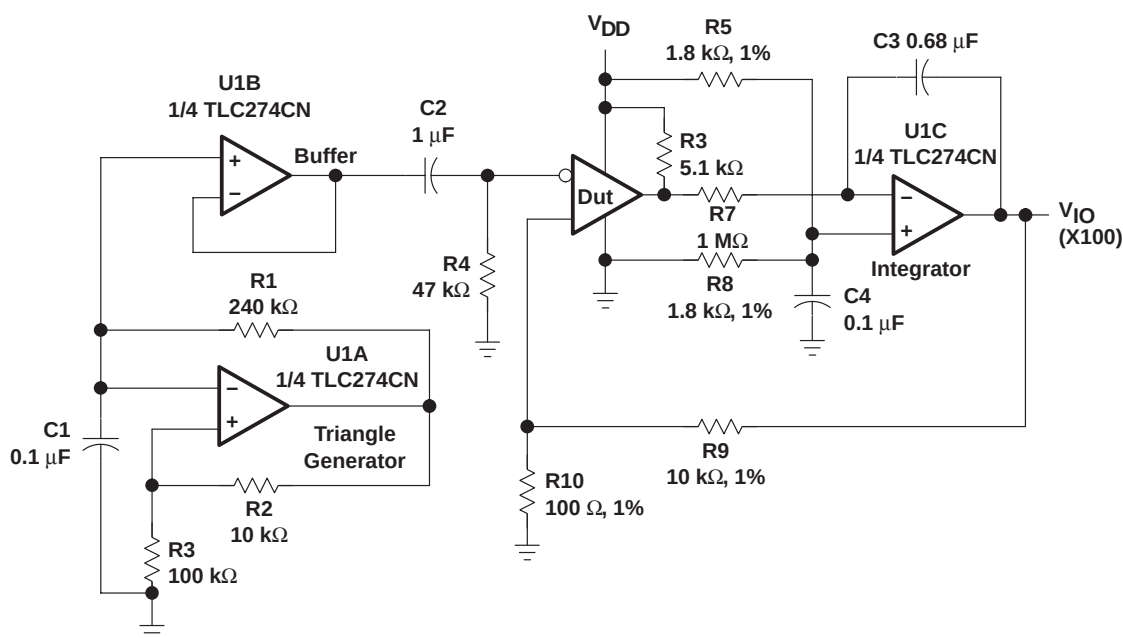
Figure 1. Method for Verifying That Input Offset Voltage Is Within Specified Limits

## PARAMETER MEASUREMENT INFORMATION

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes state.

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

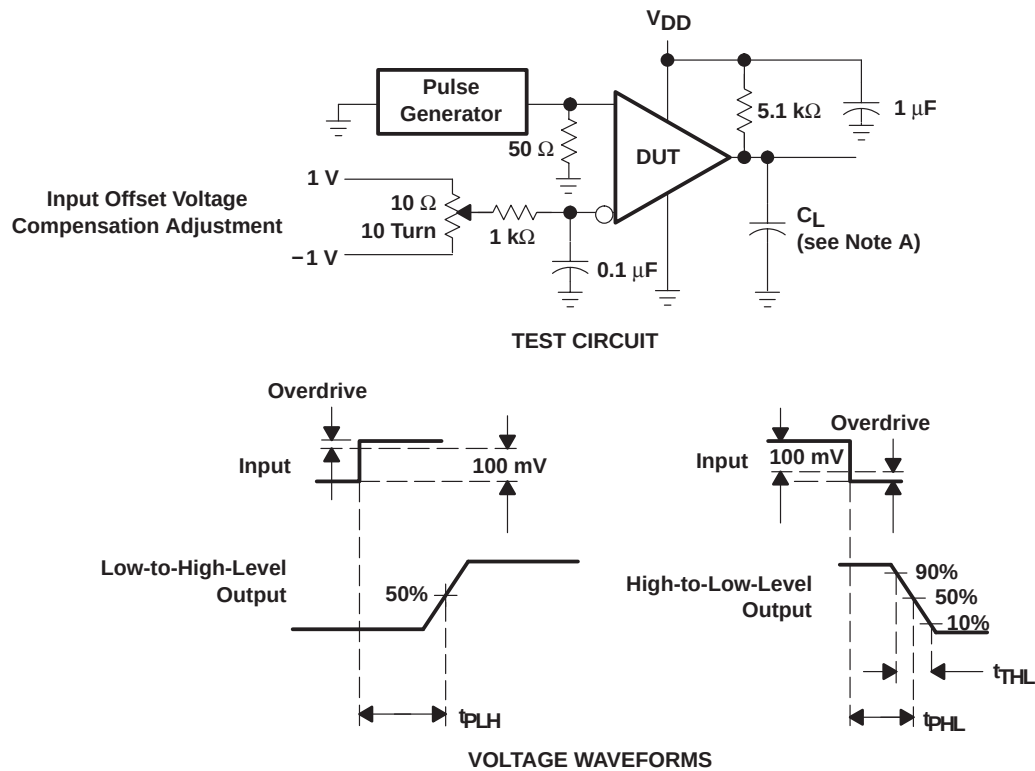


**Figure 2. Circuit for Input Offset Voltage Measurement**

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained, with a device in the socket to obtain the actual input current of the device.

## PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 3, so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.



NOTE A:  $C_L$  includes probe and jig capacitance.

**Figure 3. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

Table of Graphs

|           |                                                 |                                                    | FIGURE |
|-----------|-------------------------------------------------|----------------------------------------------------|--------|
| $V_{IO}$  | Input offset voltage                            | Distribution                                       | 4      |
| $I_{IB}$  | Input bias current                              | vs Free-air temperature                            | 5      |
| CMRR      | Common-mode rejection ratio                     | vs Free-air temperature                            | 6      |
| $k_{SVR}$ | Supply-voltage rejection ratio                  | vs Free-air temperature                            | 7      |
| $I_{OH}$  | High-level output current                       | vs High-level output voltage                       | 8      |
|           |                                                 | vs Free-air temperature                            | 9      |
| $V_{OL}$  | Low-level output voltage                        | vs Low-level output current                        | 10     |
|           |                                                 | vs Free-air temperature                            | 11     |
| $I_{DD}$  | Supply current                                  | vs Supply voltage                                  | 12     |
|           |                                                 | vs Free-air temperature                            | 13     |
| $t_{PLH}$ | Low-to-high level output propagation delay time | vs Supply voltage                                  | 14     |
| $t_{PHL}$ | Low-to-high level output propagation delay time | vs Supply voltage                                  | 15     |
|           | Overdrive voltage                               | vs Low-to-high-level output propagation delay time | 16     |
| $t_f$     | Output fall time                                | vs Supply voltage                                  | 17     |
|           | Overdrive voltage                               | vs High-to-low-level output propagation delay time | 18     |

**TYPICAL CHARACTERISTICS†**

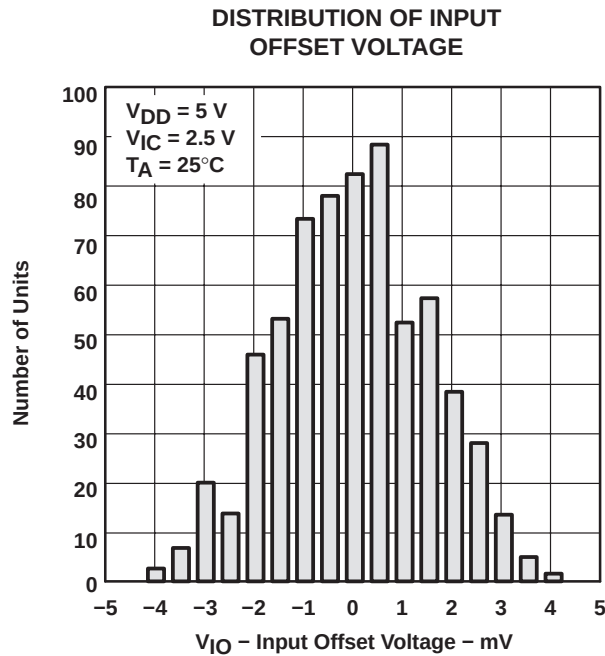


Figure 4

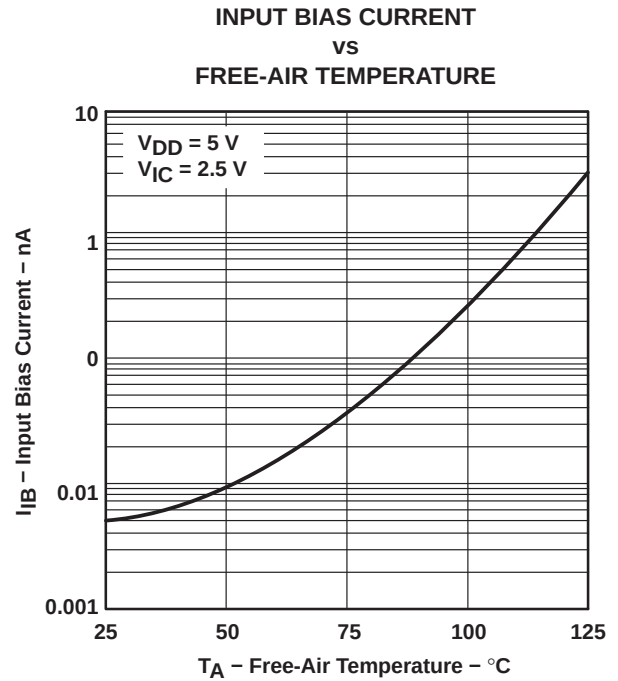


Figure 5

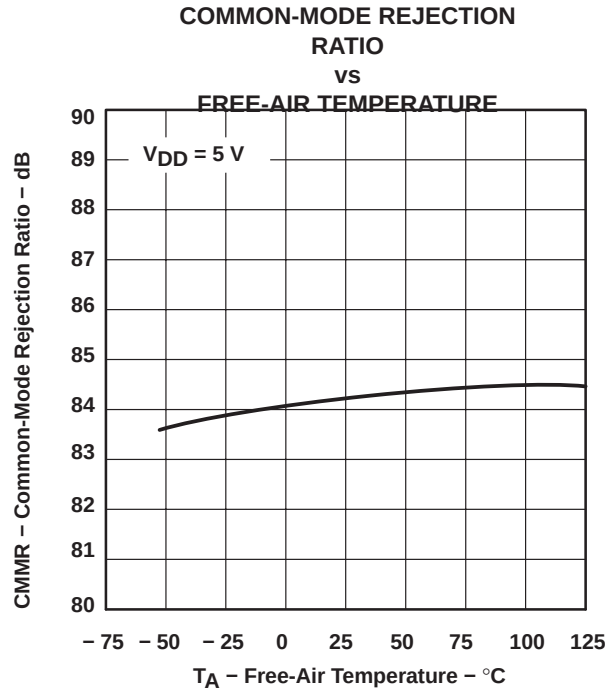


Figure 6

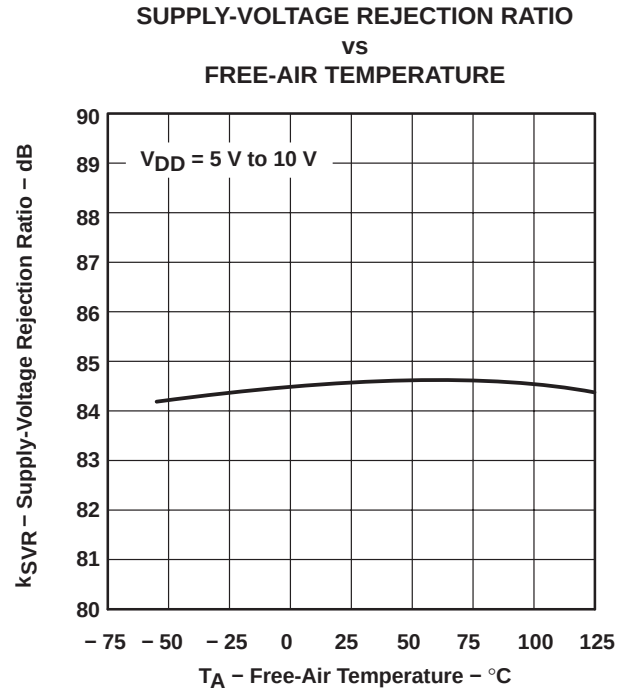
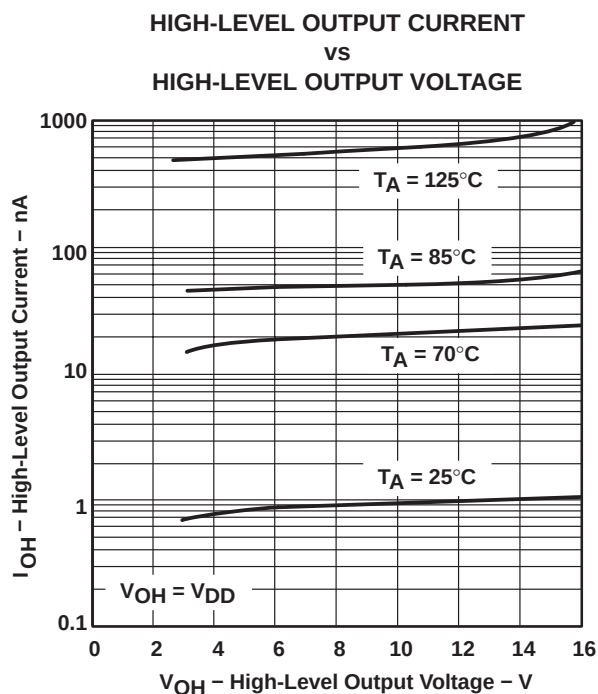


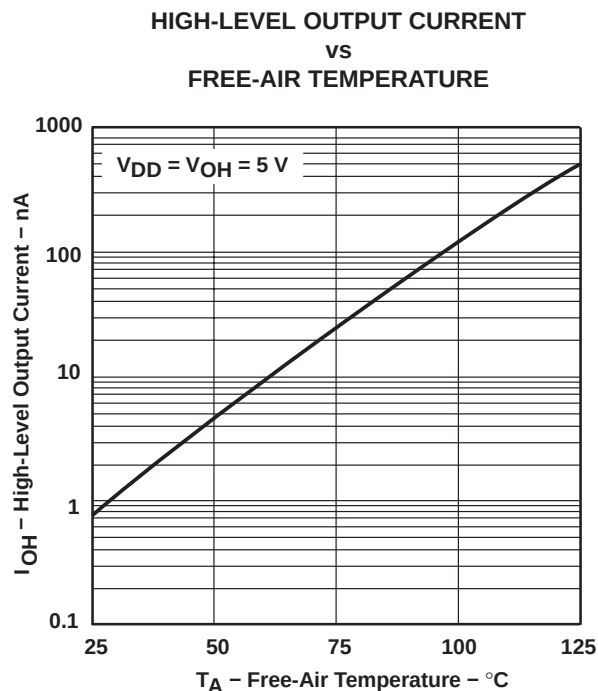
Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

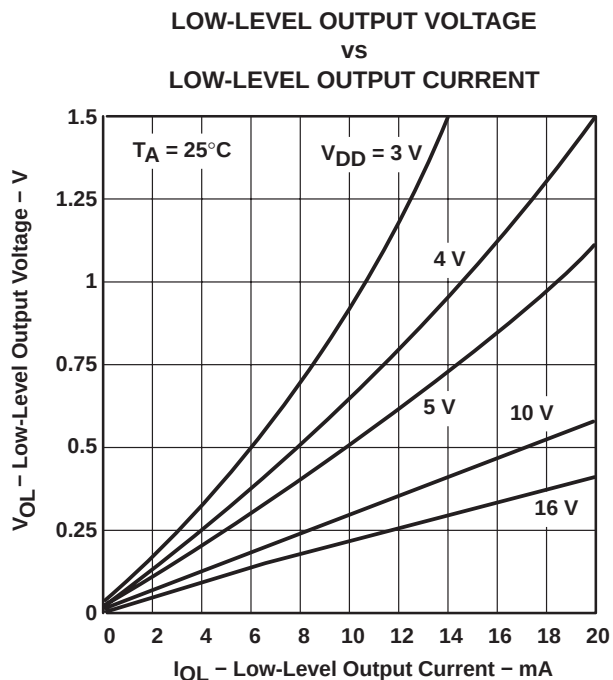
**TYPICAL CHARACTERISTICS†**



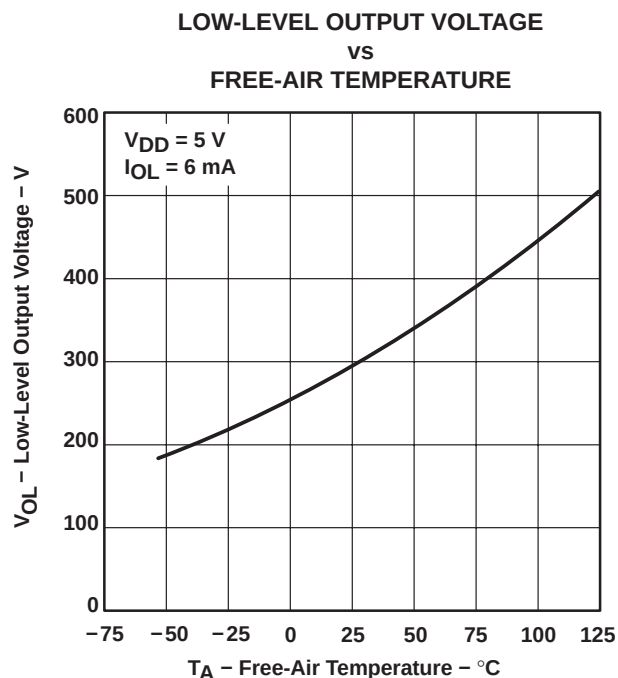
**Figure 8**



**Figure 9**



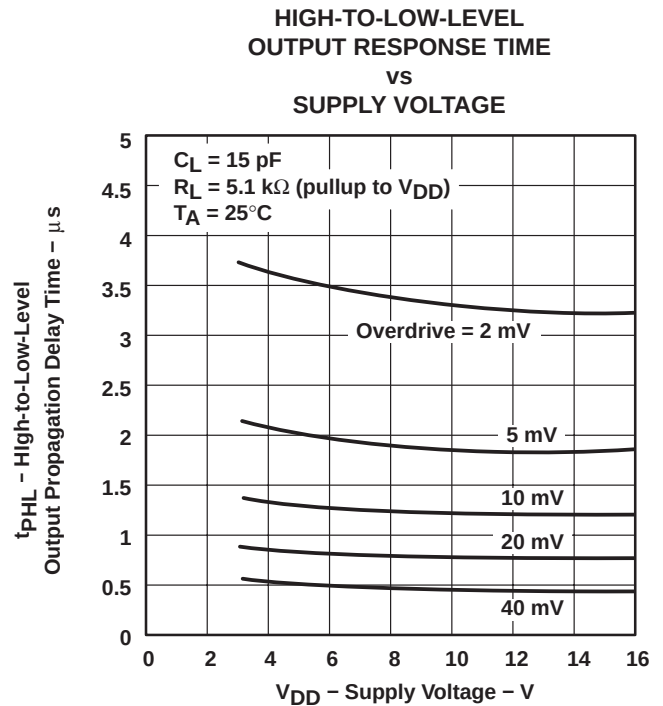
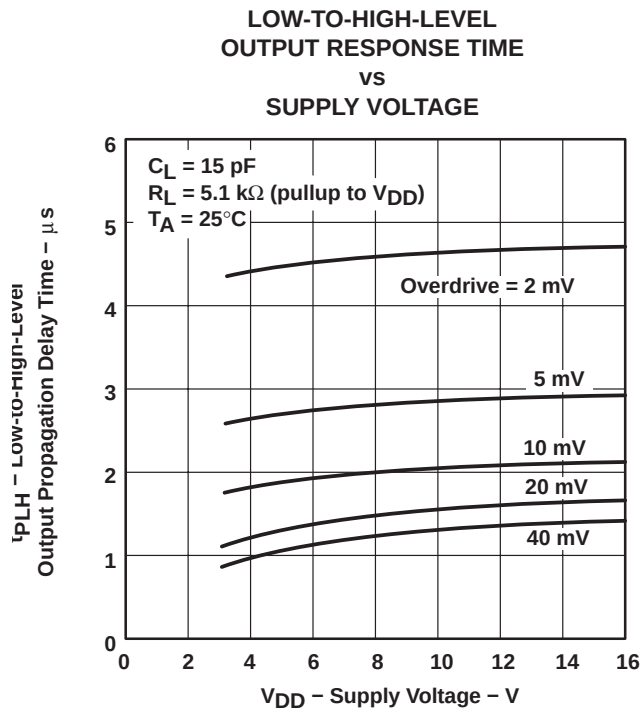
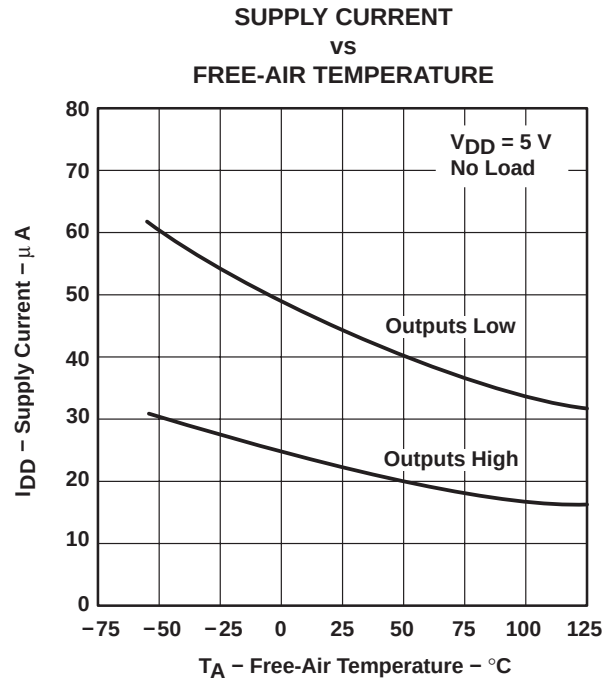
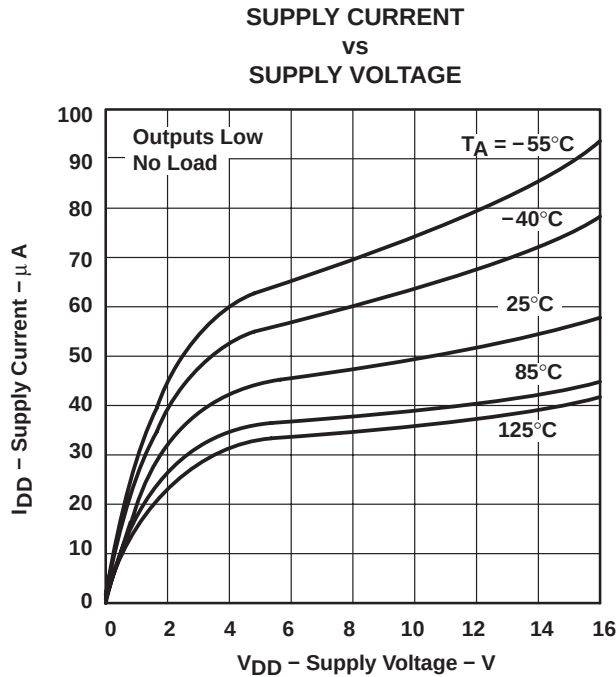
**Figure 10**



**Figure 11**

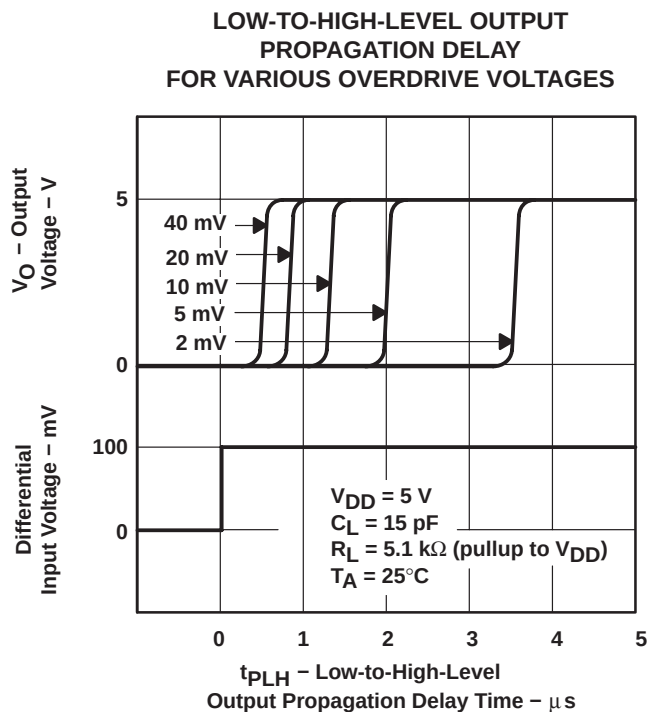
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TYPICAL CHARACTERISTICS†**

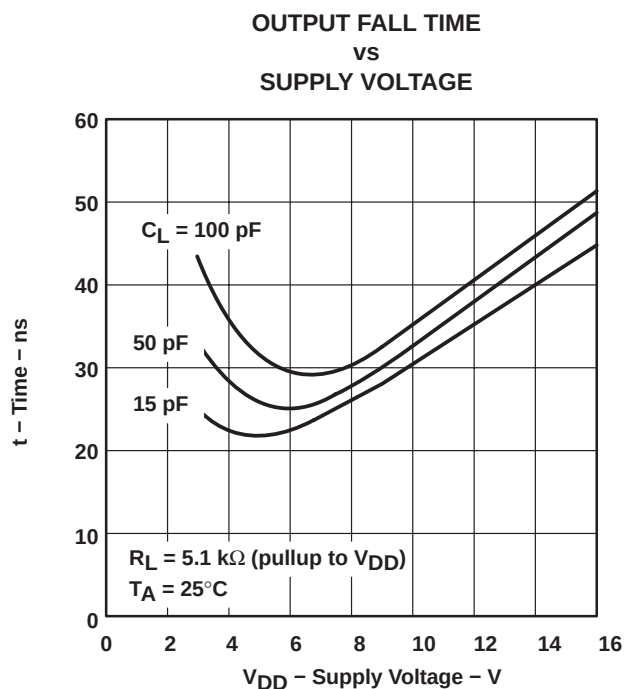


† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

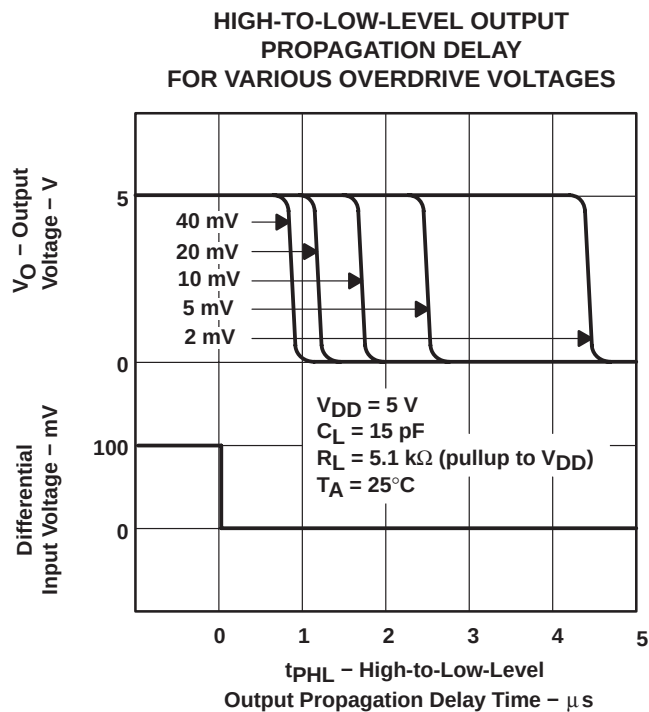
**TYPICAL CHARACTERISTICS**



**Figure 16**



**Figure 17**



**Figure 18**

## APPLICATION INFORMATION

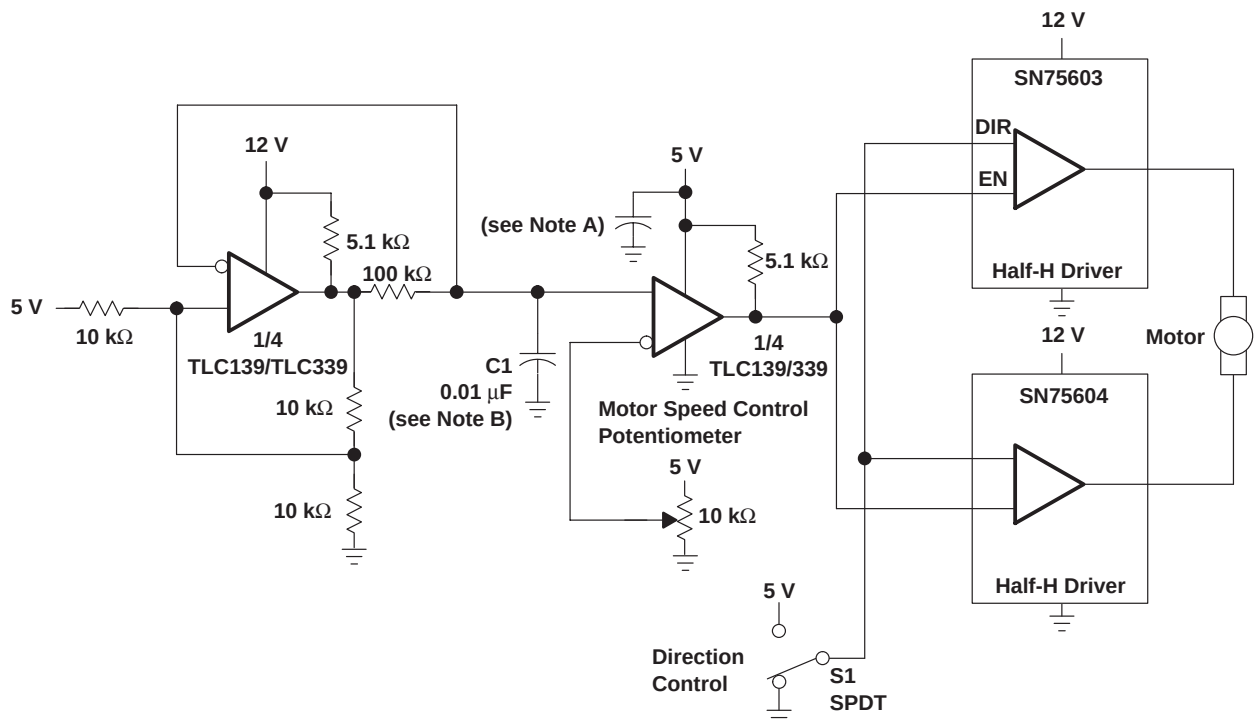
The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with  $V_{DD} = 5\text{ V}$ , both inputs must remain between  $-0.2\text{ V}$  and  $4\text{ V}$  to assure proper device operation. To assure reliable operation, the supply should be decoupled with a capacitor ( $0.1\text{ }\mu\text{F}$ ) positioned as close to the device as possible.

The output and supply currents require close observation since the TLC139/TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground has an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC139 and TLC339 have internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, exercise care when handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

Table of Applications

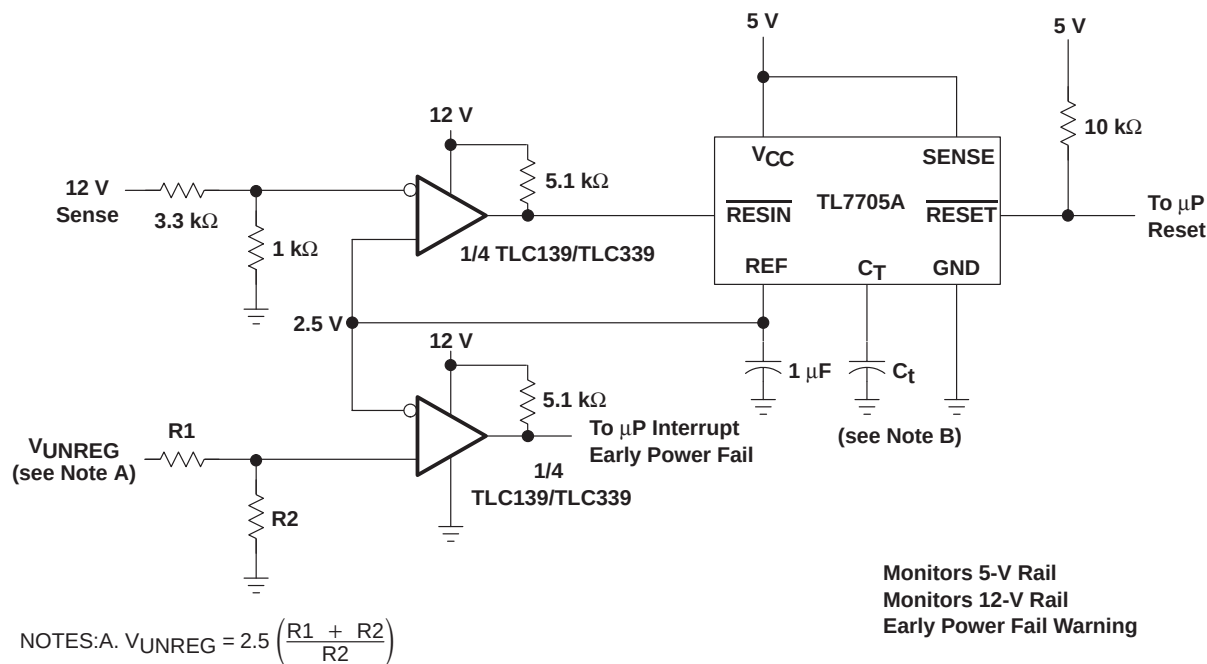
|                                              | FIGURE |
|----------------------------------------------|--------|
| Pulse-width-modulated motor speed controller | 19     |
| Enhanced supply supervisor                   | 20     |
| Two-phase nonoverlapping clock generator     | 21     |



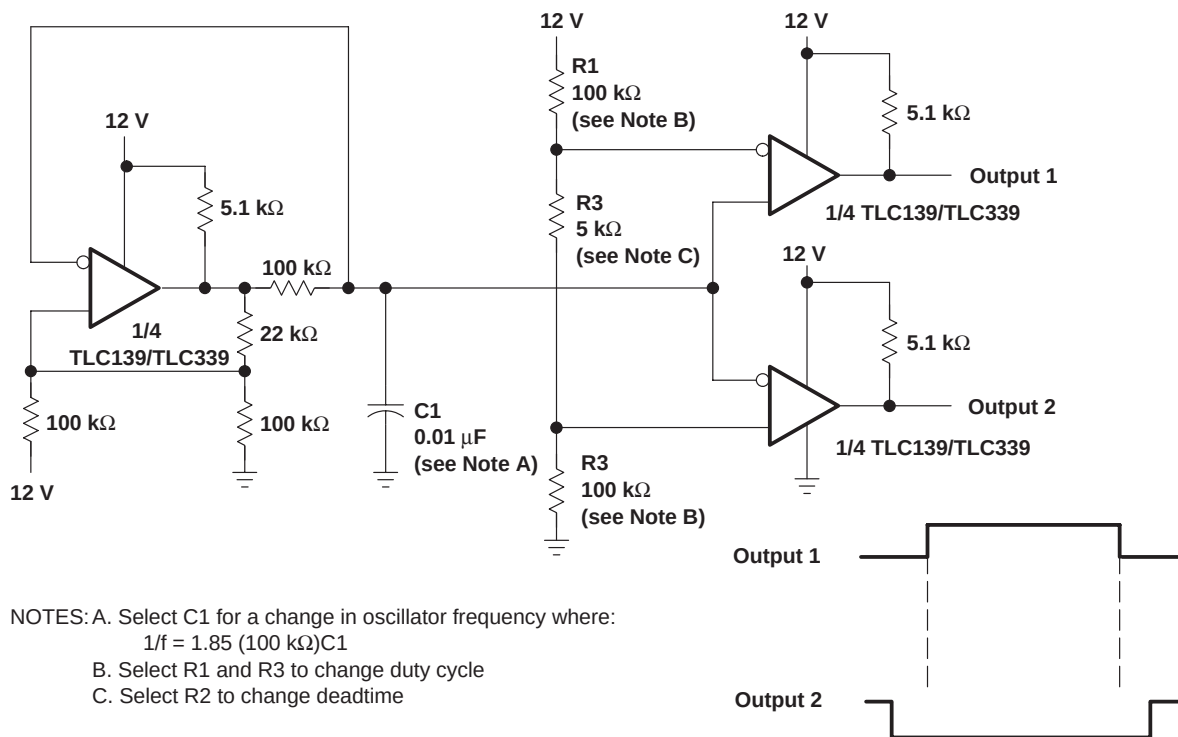
- NOTES: A. The recommended minimum capacitance is 10  $\mu\text{F}$  to eliminate common ground switching noise.  
 B. Select C1 for change in oscillator frequency.

**Figure 19. Pulse-Width-Modulated Motor Speed Controller**

**TYPICAL APPLICATION DATA**



**Figure 20. Enhanced Supply Supervisor**



**Figure 21. Two-Phase Nonoverlapping Clock Generator**

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C)            | Part marking<br>(6)              |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|-------------------------|----------------------------------|
| <a href="#">5962-87659022A</a>   | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125              | 5962-<br>87659022A<br>TLC139MFKB |
| <a href="#">5962-8765902CA</a>   | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125              | 5962-8765902CA<br>TLC139MJB      |
| 5962-9555001NXD                  | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See<br>5962-9555001NXDR | QTLC139M                         |
| <a href="#">5962-9555001NXDR</a> | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -                       | QTLC139M                         |
| 5962-9555001NXDR.A               | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125              | QTLC139M                         |
| <a href="#">TLC139MFKB</a>       | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -                       | 5962-<br>87659022A<br>TLC139MFKB |
| TLC139MFKB.A                     | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125              | 5962-<br>87659022A<br>TLC139MFKB |
| <a href="#">TLC139MJB</a>        | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -                       | 5962-8765902CA<br>TLC139MJB      |
| TLC139MJB.A                      | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125              | 5962-8765902CA<br>TLC139MJB      |
| <a href="#">TLC339CD</a>         | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -                       | TLC339C                          |
| <a href="#">TLC339CDR</a>        | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -                       | TLC339C                          |
| TLC339CDR.A                      | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125              | TLC339C                          |
| <a href="#">TLC339CN</a>         | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -                       | TLC339CN                         |
| TLC339CN.A                       | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125              | TLC339CN                         |
| <a href="#">TLC339CNSR</a>       | Active        | Production           | SOP (NS)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -                       | TLC339                           |
| TLC339CNSR.A                     | Active        | Production           | SOP (NS)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125              | TLC339                           |
| <a href="#">TLC339CPW</a>        | Obsolete      | Production           | TSSOP (PW)   14 | -                     | -           | Call TI                              | Call TI                           | -                       | P339                             |
| <a href="#">TLC339CPWR</a>       | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -                       | P339                             |
| TLC339CPWR.A                     | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125              | P339                             |
| <a href="#">TLC339ID</a>         | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -                       | TLC339I                          |
| <a href="#">TLC339IDR</a>        | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -                       | TLC339I                          |
| TLC339IDR.A                      | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125              | TLC339I                          |

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TLC339IDR1G4                | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TLC339I             |
| TLC339IDR1G4.A              | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TLC339I             |
| <a href="#">TLC339IN</a>    | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -            | TLC339IN            |
| TLC339IN.A                  | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | TLC339IN            |
| <a href="#">TLC339IPW</a>   | Obsolete      | Production           | TSSOP (PW)   14 | -                     | -           | Call TI                              | Call TI                           | -            | TLC339I             |
| <a href="#">TLC339IPWR</a>  | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -            | TLC339I             |
| TLC339IPWR.A                | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TLC339I             |
| <a href="#">TLC339MD</a>    | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | TLC339M             |
| <a href="#">TLC339MDG4</a>  | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | TLC339M             |
| <a href="#">TLC339MDR</a>   | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TLC339M             |
| TLC339MDR.A                 | Active        | Production           | SOIC (D)   14   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | TLC339M             |
| <a href="#">TLC339MDRG4</a> | Obsolete      | Production           | SOIC (D)   14   | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | TLC339M             |
| <a href="#">TLC339MN</a>    | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | TLC339MN            |
| TLC339MN.A                  | Active        | Production           | PDIP (N)   14   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | TLC339MN            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

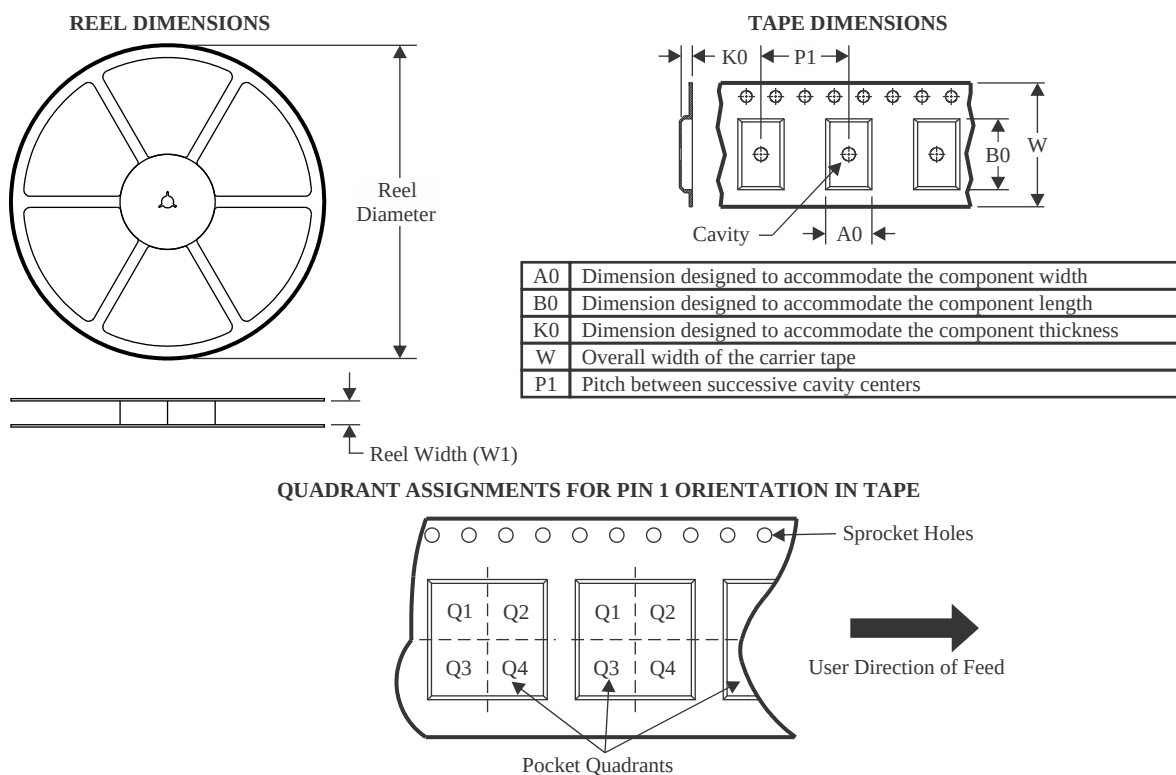
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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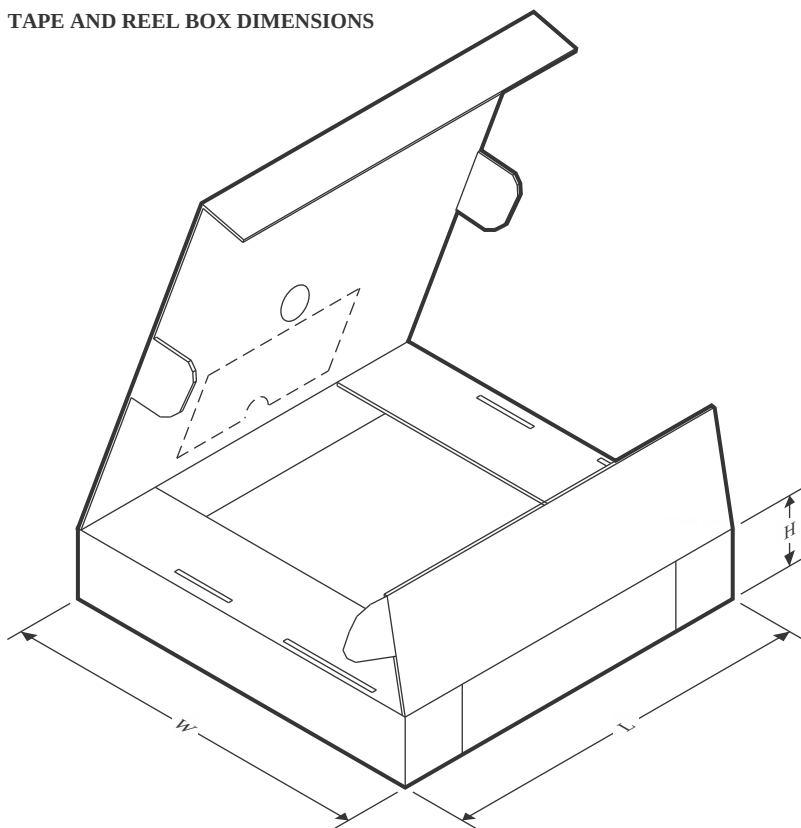
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

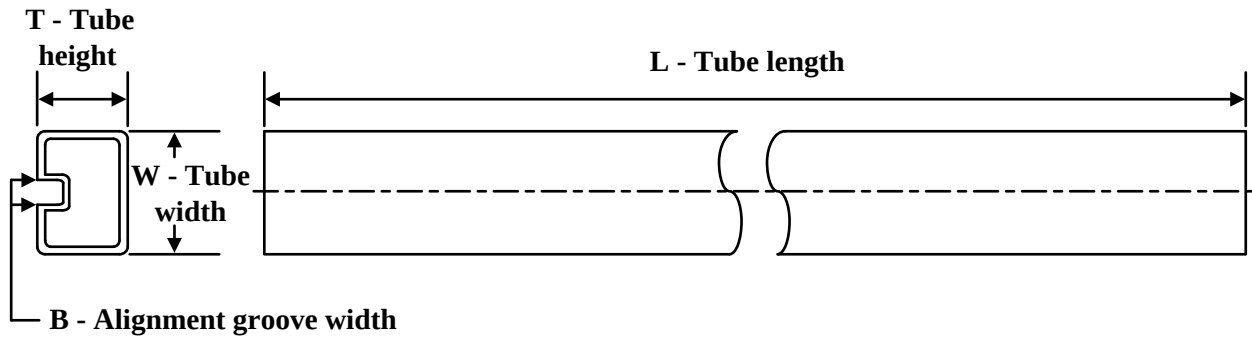
| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 5962-9555001NXDR | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLC339CDR        | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLC339CNSR       | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| TLC339CPWR       | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLC339CPWR       | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLC339IDR        | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLC339IDR1G4     | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| TLC339IPWR       | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLC339IPWR       | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| TLC339MDR        | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



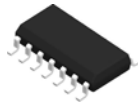
\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 5962-9555001NXDR | SOIC         | D               | 14   | 2500 | 350.0       | 350.0      | 43.0        |
| TLC339CDR        | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| TLC339CNSR       | SOP          | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| TLC339CPWR       | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| TLC339CPWR       | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| TLC339IDR        | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| TLC339IDR1G4     | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| TLC339IPWR       | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| TLC339IPWR       | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| TLC339MDR        | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |

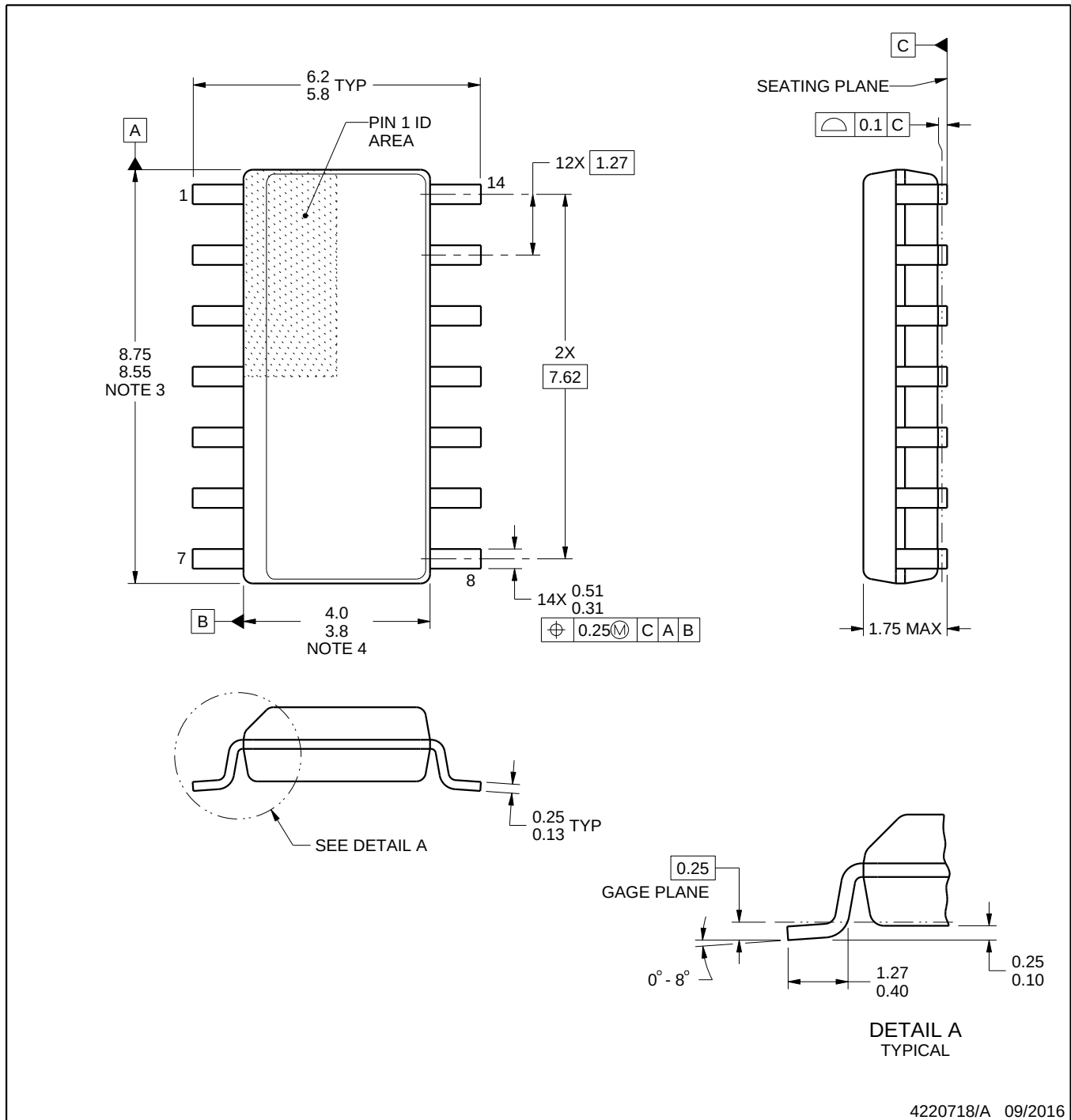
**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87659022A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| TLC139MFKB     | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| TLC139MFKB.A   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| TLC339CN       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| TLC339CN.A     | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| TLC339IN       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| TLC339IN.A     | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| TLC339MN       | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| TLC339MN.A     | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

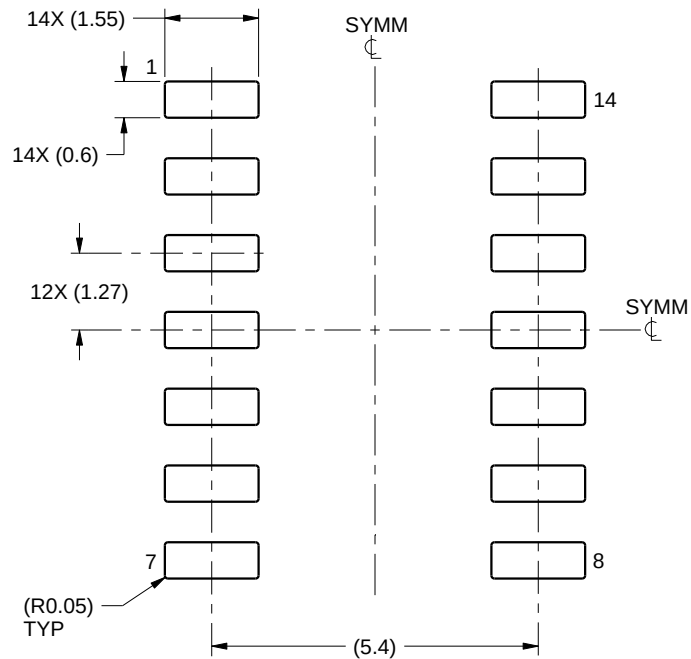
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

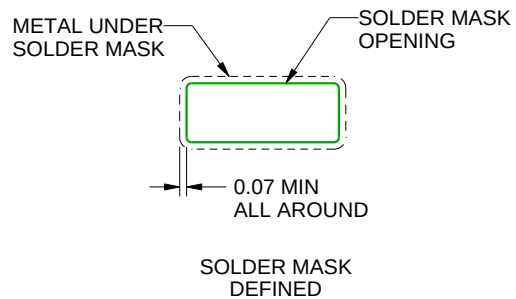
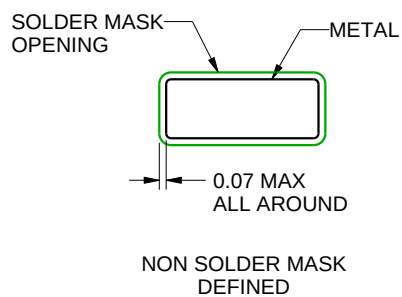
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

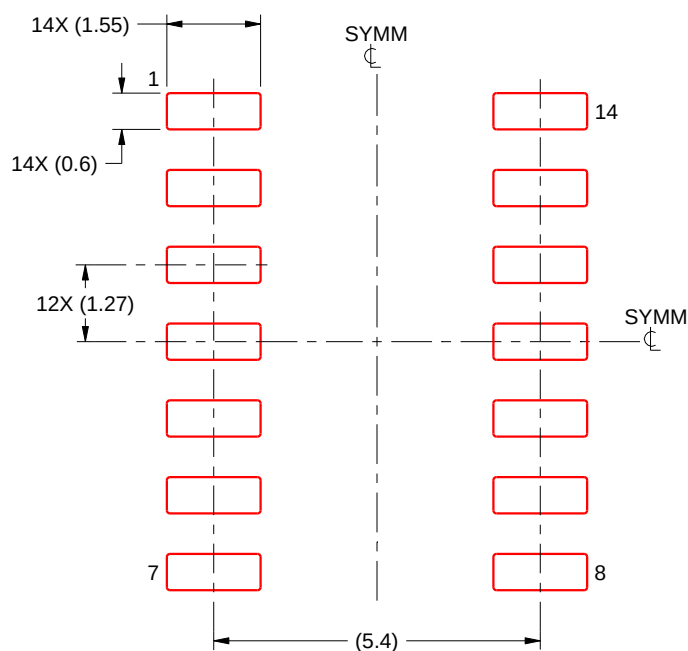
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

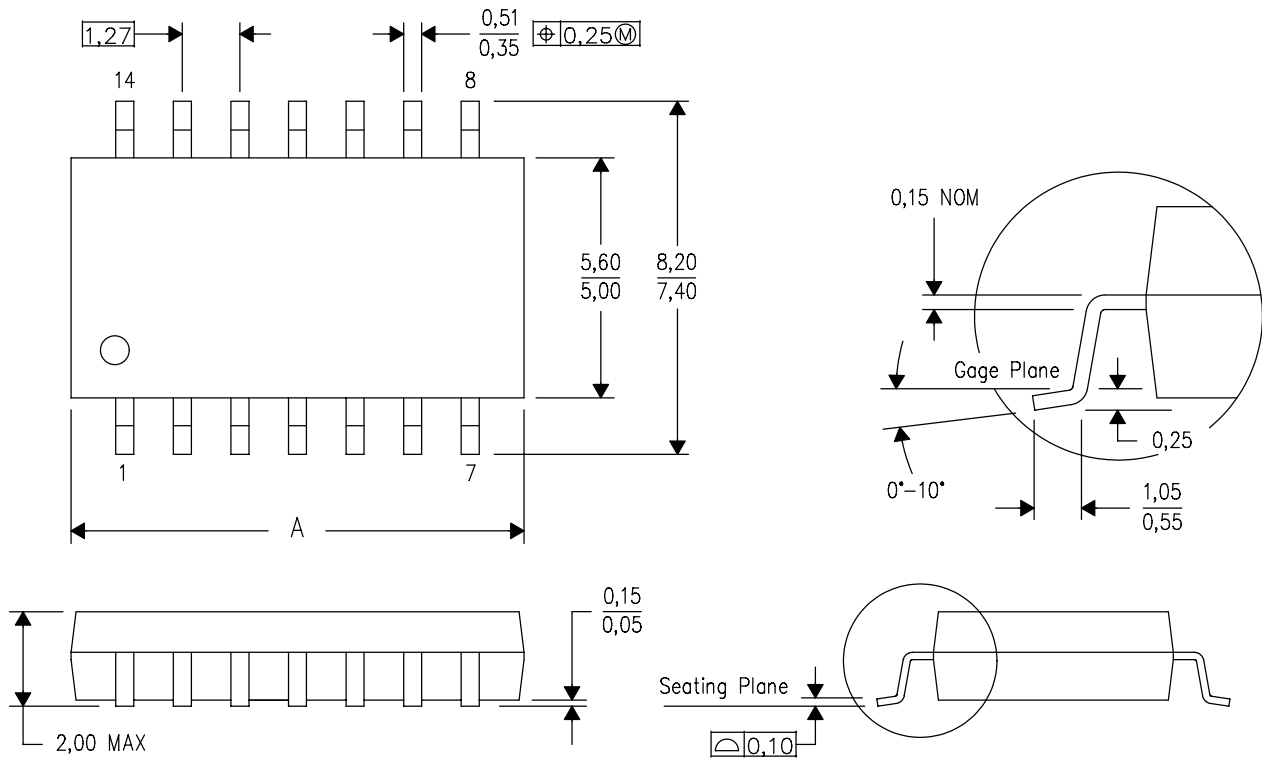
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

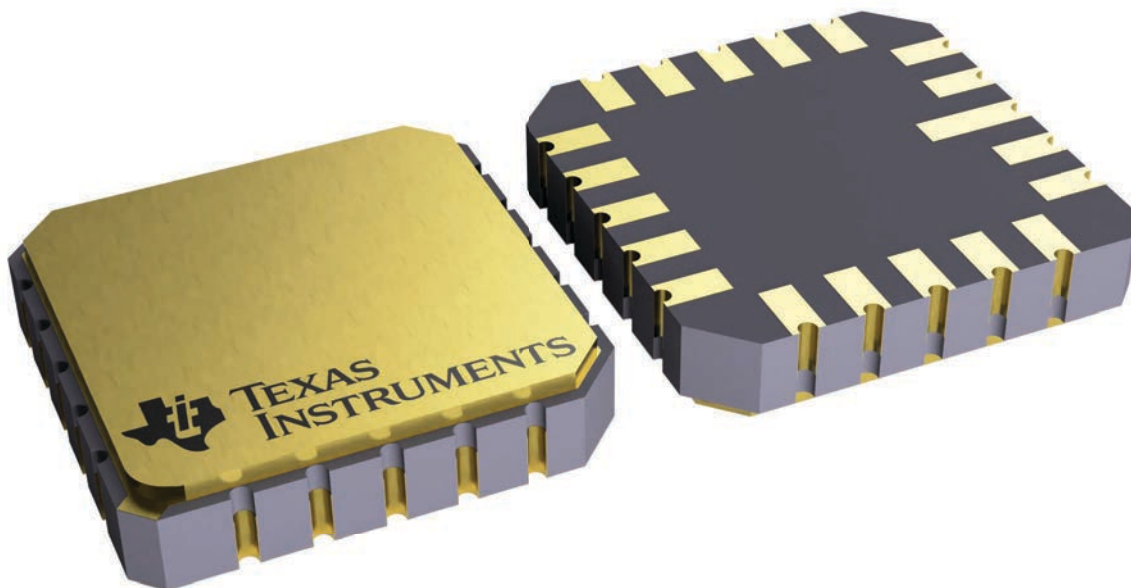
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



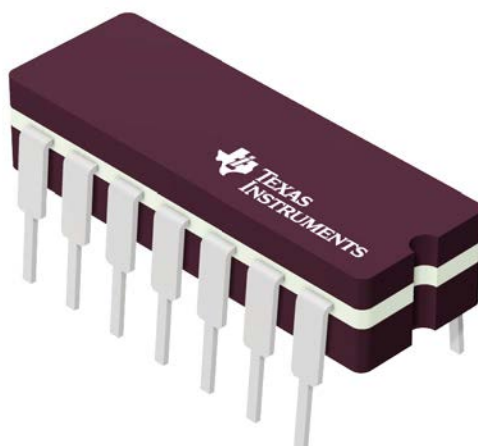
4229370VA\

**J 14**

## GENERIC PACKAGE VIEW

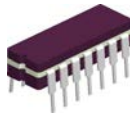
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

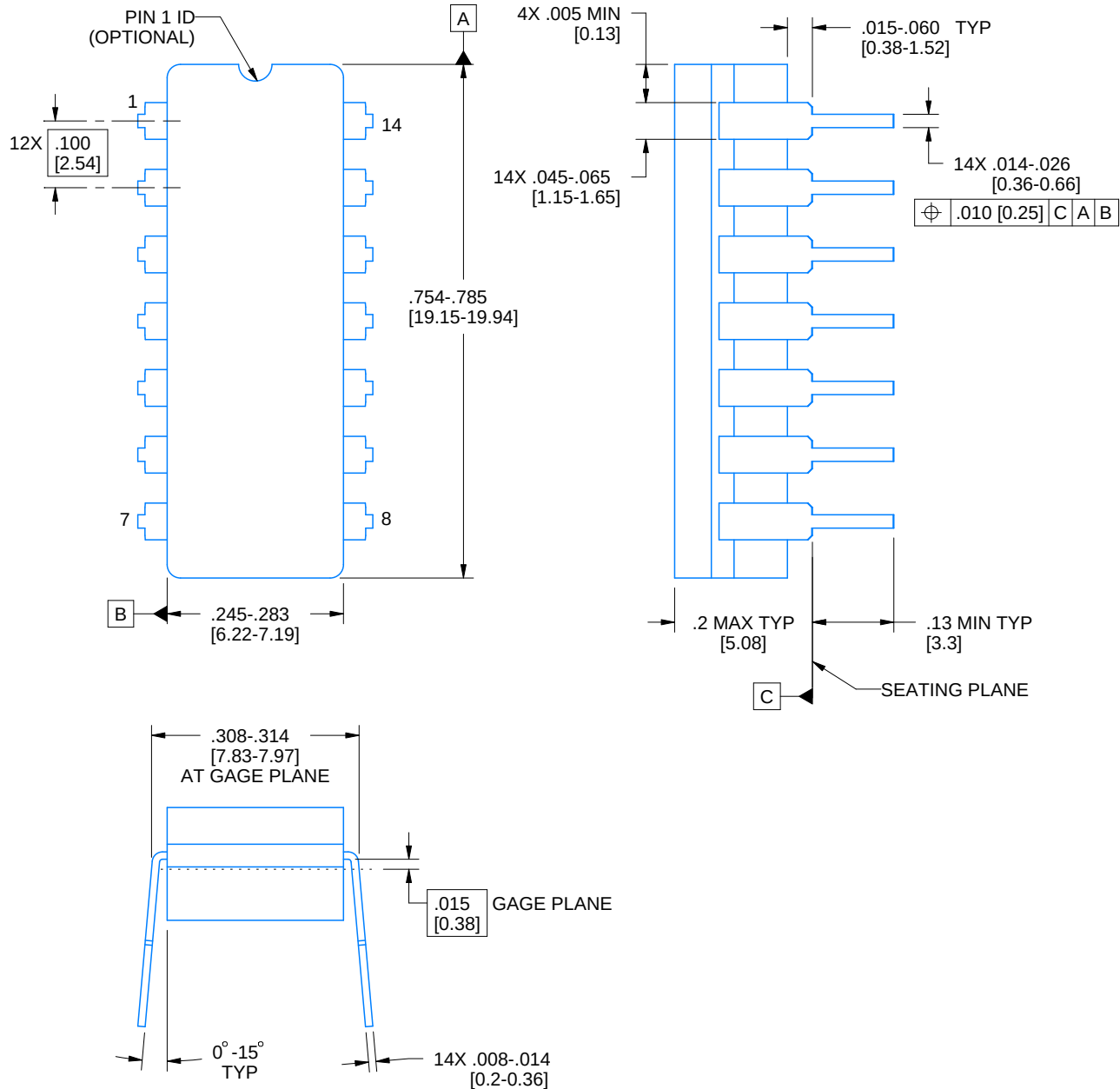


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



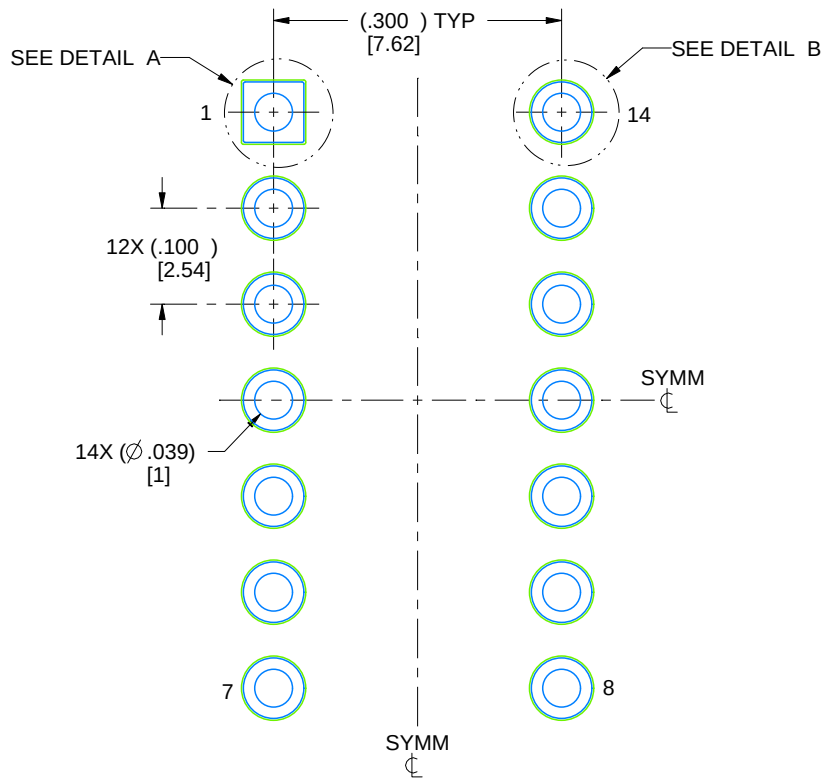
**TEXAS  
INSTRUMENTS**  
www.ti.com

# EXAMPLE BOARD LAYOUT

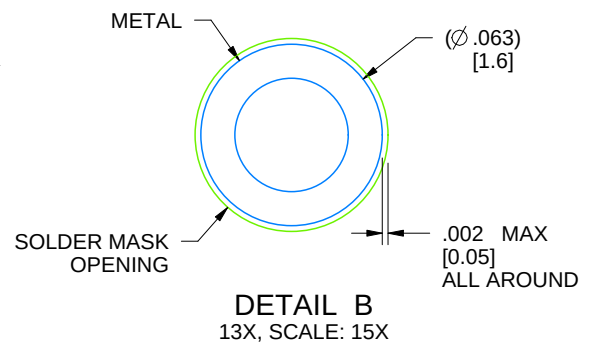
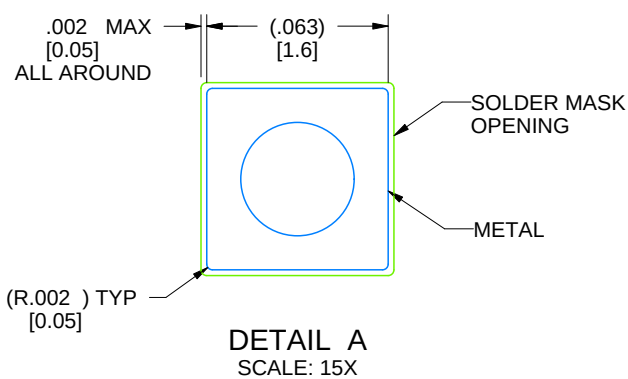
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

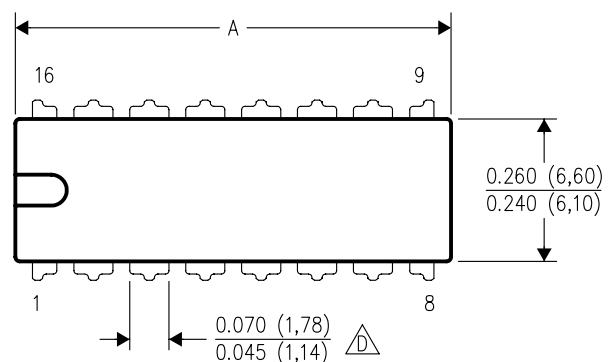


4214771/A 05/2017

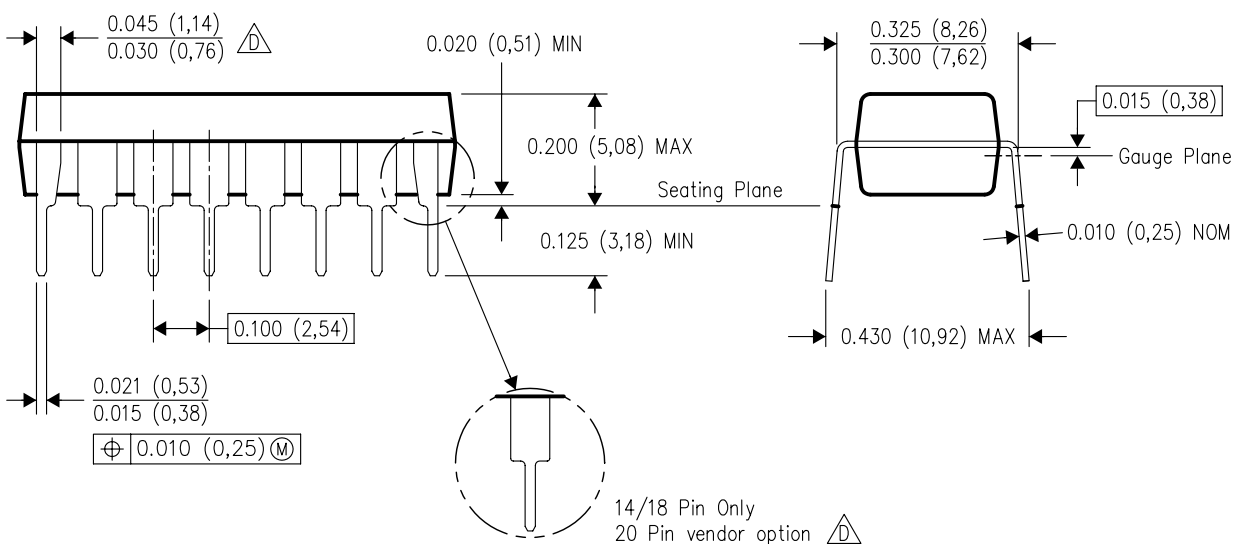
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

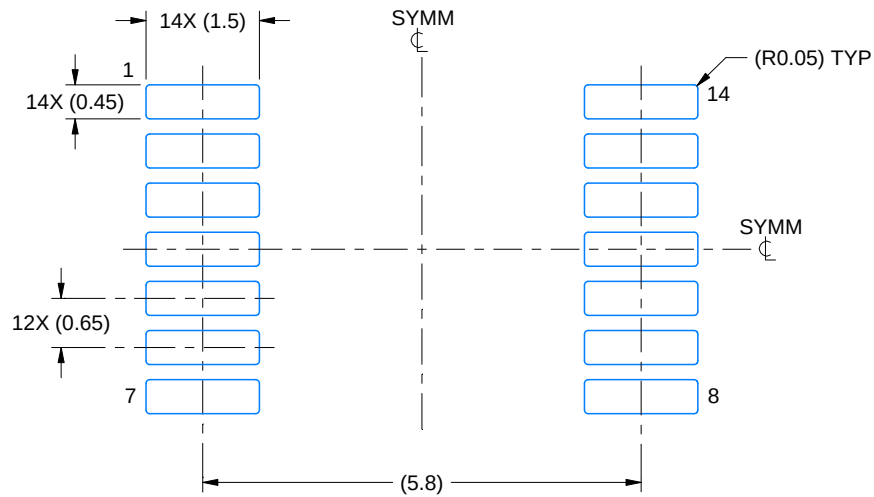


# EXAMPLE BOARD LAYOUT

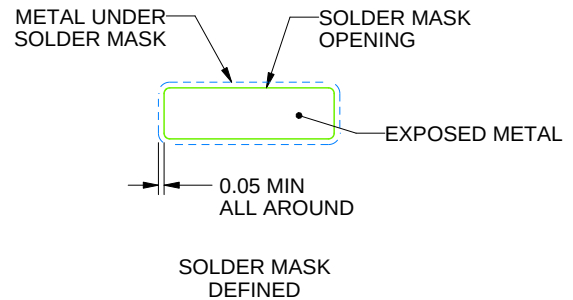
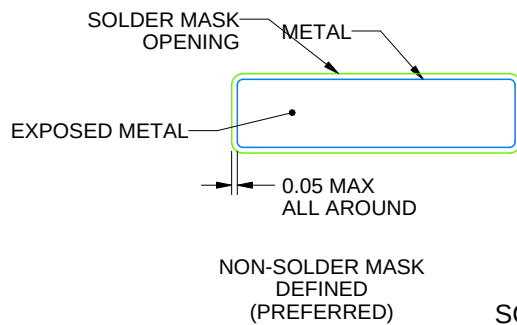
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

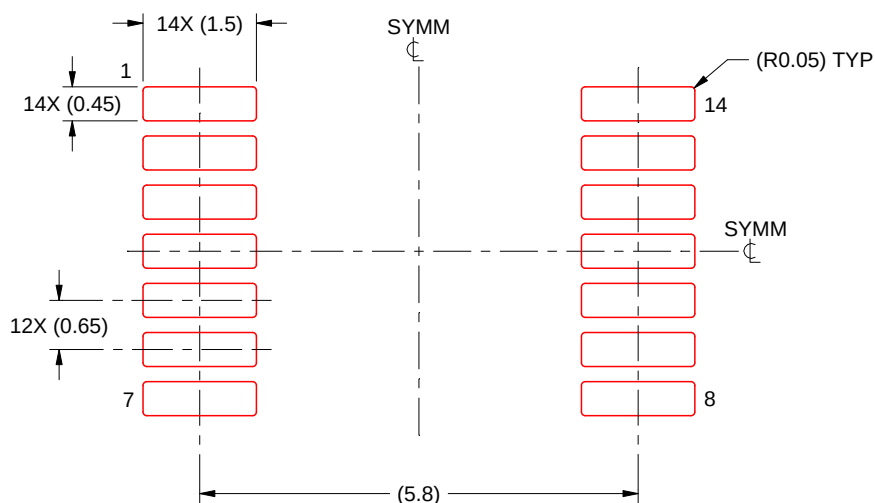
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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