Digital Control Compatible Synchronous Buck Gate Driver with Current Sense Conditioning Amplifier

Check for Samples: UCD7230A

FEATURES

- **Input from Digital Controller Sets Operating Frequency and Duty Cycle**
- **Up to 2-MHz Switching Frequency**
- **Dual Current Limit Protection with Independently Adjustable Thresholds**
- **Fast Current Sense Circuit with Adjustable Blanking Interval Prevents Catastrophic Current Levels**
- **Digital Output Current Limit Flag**
- **Low Offset, Gain of 48, Differential Current Sense Amplifier**
- **3.3-V, 10-mA Internal Regulator**
- **Dual TrueDrive™ High-Current Drivers**
- **10-ns Typical Rise/Fall Times with 2.2-nF Loads**
- **4.5-V to 15.5-V Supply Voltage Range**

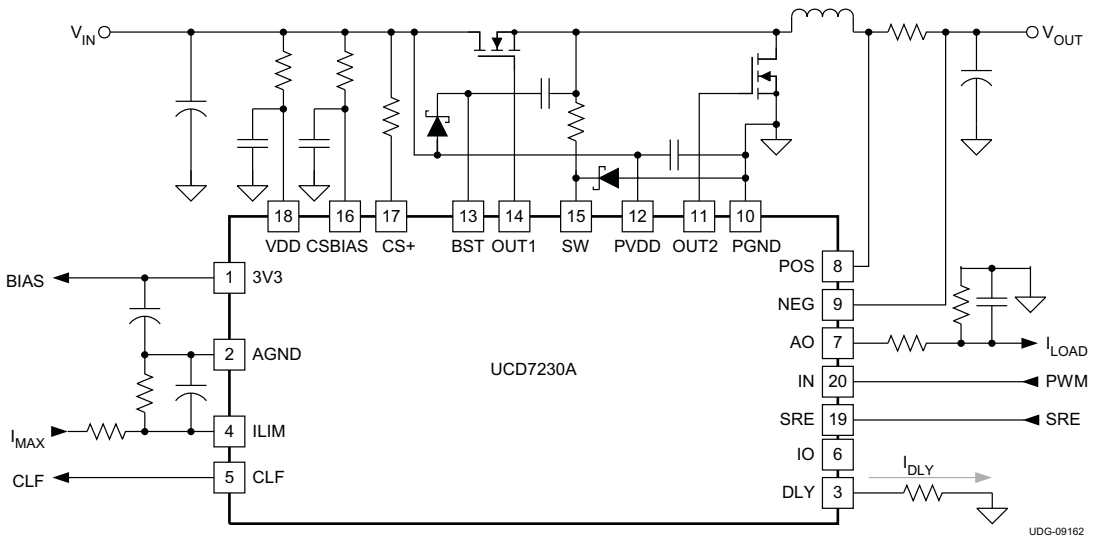
APPLICATIONS

- **Digitally-Controlled Synchronous-Buck Power Stages for Single and Multi-Phase Applications**
- **Especially Suited for Use with UCD91xx or UCD92xx Contollers**
- **High-Current Multi-Phase VRM/EVRD Regulators for Desktop, Server, Telecom and Notebook Processors**
- **Digitally-Controlled Synchronous-Buck Power Supplies Using µCs or the TMS320™ DSP Family**

DESCRIPTION

The UCD7230A is one in the UCD7k family of digital control compatible drivers for applications utilizing digital control techniques or applications requiring fast local peak current limit protection.

The UCD7230A is a MOSFET gate driver specifically designed for synchronous buck applications. It is ideally suited to provide the bridge between digital controllers such as the UCD91xx or the UCD92xx and the power stage. With cycle-by-cycle current limit protection, the UCD7230A device protects the power stage from faulty input signals or excessive load currents.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The UCD7230A includes high-side and low-side gate drivers which utilize Texas Instrument's TrueDrive™ output architecture. This architecture delivers rated current into the gate capacitance of a MOSFET during the Miller plateau region of the switching. Furthermore, the UCD7230A offers a low offset differential amplifier with a fixed gain of 48. This amplifier greatly simplifies the task of conditioning small current sense signals inherent in high efficiency buck converters.

The UCD7230A includes a 3.3-V, 10-mA linear regulator to provide power to digital controllers such as the UCD91xx. The UCD7230A is compatible with standard 3.3-V I/O ports of the UCD91xx, the TMS320™ family DSPs, microprocessors, or ASICs.

The UCD7230A is offered in the space-saving QFN package. Package pin out has been carefully designed for optimal board layout

ORDERING INFORMATION(1) (2)

TEMPERATURE RANGE	PACKAGED DEVICES	PACKAGE QUANTITY	DELIVERY MEDIA	DEVICE NUMBER
-40°C to + 125°C	QFN-20 (RGW)	250	Small tape and reel	UCD7230ARGWT
		3000	Large tape and reel	UCD7230ARGWR

(1) These products are packaged in Pb-Free and green lead finish of Pd-Ni-Au which is compatible with MSL level 1 between 255°C and 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(2) QFN-20 (RGW) package is available taped and reeled only.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VDD		16	V
	BST		V_{SW}+16 V	
Supply current	VDD		20	mA
	OUT1		200	
Output gate drive voltage	OUT1, BST	-1	36	V
	OUT2	-1	V_{VDD}+0.3	
Output gate drive current	OUT1 (sink)		4.0	A
	OUT1 (source)		-2.0	
	OUT2 (sink)		4.0	
	OUT2 (source)		-4.0	
Analog input voltage	SW	-1	20	V
	CS+	-0.3	20	
	CSBIAS	-0.3	16	
	POS, NEG	-0.3	5.6	
	ILIM, DLY, I0	-0.3	3.6	
Analog output	A0	-0.3	3.6	V
Digital I/O's	IN, SRE, CLF	-0.3	3.6	V
Electrostatic discharge, human body model(HBM)			2	kV
Electrostatic discharge, charged device model (CDM)			500	V
Operating junction temperature, T_J		-55	150	°C
Storage temperature, T_{stg}		-65	150	
Lead temperature (soldering, 10 sec)			300	°C

(1) Stresses beyond those listed in this table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult company packaging information for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
	Input voltage	VDD	4.75	12	15	V
	Switching Frequency		200	500	2000	kHz
T_A	Operating ambient temperature		-40		85	°C

DISSIPATION RATINGS TABLE (2 OZ. TRACE AND COPPER PAD WITH SOLDER)(1)

PACKAGE	T_A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T_A = 25°C (mW/°C)	θ_{JA} (°C/W)
20-pin RGW	2.4	24.0	41.7

(1) For more information on the RGW package and the test method, refer to TI technical brief, literature number SZZA017.

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ELECTRICAL CHARACTERISTICS

V_{DD} = P_{VDD} = 12 V, 4.7 µF from V_{DD} to A_{GND}, 1 µF from P_{VDD} to P_{GND}, 0.1 µF from CSBIAS to AGND, 0.22 µF from BST to SW, T_A = T_J = -40°C to +125°C, R_{CS+} = 5 kΩ, R_{DLY} = 50 kΩ over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{VDD}	Supply current, off	V_{DD} = 4.2 V		4	5.2	mA
I_{VDD}	Supply current	Outputs not switching IN = LOW		5	8	mA
LOW-VOLTAGE UNDER-VOLTAGE LOCKOUT						
	VDD UVLO ON	V_{DD} rising	4.25	4.50	4.75	V
	VDD UVLO OFF	V_{DD} falling	4.00	4.25	4.50	
	VDD UVLO hysteresis		100	250	400	mV
REFERENCE / EXTERNAL BIAS SUPPLY						
	3V3 initial set point	T_A = 25°C	3.267	3.3	3.333	V
	3V3 over temperature		3.234	3.3	3.366	
	3V3 load regulation	I_{LOAD} = 1 mA to 10 mA, V_{DD} = 5V		1	7	mV
	3V3 line regulation	V_{DD} = 4.75 V to 12 V, I_{LOAD} = 10 mA		3	10	
	Short circuit current	V_{DD} = 4.75 V to 12 V	11	20		mA
	3V3 OK threshold, ON	3.3 V rising	2.8	3	3.2	V
	3V3 OK threshold, OFF	3.3 V falling	2.6	2.8	3.0	
INPUT SIGNAL (IN)						
INHigh	Positive-going input threshold voltage		1.6	1.9	2.2	V
INLow	Negative-going input threshold voltage		1.0	1.3	1.6	
INHigh – INLow	Input voltage hysteresis		0.4	0.6	0.8	
	Input resistance to AGND		50	100	150	kΩ
	Frequency ceiling		2			MHz
t_{MIN}	PWM minimum pulse width to force OUT1 gate pulse	C_{LOAD} = 2.2 nF, V_{DD} = 12 V	120			ns
CURRENT LIMIT (ILIM)						
	ILIM internal voltage setpoint	V_{ILIM}= OPEN	0.47	0.50	0.53	V
	ILIM input impedance		20	42	65	kΩ
	CLF output high level	I_{LOAD} = 4 mA	2.7			V
	CLF output low level	I_{LOAD} = 4 mA			0.6	
	Propagation delay from IN to reset CLF	2nd IN rising to CLF falling after a current limit event		15	35	ns
CURRENT SENSE COMPARATOR (OUTPUT SENSE)						
V_{CS}	CS threshold (POS - NEG)	V_{ILIM} = open	40	50	60	mV
		V_{ILIM} = 3.3 V	80	100	120	
		V_{ILIM} = 0.75 V	60	75	90	
		V_{ILIM} = 0.25 V	15	25	35	
	Propagation delay from POS to OUT1 falling (1)	V_{ILIM} = open, V_{CS} = threshold + 60 mV		90		ns
	Propagation delay from POS to CLF (1)	V_{ILIM} = open, V_{CS} = threshold + 60 mV		100		

(1) As designed and characterized. Not 100% tested in production.

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ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = P_{VDD} = 12 V, 4.7 µF from V_{DD} to A_{GND}, 1 µF from P_{VDD} to P_{GND}, 0.1 µF from CSBIAS to AGND, 0.22 µF from BST to SW, T_A = T_J = -40°C to +125°C, R_{CS+} = 5 kΩ, R_{DLY} = 50 kΩ over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE COMPARATOR (INPUT SENSE)						
	CS threshold	R_{DLY} = 24.3 kΩ (CSBIAS-CS+)	170	235	300	mV
		R_{DLY} = 49.9 kΩ (CSBIAS-CS+)	90	114	140	
	CS blanking time(2)	R_{DLY} = 24.3 kΩ , IN rising to OUT1, IN falling to OUT2, VDD = 6 V		120		ns
		R_{DLY} = 49.9 kΩ , IN rising to OUT1, IN falling to OUT2, VDD = 6 V		230		
	R_{DELAY} range(2)		24.3	50.0	100.0	kΩ
	Propagation delay from CS+ to OUT1(2)	V_{CS} = threshold + 60 mV		80		ns
	Propagation delay from CS+ to CLF(2)			70		
CURRENT SENSE AMPLIFIER						
V_{OO}	Output offset voltage	I0 = OPEN; (V_{POS} = V_{NEG})= 1.25 V; measure AO - IO	-100	0	100	mV
	Closed loop dc gain	I0 = FLOAT; V_{POS} = 1.26 V; V_{NEG} = 1.25 V, R_{POS} = R_{NEG} = 0 C	46	48	50	V/V
	Input impedance	V_{POS} = 1.25 V, V_{NEG} = 1.29 V, R = (V_{POS} - V_{NEG}) / (I_{POS} - I_{NEG})	5.5	8.3	12	kΩ
V_{CM}	Input Common Mode Voltage Range	$V_{CM(max)}$ is limited to (V_{DD}-1.2V), R_{POS} = 0	0.3		5.6	V
A0_Vol	Minimum Output Voltage	V_{POS} = 1.2 V; V_{NEG} = 1.3 V; A0_I_{SINK} = 250 µA		0.15	0.3	V
A0_Voh	Maximum Output Voltage	V_{POS} =1.3 V; V_{NEG} = 1.2 V; A0_ I_{SOURCE} = 500 µA	3	3.1	3.5	
	Input Bias Current, POS or NEG	I0 = FLOAT; V_{POS} = V_{NEG} = 0.8 V to 5.0 V, R_{POS} = R_{NEG} = 0 V	-2		30	µA
ZERO CURRENT REFERENCE (IO)						
	Reference voltage	Measured at I0	0.54	0.6	0.66	V
	Input transition voltage	With respect to IO reference	10	60	120	mV
I_O	Output impedance	I_{ZERO} = 0.6 V	10	15	21	kΩ

(2) As designed and characterized. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = P_{VDD} = 12 V, 4.7 µF from V_{DD} to A_{GND}, 1 µF from P_{VDD} to P_{GND}, 0.1 µF from CSBIAS to AGND, 0.22 µF from BST to SW, T_A = T_J = -40°C to +125°C, R_{CS+} = 5 kΩ, R_{DLY} = 50 kΩ over operating free-air temperature range (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-SIDE OUTPUT DRIVER (OUT2)					
Source current(3)	V_{DD} = 12 V, IN = high, V_{OUT2} = 5 V		2.2		A
Sink current (3)	V_{DD} = 12 V, IN = low, V_{OUT2} = 5 V		3.5		
Source current(3)	V_{DD} = 4.75 V, IN = high, V_{OUT2} = 0		1.6		
Sink current (3)	V_{DD} = 4.75 V, IN = low, V_{OUT2} = 4.75 V		2		
Rise time(3)	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		15		ns
Fall time(3)	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		15		
Output with VDD <UVLO	V_{DD} = 1.0 V, Isink = 10 mA		0.8	1.2	V
Propagation delay from IN to OUT2(3)	C_{LOAD} = 2.2 nF, IN rising, SW = 2.5 V, BST = PVDD = VDD = 12 V		30		ns
HIGH-SIDE OUTPUT DRIVER (OUT1)					
Source current(3)	V_{DD} = 12 V, BST = 12 V IN = High, V_{OUT1} = 5 V		1.7		A
Sink current (3)	V_{DD} = 12 V, BST = 12 V IN = Low, V_{OUT1} = 5 V		3.5		
Source current (3)	V_{DD} = 4.75 V = BST = 4.75 V, IN = High, V_{OUT1} = 0		1		
Sink current (3)	V_{DD} = 4.75 V, BST = 4.75 V, IN = Low, V_{OUT1} = 4.75 V		2.4		
Rise time(3)	C_{LOAD} = 2.2 nF OUT1 to SW, VDD = 12 V		20		ns
Fall time (3)	C_{LOAD} = 2.2 nF OUT1 to SW, V_{DD} = 12 V		15		
Propagation delay from IN to OUT1(3)	C_{LOAD} = 2.2 nF, IN falling, SW = 2.5 V, BST = PVDD = VDD = 12 V		30		

(3) As designed and characterized. Not 100% tested in production.

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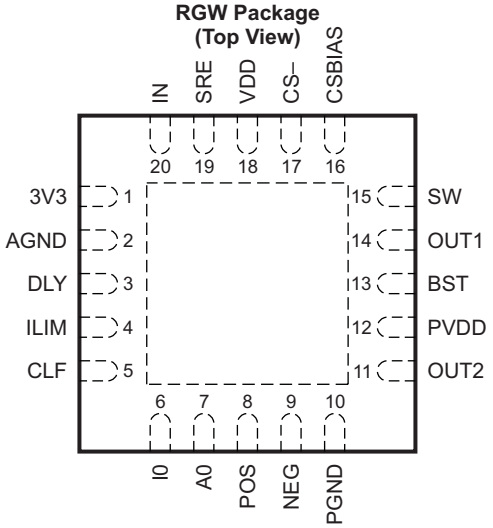
DEVICE INFORMATION



TERMINAL FUNCTIONS

NAME	No.	I/O	DESCRIPTION
3V3	1	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Bypass with 0.22-µF ceramic capacitance from this pin to analog ground, AGND.
AO	7	O	Current sense linear amplifier output. The output voltage level on this pin represents the average output current. Any value below the level on the I0 pin represents negative output current.
AGND	2	-	Analog ground return.
BST	13	I	Floating OUT1 driver supply powered by an external Schottky diode from the PVDD pin during the synchronous MOSFET on time.
CLF	5	O	Current Limit Flag. The CLF signal is a 3.3-V digital output which is latched high after an over current event, triggered by either of the two current sense comparators and reset after two rising edges received on the IN pin. CLF is also asserted on power-up while VDD is below the UVLO threshold. CLF goes low when VDD crosses the UVLO threshold.
CSBIAS	16	I	Supply pin for the high-side current sense comparator.
CS+	17	I	Non-inverting Input for the high side current sense comparator. A resistor connected between this pin and the high side MOSFET drain, in conjunction with the DLY resistor sets the high-side current limit threshold.
DLY	3	I	Requires a resistor to AGND for setting the current sense blanking time for both the high-side and low-side current sense comparators. The value of this resistor in conjunction with the resistor in series with the CS+ pin sets the high side current sense threshold.
ILIM	4	I	Output current limit threshold set pin. The output current threshold is 1/10th of the value set on this pin. If left floating the voltage on this pin is 0.55 V. The voltage on the ILIM pin can range from 0.25 V to 1V to set the threshold from 25 mV to 100 mV.
IN	20	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. A Schmitt trigger input comparator desensitizes this pin from external noise.
IO	6	I	Sets the current sense linear amplifier “Zero” output level. The default value is 0.6 V which allows negative current measurement.
OUT1	14	I	The high-side high-current TrueDrive™ driver output. Drives the gate of the high-side buck MOSFET between SW and BST.
OUT2	11	I	The low-side high-current TrueDrive™ driver output. Drives the gate of the low-side synchronous MOSFET between PVDD and PGND.
NEG	9	I	Inverting input of the output current sense amplifier and current limit comparator.
PGND	10	-	Power ground return. This pin should be connected close to the source of the low-side synchronous rectifier MOSFET.
POS	8	I	Non-inverting input of the output current sense amplifier and current limit comparator.
PPAD	PAD	–	Thermal pad. Connect directly to AGND for thermal performance and EMI reduction.
PVDD	12	-	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. The bypass capacitor for this pin should be returned to PGND.

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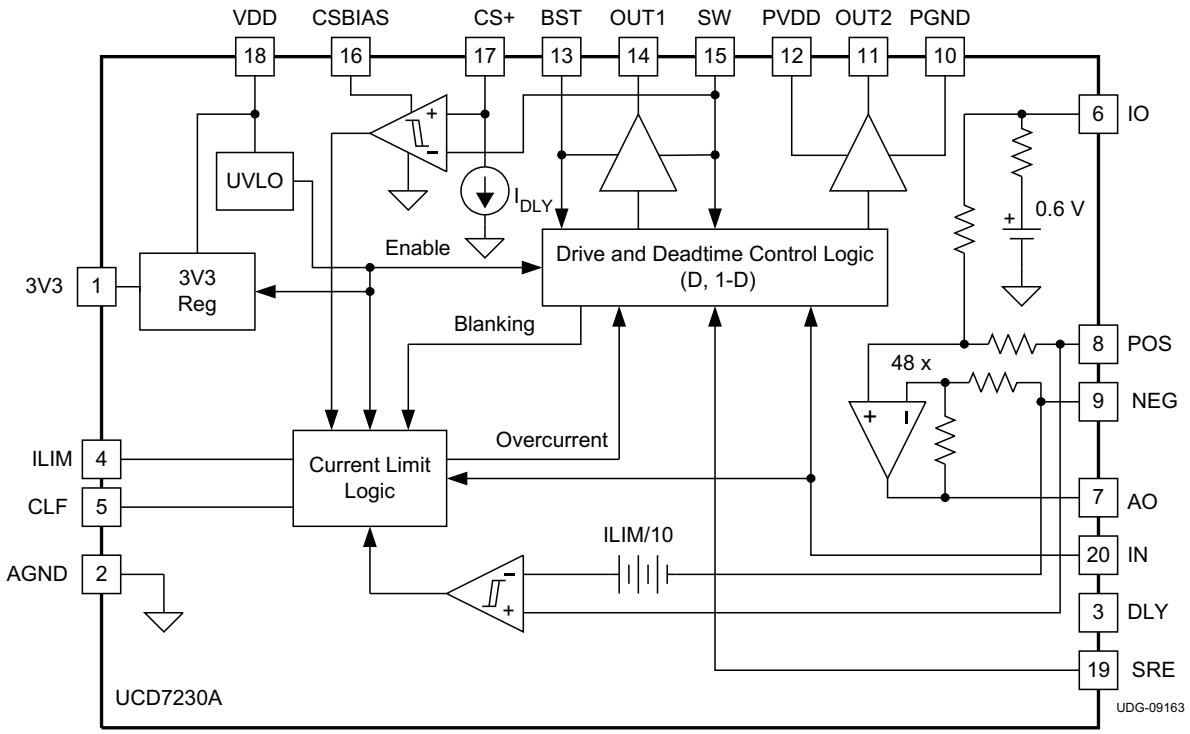
TERMINAL FUNCTIONS (continued)

NAME	No.	I/O	DESCRIPTION
SRE	19	I	Synchronous Rectifier Enable. The SRE pin is a high impedance digital input capable of accepting 3.3-V logic level signals, used to disable the synchronous rectifier switch. The synchronous rectifier is disabled when this signal is low. A Schmitt trigger input comparator desensitizes this pin from external noise.
SW	15	I/O	OUT1 gate drive return and square wave input to output inductor.
VDD	18	-	Supply input pin to power the internal circuitry except the driver outputs. The UCD7230A accepts an input range of 4.5 V to 15.5 V.

FUNCTIONAL BLOCK DIAGRAM



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APPLICATION INFORMATION

Introduction

The UCD7230A is a synchronous buck driver with peak-current limiting. It is a member of the UCD7K family of digital compatible drivers suitable either for applications utilizing digital control techniques or analog applications that require local fast peak current limit protection.

In systems using the UCD7230A, the feedback loop is closed externally and the IN signal represents the PWM information required to regulate the output voltage. The PWM signal may be implemented by either a digital or analog controller.

The UCD7230A has two over-current protection features, one that limits the peak current in the high-side switch and one that limits the output current. Both limits are individually programmable. The internal current sense blanking enables ease of design with real-world signals. In addition to over current limit protection, current sense signals can be conditioned by the on board amplifier for use by the system controller.

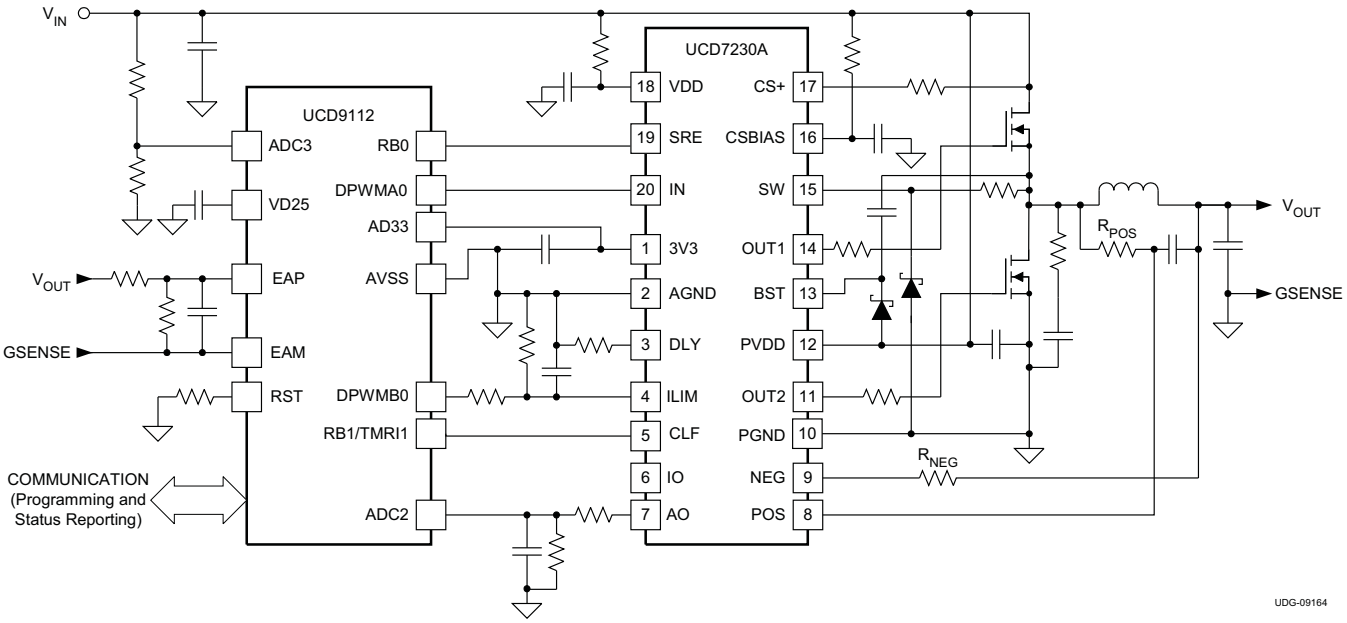

Figure 1. Single-Phase Synchronous Buck Converter using UCD9112 and one UCD7230A

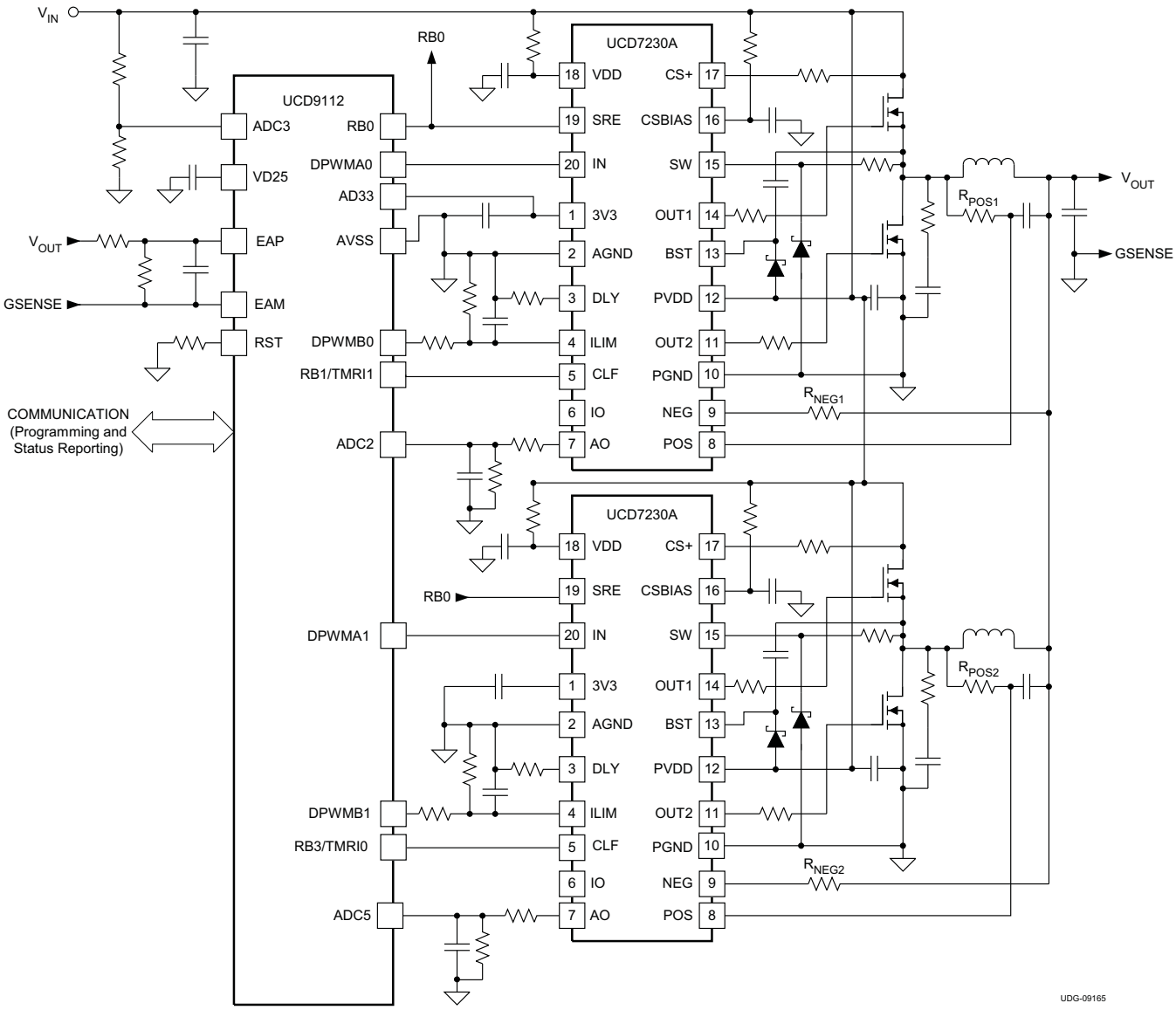

Figure 2. Multi-Phase Synchronous Buck Converter using UCD9112 and two UCD7230A

Supply Requirements

The UCD7230A operates on a supply range of 4.5 V to 15.5 V. The supply voltage should be applied to three pins, PVDD, VDD, and CSBIAS. PVDD is the supply pin for the lower driver, and has the greatest current demands. The supply connection to PVDD is also the point where an external Schottky diode provides current to the high side flying driver. PVDD should be bypassed to PGND with a low ESR ceramic capacitor. In the same fashion, the flying driver should be bypassed between BST and SW.

VDD and CSBIAS are less demanding supply pins, and should be resistively coupled to the supply voltage for isolation from noise generated by high current switching and parasitic board inductance. Use a value of 10 Ω for CSBIAS and 1 Ω for VDD. VDD should be bypassed to AGND with a 4.7-μF ceramic capacitor while CSBIAS should be bypassed to AGND with 0.1 μF. Although the three supply pins are not internally connected, they must be biased to the same voltage. It is important that all bypassing be done with low parasitic inductance techniques to good ground planes.

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PGND and AGND are the ground return connections to the chip. Ground plane construction should be used for both pins. For a MOSFET driver operating at high frequency, it is critical to minimize the stray inductance to minimize overshoot, undershoot, and ringing. The low output impedance of the drivers produces waveforms with high di/dt. This induces ringing in the parasitic inductances. It is highly desirable that the UCD7230A and the MOSFETs be collocated. PGND and the AGND pins should be connected to the PowerPAD™ of the package with two thin traces. It is critical to ensure that the voltage potential between these two pins does not exceed 0.3 V.

Although quiescent VDD current is low, total supply current depends on the gate drive output current required for the capacitive load and the switching frequency. Total supply current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from (I_{OUT} = Qg x f), where f is the operating frequency.

Reference / External Bias Supply

The UCD7230A includes a series pass regulator to provide a regulated 3.3 V at the 3V3 pin that can be used to power other circuits such as the UCD91xx, a microcontroller or an ASIC. 3V3 can source 10 mA of current. For normal operation, place a 0.22-µF ceramic capacitor between 3V3 and AGND.

Control Inputs

The IN and SRE pins are high impedance digital inputs designed for 3.3-V logic-level signals. They both have 100-kΩ pull-down resistors. Schmitt Trigger input stage design immunizes the internal circuitry from external noise. IN is the command input for the upper driver, OUT1, and can function up to 2 MHz. SRE controls the function of the lower driver, OUT2. When SRE is false (low), OUT2 is held low. When SRE is true, OUT2 is inverted from OUT1 with appropriate delays that preclude cross conduction in the Buck MOSFETs.

Driver Stages

The driver outputs utilize Texas Instruments' TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed, during the Miller plateau region of the switching transition. This provides best switching speeds and reduces switching losses. TrueDrive™ consists of pull-up/ pull-down circuits using bipolar and MOSFET transistors in parallel. This hybrid output stage also allows relatively constant current sourcing even at reduced supply voltages.

The low-side high-current output stage of the UCD7230A device is capable of sourcing 1.7-A and sinking 3.5-A current pulses and swings from PVDD to PGND. The high-side floating output driver is capable of sourcing 2.2-A and sinking 3.5-A peak-current pulses. This ratio of gate currents, common to synchronous buck applications, minimizes the possibility of parasitic turn on of the low-side power MOSFET due to dv/dt currents during the rising edge switching transition. See the typical curves of sink and source current in Figure 3 and Figure 4 .

If further limiting of the rise or fall times to the power device is desired, an external resistance can be added between the output of the driver and the power MOSFET gate. The external resistor also helps remove power dissipation from the driver.

Driver outputs follow IN and SRE as previously described provided that VDD and 3V3 are above their respective under-voltage lockout thresholds. When the supplies are insufficient, the chip holds both OUT1 and OUT2 low.

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It is worth reiterating the need mentioned in the supply section for sound high frequency design techniques in the circuit board layout and bypass capacitor selection and placement. Some applications may generate excessive ringing at the switch-inductor node. This ringing can drag SW to negative voltages that might cause functional irregularities. To prevent this, carefull board layout and appropriate snubbing are essential. In addition, it may be appropriate to couple SW to the inductor with a 1-Ω resistor, and then bypass SW to PGND with a low impedance Schottky diode.

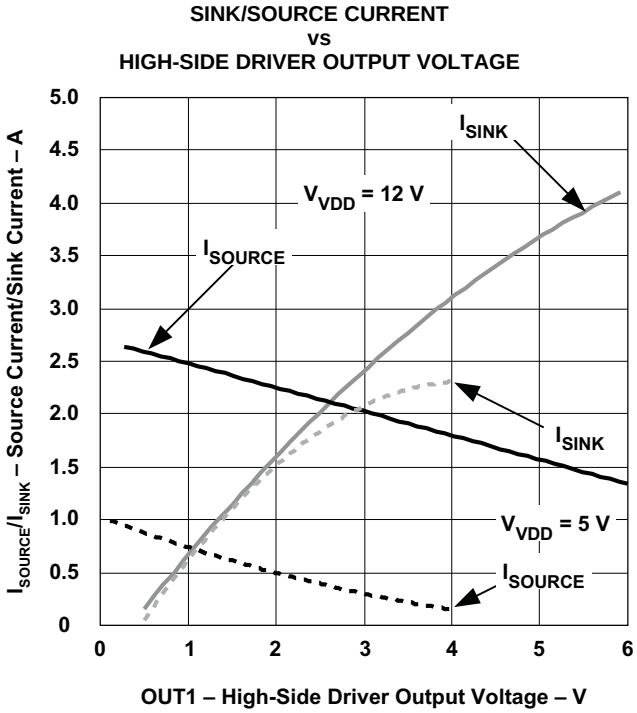

Figure 3.

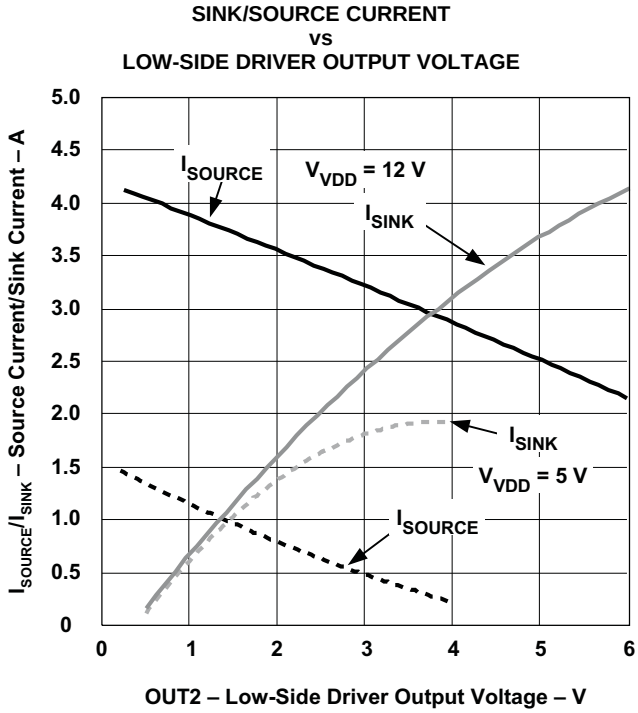

Figure 4.

Current Sensing and Overload Protection

Since the UCD7230A is physically collocated with the high-current elements of the power converter, it is logical that current be monitored by the chip. An internal instrumentation amplifier conditions current sense signals so that they can be used by the control chip generating the PWM signal.

POS and NEG are inputs to an instrumentation amplifier circuit. This amplifier has a nominal gain of 48 and presents its output at AO. This can be used to monitor either an external current sense shunt or a parallel RC around the buck inductor shown in Figure 5. The shunt yields the highest accuracy and is insensitive to inductor core saturation effects. It comes with the price of added power dissipation. Using the shunt, AO is calculated in Equation 1.

$$AO = \left(48 \times I_{OUT} \times R_{SHUNT}\right) + IO \tag{1}$$

The internal configuration of the instrumentation amplifier is such that AO is 0.6 V when POS – NEG = 0. Because of this output offset, the amplifier can accurately pass information for both positive and negative load current. The offset is controlled by IO. If IO is left to float, the offset is 0.6 V. 0.6 V is present at IO through an internal 10-kΩ resistor and should be bypassed to AGND. If a higher value of offset is desired, a voltage in excess of 0.66 V can be externally applied to IO. Once IO is forced above 0.66 V, the internal 10 kΩ is disconnected, and the AO output offset is now equal to the voltage applied to IO.

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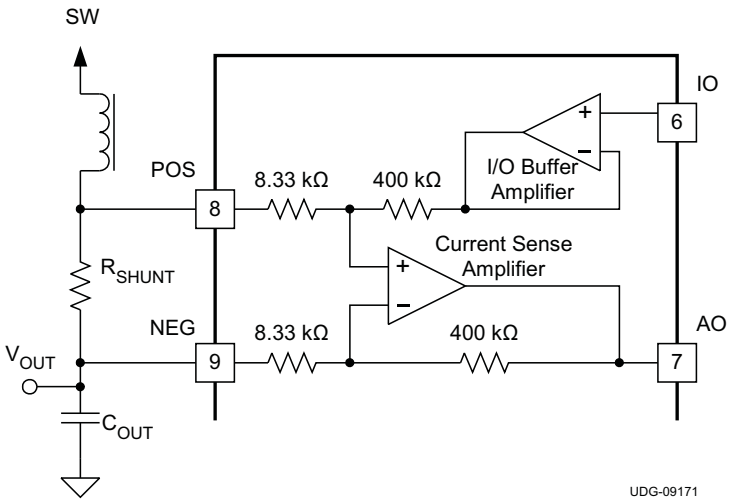

Figure 5. Current Sense Using External Shunt

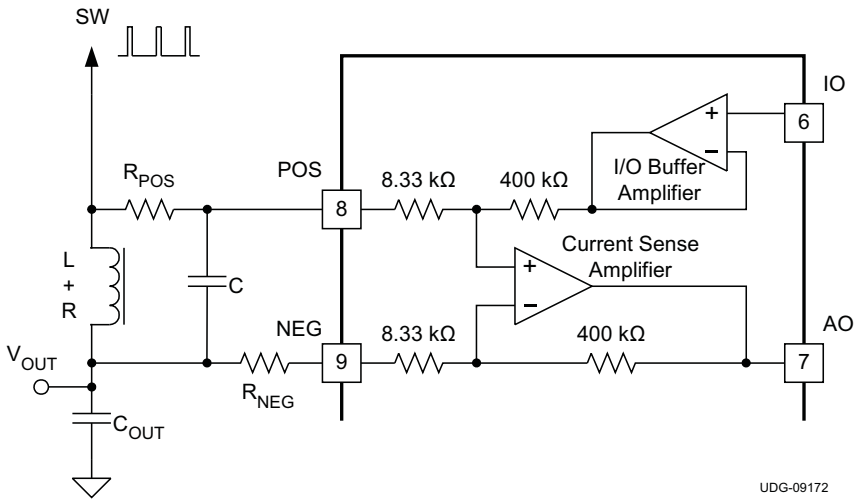

Figure 6. Lossless Average Output Current Sensing Using DC Resistance of the Output Inductor

Figure 6 also shows lossless current sensing utilizing an RC across the buck inductor to generate an analog of the IR drop in the copper of the inductor. As long as the R_{POS} x C time constant is the same as the L/R of the inductor and its parasitic equivalent series resistance, then the voltage on C is the same as the IR drop on the parasitic inductor resistance. A resistor, $R_{NEG} = R_{POS}$ is used for amplifier bias current cancellation. The transfer function of the amplifier is calculated in Equation 2.

$$AO = \left(A \times I_{OUT} \times R_{COPPER}\right) + IO \tag{2}$$

With the addition of R_{POS} and R_{NEG}, the natural gain, A, of the current sense is predictably decreased as shown in Equation 3.

$$A = \frac{48}{1 + \left(\frac{R_{POS}}{8.33\,k\Omega}\right)} \tag{3}$$

For R_{POS} << 8.33 kΩ, the gain is 48. While the 400 kΩ and 8.33 kΩ are well matched, it is important to keep R_{POS} as small as possible since they have absolute variation from chip-to-chip and over temperature. The graph in Figure 7 shows the band of expected gain for A as a function of R_{POS}. The gain variation at R_{POS} = 1 kΩ results in around ±4% error. However, the tolerance of the value of R in the inductor has a more significant effect on measurement accuracy as does the temperature coefficient of R. Copper has a temperature coefficient of approximately 3800 ppm/°C. For a 100°C rise in winding temperature, the dc resistance of the inductor increases by 38%. The worst case scenario would be a cracked core or under-designed inductor in which cases the core could tend towards saturation. In that scenario, inductor current could change slope drastically and is not correctly modeled by the capacitor voltage.

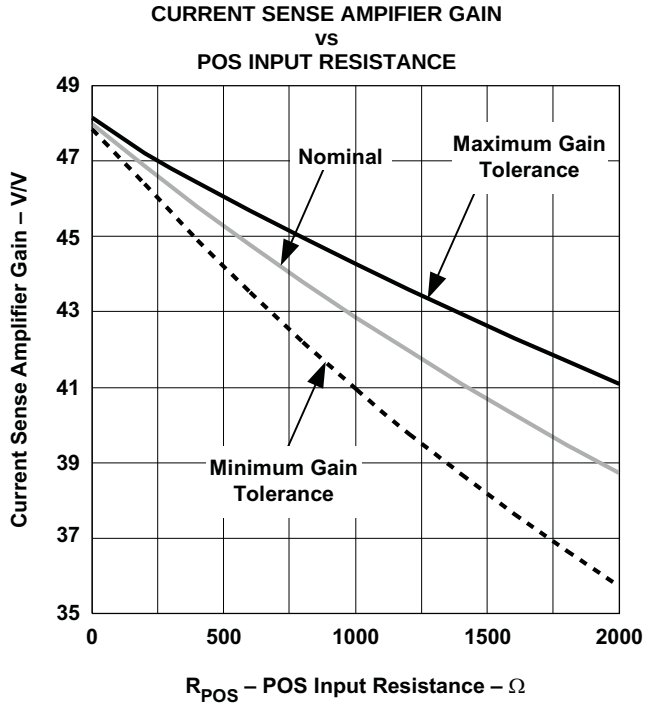

Figure 7. Current Sense Amplifier Gain as a Function of R_{POS}

The RC time constant is . The LR time constant is shown in Equation 5.

$$t_{RC} = R_{POS} \times C \tag{4}$$

$$t_{LR} = \frac{L}{R} \tag{5}$$

When Equation 4 equals Equation 5, the voltage across the capacitor is the same as the voltage drop across the equivalent resistance of the inductor. If the time constraints don't match, (Equation 4 does not equal Equation 5) the calculation of the ripple current amplitude can be incorrect. Load transients result in overshoot when t_{RC} is much shorter than t_{LR}. Load transients result in undershoot when t_{RC} is much longer than t_{LR}.

While the amplifier faithfully passes the sensed dc current signal, it should be noted that the amplifier is bandwidth limited for normal switching frequencies. Therefore, AO represents a moving average of the sensed current.

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The amplifier output can go up to 3.3 V, so reasonable designs limit full scale to 3.0 V. Should attenuation be necessary, use a resistive divider between AO and the control chip A/D input as shown in Figure 8.

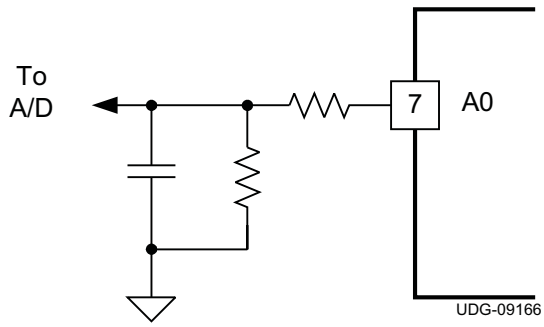

Figure 8. Attenuating and Filtering the Voltage Representation of the Average Output Current

While the current sense amplifier is useful for accurate current monitoring or controlling overload conditions, extreme overload conditions must be handled in timeframes that are generally much shorter than the A/D of a control chip can achieve. Therefore, there are two comparators on the UCD7230A to sense extreme overload and protect the driven power MOSFETs.

Extreme current overload is handled in two ways by the UCD7230A. One is a comparator that monitors the voltage between POS and NEG, or effectively the output current of the converter.. The other is a comparator that monitors the voltage drop across the high-side MOSFET, or effectively the input current. Should either condition exceed a preset value, OUT1 is immediately turned off for the remainder of the cycle.

To program the high-side MOSFET current limit threshold, a value of resistance from DLY to AGND must first be chosen to establish a blanking time during which the comparator outputs are ignored or blanked. Blanking is required because the high amplitude ringing that occurs on the rising edge of SW would otherwise cause false triggering of the fault comparators. The required amount of blanking time is a function of the switching speed of the high-side FET, the PCB layout, and whether or not a snubber network is being used. A value of 100ns after the rising edge of SW is a typical starting point. In the UCD7230A, the blanking interval timing begins at the rising edge of IN. Due to propagation delays and anti-cross-conduction intervals, there is approximately 45ns delay from the rising edge of IN to the rising edge of SW. This propagation delay must be added to the required amount of blanking time after the rising edge of SW when calculating the overall blanking time.

The overall blanking time is calculated in Equation 6.

$$t_{BLANK}(ns) \approx 5 \times R_{DLY}(k\Omega) \tag{6}$$

where

- R_{DLY} is the resistor from DLY to AGND

R_{DLY} should be limited to a range between 25 kΩ and 100 kΩ. The blanking interval should be kept as short as possible, consistent with reliable fault detection. The blanking interval (minus the 45-ns propagation delay) sets the minimum duty cycle pulse width where high-side fault detection is possible. When the on-time of the IN pulses are narrower than the blanking time, the high-side fault detection comparator is held off for the entire on-time and is, therefore, blind to any high-side faults.

Once R_{DLY} has been chosen, the value of R_{CS+} can be calculated. R_{CS+} is the resistor from the CS+ pin to the drain of the high-side FET which sets the high-side fault detection threshold. When the high-side FET is on, the current flow in the FET produces a voltage drop across the device. The magnitude of this voltage is equal to the $R_{DS(on)}$ times the current through the FET. An absolute maximum current level can be set during the design stage and the resultant voltage drop across the FET can be calculated. This maximum voltage drop, ΔV_{MAX}, sets the high-side fault threshold.

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Internally, a high-speed comparator monitors the voltage between the SW pin and the CS+ pin when the high-side FET is on. Whenever the voltage on the SW pin is lower than the voltage on the CS+ pin, a fault is flagged. To prevent false tripping during the ringing that accompanies the rising edge of SW, the output of the comparator is held off (blanked) for a time interval set by the DLY pin. The voltage on the CS+ pin is set by a resistor connected from the pin to the high-side FET drain. The R_{CS+} resistor value is calculated from Equation 7.

$$R_{CS+} = \frac{\Delta V_{MAX} \times R_{DLY}}{1200} \tag{7}$$

where

- ΔV_{MAX} is in mV
- R_{CS+} and R_{DLY} are in kΩ

For example, if ΔV_{MAX} is 100 mV and R_{DLY} is 50 kΩ, then R_{CS+} is 4.2 kΩ.

Equation 7 can be restated as Equation 8.

$$R_{CS+} = \frac{\left(R_{DS(on)HOT} \times I_{MAX}\right) \times R_{DLY}}{1200} \tag{8}$$

where

- I_{MAX} is the peak current flowing through the high-side FET when it is on
- R_{CS+} and R_{DLY} in kΩ
- $R_{DS(on)}$ in mΩ
- I_{MAX} is in amperes

I_{MAX} is the sum of the load current and one half of the inductor ripple current. As a general rule, the value of I_{MAX} should be set to about 150% of the expected maximum steady-state load current. This allows some headroom to avoid nuisance fault events due to transient load currents and the inductor ripple current. With low inductor values and lower switching frequencies, the magnitude of the inductor ripple current can be quite high. Be certain to account for it in the I_{MAX} calculation. Also, keep in mind that the $R_{DS(on)}$ of a FET has a large positive temperature coefficient of approximately 4000 ppm/°C. The junction temperature of the FET is elevated when operating at currents near the I_{MAX} threshold. In Equation 9, use a value of $R_{DS(on)HOT}$ that is approximately 140% of its typical room temperature value. Note that the FET, when turned on, is driven to a VGS enhancement voltage of approximately the value of VDD. Most FET data sheets provide $R_{DS(on)}$ values for VGS values of 4.5 V and 10 V. Most manufacturers provide a graph of $R_{DS(on)}$) vs VGS. If provided, use the graph with the value of VGS = VDD to determine the room temperature $R_{DS(on)}$ value.

A current sink proportional to R_{DLY} pulls current through R_{CS+}. This sets up a reference voltage drop equal to ΔV_{MAX}. It is important to connect the far end of the R_{CS+} resistor directly to the drain of the high-side FET. This should be made with a separate, non-current-carrying trace. This ensures that only the $R_{DS(on)}$ of the FET influences the fault threshold voltage and not the resistance of the PC board traces.

The blanking time for the output comparator is identical to the input comparator. The output comparator threshold is calculated in Equation 9.

$$V_{CS(out)} = \frac{V_{ILIM}}{10} \tag{9}$$

where

- $V_{CS(out)}$ is the threshold of allowed voltage between the POS and NEG pins
- V_{ILIM} is the voltage on the ILIM pin

Note that the ILIM is internally connected to 0.5 V through a 42-kΩ resistor. Any voltage between 0.25 V and 1.0 V can be applied to ILIM. For voltages above 1.0 V, the maximum $V_{CS(OUT)}$ threshold is clamped to 0.1 V. Possible methods for setting ILIM are shown in Figure 9.

When using the output comparator to monitor the voltage on the parallel sensing capacitor across the inductor, the same caveats apply as described for the current sense amplifier.

Figure 9 through Figure 12 show different methods of setting the current limit voltage. Table 1 lists the current limit value settings when using the GPIO outputs as show in Figure 9 only.

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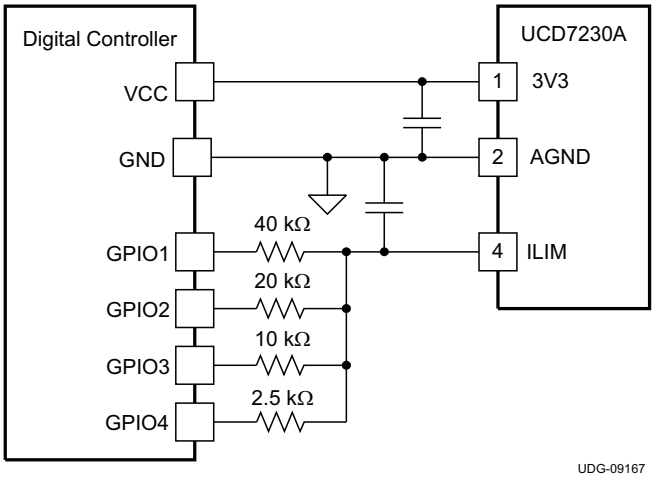

Figure 9. Setting the ILIM Voltage GPIO Outputs

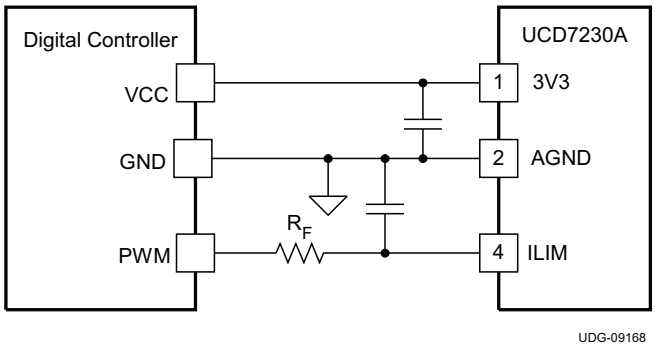

Figure 10. Setting the ILIM Voltage Using a PWM Output

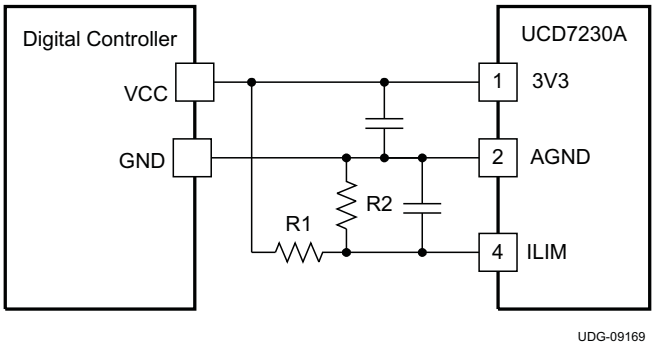

Figure 11. Setting the ILIM Voltage Using a Resistor Divider

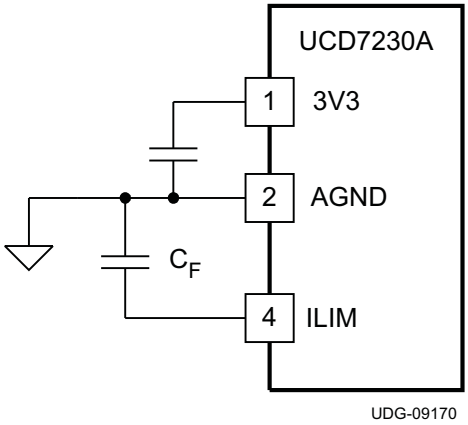

Figure 12. Setting the ILIM Voltage Using an Internal Setpoint

Table 1. Current Limit Value Settings

	CURRENT LIMIT (ILIM) SETPOINT (mV)	GPIO3	GPIO2	GPIO1	GPIO4
ILIM (open)	500	OPEN	OPEN	OPEN	OPEN
ILIM0	0	0	0	1	0
ILIM1	140	0	0	0	0
ILIM2	290	0	1	1	0
ILIM3	430	0	1	0	0
ILIM4	570	1	0	1	0
ILIM5	720	1	0	0	0
ILIM6	860	1	1	1	0
ILIM7	1000	1	1	0	0

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If either comparator threshold is exceeded, OUT1 is immediately turned off for the remainder of the cycle and CLF is asserted true. Upon the rising edge of IN, the switches resume normal operation, but the CLF assertion is maintained. If a fault is not detected in this switching cycle, then the next rising edge of IN removes the CLF assertion. However, if one of the comparators detects a fault, then CLF assertion continues. The control device monitors CLF and decides how to handle the fault condition. During this monitoring period, the protection comparators protect the power MOSFET switches on a cycle-by-cycle basis. If the output-sense comparator (POS - NEG) detects continuous overcurrent, then the driver assumes 0% duty cycle until the current drops to a safe value. Note that when a fault condition causes OUT1 to be driven low, OUT2 behaves as if the input pulse had been terminated normally. In some fault conditions, it is advantageous to drive OUT2 low. SRE can be used to cause OUT2 to remain low at the discretion of the control chip. This can be used to achieve faster discharge of the inductor and also to fully disconnect the converter from the output voltage.

Startup Handshaking

The UCD7230A has a built-in handshaking feature to facilitate efficient start-up of the digitally controlled power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the device are within their operating range. Once the supply voltages are within acceptable limits, CLF goes low and the device processes input commands. The digital controller should monitor CLF at start-up and wait for CLF to go low before sending pwm information to the UCD7230A.

Thermal Management

The usefulness of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be used over a particular temperature range, the package must allow for the efficient removal of the heat while keeping the junction temperature (T_J) within rated limits. The UCD7230A is available in the QFN package with an exposed pad that removes thermal energy from the semiconductor junction.

As illustrated in Reference [3 & 4], the QFN package offers a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the θ_{JA}. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [3].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device. The PowerPAD™ should be connected to the quiet ground (AGND) of the circuit.

REFERENCES

1. Power Supply Seminar SEM-1600 Topic 6: *A Practical Introduction to Digital Power Supply Control*, by Laszlo Balogh, Texas Instruments Literature No. SLUP224
2. Power Supply Seminar SEM–1400 Topic 2: *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, Texas Instruments Literature No. SLUP133.
3. Application Report, *Quad Flatpack No-Lead Logic Packages*, Texas Instruments Literature No. SCBA017
4. Application Report, *QFN/SON PCB Attachment*, Texas Instruments Literature No. SLUA271

RELATED PRODUCTS

DEVICE	DESCRIPTION	Literature Number
UCD9240	Digital PWM System Controller	SLUS766C
UCD9220	Digital PWM System Controller	SLUS904
UCD9112	Digital Dual-Phase Synchronous Buck Controller	SLVS711

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD7230ARGWT	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD 7230A
UCD7230ARGWT.A	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD 7230A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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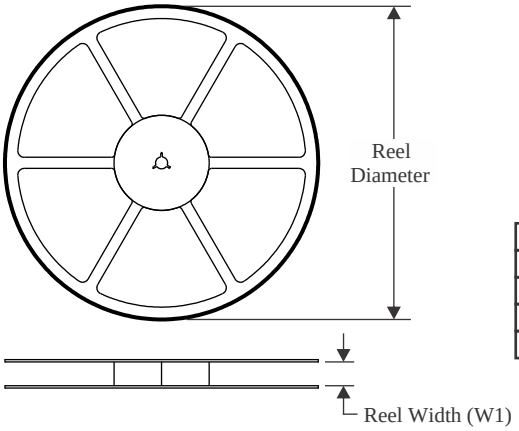
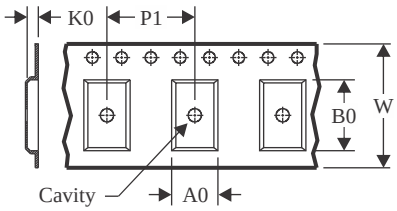
TAPE AND REEL INFORMATION

REEL DIMENSIONS

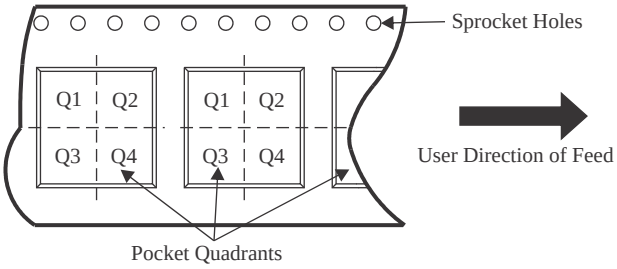


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

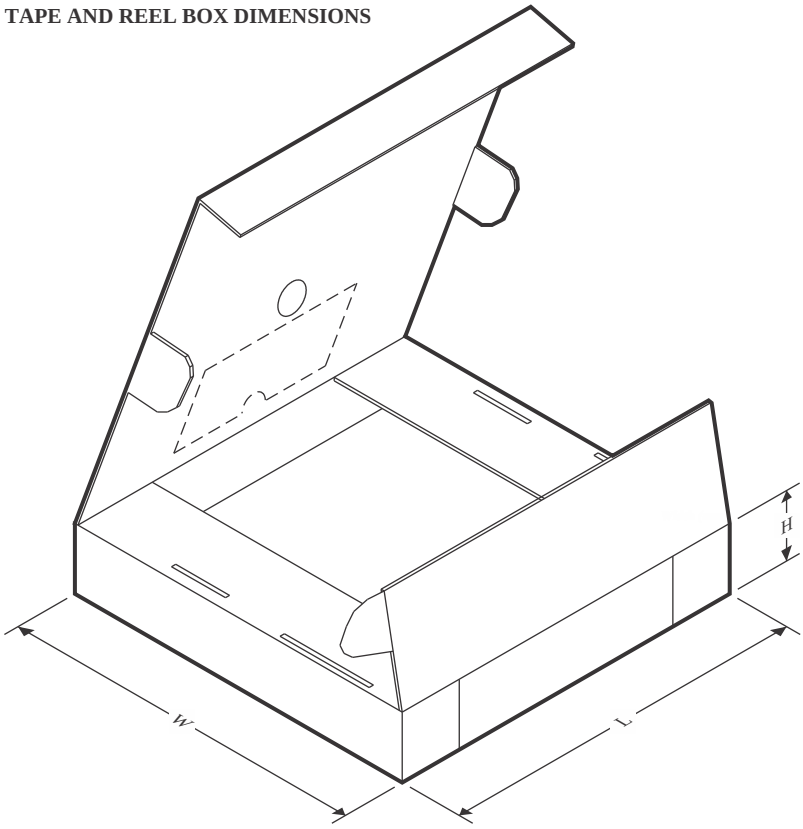
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD7230ARGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD7230ARGWT	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

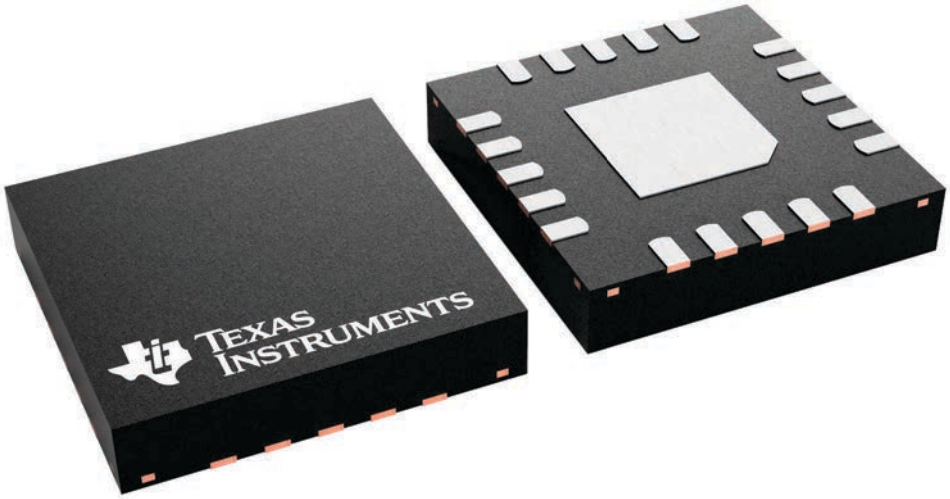
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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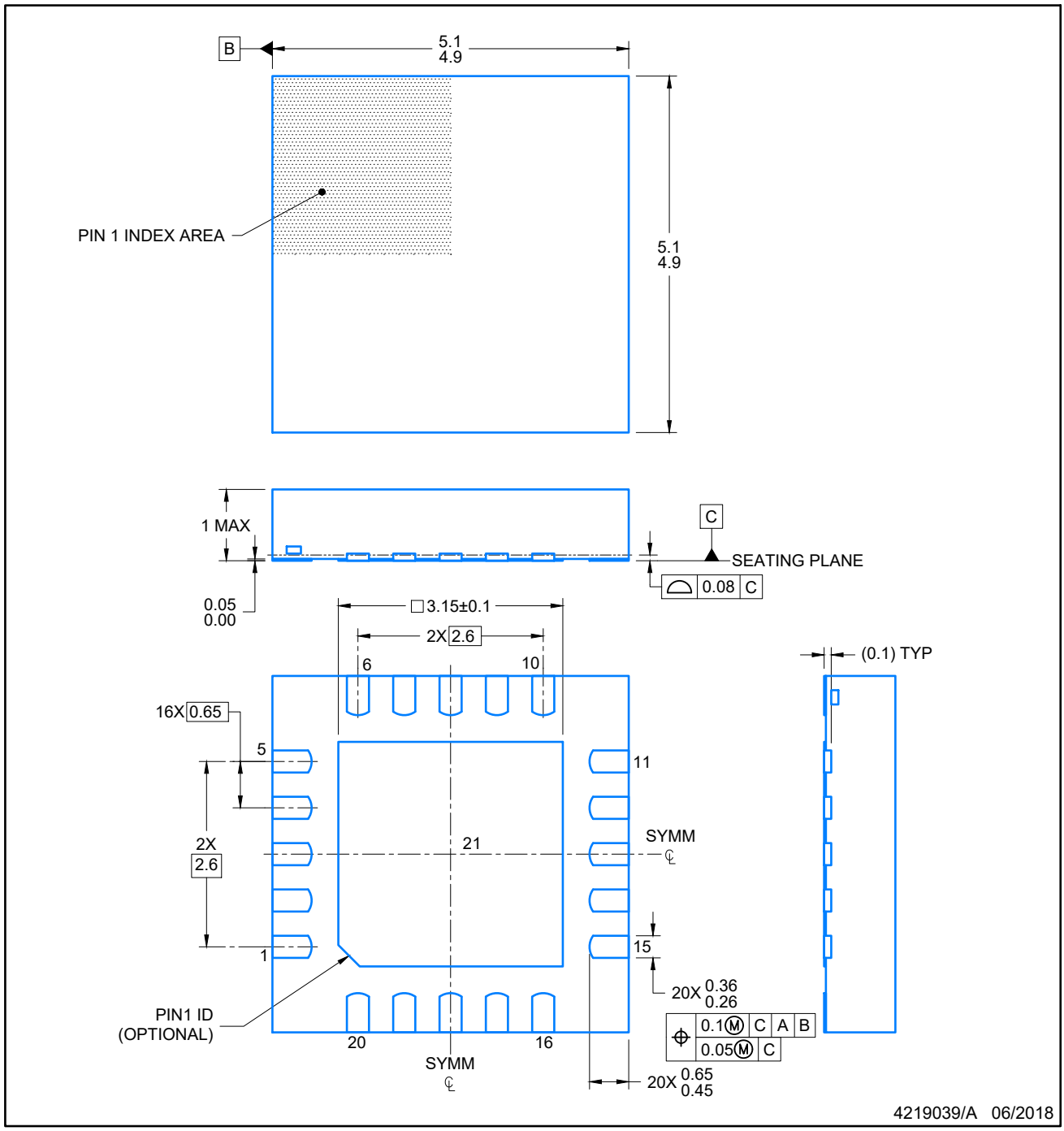
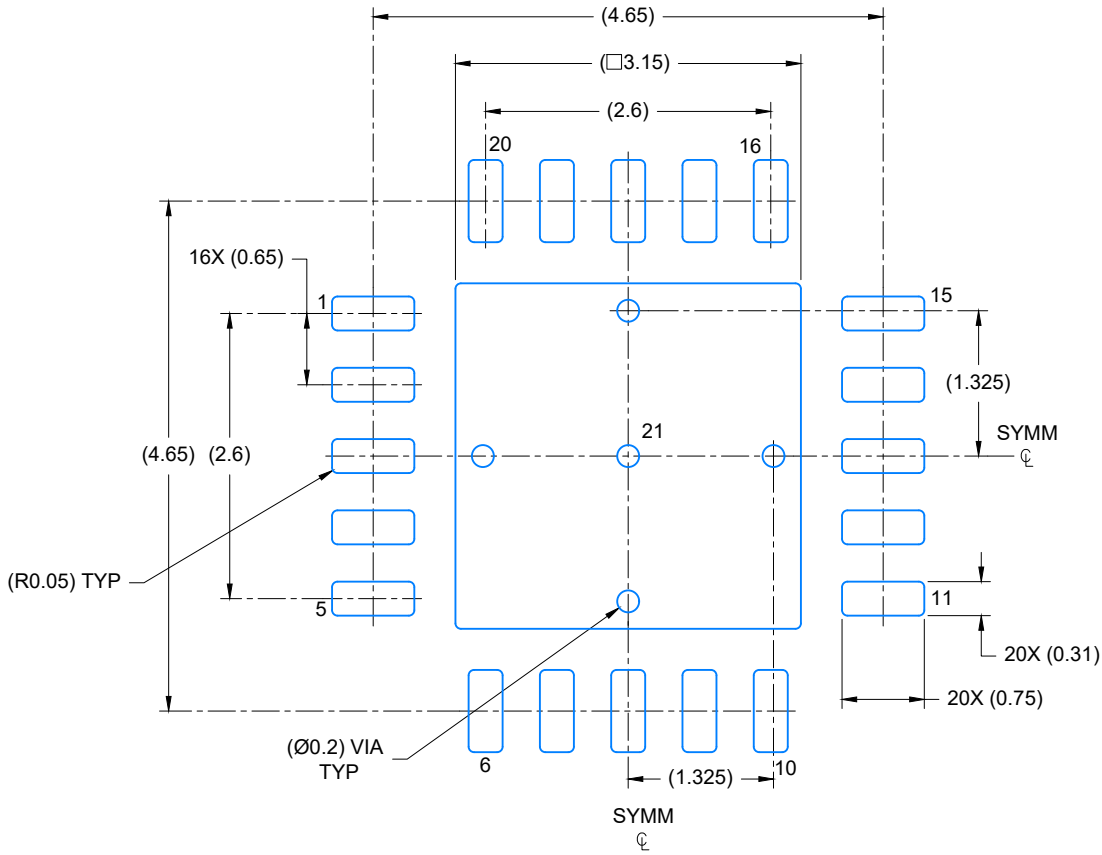
PLASTIC QUAD FLATPACK-NO LEAD



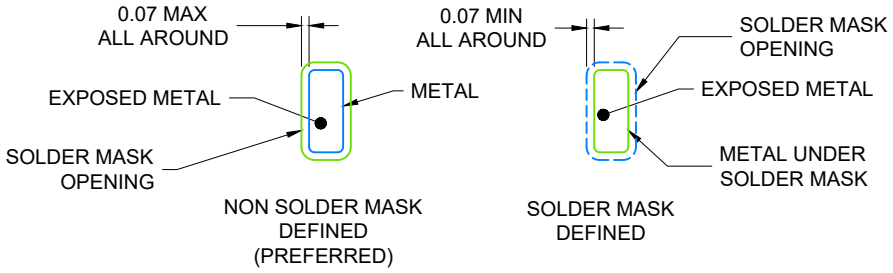
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X



SOLDER MASK DETAILS

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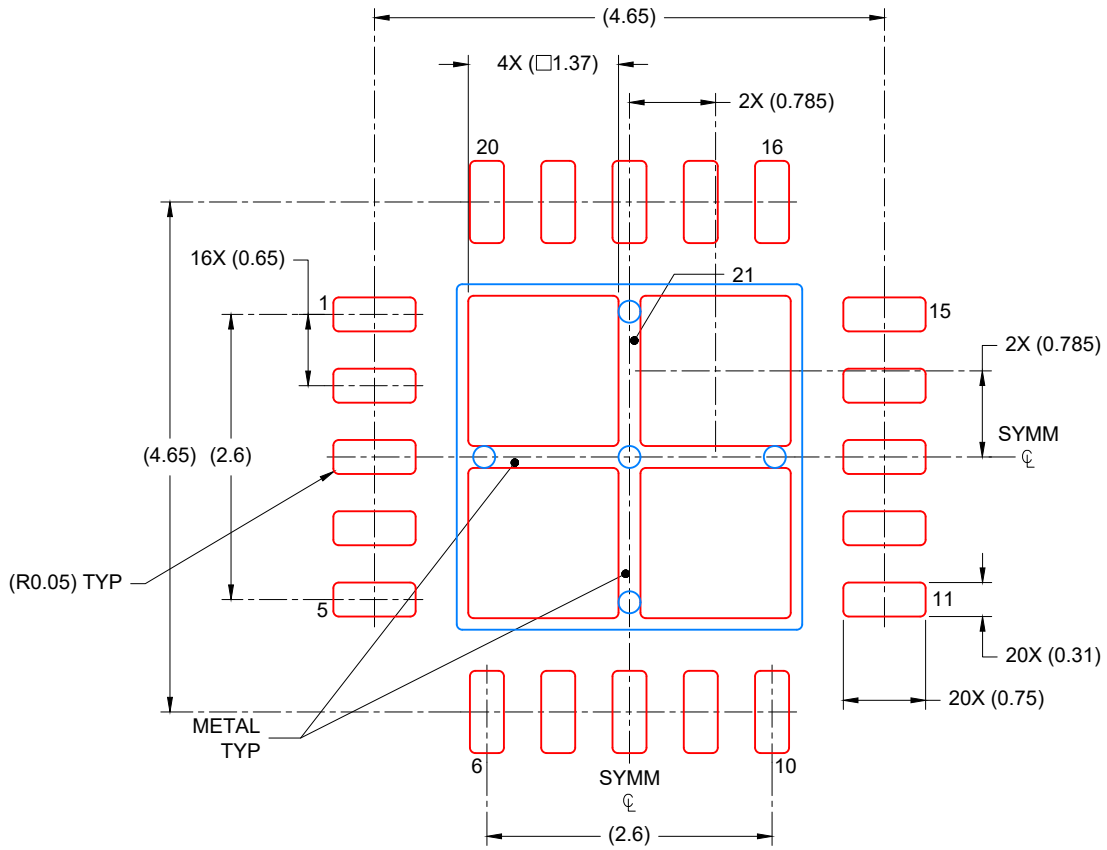
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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