- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Control Operation of Up to Six Parallel Target Scan Paths**
- **Accommodate Pipeline Delay to Target of Up to 31 Clock Cycles**
- **Scan Data Up to 2^{32} Clock Cycles**
- **Execute Instructions for Up to 2^{32} Clock Cycles**
- **Each Device Includes Four Bidirectional Event Pins for Additional Test Capability**
- **Inputs Are TTL-Voltage Compatible**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Packaged in 44-Pin Plastic Leaded Chip Carrier (FN), 68-Pin Ceramic Pin Grid Array (GB), and 68-Pin Ceramic Quad Flat Packages (HV)**

description

The ’ACT8990 test-bus controllers (TBC) are members of the Texas Instruments SCOPE™ testability integrated-circuit family. This family of components supports IEEE Standard 1149.1-1990 (JTAG) boundary scan to facilitate testing of complex circuit-board assemblies. The ’ACT8990 differ from other SCOPE™ integrated circuits. Their function is to control the JTAG serial-test bus rather than being target boundary-scannable devices.

The required signals of the JTAG serial-test bus – test clock (TCK), test mode select (TMS), test data input (TDI), and test data output (TDO) can be connected from the TBC to a target device without additional logic. This is done as a chain of IEEE Standard 1149.1-1990 boundary-scannable components that share the same serial-test bus. The TBC generates TMS and TDI signals for its target(s), receives TDO signals from its target(s), and buffers its test clock input (TCKI) to a test clock output (TCKO) for distribution to its target(s). The TMS, TDI, and TDO signals can be connected to a target directly or via a pipeline, with a retiming delay of up to 31 bits. Since the TBC can be configured to generate up to six separate TMS signals [TMS (5 – 0)], it can be used to control up to six target scan paths that are connected in parallel (i.e., sharing common TCK, TDI, and TDO signals).

While most operations of the TBC are synchronous to TCKI, a test-off ($\overline{\text{TOFF}}$) input is provided for output control of the target interface, and a test-reset ($\overline{\text{TRST}}$) input is provided for hardware/software reset of the TBC. In addition, four event [EVENT (3 – 0)] I/Os are provided for asynchronous communication to target device(s). Each event has its own event generation/detection logic, and detected events can be counted by two 16-bit counters.

The TBC operates under the control of a host microprocessor/microcontroller via the 5-bit address bus [ADRS (4 – 0)] and the 16-bit read/write data bus [DATA (15 – 0)]. Read ($\overline{\text{RD}}$) and write ($\overline{\text{WR}}$) strobes are implemented such that the critical host-interface timing is independent of the TCKI period. Any one of 24 registers can be addressed for read and/or write operations. In addition to control and status registers, the TBC contains two command registers, a read buffer, and a write buffer. Status of the TBC is transmitted to the host via ready ($\overline{\text{RDY}}$) and interrupt ($\overline{\text{INT}}$) outputs.

Major commands can be issued by the host to cause the TBC to generate the TMS sequences necessary to move the target(s) from any stable test-access-port (TAP) controller state to any other stable TAP state, to execute instructions in the Run-Test/Idle TAP state, or to scan instruction or test data through the target(s). A 32-bit counter can be preset to allow a predetermined number of execution or scan operations.

Serial data that appears at the selected TDI input (TDI1 or TDI0) is transferred into the read buffer, which can be read by the host to obtain up to 16 bits of the serial-data stream. Serial data that is transmitted from the TDO output is written by the host to the write buffer.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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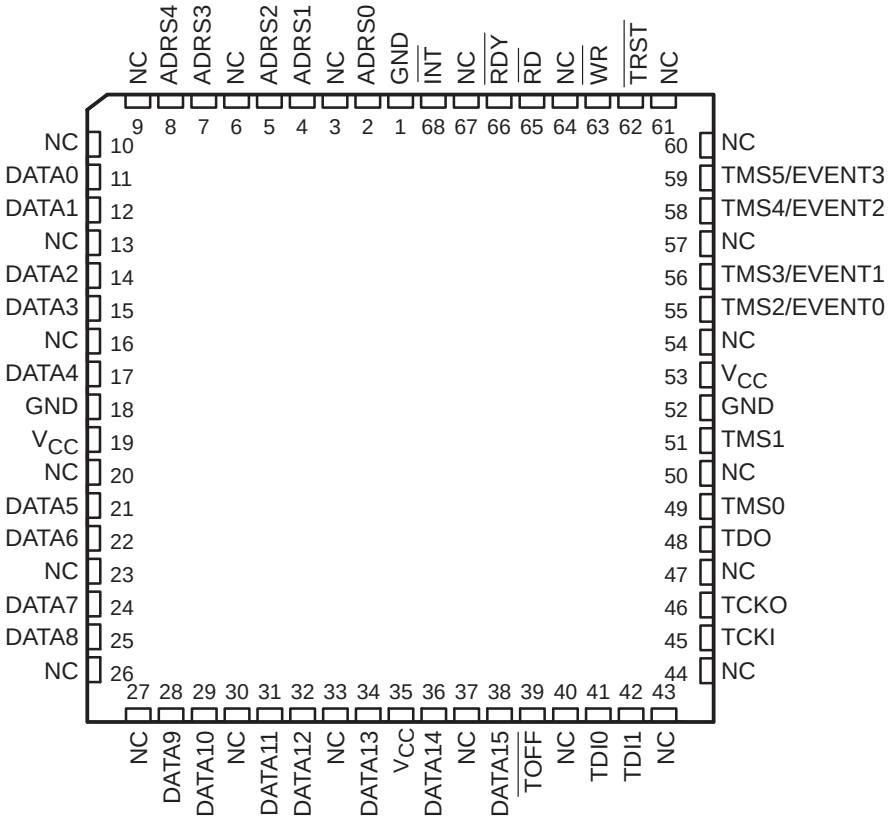
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

description (continued)

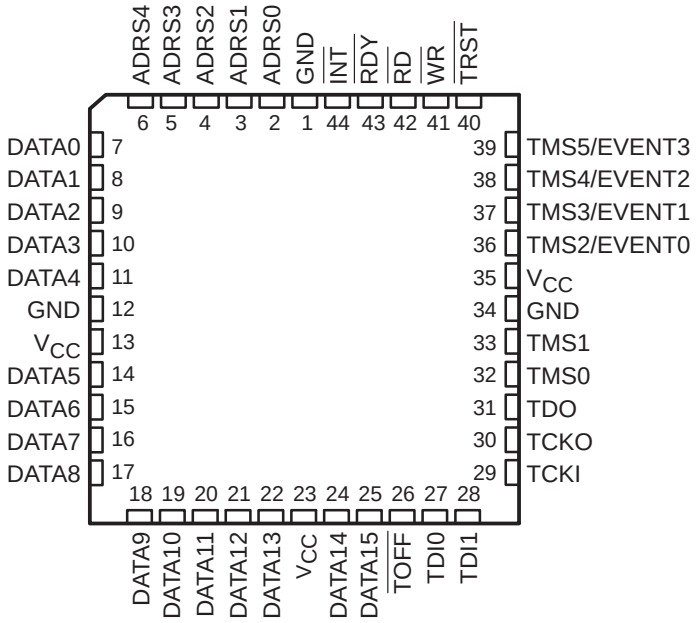
The SN54ACT8990 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT8990 is characterized for operation from 0°C to 70°C.

SN54ACT8990 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection

SN74ACT8990 . . . FN PACKAGE
(TOP VIEW)



SN54ACT8990 . . . GB PACKAGE
(TOP VIEW)

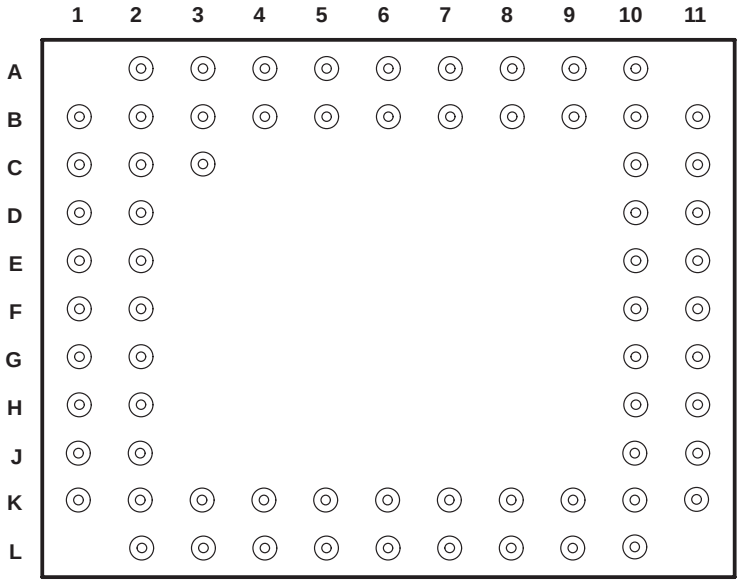
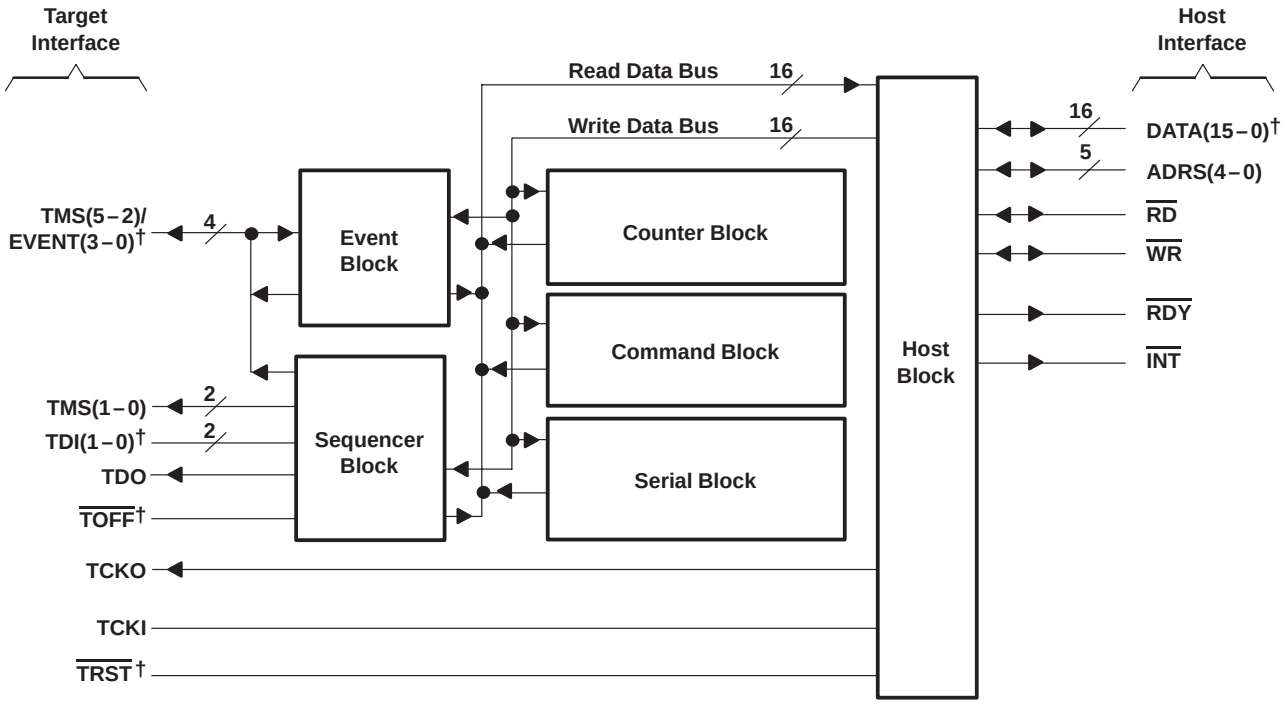


Table 1. Terminal Assignments

TERMINAL		TERMINAL		TERMINAL		TERMINAL	
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
A2	NC	B10	NC	F11	NC	K6	NC
A3	ADRS4	B11	NC	G1	DATA5	K7	V_{CC}
A4	NC	C1	DATA2	G2	NC	K8	DATA15
A5	ADRS1	C2	DATA1	G10	NC	K9	TDI0
A6	ADRS0	C3	NC	G11	TMS1	K10	NC
A7	NC	C10	TMS4/EVENT2	H1	NC	K11	TCKI
A8	$\overline{INT}$	C11	TMS5/EVENT3	H2	DATA6	L2	DATA9
A9	$\overline{RD}$	D1	DATA4	H10	TDO	L3	NC
A10	$\overline{TRST}$	D2	DATA3	H11	TMS0	L4	DATA12
B1	DATA0	D10	TMS3/EVENT1	J1	DATA8	L5	DATA13
B2	NC	D11	NC	J2	DATA7	L6	NC
B3	ADRS3	E1	NC	J10	TCKO	L7	DATA14
B4	ADRS2	E2	GND	J11	NC	L8	$\overline{TOFF}$
B5	NC	E10	V_{CC}	K1	NC	L9	TDI1
B6	NC	E11	TMS2/EVENT0	K2	NC	L10	NC
B7	GND	F1	V_{CC}	K3	DATA10		
B8	$\overline{RDY}$	F2	NC	K4	DATA11		
B9	$\overline{WR}$	F10	GND	K5	NC		

NC – No internal connection

functional block diagram



† Inputs have internal pullup resistors.

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
ADRS4 – ADRS0	I	Address inputs. ADRS4 – ADRS0 form the 5-bit address bus that interfaces the TBC to its host. These inputs specify the TBC register to be read from or written to.
DATA15 – DATA0	I/O	Data inputs and outputs. DATA15 – DATA0 form the 16-bit bidirectional data bus that interfaces the TBC to its host. Data is read from or written to the TBC register using this data bus.
GND		Ground
$\overline{\text{INT}}$	O	Interrupt. $\overline{\text{INT}}$ transmits an interrupt signal to the host. When the TBC requires service from the host, $\overline{\text{INT}}$ is asserted (low). $\overline{\text{INT}}$ will remain asserted (low) until the host has completed the required service.
NC		No connection
$\overline{\text{RD}}$	I	Read strobe. $\overline{\text{RD}}$ is the active low output enable for the data bus. $\overline{\text{RD}}$ is used as the strobe for reading data from the selected TBC register.
$\overline{\text{RDY}}$	O	Ready. $\overline{\text{RDY}}$ transmits a status signal to the host. When the TBC is ready to accept a read or write operation from the host, $\overline{\text{RDY}}$ is asserted (low). $\overline{\text{RDY}}$ is not asserted (high) when the TBC is in recovery from a read, write, command, or reset operation.
TCKI	I	Test clock input. TCKI is the clock input for the TBC. Most operations of the TBC are synchronous to TCKI. When enabled, all target interface outputs change on the falling edge of TCKI. Sampling of target interface inputs are configured to occur on either the rising edge or falling edge of TCKI.
TCKO	O	Test clock output. TCKO distributes TCK to the target(s). The TCKO is configured to be disabled, constant zero, constant one, or to follow TCKI. When TCKO follows TCKI, it is delayed to match the delay of generating the TDO and TMS signals.
TDI1 – TDI0	I	Test data inputs. The TDI1 – TDI0 serial inputs are used for shifting test data from the target(s). The TDI inputs can be directly connected to the TDO pin(s) of the target(s).
TDO	O	Test data output. TDO is used for shifting test data into the target(s). TDO can be directly connected to the TDI terminal(s) of the target(s).
TMS1 – TMS0	O	Test mode select outputs. These parallel outputs transmit TMS signals to the target(s), which direct them through their TAP controller states. TMS1 – TMS0 can be directly connected to the TMS terminals of the target(s).
TMS5 – TMS2/ EVENT3 – EVENT0	I/O	Test mode select outputs or event inputs/outputs. These I/Os can be configured for use as either TMS outputs or event inputs/outputs. As TMS outputs, they function similarly to TMS1 – TMS0 above. As event I/Os, they can be used to receive/transmit interrupt signals to/from the target(s).
$\overline{\text{TOFF}}$	I	Test-off input. $\overline{\text{TOFF}}$ is the active low output disable for all outputs and I/Os of the target interface (TCKO, TDO, TMS, TMS/EVENT).
$\overline{\text{TRST}}$	I	Test-reset input. $\overline{\text{TRST}}$ is used to initiate hardware and software reset operations of the TBC. Hardware reset begins when $\overline{\text{TRST}}$ is asserted (low). Software reset begins when $\overline{\text{TRST}}$ is released (high) and proceeds synchronously to TCKI to completion in a predetermined number of cycles.
$\overline{\text{WR}}$	I	Write input. $\overline{\text{WR}}$ is the strobe for writing data to a TBC data register. Signals present at the data and address buses are captured on the rising edge of $\overline{\text{WR}}$.
V_{CC}		Supply voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC}
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 2): FN package 1.5W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book,* literature number SCBD002.

recommended operating conditions

		SN54ACT8990		SN74ACT8990		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–8		–8	mA
I_{OL}	Low-level output current		8		8	mA
T_A	Operating free-air temperature	–55	125	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ACT8990		SN74ACT8990		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_{CC} = 4.5 V	I_{OH} = –20 µA	4.4			4.4		4.4		V
			I_{OH} = –8 mA	3.7			3.7		3.7		
		V_{CC} = 5.5 V	I_{OH} = –20 µA	5.4			5.4		5.4		
			I_{OH} = –8 mA	4.7			4.7		4.7		
V_{OL}		V_{CC} = 4.5 V to 5.5 V	I_{OL} = 20 µA			0.1		0.1		0.1	V
			I_{OL} = 8 mA			0.5		0.5		0.5	
I_I	ADRS, $\overline{RD}$, $\overline{WR}$, TCKI	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
	TDI, $\overline{TOFF}$, $\overline{TRST}$	V_{CC} = 5.5 V	$V_I = V_{CC}$			±1		±1		±1	
			V_I = GND	–35	–70	–250	–35	–250	–35	–250	
I_{OZ}‡	$\overline{INT}$, $\overline{RDY}$, TCKO, TDO, TMS	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or GND			±10		±10		±10	µA
	DATA, TMS/EVENT	V_{CC} = 5.5 V	$V_O = V_{CC}$			±10		±10		±10	
			V_O = GND	–35	–70	–250	–35	–250	–35	–250	
I_{CC}		V_{CC} = 5.5 V, I_O = 0,	$V_I = V_{CC}$ or GND			450*		450		450	µA
		V_{CC} = 5.5 V, f_{clock} = 30 MHz	C_L = 50 pF		100						mA
C_i		$V_I = V_{CC}$ or GND			5*						pF
C_{io}		$V_I = V_{CC}$ or GND			9*						pF
C_o		$V_I = V_{CC}$ or GND			8*						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† Typical values are at V_{CC} = 5 V.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

			SN54ACT8990		SN74ACT8990		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	30	0	30	MHz
t_w	Pulse duration	$\overline{RD}$ low†			5.5		ns
		$\overline{WR}$ low	5.5		5.5		ns
		EVENT high or low	8		8		
		TCKI high or low	10.5		10.5		
		$\overline{TRST}$ low	6		6		
t_{su}	Setup time	ADRS† before $\overline{RD}$↑			6.5		ns
		ADRS before $\overline{WR}$↑	6.5		6.5		ns
		DATA before $\overline{WR}$↑	6		6		
		EVENT before TCKI↑	6		5.5		
		EVENT before TCKI↓	5		5		
		TDI before TCKI↑	2		2		
		TDI before TCKI↓	2		2		
t_h	Hold time	ADRS† after $\overline{RD}$↑			5		ns
		ADRS after $\overline{WR}$↑	5.5		5		ns
		DATA after $\overline{WR}$↑	5.5		5.5		
		EVENT after TCKI↑	5.5		5		
		EVENT after TCKI↓	5		5		
		TDI after TCKI↑	4		2.5		
		TDI after TCKI↓	4		2.5		

† Applies only in the case where ADRS (4-0) = 10110 (read buffer).

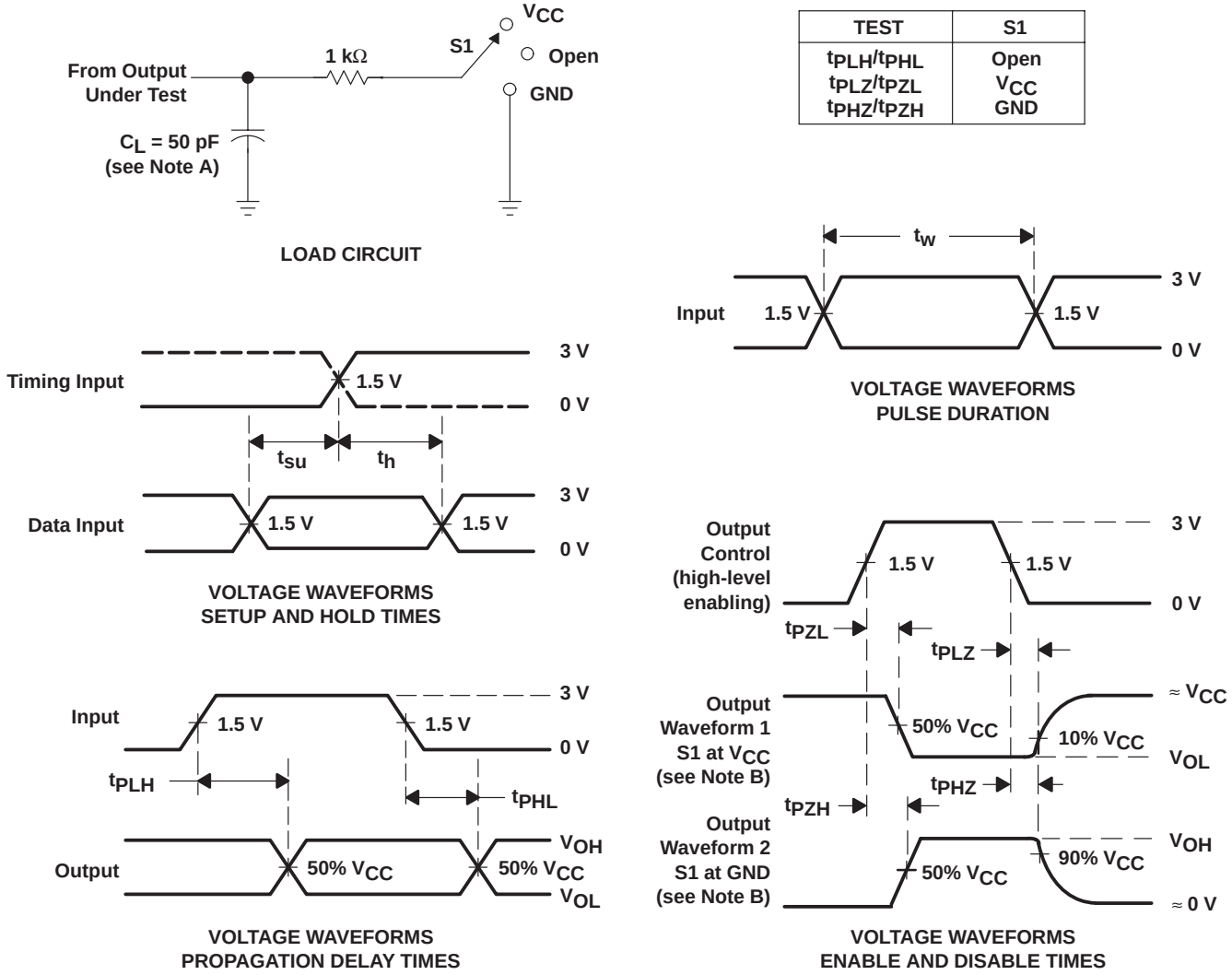
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8990		SN74ACT8990		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			30		30		MHz
t_{PLH}	ADRS	DATA	8	43	19.5	39.3	ns
t_{PHL}			8	43	19.5	39.3	
t_{PLH}	$\overline{RD}\uparrow$	$\overline{RDY}$	5.3	17	5.3	13.8	ns
	$\overline{WR}\uparrow$		2.5	16	2.5	13	
t_{PLH}	TCKI↑	$\overline{INT}$	3.7	16	3.7	12.9	ns
t_{PHL}			5.5	15	5.5	13.1	
t_{PHL}	TCKI↑	$\overline{RDY}$	4.4	15	4.4	13.4	ns
t_{PLH}	TCKI↑	TCKO	3.3	17	3.3	14.1	ns
t_{PLH}	TCKI↓	TCKO	2.3	19	2.3	15.9	ns
t_{PHL}			3.6	17	3.6	15.6	
t_{PLH}	TCKI↓	TDO	2.9	19	2.9	17.5	ns
t_{PHL}			5.2	20	5.2	17.9	
t_{PLH}	TCKI↓	TMS	3.1	19	3.1	17.5	ns
t_{PHL}			5.1	19	5.1	18.2	
t_{PLH}	TCKI↓	TMS/EVENT	1.5	19	1.5	17.5	ns
t_{PHL}			3.5	20	3.5	18.9	
t_{PZH}	$\overline{RD}\downarrow$	DATA	3.8	21	3.8	17.6	ns
t_{PZL}			6.8	28	6.8	22.6	
t_{PZH}	TCKI↑	$\overline{INT}$	4.9	19	4.9	15.3	ns
		$\overline{RDY}$	3.6	19	3.6	15.3	
t_{PZH}	TCKI↓	TCKO	4.1	23	4.1	19.2	ns
t_{PZL}			4.8	20	4.8	17.4	
t_{PZH}	TCKI↓	TDO	4.3	22	4.3	19.5	ns
t_{PZL}			5	20	5	17.7	
t_{PZH}	TCKI↓	TMS	4.6	23	4.6	19.9	ns
t_{PZL}			5.1	20	5.1	18.5	
t_{PZH}	TCKI↓	TMS/EVENT	2	21	2	18.8	ns
t_{PZL}			3.2	20	3.2	18.7	
t_{PZH}	$\overline{TOFF}\uparrow$	TCKO	4.6	16	4.6	12.2	ns
t_{PZL}			3.1	14	3.1	10.3	
t_{PZH}	$\overline{TOFF}\uparrow$	TDO	4.4	15	4.4	12.2	ns
t_{PZL}			3.5	14	3.5	10.8	
t_{PZH}	$\overline{TOFF}\uparrow$	TMS	3.1	16.2	3.1	14.7	ns
t_{PZL}			1.9	16.7	1.9	13.6	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (continued) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT8990		SN74ACT8990		UNIT
			MIN	MAX	MIN	MAX	
t_{PZH}	$\overline{TOFF}$↑	TMS/EVENT	2.3	15.3	2.3	13.8	ns
t_{PZL}			2.7	16.4	2.7	13.9	
t_{PHZ}	$\overline{RD}$↑	DATA	3.8	18.4	3.8	15.4	ns
t_{PLZ}			4.1	17.1	4.1	14.8	
t_{PHZ}	TCKI↓	TCKO	6.7	20.4	6.7	19.8	ns
t_{PLZ}			4.8	21.1	4.8	20.4	
t_{PHZ}	TCKI↓	TDO	5.1	21.7	5.1	21.3	ns
t_{PLZ}			5	20.7	5	20.3	
t_{PHZ}	TCKI↓	TMS	6.9	22.4	6.9	21.9	ns
t_{PLZ}			4.6	20.6	4.6	20.1	
t_{PHZ}	TCKI↓	TMS/EVENT	4.7	22.5	4.7	22.1	ns
t_{PLZ}			2.8	20.5	2.8	20.1	
t_{PHZ}	$\overline{TOFF}$↓	TCKO	5	15.6	5	15.4	ns
t_{PLZ}			4.4	15.5	4.4	15.3	
t_{PHZ}	$\overline{TOFF}$↓	TDO	5.6	16.6	5.6	16.5	ns
t_{PLZ}			4.6	15.4	4.6	15.4	
t_{PHZ}	$\overline{TOFF}$↓	TMS	4.8	19.1	4.8	17.1	ns
t_{PLZ}			4.4	17	4.4	15.8	
t_{PHZ}	$\overline{TOFF}$↓	TMS/EVENT	4.5	18.8	4.5	17.3	ns
t_{PLZ}			2.4	17.1	2.4	16.2	
t_{PHZ}	$\overline{TRST}$↓	DATA	5.7	23	5.7	20.8	ns
t_{PLZ}			4.2	20.3	4.2	20	
t_{PHZ}	$\overline{TRST}$↓	$\overline{INT}$	6	19.6	8	19.5	ns
t_{PLZ}			6.1	18	6.1	17.8	
t_{PHZ}	$\overline{TRST}$↓	$\overline{RDY}$	6.5	18.8	6.5	18.7	ns
t_{PLZ}			4.8	17.8	4.8	17.8	
t_{PHZ}	$\overline{TRST}$↓	TMS/EVENT	6	21.1	6	21.1	ns
t_{PLZ}			4.2	20	4.2	19.9	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: $t_r = t_f$ = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9322801MXA	Active	Production	CFP (HV) | 68	10 | TUBE	No	Call TI	Call TI	-55 to 125	(5962-9322801MX, 5962-9322801MXA) A SNJ54ACT8990HV
5962-9322801MYA	Last Time Buy	Production	CPGA (GB) | 68	21 | JEDEC TRAY (5+1)	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322801MY A SNJ54ACT8990GB
SN74ACT8990FN	Active	Production	PLCC (FN) | 44	26 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ACT8990
SN74ACT8990FN.A	Active	Production	PLCC (FN) | 44	26 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ACT8990
SN74ACT8990FNR	Active	Production	PLCC (FN) | 44	500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ACT8990
SN74ACT8990FNR.A	Active	Production	PLCC (FN) | 44	500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ACT8990
SNJ54ACT8990GB	Last Time Buy	Production	CPGA (GB) | 68	21 | JEDEC TRAY (5+1)	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322801MY A SNJ54ACT8990GB
SNJ54ACT8990GB.A	Last Time Buy	Production	CPGA (GB) | 68	21 | JEDEC TRAY (5+1)	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9322801MY A SNJ54ACT8990GB
SNJ54ACT8990HV	Active	Production	CFP (HV) | 68	10 | TUBE	No	Call TI	Call TI	-55 to 125	(5962-9322801MX, 5962-9322801MXA) A SNJ54ACT8990HV
SNJ54ACT8990HV.A	Active	Production	CFP (HV) | 68	10 | TUBE	No	Call TI	Call TI	-55 to 125	(5962-9322801MX, 5962-9322801MXA) A SNJ54ACT8990HV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

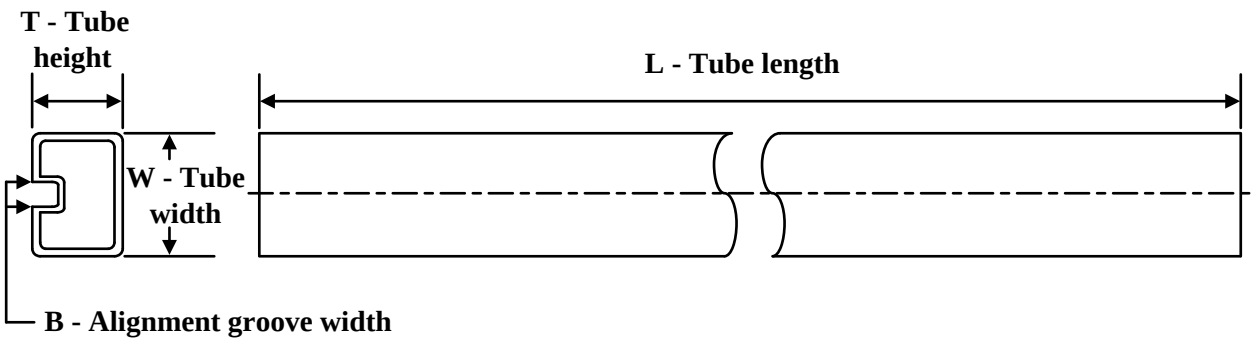
OTHER QUALIFIED VERSIONS OF SN54ACT8990, SN74ACT8990 :

- Catalog : SN74ACT8990
- Military : SN54ACT8990

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

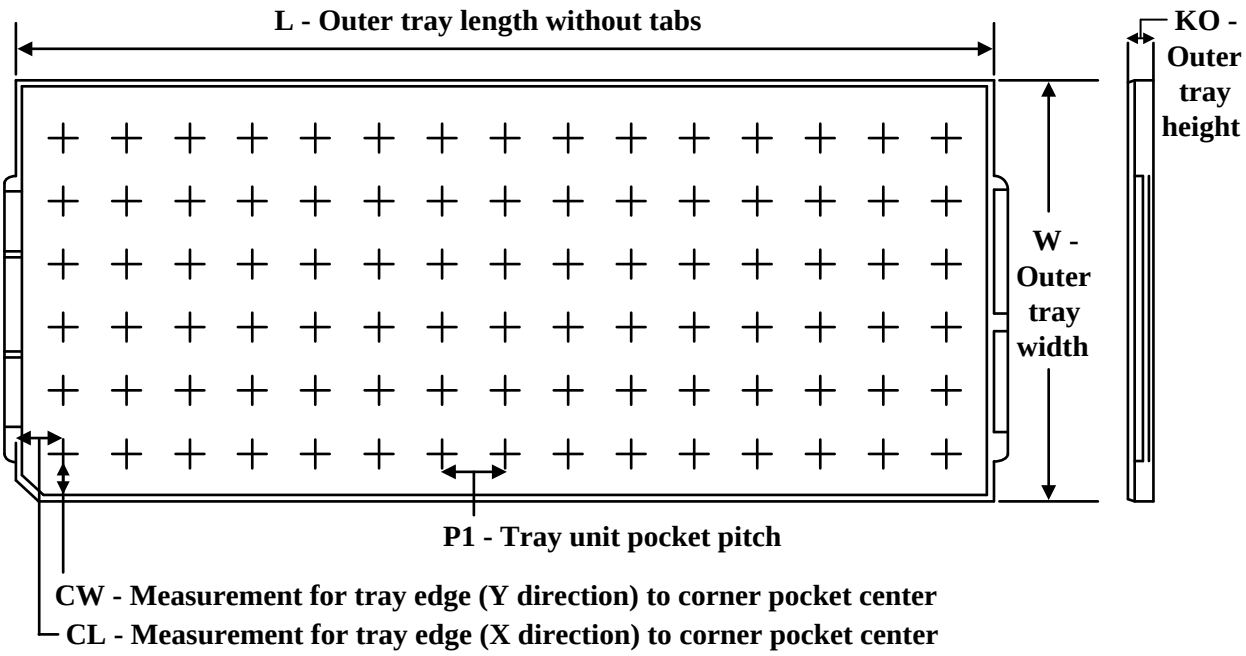
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ACT8990FN	FN	PLCC	44	26	18.42	5.13	640	NA
SN74ACT8990FN.A	FN	PLCC	44	26	18.42	5.13	640	NA

TRAY

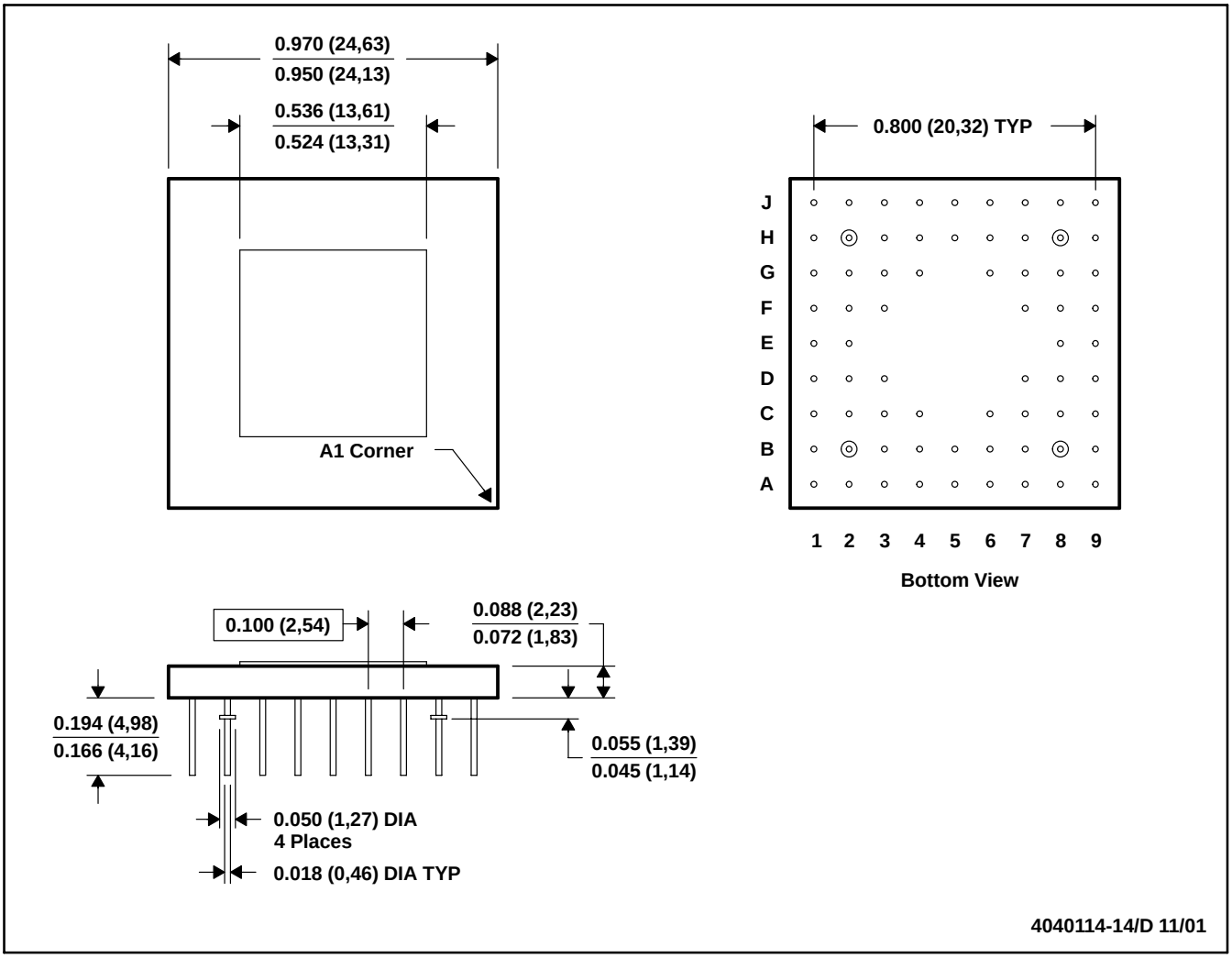


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-9322801MXA	HV	CFP	68	10	2 x 5	75	315	135.9	13000	60.96	35.58	37.47
SNJ54ACT8990HV	HV	CFP	68	10	2 x 5	75	315	135.9	13000	60.96	35.58	37.47
SNJ54ACT8990HV.A	HV	CFP	68	10	2 x 5	75	315	135.9	13000	60.96	35.58	37.47

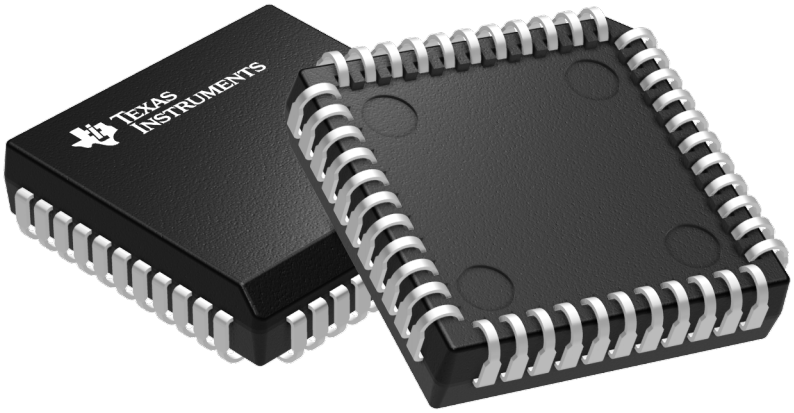
GB (S-CPGA-P68) **CERAMIC PIN GRID ARRAY**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending vendor.
D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edges of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold plated or solder dipped.
G. Falls within MIL STD 1835 CMGA1-PN, CMGA13-PN and JEDEC MO-067 AA, MO-066 AA respectively

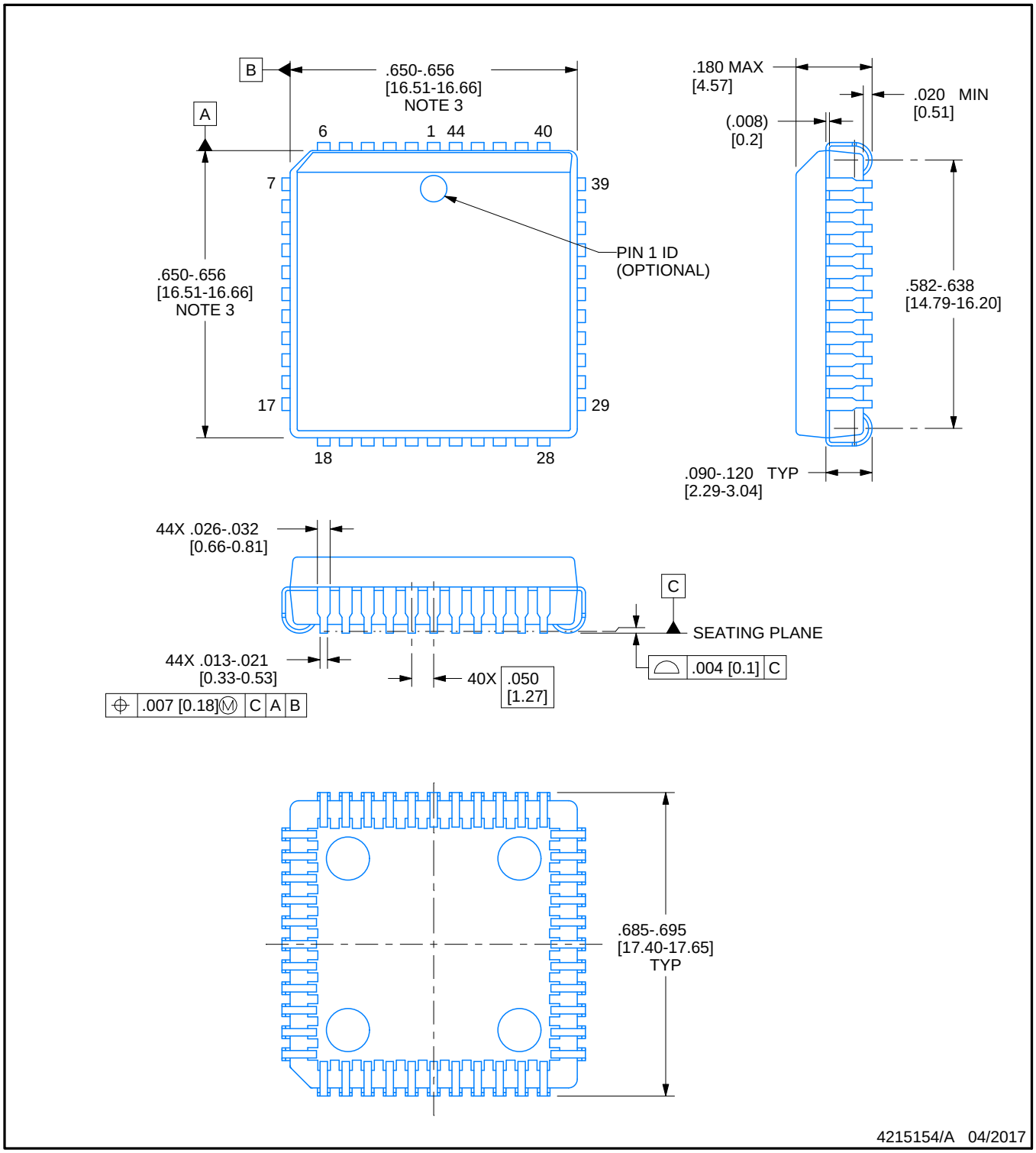
FN 44 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



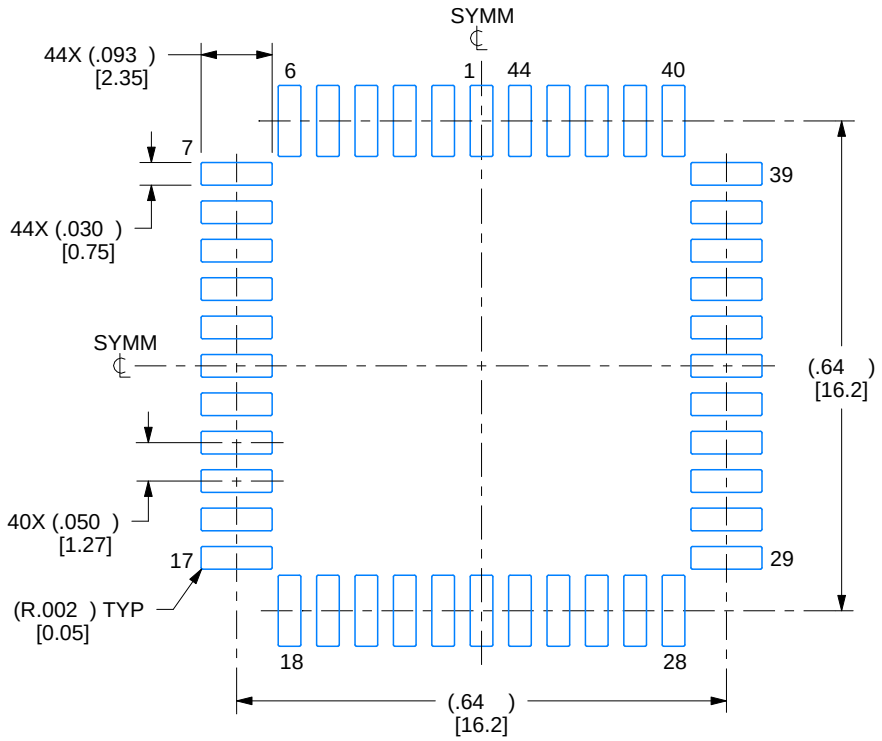
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040005-4/C

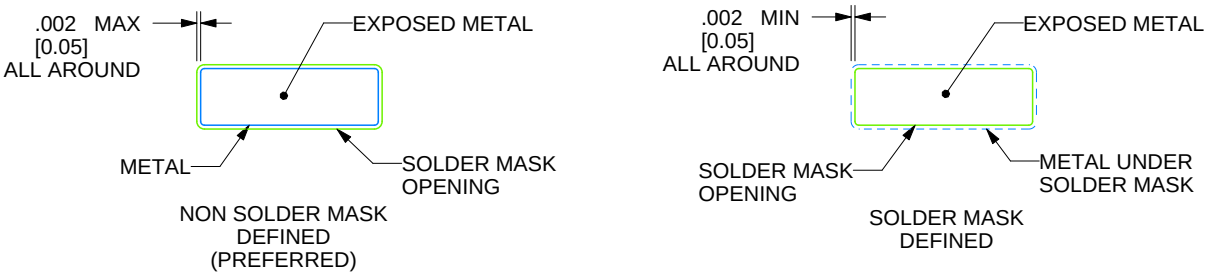


NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



SOLDER MASK DETAILS

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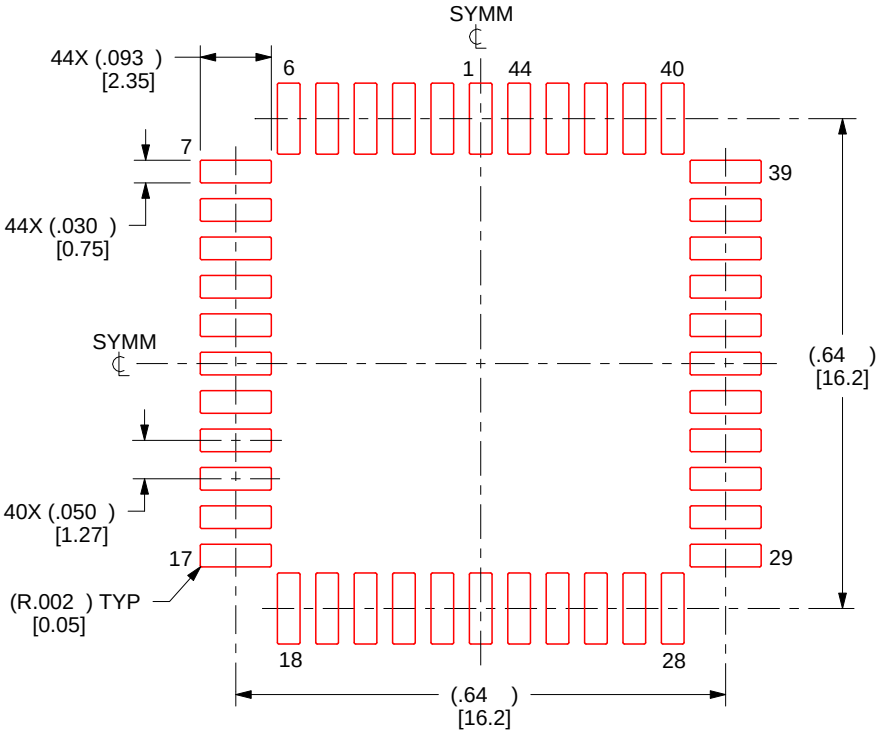
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



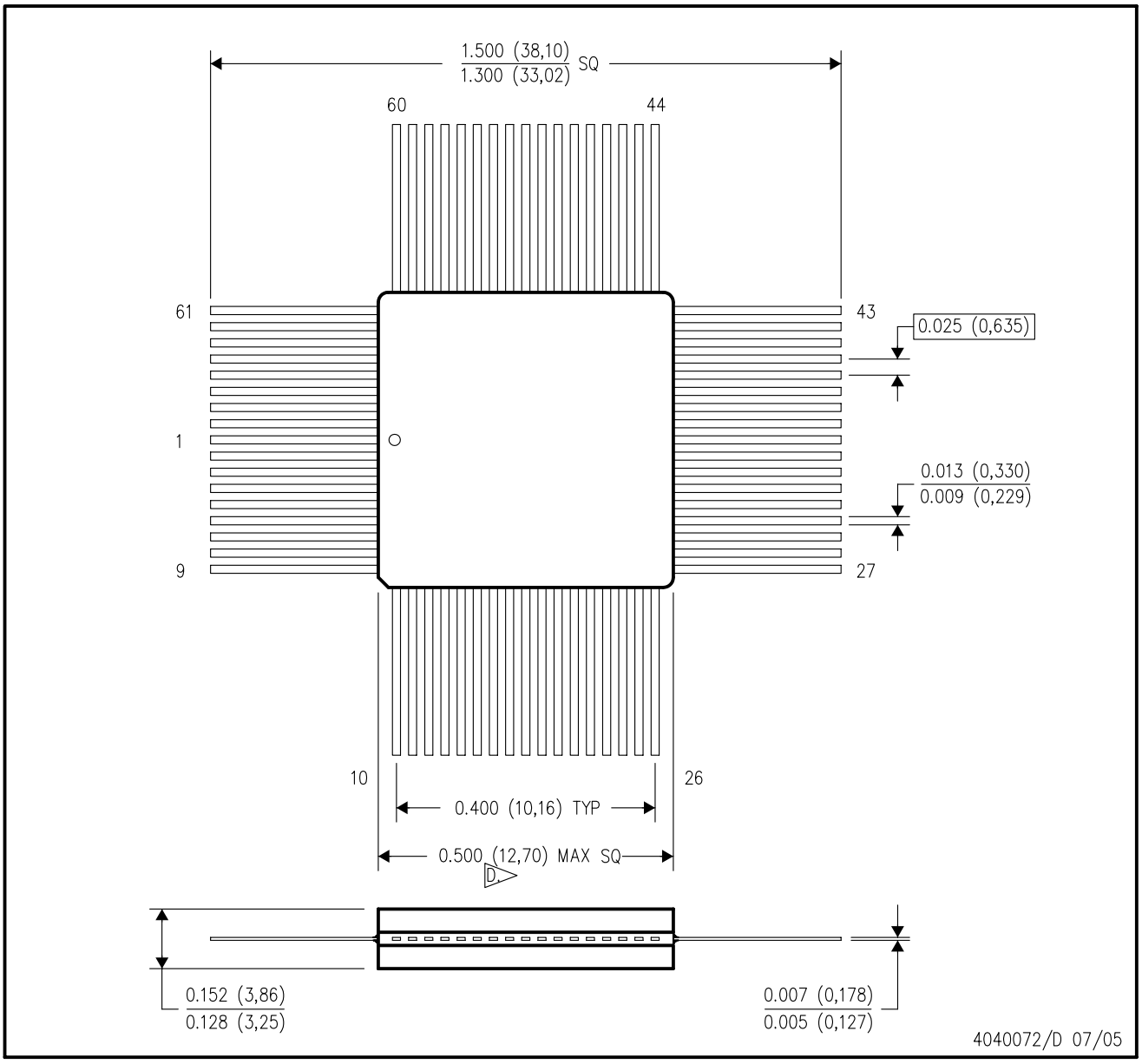
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4215154/A 04/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

HV (S–GQFP–F68) CERAMIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. This dimension allows for package edge anomalies caused by material protrusion, such as rough ceramic, misaligned ceramic layers and lids, meniscus, and glass overrun.

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