4-CHANNEL 8:16 MULTIPLEXER/DEMULTIPLEXER PCI EXPRESS SWITCH

Check for Samples: TS2PCIE412

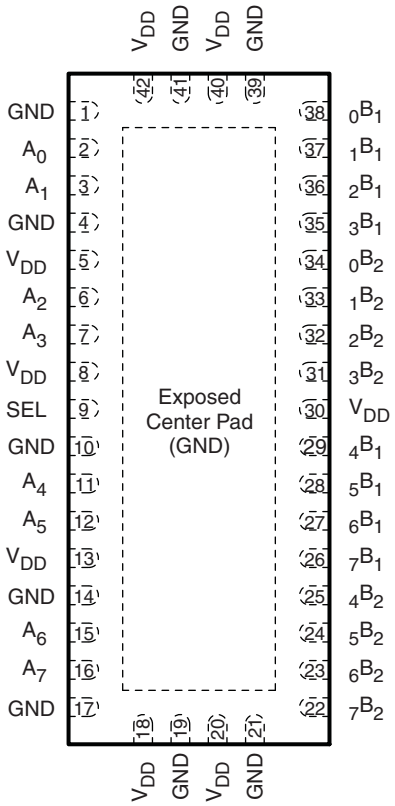
FEATURES

- **Compatible With PCI Express (PCIe) Standard**
- **Wide Bandwidth of over 3 Gbps**
- **Low Crosstalk (X_{TALK} = –32 dB Typ at 1.25 GHz)**
- **O_{IRR} = –36.3 dB Typical at 1.25 GHz**
- **Low Bit-to-Bit Skew ($t_{sk(O)}$ = 0.06 ns Typical)**
- **V_{DD} Operating Range: 1.5 V to 2 V**
- **I_{off} Supports Partial Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

APPLICATIONS

- **PCIe Bus Multiplexing and Expansion**
- **Routing PCI Express Data and/or Display Port Signals**
- **Notebook PCs**
- **Desktop PCs**
- **Servers/Storage Area Networks**

RUA PACKAGE
(TOP VIEW)



If the exposed center pad is used, it must be connected to ground.

DESCRIPTION/ ORDERING INFORMATION

The TS2PCIE412 is a 4-channel PCIe 2:1 multiplexer/demultiplexer switch that can be used to route one PCIe data lane between two possible destinations or two PCIe data lanes to one destination. Each channel consists of differential pairs of receive (RX) and transmit (TX) signals and operates at a signal-processing bandwidth speed, which supports the PCIe standard of 2.5 Gbps. The device is controlled with one select input (SEL) pin, where SEL controls the data path of the multiplexer/demultiplexer and can be connected to any GPIO in the system. The unselected channel is set in a high-impedance state.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RUA	Tape and reel	TS2PCIE412RUAR	SH412

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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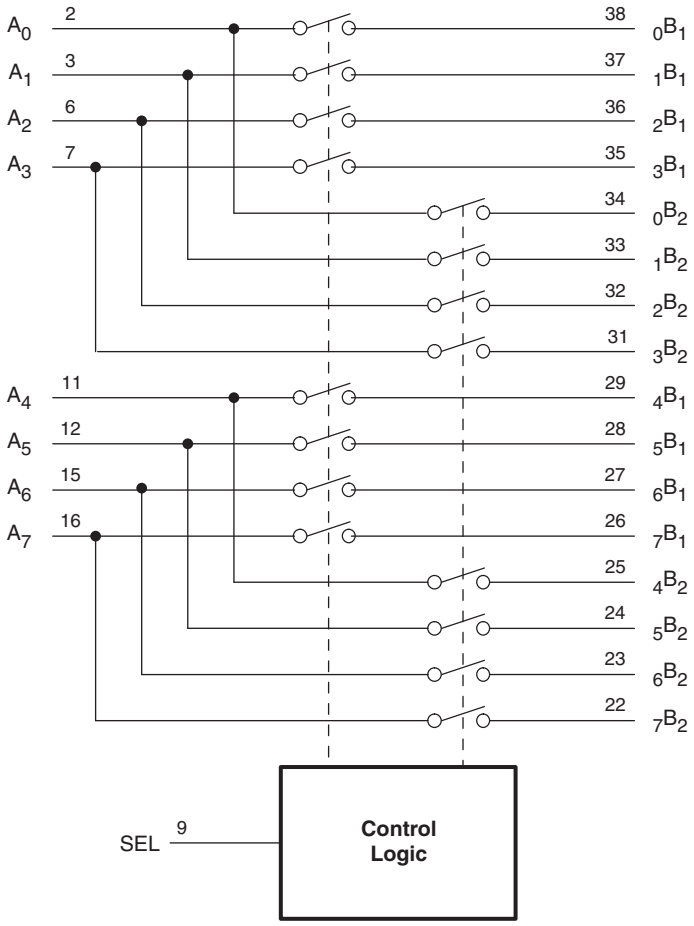
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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FUNCTION TABLE

SEL	FUNCTION
L	A_n to $_nB_1$
H	A_n to $_nB_2$

FUNCTIONAL DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A_n,	2, 3, 6, 7, 11, 12, 15, 16	I/O	Data I/Os
$_nB_m$	22–29, 31–38	I/O	Data I/Os
SEL	9	I	Select input
V_{DD}	5, 8, 13, 18, 20, 30, 40, 42	–	Power supply
GND	1, 4, 10, 14, 17, 19, 21, 39, 41, Exposed center pad	–	Ground

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ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	2.5	V
V_{IN}	Control input voltage range(2) (3)		–0.5	2.5	V
$V_{I/O}$	Switch I/O voltage range(2) (3) (4)		–0.5	2.5	V
I_{IK}	Control input clamp current	V_{IN} < GND		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < GND		–50	mA
$I_{I/O}$	ON-state switch current(5)			100	mA
I_{DD}	Continuous current through V_{DD}			100	mA
I_{GND}	Continuous current through GND			–100	mA
T_{stg}	Storage temperature range.		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise specifed.
(3) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

PACKAGE THERMAL IMPEDANCE

over operating free-air temperature range (unless otherwise noted)

				UNIT
θ_{JA}	Package thermal impedance(1)	RUA package	51.2	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	1.5	1.8	2	V
V_{IH}	High-level control input voltage (SEL)	0.65 × V_{DD}			V
V_{IL}	Low-level control input voltage (SEL)			0.35 × V_{DD}	V
V_{IO}	Switch input/output voltage	0		V_{DD}	V
T_A	Operating free air temperature	0		85	°C

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ELECTRICAL CHARACTERISTICS FOR 1.8-V SUPPLY(1)

V_{DD} = 1.5 V to 2.0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 2.0 V,	I_{IN} = –18 mA			–0.7	–1.3	V
I_{IH}	SEL	V_{DD} = 2.0 V,	V_{IN} = V_{DD}				±1	µA
I_{IL}	SEL	V_{DD} =2.0 V,	V_{IN} = GND				±1	µA
I_{off}		V_{DD} = 0,	V_O = 0 to 2 V,	V_I = 0			1	µA
I_{CC}		V_{DD} = 2.0 V,	$I_{I/O}$ = 0,	Switch ON or OFF		200	400	µA
C_{IN}	SEL	f = 10 MHz, V_{IN} = 0 V				1		pF
C_{OFF}	B port	V_I = 0 V, f = 10 MHz,	Outputs open,	Switch OFF		1.5	1.5	pF
C_{ON}		V_I = 0 V, f = 10 MHz,	Outputs open,	Switch ON		4.5	4.5	pF
r_{ON}		V_{DD} = 1.8 V,	GND ≤ V_I ≤ V_{DD},	I_O = –40 mA		12	18	Ω
$r_{ON(flat)}$ (3)		V_{DD} = 1.8 V,	V_I = 1.65 to 1.8 V,	I_O = –40 mA		0.5		Ω
Δr_{ON} (4)		V_{DD} = 1.8 V,	GND ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.2	0.8	Ω
Dynamic								
X_{TALK}		R_L = 100 Ω, f = 10 MHz		See Figure 9		–81		dB
		R_L = 100 Ω, f = 1.25 GHz				–32		
O_{IRR}		R_L = 100 Ω, f = 10 MHz		See Figure 10		–74		dB
		R_L = 100 Ω, f = 1.25 GHz				–36		
BW		R_L = 50 Ω,	See Figure 8			2.1		GHz
Max data rate		R_L = 50 Ω,	See Figure 8			4.2		Gbps

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 1.8 V (unless otherwise noted), T_A = 25°C.
(3) $r_{ON(flat)}$ is the difference of r_{ON} in a given channel at specific voltages.
(4) Δr_{ON} is the difference of ron from center ports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 1.5 V to 2.0 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd} (2) (3)	A_n or $_nB_n$	$_nB_n$ or A_n		0.28		ns
t_{PZH}, t_{PZL}	SEL	A_n or $_nB_n$		7.8	9	ns
t_{PHZ}, t_{PLZ}	SEL	A_n or $_nB_n$		2.5	4	ns
$t_{sk(O)}$ (4)	A_n or $_nB_n$	$_nB_n$ or A_n		0.06	0.1	ns
$t_{sk(p)}$ (5) (6)				0.06	0.1	ns

(1) All typical values are at V_{DD} = 1.8 V (unless otherwise noted) T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) See Figure 6
(4) Output skew between center port to any other port
(5) Skew between opposite transitions of the same output in a given device $t_{PHL} – t_{PLH}$
(6) See Figure 7

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TYPICAL PERFORMANCE

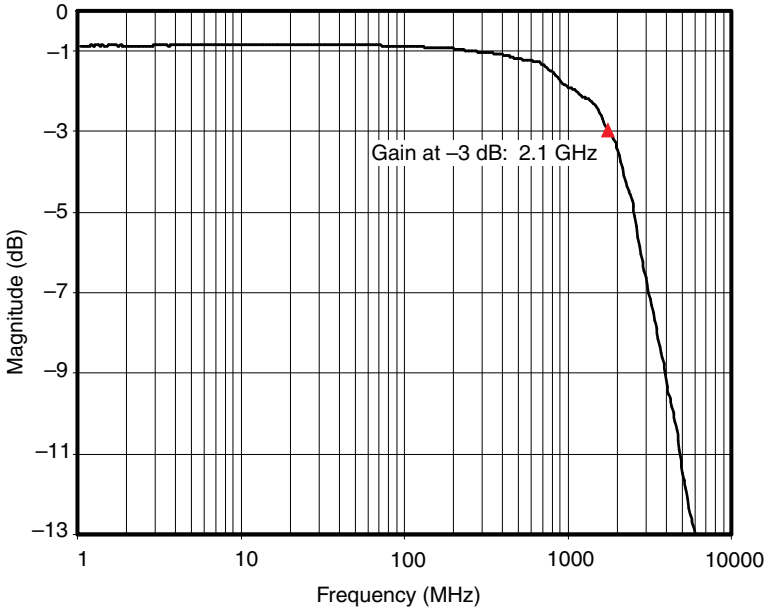


Figure 1. Frequency Response (Insertion Loss)

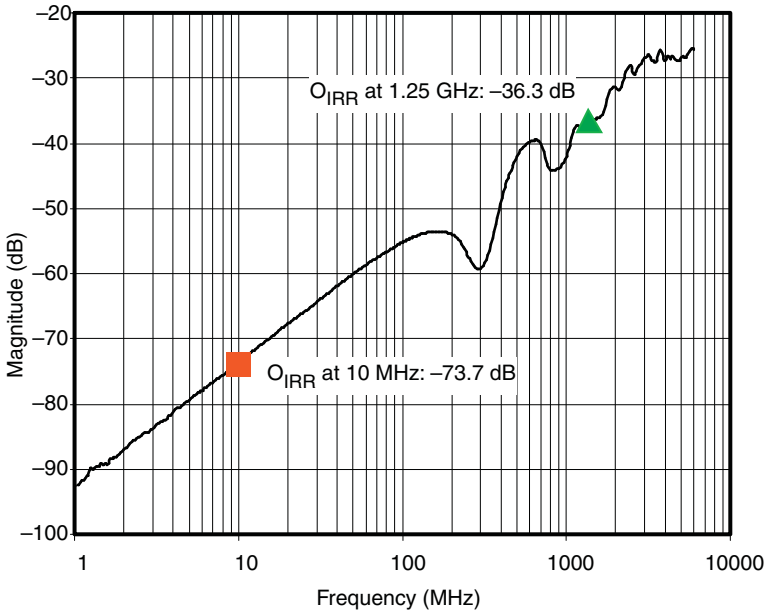


Figure 2. OFF Isolation vs Frequency

TYPICAL PERFORMANCE (continued)

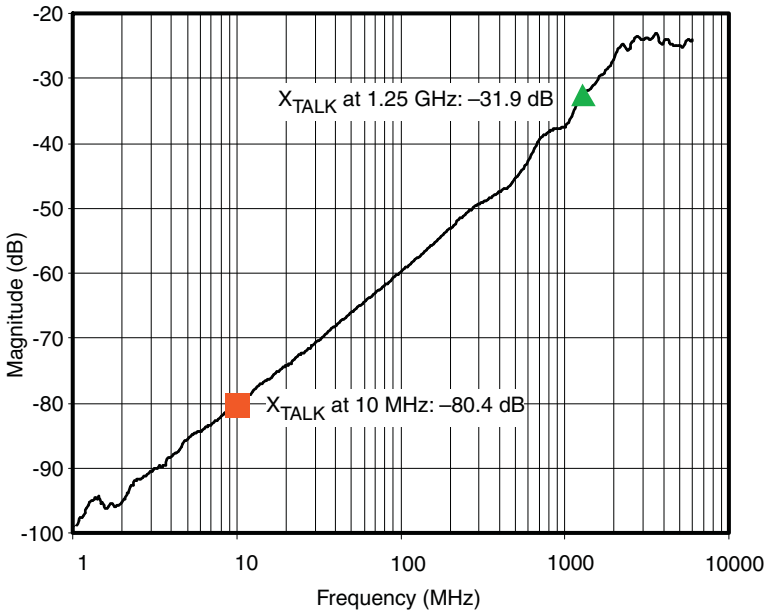


Figure 3. Crosstalk vs Frequency

Eye Diagrams

10-inch trace board for real implementation, V_{DD} = 1.8 V, f = 1.25 GHz, transitional signal and non-transitional signal eye from Tektronix TDS6154C and Tektronix RT-Eye = software

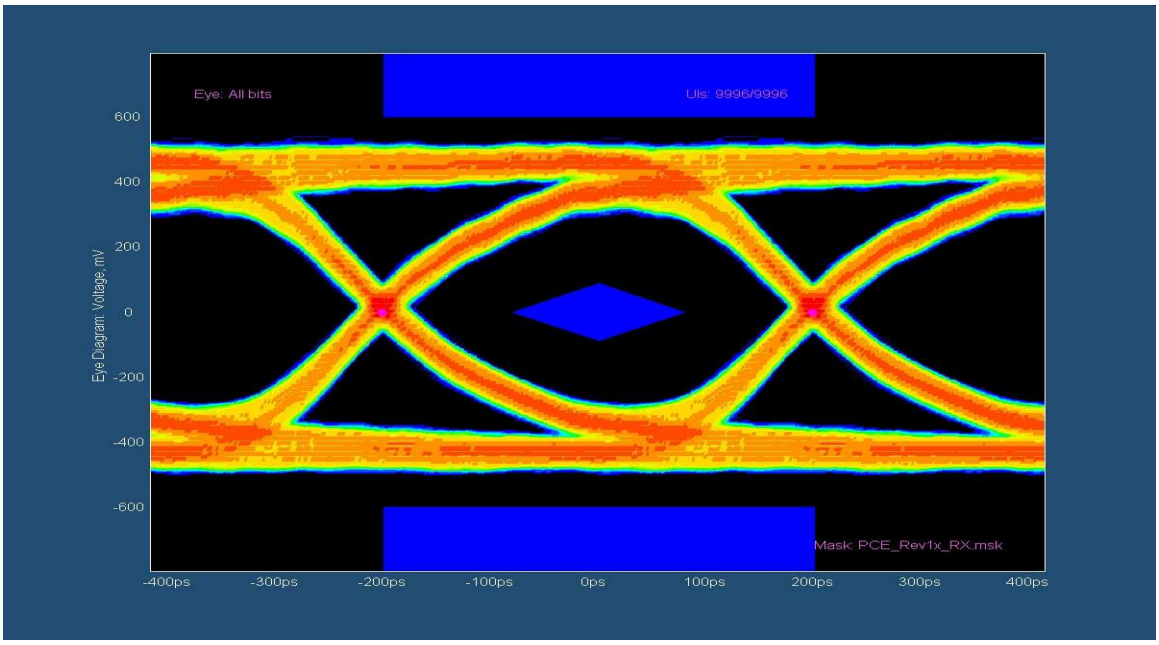


Figure 4. Transitional Signal Eye for TS2PCIE412 Using a 10-inch Trace

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TYPICAL PERFORMANCE (continued)

10-inch trace board for real implementation, V_{DD} = 1.8 V, f = 1.25 GHz, transitional signal and non-transitional signal eye from Tektronix TDS6154C and Tektronix RT-Eye = software

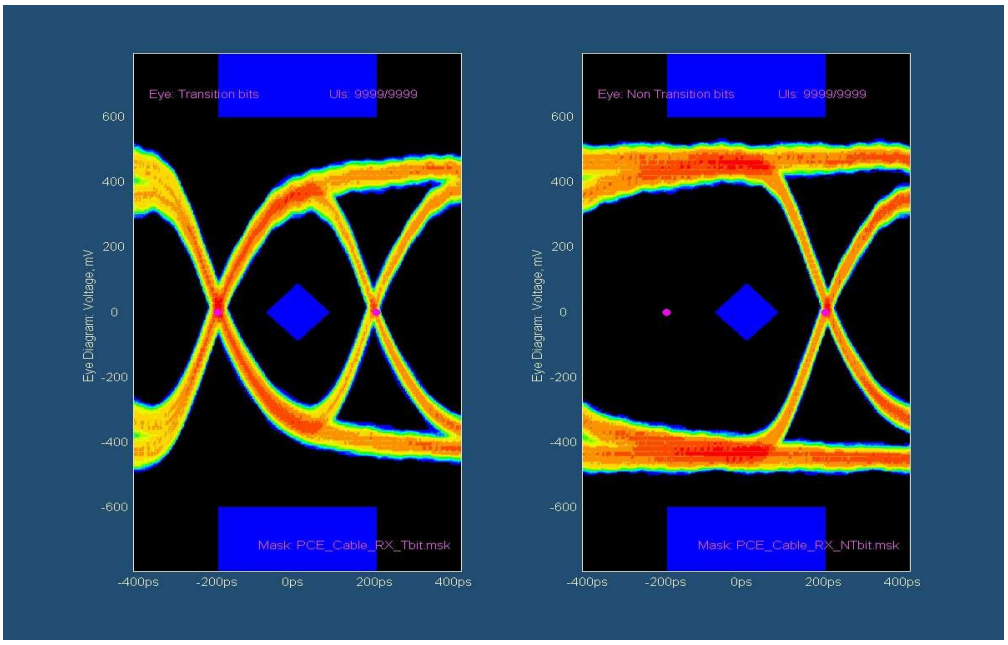
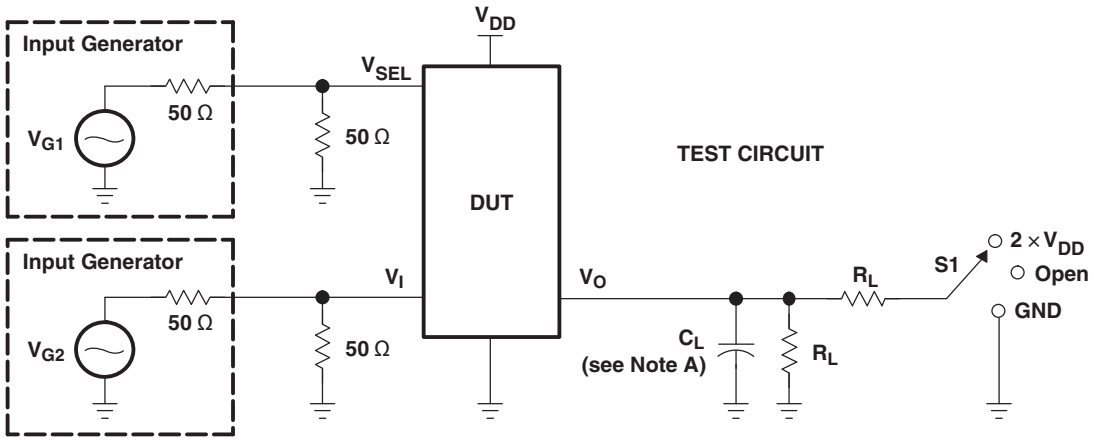


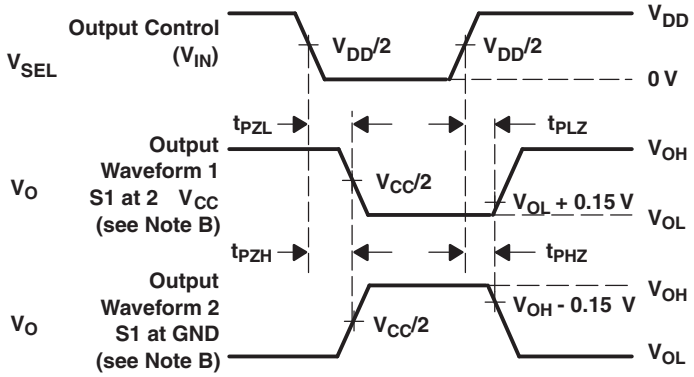
Figure 5. Transitional Signal Eye (Left) and Non-Transitional Signal Eye (Right) for TS2PCIE412 Using a 10-inch Trace

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PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	V_{DD}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	1.5 V to 2 V	2 × V_{DD}	200 Ω	GND	10 pF	0.15 V
t_{PHZ}/t_{PZH}	1.5 V to 2 V	GND	200 Ω	V_{DD}	10 pF	0.15 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

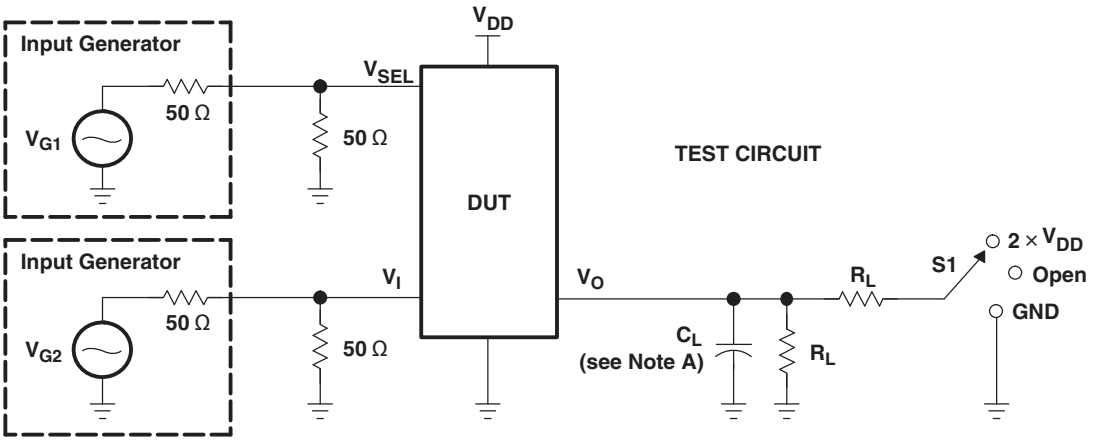
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

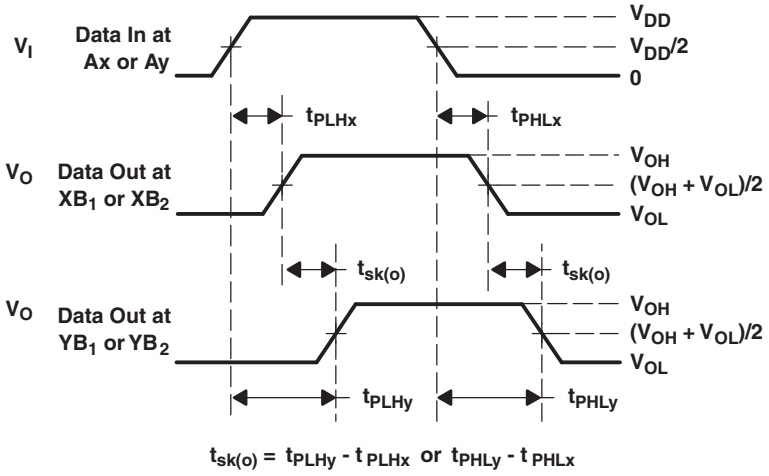
Figure 6. Test Circuit and Voltage Waveforms

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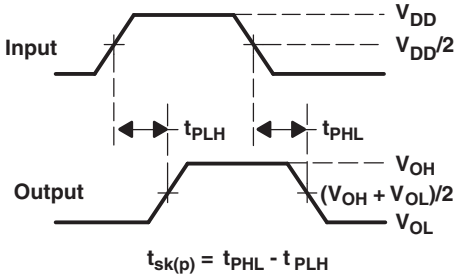
PARAMETER MEASUREMENT INFORMATION (Skew)



TEST	V_{DD}	S1	R_L	V_{SEL}	C_L
$t_{sk(o)}$	1.5 V to 2 V	Open	200 Ω	V_{DD} or GND	10 pF
$t_{sk(p)}$	1.5 V to 2 V	Open	200 Ω	V_{DD} or GND	10 pF



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤2.5 ns.

D. The outputs are measured one at a time, with one transition per measurement.

Figure 7. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

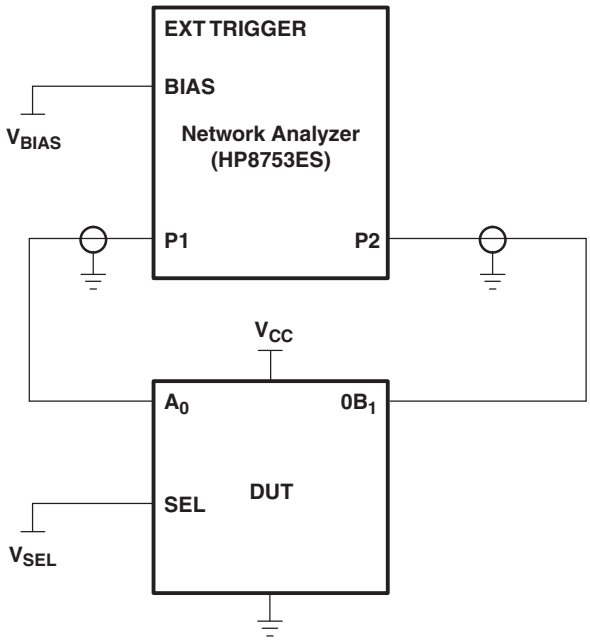


Figure 8. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 V and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

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PARAMETER MEASUREMENT INFORMATION (continued)

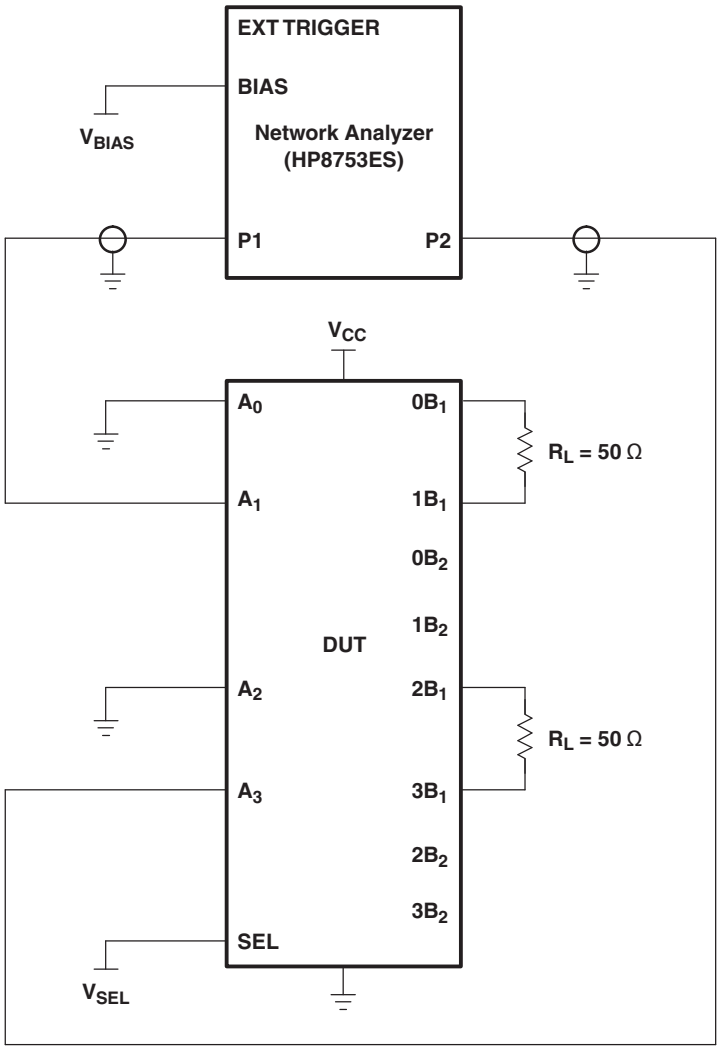


Figure 9. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the input of the nonadjacent ON channel. For example, when V_{SEL} = 0 V and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

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PARAMETER MEASUREMENT INFORMATION (continued)

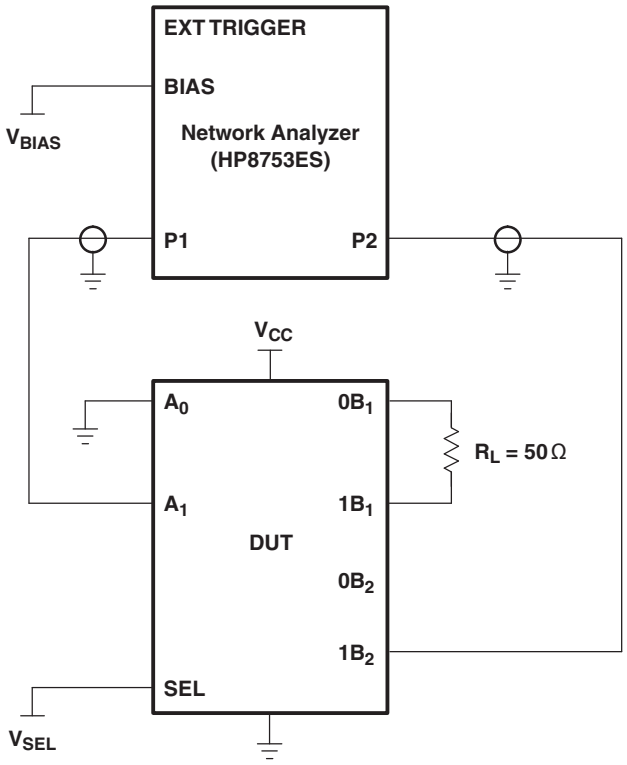


Figure 10. Test Circuit for Off Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = 0 V and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are left open, and output (B) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS2PCIE412RUAR	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SH412
TS2PCIE412RUAR.A	Active	Production	WQFN (RUA) | 42	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SH412

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

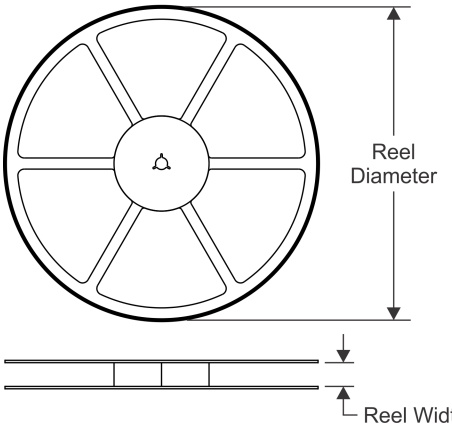
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

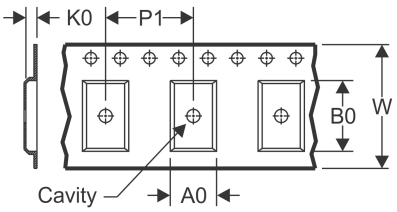
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

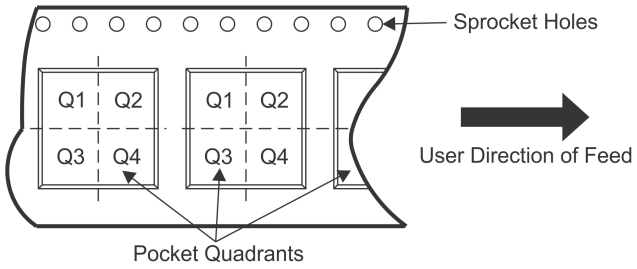


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

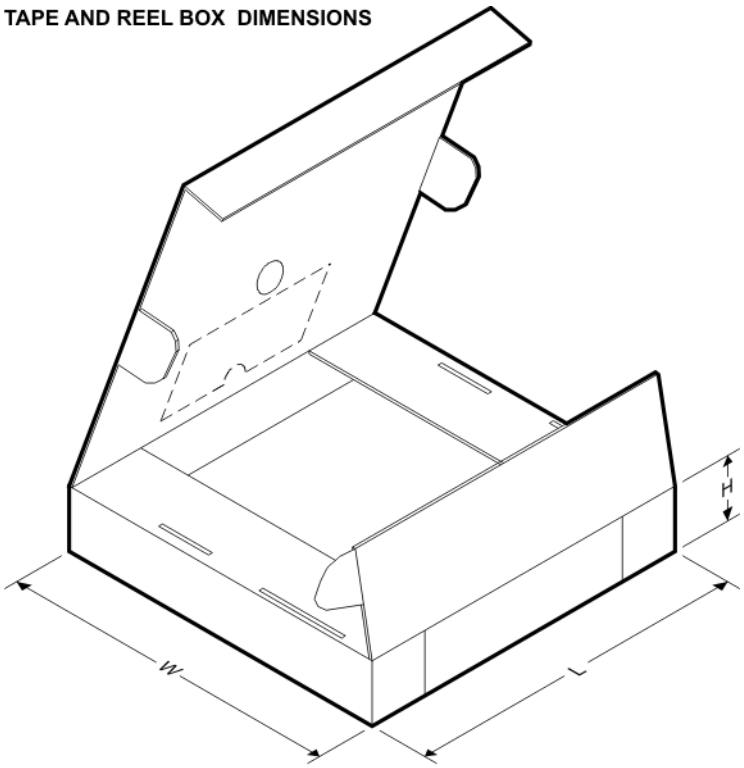
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS2PCIE412RUAR	WQFN	RUA	42	3000	330.0	24.4	3.9	9.4	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS2PCIE412RUAR	WQFN	RUA	42	3000	346.0	346.0	35.0

GENERIC PACKAGE VIEW

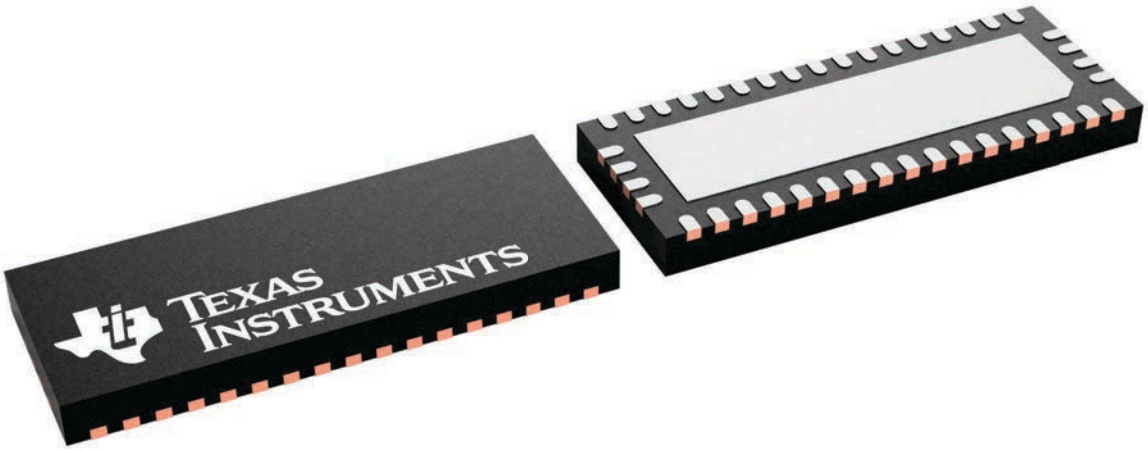
RUA 42

WQFN - 0.8 mm max height

9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

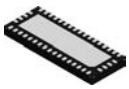
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A

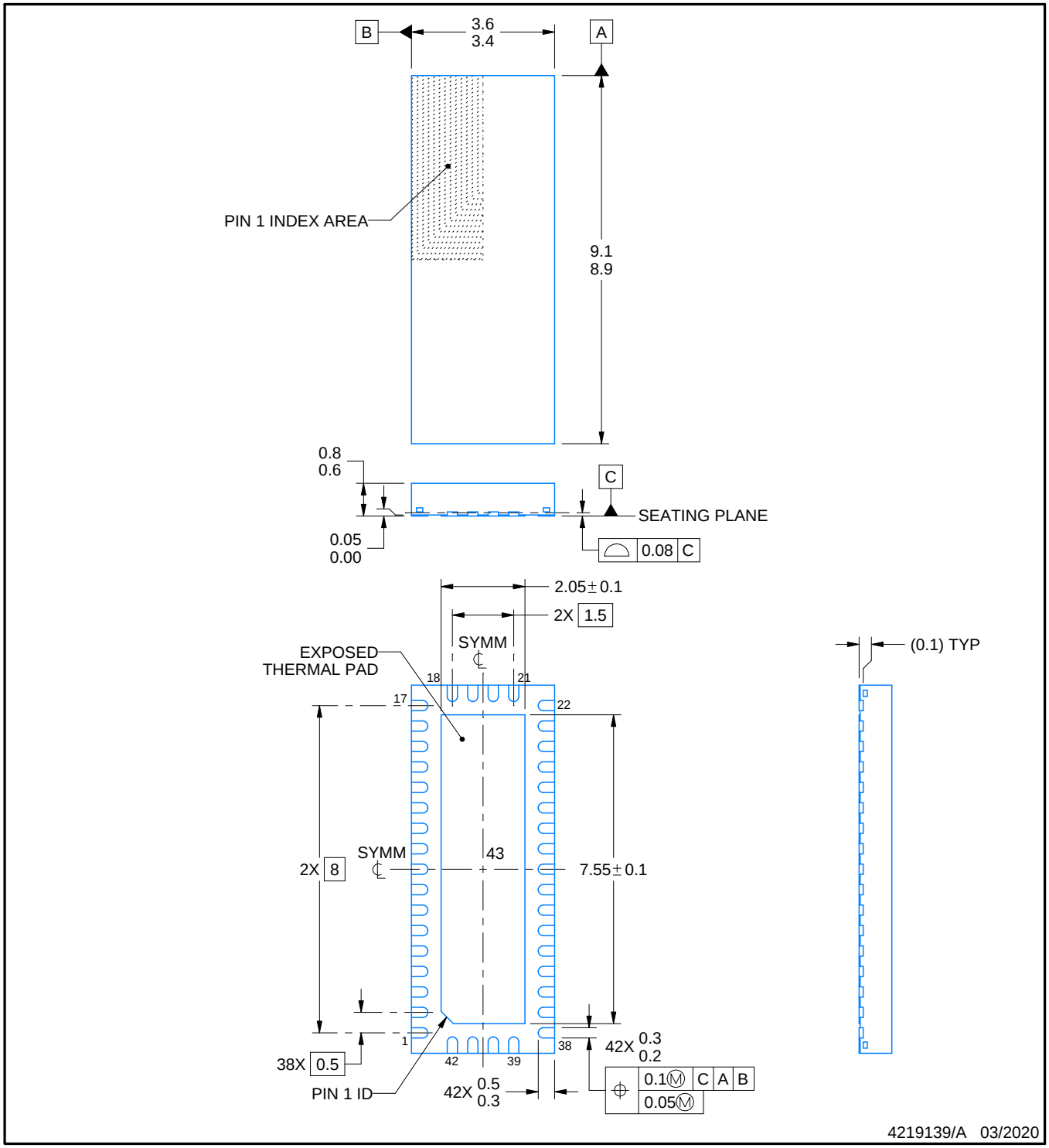
PACKAGE OUTLINE

RUA0042A



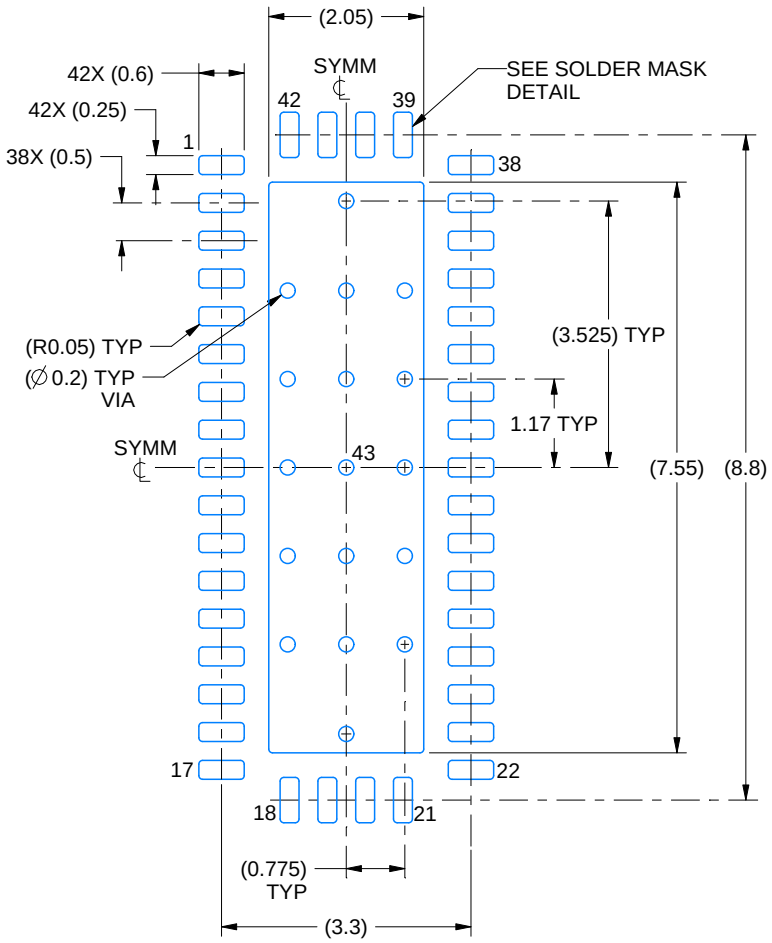
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

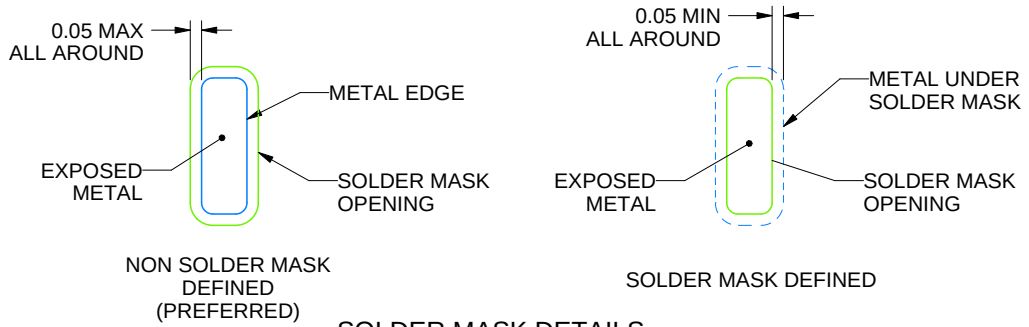


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

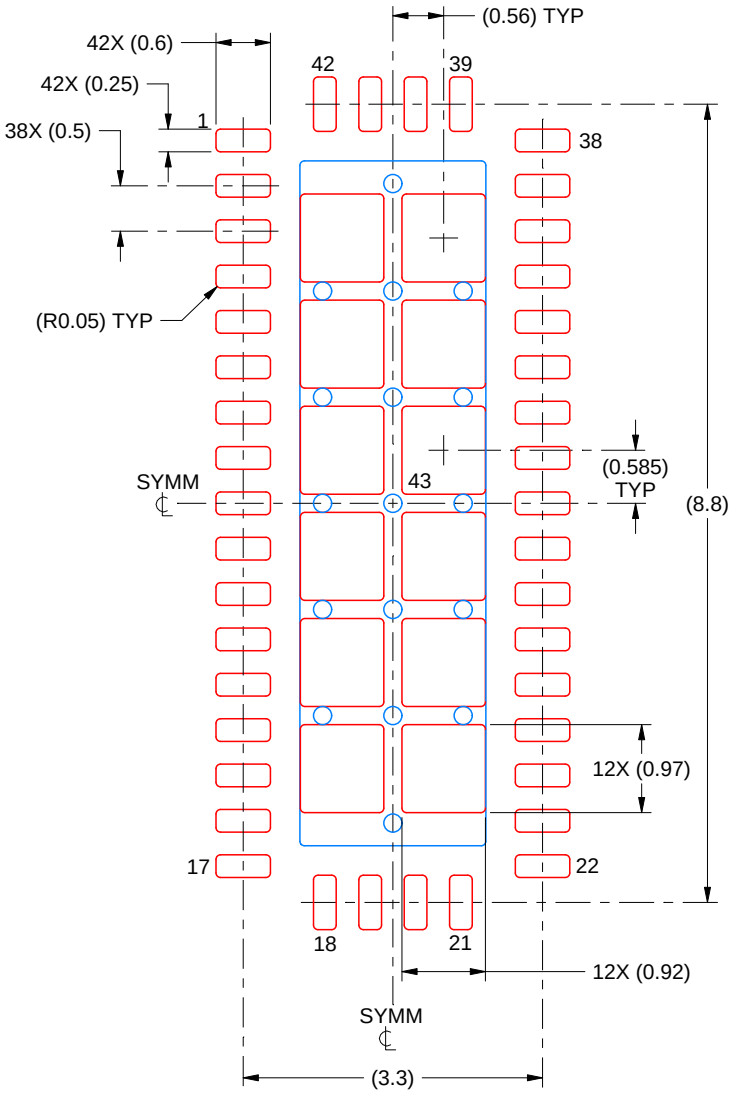
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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