



## CLASS-G DIRECTPATH™ STEREO HEADPHONE AMPLIFIER

Check for Samples: [TPA6141A2](#)

### FEATURES

- **TI Class-G Technology Significantly Prolongs Battery Life and Music Playback Time**
  - **0.6 mA / Ch Quiescent Current**
  - **50% to 80% Lower Quiescent Current Than Ground-Referenced Class-AB Headphone Amplifiers**
- **DirectPath™ Technology Eliminates Large Output DC-Blocking Capacitors**
  - **Outputs Biased at 0 V**
  - **Improves Low Frequency Audio Fidelity**
- **Active Click and Pop Suppression**
- **Fully Differential Inputs Reduce System Noise**
  - **Also Configurable as Single-Ended Inputs**
- **SGND Pin Eliminates Ground Loop Noise**
- **Wide Power Supply Range: 2.5 V to 5.5 V**
- **100 dB Power Supply Noise Rejection**
- **Built-in Input Low Pass Filter**
- **Gain Settings: 0 dB and 6dB**
- **Short-Circuit Current Limiter**
- **Thermal-Overload Protection**
- **±8 kV HBM ESD Protected Outputs**
- **0,4 mm Pitch, 1,6 mm × 1,6 mm 16-Bump WCSP (YFF) Package**

### APPLICATIONS

- **Cellular Phones / Music Phones**
- **Smart Phones**
- **Portable Media / MP3 Players**
- **Portable CD / DVD Players**

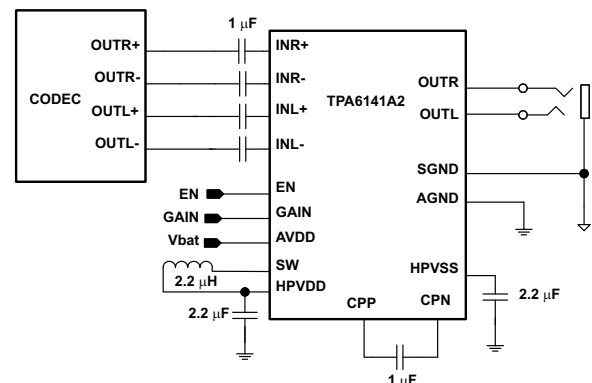
### DESCRIPTION

The TPA6141A2 (also known as TPA6141) is a Class-G DirectPath™ stereo headphone amplifier with selectable gain. Class-G technology maximizes battery life by adjusting the voltage supplies of the headphone amplifier based on the audio signal level. At low level audio signals, the internal supply voltage is reduced to minimize power dissipation. DirectPath™ technology eliminates external DC-blocking capacitors.

The device features fully differential inputs with an integrated low pass filter to reduce system noise pickup between the audio source and the headphone amplifier and to reduce DAC out-of-band noise. The high power supply noise rejection performance and differential architecture provides increased RF noise immunity. For single-ended input signals, connect INL+ and INR+ to ground.

The device operates from a 2.5 V to 5.5 V supply voltage. Class-G operation keeps total supply current below 5.0 mA while delivering 500  $\mu$ W per channel into 32  $\Omega$ . Shutdown mode reduces the supply current to less than 3  $\mu$ A and is activated through the EN pin.

The device has built-in pop suppression circuitry to completely eliminate disturbing pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection along with  $\pm 8$  kV HBM ESD protection, simplifying end equipment compliance to the IEC 61000-4-2 ESD standard.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

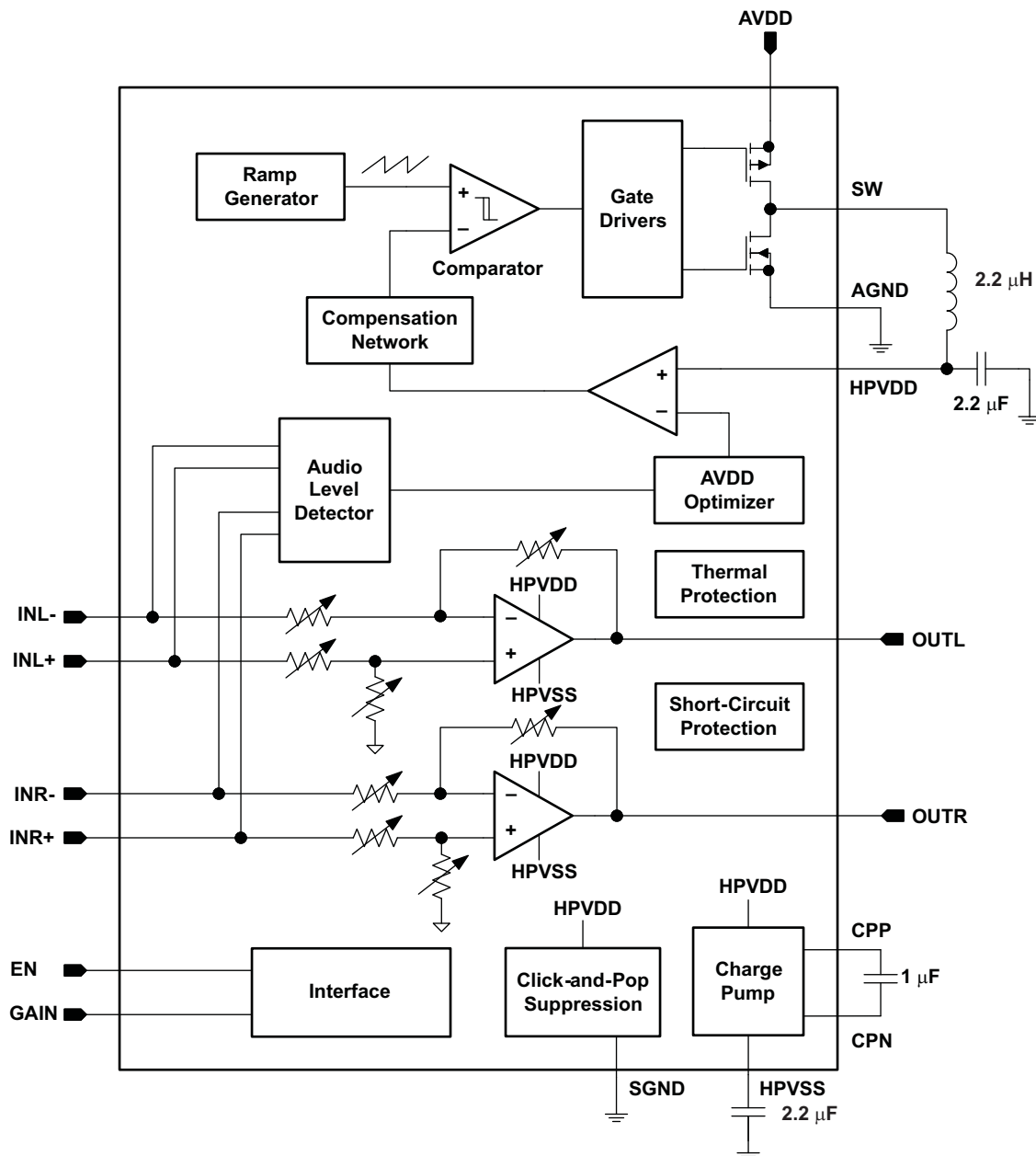
Class-G DirectPath, DirectPath are trademarks of Texas Instruments.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

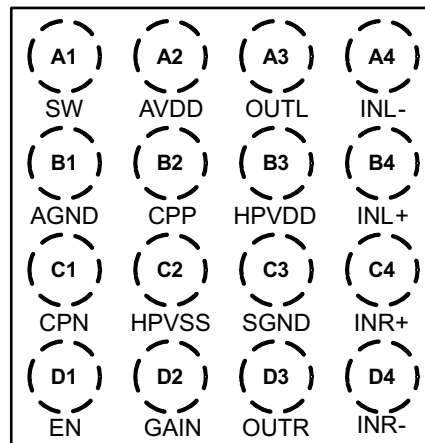
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### FUNCTIONAL BLOCK DIAGRAM



## DEVICE PINOUT

**WCSP PACKAGE  
(TOP VIEW)**



## TERMINAL FUNCTIONS

| TERMINAL |              | INPUT /<br>OUTPUT /<br>POWER<br>(I/O/P) | DESCRIPTION                                                                                                                                    |
|----------|--------------|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME     | BALL<br>WCSP |                                         |                                                                                                                                                |
| INL-     | A4           | I                                       | Inverting left input for differential signals. Connect to left input signal through 1 $\mu$ F capacitor for single-ended input applications.   |
| INL+     | B4           | I                                       | Non-inverting left input for differential signals. Connect to ground through 1 $\mu$ F capacitor for single-ended input applications.          |
| INR+     | C4           | I                                       | Non-inverting right input for differential signals. Connect to ground through 1 $\mu$ F capacitor for single-ended input applications.         |
| INR-     | D4           | I                                       | Inverting right input for differential signals. Connect to right input signal through 1 $\mu$ F capacitor for single-ended input applications. |
| SGND     | C3           | I                                       | Sense ground. Connect to shield terminal of headphone jack.                                                                                    |
| EN       | D1           | I                                       | Amplifier enable. Connect to logic low to shutdown; connect to logic high to activate.                                                         |
| GAIN     | D2           | I                                       | Amplifier gain select pin. Connect to logic low to select a gain of 0 dB; connect to logic high to select a gain of 6 dB.                      |
| OUTL     | A3           | O                                       | Left headphone amplifier output. Connect to left terminal of headphone jack.                                                                   |
| OUTR     | D3           | O                                       | Right headphone amplifier output. Connect to right terminal of headphone jack.                                                                 |
| CPP      | B2           | P                                       | Charge pump positive flying cap. Connect to positive side of capacitor between CPP and CPN.                                                    |
| CPN      | C1           | P                                       | Charge pump negative flying cap. Connect to negative side of capacitor between CPP and CPN.                                                    |
| SW       | A1           | P                                       | Buck converter switching node.                                                                                                                 |
| AVDD     | A2           | P                                       | Primary power supply for device.                                                                                                               |
| HPVDD    | B3           | P                                       | Power supply for headphone amplifier (DC/DC output node).                                                                                      |
| AGND     | B1           | P                                       | Main Ground for headphone amplifiers, DC/DC converter, and charge pump.                                                                        |
| HPVSS    | C2           | P                                       | Charge pump output. Connect 2.2 $\mu$ F capacitor to GND.                                                                                      |

## ORDERING INFORMATION

| T <sub>A</sub> | PACKAGED DEVICES <sup>(1)</sup> | PART NUMBER <sup>(2)</sup> | SYMBOL |
|----------------|---------------------------------|----------------------------|--------|
| -40°C to 85°C  | 16-ball, WCSP                   | TPA6141A2YFFR              | ASBI   |
|                | 16-ball, WCSP                   | TPA6141A2YFFT              | ASBI   |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

(2) YFF packages are only available taped and reeled. The suffix "R" indicates a reel of 3000, the suffix "T" indicates a reel of 250.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**over operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

|                                           |                                        | VALUE / UNIT                       |
|-------------------------------------------|----------------------------------------|------------------------------------|
| Supply voltage, AVDD                      |                                        | –0.3 V to 6.0 V                    |
| Amplifier supply voltage, HPVDD           |                                        | –0.3 V to 2.0 V                    |
| $V_I$                                     | Input voltage (INR+, INR-, INL+, INL-) | –0.3 V to HPV <sub>DD</sub> +0.3 V |
| Control input voltage (EN, GAIN)          |                                        | –0.3 V to AVDD                     |
| Output continuous total power dissipation |                                        | See Dissipation Rating Table       |
| $T_A$                                     | Operating free-air temperature range   | –40°C to 85°C                      |
| $T_J$                                     | Operating junction temperature range   | –40°C to 150°C                     |
| $T_{stg}$                                 | Storage temperature range              | –65°C to 85°C                      |
| $R_L$                                     | Minimum load resistance                | 12 $\Omega$                        |
| ESD Protection – HBM                      | OUTL, OUTR, SGND                       | 8 kV                               |
|                                           | All other pins                         | 2 kV                               |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

**DISSIPATION RATINGS TABLE<sup>(1) (2)</sup>**

| PACKAGE    | $T_A < 25^\circ\text{C}$<br>POWER RATING | OPERATING<br>FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>POWER RATING |
|------------|------------------------------------------|-------------------------------------------------------|------------------------------------------|------------------------------------------|
| YFF (WCSP) | 1.25 W                                   | 10 mW/°C                                              | 800 mW                                   | 650 mW                                   |

- (1) Derating factor measured with JEDEC High K board: 1S0P – One signal layer and zero plane layers.  
 (2) See JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information. See JEDEC document page for downloadable copies: <http://www.jedec.org/download/default.cfm>.

**RECOMMENDED OPERATING CONDITIONS**

|                                                             |                                |          | MIN  | MAX | UNIT |
|-------------------------------------------------------------|--------------------------------|----------|------|-----|------|
| V <sub>DD</sub>                                             | Supply voltage, AVDD           |          | 2.5  | 5.5 | V    |
| V <sub>IH</sub>                                             | High-level input voltage       | EN, GAIN | 1.3  |     | V    |
| V <sub>IL</sub>                                             | Low-level input voltage        | EN, GAIN |      | 0.6 | V    |
| Voltage applied to Output; OUTR, OUTL (when EN = logic low) |                                |          | −0.3 | 3.6 |      |
| T <sub>A</sub>                                              | Operating free-air temperature |          | −40  | +85 | °C   |

## ELECTRICAL CHARACTERISTICS

 $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

| PARAMETER  |                              | TEST CONDITIONS                                                                                           | MIN | TYP | MAX | UNIT          |
|------------|------------------------------|-----------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| PSRR       | Power supply rejection ratio | AVDD = 2.5 V to 5.5 V, inputs grounded, GAIN = 0 dB                                                       | 90  | 105 |     | dB            |
| CMRR       | Common mode rejection ratio  | HPVDD = 1.3 V to 1.8 V, GAIN = 0 dB                                                                       |     | 68  |     | dB            |
| $ I_{IH} $ | High-level input current     | AVDD = 2.5 V to 5.5 V, $V_I = \text{AVDD}$                                                                |     |     | 1   | $\mu\text{A}$ |
| $ I_{IL} $ | Low-level input current      | AVDD = 2.5 V to 5.5 V, $V_I = 0\text{ V}$                                                                 |     |     | 1   | $\mu\text{A}$ |
| $I_{SD}$   | Shutdown current             | EN = 0 V, AVDD = 2.5 V to 5.5 V                                                                           |     | 1   | 3   | $\mu\text{A}$ |
| $I_{DD}$   | Total supply current         | AVDD = 3.6 V HPVDD = 1.3 V, Amplifiers active, no load, no input signal                                   |     | 1.2 | 2.0 | mA            |
|            |                              | AVDD = 3.6 V, $P_{OUT} = 100\text{ }\mu\text{W}$ into $32\text{ }\Omega^{(1)}$ , $f_{AUD} = 1\text{ kHz}$ |     | 2.5 |     |               |
|            |                              | AVDD = 3.6 V, $P_{OUT} = 500\text{ }\mu\text{W}$ into $32\text{ }\Omega^{(1)}$ , $f_{AUD} = 1\text{ kHz}$ |     | 4.0 |     |               |
|            |                              | AVDD = 3.6 V, $P_{OUT} = 1\text{ mW}$ into $32\text{ }\Omega^{(1)}$ , $f_{AUD} = 1\text{ kHz}$            |     | 6.8 |     |               |

(1) Per channel output power assuming a 10 dB crest factor

## OPERATING CHARACTERISTICS

 $\text{AV}_{DD} = 3.6\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ , GAIN = 0 dB,  $R_L = 32\text{ }\Omega$  (unless otherwise noted)

| PARAMETER    |                                                     | TEST CONDITIONS                                                   | MIN | TYP   | MAX | UNIT                |
|--------------|-----------------------------------------------------|-------------------------------------------------------------------|-----|-------|-----|---------------------|
| $P_O$        | Output power <sup>(1)</sup> (Outputs in Phase)      | AVDD = 2.7 V, THD = 1%, $f = 1\text{ kHz}$                        |     | 26    |     | mW                  |
|              |                                                     | AVDD = 2.7 V, THD = 10%, $f = 1\text{ kHz}$                       |     | 32    |     |                     |
|              |                                                     | AVDD = 2.7 V, THD = 1%, $f = 1\text{ kHz}$ , $R_L = 16\Omega$     |     | 25    |     |                     |
| THD+N        | Total harmonic distortion plus noise <sup>(2)</sup> | $P_O = 10\text{ mW}$ into $16\text{ }\Omega$ , $f = 1\text{ kHz}$ |     | 0.02% |     |                     |
|              |                                                     | $P_O = 20\text{ mW}$ into $32\text{ }\Omega$ , $f = 1\text{ kHz}$ |     | 0.01% |     |                     |
| $k_{SVR}$    | AC-Power supply rejection ratio                     | 200 mVpp ripple, $f = 217\text{ Hz}$                              | 80  | 100   |     | dB                  |
|              |                                                     | 200 mVpp ripple, $f = 4\text{ kHz}$                               |     | 90    |     |                     |
| $A_V$        | Closed-loop voltage gain (OUT / IN–)                | GAIN = logic low                                                  |     | 0     |     | dB                  |
|              |                                                     | GAIN = logic high                                                 |     | 6     |     | dB                  |
| $\Delta A_V$ | Gain matching                                       | Between left and right channels                                   |     | 1%    |     |                     |
| $V_{OS}$     | Output offset voltage                               | AVDD = 2.5 V to 5.5 V, inputs grounded                            | 0.5 | 0     | 0.5 | mV                  |
| $E_N$        | Noise output voltage                                | A-weighted                                                        |     | 5.3   |     | $\mu\text{V}_{RMS}$ |
| $f_{BUCK}$   | Buck converter switching frequency                  | $P_O = 0.5\text{ mW}$ , $f = 1\text{ kHz}$                        |     | 600   |     | kHz                 |
| $f_{PUMP}$   | Charge pump switching frequency                     | $P_O = 0.5\text{ mW}$ , $f = 1\text{ kHz}$                        |     | 315   |     | kHz                 |
|              |                                                     | $P_O = 15\text{ mW}$ , $f = 1\text{ kHz}$                         |     | 1260  |     |                     |
|              | Start-up time from shutdown                         |                                                                   |     | 5     |     | ms                  |
| $R_{IN,SE}$  | Single Ended Input impedance                        | Gain = 6 dB, per input node                                       |     | 13.2  |     | k $\Omega$          |
| $R_{IN,DF}$  | Differential input impedance                        | Gain = 6 dB, per input node                                       |     | 26.4  |     | k $\Omega$          |
| SNR          | Signal-to-noise ratio                               | $V_{OUT} = 1\text{ V}_{RMS}$ , GAIN = 6 dB, no load               |     | 105   |     | dB                  |
|              | Thermal shutdown                                    | Threshold                                                         |     | 165   |     | $^{\circ}\text{C}$  |
|              |                                                     | Hysteresis                                                        |     | 35    |     |                     |
| $Z_{O,SD}$   | Output impedance in shutdown                        | EN = logic low, DC value                                          |     | 8     |     | k $\Omega$          |
|              | Input to Output attenuation in shutdown             | EN = logic low, $f = 1\text{ kHz}$ , $V_{OUT} = 1\text{ V}_{RMS}$ |     | 90    |     | dB                  |
|              | Crosstalk                                           | $P_O = 15\text{ mW}$ , $f = 1\text{ kHz}$                         |     | –80   |     | dB                  |
| $V_{CM}$     | Input common-mode voltage range                     |                                                                   | 0   |       | 1.4 | V                   |

(1) Per channel output power

(2) A-weighted

## TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $AV_{DD} (V_{DD}) = 3.6\text{ V}$ ,  $GAIN = 0\text{ dB}$ ,  $C_{HPVDD} = C_{HPVSS} = 2.2\text{ }\mu\text{F}$ ,  $C_{INPUT} = C_{FLYING} = 1\text{ }\mu\text{F}$ , Outputs out of phase

**QUIESCENT SUPPLY CURRENT  
vs  
SUPPLY VOLTAGE**

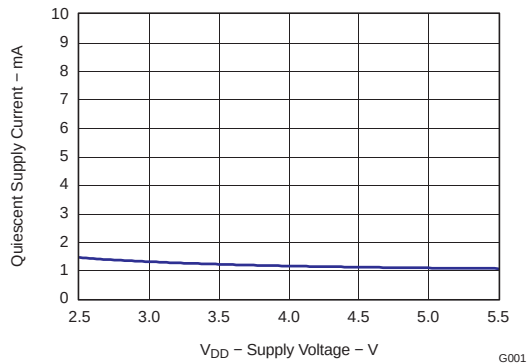


Figure 1.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
OUTPUT POWER**

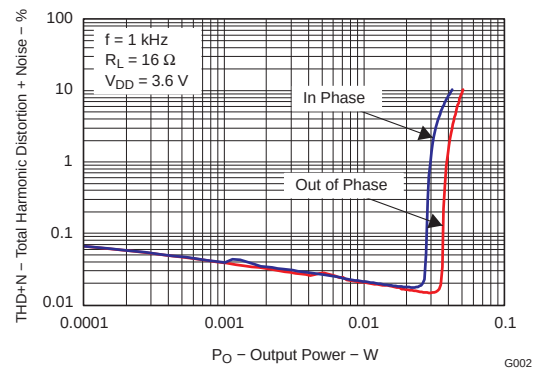


Figure 2.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
OUTPUT POWER**

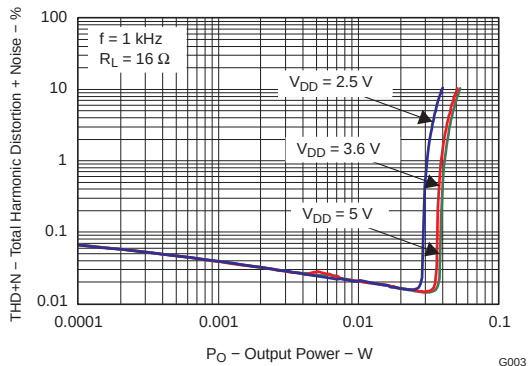


Figure 3.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
OUTPUT POWER**

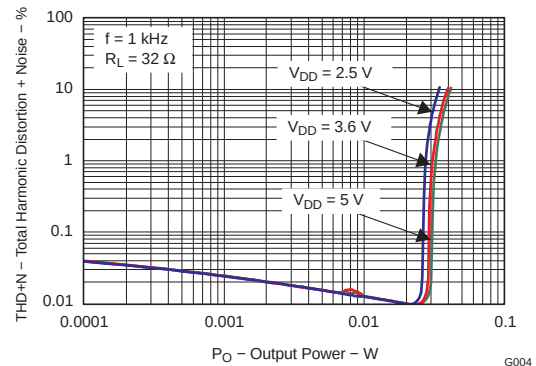


Figure 4.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

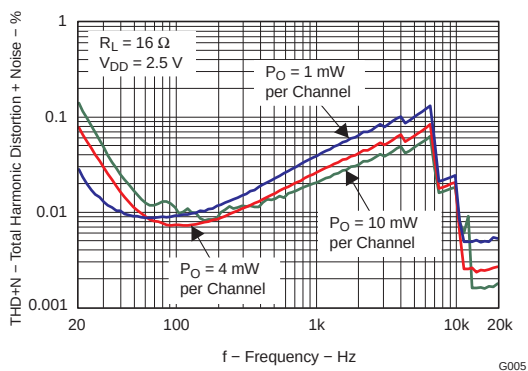


Figure 5.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

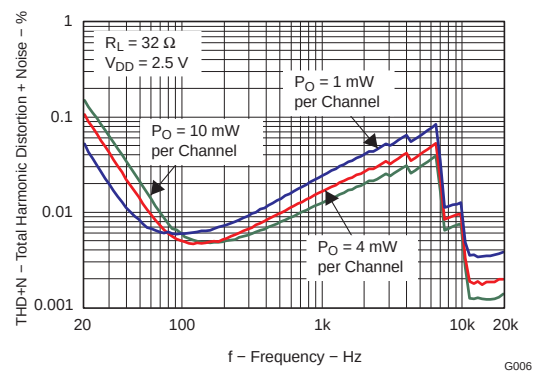


Figure 6.

## TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$ ,  $AV_{DD} (V_{DD}) = 3.6\text{ V}$ ,  $GAIN = 0\text{ dB}$ ,  $C_{HPVDD} = C_{HPVSS} = 2.2\text{ }\mu\text{F}$ ,  $C_{INPUT} = C_{FLYING} = 1\text{ }\mu\text{F}$ , Outputs out of phase

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

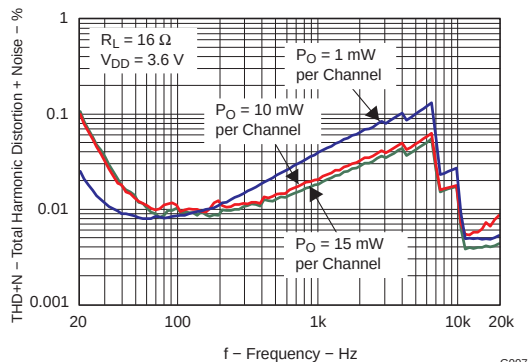


Figure 7.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

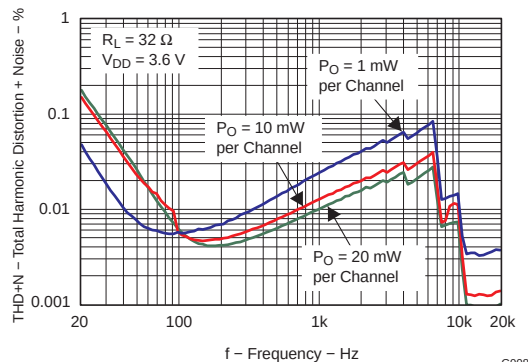


Figure 8.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

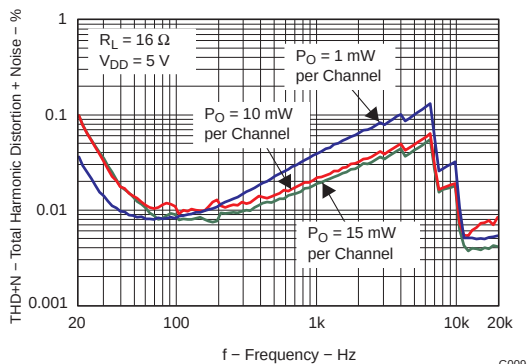


Figure 9.

**TOTAL HARMONIC DISTORTION + NOISE  
vs  
FREQUENCY**

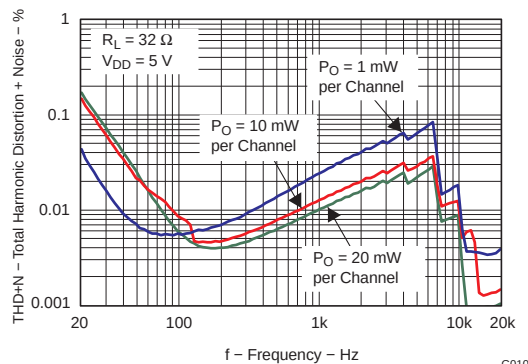


Figure 10.

**OUTPUT POWER PER CHANNEL  
vs  
SUPPLY VOLTAGE**

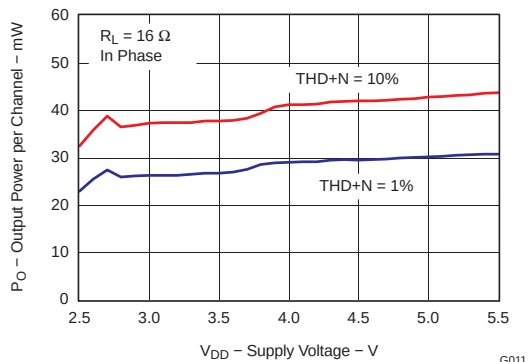


Figure 11.

**OUTPUT POWER PER CHANNEL  
vs  
SUPPLY VOLTAGE**

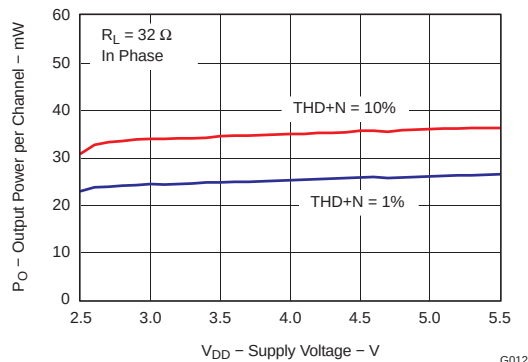


Figure 12.

### TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$ ,  $AV_{DD} (V_{DD}) = 3.6\text{ V}$ ,  $\text{GAIN} = 0\text{ dB}$ ,  $C_{HPVDD} = C_{HPVSS} = 2.2\text{ }\mu\text{F}$ ,  $C_{INPUT} = C_{FLYING} = 1\text{ }\mu\text{F}$ , Outputs out of phase

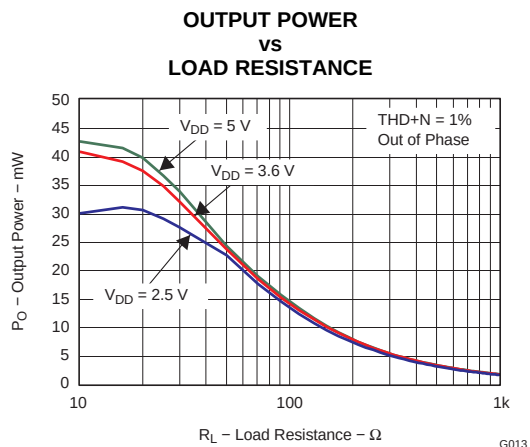


Figure 13.

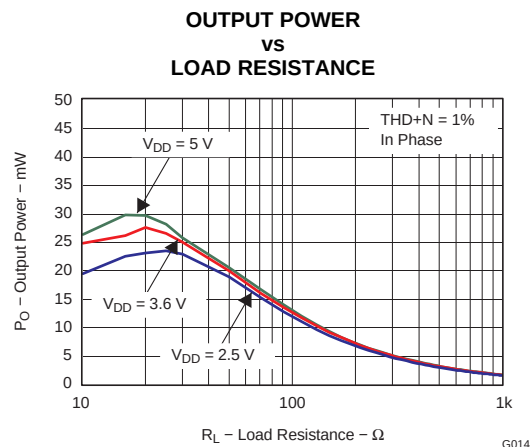


Figure 14.

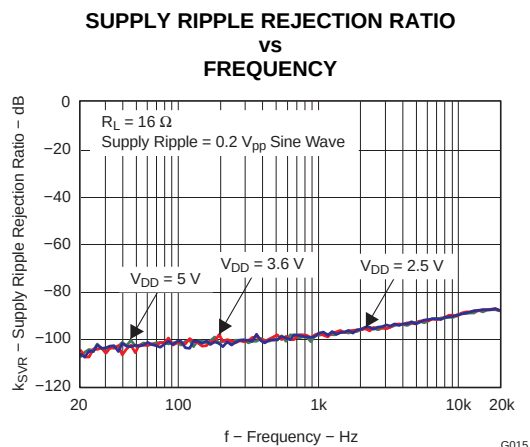


Figure 15.

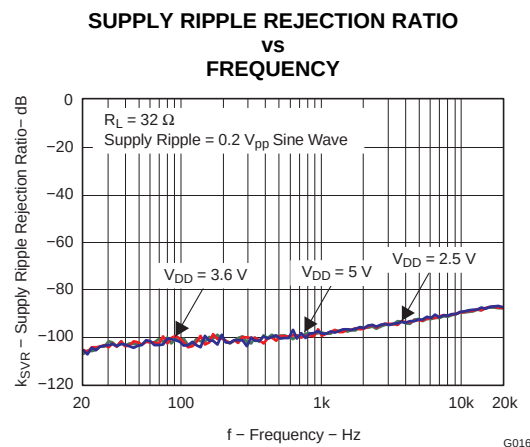


Figure 16.

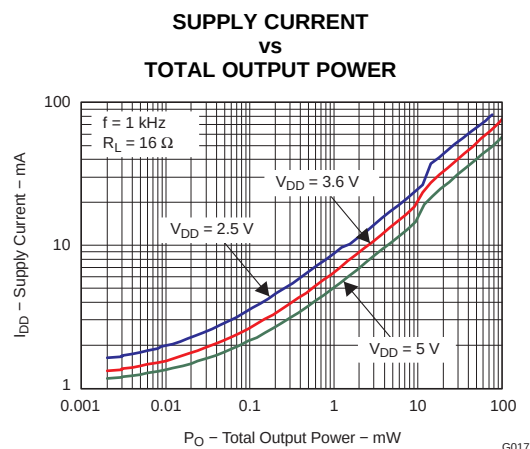


Figure 17.

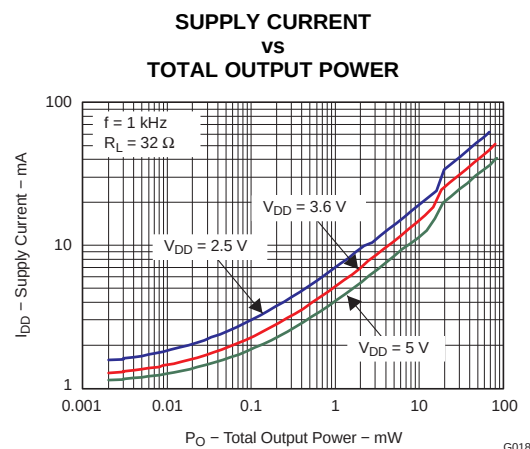


Figure 18.

## TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$ ,  $AV_{DD} (V_{DD}) = 3.6\text{ V}$ ,  $GAIN = 0\text{ dB}$ ,  $C_{HPVDD} = C_{HPVSS} = 2.2\text{ }\mu\text{F}$ ,  $C_{INPUT} = C_{FLYING} = 1\text{ }\mu\text{F}$ , Outputs out of phase

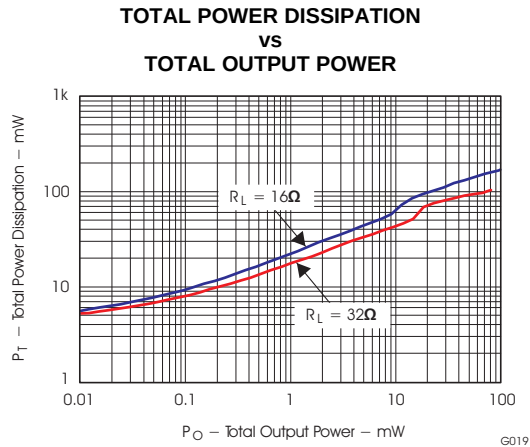


Figure 19.

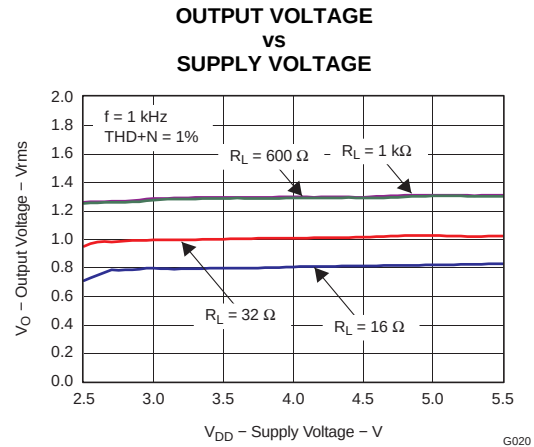


Figure 20.

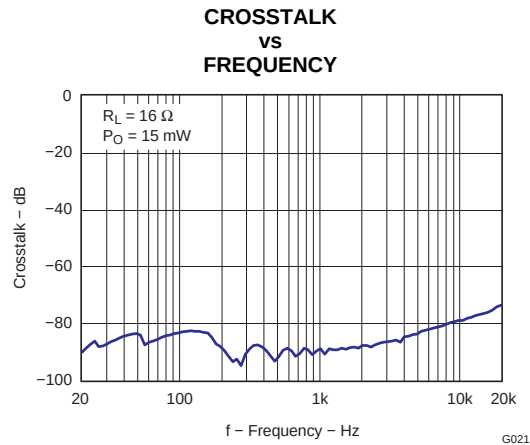


Figure 21.

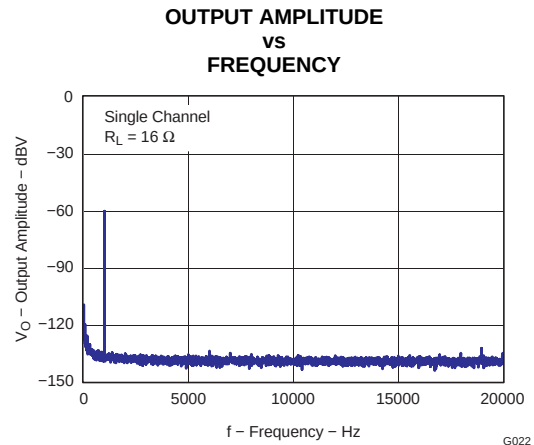


Figure 22.

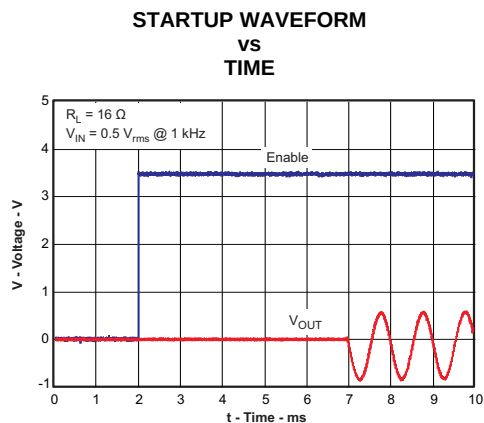


Figure 23.

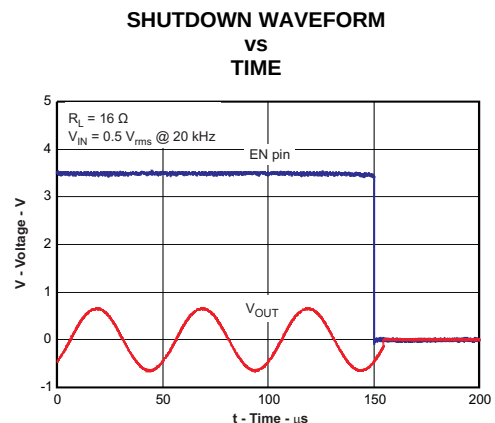


Figure 24.

## APPLICATION INFORMATION

## APPLICATION CIRCUIT

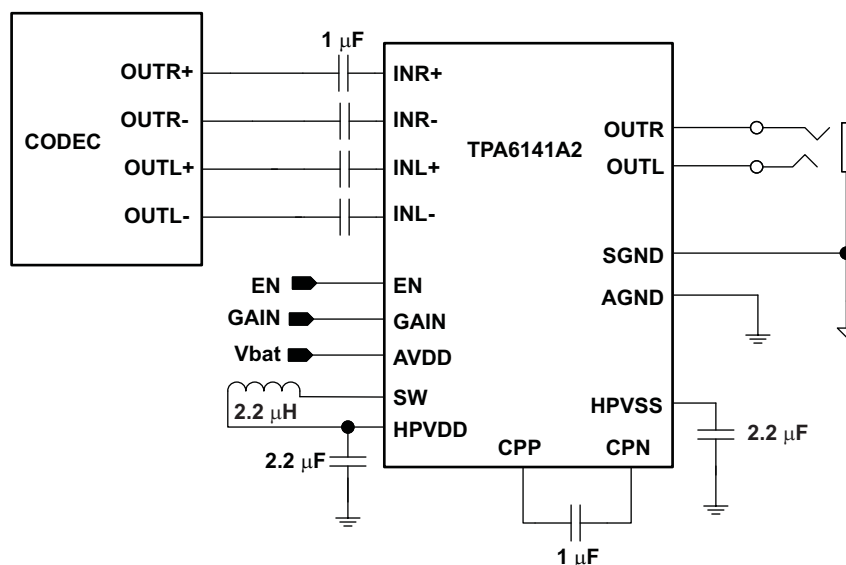


Figure 25. Typical Application Configuration with Differential Input Signals

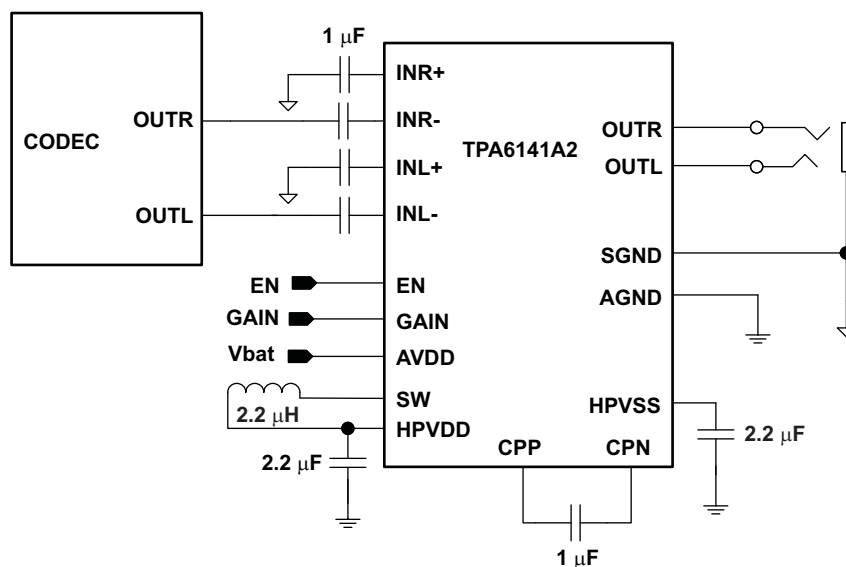


Figure 26. Typical Application Configuration with Single-Ended Input Signals

## CLASS-G HEADPHONE AMPLIFIER

Class-G amplifiers use adaptive supply rails. The TPA6141A2 includes a built-in step-down converter to create the headphone amplifier positive supply voltage, HPVDD. A charge pump inverts HPVDD and creates the amplifier negative supply voltage, HPVSS. This allows the headphone amplifier output to be centered at 0 V.

When audio signal amplitude is low, the step-down converter generates a low HPVDD voltage. This minimizes TPA6141A2 power consumption while playing low noise, high fidelity audio. If audio amplitude increases, either due to louder music or a transient peak, then the step-down converter generates a higher HPVDD voltage. The HPVDD rise rate is faster than the audio peak rise time. This prevents audio distortion or clipping. Audio quality and noise floor are not affected by HPVDD.

This adaptive HPVDD minimizes TPA6141A2 supply current while avoiding clipping and distortion. Because normal listening levels are below 200 mV<sub>RMS</sub>, HPVDD is most often at its lowest voltage. Thus, the TPA6141A2 has higher efficiency than traditional Class-AB headphone amplifiers.

The following equations compare a Class-AB amplifier to a Class-G amplifier. Both operate with identical battery voltage, load impedance, and output voltage swing. For this study case, we assume a normal listening level of 200 mV<sub>RMS</sub> with no DirectPath™ in order to simplify the calculations.

- P<sub>SUP</sub>: Supplied power
- V<sub>SUP</sub>: Supply voltage
- I<sub>SUP</sub>: Supply current
- V<sub>REG</sub>: DC/DC converter output voltage
- P<sub>REG</sub>: DC/DC converter output power
- V<sub>LOAD</sub>: Voltage across the load
- R<sub>LOAD</sub>: Load impedance
- P<sub>LOAD</sub>: Power dissipated at the load
- I<sub>LOAD</sub>: Current supplied to the load

Given an amplifier driving 200 mV<sub>RMS</sub> into a 32 Ω load, the output current to the load is:

$$I_{LOAD} = \frac{V_{LOAD}}{R_{LOAD}} = \frac{200 \text{ mV}_{RMS}}{32 \Omega} = 6.25 \text{ mA} \quad (1)$$

Assuming a quiescent current of 1 mA (I<sub>DDQ</sub>) the total current supplied to the amplifier is:

$$I_{SUP} = I_{LOAD} + I_{DDQ} = 7.25 \text{ mA} \quad (2)$$

The total power supplied to a Class-AB amplifier is then calculated as:

$$P_{SUP} = V_{SUP} \times I_{SUP} = 4.2 \text{ V} \times 7.25 \text{ mA} = 30.45 \text{ mW} \quad (3)$$

For a Class-G amplifier where the voltage rails are generated by a switching DC/DC converter, the supplied power will depend on the DC/DC converter output voltage and efficiency. Assuming the DC/DC converter output voltage is 1.3 V:

$$P_{REG} = V_{REG} \times I_{SUP} = 1.3 \text{ V} \times 7.25 \text{ mA} = 9.425 \text{ mW} \quad (4)$$

The total supplied power will be the DC/DC converter output power divided by the efficiency of the DC/DC converter. Assuming 90% step-down efficiency, total power supplied to the Class-G amplifier is:

$$P_{SUP} = \frac{P_{REG}}{90\%} = 11.09 \text{ mW} \quad (5)$$

Class-G headphone amplifiers achieve much higher efficiency than equivalent Class-AB amplifiers.

## INDUCTOR SELECTION

The TPA6141A2 requires one inductor for its DC/DC converter. The following table lists recommended inductors. Inductors not shown on this table can be used if they have similar performance characteristics.

When selecting an inductor observe the following rules:

- Lower DCR increases DC/DC converter efficiency.
- The minimum working inductance should never be below 1  $\mu\text{H}$ .
- Include temperature and aging derating factors into the inductor value calculations.

| MANUFACTURER | PART NUMBER    |
|--------------|----------------|
| TOKO         | MDT2012-CH2R2A |
| Murata       | LQM21PN2R2MC0D |
|              | LQH2MCN2R2M02L |
| Taiyo Yuden  | BRL2012T2R2M   |
|              | BRC1608T2R2M   |

## GAIN CONTROL

The TPA6141A2 has two gain settings which are controlled with the GAIN pin. The following table gives an overview of the gain function.

| GAIN VOLTAGE        | AMPLIFIER GAIN |
|---------------------|----------------|
| $\leq 0.6\text{ V}$ | 0 dB           |
| $\geq 1.3\text{ V}$ | 6 dB           |

## GROUND SENSE FUNCTION

The ground sense pin, SGND, reduces ground-loop noise when the audio output jack is connected to a different ground reference than codec and amplifier ground. Always connect the SGND pin to the headphone jack. This reduces output offset voltage and eliminates turn-on pop. Figure 27 shows how to connect SGND when an FM radio antenna function is implemented on the headphone wire. The nH coil and capacitor separate the RF signal from the audio GND signal. In this case, SGND is used to eliminate the offset voltage that is generated from the audio signal current and the RF coil low-frequency impedance.

The voltage difference between SGND and AGND cannot be greater than  $\pm 300\text{ mV}$ . The amplifier performance degrades if the voltage difference between SGND and AGND is greater than  $\pm 300\text{ mV}$ .

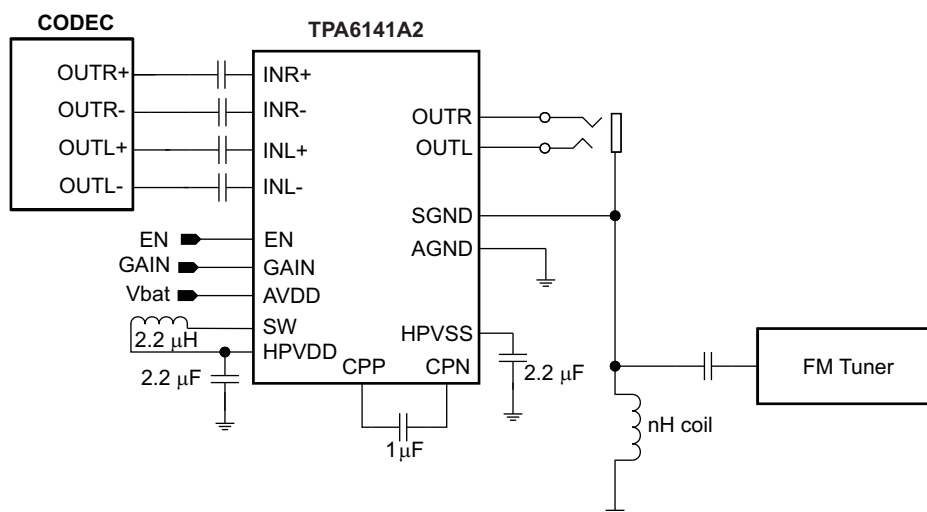


Figure 27. Sense Ground

## HEADPHONE AMPLIFIERS

Single-supply headphone amplifiers typically require dc-blocking capacitors to remove dc bias from their output voltage. The top drawing in [Figure 28](#) illustrates this connection. If dc bias is not removed, large dc current will flow through the headphones which wastes power, clips the output signal, and potentially damages the headphones.

These dc-blocking capacitors are often large in value and size. Headphone speakers have a typical resistance between 16  $\Omega$  and 32  $\Omega$ . This combination creates a high-pass filter with a cutoff frequency as shown in [Equation 6](#), where  $R_L$  is the load impedance,  $C_O$  is the dc-block capacitor, and  $f_C$  is the cutoff frequency.

$$f_C = \frac{1}{2\pi R_L C_O} \quad (6)$$

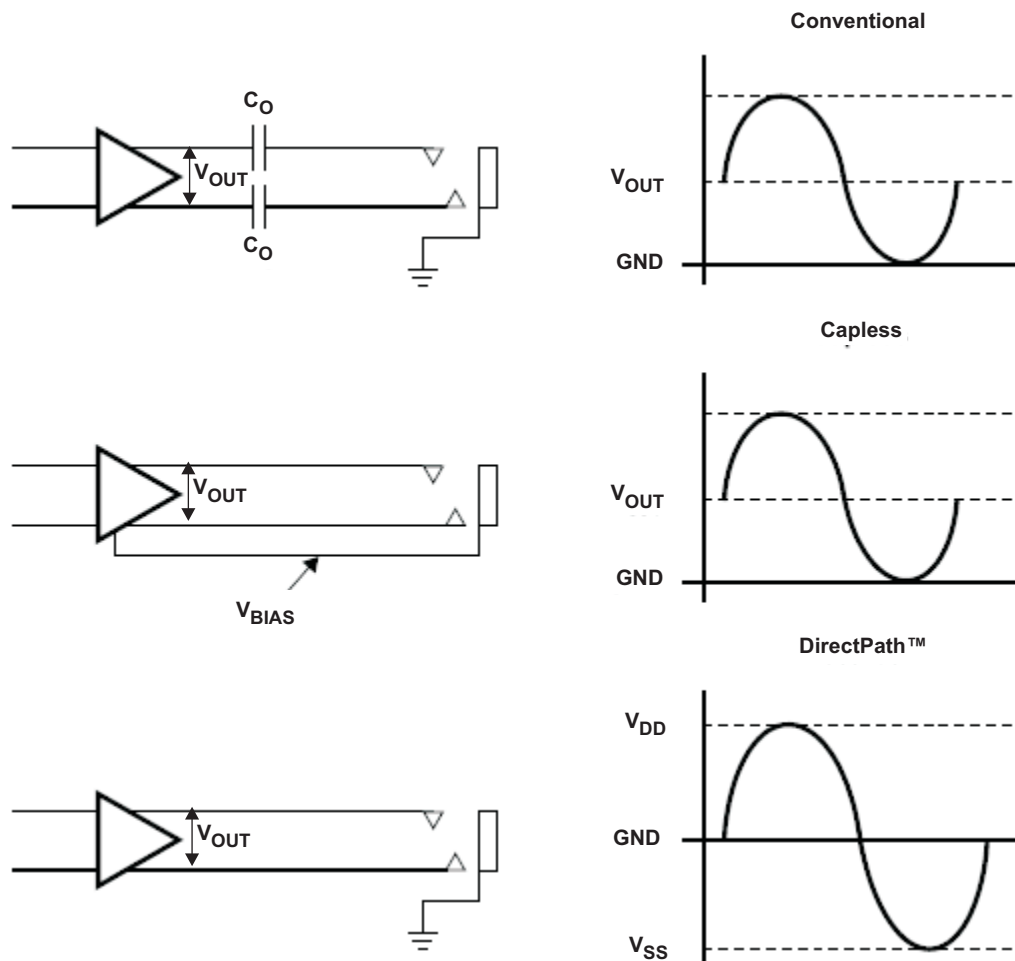
For a given high-pass cutoff frequency and load impedance, the required dc-blocking capacitor is found as:

$$C_O = \frac{1}{2\pi f_C R_L} \quad (7)$$

Reducing  $f_C$  improves low frequency fidelity and requires a larger dc-blocking capacitor. To achieve a 20 Hz cutoff with 16  $\Omega$  headphones,  $C_O$  must be at least 500  $\mu\text{F}$ . Large capacitor values require large packages, consuming PCB area, increasing height, and increasing cost of assembly. During start-up or shutdown the dc-blocking capacitor has to be charged or discharged. This causes an audible pop on start-up and power-down. Large dc-blocking capacitors also reduce audio output signal fidelity.

Two different headphone amplifier architectures are available to eliminate the need for dc-blocking capacitors. The capless amplifier architecture provides a reference voltage to the headphone connector shield pin as shown in the middle drawing of [Figure 28](#). The audio output signals are centered around this reference voltage, which is typically half of the supply voltage to allow symmetrical output voltage swing.

When using a capless amplifier do not connect the headphone jack shield to any ground reference or large currents will result. This makes capless amplifiers ineffective for plugging non-headphone accessories into the headphone connector. capless amplifiers are useful only with floating GND headphones.

**Figure 28. Amplifier Applications**

The DirectPath™ amplifier architecture operates from a single supply voltage and uses an internal charge pump to generate a negative supply rail for the headphone amplifier. The output voltages are centered around 0 V and are capable of positive and negative voltage swings as shown in the bottom drawing of Figure 28. DirectPath amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The TPA6141A2 is a DirectPath amplifier.

### ELIMINATING TURN-ON POP AND POWER SUPPLY SEQUENCING

The TPA6141A2 has excellent noise and turn-on / turn-off pop performance. It uses an integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5 ms.

DirectPath technology keeps the output dc voltage at 0 V even when the amplifier is powered up. The DirectPath technology together with the active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the TPA6141A2 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the TPA6141A2 before deactivating the audio input source. The EN pin controls device shutdown: Set to  $V_{IL}$  or lower to deactivate the TPA6141A2; set to  $V_{IH}$  or higher to activate. Refer to the Recommended Operating Conditions table for the  $V_{IL}$  and  $V_{IH}$  values.

## RF AND POWER SUPPLY NOISE IMMUNITY

The TPA6141A2 employs a new differential amplifier architecture to achieve high power supply noise rejection and RF noise rejection. RF and power supply noise are common in modern electronics. Although RF frequencies are much higher than the 20 kHz audio band, signal modulation often falls in-band. This, in turn, modulates the supply voltage, allowing a coupling path into the audio amplifier. A common example is the 217 Hz GSM frame-rate buzz often heard from an active speaker when a cell phone is placed nearby during a phone call.

The TPA6141A2 has excellent rejection of power supply and RF noise, preventing audio signal degradation.

## INPUT COUPLING CAPACITORS

Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize TPA6141A2 turn-on pop to an inaudible level.

The input capacitors are in series with TPA6141A2 internal input resistors, creating a high-pass filter. [Equation 8](#) calculates the high-pass filter corner frequency. The input impedance,  $R_{IN}$ , is dependent on device gain. Larger input capacitors decrease the corner frequency. See the Operating Characteristics table for input impedance values.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \quad (8)$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}} \quad (9)$$

Example: Design for a 20 Hz corner frequency with a TPA6141A2 gain of +6 dB. The Operating Characteristics table gives  $R_{IN}$  as 13.2 kΩ. [Equation 9](#) shows the input coupling capacitors must be at least 0.6 μF to achieve a 20 Hz high-pass corner frequency. Choose a 0.68 μF standard value capacitor for each TPA6141A2 input (X5R material or better is required for best performance).

Input capacitors can be removed provided the TPA6141A2 inputs are driven differentially with less than ±1 V<sub>RMS</sub> and the common-mode voltage is within the input common-mode range of the amplifier. Without input capacitors turn-on pop performance may be degraded and should be evaluated in the system.

## CHARGE PUMP FLYING CAPACITOR AND HPVSS CAPACITOR

The TPA6141A2 uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CPP and CPN. It transfers charge to generate the negative supply voltage. The HPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1 μF to 2.2 μF for the HPVSS and flying capacitors. Although values down to 0.47 μF can be used, total harmonic distortion (THD) will increase.

## OPERATION WITH DACs AND CODECs AND INPUT RF NOISE REJECTION

When using amplifiers with CODECs and DACs, sometimes there is an increase in the output noise floor from the audio amplifier. This occurs when the output out-of-band noise of the CODEC/DAC folds back into the audio frequency due to the limited gain bandwidth product of the audio amplifier. Single-ended RF noise can also fold back into the audio band thus degrading the audio signal even further.

The TPA6141A2 has a built-in low-pass filter to reduce CODEC/DAC out-of-band noise and RF noise, that could fold back into the audio frequency.

## POWER SUPPLY AND HPVDD DECOUPLING CAPACITORS AND CONNECTIONS

The TPA6141A2 DirectPath headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2  $\mu\text{F}$  capacitor within 5 mm of the AVDD pin. Reducing the distance between the decoupling capacitor and AVDD minimizes parasitic inductance and resistance, improving TPA6141A2 supply rejection performance. Use 0402 or smaller size capacitors if possible. Ensure that the ground connection of each of the capacitors has a minimum length return path to the device. Failure to properly decouple the TPA6141A2 may degrade audio or EMC performance.

For additional supply rejection, connect an additional 10  $\mu\text{F}$  or higher value capacitor between AVDD and ground. This will help filter lower frequency power supply noise. The high power supply rejection ratio (PSRR) of the TPA6141A2 makes the 10  $\mu\text{F}$  capacitor unnecessary in most applications.

Connect a 2.2  $\mu\text{F}$  capacitor between HPVDD and ground. This ensures the amplifier internal bias supply remains stable and maximizes headphone amplifier performance.

**DO NOT connect HPVDD directly to AVDD or an external supply voltage. The voltage at HPVDD is generated internally. Connecting HPVDD to an external voltage can damage the device.**

## LAYOUT RECOMMENDATIONS

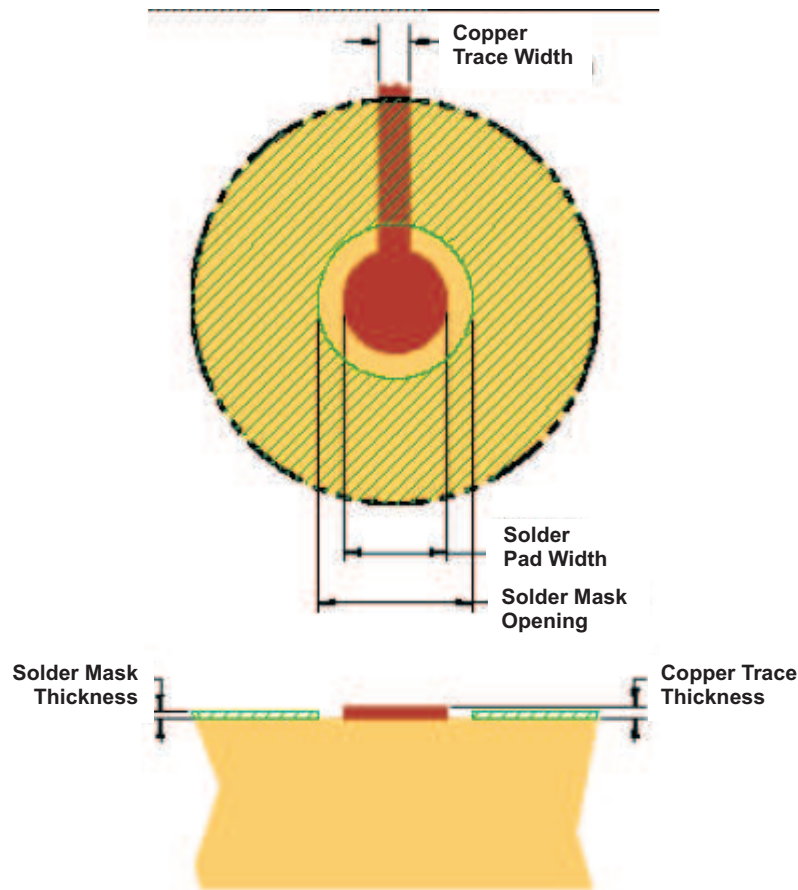
### GND CONNECTIONS

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than  $\pm 0.3$  V to SGND.

AGND is a power ground. Connect supply decoupling capacitors for AVDD, HPVDD, and HPVSS to AGND.

### BOARD LAYOUT

In making the pad size for the WCSP balls, it is recommended that the layout use non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. [Figure 29](#) and [Table 1](#) shows the appropriate diameters for a WCSP layout.



**Figure 29. Land Pattern Dimensions**

**Table 1. Land Pattern Dimensions<sup>(1) (2) (3) (4)</sup>**

| <b>SOLDER PAD DEFINITIONS</b>  | <b>COPPER PAD</b>                            | <b>SOLDER MASK <sup>(5)</sup> OPENING</b>    | <b>COPPER THICKNESS</b>      | <b>STENCIL <sup>(6) (7)</sup> OPENING</b>                          | <b>STENCIL THICKNESS</b> |
|--------------------------------|----------------------------------------------|----------------------------------------------|------------------------------|--------------------------------------------------------------------|--------------------------|
| Non-solder-mask defined (NSMD) | 230 $\mu\text{m}$ (+0.0, -25 $\mu\text{m}$ ) | 310 $\mu\text{m}$ (+0.0, -25 $\mu\text{m}$ ) | 1 oz max (32 $\mu\text{m}$ ) | 275 $\mu\text{m}$ $\times$ 275 $\mu\text{m}$ Sq. (rounded corners) | 100 $\mu\text{m}$ thick  |

- (1) Circuit traces from NSMD defined PWB lands should be 75  $\mu\text{m}$  to 100  $\mu\text{m}$  wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and impact reliability.
- (2) Best reliability results are achieved when the PWB laminate glass transition temperature is above the operating the range of the intended application
- (3) Recommend solder paste is Type 3 or Type 4.
- (4) For a PWB using a Ni/Au surface finish, the gold thickness should be less 0,5 mm to avoid a reduction in thermal fatigue performance.
- (5) Solder mask thickness should be less than 20  $\mu\text{m}$  on top of the copper circuit pattern
- (6) Best solder stencil performance is achieved using laser cut stencils with electro polishing. Use of chemically etched stencils results in inferior solder paste volume control.
- (7) Trace routing away from WCSP device should be balanced in X and Y directions to avoid unintentional component movement due to solder wetting forces.

## TRACE WIDTH

Recommended trace width at the solder balls is 75  $\mu\text{m}$  to 100  $\mu\text{m}$  to prevent solder wicking onto wider PCB traces. For high current pins (VDD, HPVDD, HPVSS, CPP, CPN, OUTL, and OUTR) of the TPA6141A2, use 100  $\mu\text{m}$  trace widths at the solder balls and at least 500  $\mu\text{m}$  PCB traces to ensure proper performance and output power for the device. For the remaining signals of the TPA6141A2, use 75  $\mu\text{m}$  to 100  $\mu\text{m}$  trace widths at the solder balls. The audio input pins (INL–, INL+, INR– and INR+) must run side-by-side to maximize common-mode noise cancellation.

## Package Dimensions

| D                        | E                        |
|--------------------------|--------------------------|
| Max = 1590 $\mu\text{m}$ | Max = 1590 $\mu\text{m}$ |
| Min = 1530 $\mu\text{m}$ | Min = 1530 $\mu\text{m}$ |

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPA6141A2YFFR</a> | Active        | Production           | DSBGA (YFF)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | ASBI                |
| TPA6141A2YFFR.A               | Active        | Production           | DSBGA (YFF)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | ASBI                |
| TPA6141A2YFFR.B               | Active        | Production           | DSBGA (YFF)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | ASBI                |
| <a href="#">TPA6141A2YFFT</a> | Active        | Production           | DSBGA (YFF)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | ASBI                |
| TPA6141A2YFFT.A               | Active        | Production           | DSBGA (YFF)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | ASBI                |
| TPA6141A2YFFT.B               | Active        | Production           | DSBGA (YFF)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | ASBI                |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

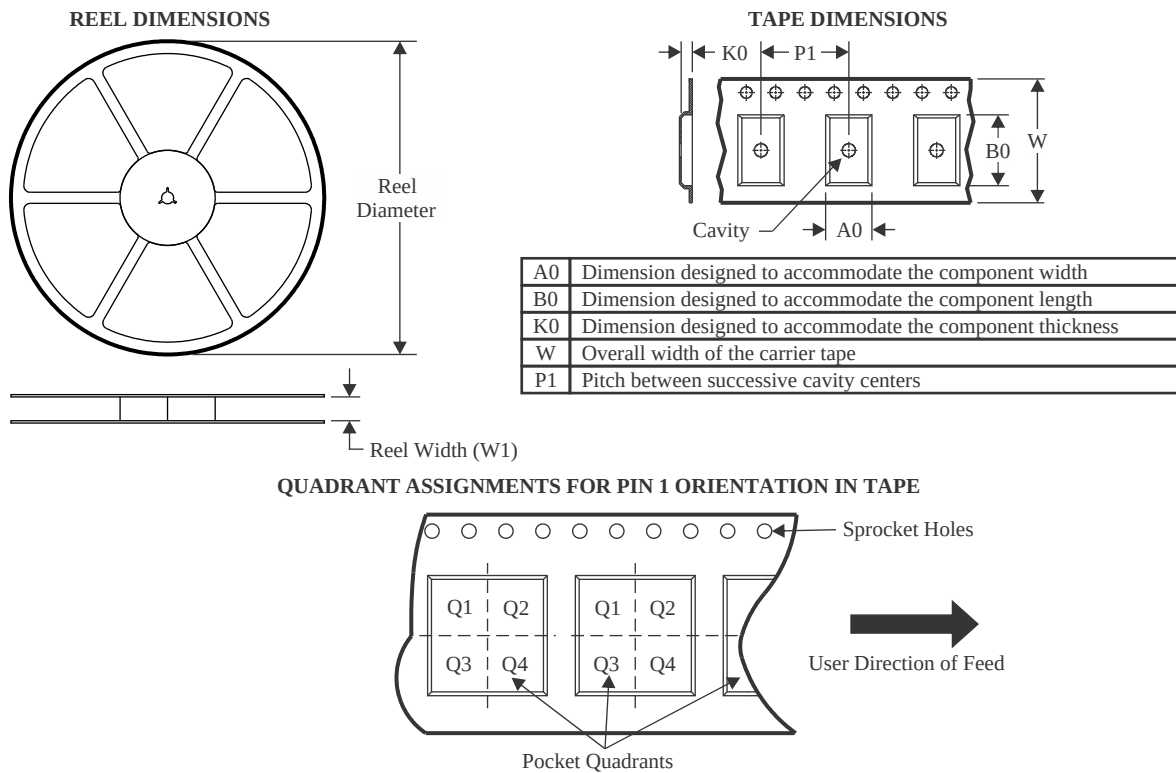
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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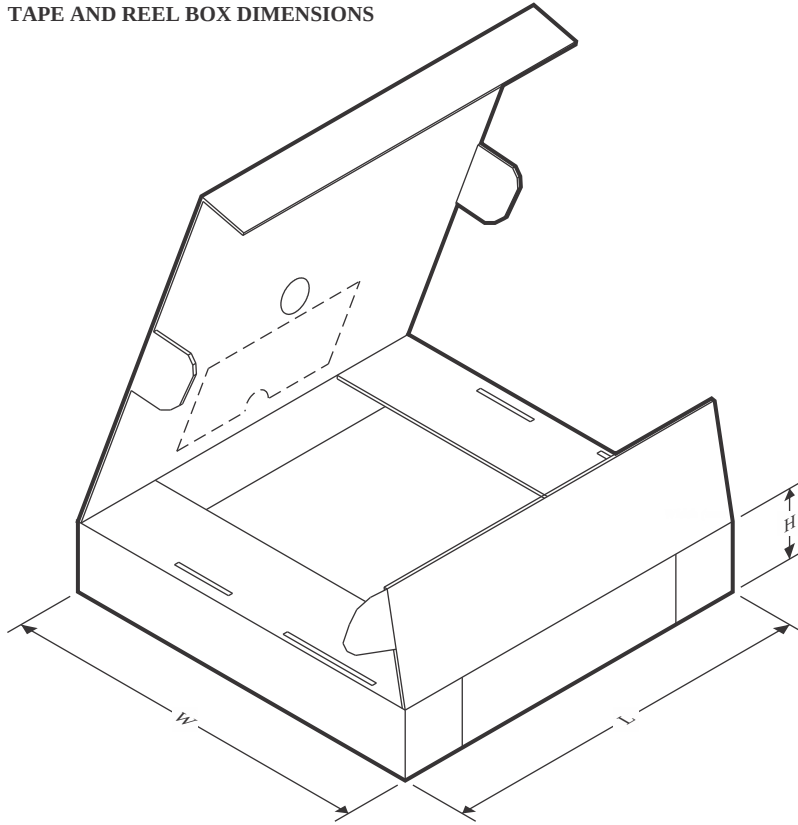
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPA6141A2YFFR | DSBGA        | YFF             | 16   | 3000 | 180.0              | 8.4                | 1.71    | 1.71    | 0.81    | 4.0     | 8.0    | Q1            |
| TPA6141A2YFFT | DSBGA        | YFF             | 16   | 250  | 180.0              | 8.4                | 1.71    | 1.71    | 0.81    | 4.0     | 8.0    | Q1            |

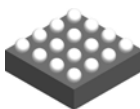
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPA6141A2YFFR | DSBGA        | YFF             | 16   | 3000 | 182.0       | 182.0      | 20.0        |
| TPA6141A2YFFT | DSBGA        | YFF             | 16   | 250  | 182.0       | 182.0      | 20.0        |

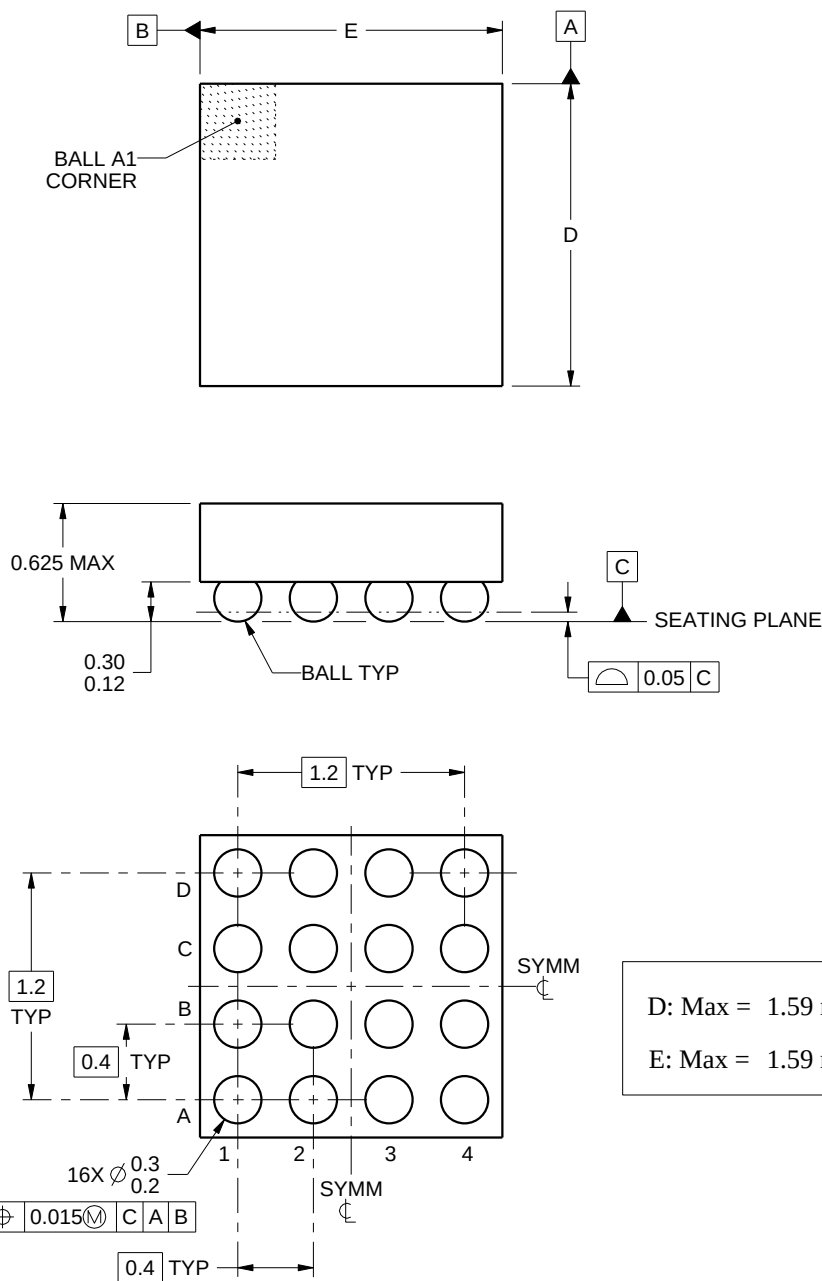
YFF0016



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4219386/A 05/2016

## NOTES:

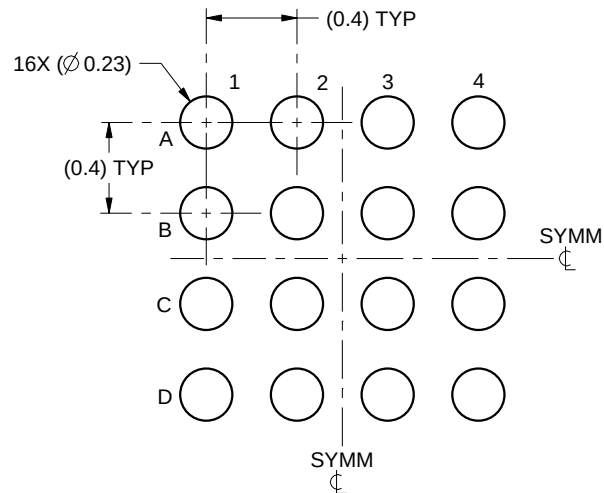
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

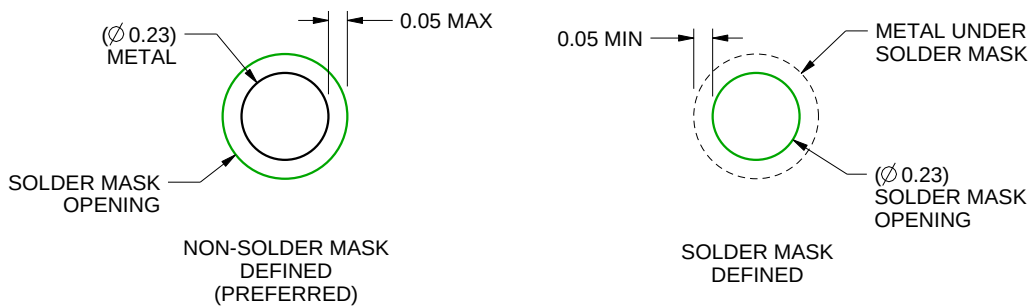
YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

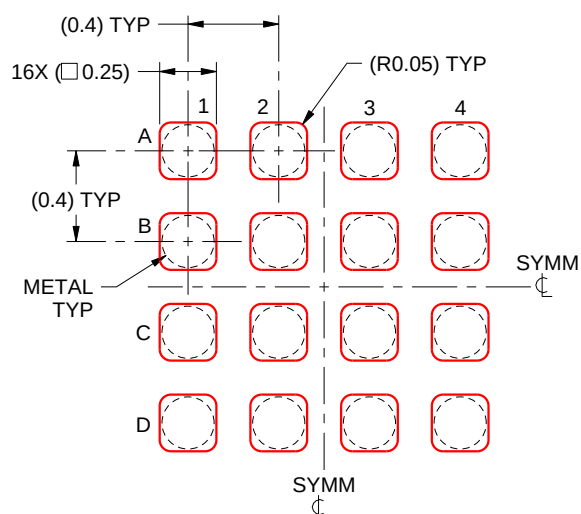
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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