DRV8428E/P Dual H-Bridge Motor Drivers With Integrated Current Sense and Smart Tune Technology

1 Features

- Dual H-bridge motor driver
  - One bipolar stepper motor
  - Dual bidirectional brushed-DC motors
  - Four unidirectional brushed-DC motors
- Integrated current sense functionality
  - No sense resistors required
  - ±6% Full-scale current accuracy
- 4.2-V to 33-V Operating supply voltage range
- Multiple control interface options
  - PHASE/ENABLE (PH/EN)
  - PWM (IN/IN)
- Smart tune, and mixed decay options
- 1500 mΩ HS + LS $R_{DS(ON)}$ at 24 V, 25°C
- Current Capacity: 1.7-A peak, 0.7-A rms
- Configurable Off-Time PWM Chopping
  - 7, 16 or 32 µs
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (2 µA)
- Spread spectrum clocking for low EMI
- Inrush current limiting in brushed-DC applications
- Small package and footprint
- Protection features
  - VM undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)

2 Applications

- Brushed DC Motors
- Printers and scanners
- Currency counters, and EPOS
- Office and home automation
- Factory automation and robotics
- Small home appliances
- Sewing Machines
- Vacuum, humanoid, and toy robotics
- Smart Meters

3 Description

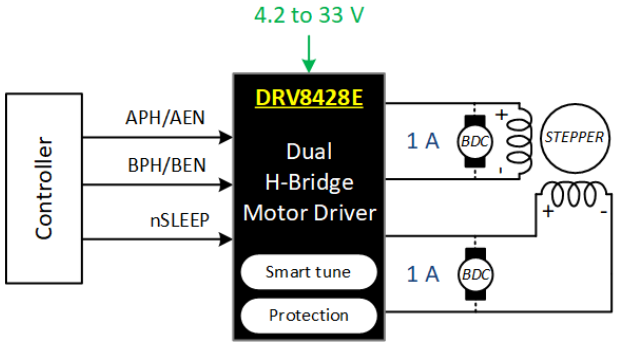
The DRV8428E/P devices are dual H-bridge motor drivers for a wide variety of industrial applications. The devices can be used for driving two DC motors, or a bipolar stepper motor. The DRV8428E/P are capable of driving up to 1-A full scale or 0.7-A rms output current (dependent on PCB design).

The output stage of the driver consists of N-channel power MOSFETs configured as two full H-bridges, current sensing and regulation, and protection circuitry. The integrated current sensing uses an internal current mirror architecture, removing the need for a large power shunt resistor, saving board area and reducing system cost. A low-power sleep mode is provided to achieve ultra- low quiescent current draw by shutting down most of the internal circuitry. Internal protection features are provided for supply undervoltage lockout (UVLO), output overcurrent (OCP), and device overtemperature (TSD).

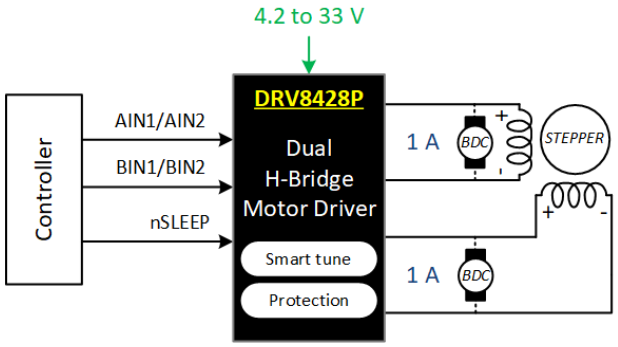
Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8428EPWPR	HTSSOP (16)	5mm x 4.4mm
DRV8428ERTER	WQFN (16)	3.0mm x 3.0mm
DRV8428PPWPR	HTSSOP (16)	5mm x 4.4mm
DRV8428PRTER	WQFN (16)	3.0mm x 3.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DRV8428E Simplified Schematic



DRV8428P Simplified Schematic

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• Changed device status to production data	1

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5 Pin Configuration and Functions

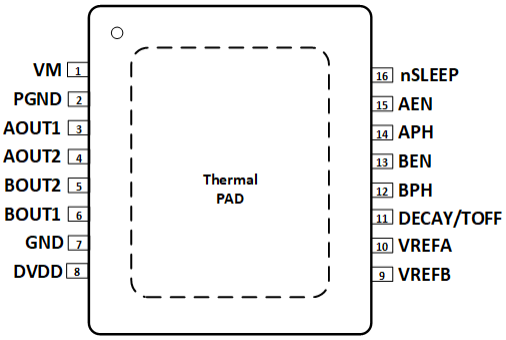

Figure 5-1. PWP PowerPAD™ Package 16-Pin HTSSOP Top View DRV8428E

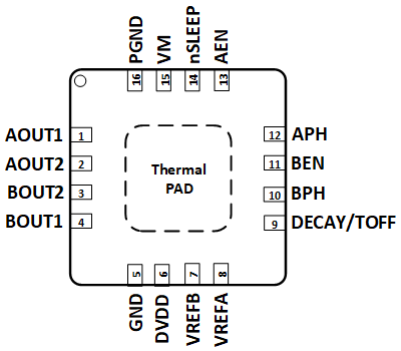

Figure 5-2. RTE Package 16-Pin WQFN with Exposed Thermal PAD Top View DRV8428E

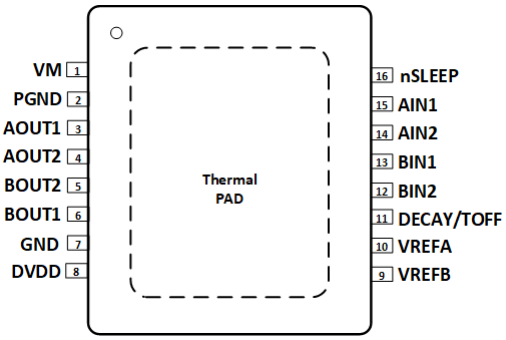

Figure 5-3. PWP PowerPAD™ Package 16-Pin HTSSOP Top View DRV8428P

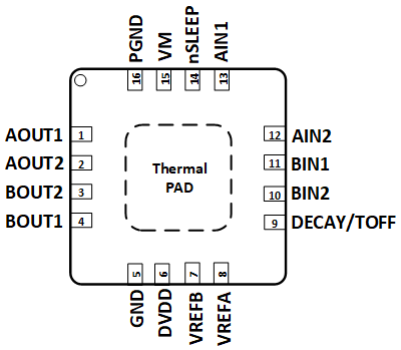

Figure 5-4. RTE Package 16-Pin WQFN with Exposed Thermal PAD Top View DRV8428P

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5.1 Pin Functions

PIN					TYPE	DESCRIPTION
NAME	PWP		RTE			
	DRV8428E	DRV8428P	DRV8428E	DRV8428P		
DECAY/ TOFF	11	11	9	9	I	Decay mode and off-time setting pin; seven-level pin.
AEN	15	—	13	—	I	Bridge A enable input. Logic high enables bridge A; logic low disables the bridge Hi-Z.
AIN1	—	15	—	13	I	Bridge A PWM input. Logic controls the state of H-bridge A; internal pulldown.
AIN2	—	14	—	12	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
AOUT1	3	3	1	1	O	Winding A output. Connect to motor winding.
AOUT2	4	4	2	2	O	Winding A output. Connect to motor winding.
APH	14	—	12	—	I	Bridge A phase input. Logic high drives current from AOUT1 to AOUT2.
VREFA	10	10	8	8	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge A.
BEN	13	—	11	—	I	Bridge B enable input. Logic high enables bridge B; logic low disables the bridge Hi-Z.
BIN1	—	13	—	11	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BIN2	—	12	—	10	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BOUT1	6	6	4	4	O	Winding B output. Connect to motor winding.
BOUT2	5	5	3	3	O	Winding B output. Connect to motor winding.
BPH	12	—	10	—	I	Bridge B phase input. Logic high drives current from BOUT1 to BOUT2.
VREFB	9	9	7	7	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge B.
GND	7	7	5	5	PWR	Device ground. Connect to system ground.
DVDD	8	8	6	6	PWR	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VM	1	1	15	15	PWR	Power supply. Connect to motor supply voltage and bypass to PGND with a 0.01-µF ceramic capacitor plus a bulk capacitor rated for VM.
PGND	2	2	16	16	PWR	Power ground. Connect to system ground.
nSLEEP	16	16	14	14	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor. An nSLEEP low pulse clears faults.
PAD	-	-	-	-	-	Thermal pad. Connect to system ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	35	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, DECAY/TOFF)	–0.3	5.75	V
Reference input pin voltage (VREFA, VREFB)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins	±750	
			Other pins	±500	

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.2	33	V
V_I	Logic level input voltage	0	5.5	V
V_{REF}	Reference rms voltage range (VREFA, VREFB)	0.05	3	V
f_{PWM}	Applied PWM signal (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2)	0	100	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	1	A
I_{rms}	Motor RMS current (xOUTx)	0	0.7	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC[1]		PWP (HTSSOP)	RTE (WQFN)	UNIT
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	47	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.8	46.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	19.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	19.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.3	8.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No motor load		3.8	5.6	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 33 V	4.5	5	5.5	V
		No external load, V_{VM} = 4.2 V	3.9	4.05		V
LOGIC-LEVEL INPUTS (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
t_{PD}	Propagation delay	xPH, xEN, xINx input to current change		750		ns
SEVEN-LEVEL INPUT (DECAY/TOFF)						
V_{I1}	Voltage level 1	Tied to GND	0		0.1	V
V_{I2}	Voltage level 2	14.7kΩ ± 1% to GND	0.2		0.35	V
V_{I3}	Voltage level 3	44.2kΩ ± 1% to GND	0.55		0.8	V
V_{I4}	Voltage level 4	100kΩ ± 1% to GND	1		1.25	V
V_{I5}	Voltage level 5	249kΩ ± 1% to GND	1.5		1.75	V
V_{I6}	Voltage level 6	Hi-Z	2.1		2.4	V
V_{I7}	Voltage level 7	Tied to DVDD	3		5.5	V
I_O	Output pull-up current			22.5		µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -0.5 A		750	875	mΩ
		T_J = 125 °C, I_O = -0.5 A		1130	1350	mΩ
		T_J = 150 °C, I_O = -0.5 A		1250	1450	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 0.5 A		750	875	mΩ
		T_J = 125 °C, I_O = 0.5 A		1130	1350	mΩ
		T_J = 150 °C, I_O = 0.5 A		1250	1450	mΩ
t_{SR}	Output slew rate	VM = 24V, I_O = 0.5 A, Between 10% and 90%		240		V/µs
PWM CURRENT CONTROL (VREFA, VREFB)						
K_V	Transimpedance gain	VREF = 3 V	2.805	3	3.195	V/A
t_{OFF}	PWM off-time, mixed 30% decay	DECAY/TOFF = 14.7kΩ to GND		7		µs
		DECAY/TOFF = 44.2kΩ to GND		16		
		DECAY/TOFF = 100kΩ to GND		32		
	PWM off-time, smart tune dynamic decay	DECAY/TOFF = 249kΩ to GND		7		
		DECAY/TOFF = Hi-Z		16		
		DECAY/TOFF = DVDD		32		

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{TRIP}	Current trip accuracy	I_O = 1 A, 10% to 20% current setting	–15		15	%
		I_O = 1 A, 20% to 67% current setting	–10		10	
		I_O = 1 A, 68% to 100% current setting	-6		6	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 1 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	3.8	3.95	4.05	V
		VM rising, UVLO rising	3.9	4.05	4.15	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
I_{OCP}	Overcurrent protection	Current through any FET	1.7			A
t_{OCP}	Overcurrent deglitch time			1.8		µs
t_{RETRY}	Overcurrent retry time			4		ms
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.5.1 Typical Characteristics

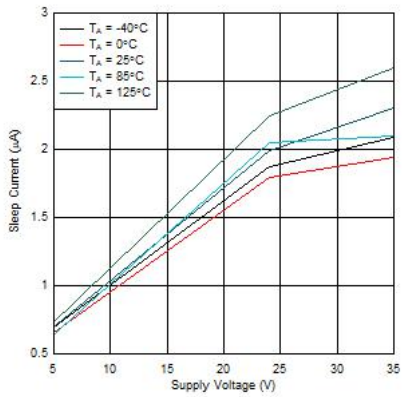

Figure 6-1. Sleep Current over Supply Voltage

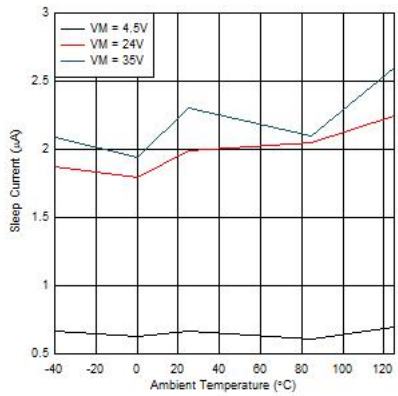

Figure 6-2. Sleep Current over Temperature

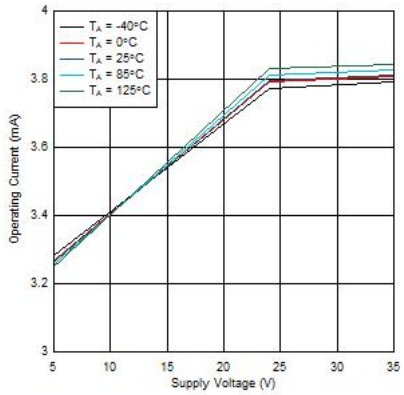

Figure 6-3. Operating Current over Supply Voltage

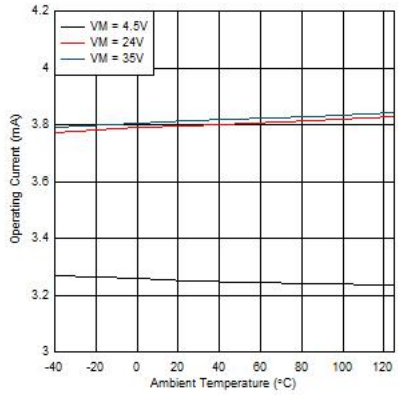

Figure 6-4. Operating Current over Temperature

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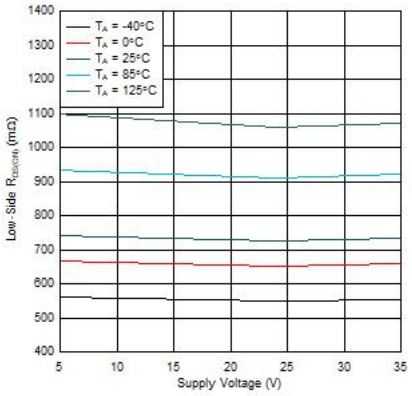

Figure 6-5. Low-Side $R_{DS(ON)}$ over Supply Voltage

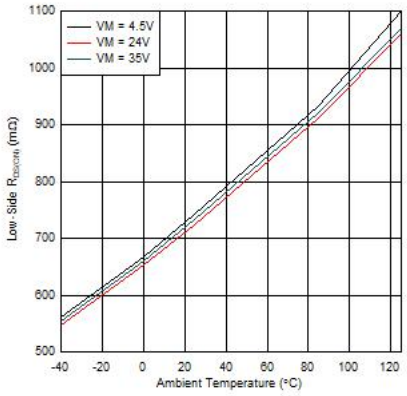

Figure 6-6. Low-Side $R_{DS(ON)}$ over Temperature

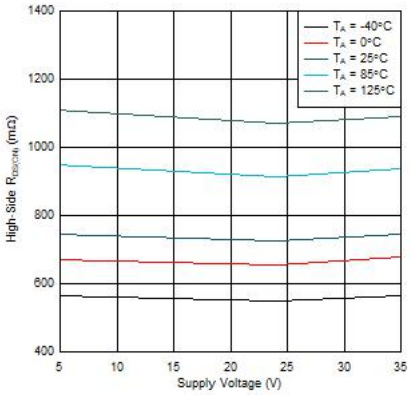

Figure 6-7. High-Side $R_{DS(ON)}$ over Supply Voltage

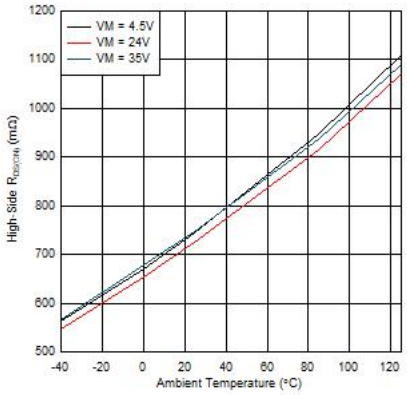

Figure 6-8. High-Side $R_{DS(ON)}$ over Temperature

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7 Detailed Description

7.1 Overview

The DRV8428E/P are integrated motor driver solutions for bipolar stepper motors or dual brushed-DC motors. The devices integrate two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry. The DRV8428E/P can be powered with a supply voltage between 4.2 V and 33 V. The DRV8428E/P are capable of providing an output current up to 1.7-A peak, 1-A full-scale, or 0.7-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8428E/P devices use an integrated current-sense architecture which eliminates the need for two external power sense resistors, hence saving significant board space, BOM cost, design efforts and reduces significant power consumption. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREFA and VREFB pins.

A simple PH/**E**N (DRV8428**E**) or **P**WM (DRV8428**P**) interface allows easy interfacing to the controller circuit.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a smart tune Dynamic Decay, smart tune Ripple Control, or mixed decay. The smart tune decay modes automatically adjust the decay setting to minimize current ripple while still reacting quickly to step changes. This feature greatly simplifies stepper driver integration into a motor drive system. The PWM off-time, t_{OFF}, can be adjusted to 7, 16, or 32 µs.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

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7.2 Functional Block Diagrams

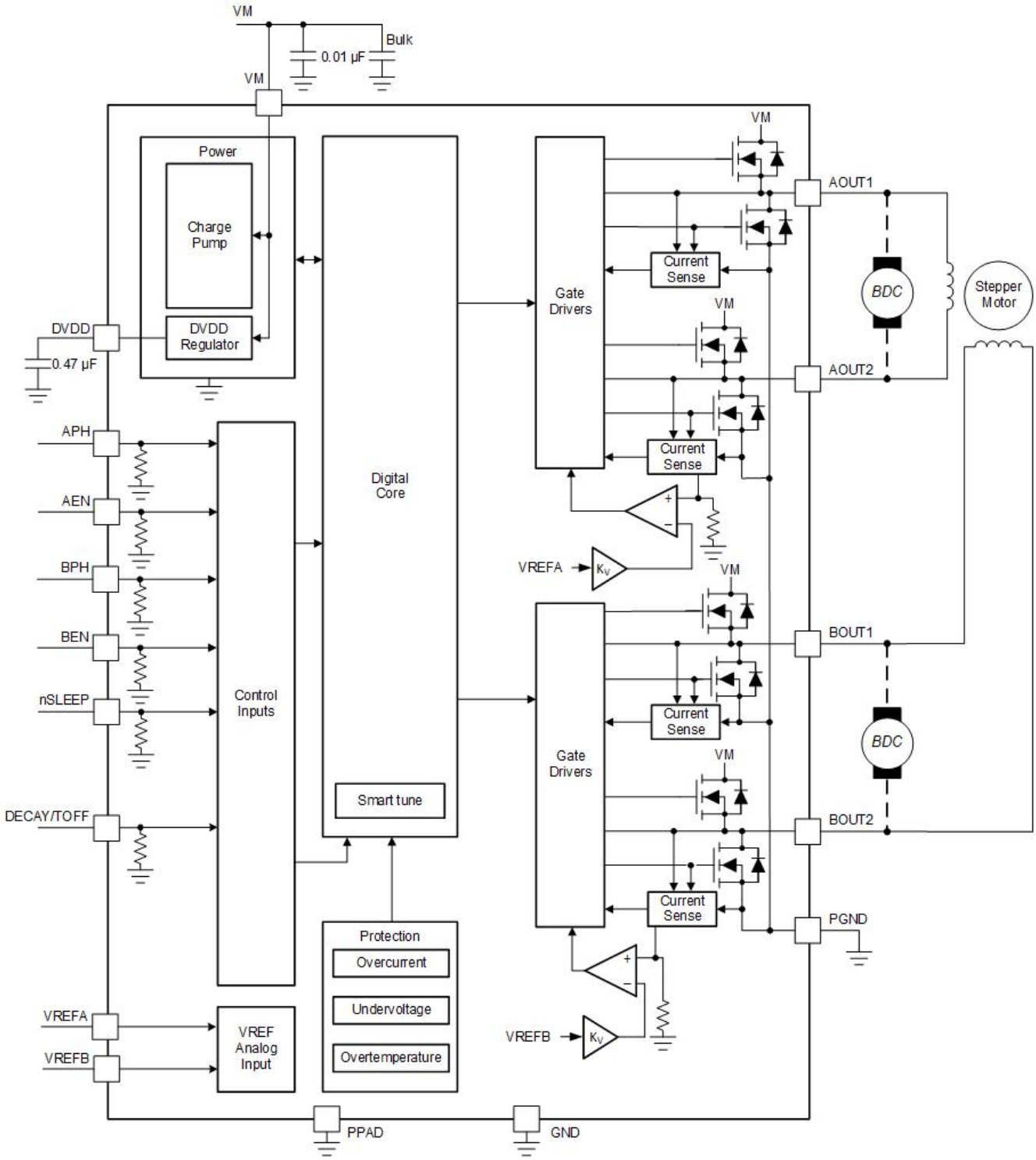

Figure 7-1. DRV8428E Block Diagram

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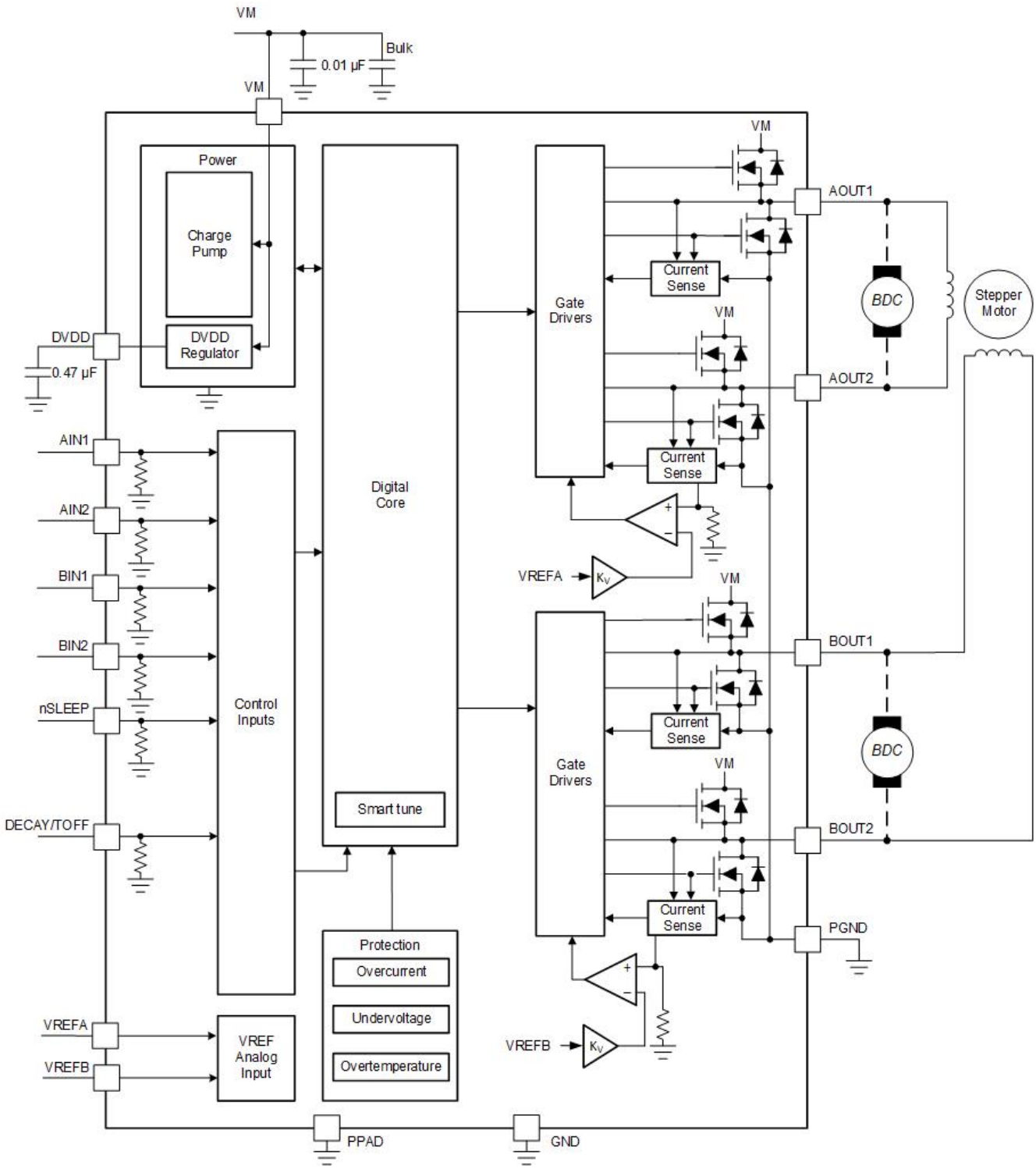

Figure 7-2. DRV8428P Block Diagram

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7.3 Feature Description

Table 7-1 shows the recommended values of the external components for the driver.

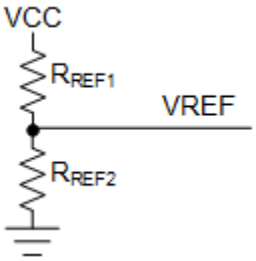

Figure 7-3. Resistor divider connected to the VREF pins

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X7R, 0.01-µF, VM-rated ceramic capacitor
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{REF1}	VREFx	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREFx	GND	

VCC is not a pin on the DRV8428E/P device. VCC can either be an external supply voltage or DVDD.

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7.3.1 PWM Motor Drivers

The DRV8428E and DRV8428P contain drivers for two full H-bridges. Figure 7-4 shows a block diagram of the circuitry.

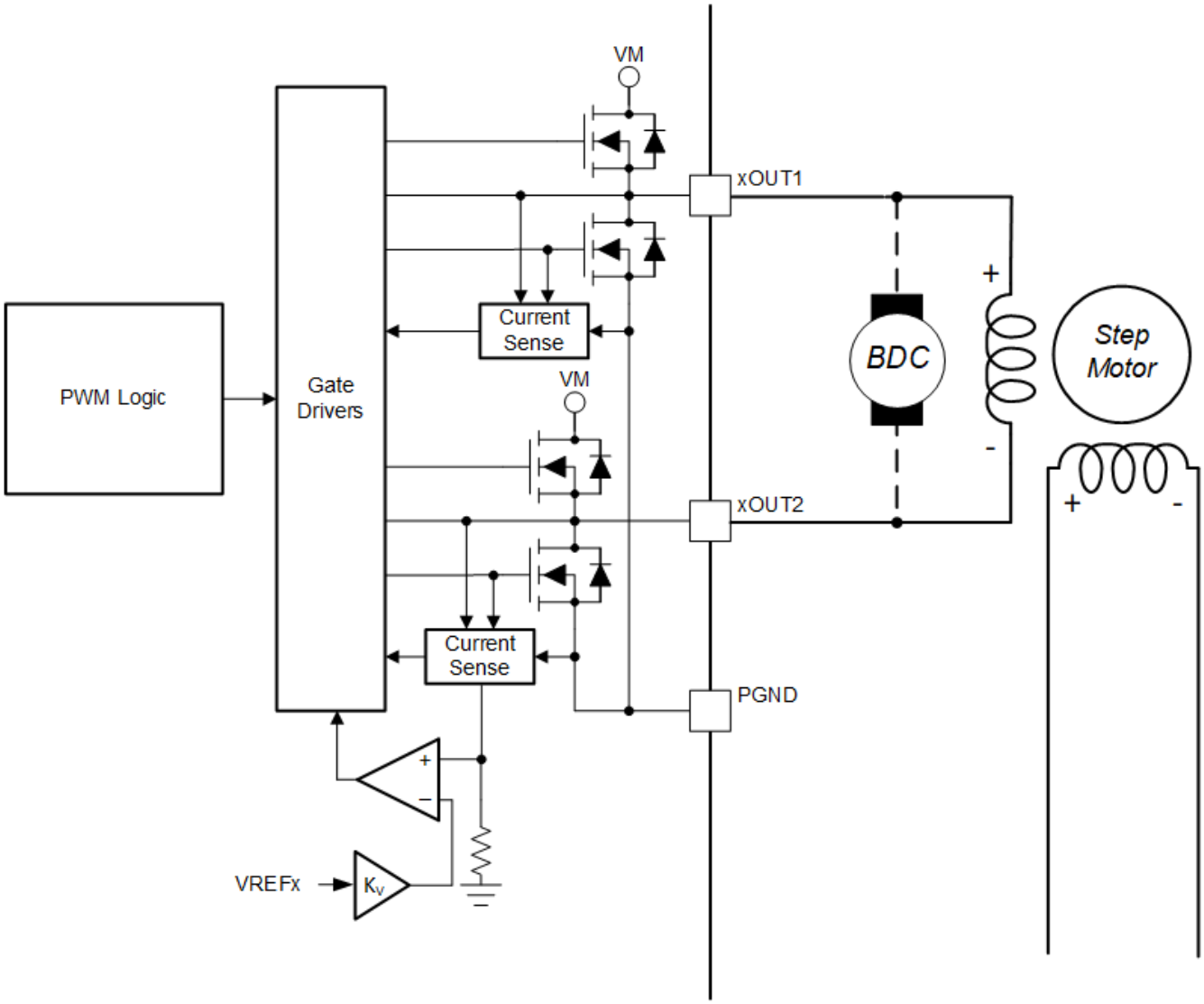

Figure 7-4. PWM Motor Driver Block Diagram

7.3.2 Bridge Control

The DRV8428E is controlled using a PH/EN interface. Table 7-2 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8428E. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 7-2. DRV8428E (PH/EN) Control Interface

nSLEEP	xEN	xPH	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	X	Hi-Z	Hi-Z	H-bridge disabled Hi-Z
1	1	0	L	H	Reverse (current xOUT2 to xOUT1)
1	1	1	H	L	Forward (current xOUT1 to xOUT2)

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The DRV8428P is controlled using a PWM interface. Table 7-3 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8428P. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 7-3. DRV8428P (PWM) Control Interface

nSLEEP	xIN1	xIN2	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	0	L	L	Brake; low-side slow decay
1	0	1	L	H	Reverse (current xOUT2 to xOUT1)
1	1	0	H	L	Forward (current xOUT1 to xOUT2)
1	1	1	H	H	Brake; high-side slow decay

7.3.3 Current Regulation, Off-time and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-5, Item 1.

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the seven-level DECAY/TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 7-5, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7-5, Item 3.

The PWM chopping current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. To generate the reference voltage for the current chopping comparator, the VREFx input is attenuated by a factor of Kv.

The chopping current (I_{FS}) can be calculated as I_{FS} (A) = V_{REFx} (V) / K_V (V/A) = V_{REFx} (V) / 3 (V/A).

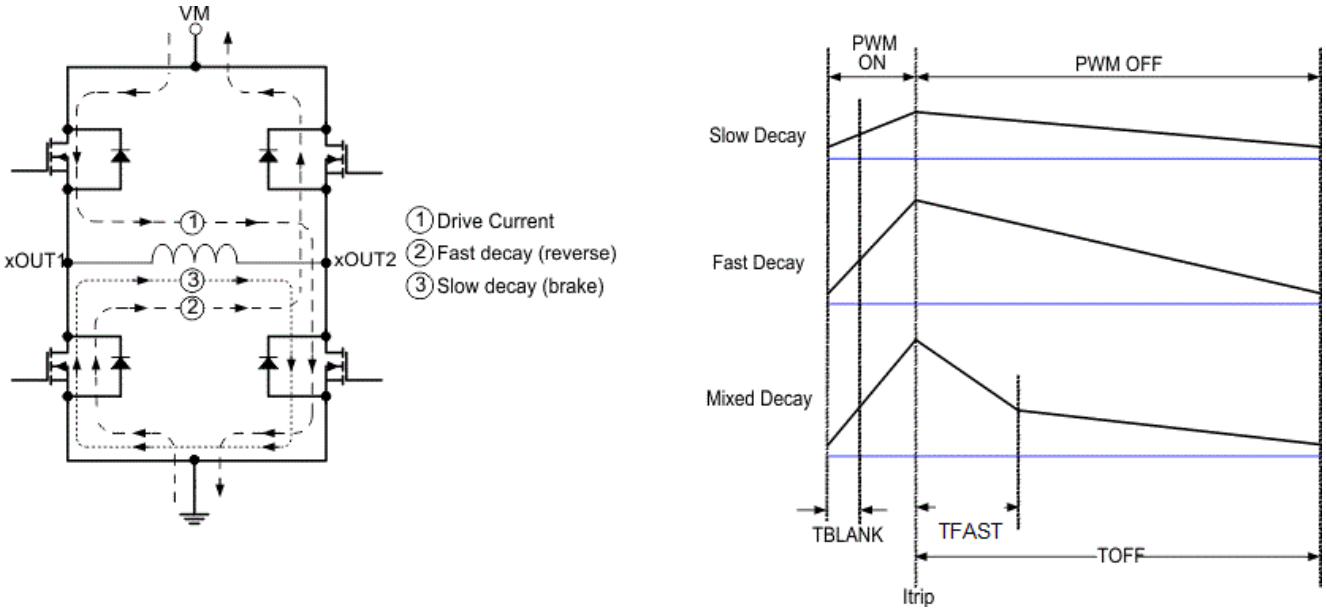

Figure 7-5. Decay Modes

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The decay mode and off time for each bridge is selected by setting the seven-level DECAY/TOFF pin as shown in Table 7-4.

Table 7-4. Decay Mode Settings

DECAY/TOFF	DECAY MODE	OFF TIME
0	Smart tune Ripple Control	-
14.7kΩ to GND	Mixed 30% Decay	7µs
44.2kΩ to GND		16µs
100kΩ to GND		32µs
249kΩ to GND	Smart tune Dynamic Decay	7µs
Hi-Z		16µs
DVDD		32µs

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7.3.3.1 Mixed Decay

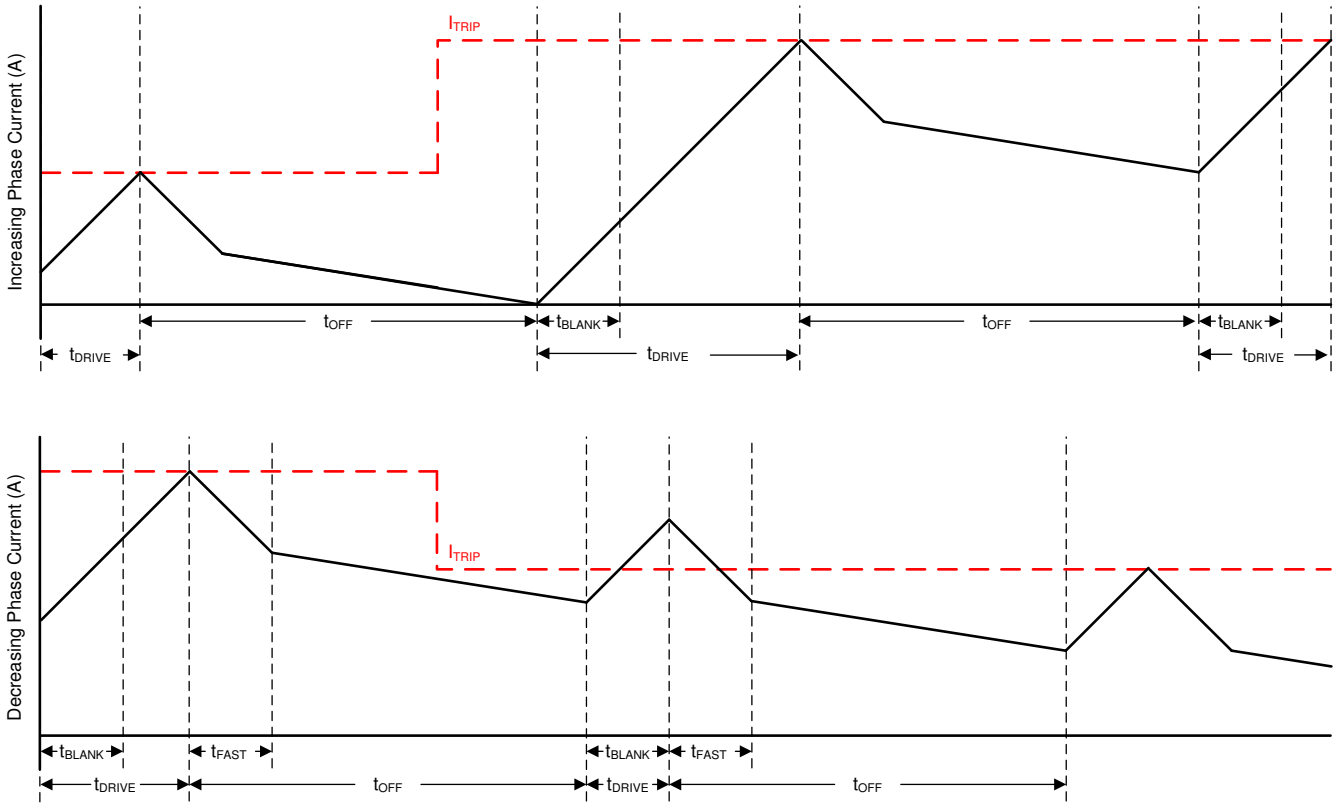

Figure 7-6. Mixed Decay Mode

Mixed decay begins as fast decay for 30% of t_{OFF}, followed by slow decay for the remainder of t_{OFF}.

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7.3.3.2 Smart tune Dynamic Decay

The smart tune current regulation scheme is an advanced current-regulation control method compared to traditional fixed off-time current regulation schemes. Smart tune current regulation scheme helps the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Low-current versus high-current dI/dt

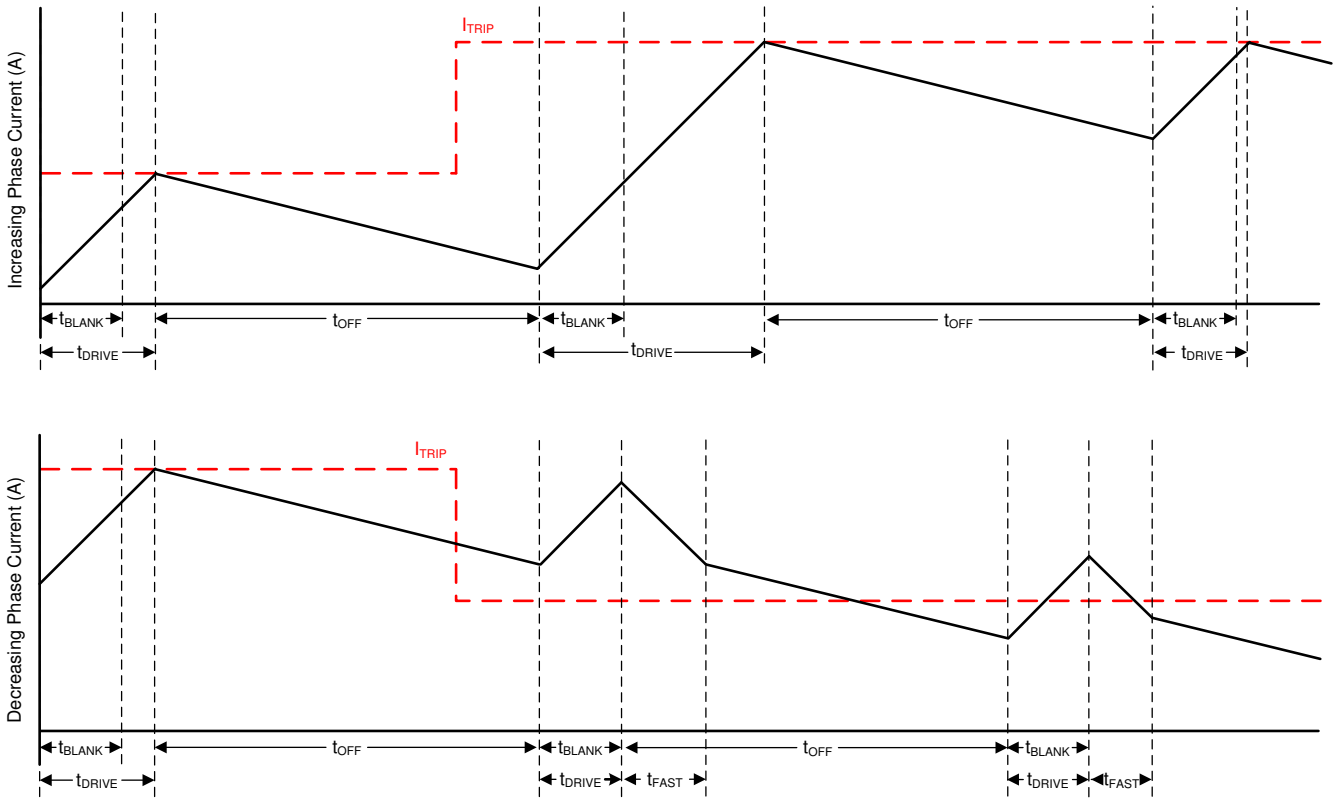

Figure 7-7. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

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7.3.3.3 Smart tune Ripple Control

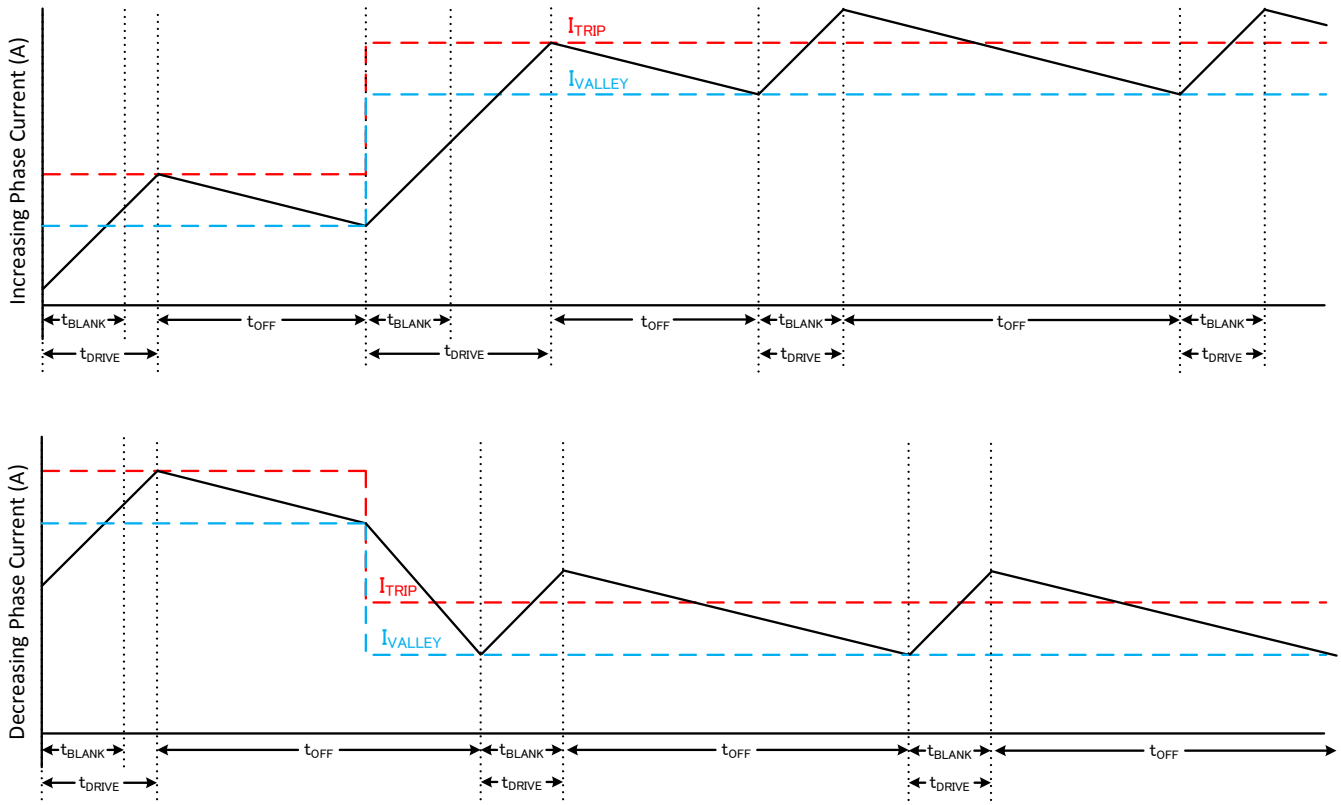

Figure 7-8. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

The ripple current in this decay mode is 7.5mA + 1% of the ITRIP at a specific microstep level.

7.3.3.4 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

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7.3.4 Linear Voltage Regulators

A linear voltage regulator is integrated in the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

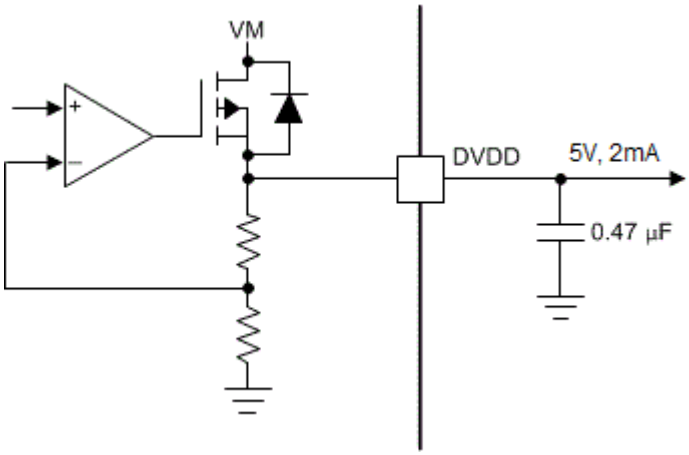

Figure 7-9. Linear Voltage Regulator Block Diagram

If DECAY/TOFF pin must be tied permanently high, tying it to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

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7.3.5 Logic and Seven-Level Pin Diagrams

Figure 7-10 gives the input structure for logic-level pins APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2 and nSLEEP:

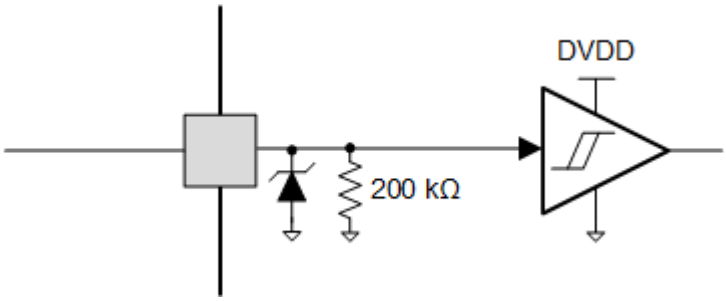

Figure 7-10. Logic-level Input Pin Diagram

Seven-level logic pin DECAY/TOFF has the following structure as shown in Figure 7-11.

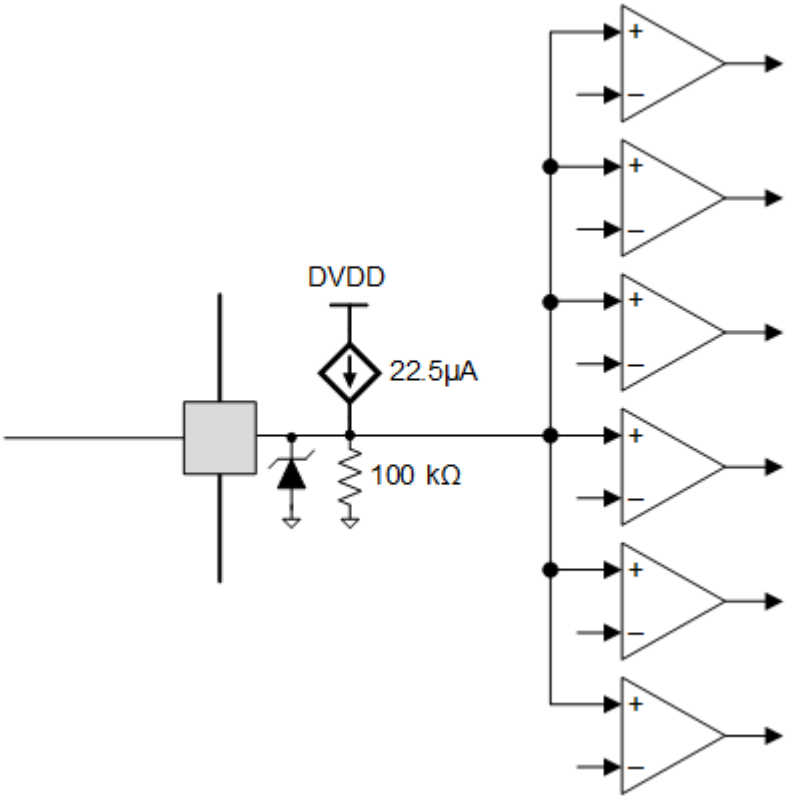

Figure 7-11. Seven-Level Input Pin Diagram

7.3.6 Protection Circuits

The devices are fully protected against supply undervoltage, output overcurrent, and device overtemperature events.

7.3.6.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled. Normal operation resumes when the VM undervoltage condition is removed.

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7.3.6.2 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in both H-bridges are disabled. Normal operation resumes automatically after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.6.3 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}), all MOSFETs in the H-bridge are disabled. Normal operation resumes when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS_OTSD}$).

7.3.6.4 Fault Condition Summary

Table 7-5. Fault Condition Summary

FAULT	CONDITION	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	Disabled	Reset (V_{DVDD} < 3.6 V)	Automatic: VM > V_{UVLO}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	Disabled	Operating	Automatic retry: t_{RETRY}
Thermal Shutdown (OTSD)	T_J > T_{TSD}	Disabled	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The state of the device is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.3 Functional Modes Summary

Table 7-6 lists a summary of the functional modes.

Table 7-6. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	Logic
Sleep mode	4.2 V < VM < 33 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled
Operating	4.2 V < VM < 33 V	nSLEEP pin = 1	Operating	Operating	Operating

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8428E/P is used in brushed or stepper motor control.

8.2 Typical Application

In this application, the device is configured to drive bidirectional currents through two external loads (such as two brushed DC motors) using H-bridge configuration. The H-bridge polarity and duty cycle are controlled from the external controller to the xEN/xIN1 and xPH/xIN2 pins.

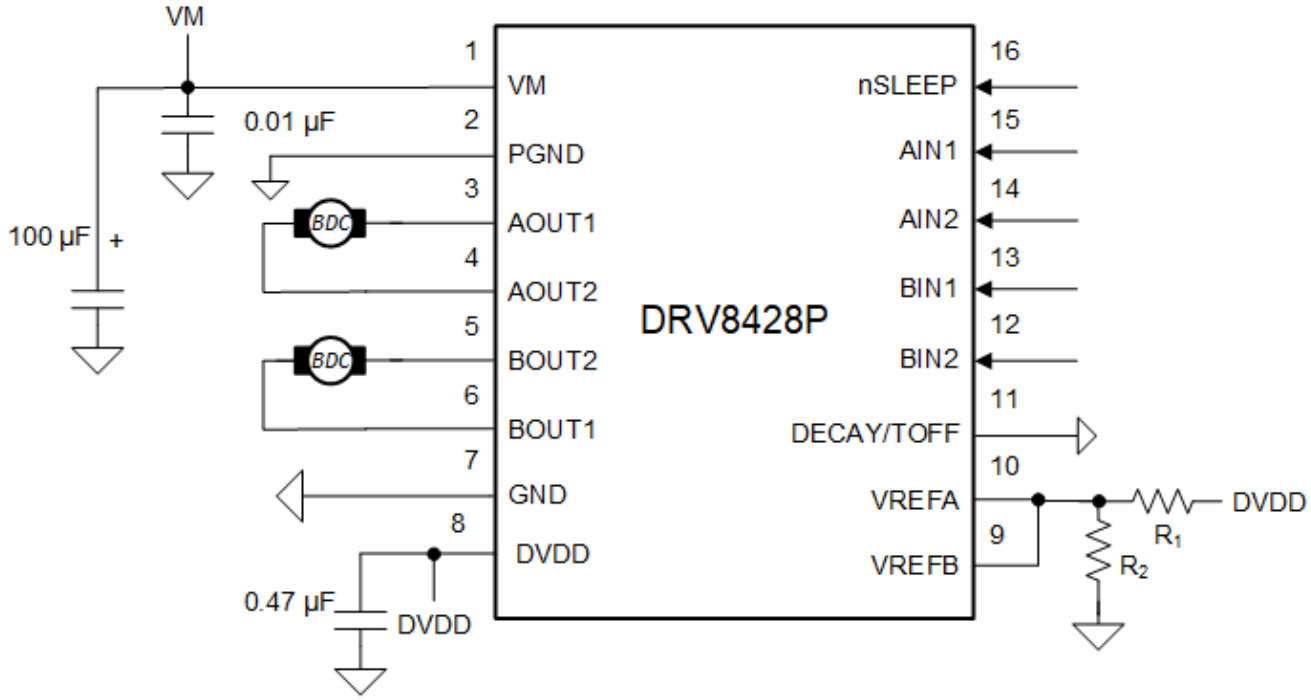

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	6 Ω
Motor winding inductance	L_L	4.1 mH
Switching Frequency	f_{PWM}	40 kHz
Regulated Current for Each Motor	I_{REG}	500 mA

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8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

The regulated current (I_{REG}) is set by the VREFx analog voltage. When starting a brushed-DC motor, a large inrush current may occur because there is no back-EMF. Current regulation will act to limit this inrush current and prevent high current on startup. The regulated current (I_{REG}) can be calculated as I_{REG} (A) = V_{REFx} (V) / K_V (V/A) = V_{REFx} (V) / 3 (V/A).

8.2.2.2 Power Dissipation and Thermal Calculation

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation (P_{TOT}) for the device is composed of three main components. These are the power MOSFET $R_{DS(ON)}$ (conduction) losses, the power MOSFET switching losses and the quiescent supply current dissipation. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$P_{TOT} = P_{COND} + P_{SW} + P_Q$

P_{COND} for each brushed-DC motor can be calculated from the device $R_{DS(ON)}$ and regulated output current (I_{REG}). Assuming same I_{REG} for both brushed-DC motors,

$P_{COND} = 2 \times (I_{REG})^2 \times (R_{DS(ONH)} + R_{DS(ONL)})$

It should be noted that $R_{DS(ON)}$ has a strong correlation with the device temperature. A curve showing the normalized $R_{DS(ON)}$ with temperature can be found in the Typical Characteristics curves.

$P_{COND} = 2 \times (0.5\text{-A})^2 \times (0.75\text{-}\Omega + 0.75\text{-}\Omega) = 0.75\text{-W}$

P_{SW} can be calculated from the nominal supply voltage (VM), regulated output current (I_{REG}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

$P_{SW} = 2 \times (P_{SW_RISE} + P_{SW_FALL})$

$P_{SW_RISE} = 0.5 \times VM \times I_{REG} \times t_{RISE} \times f_{PWM}$

$P_{SW_FALL} = 0.5 \times VM \times I_{REG} \times t_{FALL} \times f_{PWM}$

$P_{SW_RISE} = 0.5 \times 24\text{ V} \times 0.5\text{ A} \times 100\text{ ns} \times 40\text{ kHz} = 0.024\text{ W}$

$P_{SW_FALL} = 0.5 \times 24\text{ V} \times 1.5\text{ A} \times 100\text{ ns} \times 40\text{ kHz} = 0.024\text{ W}$

$P_{SW} = 2 \times (0.024\text{W} + 0.024\text{W}) = 0.096\text{ W}$

P_Q can be calculated from the nominal supply voltage (VM) and the I_{VM} current specification.

$P_Q = VM \times I_{VM} = 24\text{ V} \times 3.8\text{ mA} = 0.0912\text{ W}$

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss.

$P_{TOT} = P_{COND} + P_{SW} + P_Q = 0.75\text{-W} + 0.096\text{-W} + 0.0912\text{-W} = 0.9372\text{-W}$

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 46.4 °C/W for the HTSSOP package, 47 °C/W for the WQFN package and 90.6 °C/W for the TSOT package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as shown below -

$$T_J = 25°C + (0.9372\text{-W} \times 46.4°C/W) = 68.49\ °C \quad (1)$$

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The junction temperature for the WQFN package is calculated as shown below -

$$T_J = 25°C + (0.9372\text{-}W \times 47°C/W) = 69.05\ °C \quad (2)$$

Therefore, the HTSSOP and the WQFN packages result in almost identical junction temperature. It should be ensured that the device junction temperature is within the specified operating region.

8.2.2.2.1 Application Curves

CH1 = IN1 (3V/div), CH7 = I_{REG} (0.5A/div), CH3 = AOUT1 (24V/div), CH2 = AOUT2 (24V/div)

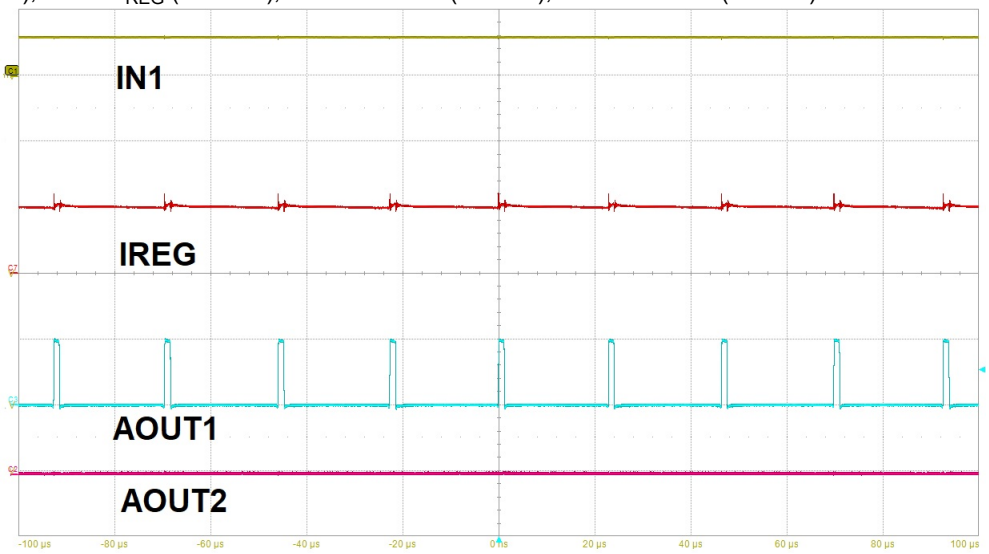

Figure 8-2. Driver Full On Operation with Current Regulation

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8.3 Alternate Application

The following design procedure can be used to configure the DRV8428E/P to drive a stepper motor.

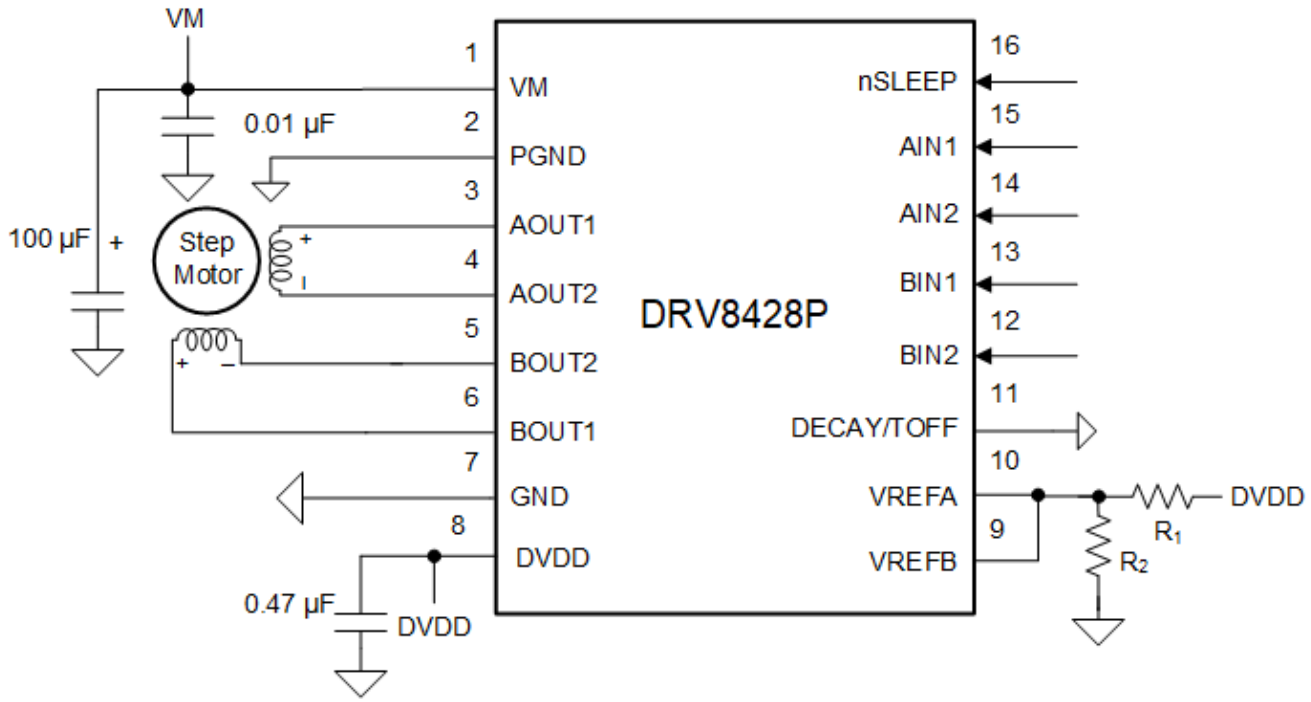

Figure 8-3. Typical Application Schematic

8.3.1 Design Requirements

Table 8-2 gives design input parameters for system design.

Table 8-2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	6 Ω/phase
Motor winding inductance	L_L	4.1 mH/phase
Motor Full Step Angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/2 step
Target motor speed	v	90 rpm
Target full-scale current	I_{FS}	500 mA

8.3.2 Detailed Design Procedure

8.3.2.1 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREFx voltage. The maximum allowable voltage on the VREFx pins is 3 V. DVDD can be used to provide VREFx through a resistor divider.

I_{FS} (A) = V_{REF} (V) / 3 (V/A)

Note

The I_{FS} current must also follow Equation 3 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

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$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{3}$$

8.3.2.1.1 Stepper Motor Speed

Next, the driving waveform needs to be planned. In order to command the correct speed, determine the frequency of the input waveform.If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\ (steps / s) = \frac{v\ (rpm) \times 360\ (° / rot)}{\theta_{step}\ (° / step) \times n_m\ (steps / microstep) \times 60\ (s / min)}$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.The frequency f_{step} gives the frequency of input change on the device. For the design parameters mentioned in Design Parameters, f_{step} can be calculated as 600 Hz.

8.3.2.1.1.1 Decay Modes

The device supports mixed decay, and smart tune. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the device will place the winding in one of the decay modes for TOFF. After TOFF, a new drive phase starts.

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.2 V to 33 V. A 0.01-µF ceramic capacitor rated for VM must be placed at VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

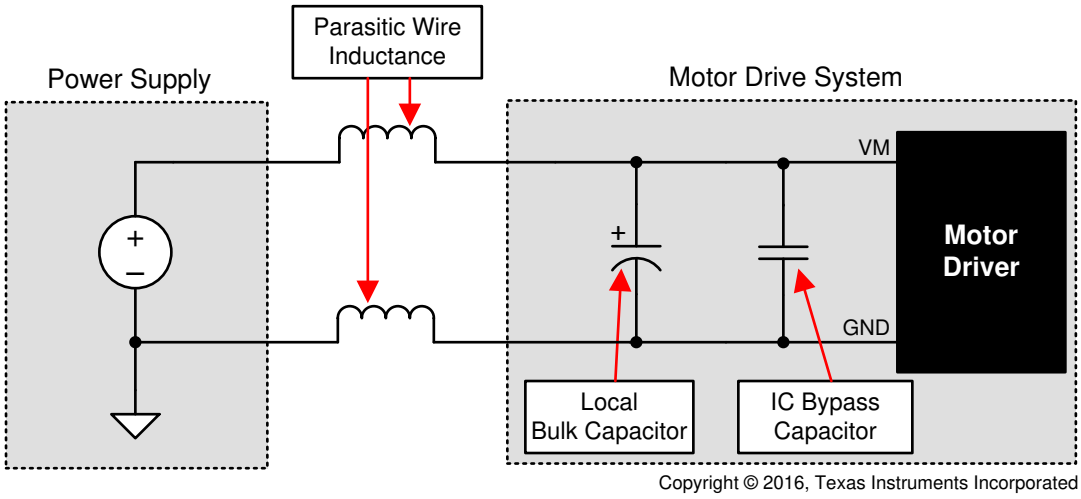

Figure 9-1. Example Setup of Motor Drive System With External Power Supply

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10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

10.1.1 Layout Example

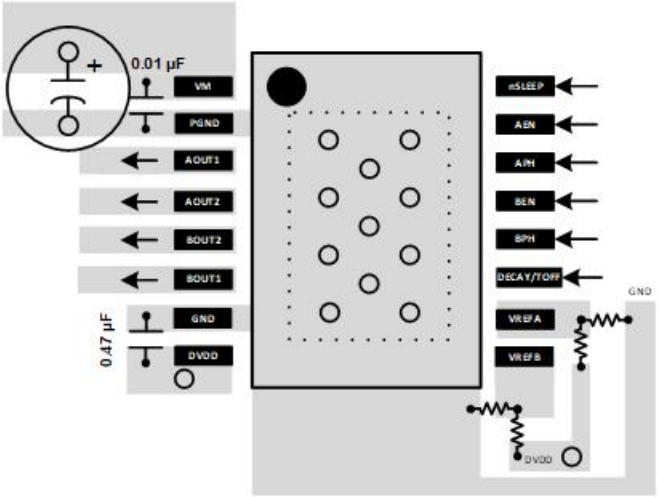

Figure 10-1. HTSSOP Layout Example

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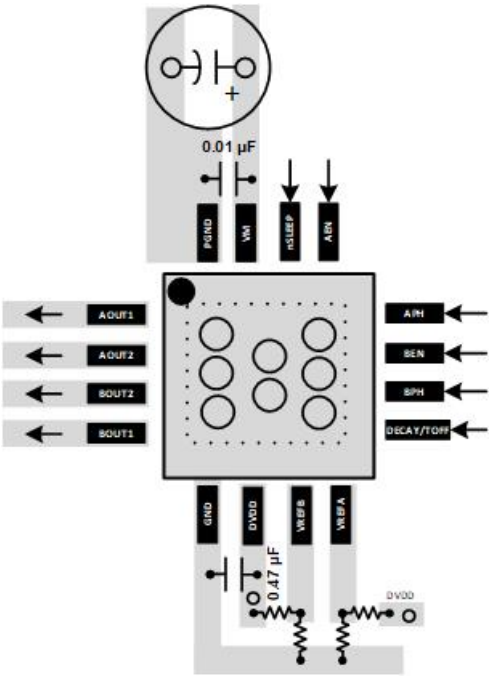

Figure 10-2. QFN Layout Example

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8428E	Click here	Click here	Click here	Click here	Click here
DRV8428P	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

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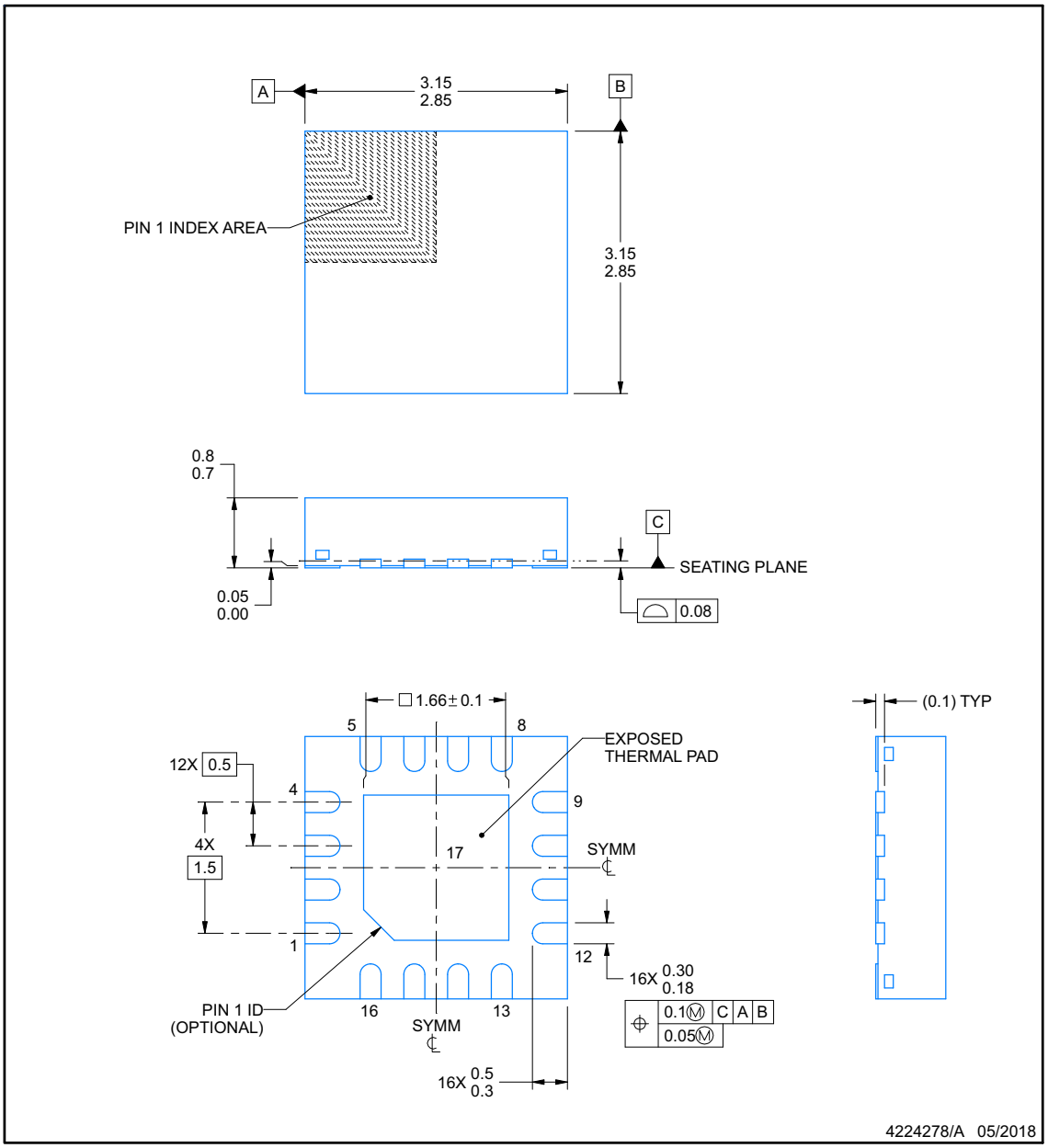
PACKAGE OUTLINE

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

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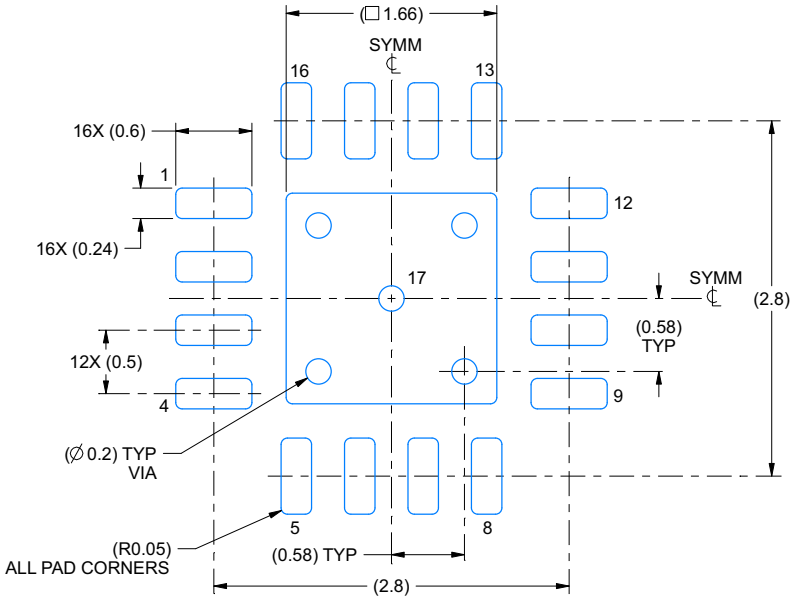
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

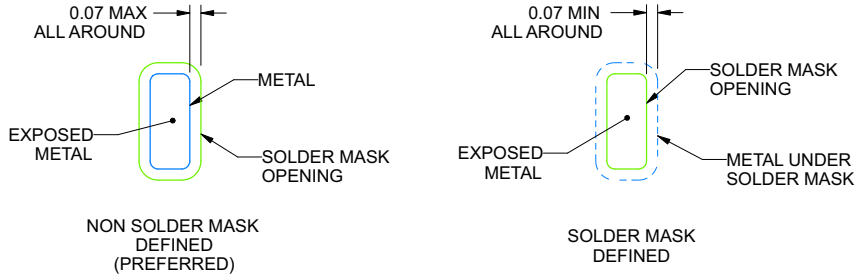
RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224278/A 05/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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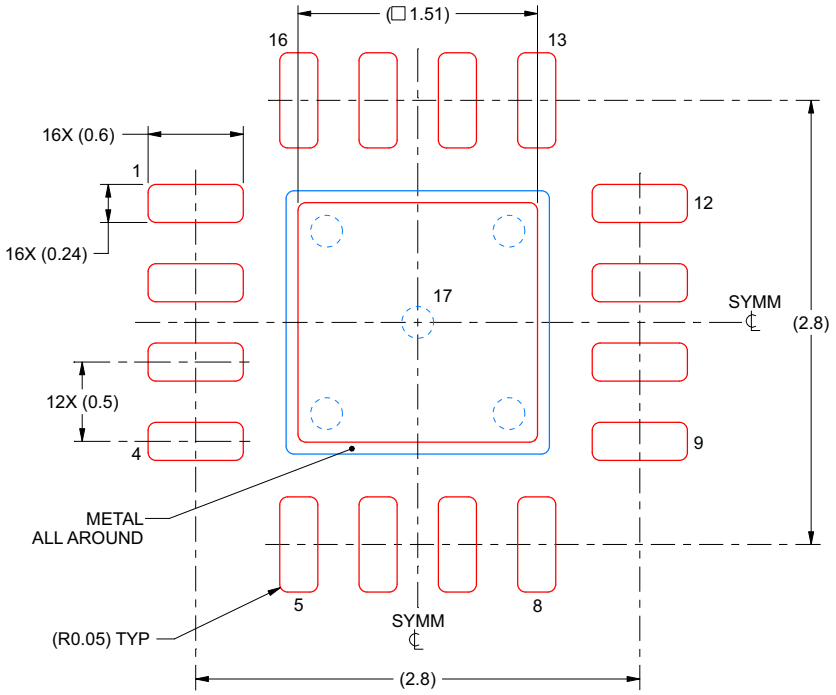
EXAMPLE STENCIL DESIGN

RTE0016J **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224278/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

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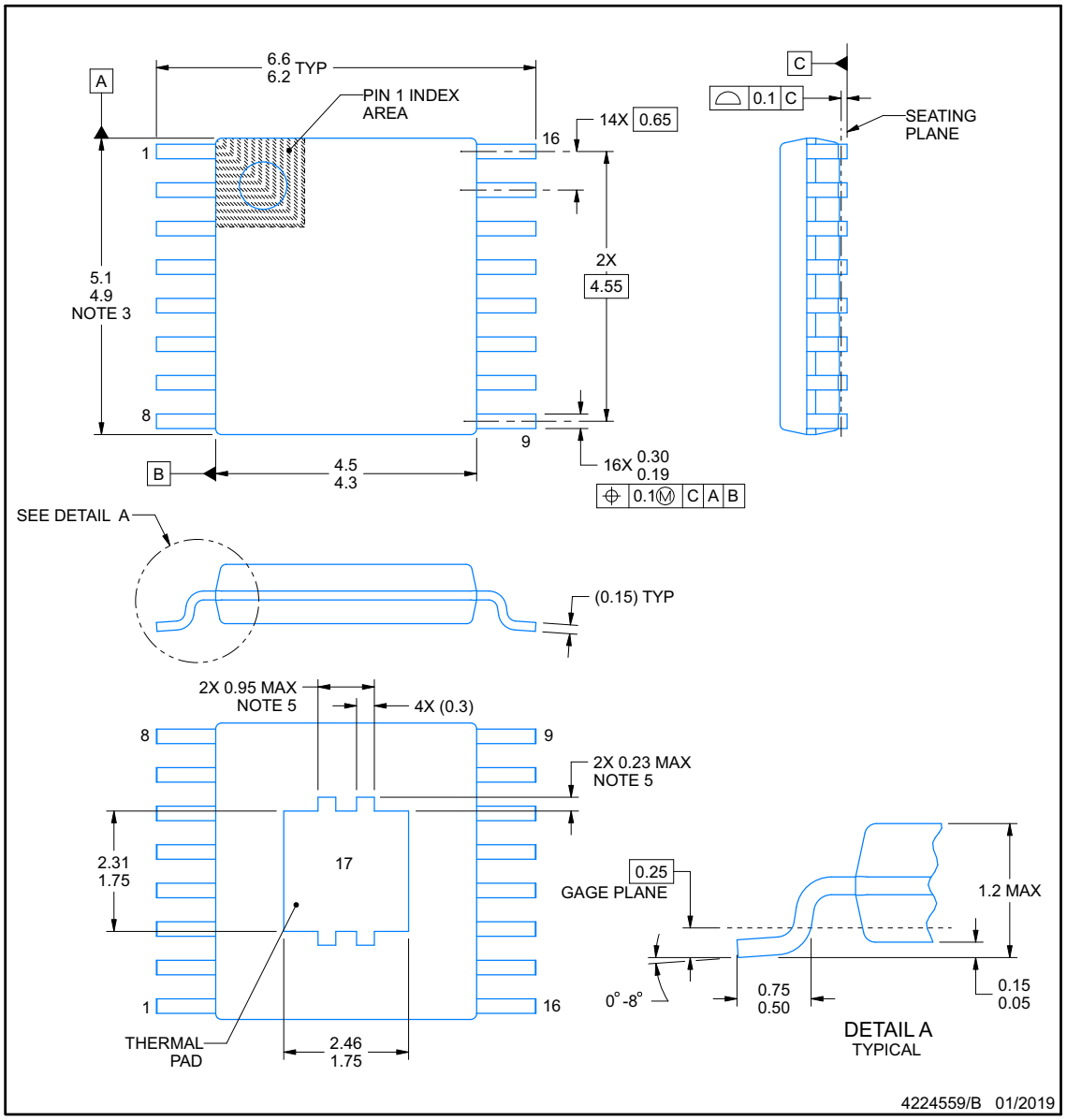
ADVANCE INFORMATION

PACKAGE OUTLINE

PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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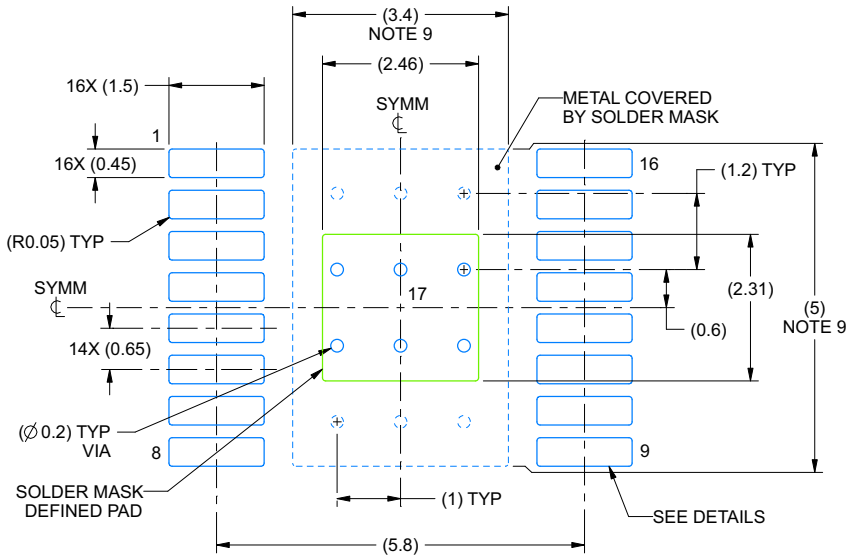
EXAMPLE BOARD LAYOUT

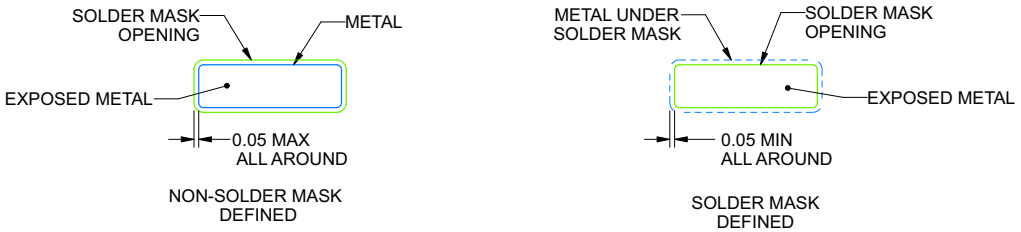
PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4224559/B 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

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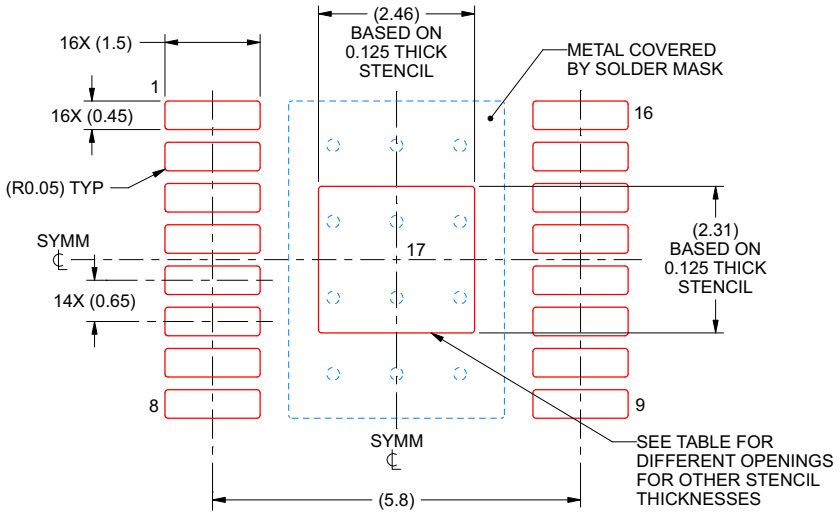
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PWP0016C **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

4224559/B 01/2019

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8428EPWPR	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8428E
DRV8428EPWPR.A	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8428E
DRV8428ERTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8428E
DRV8428ERTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8428E
DRV8428PPWPR	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8428P
DRV8428PPWPR.A	Active	Production	HTSSOP (PWP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8428P
DRV8428PRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8428P
DRV8428PRTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8428P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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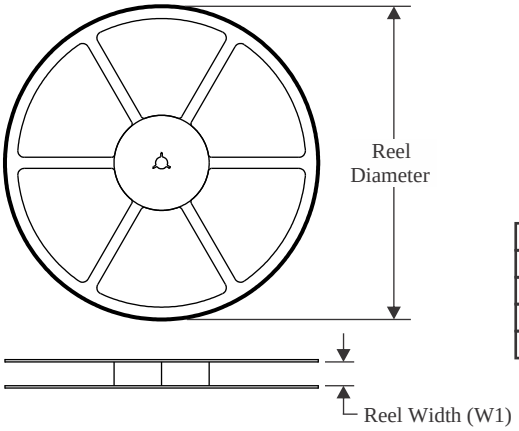
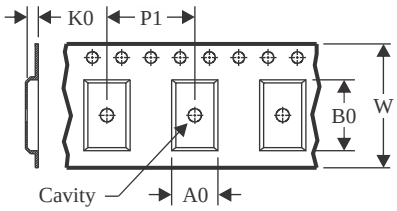
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

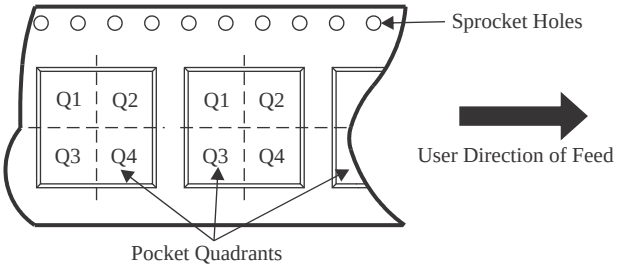


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

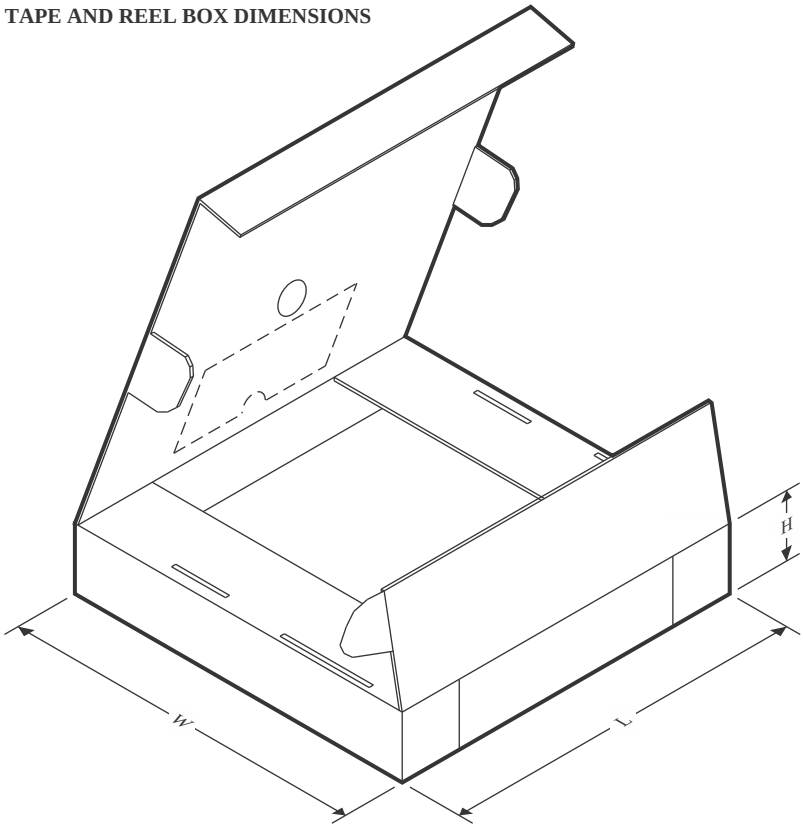
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8428EPWPR	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8428ERTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
DRV8428PPWPR	HTSSOP	PWP	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV8428PRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

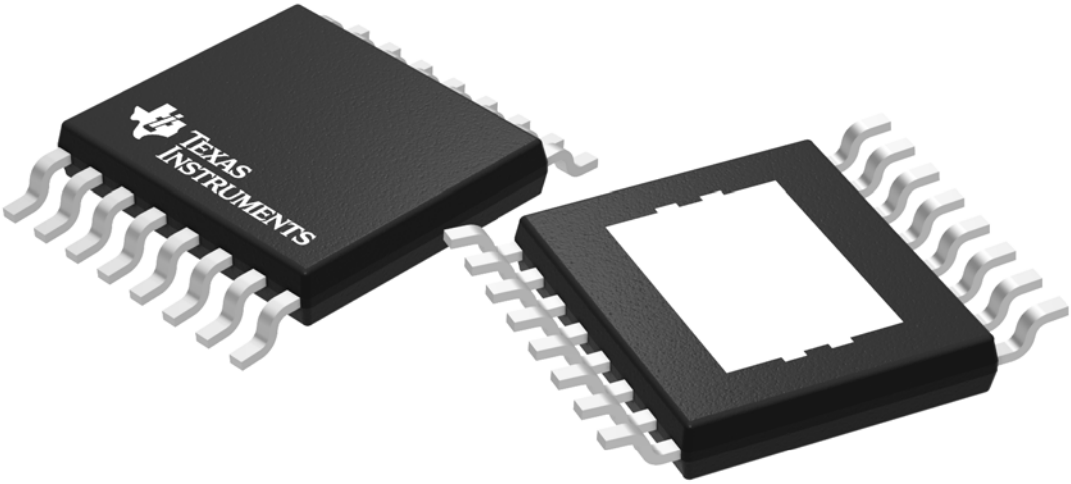


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8428EPWPR	HTSSOP	PWP	16	3000	356.0	356.0	35.0
DRV8428ERTER	WQFN	RTE	16	3000	367.0	367.0	35.0
DRV8428PPWPR	HTSSOP	PWP	16	3000	356.0	356.0	35.0
DRV8428PRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

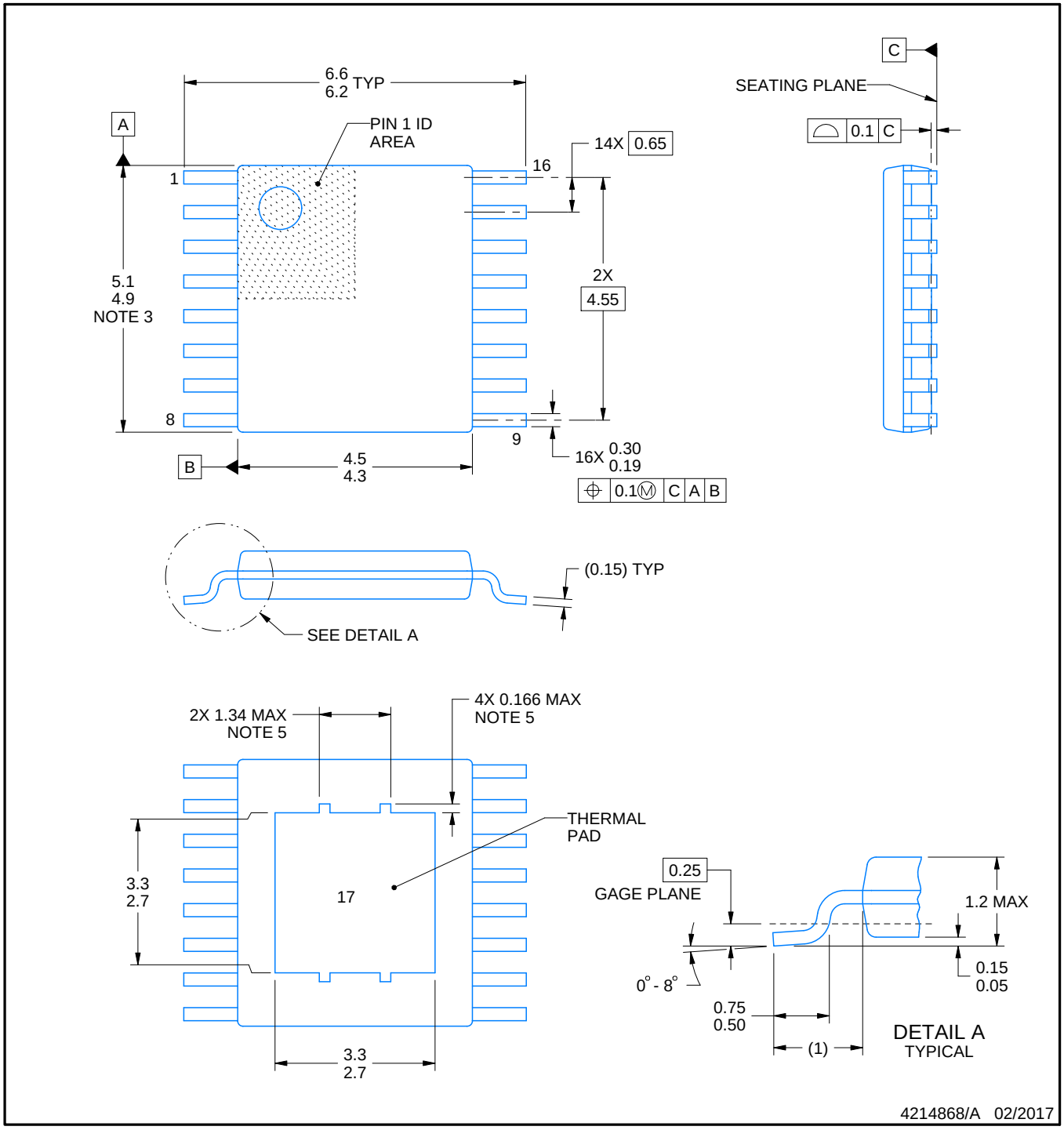
PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

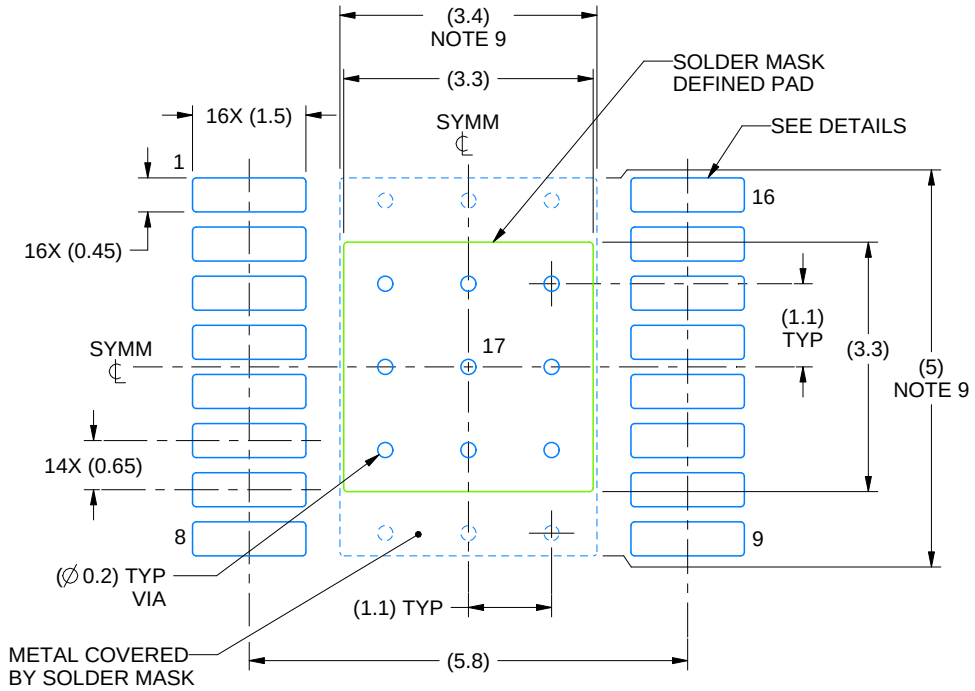
4073225-3/J



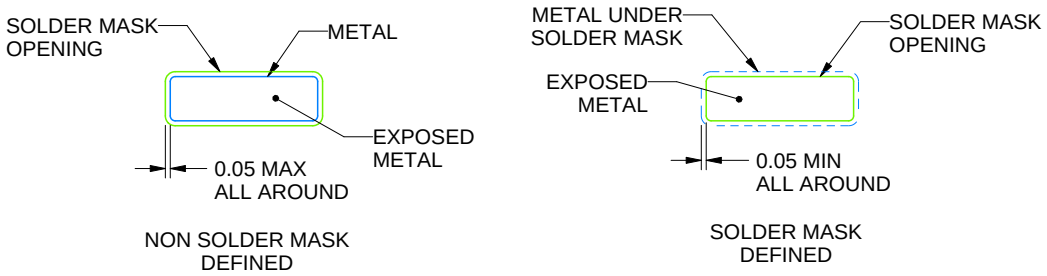
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

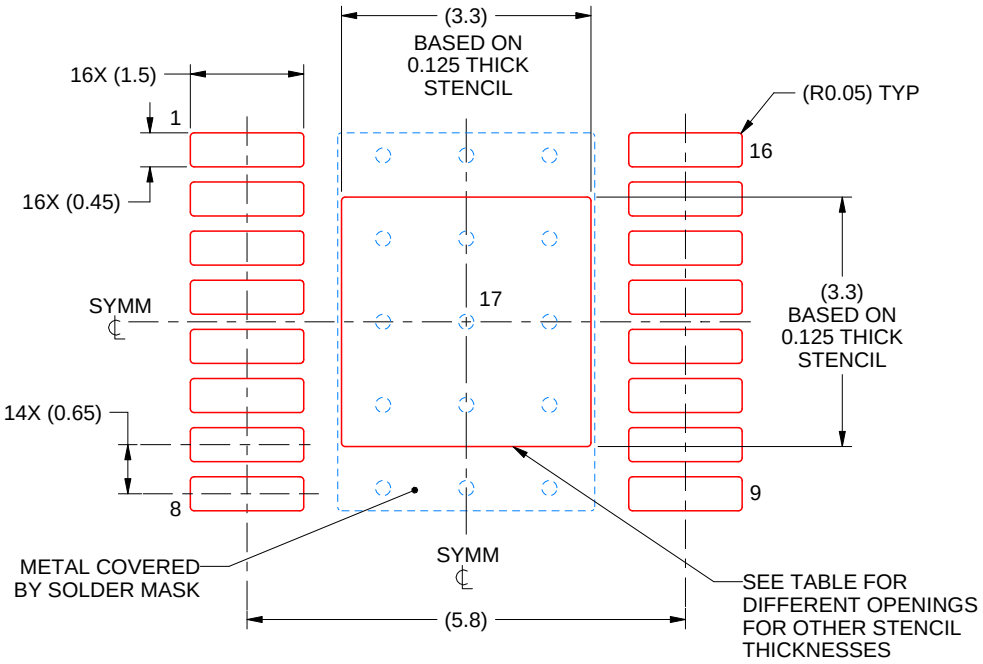


SOLDER MASK DETAILS
PADS 1-16

4214868/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

4214868/A 02/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

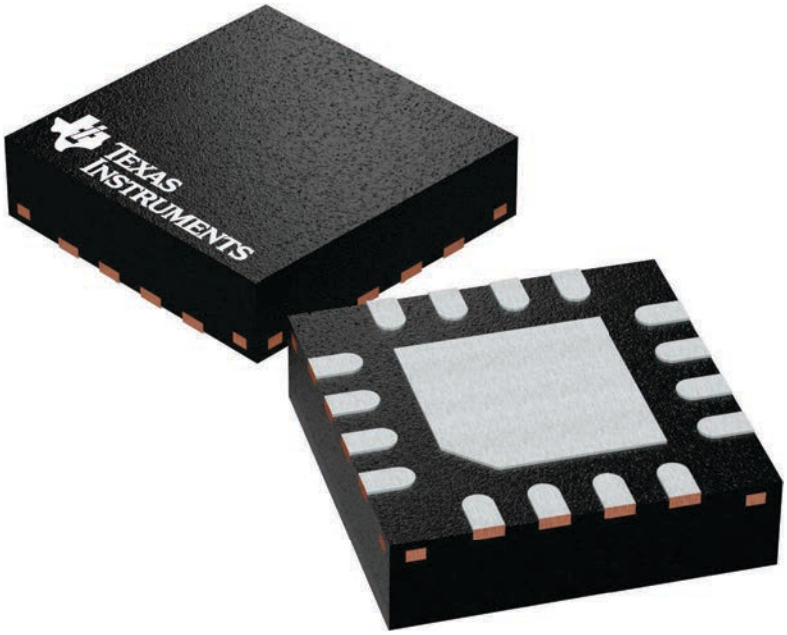
RTE 16

WQFN - 0.8 mm max height

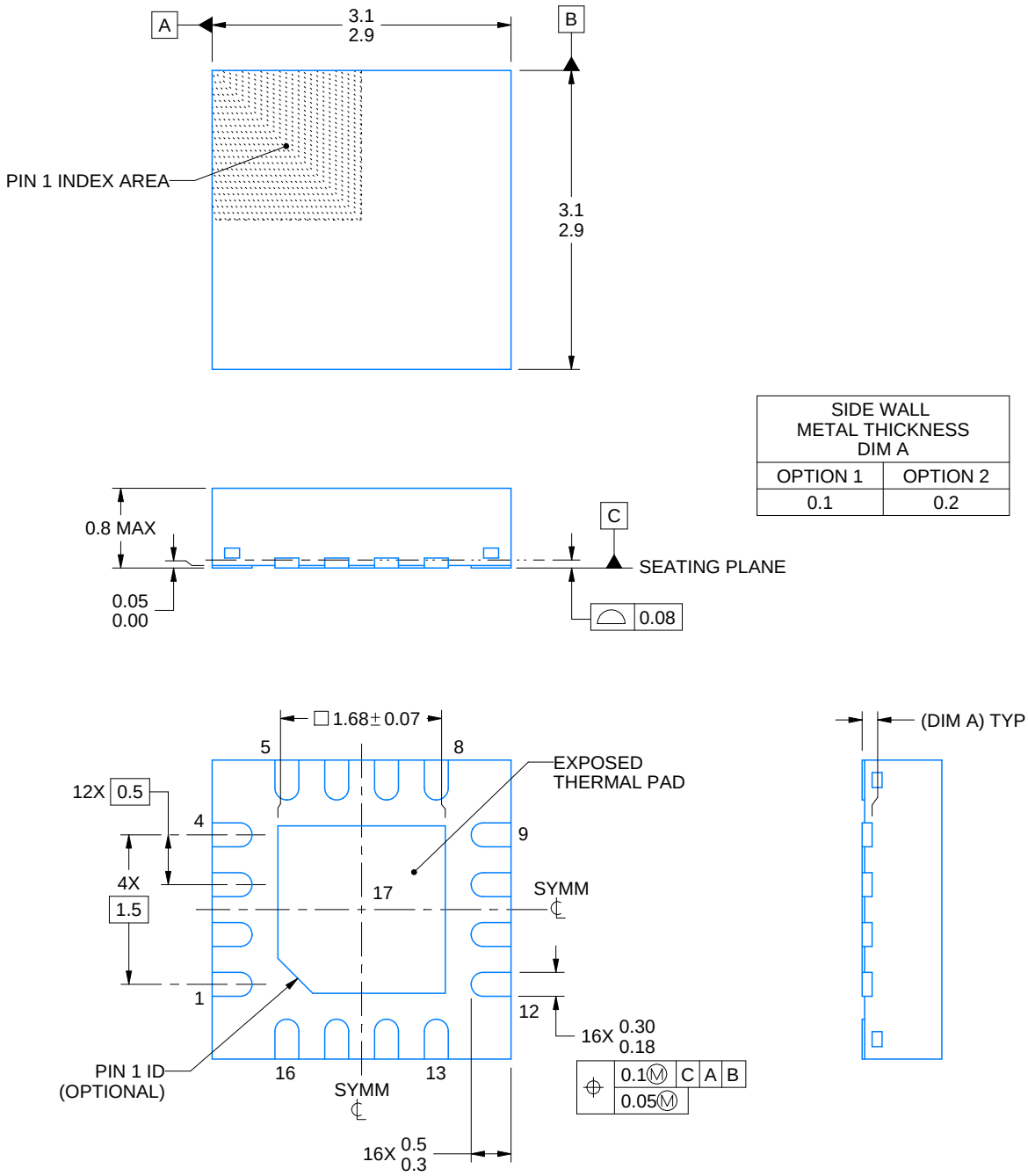
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



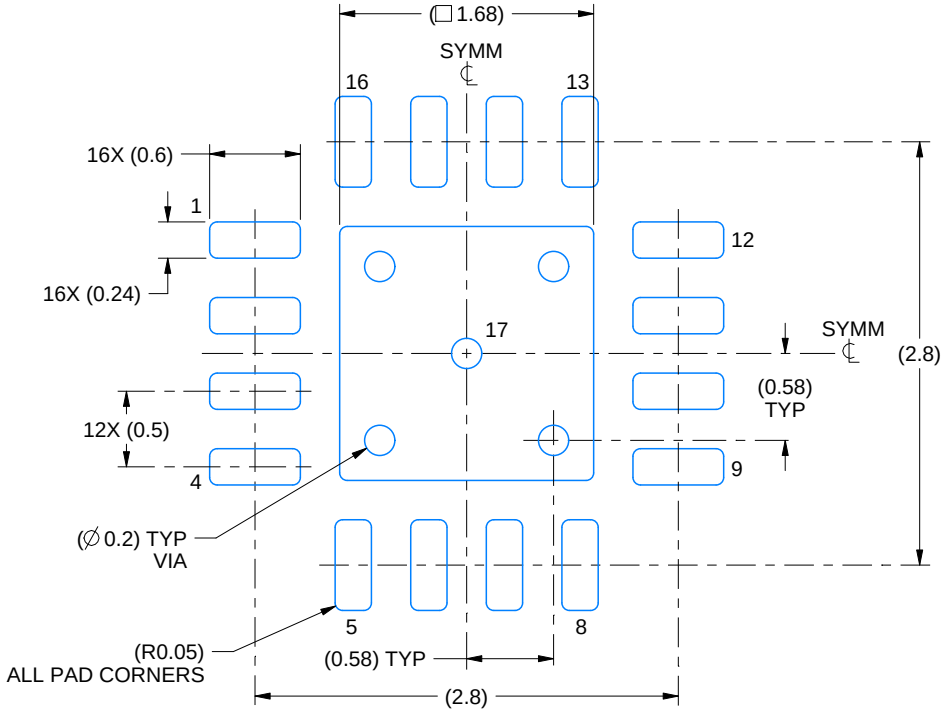
4225944/A



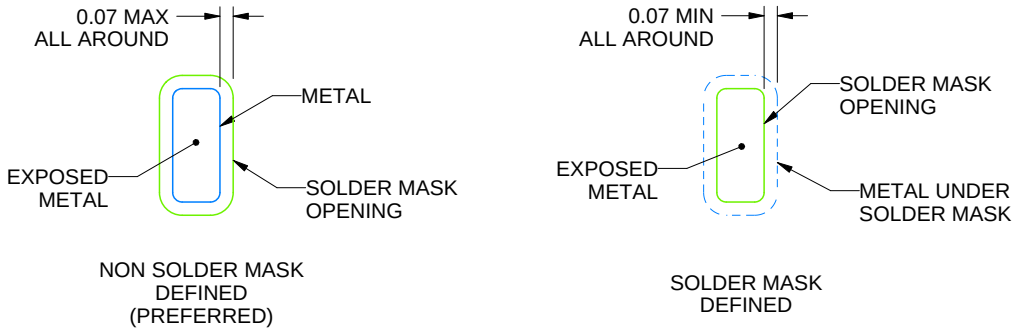
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

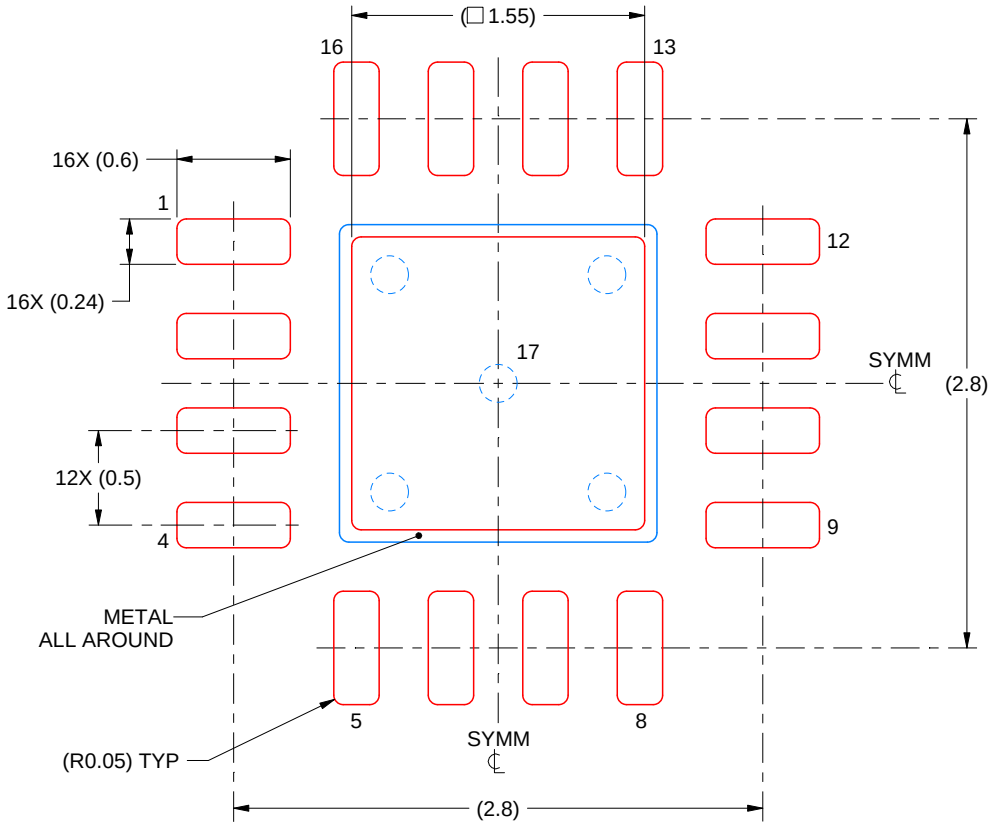


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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