Dual Wideband, Current-Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- FLEXIBLE SUPPLY RANGE:
  - +5V to +12V Single Supply
  - ±2.5V to ±6V Dual Supply
- WIDEBAND +5V OPERATION: 190MHz (G = +2)
- UNITY-GAIN STABLE: 280MHz (G = 1)
- HIGH OUTPUT CURRENT: 190mA
- OUTPUT VOLTAGE SWING: ±4.0V
- HIGH SLEW RATE: 2100V/μs
- LOW SUPPLY CURRENT: 5.1mA/ch
- LOW DISABLED CURRENT: 150μA/ch

APPLICATIONS

- xDSL LINE DRIVER / RECEIVER
- MATCHED I/Q CHANNEL AMPLIFIER
- BROADBAND VIDEO BUFFERS
- HIGH-SPEED IMAGING CHANNELS
- PORTABLE INSTRUMENTS
- DIFFERENTIAL ADC DRIVERS
- ACTIVE FILTERS
- WIDEBAND INVERTING SUMMING

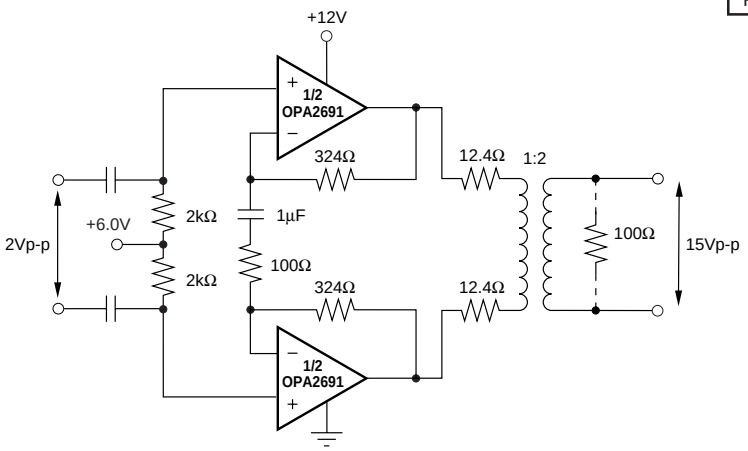
DESCRIPTION

The OPA2691 sets a new level of performance for broadband dual current-feedback op amps. Operating on a very low 5.1mA/ch supply current, the OPA2691 offers a slew rate and output power normally associated with a much higher supply current. A new output stage architecture delivers a high output current with minimal voltage headroom and crossover distortion. This gives exceptional single-supply operation. Using a single +5V supply, the OPA2691 can deliver a 1V to 4V output swing with over 150mA drive current and 190MHz bandwidth. This combination of features makes the OPA2691 an ideal RGB line driver or single-supply Analog-to-Digital Converter (ADC) input driver.

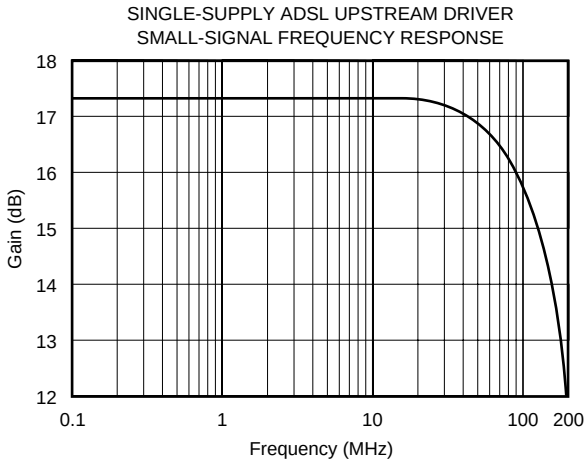
The OPA2691's low 5.1mA/ch supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, ensures lower maximum supply current than competing products. System power may be further reduced by using the optional disable control pin (SO-14 only). Leaving this disable pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA2691 supply current drops to less than 150μA/ch while the output goes into a high impedance state. This feature may be used for power savings.

OPA2691 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage-Feedback	OPA690	OPA2690	OPA3690
Current-Feedback	OPA691	OPA2681	OPA3691
Fixed Gain	OPA692	—	OPA3692



Single-Supply ADSL Upstream Driver



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2691	SO-8	D	–40°C to +85°C	OPA2691	OPA2691ID	Rails, 100
"	"	"	"	"	OPA2691IDR	Tape and Reel, 2500
OPA2691	SO-14	D	–40°C to +85°C	OPA2691	OPA2691I-14D	Rails, 58
"	"	"	"	"	OPA2691I-14DR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	$\pm 6.5 V_{DC}$
Internal Power Dissipation[2]	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: D, 14D	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C
ESD Performance:	
HBM	2000V
CDM	1500V

NOTES: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

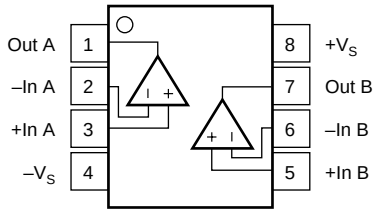
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

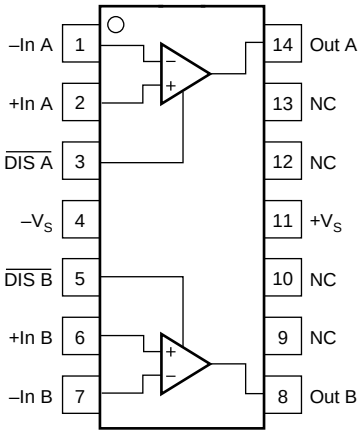
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS

Top View **SO-8**



SO-14



NC = No Connection

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA2691ID, I-14D						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, $R_F = 453\Omega$	280				MHz	typ	C
	G = +2, $R_F = 402\Omega$	225	200	190	180	MHz	min	B
	G = +5, $R_F = 261\Omega$	210				MHz	typ	C
	G = +10, $R_F = 180\Omega$	200				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O = 0.5Vp-p	90	40	35	20	MHz	min	B
Peaking at a Gain of +1	$R_F = 453\Omega$, V_O = 0.5Vp-p	0.2	1	1.5	2	dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 5Vp-p	200				MHz	typ	C
Slew Rate	G = +2, 4V Step	2100	1400	1375	1350	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.6				ns	typ	C
	G = +2, 5V Step	1.9				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd-Harmonic	$R_L = 100\Omega$	–70	–63	–60	–58	dBc	max	B
	$R_L \geq 500\Omega$	–79	–70	–67	–65	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–74	–72	–70	–68	dBc	max	B
	$R_L \geq 500\Omega$	–93	–87	–82	–78	dBc	max	B
Input Voltage Noise	f > 1MHz	1.7	2.5	2.9	3.1	nV/$\sqrt{Hz}$	max	B
Noninverting Input Current Noise	f > 1MHz	12	14	15	15	pA/$\sqrt{Hz}$	max	B
Inverting Input Current Noise	f > 1MHz	15	17	18	19	pA/$\sqrt{Hz}$	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.07				%	typ	C
	$R_L = 37.5\Omega$	0.17				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.02				deg	typ	C
	$R_L = 37.5\Omega$	0.07				deg	typ	C
Channel-to-Channel Crosstalk	f = 5MHz	–86				dBc	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 100\Omega$	225	**125**	110	100	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±0.8	**±3**	±3.7	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+15	**+35**	+43	+45	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			–300	–300	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±5	**±25**	±30	±40	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±90	±200	nA°/C	max	B
INPUT								
Common-Mode Input Range (CMIR)(5)		±3.5	**±3.4**	±3.3	±3.2	V	min	A
Common-Mode Rejection (CMRR)	V_{CM} = 0V	56	**52**	51	50	dB	min	A
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	37				Ω	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing	V_O = 0	+190	**+160**	+140	+100	mA	min	A
Current Output, Sinking	V_O = 0	–190	**–160**	–140	–100	mA	min	A
Short-Circuit Current		±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C
DISABLE (Disabled LOW) (SO-14 only)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, Both Channels	–300	**–600**	–700	–800	µA	max	A
Disable Time	$V_{IN} = 1V_{DC}$	400				ns	typ	C
Enable Time	$V_{IN} = 1V_{DC}$	25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±50				mV	typ	C
Turn-Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	75	**130**	150	160	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Minimum Operating Voltage Range		±2				V	min	C
Max Quiescent Current	V_S = ±5V, Both Channels	10.2	**10.6**	11.2	11.5	mA	max	A
Min Quiescent Current	V_S = ±5V, Both Channels	10.2	**9.8**	9.2	8.9	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	58	**52**	50	49	dB	min	A
TEMPERATURE RANGE								
Specification: D, 14D		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
14D SO-14		100				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25° C specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +15°C at high temperature limit for over temperature specifications. (3) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 453Ω, R_L = 100Ω to V_S/2, and G = +2, (see Figure 1 for AC performance only), unless otherwise noted.

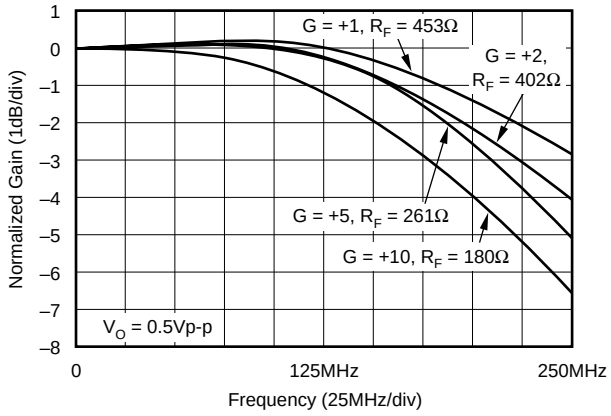
		OPA2691ID, I-14D						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 2)								
Small-Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, R_F = 499Ω	210				MHz	typ	C
	G = +2, R_F = 453Ω	190	168	160	140	MHz	min	B
	G = +5, R_F = 340Ω	180				MHz	typ	C
	G = +10, R_F = 180Ω	155				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p	90	40	30	25	MHz	min	B
Peaking at a Gain of +1	R_F = 649Ω, V_O < 0.5Vp-p	0.2	1	2.5	3.0	dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 2Vp-p	210				MHz	typ	C
Slew Rate	G = +2, 2V Step	850	600	575	550	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	2.0				ns	typ	C
	G = +2, V_O = 2V Step	2.3				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	14				ns	typ	C
0.1%	G = +2, V_O = 2V Step	10				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2Vp-p							
2nd-Harmonic	R_L = 100Ω to V_S/2	–66	–58	–57	–56	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–73	–65	–63	–62	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–71	–68	–67	–65	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–77	–72	–70	–69	dBc	max	B
Input Voltage Noise	f > 1MHz	1.7	2.5	2.9	3.1	nV/$\sqrt{Hz}$	max	B
Noninverting Input Current Noise	f > 1MHz	12	14	15	15	pA/$\sqrt{Hz}$	max	B
Inverting Input Current Noise	f > 1MHz	15	17	18	19	pA/$\sqrt{Hz}$	max	B
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 100Ω to V_S/2	200	**100**	90	80	kΩ	min	A
Input Offset Voltage	V_{CM} = 2.5V	±0.8	**±3.5**	±4.1	±4.8	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 2.5V	+20	**+40**	+48	+56	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 2.5V			–250	–250	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 2.5V	±5	**±20**	±25	±35	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 2.5V			±112	±250	nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		1.5	**1.6**	1.7	1.8	V	max	A
Most Positive Input Voltage(5)		3.5	**3.4**	3.3	3.2	V	min	A
Common-Mode Rejection (CMRR)	V_{CM} = 2.5V	54	**50**	49	48	dB	min	A
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	40				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4	**3.8**	3.7	3.5	V	min	A
	R_L = 100Ω, 2.5V	3.9	**3.7**	3.6	3.4	V	min	A
Least Positive Output Voltage	No Load	1	**1.2**	1.3	1.5	V	max	A
	R_L = 100Ω, 2.5V	1.1	**1.3**	1.4	1.6	V	max	A
Current Output, Sourcing	V_O = V_S/2	+160	**+120**	+100	+80	mA	min	A
Current Output, Sinking	V_O = V_S/2	–160	**–120**	–100	–80	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.03				Ω	typ	C
DISABLE (Disabled LOW) (SO-14 only)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, Both Channels	–300	**–600**	–700	–800	µA	max	A
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±50				mV	typ	C
Turn-Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	75	130	150	160	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			**12**	12	12	V	max	A
Minimum Single-Supply Operating Voltage		4				V	min	C
Max Quiescent Current	V_S = +5V, Both Channels	9	**9.6**	10	10.4	mA	max	A
Min Quiescent Current	V_S = +5V, Both Channels	9	**8.2**	8.0	7.8	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	55				dB	typ	C
TEMPERATURE RANGE								
Specification: D, 14D		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
14D SO-14		100				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for +25°C specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +15°C at high temperature limit for over temperature specifications. (3) Test Levels: (A) 100% tested at +25°C. Over-temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out of node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

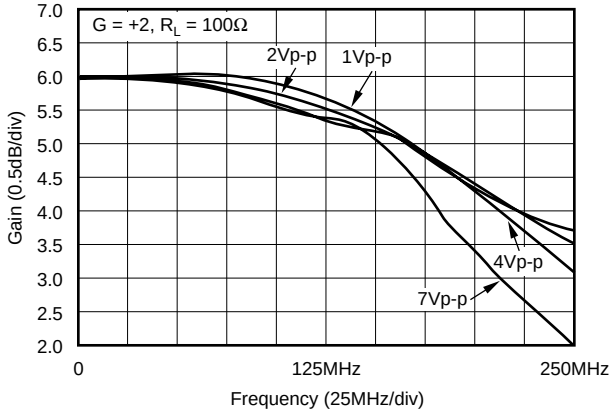
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

G = +2, R_F = 402Ω, R_L = 100Ω, unless otherwise noted (see Figure 1 for AC performance only).

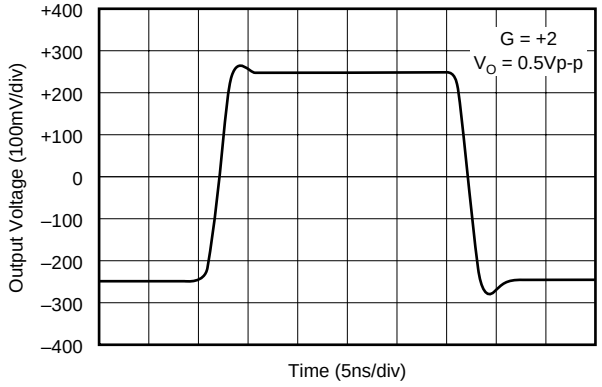
SMALL-SIGNAL FREQUENCY RESPONSE



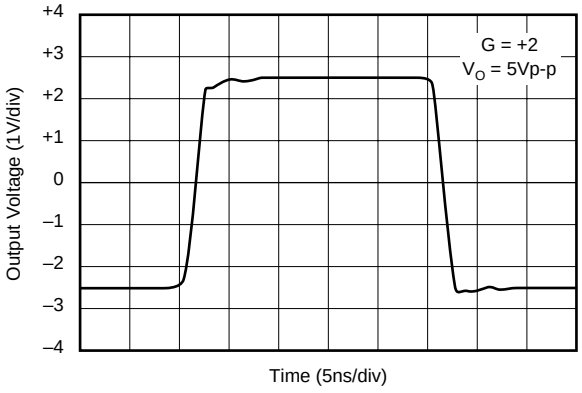
LARGE-SIGNAL FREQUENCY RESPONSE



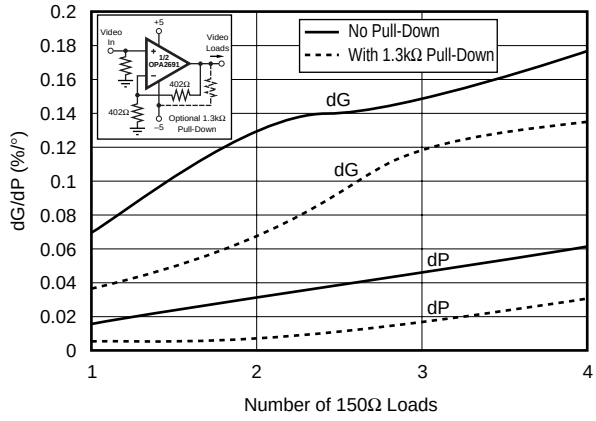
SMALL-SIGNAL PULSE RESPONSE



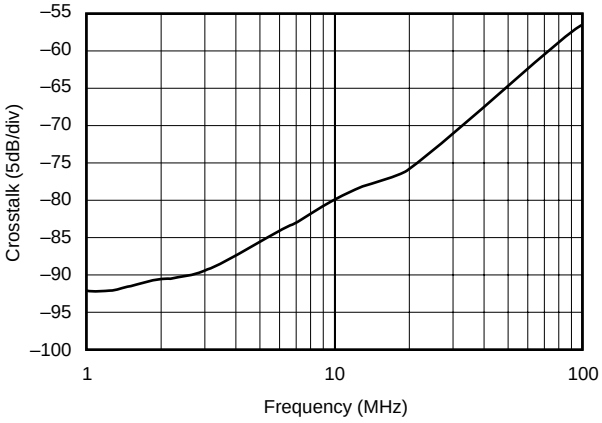
LARGE-SIGNAL PULSE RESPONSE



COMPOSITE VIDEO dG/dP



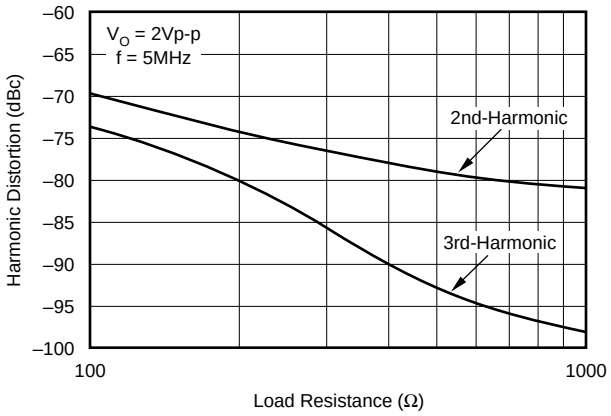
CHANNEL-TO-CHANNEL CROSSTALK



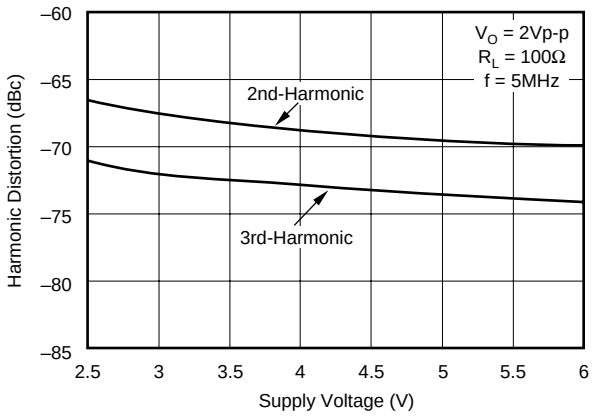
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

G = +2, R_F = 402Ω, R_L = 100Ω, unless otherwise noted (see Figure 1 for AC performance only).

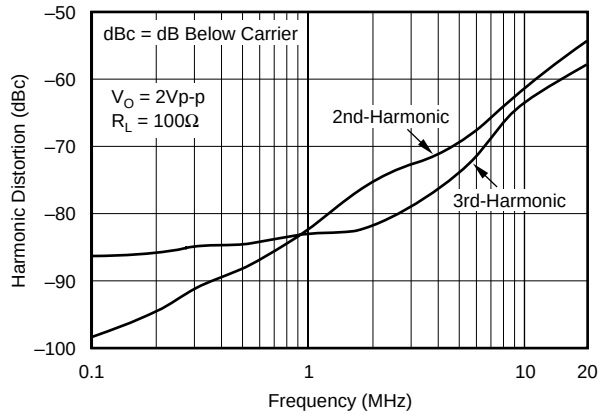
HARMONIC DISTORTION vs LOAD RESISTANCE



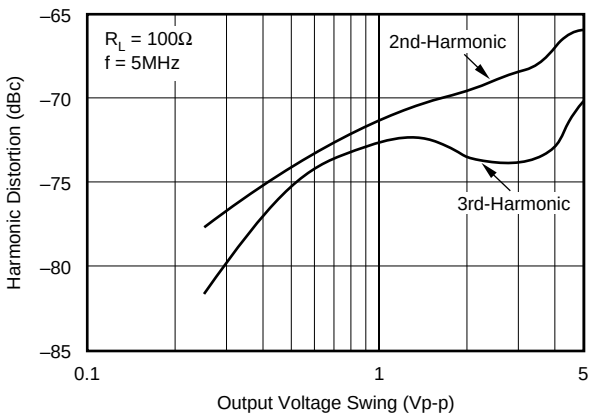
HARMONIC DISTORTION vs SUPPLY VOLTAGE



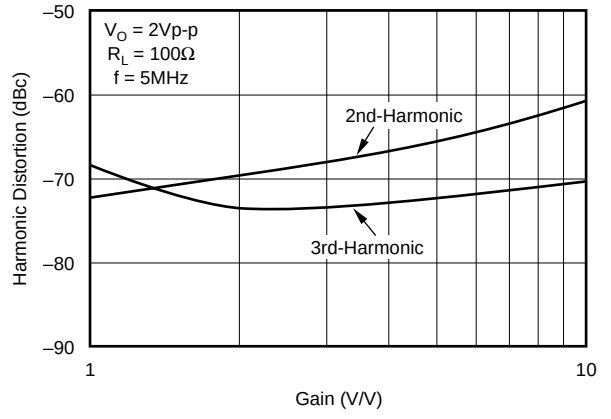
HARMONIC DISTORTION vs FREQUENCY



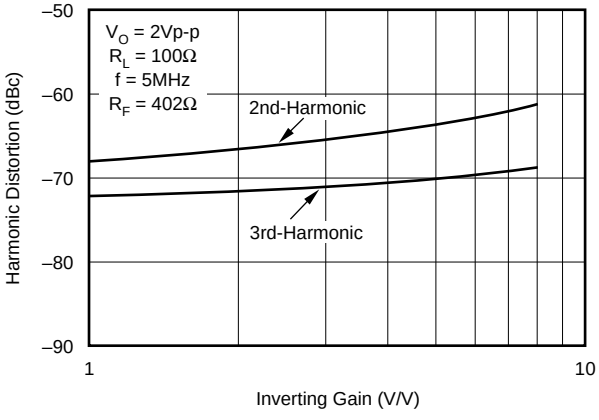
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



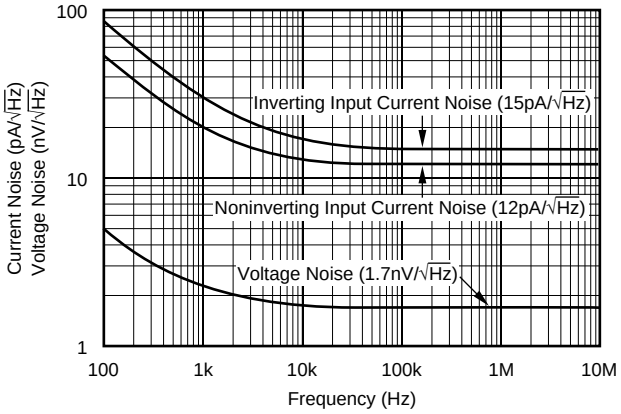
HARMONIC DISTORTION vs INVERTING GAIN



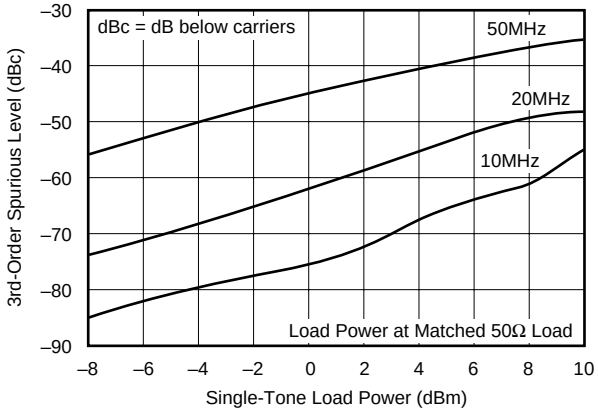
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

G = +2, R_F = 402Ω, R_L = 100Ω, unless otherwise noted (see Figure 1 for AC performance only).

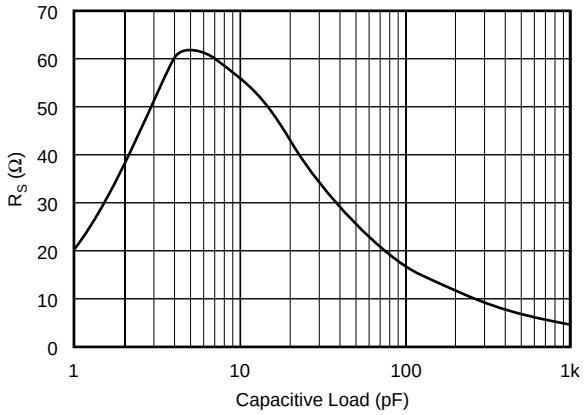
INPUT VOLTAGE AND CURRENT NOISE DENSITY



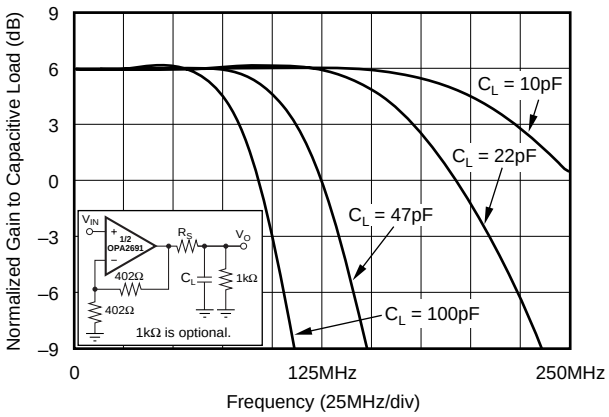
2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



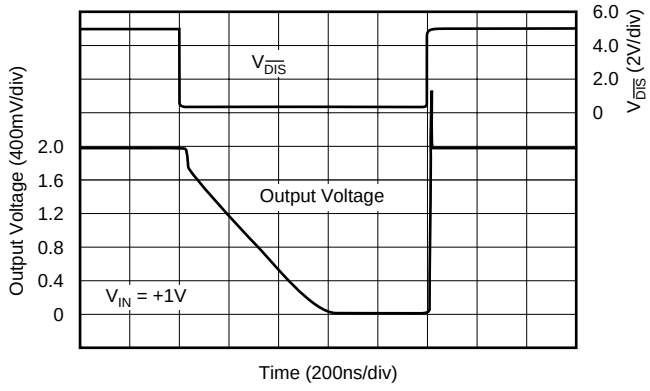
RECOMMENDED R_S vs CAPACITIVE LOAD



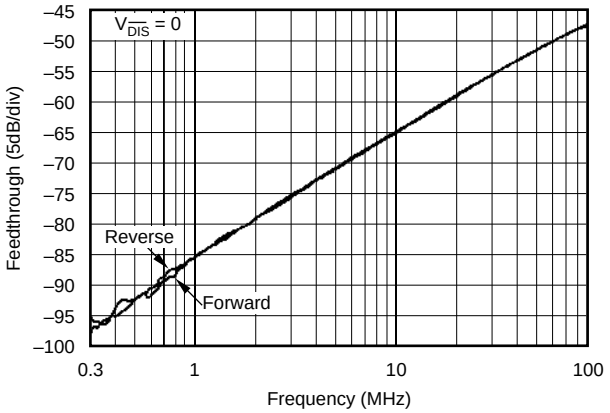
FREQUENCY RESPONSE vs CAPACITIVE LOAD



LARGE-SIGNAL DISABLE/ENABLE RESPONSE



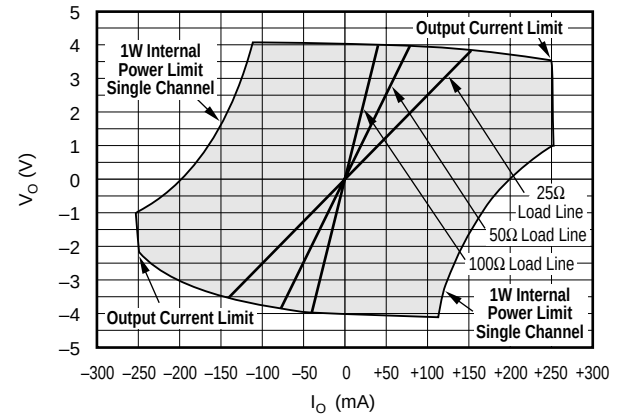
DISABLED FEEDTHROUGH vs FREQUENCY



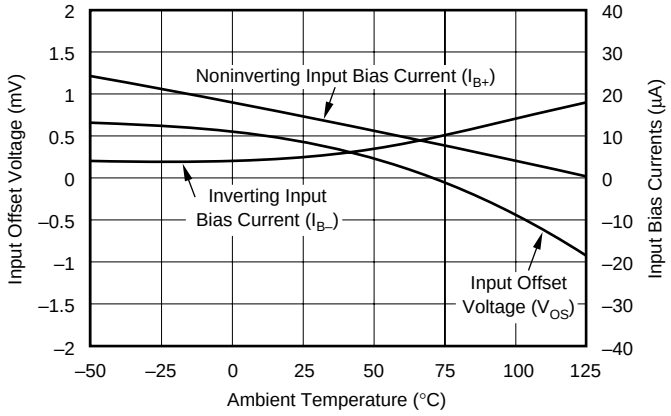
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

G = +2, R_F = 402Ω, R_L = 100Ω, unless otherwise noted (see Figure 1 for AC performance only).

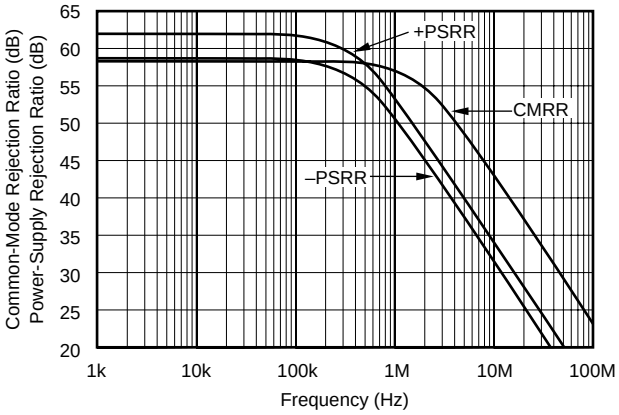
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



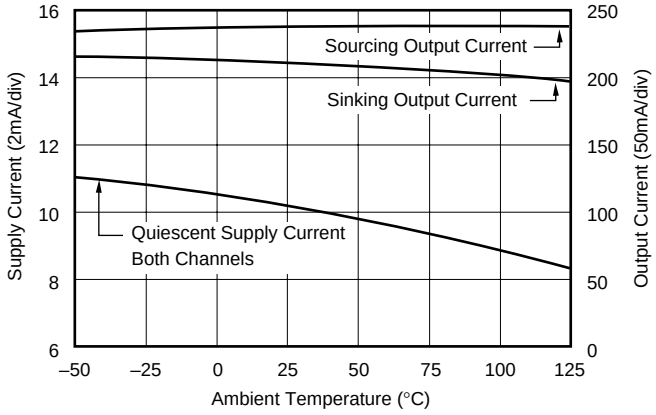
TYPICAL DC DRIFT OVER TEMPERATURE



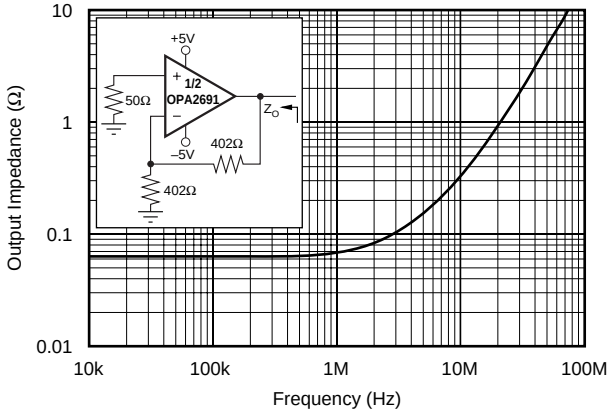
CMRR AND PSRR vs FREQUENCY



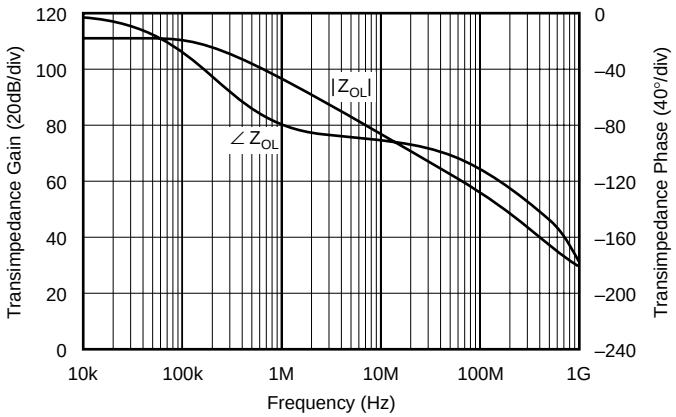
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



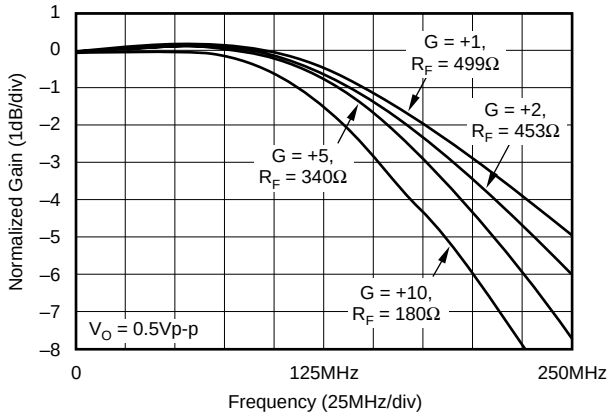
OPEN-LOOP TRANSIMPEDANCE GAIN/PHASE



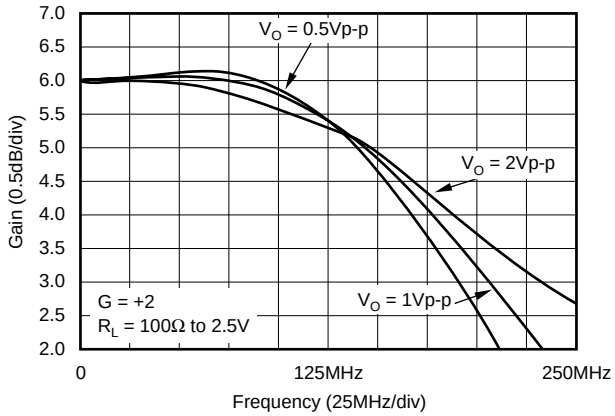
TYPICAL CHARACTERISTICS: V_S = +5V

G = +2, R_F = 499Ω, R_L = 100Ω to +2.5V, unless otherwise noted (see Figure 2 for AC performance only).

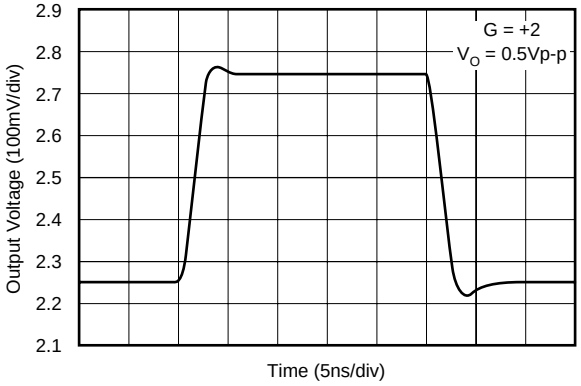
SMALL-SIGNAL FREQUENCY RESPONSE



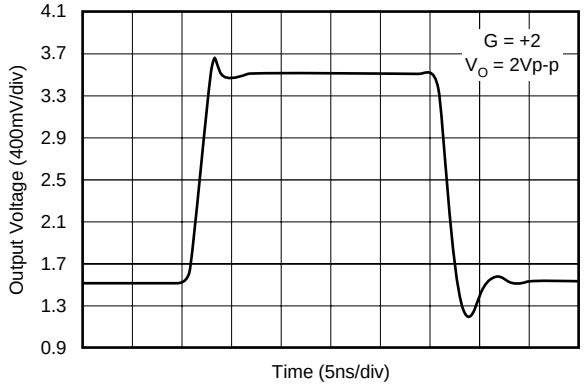
LARGE-SIGNAL FREQUENCY RESPONSE



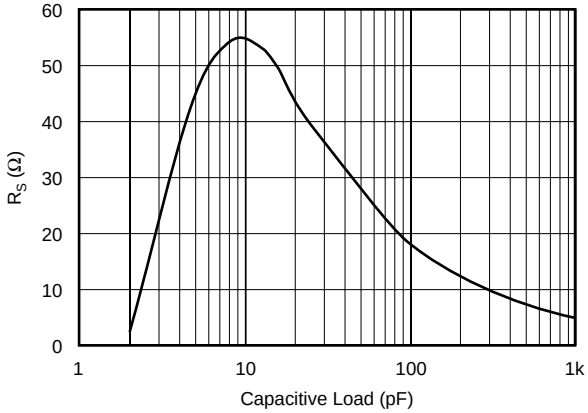
SMALL-SIGNAL PULSE RESPONSE



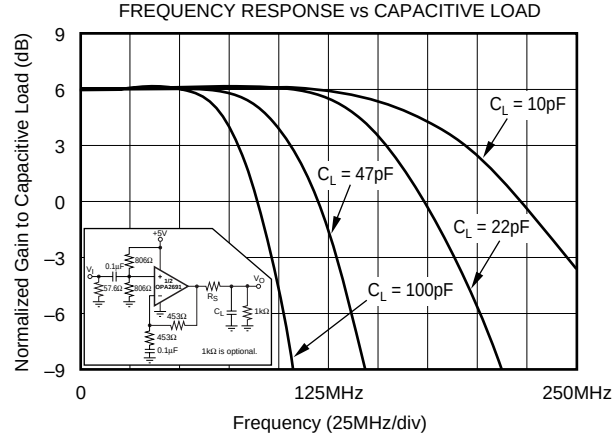
LARGE-SIGNAL PULSE RESPONSE



RECOMMENDED R_S vs CAPACITIVE LOAD



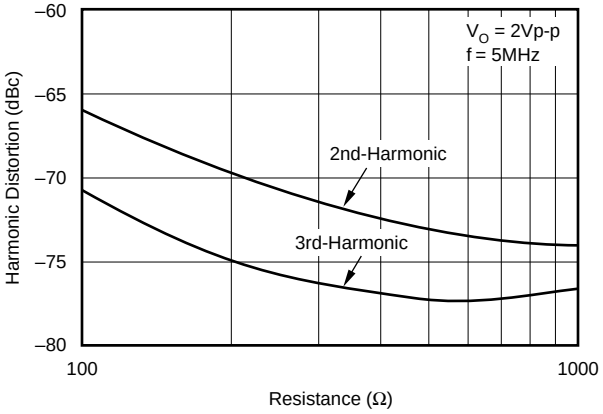
FREQUENCY RESPONSE vs CAPACITIVE LOAD



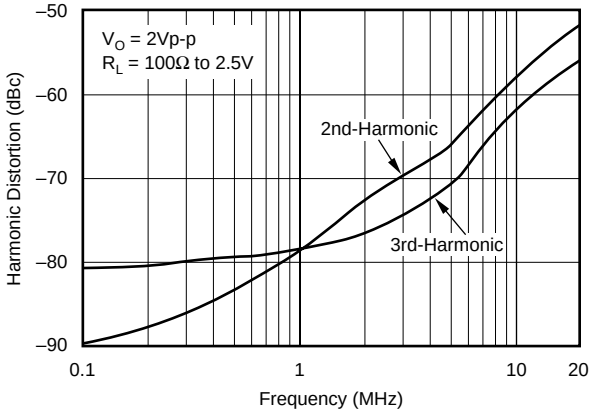
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

G = +2, R_F = 499Ω, R_L = 100Ω to +2.5V, unless otherwise noted (see Figure 2 for AC performance only).

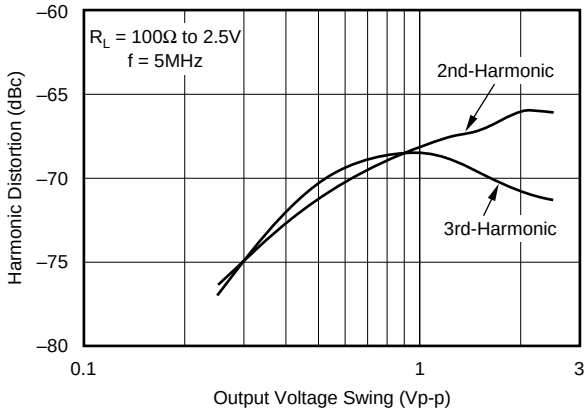
HARMONIC DISTORTION vs LOAD RESISTANCE



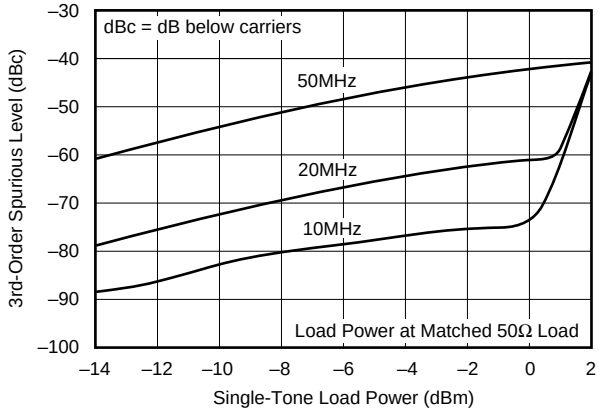
HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs OUTPUT VOLTAGE



2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



APPLICATIONS INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA2691 gives the exceptional AC performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 5.1mA/ch quiescent current, the OPA2691 will swing to within 1V of either supply rail and deliver in excess of 160mA tested at room temperature. This low output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA2691 will deliver greater than 200MHz bandwidth driving a 2Vp-p output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers have typically suffered from very poor crossover distortion as the output current goes through zero. The OPA2691 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that AC performance (bandwidth and distortion) is relatively independent of signal gain. For similar AC performance with improved DC accuracy, consider the high slew rate, unity-gain stable, voltage-feedback OPA2690.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the electrical characteristics are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 804Ω = 89Ω. The disable control line ($\overline{DIS}$) is typically left open (SO-14 only) to ensure normal amplifier operation. One optional component is included in Figure 1. In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

Figure 2 shows the AC-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Electrical Characteristics and Typical Characteristics. Though not a *rail-to-rail* design, the OPA2691 requires minimal input and output voltage headroom compared to other very wideband current-feedback op amps. It will deliver a 3Vp-p output swing on a single +5V supply with greater than 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 2 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a 2Vp-p input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1—which puts the input DC bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5V operation, gain of +2, operation (see the Setting Resistor Values to Optimize Bandwidth section). Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 75mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA2691 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, 3rd-harmonic distortion plots.

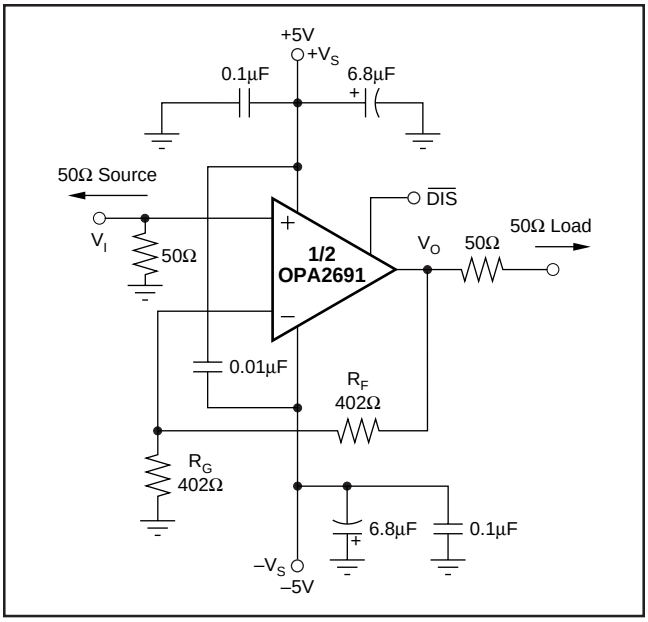


FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

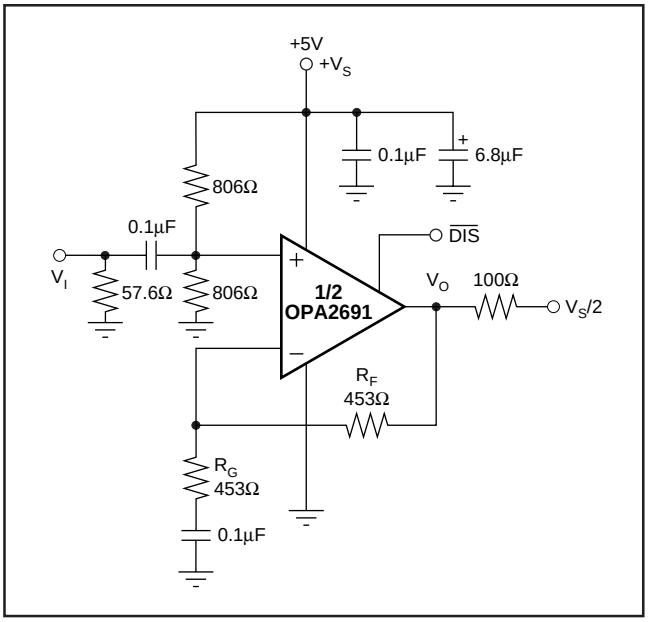


FIGURE 2. AC-Coupled, G = +2, Single-Supply Specification and Test Circuit.

SINGLE-SUPPLY DIFFERENTIAL ADC DRIVER

Figure 3 shows a gain of +10 Single-Ended In/Diff. Out single-supply ADC driver. Using a dual amplifier like the OPA2691 helps reduce the necessary board space, as it also reduces the amount of required supply bypassing components. From a signal point of view, dual amplifiers provide excellent performance matching (for example, gain and phase matching). The differential ADC driver circuit shown in Figure 3 takes advantage of this fact. A transformer converts the single-ended input signal into a low-level differential signal which is applied to the high impedance noninverting inputs of each of the two amplifiers in the OPA2691. Resistor R_G between the inverting inputs controls the AC-gain of this circuit according to equation $G = 1 + 2R_F/R_G$. With the resistor values shown, the AC-gain is set to 10. Adding a capacitor (0.1µF) in series with R_G blocks, the DC-path gives a DC gain of +1 for the common-mode voltage. This allows, in a very simple way, to apply the required DC bias voltage of +2.5V to the inputs of the amplifiers, which will also appear at their outputs. Like the OPA2691, the ADC ADS823 operates on a single +5V supply. Its internal common-mode voltage is typically +2.5V which equals the required bias voltage for the OPA2691.

Connecting two resistors between the top reference (REFT = +3.5V) and bottom reference (REFB = +1.5V) develops a +2.5V voltage level at their midpoint. Applying that to the center tap of the transformer biases the amplifiers appropriately. Sufficient bypassing at the center tap must be provided to keep this point at a solid AC ground. Resistors R_S isolate the op amp output from the capacitive input of the converter, as well as forming a 1st-order, low-pass filter with capacitor C_1 to attenuate some of the wideband noise. This interface will provide > 150MHz full-scale input bandwidth to the ADS823.

WIDEBAND VIDEO MULTIPLEXING

One common application for video speed amplifiers which include a disable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple *Wired-OR Video Multiplexer* can be easily implemented using the OPA2691I-14D, see Figure 4.

Typically, channel switching is performed either on sync or retrace time in the video signal. The two inputs are approximately equal at this time. The *make-before-break* disable characteristic of the OPA2691 ensures that there is always one amplifier controlling the line when using a wired-OR circuit like that presented in Figure 4. Since both inputs may be on for a short period during the transition between channels, the outputs are combined through the output impedance matching resistors (82.5Ω in this case). When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal in getting out onto the cable. The gain and output matching resistors have been slightly increased to get a signal gain of +1 at the matched load and provide a 75Ω output impedance to the cable. The video multiplexer connection (see Figure 4) also insures that the maximum differential voltage across the inputs of the unselected channel do not exceed the rated ±1.2V maximum for standard video signal levels.

The section on Disable Operation shows the turn-on and turn-off switching glitches using a grounded input for a single channel is typically less than ±50mV. Where two outputs are switched (see Figure 4), the output line is always under the control of one amplifier or the other due to the “make-before-break” disable timing. In this case, the switching glitches for two 0V inputs drop to < 20mV.

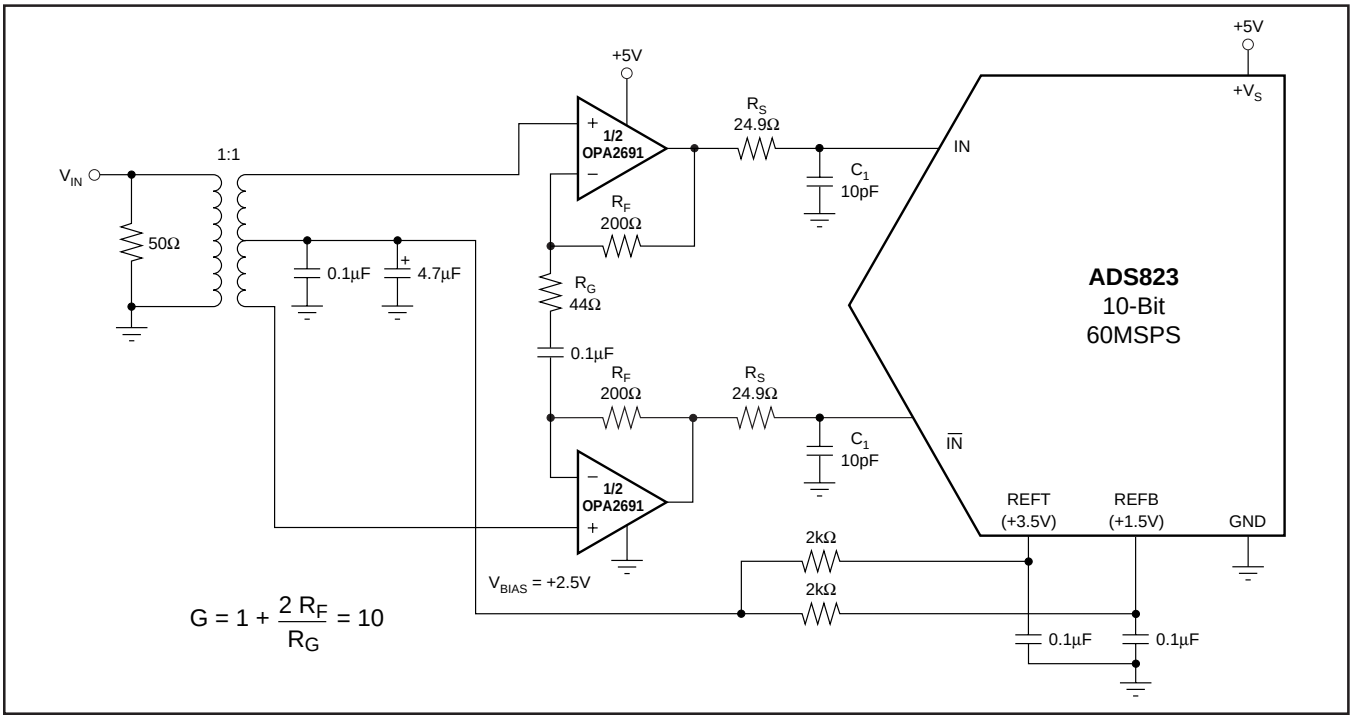


FIGURE 3. Wideband, Single-Supply, Differential ADC Driver.

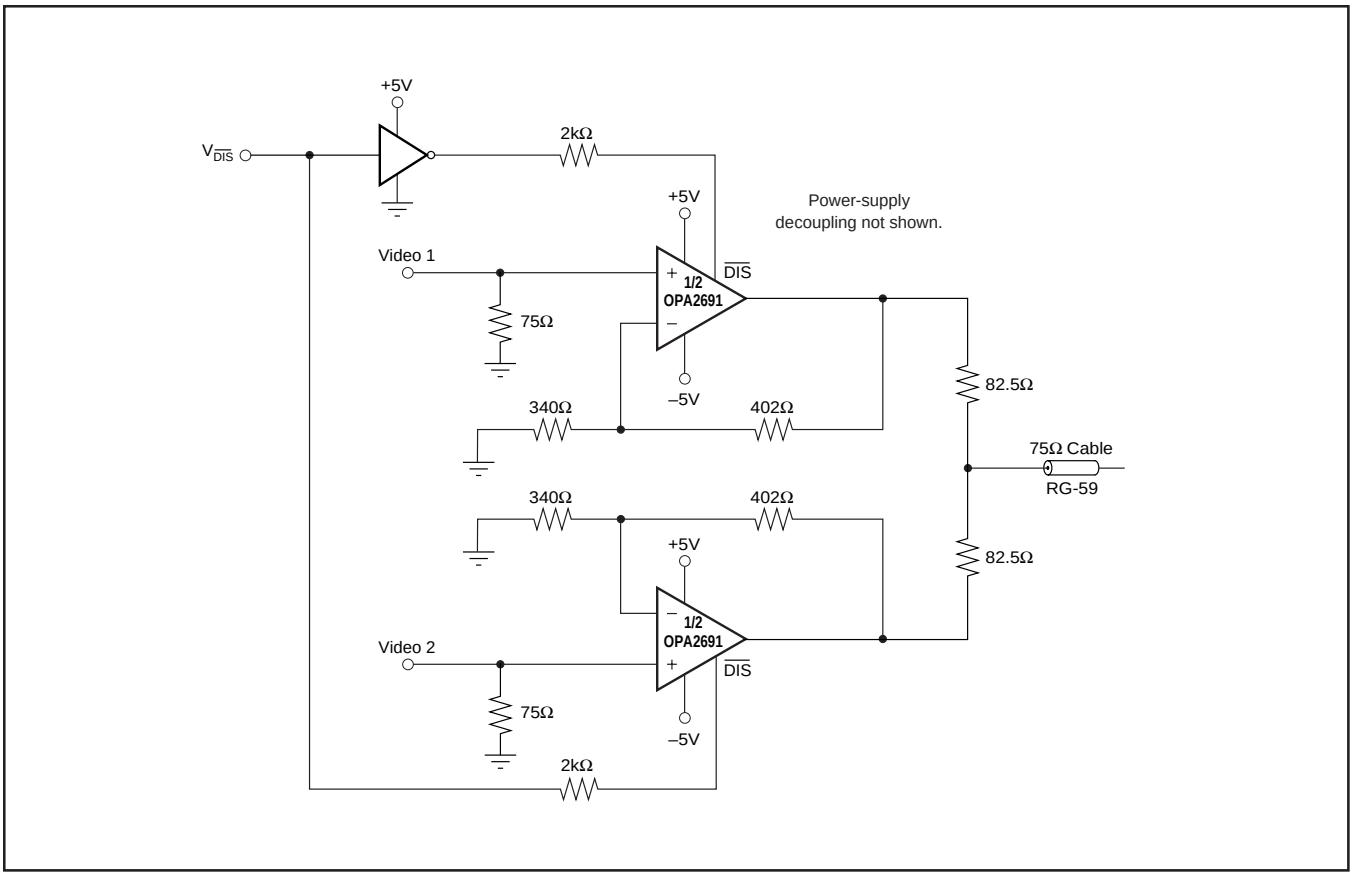


FIGURE 4. Two-Channel Video Multiplexer.

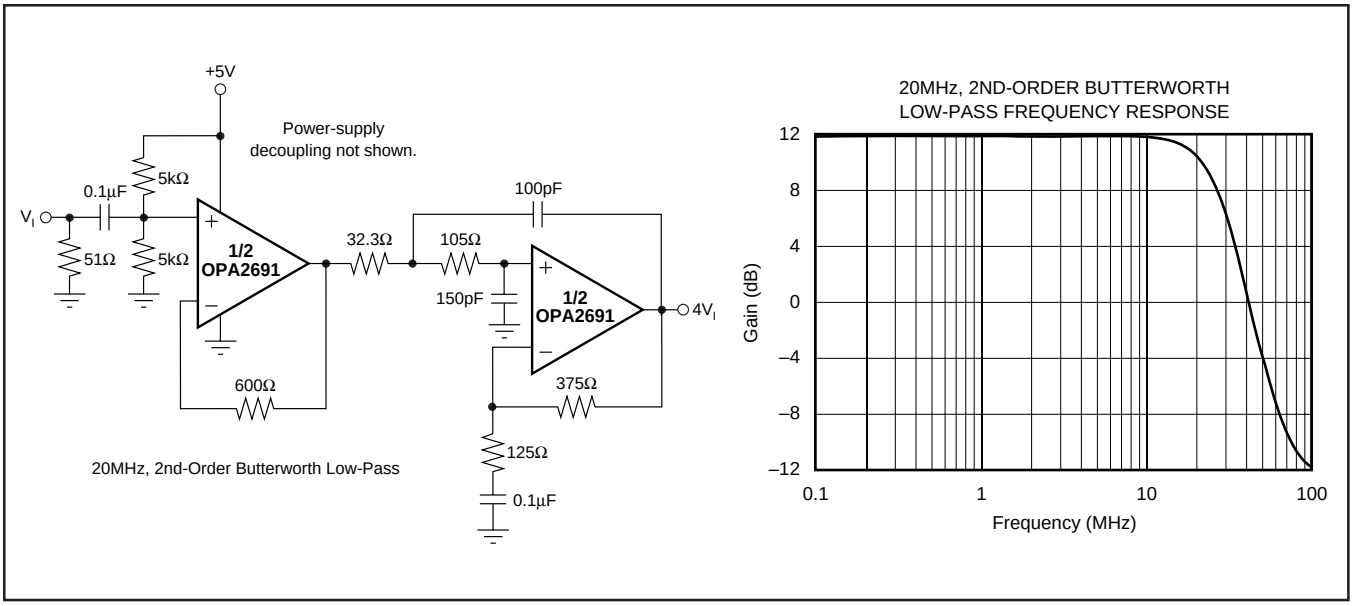


FIGURE 5. Buffered Single-Supply Active Filter.

HIGH-SPEED ACTIVE FILTERS

Wideband current-feedback op amps make ideal elements for implementing high-speed active filters where the amplifier is used as a fixed gain block inside a passive RC circuit network. Their relatively constant bandwidth versus gain, provides low interaction between the actual filter poles and the required gain for the amplifier. Figure 5 shows an example single-supply buffered filter application. In this case, one of the OPA2691 channels is used to setup the DC operating point and provide impedance isolation from the signal source into the 2nd-stage filter. That stage is set up to implement a 20MHz maximally flat Butterworth frequency response and provide an AC gain of +4.

The 51Ω input matching resistor is optional in this case. The input signal is AC-coupled to the 2.5V DC reference voltage developed through the resistor divider from the +5V power supply. This first stage acts as a gain of +1 voltage buffer for the signal where the 600Ω feedback resistor is required for stability. This first stage easily drives the low input resistors required at the input of this high-frequency filter. The 2nd stage is set for a DC gain of +1—carrying the 2.5V operating point through to the output pin, and an AC gain of +4. The feedback resistor has been adjusted to optimize bandwidth for the amplifier itself. As the single-supply frequency response plots show, the OPA2691 in this configuration will give > 200MHz small-signal bandwidth. The capacitor values were chosen as low as possible but adequate to swamp out the parasitic input capacitance of the amplifier. The resistor values were slightly adjusted to give the desired filter frequency response while accounting for the approximate 1ns propagation delay through each channel of the OPA2691.

HIGH-POWER TWISTED-PAIR DRIVER

A very demanding application for a high-speed amplifier is to drive a low load impedance while maintaining a high output voltage swing to high frequencies. Using the dual current-feedback op amp OPA2691, a 15Vp-p output signal swing into a twisted-pair line with a typical impedance of 100Ω can be realized. Configured as shown on the front page, the two amplifiers of the OPA2691 drive the output transformer in a push-pull configuration thus doubling the peak-to-peak signal swing at each op amp's output to 15Vp-p. The transformer has a turns ratio of 2. In order to provide a matched source, this requires a 25Ω source impedance (R_S), for the primary side, given the transformer equation $n^2 = R_L/R_S$. Dividing this impedance equally between the outputs requires a series termination matching resistor at each output of 12.4Ω. Taking the total resistive load of 25Ω (for the differential output signal) and drawing a load line on the *Output Voltage and Current Limitations* plot it can be seen that a 1.5V headroom is required at both the positive and negative peak currents of 150mA.

Line driver applications usually have a high demand for transmitting the signal with low distortion. Current-feedback amplifiers like the OPA2691 are ideal for delivering low distortion performance to higher gains. The example shown is set for a differential gain of 7.5. This circuit can deliver the maximum 15Vp-p signal with over 60MHz bandwidth.

WIDEBAND (200MHz) INSTRUMENTATION AMPLIFIER

As discussed previously, the current-feedback topology of the OPA2691 provides a nearly constant bandwidth as signal gain is increased. The three op amp wideband instrumentation amplifiers depicted in Figure 6 takes advantage of this, achieving a differential bandwidth of 200MHz. The signal is applied to the high-impedance noninverting inputs of the OPA2691. The differential gain is set by $(1 + 2R_F/R_G)$—which is equal to 5 using the values shown in Figure 6. The feedback resistors, R_F, are optimized at this particular gain. Gain adjustments can be made by adjusting R_G. The differential to single-ended conversion is performed by the voltage-feedback amplifier OPA690, configured as a standard difference amplifier. To maintain good distortion performance for the OPA2691, the loading at each amplifier output has been matched by setting $R_3 + R_4 = R_1$, rather than using the same resistor values within the difference amplifier.

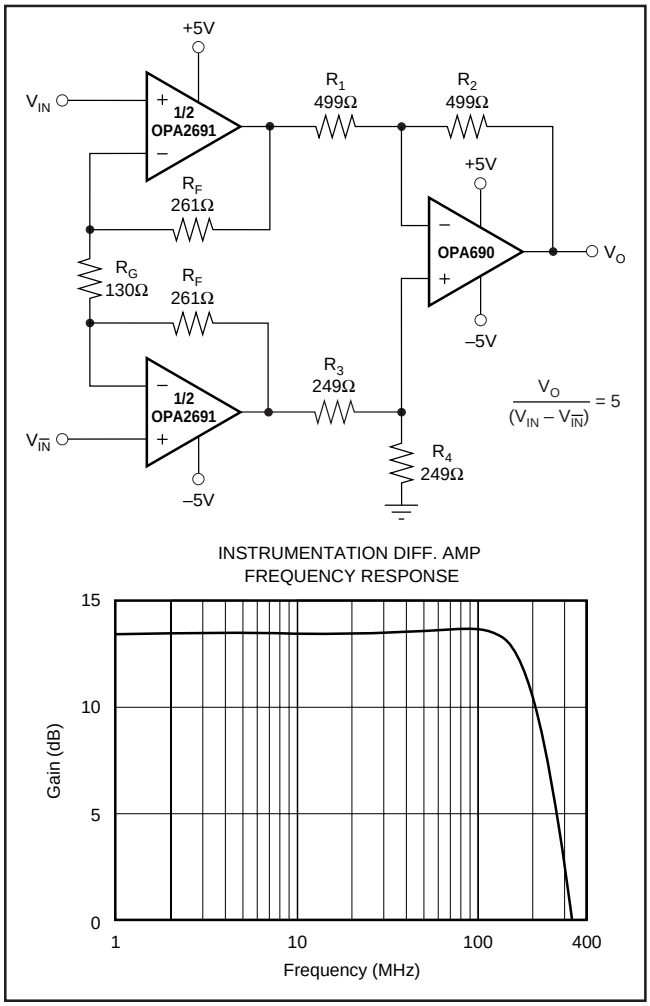


FIGURE 6. Wideband, 3-Op Amp Instrumentation Diff. Amp.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2691 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown Table I below.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2691ID	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2691I-14D	SO-14	DEM-OPA-SO-2B	SBOU002

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2691 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2691 is available through the TI web site (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance, nor do they attempt to simulate channel-to-channel coupling.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

A current-feedback op amp like the OPA2691 can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This is shown in the Typical Characteristics; the small-signal bandwidth decreases only slightly with increasing gain. Those curves also show that the feedback resistor has been changed for each gain setting. The resistor *values* on the inverting side of the circuit for a current-feedback op amp can be treated as frequency response compensation elements while their *ratios* set the signal gain. Figure 7 shows the small-signal frequency response analysis circuit for the OPA2691.

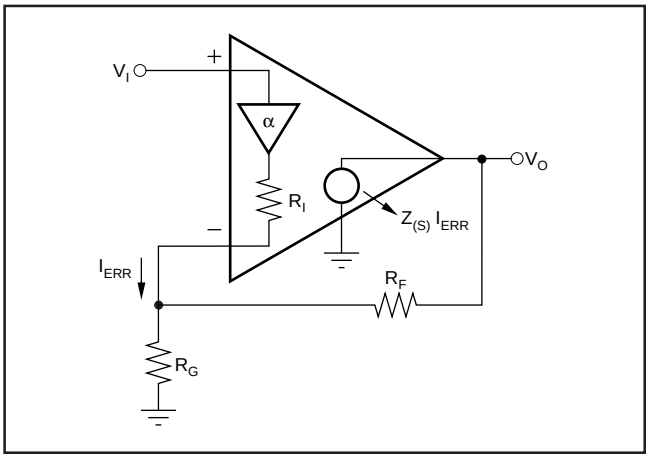


FIGURE 7. Current-Feedback Transfer Function Analysis Circuit.

The key elements of this current-feedback op amp model are:

$\alpha \rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \rightarrow$ Buffer output impedance

$i_{ERR} \rightarrow$ Feedback error current signal

$Z(s) \rightarrow$ Frequency dependent open-loop transimpedance gain from i_{ERR} to V_O

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For a buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log(1 - \alpha)$dB. R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2691 is typically about 37Ω.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency-dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 7 gives Equation 1:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1+\frac{R_F + R_I NG}{Z_{(S)}}} \quad (1)$$

$$\left[NG \equiv \left(1+\frac{R_F}{R_G}\right)\right]$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If $Z_{(S)}$ were infinite over all frequencies, the denominator of Equation 1 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 1 determines the frequency response. Equation 2 shows this as the loop-gain equation:

$$\frac{Z_{(S)}}{R_F + R_I NG} = \text{Loop Gain} \quad (2)$$

If $20 \cdot \log(R_F + NG \cdot R_I)$ were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, $Z_{(S)}$ rolls off to equal the denominator of Equation 2 at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier's closed-loop frequency response given by Equation 1 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 2 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA2691 is internally compensated to give a maximally flat frequency response for R_F = 402Ω at NG = 2 on ±5V supplies. Evaluating the denominator of Equation 2 (which is the feedback transimpedance) gives an optimal target of 476Ω. As the signal gain changes, the contribution of the $NG \cdot R_I$ term in the feedback transimpedance will change, but the total can be held constant by adjusting R_F. Equation 3 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 476\Omega - NG\,R_I \quad (3)$$

As the desired signal gain increases, this equation will eventually predict a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values will load both the buffer stage at the input and the output stage if R_F gets too low—actually decreasing

the bandwidth. Figure 8 shows the recommended R_F versus NG for both ±5V and a single +5V operation. The values for R_F versus Gain shown here are approximately equal to the values used to generate the Typical Characteristics. They differ in that the optimized values used in the Typical Characteristics are also correcting for board parasitics not considered in the simplified analysis leading to Equation 3. The values shown in Figure 8 give a good starting point for design where bandwidth optimization is desired.

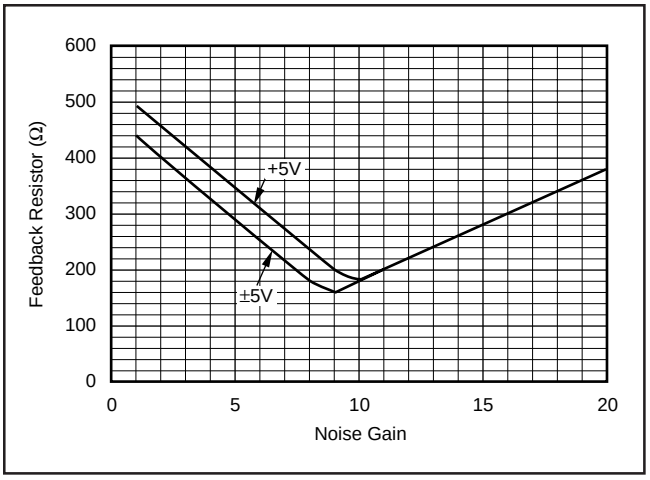


FIGURE 8. Recommended Feedback Resistor vs Noise Gain.

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction will increase the feedback impedance (denominator of Equation 2), decreasing the bandwidth. The internal buffer output impedance for the OPA2691 is slightly influenced by the source impedance looking out of the noninverting input terminal. High source resistors will have the effect of increasing R_I, decreasing the bandwidth. For those single-supply applications which develop a midpoint bias at the noninverting input through high valued resistors, the decoupling capacitor is essential for power-supply ripple rejection, noninverting input noise current shunting, and to minimize the high-frequency value for R_I in Figure 7.

INVERTING AMPLIFIER OPERATION

Since the OPA2691 is a general-purpose, wideband current-feedback op amp, most of the familiar op amp application circuits are available to the designer. Those dual op amp applications that require considerable flexibility in the feedback element (for example, integrators, transimpedance, and some filters) should consider the unity-gain stable voltage-feedback OPA2690, since the feedback resistor is the compensation element for a current-feedback op amp. Wideband inverting operation (and especially summing) is particularly suited to the OPA2691. Figure 9 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

In the inverting configuration, two key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input

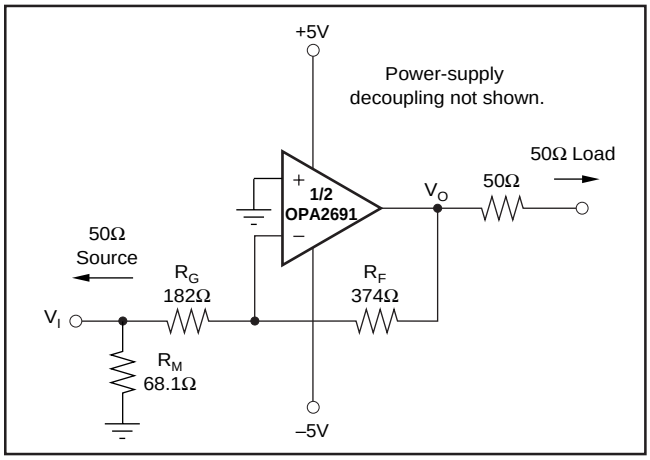


FIGURE 9. Inverting Gain of –2 with Impedance Matching.

impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PCB trace, or other transmission line conductor), it is normally necessary to add an additional matching resistor to ground. R_G by itself is normally not set to the required input impedance since its value, along with the desired gain, will determine an R_F which may be non-optimal from a frequency response standpoint. The total input impedance for the source becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and will have slight effect on the bandwidth through Equation 1. The values shown in Figure 9 have accounted for this by slightly decreasing R_F (from Figure 1) to re-optimize the bandwidth for the noise gain of Figure 9 (NG = 2.74) In the example of Figure 9, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 68Ω = 28.8Ω. This impedance is added in series with R_G for calculating the noise gain—which gives NG = 2.74. This value, along with the R_F of Figure 8 and the inverting input impedance of 37Ω, are inserted into Equation 3 to get a feedback transimpedance nearly equal to the 476Ω optimum value.

Note that the noninverting input in this bipolar supply inverting application is connected directly to ground. It is often suggested that an additional resistor be connected to ground on the noninverting input to achieve bias current error cancellation at the output. The input bias currents for a current-feedback op amp are not generally matched in either magnitude or polarity. Connecting a resistor to ground on the noninverting input of the OPA2691 in the circuit of Figure 9 will actually provide additional gain for that input's bias and noise currents, but will not decrease the output DC error since the input bias currents are not matched.

OUTPUT CURRENT AND VOLTAGE

The OPA2691 provides output voltage and current capabilities that are unsurpassed in a low-cost, dual monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; the tested

swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±160mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage x current, or V-I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2691's output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation (in this case for 1 channel only). Superimposing resistor load lines onto the plot shows that the OPA2691 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability, as shown in the Electrical Characteristics.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold start-up will the output current and voltage decrease to the numbers shown in the electrical characteristic tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To protect the output stage from accidental shorts to ground and the power supplies, output short-circuit protection is included in the OPA2691. The circuit acts to limit the maximum source or sink current to approximately 250mA.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve the ADC's linearity. A high-speed, high open-loop gain amplifier like the OPA2691 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended *R_S vs Capacitive Load* and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2691. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2691 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA2691 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2x rate while the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd-harmonic decreases less than the expected 6dB while the difference between it and the 3rd-harmonic decreases by less than the expected 12dB. This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (i.e., 2Vp-p for each tone at the load, which requires 8Vp-p for the overall 2-tone envelope at the output pin), the Typical Characteristics show 48dBc difference between the test-tone power and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2691 offers an excellent balance between voltage and

current noise terms to achieve low output noise. The inverting current noise (15pA/√Hz) is significantly lower than earlier solutions while the input voltage noise (1.7nV/√Hz) is lower than most unity-gain stable, wideband, voltage-feedback op amps. This low input voltage noise was achieved at the price of higher noninverting input current noise (12pA/√Hz). As long as the AC source impedance looking out of the noninverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 10 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

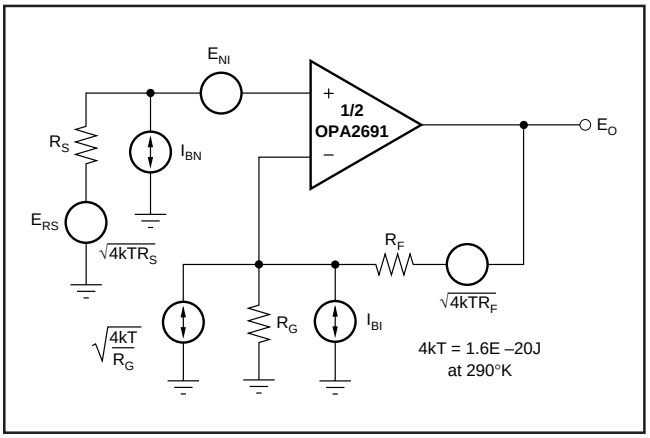


FIGURE 10. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 4 shows the general form for the output noise voltage using the terms shown in Figure 10.

(4)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_F NG}$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 5.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (5)$$

Evaluating these two equations for the OPA2691 circuit and component values presented in Figure 1 will give a total output spot noise voltage of 8.08nV/√Hz and a total equivalent input spot noise voltage of 4.04nV/√Hz. This total input referred spot noise voltage is higher than the 1.7nV/√Hz specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations (as suggested previously), the total input referred voltage noise given by Equation 5 will approach just the 1.7nV/√Hz of the op amp itself. For example, going to a gain of +10 using R_F = 180Ω will give a total input referred noise of 2.1nV/√Hz.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA2691 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm$ (NG • $V_{OS(MAX)}$) + (I_{BN} • R_S/2 • NG) $\pm$ (I_{BI} • R_F)

where NG = noninverting signal gain

= $\pm$ (2 • 3.0mV) + (35µA • 25Ω • 2) $\pm$ (402Ω • 25µA)

= ±6mV + 1.75mV ± 10.05mV

= –14.3mV → +17.8mV

DISABLE OPERATION (SO-14 ONLY)

The OPA2691I-14D provides an optional disable feature that may be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is left unconnected, the OPA2691I-14D will operate normally. To disable, the control pin must be asserted low. Figure 11 shows a simplified internal circuit for the disable control feature.

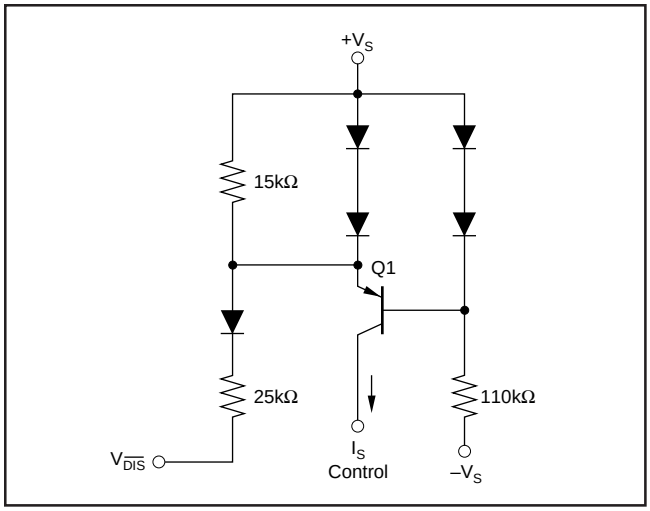


FIGURE 11. Simplified Disable Control Circuit, Each Channel.

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled low, additional current is pulled through the 15kΩ resistor, eventually turning on these two diodes (≈ 100µA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes

holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply currents in the disable mode are only those required to operate the circuit of Figure 11. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high impedance state. If the OPA2691 is operating in a gain of +1, this will show a very high impedance (4pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode. Figure 12 shows these glitches for the circuit of Figure 1 with the input signal set to 0V. The glitch waveform at the output pin is plotted along with the $\overline{DIS}$ pin voltage.

The transition edge rate (dv/dt) of the $\overline{DIS}$ control line will influence this glitch. For the plot of Figure 12, the edge rate was reduced until no further reduction in glitch amplitude was observed. This approximately 1V/ns maximum slew rate may be achieved by adding a simple RC filter into the $V_{\overline{DIS}}$ pin from a higher speed logic line. If extremely fast transition logic is used, a 2kΩ series resistor between the logic gate and the $V_{\overline{DIS}}$ input pin will provide adequate bandlimiting using just the parasitic input capacitance on the $V_{\overline{DIS}}$ pin while still ensuring adequate logic level swing.

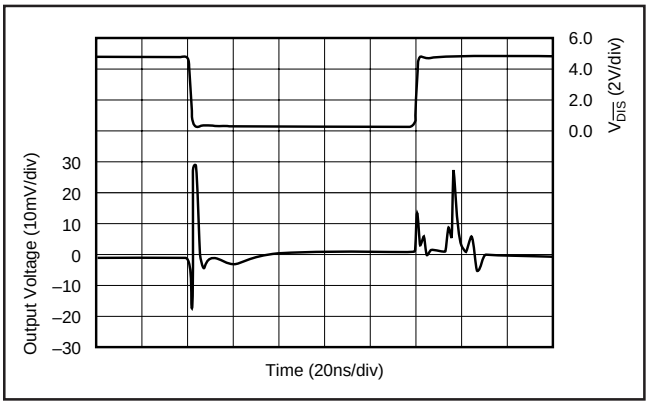


FIGURE 12. Disable/Enable Glitch.

THERMAL ANALYSIS

Due to the high output power capability of the OPA2691, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C. Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2691 SO-8 in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with both outputs driving a grounded 20Ω load to +2.5V.

$P_D = 10V \bullet 11.5mA + 2 \bullet [5^2/(4 \bullet (20\Omega \parallel 804\Omega))] = 756mW$

Maximum $T_J = +85°C + (0.756 \bullet 125°C/W) = 179.5°C$

This absolute worst-case condition exceeds specified maximum junction temperature. Normally this extreme case will not be encountered. Careful attention to internal power dissipation is required.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2691 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2691. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as

short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the bandwidth, while decreasing it will give a more peaked frequency response. The 402Ω feedback resistor used in the electrical characteristics at a gain of +2 on ±5V supplies is a good starting point for design. Note that a 453Ω feedback resistor, rather than a direct short, is recommended for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA2691 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the *Distortion vs Load* plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2691 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2691 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2691 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2691 onto the board.

INPUT AND ESD PROTECTION

The OPA2691 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 13.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2691), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

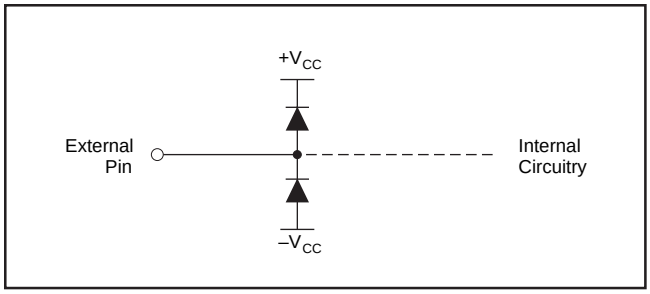


FIGURE 12. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
7/08	D	2	Abs Max Ratings	Changed Storage Temperature Range from –40°C to +125C to –65°C to +125C.
		3, 4	Electrical Characteristics, Power Supply	Added minimum supply voltage.
2/07	C	8	Typical Characteristics	Changed *Closed-Loop Output Impedance vs Frequency* plot.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2691I-14D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA2691
OPA2691I-14D.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA2691
OPA2691I-14DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA2691
OPA2691I-14DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA2691
OPA2691ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2691
OPA2691ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2691
OPA2691IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2691
OPA2691IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2691

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

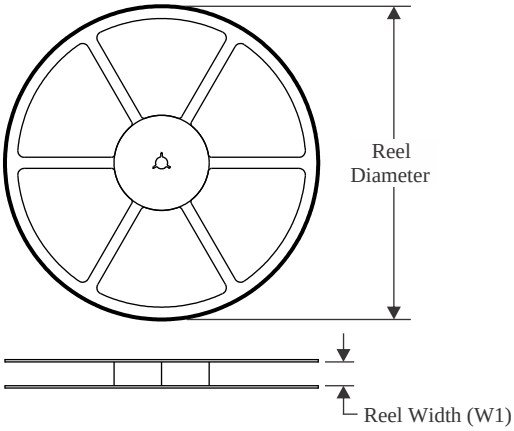
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

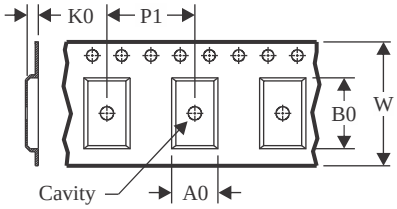
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

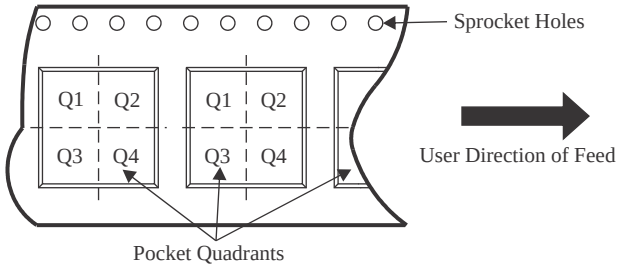


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

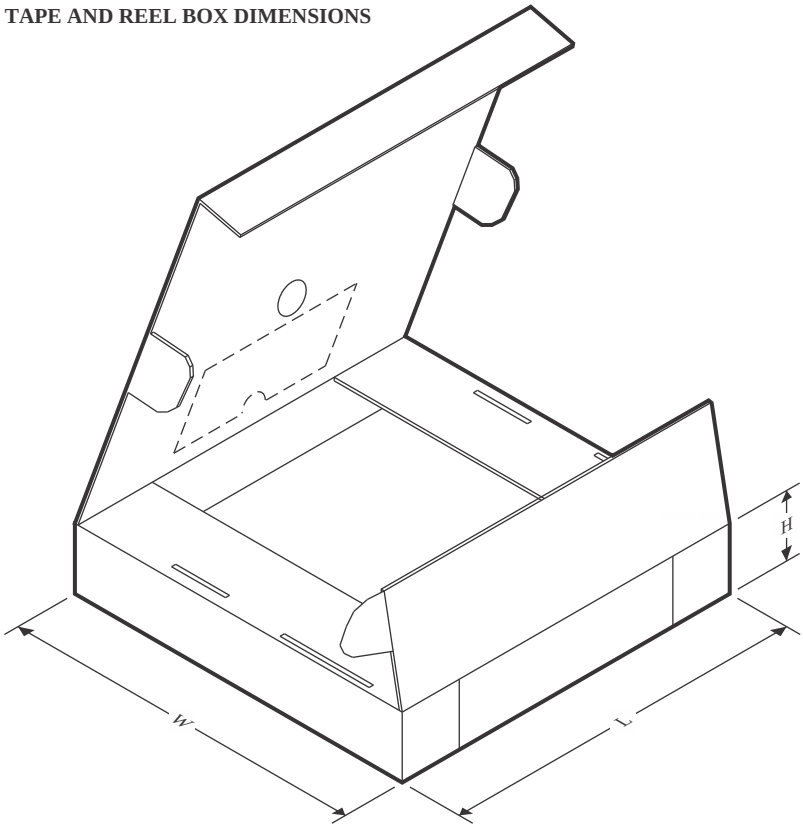
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2691I-14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA2691IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

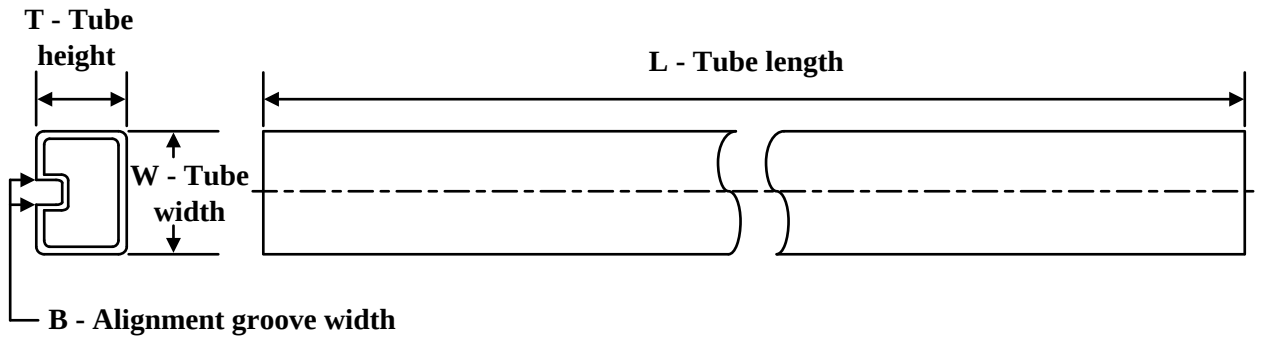
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

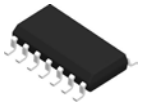
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2691I-14DR	SOIC	D	14	2500	356.0	356.0	35.0
OPA2691IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2691I-14D	D	SOIC	14	50	506.6	8	3940	4.32
OPA2691I-14D.A	D	SOIC	14	50	506.6	8	3940	4.32
OPA2691ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2691ID.A	D	SOIC	8	75	506.6	8	3940	4.32

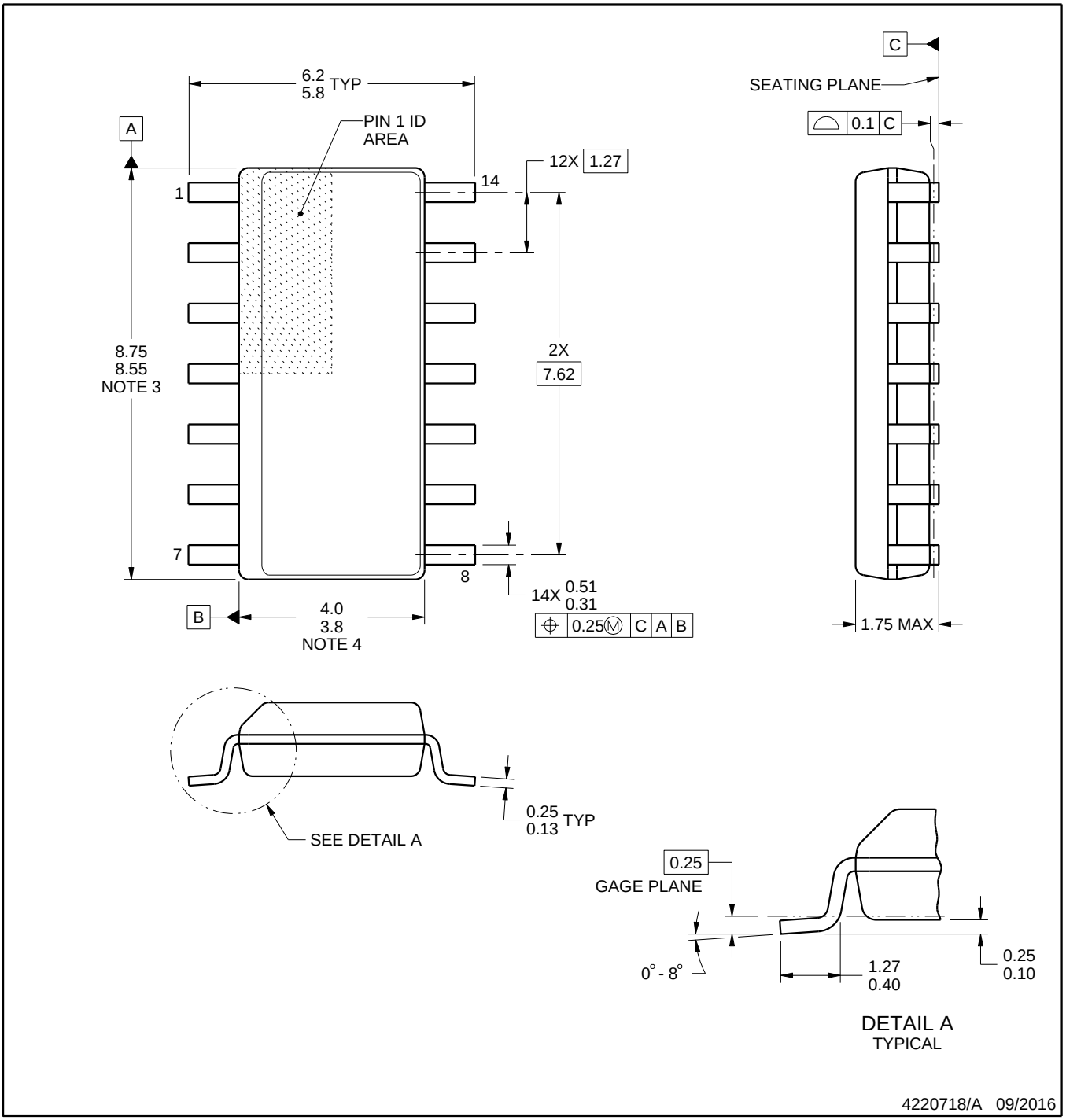


PACKAGE OUTLINE

D0014A

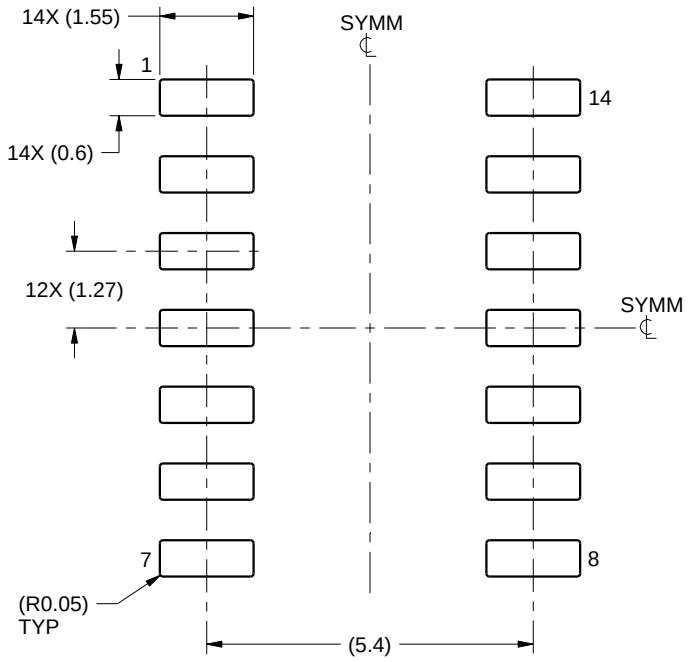
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

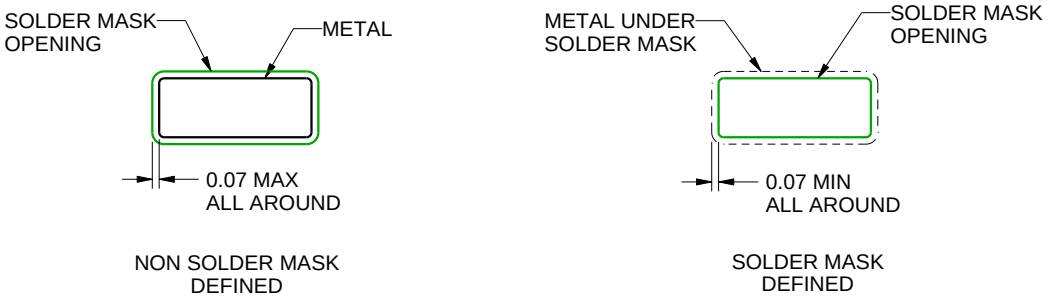


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

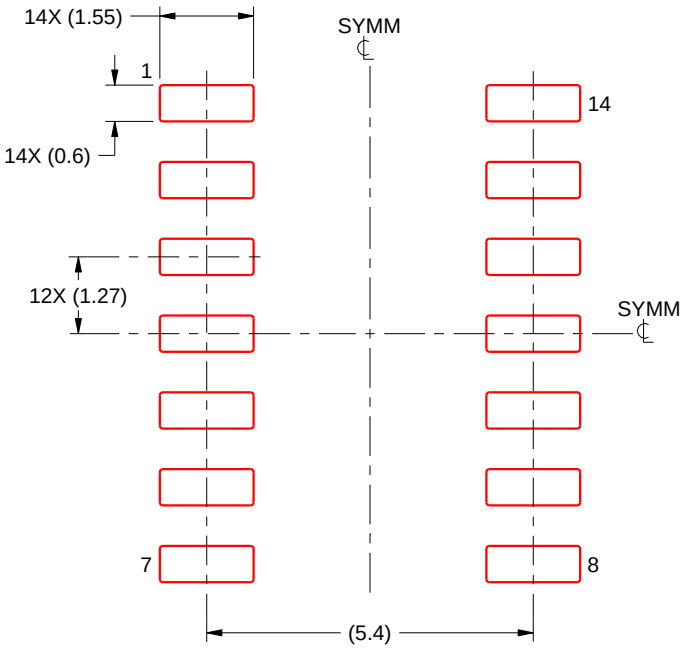
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

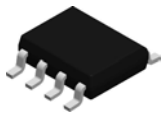


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

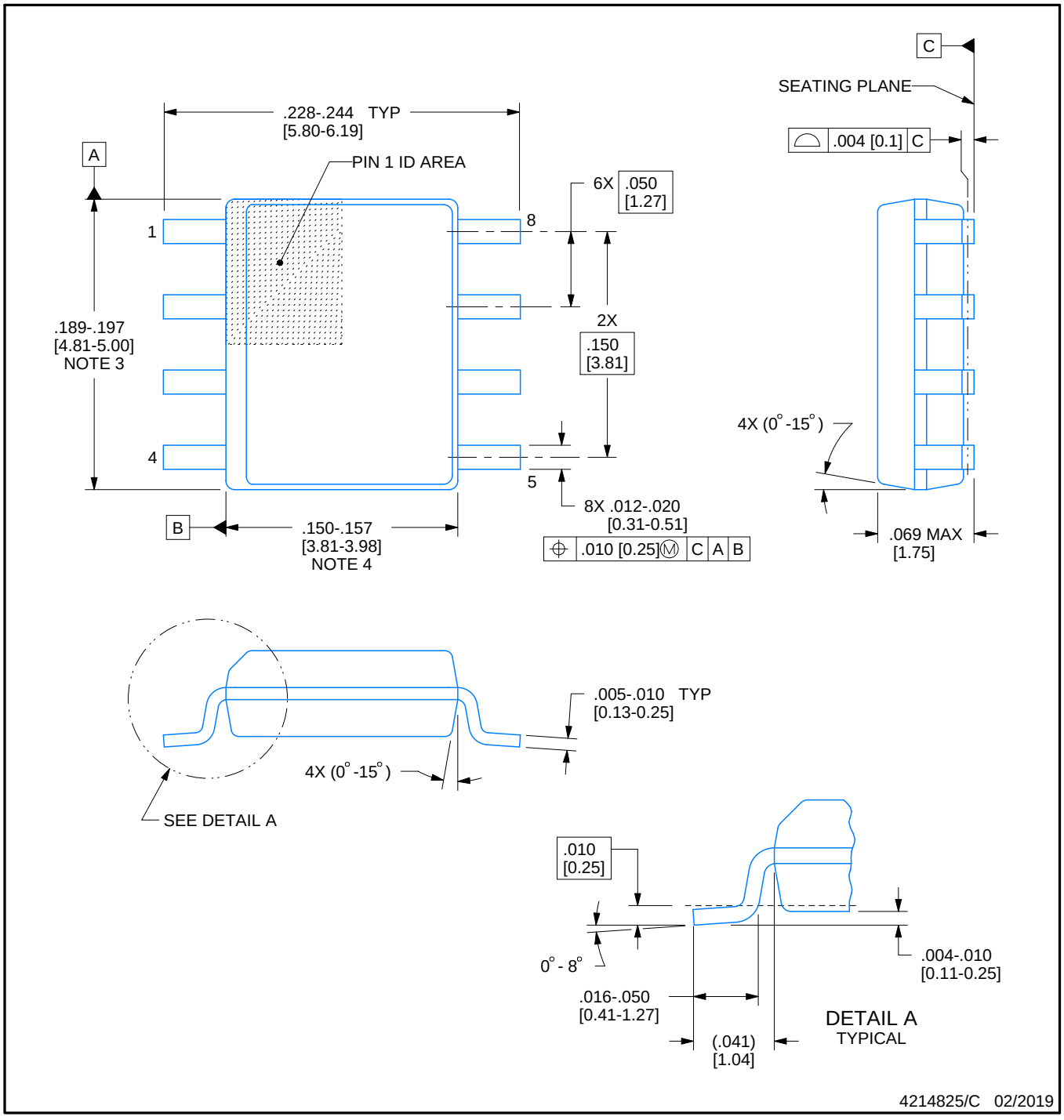


PACKAGE OUTLINE

D0008A

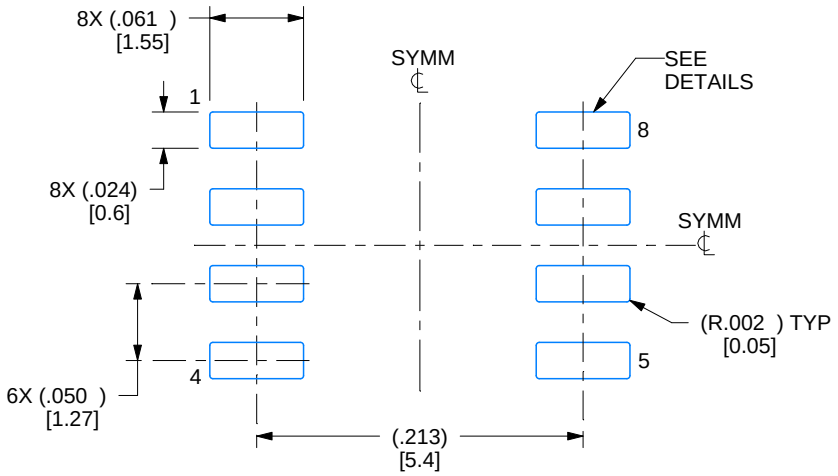
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

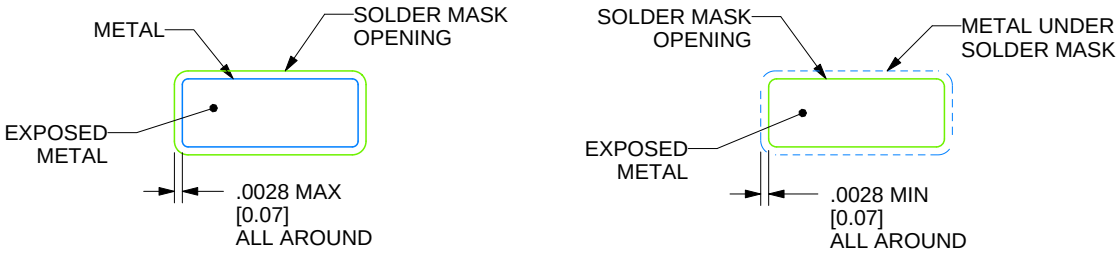


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

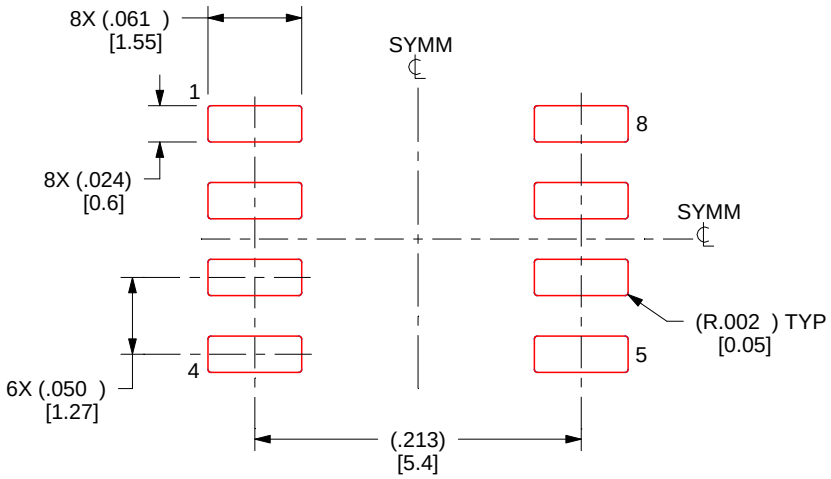
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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