



# MSP430G2231 Automotive Mixed-Signal Microcontroller

## 1 Features

- Qualified for Automotive Applications
- Low Supply-Voltage Range: 1.8 V to 3.6 V
- Ultra-Low-Power Consumption
  - Active Mode: 220  $\mu$ A at 1 MHz, 2.2 V
  - Standby Mode: 0.5  $\mu$ A
  - Off Mode (RAM Retention): 0.1  $\mu$ A
- Five Power-Saving Modes
- Ultra-Fast Wakeup From Standby Mode in Less Than 1  $\mu$ s
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With One Calibrated Frequency
  - Internal Very Low Power Low-Frequency (LF) Oscillator
  - 32-kHz Crystal
  - External Digital Clock Source
- 16-Bit Timer\_A With Two Capture/Compare Registers
- Universal Serial Interface (USI) Supports SPI and I<sup>2</sup>C
- Brownout Detector
- 10-Bit 200-ksps Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold, and Autoscan
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- On-Chip Emulation Logic With Spy-Bi-Wire Interface
- For Family Members Details, See [Device Characteristics](#)
- Available Packages
  - 14-Pin Plastic Small-Outline Thin Package (TSSOP) (PW)
  - 16-Pin QFN Package (RSA)
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide (SLAU144)*

## 2 Applications

- Low-Cost Sensor Systems

## 3 Description

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1  $\mu$ s.

The MSP430G2231 devices are ultra-low-power mixed signal microcontrollers with a built-in 16-bit timer and ten I/O pins. The MSP430G2231 devices have a 10-bit A/D converter and built-in communication capability using synchronous protocols (SPI or I2C). For configuration details, see [Table 1](#).

Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

**Device Information<sup>(1)</sup>**

| ORDER NUMBER       | PACKAGE (PIN) | BODY SIZE     |
|--------------------|---------------|---------------|
| MSP430G2231IRSARQ1 | RSA (16)      | 4 mm x 4 mm   |
| MSP430G2231IPW4RQ1 | PW (14)       | 5 mm x 4.4 mm |

(1) For the most current part, package, and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).



## 4 Functional Block Diagram

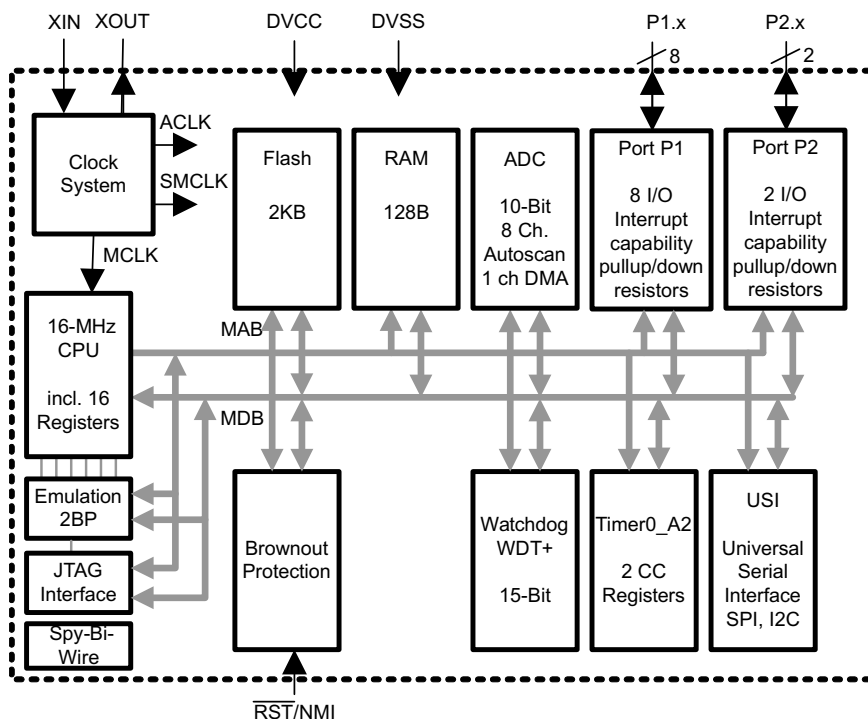


**Figure 1. Functional Block Diagram**

## Table of Contents

|                                                                                |           |                                                                             |           |
|--------------------------------------------------------------------------------|-----------|-----------------------------------------------------------------------------|-----------|
| <b>1 Features</b>                                                              | <b>1</b>  | 9.18 Crystal Oscillator, Xt1, Low-Frequency Mode                            | 25        |
| <b>2 Applications</b>                                                          | <b>1</b>  | 9.19 Internal Very-Low-Power Low-Frequency Oscillator (VLO)                 | 25        |
| <b>3 Description</b>                                                           | <b>1</b>  | 9.20 Timer_A                                                                | 25        |
| <b>4 Functional Block Diagram</b>                                              | <b>2</b>  | 9.21 USI, Universal Serial Interface                                        | 26        |
| <b>5 Revision History</b>                                                      | <b>4</b>  | 9.22 Typical Characteristics – USI Low-Level Output Voltage On SDA and SCL  | 26        |
| <b>6 Device Characteristics</b>                                                | <b>4</b>  | 9.23 10-Bit ADC, Power Supply and Input Range Conditions                    | 27        |
| <b>7 Terminal Configuration and Functions</b>                                  | <b>5</b>  | 9.24 10-Bit ADC, Built-In Voltage Reference                                 | 28        |
| 7.1 14-Pin PW Package (Top View)                                               | 5         | 9.25 10-Bit ADC, External Reference                                         | 29        |
| 7.2 16-Pin RSA Package (Top View)                                              | 5         | 9.26 10-Bit ADC, Timing Parameters                                          | 29        |
| 7.3 Terminal Functions                                                         | 6         | 9.27 10-Bit ADC, Linearity Parameters                                       | 29        |
| <b>8 Detailed Description</b>                                                  | <b>7</b>  | 9.28 10-Bit ADC, Temperature Sensor and Built-In $V_{MID}$                  | 30        |
| 8.1 CPU                                                                        | 7         | 9.29 Flash Memory                                                           | 30        |
| 8.2 Instruction Set                                                            | 7         | 9.30 RAM                                                                    | 31        |
| 8.3 Operating Modes                                                            | 8         | 9.31 JTAG and Spy-Bi-Wire Interface                                         | 31        |
| 8.4 Interrupt Vector Addresses                                                 | 9         | 9.32 JTAG Fuse                                                              | 31        |
| 8.5 Special Function Registers (SFRs)                                          | 10        | <b>10 I/O Port Schematics</b>                                               | <b>32</b> |
| 8.6 Memory Organization                                                        | 11        | 10.1 Port P1 Pin Schematic: P1.0 To P1.2, Input/Output With Schmitt Trigger | 32        |
| 8.7 Flash Memory                                                               | 11        | 10.2 Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger         | 34        |
| 8.8 Peripherals                                                                | 12        | 10.3 Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger         | 35        |
| <b>9 Specifications</b>                                                        | <b>16</b> | 10.4 Port P1 Pin Schematic: P1.5, Input/Output With Schmitt Trigger         | 36        |
| 9.1 Absolute Maximum Ratings                                                   | 16        | 10.5 Port P1 Pin Schematic: P1.6, Input/Output With Schmitt Trigger         | 37        |
| 9.2 Recommended Operating Conditions                                           | 16        | 10.6 Port P1 Pin Schematic: P1.7, Input/Output With Schmitt Trigger         | 38        |
| 9.3 Active Mode Supply Current Into $V_{CC}$ Excluding External Current        | 17        | 10.7 Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger         | 39        |
| 9.4 Typical Characteristics – Active Mode Supply Current (Into $V_{CC}$ )      | 17        | 10.8 Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger         | 40        |
| 9.5 Low-Power Mode Supply Currents (Into $V_{CC}$ ) Excluding External Current | 18        | <b>11 Device and Documentation Support</b>                                  | <b>41</b> |
| 9.6 Typical Characteristics, Low-Power Mode Supply Currents                    | 18        | 11.1 Device Support                                                         | 41        |
| 9.7 Schmitt-Trigger Inputs – Ports Px                                          | 19        | 11.2 Documentation Support                                                  | 43        |
| 9.8 Leakage Current – Ports Px                                                 | 19        | 11.3 Community Resources                                                    | 43        |
| 9.9 Outputs – Ports Px                                                         | 19        | 11.4 Trademarks                                                             | 44        |
| 9.10 Output Frequency – Ports Px                                               | 19        | 11.5 Electrostatic Discharge Caution                                        | 44        |
| 9.11 Typical Characteristics – Outputs                                         | 20        | 11.6 Glossary                                                               | 44        |
| 9.12 POR, BOR                                                                  | 21        | <b>12 Mechanical, Packaging, and Orderable Information</b>                  | <b>44</b> |
| 9.13 Main DCO Characteristics                                                  | 23        |                                                                             |           |
| 9.14 DCO Frequency                                                             | 23        |                                                                             |           |
| 9.15 Calibrated DCO Frequencies – Tolerance                                    | 24        |                                                                             |           |
| 9.16 Wakeup From Lower-Power Modes (LPM3, LPM4) – Electrical Characteristics   | 24        |                                                                             |           |
| 9.17 Typical Characteristics – DCO Clock Wakeup Time From LPM3, LPM4           | 24        |                                                                             |           |

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| REVISION | DESCRIPTION                                                                                                                                                                                                                                                                                                |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SLAS787  | Product Preview release                                                                                                                                                                                                                                                                                    |
| SLAS787A | Production Data release                                                                                                                                                                                                                                                                                    |
| SLAS787B | Formatting and document organization changes throughout.<br>Removed all information related to operation at 105°C.<br>Removed all device variants except for MSP430G2231.<br>Added <a href="#">Device and Documentation Support</a> and <a href="#">Mechanical, Packaging, and Orderable Information</a> . |

## 6 Device Characteristics

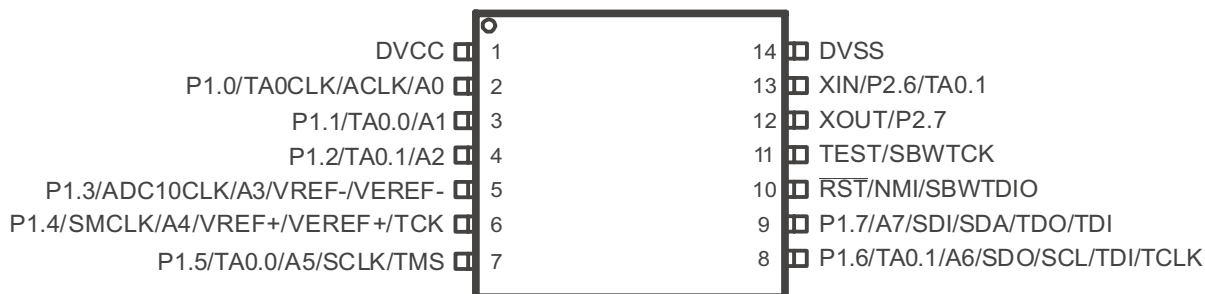
[Table 1](#) shows the features of the MSP430G2231 device.

**Table 1. Family Members**

| Device      | BSL | EEM | Flash (KB) | RAM (B) | Timer_A | USI | ADC10 Channel | Clock        | I/O | Package Type       |
|-------------|-----|-----|------------|---------|---------|-----|---------------|--------------|-----|--------------------|
| MSP430G2231 | -   | 1   | 2          | 128     | 1x TA2  | 1   | 8             | LF, DCO, VLO | 10  | 16-QFN<br>14-TSSOP |

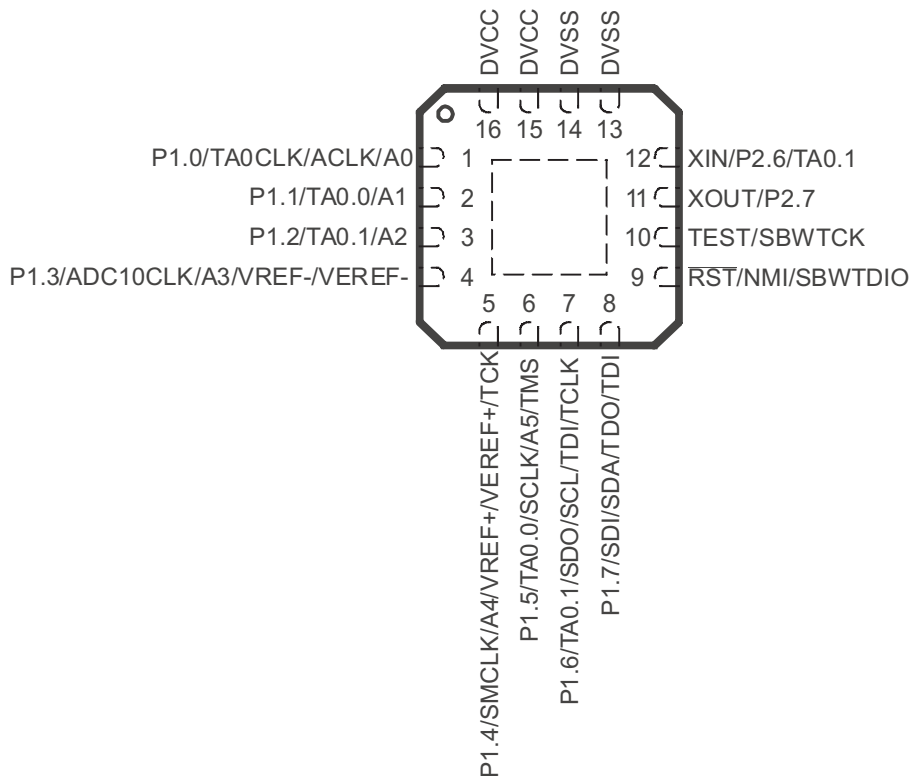
## 7 Terminal Configuration and Functions

### 7.1 14-Pin PW Package (Top View)



NOTE: See port schematics in [I/O Port Schematics](#) for detailed I/O information.

### 7.2 16-Pin RSA Package (Top View)



NOTE: See port schematics in [I/O Port Schematics](#) for detailed I/O information.

## 7.3 Terminal Functions

**Table 2. Terminal Functions**

| TERMINAL                                               |     |        | I/O | DESCRIPTION                                                                                                                                                                                                                                            |
|--------------------------------------------------------|-----|--------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                                   | NO. |        |     |                                                                                                                                                                                                                                                        |
|                                                        | PW  | RSA    |     |                                                                                                                                                                                                                                                        |
| P1.0/<br>TA0CLK/<br>ACLK/<br>A0                        | 2   | 1      | I/O | General-purpose digital I/O pin<br>Timer0_A, clock signal TACLK input<br>ACLK signal output<br>ADC10 analog input A0                                                                                                                                   |
| P1.1/<br>TA0.0/<br>A1                                  | 3   | 2      | I/O | General-purpose digital I/O pin<br>Timer0_A, capture: CCI0A input, compare: Out0 output<br>ADC10 analog input A1                                                                                                                                       |
| P1.2/<br>TA0.1/<br>A2                                  | 4   | 3      | I/O | General-purpose digital I/O pin<br>Timer0_A, capture: CCI1A input, compare: Out1 output<br>ADC10 analog input A2                                                                                                                                       |
| P1.3/<br>ADC10CLK/<br>A3/<br>VREF-/VEREF               | 5   | 4      | I/O | General-purpose digital I/O pin<br>ADC10, conversion clock output<br>ADC10 analog input A3<br>ADC10 negative reference voltage                                                                                                                         |
| P1.4/<br>SMCLK/<br>A4/<br>VREF+/VEREF+/<br>TCK         | 6   | 5      | I/O | General-purpose digital I/O pin<br>SMCLK signal output<br>ADC10 analog input A4<br>ADC10 positive reference voltage<br>JTAG test clock, input terminal for device programming and test                                                                 |
| P1.5/<br>TA0.0/<br>A5/<br>SCLK/<br>TMS                 | 7   | 6      | I/O | General-purpose digital I/O pin<br>Timer0_A, compare: Out0 output<br>ADC10 analog input A5<br>USI: clock input in I2C mode; clock input/output in SPI mode<br>JTAG test mode select, input terminal for device programming and test                    |
| P1.6/<br>TA0.1/<br>A6/<br>SDO/<br>SCL/<br>TDI/TCLK     | 8   | 7      | I/O | General-purpose digital I/O pin<br>Timer0_A, capture: CCI1A input, compare: Out1 output<br>ADC10 analog input A6<br>USI: Data output in SPI mode<br>USI: I2C clock in I2C mode<br>JTAG test data input or test clock input during programming and test |
| P1.7/<br>A7/<br>SDI/<br>SDA/<br>TDO/TDI <sup>(1)</sup> | 9   | 8      | I/O | General-purpose digital I/O pin<br>ADC10 analog input A7<br>USI: Data input in SPI mode<br>USI: I2C data in I2C mode<br>JTAG test data output terminal or test data input during programming and test                                                  |
| XIN/<br>P2.6/<br>TA0.1                                 | 13  | 12     | I/O | Input terminal of crystal oscillator<br>General-purpose digital I/O pin<br>Timer0_A, compare: Out1 output                                                                                                                                              |
| XOUT/<br>P2.7                                          | 12  | 11     | I/O | Output terminal of crystal oscillator <sup>(2)</sup><br>General-purpose digital I/O pin                                                                                                                                                                |
| RST/<br>NMI/<br>SBWTDIO                                | 10  | 9      | I   | Reset<br>Nonmaskable interrupt input<br>Spy-Bi-Wire test data input/output during programming and test                                                                                                                                                 |
| TEST/<br>SBWTCK                                        | 11  | 10     | I   | Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST.<br>Spy-Bi-Wire test clock input during programming and test                                                                                                |
| DVCC                                                   | 1   | 15, 16 | NA  | Supply voltage                                                                                                                                                                                                                                         |
| DVSS                                                   | 14  | 13, 14 | NA  | Ground reference                                                                                                                                                                                                                                       |
| QFN Pad                                                | -   | Pad    | NA  | QFN package pad connection to V <sub>SS</sub> recommended.                                                                                                                                                                                             |

(1) TDO or TDI is selected via JTAG instruction.

(2) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

## 8 Detailed Description

### 8.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

### 8.2 Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 3](#) shows examples of the three types of instruction formats, and [Table 4](#) shows the address modes.

### Instruction Set (continued)

|                          |           |
|--------------------------|-----------|
| Program Counter          | PC/R0     |
| Stack Pointer            | SP/R1     |
| Status Register          | SR/CG1/R2 |
| Constant Generator       | CG2/R3    |
| General-Purpose Register | R4        |
| General-Purpose Register | R5        |
| General-Purpose Register | R6        |
| General-Purpose Register | R7        |
| General-Purpose Register | R8        |
| General-Purpose Register | R9        |
| General-Purpose Register | R10       |
| General-Purpose Register | R11       |
| General-Purpose Register | R12       |
| General-Purpose Register | R13       |
| General-Purpose Register | R14       |
| General-Purpose Register | R15       |

**Table 3. Instruction Word Formats**

| INSTRUCTION FORMAT                | SYNTAX    | OPERATION             |
|-----------------------------------|-----------|-----------------------|
| Dual operands, source-destination | ADD R4,R5 | R4 + R5 --> R5        |
| Single operands, destination only | CALL R8   | PC -->(TOS), R8--> PC |
| Relative jump, un/conditional     | JNE       | Jump-on-equal bit = 0 |

**Table 4. Address Mode Descriptions<sup>(1)</sup>**

| ADDRESS MODE           | S | D | SYNTAX          | EXAMPLE          | OPERATION                              |
|------------------------|---|---|-----------------|------------------|----------------------------------------|
| Register               | ✓ | ✓ | MOV Rs,Rd       | MOV R10,R11      | R10 -- --> R11                         |
| Indexed                | ✓ | ✓ | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6)  | M(2+R5) -- --> M(6+R6)                 |
| Symbolic (PC relative) | ✓ | ✓ | MOV EDE,TONI    |                  | M(EDE) -- --> M(TONI)                  |
| Absolute               | ✓ | ✓ | MOV &MEM,&TCDAT |                  | M(MEM) -- --> M(TCDAT)                 |
| Indirect               | ✓ |   | MOV @Rn,Y(Rm)   | MOV @R10,Tab(R6) | M(R10) -- --> M(Tab+R6)                |
| Indirect autoincrement | ✓ |   | MOV @Rn+,Rm     | MOV @R10+,R11    | M(R10) -- --> R11<br>R10 + 2-- --> R10 |
| Immediate              | ✓ |   | MOV #X,TONI     | MOV #45,TONI     | #45 -- --> M(TONI)                     |

(1) S = source, D = destination

### 8.3 Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

## 8.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed) the CPU goes into LPM4 immediately after power-up.

**Table 5. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE                                                                                       | INTERRUPT FLAG                                    | SYSTEM INTERRUPT                                   | WORD ADDRESS     | PRIORITY        |
|--------------------------------------------------------------------------------------------------------|---------------------------------------------------|----------------------------------------------------|------------------|-----------------|
| Power-Up<br>External Reset<br>Watchdog Timer+<br>Flash key violation<br>PC out-of-range <sup>(1)</sup> | PORIFG<br>RSTIFG<br>WDTIFG<br>KEYV <sup>(2)</sup> | Reset                                              | 0FFFEh           | 31, highest     |
| NMI<br>Oscillator fault<br>Flash memory access violation                                               | NMIIFG<br>OFIFG<br>ACCVIFG <sup>(2)(3)</sup>      | (non)-maskable<br>(non)-maskable<br>(non)-maskable | 0FFFCCh          | 30              |
|                                                                                                        |                                                   |                                                    | 0FFFAh           | 29              |
|                                                                                                        |                                                   |                                                    | 0FFF8h           | 28              |
|                                                                                                        |                                                   |                                                    | 0FFF6h           | 27              |
| Watchdog Timer+                                                                                        | WDTIFG                                            | maskable                                           | 0FFF4h           | 26              |
| Timer_A2                                                                                               | TACCR0 CCIFG <sup>(4)</sup>                       | maskable                                           | 0FFF2h           | 25              |
| Timer_A2                                                                                               | TACCR1 CCIFG, TAIFG <sup>(2)(4)</sup>             | maskable                                           | 0FFF0h           | 24              |
|                                                                                                        |                                                   |                                                    | 0FFEEh           | 23              |
|                                                                                                        |                                                   |                                                    | 0FFECCh          | 22              |
| ADC10                                                                                                  | ADC10IFG <sup>(4)(5)</sup>                        | maskable                                           | 0FFEAh           | 21              |
| USI                                                                                                    | USIIFG, USISTTIFG <sup>(2)(4)</sup>               | maskable                                           | 0FFE8h           | 20              |
| I/O Port P2 (two flags)                                                                                | P2IFG.6 to P2IFG.7 <sup>(2)(4)</sup>              | maskable                                           | 0FFE6h           | 19              |
| I/O Port P1 (eight flags)                                                                              | P1IFG.0 to P1IFG.7 <sup>(2)(4)</sup>              | maskable                                           | 0FFE4h           | 18              |
|                                                                                                        |                                                   |                                                    | 0FFE2h           | 17              |
|                                                                                                        |                                                   |                                                    | 0FFE0h           | 16              |
| See <sup>(6)</sup>                                                                                     |                                                   |                                                    | 0FFDEh to 0FFC0h | 15 to 0, lowest |

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.

(2) Multiple source flags

(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.

(4) Interrupt flags are located in the module.

(5) MSP430G2x31 only

(6) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

## 8.5 Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

|               |                                                                                   |                                                         |
|---------------|-----------------------------------------------------------------------------------|---------------------------------------------------------|
| <b>Legend</b> | <b>rw:</b>                                                                        | Bit can be read and written.                            |
|               | <b>rw-0,1:</b>                                                                    | Bit can be read and written. It is reset or set by PUC. |
|               | <b>rw-(0,1):</b>                                                                  | Bit can be read and written. It is reset or set by POR. |
|               |  | SFR bit is not present in device.                       |

**Table 6. Interrupt Enable Register 1 and 2**

| Address | 7                                                                                 | 6                                                                                 | 5      | 4     | 3                                                                                  | 2                                                                                   | 1    | 0     |
|---------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|--------|-------|------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|------|-------|
| 00h     |  |  | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
|         |                                                                                   |                                                                                   | rw-0   | rw-0  |                                                                                    |                                                                                     | rw-0 | rw-0  |

**WDTIE** Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.  
**OFIE** Oscillator fault interrupt enable  
**NMIIE** (Non)maskable interrupt enable  
**ACCVIE** Flash access violation interrupt enable

| Address | 7                                                                                 | 6                                                                                 | 5                                                                                 | 4                                                                                 | 3                                                                                  | 2                                                                                   | 1                                                                                   | 0                                                                                   |
|---------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 01h     |  |  |  |  |  |  |  |  |

**Table 7. Interrupt Flag Register 1 and 2**

| Address | 7                                                                                   | 6                                                                                   | 5                                                                                   | 4      | 3      | 2      | 1     | 0      |
|---------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------|--------|--------|-------|--------|
| 02h     |  |  |  | NMIIFG | RSTIFG | PORIFG | OFIFG | WDTIFG |
|         |                                                                                     |                                                                                     |                                                                                     | rw-0   | rw-(0) | rw-(1) | rw-1  | rw-(0) |

**WDTIFG** Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V<sub>CC</sub> power-on or a reset condition at the RST/NMI pin in reset mode.  
**OFIFG** Flag set on oscillator fault.  
**PORIFG** Power-On Reset interrupt flag. Set on V<sub>CC</sub> power-up.  
**RSTIFG** External reset interrupt flag. Set on a reset condition at RST/NMI pin in reset mode. Reset on V<sub>CC</sub> power-up.  
**NMIIFG** Set via RST/NMI pin

| Address | 7                                                                                   | 6                                                                                   | 5                                                                                   | 4                                                                                   | 3                                                                                    | 2                                                                                     | 1                                                                                     | 0                                                                                     |
|---------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 03h     |  |  |  |  |  |  |  |  |

## 8.6 Memory Organization

**Table 8. Memory Organization**

|                                                       |                              | <b>MSP430G2231</b>                           |
|-------------------------------------------------------|------------------------------|----------------------------------------------|
| Memory<br>Main: interrupt vector<br>Main: code memory | Size<br>Flash<br>Flash       | 2KB<br>0xFFFF to 0xFFC0<br>0xFFFF to 0xF800  |
| Information memory                                    | Size<br>Flash                | 256 Byte<br>010FFh to 01000h                 |
| RAM                                                   | Size                         | 128B<br>027Fh to 0200h                       |
| Peripherals                                           | 16-bit<br>8-bit<br>8-bit SFR | 01FFh to 0100h<br>0FFh to 010h<br>0Fh to 00h |

## 8.7 Flash Memory

The flash memory can be programmed using the Spy-Bi-Wire or JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

## 8.8 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

### 8.8.1 Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 $\mu$ s. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

**Table 9. DCO Calibration Data (Provided From Factory In Flash Information Memory Segment A)**

| DCO FREQUENCY | CALIBRATION REGISTER | SIZE | ADDRESS |
|---------------|----------------------|------|---------|
| 1 MHz         | CALBC1_1MHZ          | byte | 010FFh  |
|               | CALDCO_1MHZ          | byte | 010FEh  |

### 8.8.2 Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

### 8.8.3 Digital I/O

There is one 8-bit I/O port implemented—port P1—and two bits of I/O port P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and the two bits of port P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pull-up/pull-down resistor.

### 8.8.4 WDT+ Watchdog Timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

### 8.8.5 Timer\_A2

Timer\_A2 is a 16-bit timer/counter with two capture/compare registers. Timer\_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer\_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 10. Timer\_A2 Signal Connections – Device With ADC10**

| INPUT PIN NUMBER |          | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |           |
|------------------|----------|---------------------|-------------------|--------------|----------------------|-------------------|-----------|
| PW               | RSA      |                     |                   |              |                      | PW                | RSA       |
| 2 - P1.0         | 1 - P1.0 | TACLK               | TACLK             | Timer        | NA                   |                   |           |
|                  |          | ACLK                | ACLK              |              |                      |                   |           |
|                  |          | SMCLK               | SMCLK             |              |                      |                   |           |
| 2 - P1.0         | 1 - P1.0 | TACLK               | INCLK             |              |                      |                   |           |
| 3 - P1.1         | 2 - P1.1 | TA0                 | CCI0A             | CCR0         | TA0                  | 3 - P1.1          | 2 - P1.1  |
|                  |          | ACLK (internal)     | CCI0B             |              |                      | 7 - P1.5          | 6 - P1.5  |
|                  |          | VSS                 | GND               |              |                      |                   |           |
|                  |          | VCC                 | VCC               |              |                      |                   |           |
| 4 - P1.2         | 3 - P1.2 | TA1                 | CCI1A             | CCR1         | TA1                  | 4 - P1.2          | 3 - P1.2  |
| 8 - P1.6         | 7 - P1.6 | TA1                 | CCI1B             |              |                      | 8 - P1.6          | 7 - P1.6  |
|                  |          | VSS                 | GND               |              |                      | 13 - P2.6         | 12 - P2.6 |
|                  |          | VCC                 | VCC               |              |                      |                   |           |

### 8.8.6 USI

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

### 8.8.7 ADC10

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

## 8.8.8 Peripheral File Map

**Table 11. Peripherals With Word Access**

| MODULE                 | REGISTER DESCRIPTION            | REGISTER NAME | OFFSET |
|------------------------|---------------------------------|---------------|--------|
| <b>ADC10</b>           | ADC data transfer start address | ADC10SA       | 1BCh   |
|                        | ADC control 0                   | ADC10CTL0     | 01B0h  |
|                        | ADC control 1                   | ADC10CTL0     | 01B2h  |
|                        | ADC memory                      | ADC10MEM      | 01B4h  |
| <b>Timer_A</b>         | Capture/compare register        | TACCR1        | 0174h  |
|                        | Capture/compare register        | TACCR0        | 0172h  |
|                        | Timer_A register                | TAR           | 0170h  |
|                        | Capture/compare control         | TACCTL1       | 0164h  |
|                        | Capture/compare control         | TACCTL0       | 0162h  |
|                        | Timer_A control                 | TACTL         | 0160h  |
|                        | Timer_A interrupt vector        | TAIV          | 012Eh  |
| <b>Flash Memory</b>    | Flash control 3                 | FCTL3         | 012Ch  |
|                        | Flash control 2                 | FCTL2         | 012Ah  |
|                        | Flash control 1                 | FCTL1         | 0128h  |
| <b>Watchdog Timer+</b> | Watchdog/timer control          | WDTCTL        | 0120h  |

**Table 12. Peripherals With Byte Access**

| MODULE                     | REGISTER DESCRIPTION          | REGISTER NAME | OFFSET |
|----------------------------|-------------------------------|---------------|--------|
| <b>ADC10</b>               | ADC analog enable             | ADC10AE0      | 04Ah   |
|                            | ADC data transfer control 1   | ADC10DTC1     | 049h   |
|                            | ADC data transfer control 0   | ADC10DTC0     | 048h   |
| <b>USI</b>                 | USI control 0                 | USICTL0       | 078h   |
|                            | USI control 1                 | USICTL1       | 079h   |
|                            | USI clock control             | USICKCTL      | 07Ah   |
|                            | USI bit counter               | USICNT        | 07Bh   |
|                            | USI shift register            | USISR         | 07Ch   |
| <b>Basic Clock System+</b> | Basic clock system control 3  | BCSCTL3       | 053h   |
|                            | Basic clock system control 2  | BCSCTL2       | 058h   |
|                            | Basic clock system control 1  | BCSCTL1       | 057h   |
|                            | DCO clock frequency control   | DCOCTL        | 056h   |
| <b>Port P2</b>             | Port P2 resistor enable       | P2REN         | 02Fh   |
|                            | Port P2 selection             | P2SEL         | 02Eh   |
|                            | Port P2 interrupt enable      | P2IE          | 02Dh   |
|                            | Port P2 interrupt edge select | P2IES         | 02Ch   |
|                            | Port P2 interrupt flag        | P2IFG         | 02Bh   |
|                            | Port P2 direction             | P2DIR         | 02Ah   |
|                            | Port P2 output                | P2OUT         | 029h   |
|                            | Port P2 input                 | P2IN          | 028h   |

**Table 12. Peripherals With Byte Access (continued)**

| MODULE                  | REGISTER DESCRIPTION          | REGISTER NAME | OFFSET |
|-------------------------|-------------------------------|---------------|--------|
| <b>Port P1</b>          | Port P1 resistor enable       | P1REN         | 027h   |
|                         | Port P1 selection             | P1SEL         | 026h   |
|                         | Port P1 interrupt enable      | P1IE          | 025h   |
|                         | Port P1 interrupt edge select | P1IES         | 024h   |
|                         | Port P1 interrupt flag        | P1IFG         | 023h   |
|                         | Port P1 direction             | P1DIR         | 022h   |
|                         | Port P1 output                | P1OUT         | 021h   |
|                         | Port P1 input                 | P1IN          | 020h   |
| <b>Special Function</b> | SFR interrupt flag 2          | IFG2          | 003h   |
|                         | SFR interrupt flag 1          | IFG1          | 002h   |
|                         | SFR interrupt enable 2        | IE2           | 001h   |
|                         | SFR interrupt enable 1        | IE1           | 000h   |

## 9 Specifications

### 9.1 Absolute Maximum Ratings <sup>(1)</sup>

|                                                     |                     |                            |
|-----------------------------------------------------|---------------------|----------------------------|
| Voltage applied at $V_{CC}$ to $V_{SS}$             |                     | –0.3 V to 4.1 V            |
| Voltage applied to any pin <sup>(2)</sup>           |                     | –0.3 V to $V_{CC} + 0.3$ V |
| Diode current at any device pin                     |                     | ±2 mA                      |
| Storage temperature range, $T_{stg}$ <sup>(3)</sup> | Unprogrammed device | –55°C to 150°C             |
|                                                     | Programmed device   | –55°C to 150°C             |

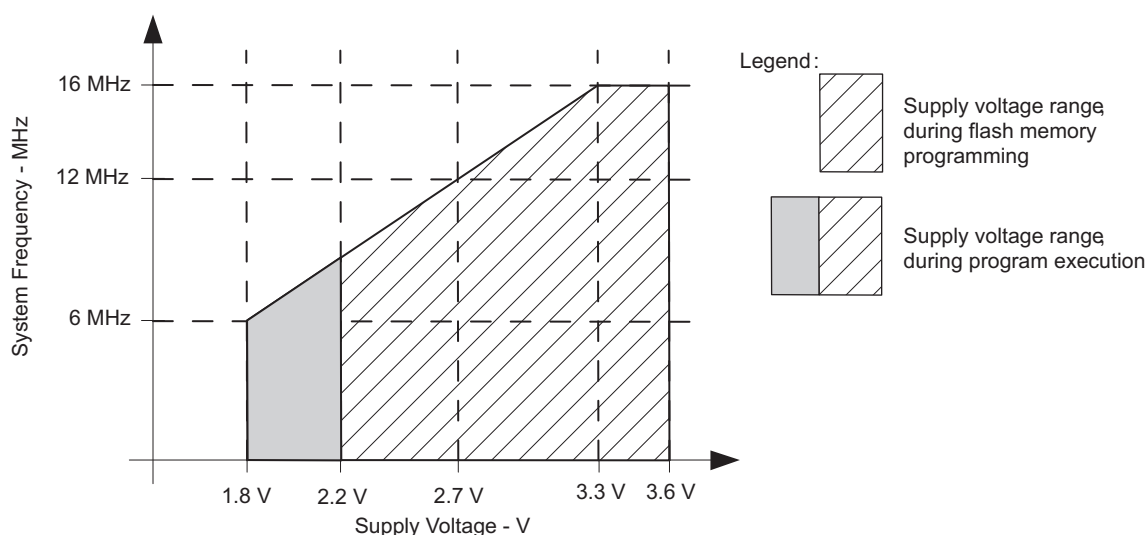
- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to  $V_{SS}$ . The JTAG fuse-blow voltage,  $V_{FB}$ , is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
- (3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

### 9.2 Recommended Operating Conditions

Typical values are specified at  $V_{CC} = 3.3$  V and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

|                     |                                                                |                                                    | MIN | NOM | MAX | UNIT |
|---------------------|----------------------------------------------------------------|----------------------------------------------------|-----|-----|-----|------|
| V <sub>CC</sub>     | Supply voltage                                                 | During program execution                           | 1.8 |     | 3.6 | V    |
|                     |                                                                | During flash programming                           | 2.2 |     | 3.6 |      |
| V <sub>SS</sub>     | Supply voltage                                                 |                                                    |     | 0   |     | V    |
| T <sub>A</sub>      | Operating free-air temperature                                 | I version                                          | −40 |     | 85  | °C   |
| f <sub>SYSTEM</sub> | Processor frequency (maximum MCLK frequency) <sup>(1)(2)</sup> | V <sub>CC</sub> = 1.8 V,<br>Duty cycle = 50% ± 10% | dc  |     | 6   | MHz  |
|                     |                                                                | V <sub>CC</sub> = 2.7 V,<br>Duty cycle = 50% ± 10% | dc  |     | 12  |      |
|                     |                                                                | V <sub>CC</sub> = 3.3 V,<br>Duty cycle = 50% ± 10% | dc  |     | 16  |      |

- (1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- (2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum  $V_{CC}$  of 2.2 V.

**Figure 2. Safe Operating Area**

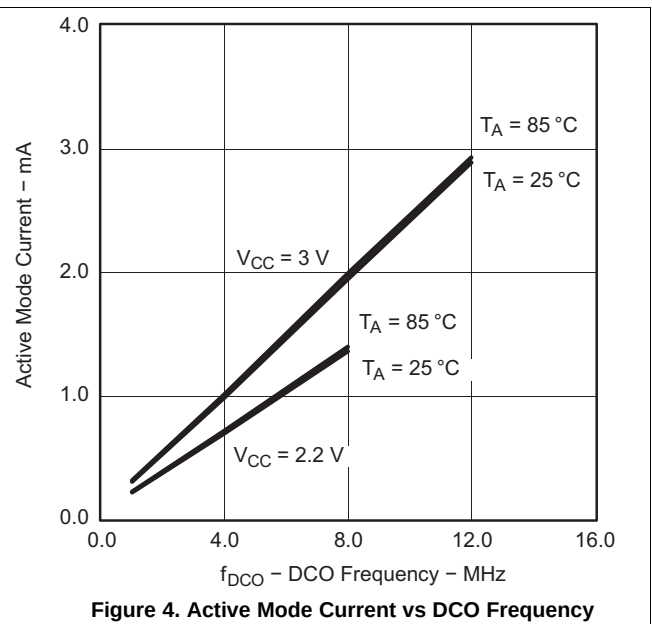
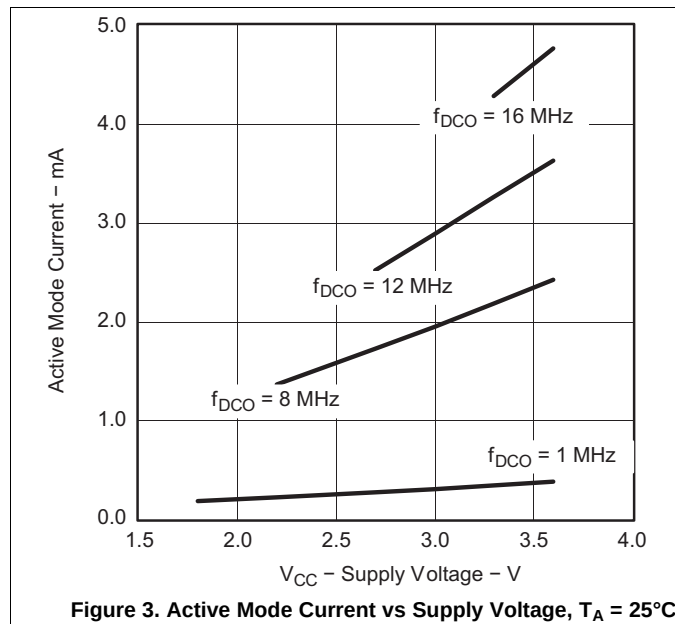
### 9.3 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)(2)</sup>

| PARAMETER                                      | TEST CONDITIONS                                                                                                                                                                                                       | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT          |
|------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|----------|-----|-----|-----|---------------|
| $I_{AM,1MHz}$ Active mode (AM) current (1 MHz) | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 1\text{ MHz}$ ,<br>$f_{ACLK} = 32768\text{ Hz}$ ,<br>Program executes in flash,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 0, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0 |       | 2.2 V    |     | 220 |     | $\mu\text{A}$ |
|                                                |                                                                                                                                                                                                                       |       | 3 V      |     | 300 | 370 |               |

- (1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.  
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

### 9.4 Typical Characteristics – Active Mode Supply Current (Into $V_{CC}$ )



## 9.5 Low-Power Mode Supply Currents (Into $V_{CC}$ ) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                                                       | TEST CONDITIONS                                                                                                                                                                     | $T_A$ | $V_{CC}$ | MIN | TYP | MAX | UNIT    |
|-----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|----------|-----|-----|-----|---------|
| $I_{LPM0,1MHz}$ Low-power mode 0 (LPM0) current <sup>(3)</sup>  | $f_{MCLK} = 0$ MHz,<br>$f_{SMCLK} = f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 0,<br>OSCOFF = 0 | 25°C  | 2.2 V    |     | 65  |     | $\mu A$ |
| $I_{LPM2}$ Low-power mode 2 (LPM2) current <sup>(4)</sup>       | $f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{DCO} = 1$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>BCSCTL1 = CALBC1_1MHZ,<br>DCOCTL = CALDCO_1MHZ,<br>CPUOFF = 1, SCG0 = 0, SCG1 = 1,<br>OSCOFF = 0 | 25°C  | 2.2 V    |     | 22  |     | $\mu A$ |
| $I_{LPM3,LFXT1}$ Low-power mode 3 (LPM3) current <sup>(4)</sup> | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 32768$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0                                                                | 25°C  | 2.2 V    |     | 0.7 | 1.5 | $\mu A$ |
| $I_{LPM3,VLO}$ Low-power mode 3 current, (LPM3) <sup>(4)</sup>  | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK}$ from internal LF oscillator (VLO),<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 0                                         | 25°C  | 2.2 V    |     | 0.5 | 0.7 | $\mu A$ |
| $I_{LPM4}$ Low-power mode 4 (LPM4) current <sup>(5)</sup>       | $f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz,<br>$f_{ACLK} = 0$ Hz,<br>CPUOFF = 1, SCG0 = 1, SCG1 = 1,<br>OSCOFF = 1                                                                    | 25°C  | 2.2 V    |     | 0.1 | 0.5 | $\mu A$ |
|                                                                 |                                                                                                                                                                                     | 85°C  | 2.2 V    |     | 0.8 | 1.5 | $\mu A$ |

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.

(3) Current for brownout and WDT clocked by SMCLK included.

(4) Current for brownout and WDT clocked by ACLK included.

(5) Current for brownout included.

## 9.6 Typical Characteristics, Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

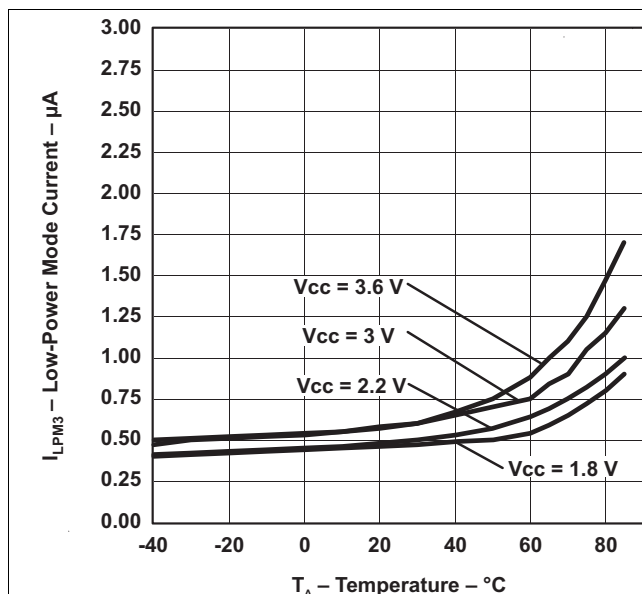


Figure 5. LPM3 Current vs Temperature

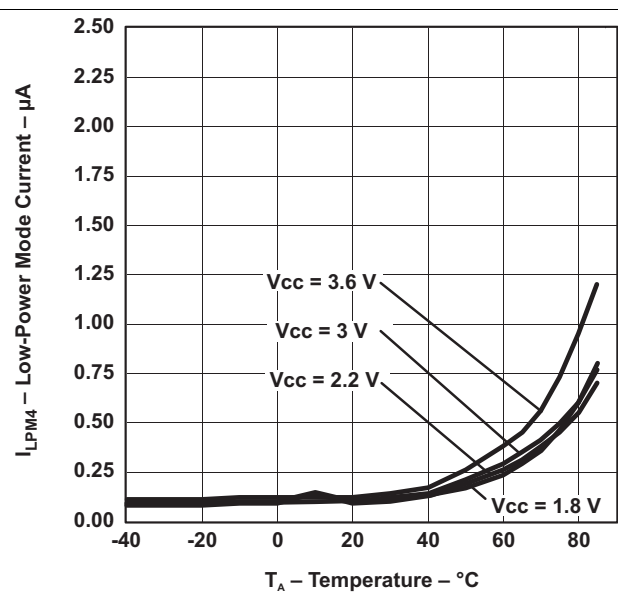


Figure 6. LPM4 Current vs Temperature

## 9.7 Schmitt-Trigger Inputs – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                        | TEST CONDITIONS                                                                                  | V <sub>CC</sub> | MIN                  | TYP | MAX                  | UNIT |
|----------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|-----------------|----------------------|-----|----------------------|------|
| V <sub>IT+</sub> Positive-going input threshold voltage                          |                                                                                                  |                 | 0.45 V <sub>CC</sub> |     | 0.75 V <sub>CC</sub> | V    |
|                                                                                  |                                                                                                  | 3 V             | 1.35                 |     | 2.25                 |      |
| V <sub>IT–</sub> Negative-going input threshold voltage                          |                                                                                                  |                 | 0.25 V <sub>CC</sub> |     | 0.55 V <sub>CC</sub> | V    |
|                                                                                  |                                                                                                  | 3 V             | 0.75                 |     | 1.65                 |      |
| V <sub>hys</sub> Input voltage hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> ) |                                                                                                  | 3 V             | 0.3                  |     | 1                    | V    |
| R <sub>Pull</sub> Pullup/pulldown resistor                                       | For pullup: V <sub>IN</sub> = V <sub>SS</sub><br>For pulldown: V <sub>IN</sub> = V <sub>CC</sub> | 3 V             | 20                   | 35  | 50                   | kΩ   |
| C <sub>I</sub> Input capacitance                                                 | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>CC</sub>                                             |                 |                      | 5   |                      | pF   |

## 9.8 Leakage Current – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                              | TEST CONDITIONS | V <sub>CC</sub> | MIN | MAX | UNIT |
|--------------------------------------------------------|-----------------|-----------------|-----|-----|------|
| I <sub>lkg</sub> (Px,y) High-impedance leakage current | (1) (2)         | 3 V             |     | ±50 | nA   |

- (1) The leakage current is measured with V<sub>SS</sub> or V<sub>CC</sub> applied to the corresponding pin(s), unless otherwise noted.  
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

## 9.9 Outputs – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS                             | V <sub>CC</sub> | MIN | TYP                   | MAX | UNIT |
|-------------------------------------------|---------------------------------------------|-----------------|-----|-----------------------|-----|------|
| V <sub>OH</sub> High-level output voltage | I <sub>(OHmax)</sub> = –6 mA <sup>(1)</sup> | 3 V             |     | V <sub>CC</sub> – 0.3 |     | V    |
| V <sub>OL</sub> Low-level output voltage  | I <sub>(OLmax)</sub> = 6 mA <sup>(1)</sup>  | 3 V             |     | V <sub>SS</sub> + 0.3 |     | V    |

- (1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

## 9.10 Output Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                           | TEST CONDITIONS                                                        | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------|------------------------------------------------------------------------|-----------------|-----|-----|-----|------|
| f <sub>Px,y</sub> Port output frequency (with load) | Px,y, C <sub>L</sub> = 20 pF, R <sub>L</sub> = 1 kΩ <sup>(1)</sup> (2) | 3 V             |     | 12  |     | MHz  |
| f <sub>Port_CLK</sub> Clock output frequency        | Px,y, C <sub>L</sub> = 20 pF <sup>(2)</sup>                            | 3 V             |     | 16  |     | MHz  |

- (1) A resistive divider with 2 × 0.5 kΩ between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider.  
(2) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

## 9.11 Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

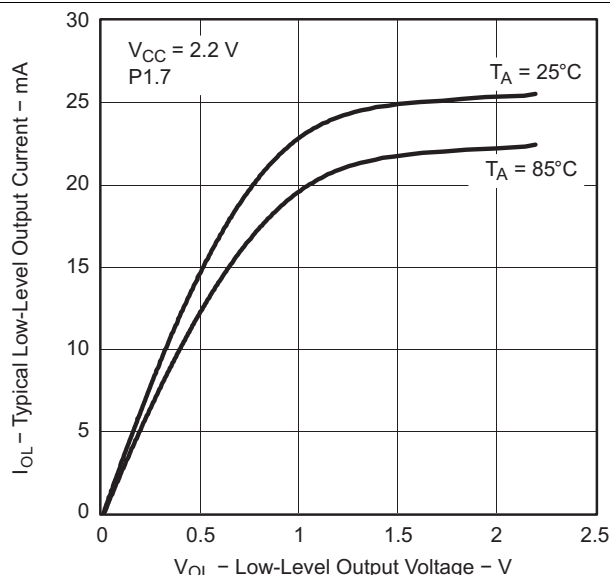


**Figure 7. Typical Low-Level Output Current vs Low-Level Output Voltage**

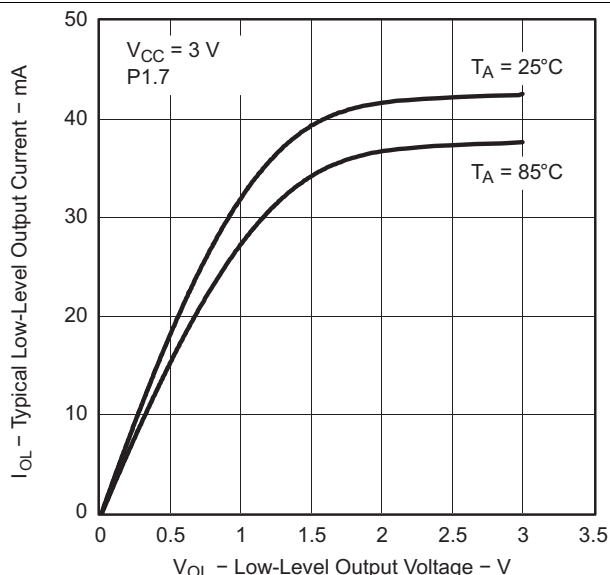


**Figure 8. Typical Low-Level Output Current vs Low-Level Output Voltage**

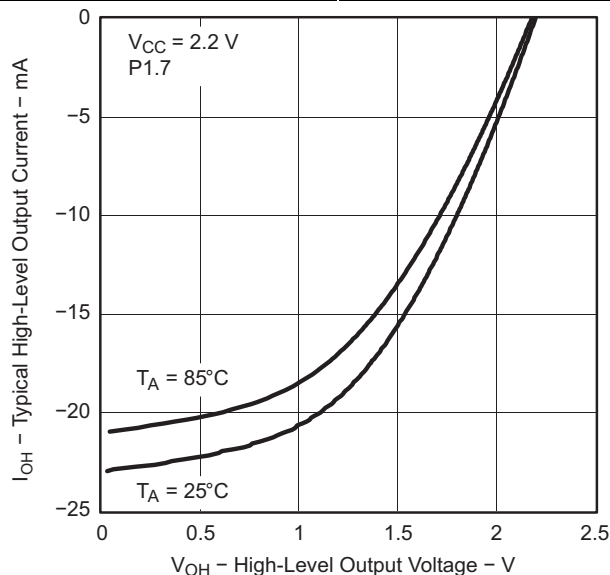


**Figure 9. Typical High-Level Output Current vs High-Level Output Voltage**

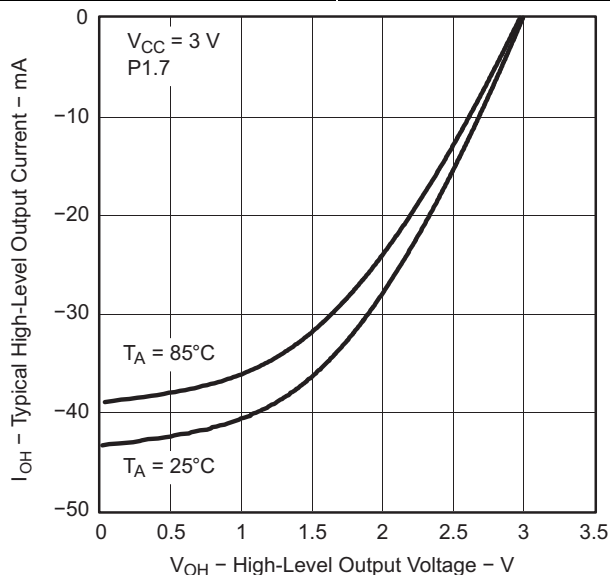


**Figure 10. Typical High-Level Output Current vs High-Level Output Voltage**

## 9.12 POR, BOR<sup>(1)(2)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS                                                                              | V <sub>CC</sub>              | MIN | TYP                        | MAX  | UNIT |
|-------------------------|----------------------------------------------------------------------------------------------|------------------------------|-----|----------------------------|------|------|
| V <sub>CC(start)</sub>  | See Figure 11                                                                                | dV <sub>CC</sub> /dt ≤ 3 V/s |     | 0.7 × V <sub>(B_IT-)</sub> |      | V    |
| V <sub>(B_IT-)</sub>    | See Figure 11 through Figure 13                                                              | dV <sub>CC</sub> /dt ≤ 3 V/s |     | 1.35                       |      | V    |
| V <sub>hys(B_IT-)</sub> | See Figure 11                                                                                | dV <sub>CC</sub> /dt ≤ 3 V/s |     | 130                        |      | mV   |
| t <sub>d(BOR)</sub>     | See Figure 11                                                                                |                              |     |                            | 2000 | μs   |
| t <sub>(reset)</sub>    | Pulse duration needed at $\overline{\text{RST}}/\text{NMI}$ pin to accepted reset internally | 2.2 V, 3 V                   | 2   |                            |      | μs   |

- (1) The current consumption of the brownout module is already included in the I<sub>CC</sub> current consumption data. The voltage level V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub> is ≤ 1.8 V.
- (2) During power up, the CPU begins code execution following a period of t<sub>d(BOR)</sub> after V<sub>CC</sub> = V<sub>(B\_IT-)</sub> + V<sub>hys(B\_IT-)</sub>. The default DCO settings must not be changed until V<sub>CC</sub> ≥ V<sub>CC(min)</sub>, where V<sub>CC(min)</sub> is the minimum supply voltage for the desired operating frequency.

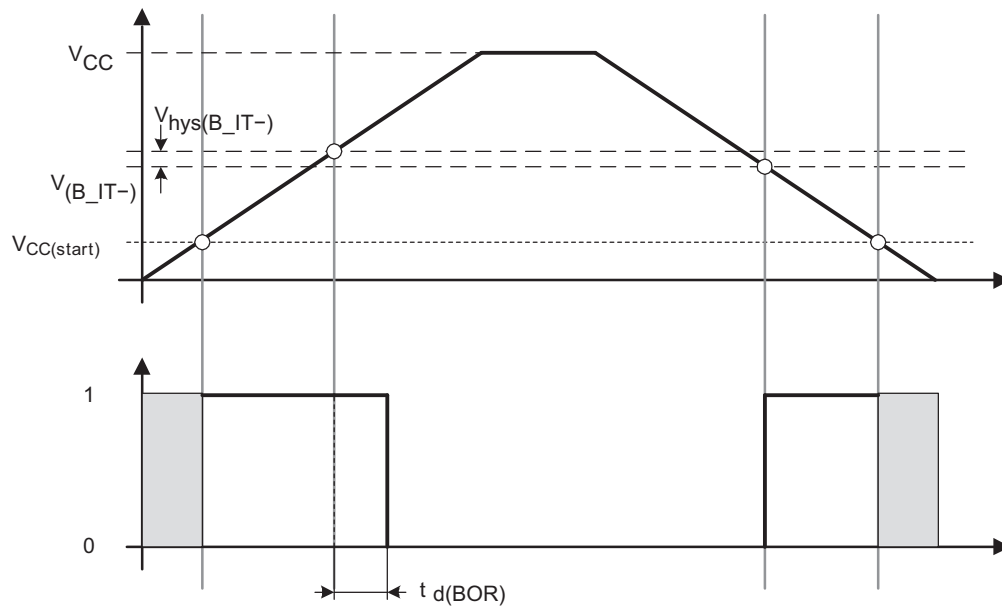


Figure 11. POR and BOR vs Supply Voltage

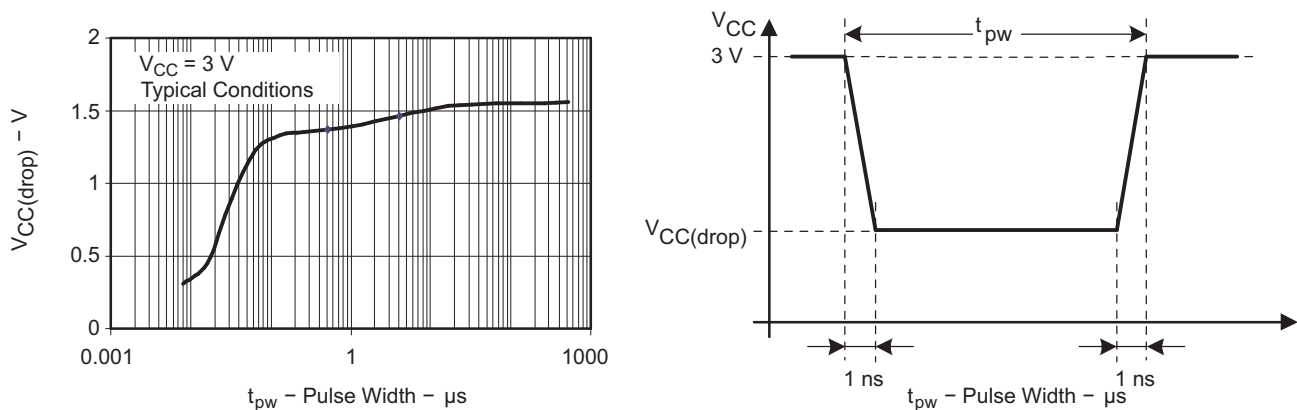


Figure 12. V<sub>CC(drop)</sub> Level With a Square Voltage Drop to Generate a POR or BOR Signal

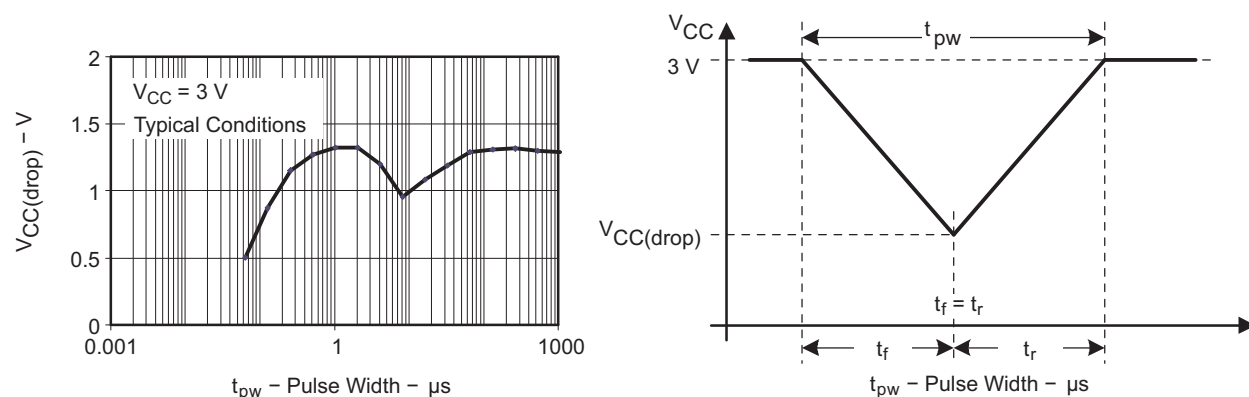


**Figure 13.  $V_{CC(drop)}$  Level With a Triangle Voltage Drop to Generate a POR or BOR Signal**

### 9.13 Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S<sub>DCO</sub>.
- Modulation control bits MODx select how often f<sub>DCO(RSEL,DCO+1)</sub> is used within the period of 32 DCOCLK cycles. The frequency f<sub>DCO(RSEL,DCO)</sub> is used for the remaining cycles. The frequency is an average equal to:

$$f_{\text{average}} = \frac{32 \times f_{\text{DCO(RSEL,DCO)}} \times f_{\text{DCO(RSEL,DCO+1)}}}{\text{MOD} \times f_{\text{DCO(RSEL,DCO)}} + (32 - \text{MOD}) \times f_{\text{DCO(RSEL,DCO+1)}}}$$

### 9.14 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER              |                                              | TEST CONDITIONS                                                              | V <sub>CC</sub> | MIN  | TYP   | MAX  | UNIT  |
|------------------------|----------------------------------------------|------------------------------------------------------------------------------|-----------------|------|-------|------|-------|
| V <sub>CC</sub>        | Supply voltage                               | RSELx < 14                                                                   |                 | 1.8  |       | 3.6  | V     |
|                        |                                              | RSELx = 14                                                                   |                 | 2.2  |       | 3.6  | V     |
|                        |                                              | RSELx = 15                                                                   |                 | 3    |       | 3.6  | V     |
| f <sub>DCO(0,0)</sub>  | DCO frequency (0, 0)                         | RSELx = 0, DCOx = 0, MODx = 0                                                | 3 V             | 0.06 |       | 0.14 | MHz   |
| f <sub>DCO(0,3)</sub>  | DCO frequency (0, 3)                         | RSELx = 0, DCOx = 3, MODx = 0                                                | 3 V             |      | 0.12  |      | MHz   |
| f <sub>DCO(1,3)</sub>  | DCO frequency (1, 3)                         | RSELx = 1, DCOx = 3, MODx = 0                                                | 3 V             |      | 0.15  |      | MHz   |
| f <sub>DCO(2,3)</sub>  | DCO frequency (2, 3)                         | RSELx = 2, DCOx = 3, MODx = 0                                                | 3 V             |      | 0.21  |      | MHz   |
| f <sub>DCO(3,3)</sub>  | DCO frequency (3, 3)                         | RSELx = 3, DCOx = 3, MODx = 0                                                | 3 V             |      | 0.30  |      | MHz   |
| f <sub>DCO(4,3)</sub>  | DCO frequency (4, 3)                         | RSELx = 4, DCOx = 3, MODx = 0                                                | 3 V             |      | 0.41  |      | MHz   |
| f <sub>DCO(5,3)</sub>  | DCO frequency (5, 3)                         | RSELx = 5, DCOx = 3, MODx = 0                                                | 3 V             |      | 0.58  |      | MHz   |
| f <sub>DCO(6,3)</sub>  | DCO frequency (6, 3)                         | RSELx = 6, DCOx = 3, MODx = 0                                                | 3 V             |      | 0.80  |      | MHz   |
| f <sub>DCO(7,3)</sub>  | DCO frequency (7, 3)                         | RSELx = 7, DCOx = 3, MODx = 0                                                | 3 V             | 0.8  |       | 1.5  | MHz   |
| f <sub>DCO(8,3)</sub>  | DCO frequency (8, 3)                         | RSELx = 8, DCOx = 3, MODx = 0                                                | 3 V             |      | 1.6   |      | MHz   |
| f <sub>DCO(9,3)</sub>  | DCO frequency (9, 3)                         | RSELx = 9, DCOx = 3, MODx = 0                                                | 3 V             |      | 2.3   |      | MHz   |
| f <sub>DCO(10,3)</sub> | DCO frequency (10, 3)                        | RSELx = 10, DCOx = 3, MODx = 0                                               | 3 V             |      | 3.4   |      | MHz   |
| f <sub>DCO(11,3)</sub> | DCO frequency (11, 3)                        | RSELx = 11, DCOx = 3, MODx = 0                                               | 3 V             |      | 4.25  |      | MHz   |
| f <sub>DCO(12,3)</sub> | DCO frequency (12, 3)                        | RSELx = 12, DCOx = 3, MODx = 0                                               | 3 V             | 4.3  |       | 7.3  | MHz   |
| f <sub>DCO(13,3)</sub> | DCO frequency (13, 3)                        | RSELx = 13, DCOx = 3, MODx = 0                                               | 3 V             |      | 7.8   |      | MHz   |
| f <sub>DCO(14,3)</sub> | DCO frequency (14, 3)                        | RSELx = 14, DCOx = 3, MODx = 0                                               | 3 V             | 8.6  |       | 13.9 | MHz   |
| f <sub>DCO(15,3)</sub> | DCO frequency (15, 3)                        | RSELx = 15, DCOx = 3, MODx = 0                                               | 3 V             |      | 15.25 |      | MHz   |
| f <sub>DCO(15,7)</sub> | DCO frequency (15, 7)                        | RSELx = 15, DCOx = 7, MODx = 0                                               | 3 V             |      | 21    |      | MHz   |
| S <sub>RSEL</sub>      | Frequency step between range RSEL and RSEL+1 | S <sub>RSEL</sub> = f <sub>DCO(RSEL+1,DCO)</sub> /f <sub>DCO(RSEL,DCO)</sub> | 3 V             |      | 1.35  |      | ratio |
| S <sub>DCO</sub>       | Frequency step between tap DCO and DCO+1     | S <sub>DCO</sub> = f <sub>DCO(RSEL,DCO+1)</sub> /f <sub>DCO(RSEL,DCO)</sub>  | 3 V             |      | 1.08  |      | ratio |
|                        | Duty cycle                                   | Measured at SMCLK output                                                     | 3 V             |      | 50    |      | %     |

## 9.15 Calibrated DCO Frequencies – Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                       | TEST CONDITIONS                                                              | T <sub>A</sub>                  | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|-------------------------------------------------|------------------------------------------------------------------------------|---------------------------------|-----------------|-----|------|-----|------|
| 1-MHz tolerance over temperature <sup>(1)</sup> | BCSCTL1= CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>calibrated at 30°C and 3 V | 0°C to 85°C<br>-40°C to 105°C   | 3 V             | -3  | ±0.5 | +3  | %    |
| 1-MHz tolerance over V <sub>CC</sub>            | BCSCTL1= CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>calibrated at 30°C and 3 V | 30°C                            | 1.8 V to 3.6 V  | -3  | ±2   | +3  | %    |
| 1-MHz tolerance overall                         | BCSCTL1= CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz,<br>calibrated at 30°C and 3 V | -40°C to 85°C<br>-40°C to 105°C | 1.8 V to 3.6 V  | -6  | ±3   | +6  | %    |

(1) This is the frequency change from the measured frequency at 30°C over temperature.

## 9.16 Wakeup From Lower-Power Modes (LPM3, LPM4) – Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS                                        | V <sub>CC</sub>                               | MIN | TYP                                                | MAX | UNIT |
|-------------------------|--------------------------------------------------------|-----------------------------------------------|-----|----------------------------------------------------|-----|------|
| t <sub>DCO,LPM3/4</sub> | DCO clock wakeup time from LPM3 or LPM4 <sup>(1)</sup> | BCSCTL1= CALBC1_1MHz,<br>DCOCTL = CALDCO_1MHz | 3 V | 1.5                                                |     | μs   |
| t <sub>CPU,LPM3/4</sub> | CPU wakeup time from LPM3 or LPM4 <sup>(2)</sup>       |                                               |     | 1/f <sub>MCLK</sub> +<br>t <sub>Clock,LPM3/4</sub> |     |      |

(1) The DCO clock wakeup time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).

(2) Parameter applicable only if DCOCLK is used for MCLK.

## 9.17 Typical Characteristics – DCO Clock Wakeup Time From LPM3, LPM4

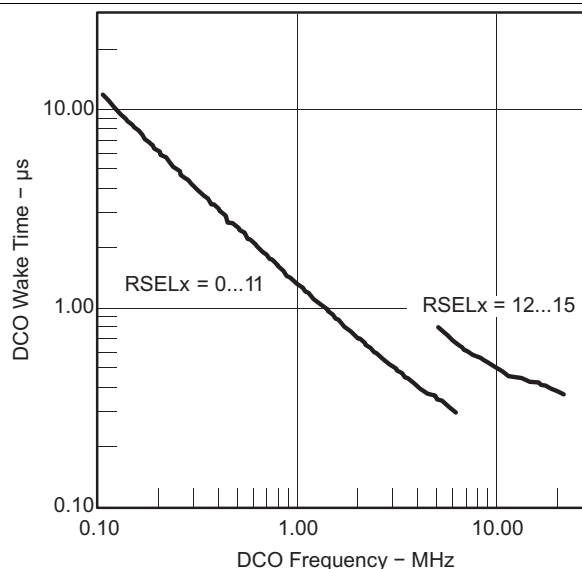


Figure 14. DCO Wakeup Time From LPM3 vs DCO Frequency

## 9.18 Crystal Oscillator, Xt1, Low-Frequency Mode <sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                   |                                                                   | TEST CONDITIONS                                                                    | V <sub>CC</sub> | MIN   | TYP   | MAX   | UNIT |
|-----------------------------|-------------------------------------------------------------------|------------------------------------------------------------------------------------|-----------------|-------|-------|-------|------|
| f <sub>LFXT1,LF</sub>       | LFXT1 oscillator crystal frequency, LF mode 0, 1                  | XTS = 0, LFXT1Sx = 0 or 1                                                          | 1.8 V to 3.6 V  | 32768 |       |       | Hz   |
| f <sub>LFXT1,LF,logic</sub> | LFXT1 oscillator logic level square wave input frequency, LF mode | XTS = 0, XCAPx = 0, LFXT1Sx = 3                                                    | 1.8 V to 3.6 V  | 10000 | 32768 | 50000 | Hz   |
| O <sub>A,LF</sub>           | Oscillation allowance for LF crystals                             | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 6 pF  |                 | 500   |       |       | kΩ   |
|                             |                                                                   | XTS = 0, LFXT1Sx = 0, f <sub>LFXT1,LF</sub> = 32768 Hz, C <sub>L,eff</sub> = 12 pF |                 | 200   |       |       |      |
| C <sub>L,eff</sub>          | Integrated effective load capacitance, LF mode <sup>(2)</sup>     | XTS = 0, XCAPx = 0                                                                 |                 | 1     |       |       | pF   |
|                             |                                                                   | XTS = 0, XCAPx = 1                                                                 |                 | 5.5   |       |       |      |
|                             |                                                                   | XTS = 0, XCAPx = 2                                                                 |                 | 8.5   |       |       |      |
|                             |                                                                   | XTS = 0, XCAPx = 3                                                                 |                 | 11    |       |       |      |
|                             | Duty cycle, LF mode                                               | XTS = 0, Measured at P2.0/ACLK, f <sub>LFXT1,LF</sub> = 32768 Hz                   | 2.2 V           | 30    | 50    | 70    | %    |
| f <sub>Fault,LF</sub>       | Oscillator fault frequency, LF mode <sup>(3)</sup>                | XTS = 0, XCAPx = 0, LFXT1Sx = 3 <sup>(4)</sup>                                     | 2.2 V           | 10    | 10000 |       | Hz   |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  - (a) Keep the trace between the device and the crystal as short as possible.
  - (b) Design a good ground plane around the oscillator pins.
  - (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  - (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  - (e) Use assembly materials and techniques that avoid any parasitic load on the oscillator XIN and XOUT pins.
  - (f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
  - (g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).  
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (4) Measured with logic-level input frequency but also applies to operation with crystals.

## 9.19 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                           |                                    | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|----------------|-----------------|-----|-----|-----|------|
| f <sub>VLO</sub>                    | VLO frequency                      | -40°C to 85°C  | 3 V             | 4   | 12  | 20  | kHz  |
| df <sub>VLO</sub> /dT               | VLO frequency temperature drift    | -40°C to 85°C  | 3 V             |     | 0.5 |     | %/°C |
| df <sub>VLO</sub> /dV <sub>CC</sub> | VLO frequency supply voltage drift | 25°C           | 1.8 V to 3.6 V  |     | 4   |     | %/V  |

## 9.20 Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS                                                                                            | V <sub>CC</sub> | MIN | TYP                 | MAX | UNIT |
|---------------------|------------------------------------------------------------------------------------------------------------|-----------------|-----|---------------------|-----|------|
| f <sub>TA</sub>     | Timer_A input clock frequency<br>Internal: SMCLK, ACLK<br>External: TACLK, INCLK<br>Duty cycle = 50% ± 10% |                 |     | f <sub>SYSTEM</sub> |     | MHz  |
| t <sub>TA,cap</sub> | Timer_A capture timing                                                                                     | TA0, TA1        | 3 V | 20                  |     | ns   |

## 9.21 USI, Universal Serial Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           | TEST CONDITIONS                                                          | V <sub>CC</sub> | MIN             | TYP                 | MAX                   | UNIT |
|---------------------|--------------------------------------------------------------------------|-----------------|-----------------|---------------------|-----------------------|------|
| f <sub>USI</sub>    | USI clock frequency                                                      |                 |                 | f <sub>SYSTEM</sub> |                       | MHz  |
| V <sub>OL,I2C</sub> | Low-level output voltage on SDA and SCL<br>I <sub>(OLmax)</sub> = 1.5 mA | 3 V             | V <sub>SS</sub> |                     | V <sub>SS</sub> + 0.4 | V    |

## 9.22 Typical Characteristics – USI Low-Level Output Voltage On SDA and SCL

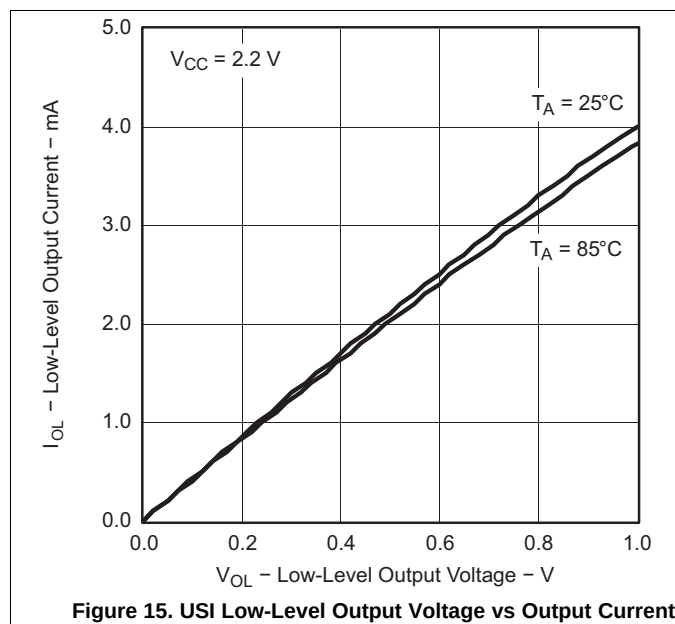


Figure 15. USI Low-Level Output Voltage vs Output Current

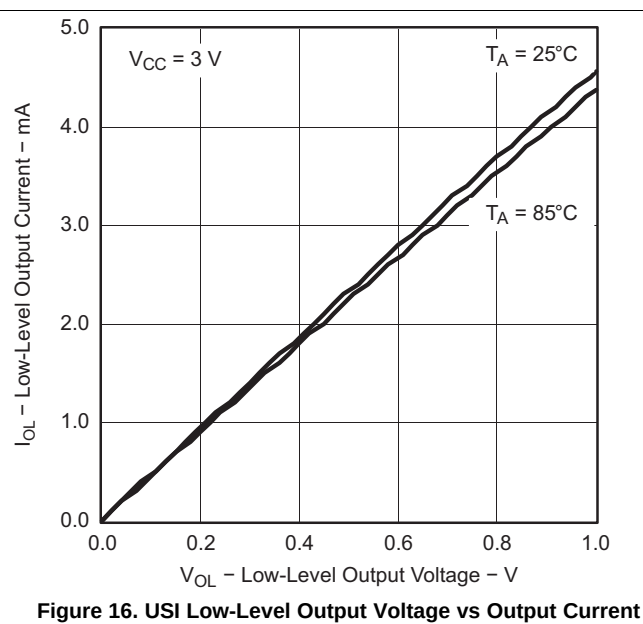


Figure 16. USI Low-Level Output Voltage vs Output Current

## 9.23 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

| PARAMETER           |                                                                       | TEST CONDITIONS                                                                                              | T <sub>A</sub> | V <sub>CC</sub> | MIN | TYP  | MAX             | UNIT |
|---------------------|-----------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|----------------|-----------------|-----|------|-----------------|------|
| V <sub>CC</sub>     | Analog supply voltage                                                 | V <sub>SS</sub> = 0 V                                                                                        |                |                 | 2.2 |      | 3.6             | V    |
| V <sub>AX</sub>     | Analog input voltage <sup>(2)</sup>                                   | All Ax terminals, Analog inputs selected in ADC10AE register                                                 |                | 3 V             | 0   |      | V <sub>CC</sub> | V    |
| I <sub>ADC10</sub>  | ADC10 supply current <sup>(3)</sup>                                   | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 1, REFON = 0,<br>ADC10SHT0 = 1, ADC10SHT1 = 0,<br>ADC10DIV = 0 |                | 3 V             |     | 0.6  | 1.2             | mA   |
| I <sub>REF+</sub>   | Reference supply current,<br>reference buffer disabled <sup>(4)</sup> | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REF2_5V = 0,<br>REFON = 1, REFOUT = 0                       |                | 3 V             |     | 0.25 | 0.4             | mA   |
|                     |                                                                       | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REF2_5V = 1,<br>REFON = 1, REFOUT = 0                       |                |                 |     | 0.25 | 0.4             |      |
| I <sub>REFB,0</sub> | Reference buffer supply<br>current with ADC10SR = 0 <sup>(4)</sup>    | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REFON = 1,<br>REF2_5V = 0, REFOUT = 1,<br>ADC10SR = 0       |                | 3 V             |     | 1.1  | 1.4             | mA   |
| I <sub>REFB,1</sub> | Reference buffer supply<br>current with ADC10SR = 1 <sup>(4)</sup>    | f <sub>ADC10CLK</sub> = 5.0 MHz,<br>ADC10ON = 0, REFON = 1,<br>REF2_5V = 0, REFOUT = 1,<br>ADC10SR = 1       |                | 3 V             |     | 0.5  | 0.7             | mA   |
| C <sub>I</sub>      | Input capacitance                                                     | Only one terminal Ax can be selected<br>at one time                                                          |                | 3 V             |     |      | 27              | pF   |
| R <sub>I</sub>      | Input MUX ON resistance                                               | 0 V ≤ V <sub>AX</sub> ≤ V <sub>CC</sub>                                                                      |                | 3 V             |     | 1000 | 2000            | Ω    |

- (1) The leakage current is defined in the leakage current table with Px.y/Ax parameter.
- (2) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results.
- (3) The internal reference supply current is not included in current consumption parameter I<sub>ADC10</sub>.
- (4) The internal reference current is supplied via terminal V<sub>CC</sub>. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

## 9.24 10-Bit ADC, Built-In Voltage Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                       | TEST CONDITIONS                                                                                                               | V <sub>CC</sub> | MIN  | TYP | MAX  | UNIT   |
|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-----------------|------|-----|------|--------|
| V <sub>CC,REF+</sub>                            | Positive built-in reference analog supply voltage range<br>I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 0                             |                 | 2.2  |     |      | V      |
|                                                 | I <sub>VREF+</sub> ≤ 1 mA, REF2_5V = 1                                                                                        |                 | 2.9  |     |      |        |
| V <sub>REF+</sub>                               | Positive built-in reference voltage<br>I <sub>VREF+</sub> ≤ I <sub>VREF+max</sub> , REF2_5V = 0                               | 3 V             | 1.41 | 1.5 | 1.59 | V      |
|                                                 | I <sub>VREF+</sub> ≤ I <sub>VREF+max</sub> , REF2_5V = 1                                                                      |                 | 2.35 | 2.5 | 2.65 |        |
| I <sub>LD,VREF+</sub>                           | Maximum VREF+ load current                                                                                                    | 3 V             |      |     | ±1   | mA     |
| VREF+ load regulation                           | I <sub>VREF+</sub> = 500 μA ± 100 μA,<br>Analog input voltage V <sub>AX</sub> ≈ 0.75 V,<br>REF2_5V = 0                        | 3 V             |      |     | ±2   | LSB    |
|                                                 | I <sub>VREF+</sub> = 500 μA ± 100 μA,<br>Analog input voltage V <sub>AX</sub> ≈ 1.25 V,<br>REF2_5V = 1                        |                 |      |     | ±2   |        |
| V <sub>REF+</sub> load regulation response time | I <sub>VREF+</sub> = 100 μA → 900 μA,<br>V <sub>AX</sub> ≈ 0.5 × VREF+,<br>Error of conversion result ≤ 1 LSB,<br>ADC10SR = 0 | 3 V             |      |     | 400  | ns     |
| C <sub>VREF+</sub>                              | Maximum capacitance at pin VREF+                                                                                              | 3 V             |      |     | 100  | pF     |
| TC <sub>REF+</sub>                              | Temperature coefficient                                                                                                       | 3 V             |      |     | ±100 | ppm/°C |
| t <sub>REFON</sub>                              | Settling time of internal reference voltage to 99.9% VREF                                                                     | 3.6 V           |      |     | 30   | μs     |
| t <sub>REFBURST</sub>                           | Settling time of reference buffer to 99.9% VREF                                                                               | 3 V             |      |     | 2    | μs     |

## 9.25 10-Bit ADC, External Reference<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                            | TEST CONDITIONS                                                                    | V <sub>CC</sub> | MIN | TYP | MAX             | UNIT |
|--------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----------------|-----|-----|-----------------|------|
| VEREF+ Positive external reference input voltage range <sup>(2)</sup>                | VEREF+ > VEREF–, SREF1 = 1, SREF0 = 0                                              |                 | 1.4 |     | V <sub>CC</sub> | V    |
|                                                                                      | VEREF– ≤ VEREF+ ≤ V <sub>CC</sub> – 0.15 V, SREF1 = 1, SREF0 = 1 <sup>(3)</sup>    |                 | 1.4 |     | 3               |      |
| VEREF– Negative external reference input voltage range <sup>(4)</sup>                | VEREF+ > VEREF–                                                                    |                 | 0   |     | 1.2             | V    |
| ΔVEREF Differential external reference input voltage range, ΔVEREF = VEREF+ – VEREF– | VEREF+ > VEREF– <sup>(5)</sup>                                                     |                 | 1.4 |     | V <sub>CC</sub> | V    |
| I <sub>VEREF+</sub> Static input current into VREF+                                  | 0 V ≤ VEREF+ ≤ V <sub>CC</sub> , SREF1 = 1, SREF0 = 0                              | 3 V             |     | ±1  |                 | μA   |
|                                                                                      | 0 V ≤ VEREF+ ≤ V <sub>CC</sub> – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 <sup>(3)</sup> | 3 V             |     | 0   |                 |      |
| I <sub>VEREF–</sub> Static input current into VREF–                                  | 0 V ≤ VEREF– ≤ V <sub>CC</sub>                                                     | 3 V             |     | ±1  |                 | μA   |

- (1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C<sub>I</sub>, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- (2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- (3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I<sub>REFB</sub>. The current consumption can be limited to the sample and conversion period with REBURST = 1.
- (4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- (5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

## 9.26 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                 | TEST CONDITIONS                                                                          | V <sub>CC</sub> | MIN  | TYP                                     | MAX  | UNIT |
|-----------------------------------------------------------|------------------------------------------------------------------------------------------|-----------------|------|-----------------------------------------|------|------|
| f <sub>ADC10CLK</sub> ADC10 input clock frequency         | For specified performance of ADC10 linearity parameters                                  | 3 V             | 0.45 |                                         | 6.3  | MHz  |
|                                                           | ADC10SR = 0<br>ADC10SR = 1                                                               |                 | 0.45 |                                         | 1.5  |      |
| f <sub>ADC10OSC</sub> ADC10 built-in oscillator frequency | ADC10DIVx = 0, ADC10SSELx = 0, f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub>             | 3 V             | 3.7  |                                         | 6.3  | MHz  |
| t <sub>CONVERT</sub> Conversion time                      | ADC10 built-in oscillator, ADC10SSELx = 0, f <sub>ADC10CLK</sub> = f <sub>ADC10OSC</sub> | 3 V             | 2.06 |                                         | 3.51 | μs   |
|                                                           | f <sub>ADC10CLK</sub> from ACLK, MCLK, or SMCLK, ADC10SSELx ≠ 0                          |                 |      | 13 × ADC10DIV × 1/f <sub>ADC10CLK</sub> |      |      |
| t <sub>ADC10ON</sub> Turn-on settling time of the ADC     | (1)                                                                                      |                 |      |                                         | 100  | ns   |

- (1) The condition is that the error in a conversion started after t<sub>ADC10ON</sub> is less than ±0.5 LSB. The reference and input signal are already settled.

## 9.27 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                   | TEST CONDITIONS                         | V <sub>CC</sub> | MIN | TYP  | MAX | UNIT |
|---------------------------------------------|-----------------------------------------|-----------------|-----|------|-----|------|
| E <sub>I</sub> Integral linearity error     |                                         | 3 V             |     |      | ±1  | LSB  |
| E <sub>D</sub> Differential linearity error |                                         | 3 V             |     |      | ±1  | LSB  |
| E <sub>O</sub> Offset error                 | Source impedance R <sub>S</sub> < 100 Ω | 3 V             |     |      | ±1  | LSB  |
| E <sub>G</sub> Gain error                   |                                         | 3 V             |     | ±1.1 | ±2  | LSB  |
| E <sub>T</sub> Total unadjusted error       |                                         | 3 V             |     | ±2   | ±5  | LSB  |

## 9.28 10-Bit ADC, Temperature Sensor and Built-In $V_{MID}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER            |                                                               | TEST CONDITIONS                                                   | $V_{CC}$ | MIN  | TYP  | MAX            | UNIT                       |
|----------------------|---------------------------------------------------------------|-------------------------------------------------------------------|----------|------|------|----------------|----------------------------|
| $I_{SENSOR}$         | Temperature sensor supply current <sup>(1)</sup>              | REFON = 0, INCHx = 0Ah, $T_A = 25^\circ\text{C}$                  | 3 V      |      | 60   |                | $\mu\text{A}$              |
| $TC_{SENSOR}$        |                                                               | ADC10ON = 1, INCHx = 0Ah <sup>(2)</sup>                           | 3 V      |      | 3.55 |                | $\text{mV}/^\circ\text{C}$ |
| $t_{Sensor(sample)}$ | Sample time required if channel 10 is selected <sup>(3)</sup> | ADC10ON = 1, INCHx = 0Ah, Error of conversion result $\leq 1$ LSB | 3 V      | 30   |      |                | $\mu\text{s}$              |
| $I_{VMID}$           | Current into divider at channel 11                            | ADC10ON = 1, INCHx = 0Bh                                          | 3 V      |      |      | <sup>(4)</sup> | $\mu\text{A}$              |
| $V_{MID}$            | $V_{CC}$ divider at channel 11                                | ADC10ON = 1, INCHx = 0Bh, $V_{MID} \neq 0.5 \times V_{CC}$        | 3 V      |      | 1.5  |                | V                          |
| $t_{VMID(sample)}$   | Sample time required if channel 11 is selected <sup>(5)</sup> | ADC10ON = 1, INCHx = 0Bh, Error of conversion result $\leq 1$ LSB | 3 V      | 1220 |      |                | ns                         |

- (1) The sensor current  $I_{SENSOR}$  is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1,  $I_{SENSOR}$  is included in  $I_{REF+}$ . When REFON = 0,  $I_{SENSOR}$  applies during conversion of the temperature sensor input (INCH = 0Ah).
- (2) The following formula can be used to calculate the temperature sensor output voltage:  
 $V_{Sensor,typ} = TC_{Sensor} (273 + T [^\circ\text{C}]) + V_{Offset,sensor} [\text{mV}]$  or  
 $V_{Sensor,typ} = TC_{Sensor} T [^\circ\text{C}] + V_{Sensor}(T_A = 0^\circ\text{C}) [\text{mV}]$
- (3) The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor-on time  $t_{SENSOR(on)}$ .
- (4) No additional current is needed. The  $V_{MID}$  is used during sampling.
- (5) The on-time  $t_{VMID(on)}$  is included in the sampling time  $t_{VMID(sample)}$ ; no additional on time is needed.

## 9.29 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER           |                                                     | TEST CONDITIONS          | $V_{CC}$     | MIN    | TYP    | MAX | UNIT      |
|---------------------|-----------------------------------------------------|--------------------------|--------------|--------|--------|-----|-----------|
| $V_{CC(PGM/ERASE)}$ | Program and erase supply voltage                    |                          |              | 2.2    |        | 3.6 | V         |
| $f_{FTG}$           | Flash timing generator frequency                    |                          |              | 257    |        | 476 | kHz       |
| $I_{PGM}$           | Supply current from $V_{CC}$ during program         |                          | 2.2 V, 3.6 V |        | 1      | 5   | mA        |
| $I_{ERASE}$         | Supply current from $V_{CC}$ during erase           |                          | 2.2 V, 3.6 V |        | 1      | 7   | mA        |
| $t_{CPT}$           | Cumulative program time <sup>(1)</sup>              |                          | 2.2 V, 3.6 V |        |        | 10  | ms        |
| $t_{CMErase}$       | Cumulative mass erase time                          |                          | 2.2 V, 3.6 V | 20     |        |     | ms        |
|                     | Program/erase endurance                             |                          |              | $10^4$ | $10^5$ |     | cycles    |
| $t_{Retention}$     | Data retention duration                             | $T_J = 25^\circ\text{C}$ |              | 15     |        |     | years     |
| $t_{Word}$          | Word or byte program time                           | <sup>(2)</sup>           |              |        | 30     |     | $t_{FTG}$ |
| $t_{Block, 0}$      | Block program time for first byte or word           | <sup>(2)</sup>           |              |        | 25     |     | $t_{FTG}$ |
| $t_{Block, 1-63}$   | Block program time for each additional byte or word | <sup>(2)</sup>           |              |        | 18     |     | $t_{FTG}$ |
| $t_{Block, End}$    | Block program end-sequence wait time                | <sup>(2)</sup>           |              |        | 6      |     | $t_{FTG}$ |
| $t_{Mass Erase}$    | Mass erase time                                     | <sup>(2)</sup>           |              |        | 10593  |     | $t_{FTG}$ |
| $t_{Seg Erase}$     | Segment erase time                                  | <sup>(2)</sup>           |              |        | 4819   |     | $t_{FTG}$ |

- (1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
- (2) These values are hardwired into the Flash Controller's state machine ( $t_{FTG} = 1/f_{FTG}$ ).

### 9.30 RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------------------------------------------------|-----------------|-----|-----|------|
| $V_{(RAMh)}$ RAM retention supply voltage <sup>(1)</sup> | CPU halted      | 1.6 |     | V    |

- (1) This parameter defines the minimum supply voltage  $V_{CC}$  when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

### 9.31 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                                                                          | TEST CONDITIONS | $V_{CC}$   | MIN   | TYP | MAX | UNIT       |
|----------------------------------------------------------------------------------------------------|-----------------|------------|-------|-----|-----|------------|
| $f_{SBW}$ Spy-Bi-Wire input frequency                                                              |                 | 2.2 V, 3 V | 0     |     | 20  | MHz        |
| $t_{SBW,Low}$ Spy-Bi-Wire low clock pulse length                                                   |                 | 2.2 V, 3 V | 0.025 |     | 15  | $\mu$ s    |
| $t_{SBW,En}$ Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge <sup>(1)</sup> ) |                 | 2.2 V, 3 V |       |     | 1   | $\mu$ s    |
| $t_{SBW,Ret}$ Spy-Bi-Wire return to normal operation time                                          |                 | 2.2 V, 3 V | 15    |     | 100 | $\mu$ s    |
| $f_{TCK}$ TCK input frequency <sup>(2)</sup>                                                       |                 | 2.2 V      | 0     |     | 5   | MHz        |
|                                                                                                    |                 | 3 V        | 0     |     | 10  | MHz        |
| $R_{Internal}$ Internal pulldown resistance on TEST                                                |                 | 2.2 V, 3 V | 25    | 60  | 90  | k $\Omega$ |

- (1) Tools that access the Spy-Bi-Wire interface must wait for the maximum  $t_{SBW,En}$  time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.  
(2)  $f_{TCK}$  may be restricted to meet the timing requirements of the module selected.

### 9.32 JTAG Fuse <sup>(1)</sup>

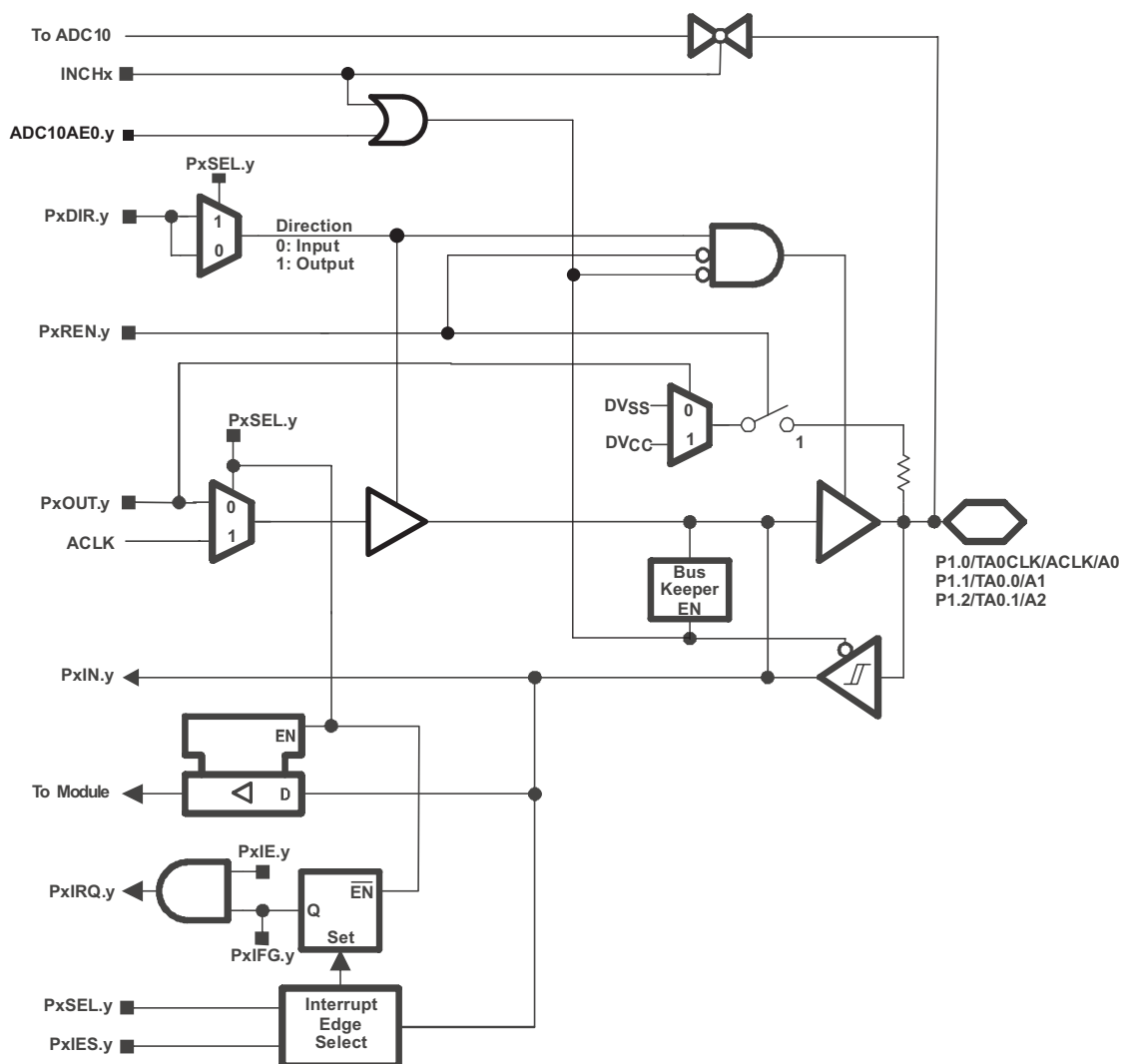
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER                                              | TEST CONDITIONS            | MIN | MAX | UNIT |
|--------------------------------------------------------|----------------------------|-----|-----|------|
| $V_{CC(FB)}$ Supply voltage during fuse-blow condition | $T_A = 25^{\circ}\text{C}$ | 2.5 |     | V    |
| $V_{FB}$ Voltage level on TEST for fuse blow           |                            | 6   | 7   | V    |
| $I_{FB}$ Supply current into TEST during fuse blow     |                            |     | 100 | mA   |
| $t_{FB}$ Time to blow fuse                             |                            |     | 1   | ms   |

- (1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

## 10 I/O Port Schematics

### 10.1 Port P1 Pin Schematic: P1.0 To P1.2, Input/Output With Schmitt Trigger



**Port P1 Pin Schematic: P1.0 To P1.2, Input/Output With Schmitt Trigger (continued)**
**Table 13. Port P1 (P1.0 To P1.2) Pin Functions**

| PIN NAME (P1.x)                 | x | FUNCTION   | CONTROL BITS OR SIGNALS |         |                           |
|---------------------------------|---|------------|-------------------------|---------|---------------------------|
|                                 |   |            | P1DIR.x                 | P1SEL.x | ADC10AE.x<br>(INCH.y = 1) |
| P1.0/<br>TA0CLK/<br>ACLK/<br>A0 | 0 | P1.x (I/O) | I: 0; O: 1              | 0       | 0                         |
|                                 |   | TA0.TACLK  | 0                       | 1       | 0                         |
|                                 |   | ACLK       | 1                       | 1       | 0                         |
|                                 |   | A0         | X                       | X       | 1 (y = 0)                 |
| P1.1/<br>TA0.0/<br><br>A1       | 1 | P1.x (I/O) | I: 0; O: 1              | 0       | 0                         |
|                                 |   | TA0.0      | 1                       | 1       | 0                         |
|                                 |   | TA0.CCI0A  | 0                       | 1       | 0                         |
|                                 |   | A1         | X                       | X       | 1 (y = 1)                 |
| P1.2/<br>TA0.1/<br><br>A2       | 2 | P1.x (I/O) | I: 0; O: 1              | 0       | 0                         |
|                                 |   | TA0.1      | 1                       | 1       | 0                         |
|                                 |   | TA0.CCI1A  | 0                       | 1       | 0                         |
|                                 |   | A2         | X                       | X       | 1 (y = 2)                 |

## 10.2 Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger

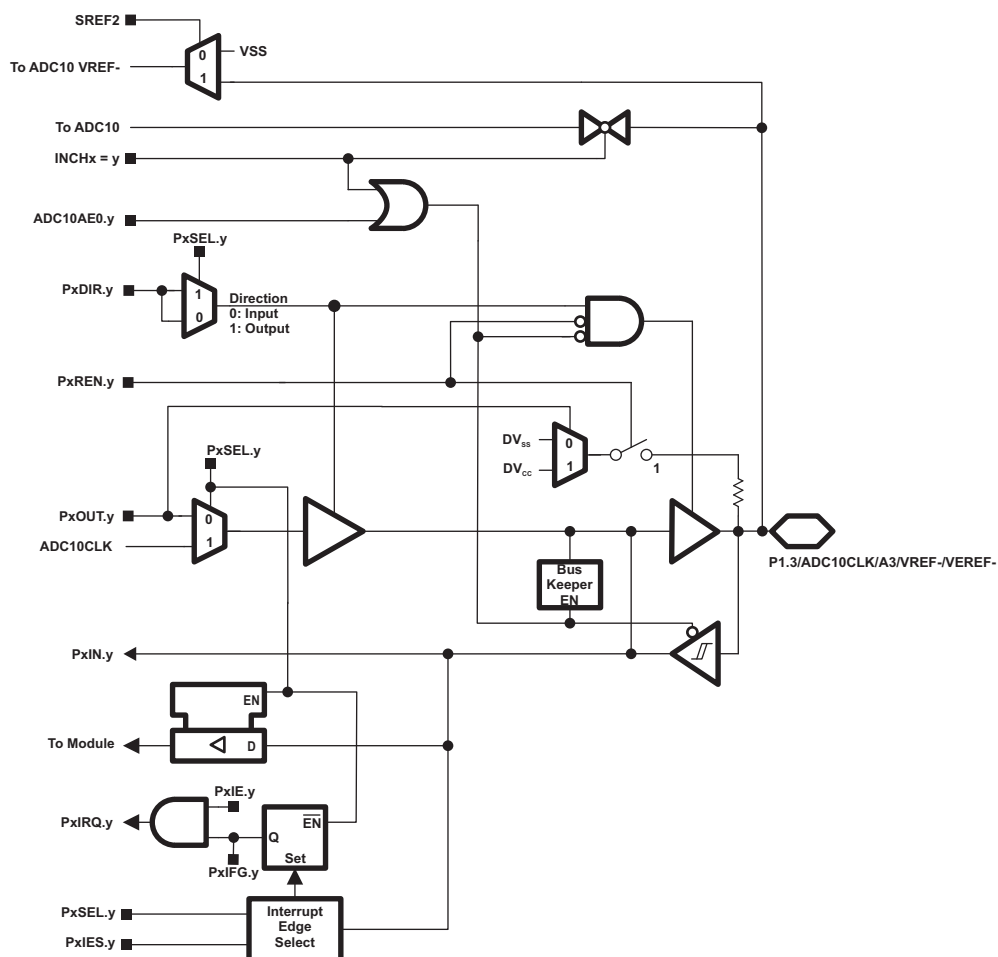


Table 14. Port P1 (P1.3) Pin Functions

| PIN NAME (P1.x)                               | x | FUNCTION   | CONTROL BITS OR SIGNALS |         |                           |
|-----------------------------------------------|---|------------|-------------------------|---------|---------------------------|
|                                               |   |            | P1DIR.x                 | P1SEL.x | ADC10AE.x<br>(INCH.x = 1) |
| P1.3/<br>ADC10CLK/<br>A3/<br>VREF-/<br>VEREF- | 3 | P1.x (I/O) | I: 0; O: 1              | 0       | 0                         |
|                                               |   | ADC10CLK   | 1                       | 1       | 0                         |
|                                               |   | A3         | X                       | X       | 1 (y = 3)                 |
|                                               |   | VREF-      | X                       | X       | 1                         |
|                                               |   | VEREF-     | X                       | X       | 1                         |

### 10.3 Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger

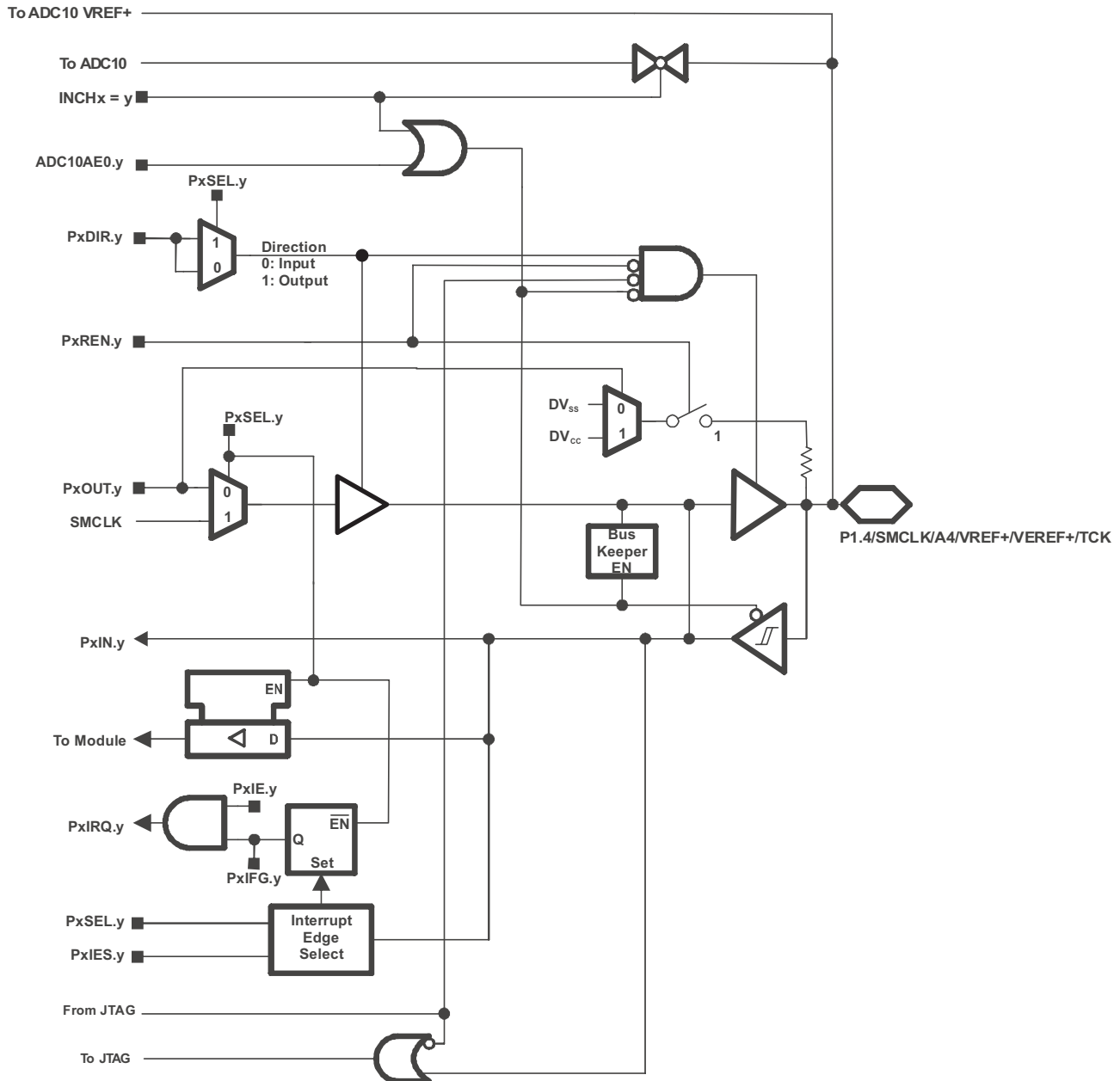


Table 15. Port P1 (P1.4) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION   | CONTROL BITS OR SIGNALS |         |                           |              |
|-----------------|---|------------|-------------------------|---------|---------------------------|--------------|
|                 |   |            | P1DIR.x                 | P1SEL.x | ADC10AE.x<br>(INCH.x = 1) | JTAG<br>Mode |
| P1.4/           | 4 | P1.x (I/O) | I: 0; O: 1              | 0       | 0                         | 0            |
| SMCLK/          |   | SMCLK      | 1                       | 1       | 0                         | 0            |
| A4/             |   | A4         | X                       | X       | 1 (y = 4)                 | 0            |
| VREF+/          |   | VREF+      | X                       | X       | 1                         | 0            |
| VEREF+/         |   | VEREF+     | X                       | X       | 1                         | 0            |
| TCK             |   | TCK        | X                       | X       | 0                         | 1            |

## 10.4 Port P1 Pin Schematic: P1.5, Input/Output With Schmitt Trigger

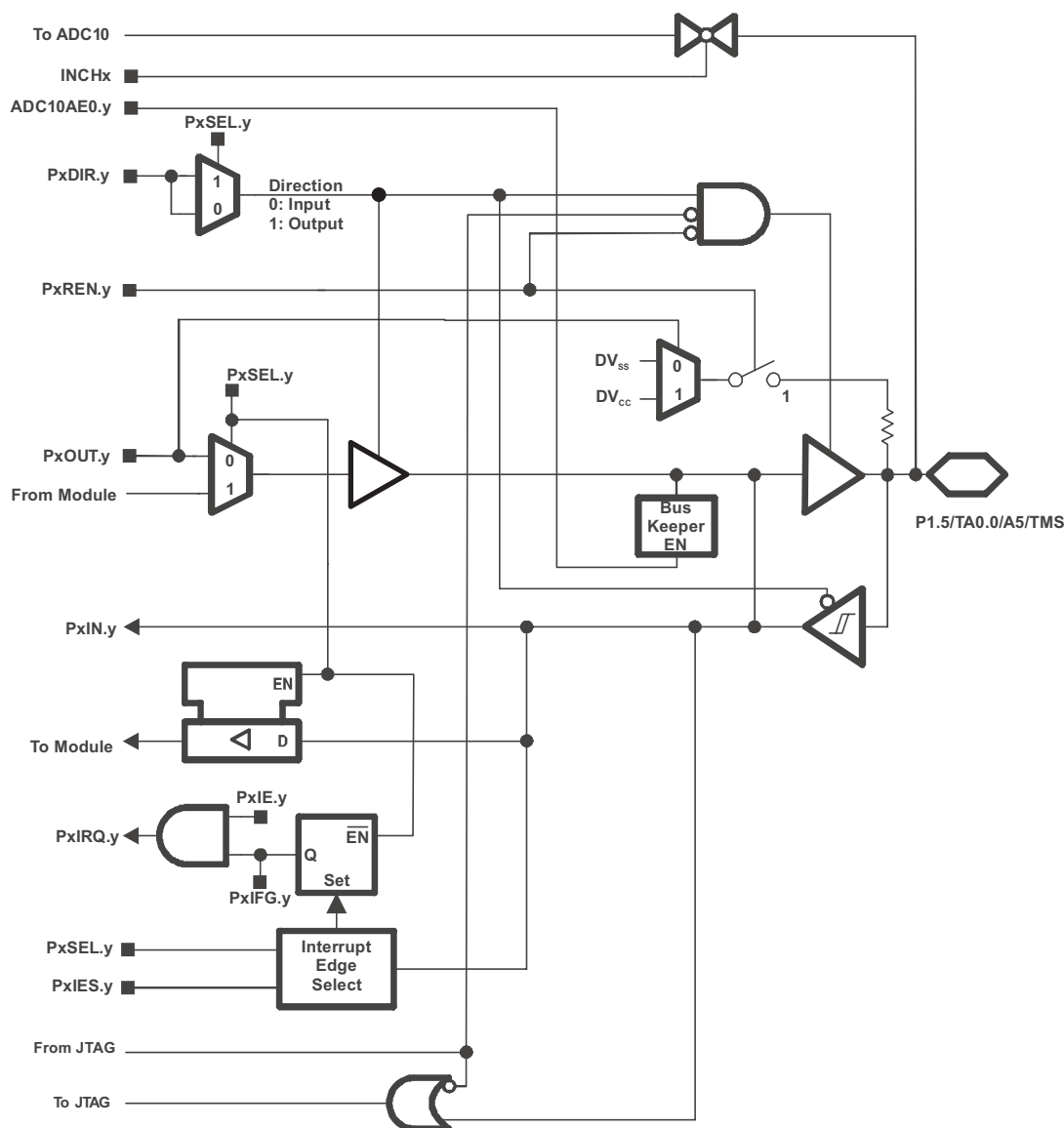
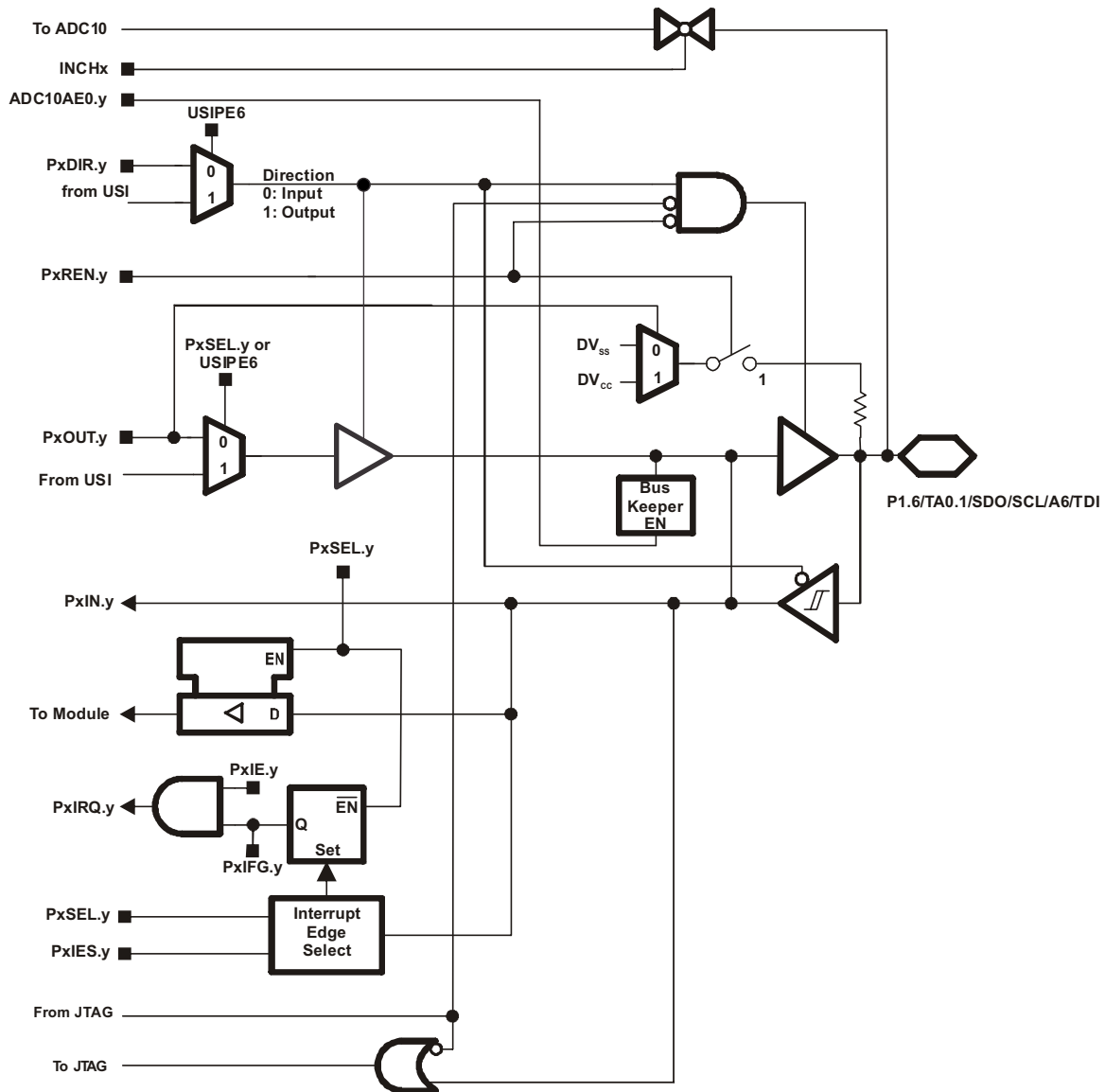


**Table 16. Port P1 (P1.5) Pin Functions**

| PIN NAME (P1.x)                        | x | FUNCTION   | CONTROL BITS OR SIGNALS |         |        |                           |              |
|----------------------------------------|---|------------|-------------------------|---------|--------|---------------------------|--------------|
|                                        |   |            | P1DIR.x                 | P1SEL.x | USIP.x | ADC10AE.x<br>(INCH.x = 1) | JTAG<br>Mode |
| P1.5/<br>TA0.0/<br>A5/<br>SCLK/<br>TMS | 5 | P1.x (I/O) | I: 0; O: 1              | 0       | 0      | 0                         | 0            |
|                                        |   | TA0.0      | 1                       | 1       | 0      | 0                         | 0            |
|                                        |   | A5         | X                       | X       | X      | 1 (y = 5)                 | 0            |
|                                        |   | SCLK       | X                       | X       | 1      | 0                         | 0            |
|                                        |   | TMS        | X                       | X       | 0      | 0                         | 1            |

## 10.5 Port P1 Pin Schematic: P1.6, Input/Output With Schmitt Trigger

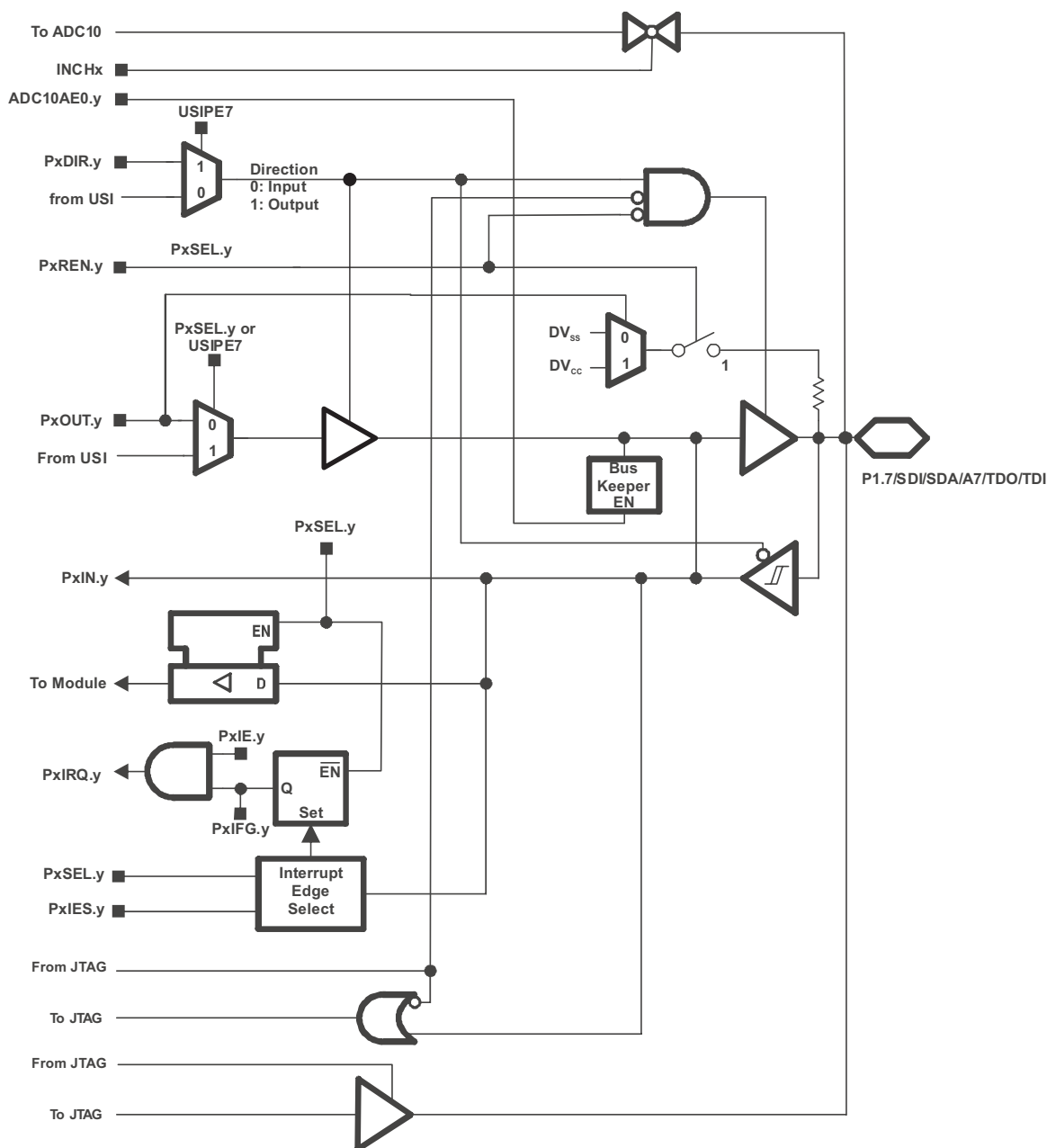


USI in I2C mode: Output driver drives low level only. Driver is disabled in JTAG mode.

Table 17. Port P1 (P1.6) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION   | CONTROL BITS OR SIGNALS |         |        |                           |              |
|-----------------|---|------------|-------------------------|---------|--------|---------------------------|--------------|
|                 |   |            | P1DIR.x                 | P1SEL.x | USIP.x | ADC10AE.x<br>(INCH.x = 1) | JTAG<br>Mode |
| P1.6/<br>TA0.1/ | 6 | P1.x (I/O) | I: 0; O: 1              | 0       | 0      | 0                         | 0            |
|                 |   | TA0.1      | 1                       | 1       | 0      | 0                         | 0            |
|                 |   | TA0.CCR1B  | 0                       | 1       | 0      | 0                         | 0            |
| A6/             |   | A6         | X                       | X       | 0      | 1 (y = 6)                 | 0            |
| SDO/            |   | SDO        | X                       | X       | 1      | 0                         | 0            |
| TDI/TCLK        |   | TDI/TCLK   | X                       | X       | 0      | 0                         | 1            |

## 10.6 Port P1 Pin Schematic: P1.7, Input/Output With Schmitt Trigger



USI in I2C mode: Output driver drives low level only. Driver is disabled in JTAG mode.

**Table 18. Port P1 (P1.7) Pin Functions**

| PIN NAME (P1.x)                    | x | FUNCTION   | CONTROL BITS OR SIGNALS |         |        |                           |              |
|------------------------------------|---|------------|-------------------------|---------|--------|---------------------------|--------------|
|                                    |   |            | P1DIR.x                 | P1SEL.x | USIP.x | ADC10AE.x<br>(INCH.x = 1) | JTAG<br>Mode |
| P1.7/<br>A7/<br>SDI/SDO<br>TDO/TDI | 7 | P1.x (I/O) | I: 0; O: 1              | 0       | 0      | 0                         | 0            |
|                                    |   | A7         | X                       | X       | 0      | 1 (y = 7)                 | 0            |
|                                    |   | SDI/SDO    | X                       | X       | 1      | 0                         | 0            |
|                                    |   | TDO/TDI    | X                       | X       | 0      | 0                         | 1            |

## 10.7 Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger

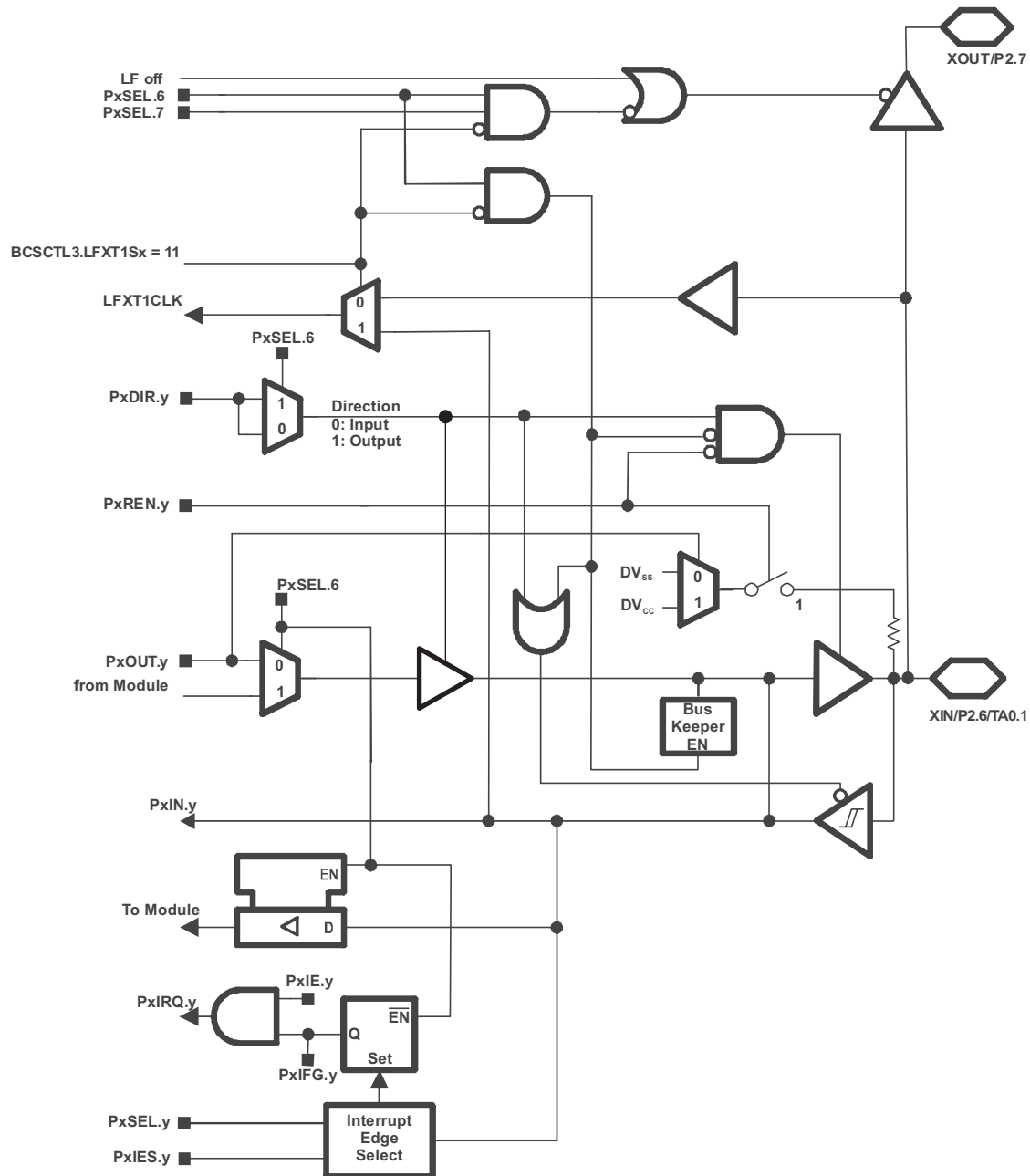


Table 19. Port P2 (P2.6) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION             | CONTROL BITS OR SIGNALS |         |         |
|-----------------|---|----------------------|-------------------------|---------|---------|
|                 |   |                      | P2DIR.x                 | P2SEL.6 | P2SEL.7 |
| XIN             | 6 | XIN                  | 0                       | 1       | 1       |
| P2.6            |   | P2.x (I/O)           | I: 0; O: 1              | 0       | X       |
| TA0.1           |   | TA0.1 <sup>(1)</sup> | 1                       | 1       | X       |

(1) BCSCTL3.LFXT1Sx = 11 is required.

## 10.8 Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

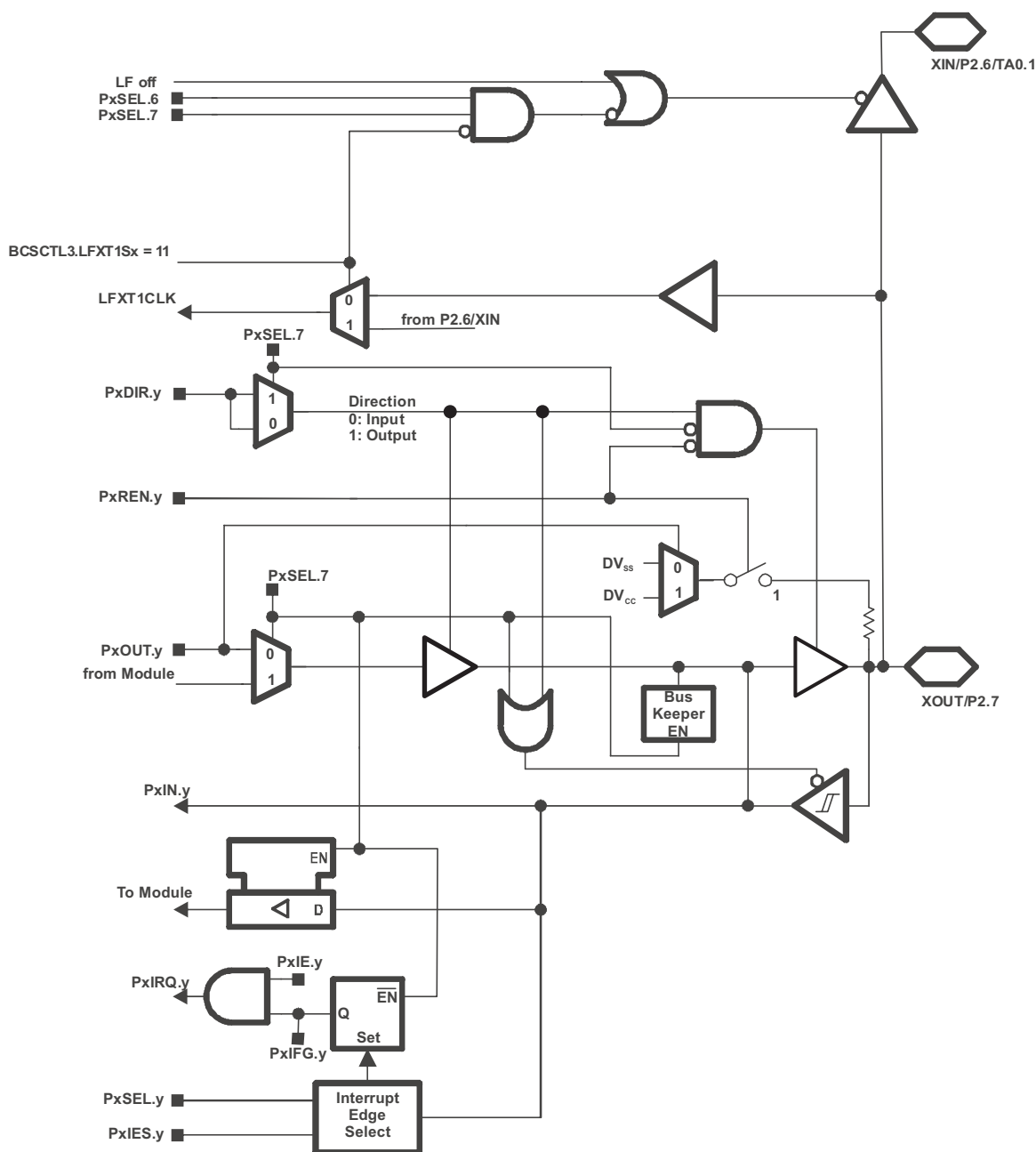


Table 20. Port P2 (P2.7) Pin Functions

| PIN NAME (P2.x) | x | FUNCTION   | CONTROL BITS OR SIGNALS |         |         |
|-----------------|---|------------|-------------------------|---------|---------|
|                 |   |            | P2DIR.x                 | P2SEL.6 | P2SEL.7 |
| XOUT<br>P2.7    | 7 | XOUT       | 1                       | 1       | 1       |
|                 |   | P2.x (I/O) | I: 0; O: 1              | X       | 0       |

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at [www.ti.com/msp430tools](http://www.ti.com/msp430tools).

##### 11.1.1.1 Hardware Features

See the *Code Composer Studio for MSP430 User's Guide* (SLAU157) for details on the available features.

| MSP430 Architecture | 4-Wire JTAG | 2-Wire JTAG | Break-points (N) | Range Break-points | Clock Control | State Sequencer | Trace Buffer | LPMx.5 Debugging Support |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|
| MSP430              | Yes         | Yes         | 2                | No                 | Yes           | No              | No           | No                       |

##### 11.1.1.2 Recommended Hardware Options

###### 11.1.1.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

| Package           | Target Board and Programmer Bundle | Target Board Only              |
|-------------------|------------------------------------|--------------------------------|
| 14-pin TSSOP (PW) | <a href="#">MSP-FET430U14</a>      | <a href="#">MSP-TS430PW14</a>  |
|                   | <a href="#">MSP-FET430U28A</a>     | <a href="#">MSP-TS430PW28A</a> |

###### 11.1.1.2.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See [www.ti.com/msp430tools](http://www.ti.com/msp430tools) for details.

###### 11.1.1.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at [www.ti.com/msp430tools](http://www.ti.com/msp430tools).

###### 11.1.1.2.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

| Part Number              | PC Port        | Features                                                            | Provider          |
|--------------------------|----------------|---------------------------------------------------------------------|-------------------|
| <a href="#">MSP-GANG</a> | Serial and USB | Program up to eight devices at a time. Works with PC or standalone. | Texas Instruments |

##### 11.1.1.3 Recommended Software Options

###### 11.1.1.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available. This device is supported by Code Composer Studio™ IDE (CCS).

###### 11.1.1.3.2 MSP430Ware

[MSP430Ware](#) is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. MSP430Ware is available as a component of CCS or as a standalone package.

#### 11.1.1.3.3 Command-Line Programmer

**MSP430 Flasher** is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 Flash without the need for an IDE.

#### 11.1.1.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

##### [TI E2E Community](#)

*TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

##### [TI Embedded Processors Wiki](#)

*Texas Instruments Embedded Processors Wiki.* Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

#### 11.1.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430™ MCU devices and support tools. Each MSP430™ MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430F5259). Texas Instruments recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**PMS** – Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

**MSP** – Fully qualified production device

Support tool development evolutionary flow:

**MSPX** – Development-support product that has not yet completed Texas Instruments internal qualification testing.

**MSP** – Fully-qualified development-support product

XMS and PMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS and PMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). [Figure 17](#) provides a legend for reading the complete device name for any family member.

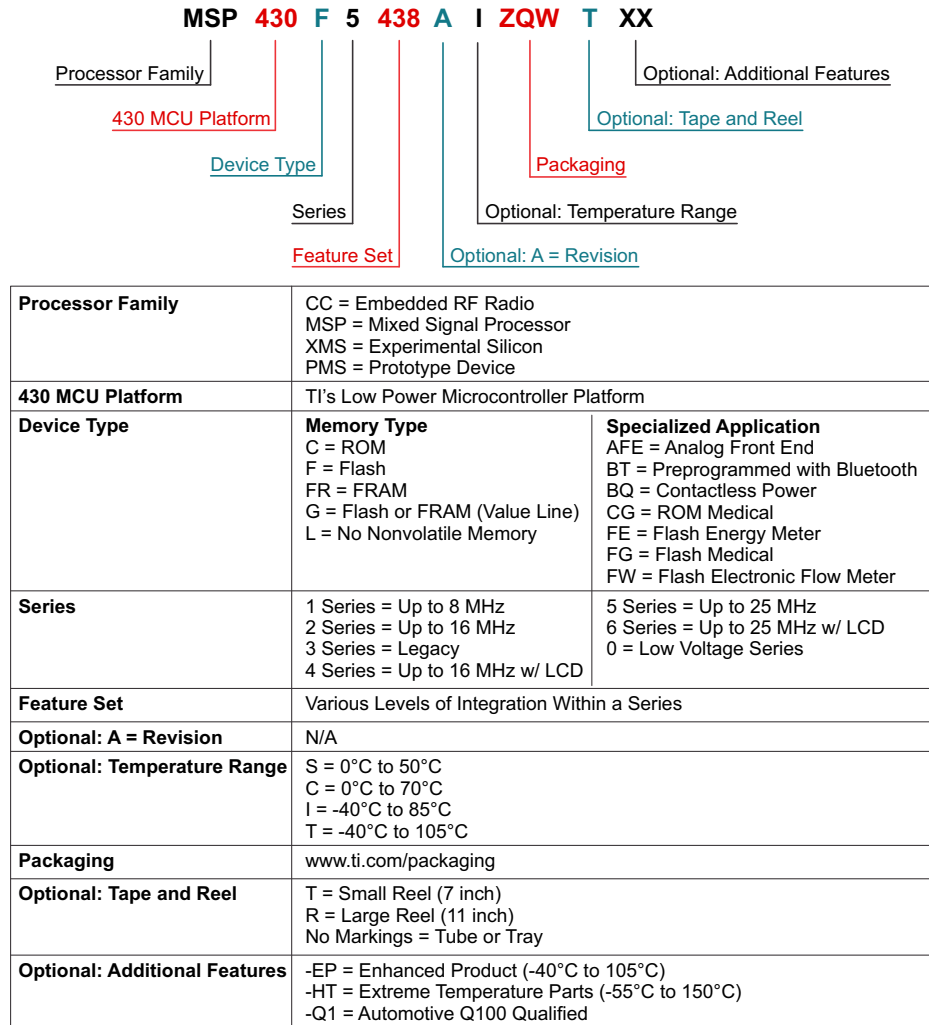


**Figure 17. Device Nomenclature**

## 11.2 Documentation Support

### 11.2.1 Related Documents

The following documents describe the MSP430G2231 device. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com).

**SLAU144 MSP430x2xx Family User's Guide.** Detailed information on the modules and peripherals available in this device family.

**SLA2417 MSP430G2231 Device Erratasheet.** Describes the known exceptions to the functional specifications for the MSP430G2231 device.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### TI E2E Community

*TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

## Community Resources (continued)

### [TI Embedded Processors Wiki](#)

*Texas Instruments Embedded Processors Wiki*. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 11.4 Trademarks

MSP430, Code Composer Studio are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">MSP430G2231IPW4RQ1</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2231Q1             |
| MSP430G2231IPW4RQ1.B               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | G2231Q1             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF MSP430G2231-Q1 :

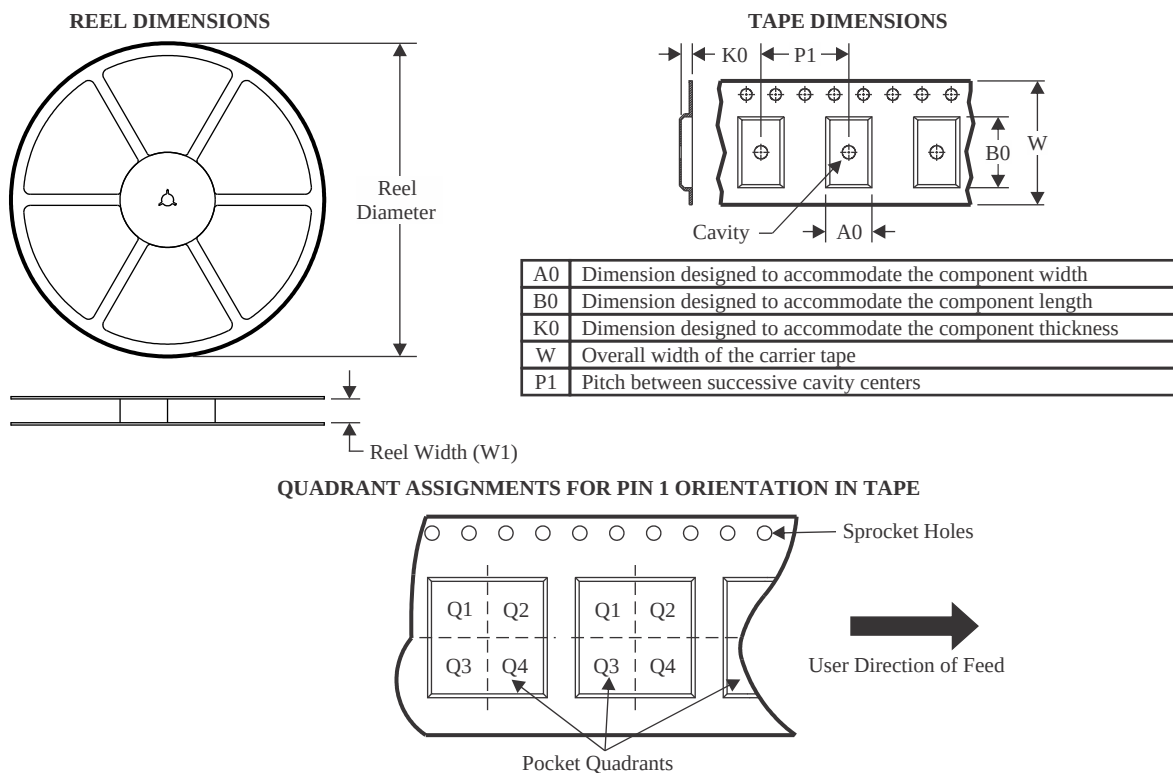
- Catalog : [MSP430G2231](#)

- Enhanced Product : [MSP430G2231-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

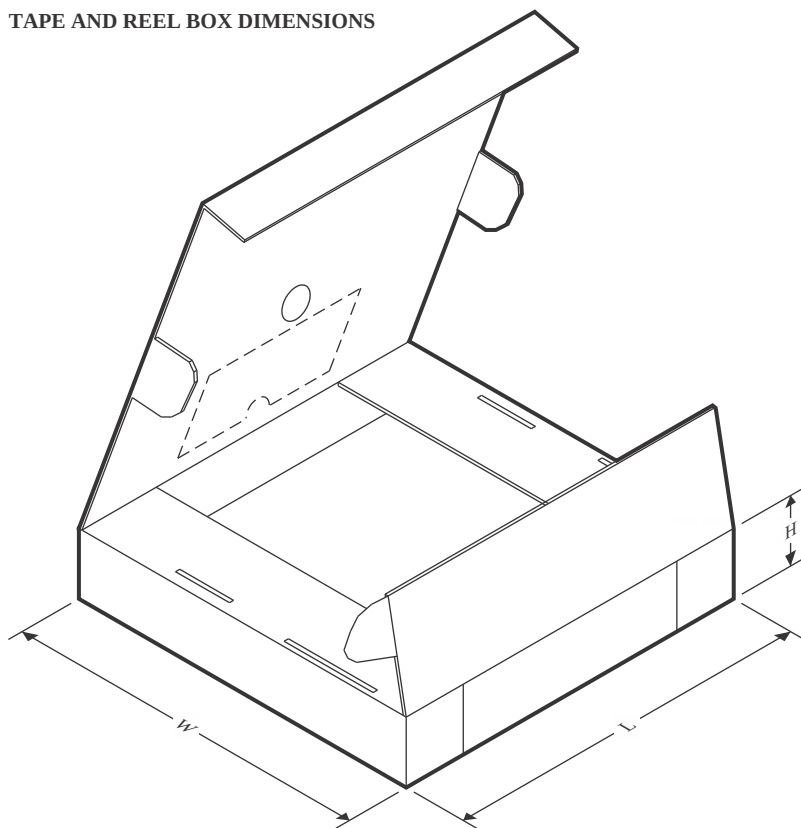
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

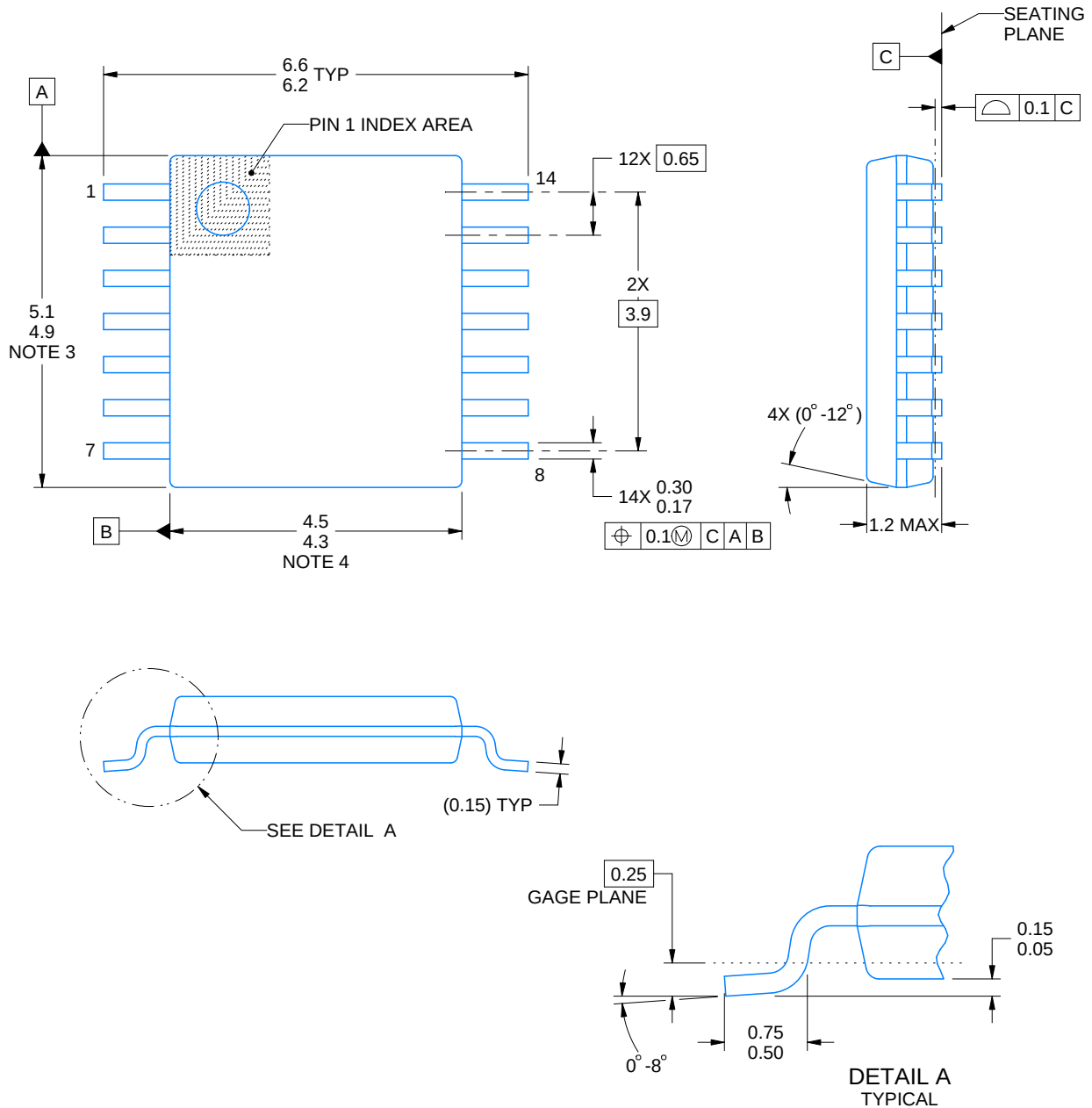
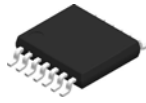
| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430G2231IPW4RQ1 | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430G2231IPW4RQ1 | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |



4220202/B 12/2023

## NOTES:

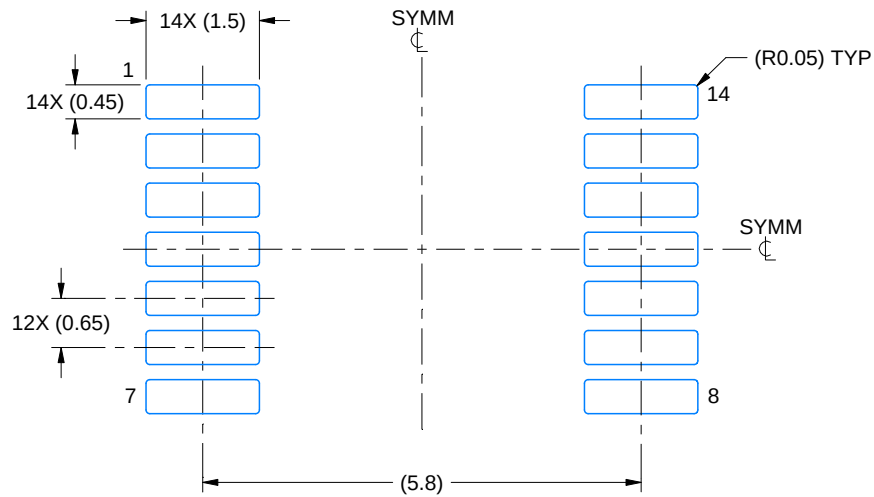
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

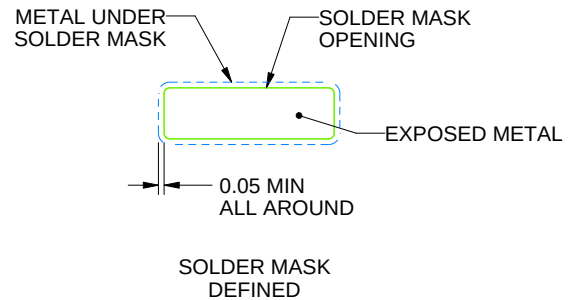
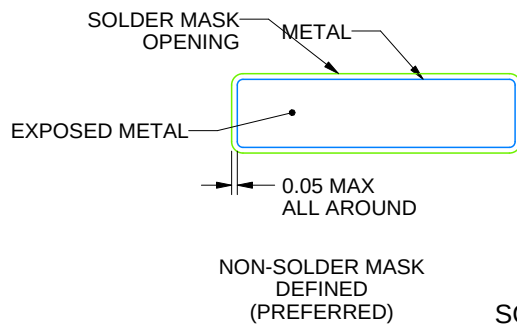
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

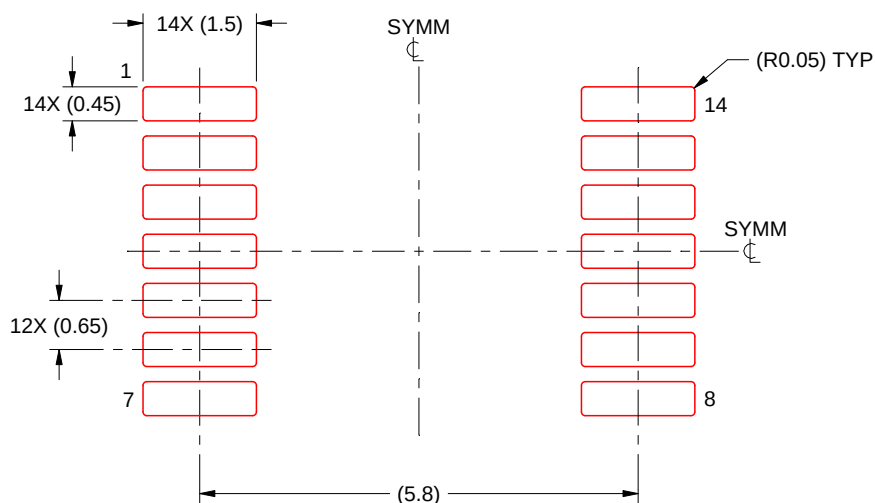
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated