TLC694x 16-Channel 32-, 48-Multiplexing 16-Bit ES-PWM Constant-Current LED Driver

1 Features

- Power Supply Voltage Ranges
  - V_{CC} Voltage Range: 3 V to 5.5 V
  - V_{LED} Voltage Range: Up to V_{CC} + 0.3 V
- 16 Constant-Current-Sink Channels
  - 0.3 mA to 25 mA (3 V ≤ V_{CC} ≤ 5.5 V)
  - Channel Current Deviation: ±1% (typical)
  - Device Current Deviation: ±1% (typical)
  - Low Knee Voltage: 0.3 V (typical) at 10 mA
- 7-Bit (128 Steps) Global Brightness Control (BC)
- 16-Bit (65,536 Steps) Enhanced Spectrum PWM Grayscale Control
- Built-In Memory Supports 32 Multiplexing for TLC6946 and 48 Multiplexing for TLC6948
- LED Display Performance Enhancement
  - Low-Grayscale Uniformity Improvement
  - Low-Grayscale Coupling Issue Elimination
  - Ghosting Removal and Caterpillar Elimination
- High-Speed Serial-Data Interface
  - Data-Shift Clock: 33 MHz (maximum)
  - Grayscale Control Clock: 33 MHz (maximum)
  - Supports Dual-Edge Grayscale Control
- Diagnostics and Protection
  - LED-Open Detection (LOD)
  - IREF Resistor Short Protection (ISP)
  - Thermal Shutdown (TSD)
- Smart Power-Save Mode

2 Applications

- Mono-Color, Multi-Color, Full-Color LED Displays
- High-Refresh-Rate LED Video Displays
- High-Density, Fine-Pitch LED Matrix Displays

3 Description

In high-density, fine-pitch LED panel applications, the performance demand for multi-channel LED drivers is increasing to achieve high multiplexing, high PWM resolution, and high refresh rates. To meet strict display quality requirements, the LED drivers must have the ability to solve various issues in different LED-matrix application scenarios.

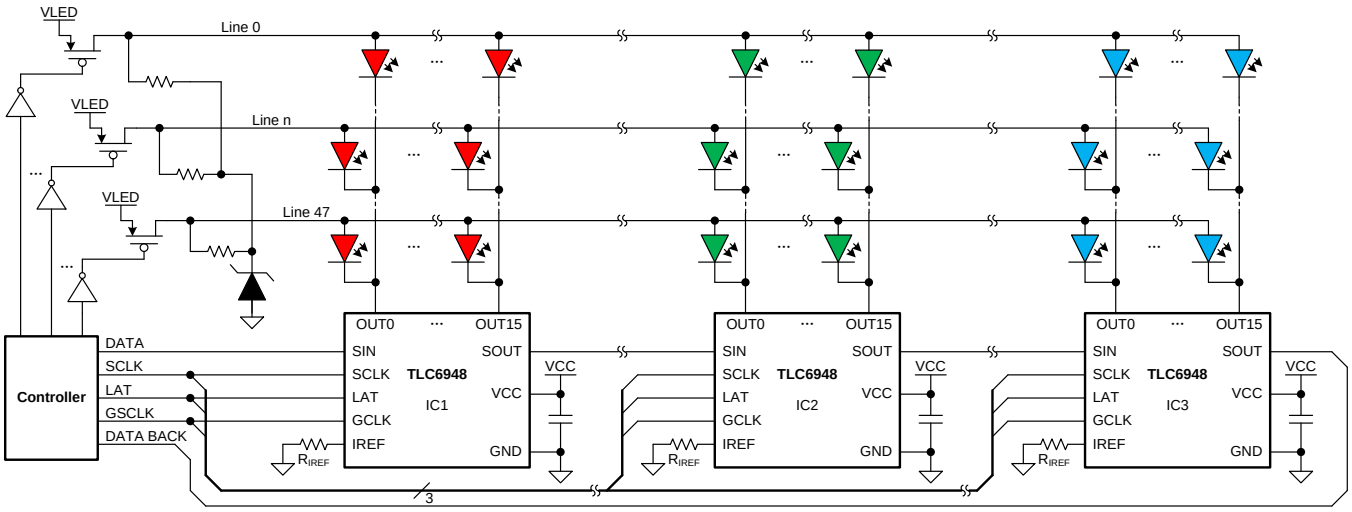
The TLC694x device is a 16-channel, constant-current-sink LED driver. Each channel has an individually adjustable 65,536 steps of PWM grayscale control. The maximum constant-current value of all 16 channels is set by a single external resistor with 128 steps of global brightness control from 0.3 mA to 25 mA.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC6946	SSOP (24)	8.65 mm × 3.90 mm
	VQFN (24)	4.00 mm × 4.00 mm
TLC6948	SSOP (24)	8.65 mm × 3.90 mm
	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic of TLC6948 With 48-Multiplexing



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (June 2018) to Revision A	Page
• First release of production-data data sheet	1

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5 Description (continued)

The TLC694x device integrates enhanced circuits to solve the various display issues in fine-pitch LED display applications: the low-grayscale uniformity issue, coupling issue, ghosting issue, and caterpillar issue.

The TLC694x device features an LED-open detection function, and the error detection results can be read via a serial data interface port. Thermal shutdown and IREF resistor short protection ensure a higher system reliability. The TLC694x device also has an smart power-save mode that sets the total current consumption to 1 mA (typical) when all outputs are off.

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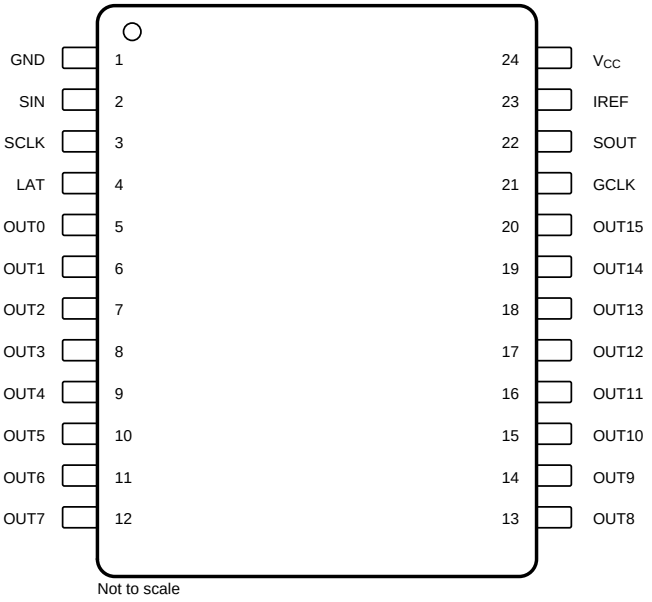
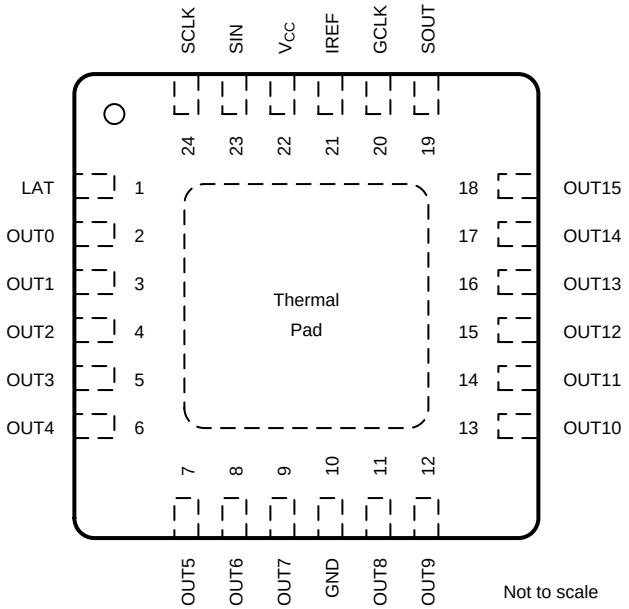
6 Pin Configuration and Functions

DBQ Package
24-Pin SSOP
Top View



RGE Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DBQ	RGE		
GCLK	21	20	I	Grayscale (GS) pulse-width modulation (PWM) reference-clock-signal input pin. In the default operating mode, each GCLK rising edge increments the GS counter for PWM control. GCLK supports dual-edge operation.
GND	1	10	—	Power-ground reference
IREF	23	21	I	Pin for setting the maximum constant-current value. Connecting an external resistor between IREF and GND sets the maximum current for each constant-current output channel. When this pin is connected directly to GND, all outputs are forced off. The external resistor should be placed close to the device.
LAT	4	1	I	Data latch pin. The falling edge of LAT latches the data from the common shift register into the GS data memory or the function control register.

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Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	DBQ	RGE		
OUT0	5	2	O	Constant-current output. Each output can be tied together with others to increase the constant current. A different voltage can be applied to each output.
OUT1	6	3	O	
OUT2	7	4	O	
OUT3	8	5	O	
OUT4	9	6	O	
OUT5	10	7	O	
OUT6	11	8	O	
OUT7	12	9	O	
OUT8	13	11	O	
OUT9	14	12	O	
OUT10	15	13	O	
OUT11	16	14	O	
OUT12	17	15	O	
OUT13	18	16	O	
OUT14	19	17	O	
OUT15	20	18	O	
SCLK	3	24	I	Clock-signal input pin. Serial data present on SIN are shifted to the LSB of the internal 16-bit common shift register on the SCLK rising edge. All data in the shift register are shifted toward the MSB of the internal 16-bit common shift register on each SCLK rising edge.
SIN	2	23	I	Serial-data input pin of the internal 16-bit common shift register. When SIN is high, the LSB of the internal 16-bit common shift register is set to 1 on the SCLK input rising edge. When SIN is low, the LSB of the internal 16-bit common shift register is set to 0 on the SCLK input rising edge.
SOUT	22	19	O	Serial data output pin of the internal 16-bit common shift register. The MSB of the internal 16-bit common shift register appears on SOUT.
V_{CC}	24	22	I	Power supply pin
Thermal pad	—	—	—	Internally connected to GND in the RGE package only. The thermal pad and the GND pin must be connected together on the board.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1) (2)]

		MIN	MAX	UNIT
Voltage	V_{CC}	–0.3	6	V
	GCLK, IREF, LAT, SCLK, SIN, SOUT	–0.3	V_{CC} + 0.3	V
	OUT0 to OUT15	–0.3	V_{CC} + 0.3	V
Current	OUT0 to OUT15	0	27	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) All voltage values are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±7000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Supply voltage	3		5.5	V
V_{OUTn}	Voltage applied to OUT0 to OUT15	Voltage applied to OUT0 to OUT15	0		VCC	V
VIH	High-level input voltage	GCLK, LAT, SCLK, SIN	0.7 × VCC		VCC	V
V_{IL}	Low-level input voltage	GCLK, LAT, SCLK, SIN	0		0.3 × VCC	V
I_{OH}	High-level output current	SOUT			–2	mA
I_{OL}	Low-level output current	SOUT			2	mA
$I_{OLC,max}$	Maximum constant-output sink current	OUT0 to OUT15	0.3		25	mA
f_{SCLK}	Data-shift clock frequency	SCLK			33	MHz
f_{GCLK}	Grayscale control clock frequency	GCLK			33	MHz
$f_{GCLK,B}$	Grayscale control clock frequency for dual-edge operation	GCLK			25	MHz
$t_{w(H0)}$	Pulse width duration	SCLK	10			ns
$t_{w(L0)}$	Pulse width duration	SCLK	10			ns
$t_{w(H1)}$	Pulse width duration	GCLK	10			ns
$t_{w(L1)}$	Pulse width duration	GCLK	10			ns
$t_{w(H2)}$	Pulse width duration	GCLK (for dual-edge operation)	18			ns
$t_{w(L2)}$	Pulse width duration	GCLK (for dual-edge operation)	18			ns
$t_{su(0)}$	Setup time	SIN to SCLK↑	2			ns
$t_{su(1)}$	Setup time	LAT ↑ to SCLK ↑	5			ns
$t_{su(2)}$	Setup time	LAT ↓ to SCLK ↑	5			ns
$t_{su(3)}$	Setup time	LAT ↓ to SCLK ↑ ,read data from SOUT	50			ns
$t_{su(4)}$	Setup time	LAT ↓ (WRTGS) to LAT ↓ (WRTGS)	1.5			µs

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Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{su(5)}$	Setup time	LAT ↓ (WRTGS) to LAT ↓ (VSYNC)	1.5			µs
$t_{su(6)}$	Setup time	LAT ↓ (VSYNC) to GCLK ↑	2.5			µs
$t_{su(7)}$	Setup time	LAT ↓ (VSYNC) to LAT ↓ (WRTGS)	2.5			µs
$t_{su(8)}$	Setup time	Last LAT (non-0 GS data latched) ↓ to the first GCLK ↑ of next frame (wake up from power-save mode)	50			µs
t_{LSW}	Line switching time	Last GCLK ↓ to the first GCLK ↑ of next line	1			µs
$t_{h(0)}$	Hold time	SCLK ↑ to SIN	2			ns
$t_{h(1)}$	Hold time	SCLK ↑ to LAT ↑	2			ns
$t_{h(2)}$	Hold time	SCLK ↑ to LAT ↓	10			ns
T_A	Operating ambient temperature	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TLC6946		UNIT
		DBQ (SSOP)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.2	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	34.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.4	15.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41	15.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	5	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{CC} = 3 V to 5.5 V and T_A = –40°C to 85°C; typical values are at V_{CC} = V_{LED} = 3.5 V, T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA at SOUT			0.4	V
V_{IREF}	Reference voltage	BC = 00h, R_{IREF} = 10.7 kΩ (I_{OUTn} = 0.3-mA target)		0.8		V
$V_{(LOD)}$	LED open-detection threshold	All OUTn = on, LODVTH = 00b	0.12	0.2	0.28	V
		All OUTn = on, LODVTH = 01b	0.42	0.5	0.58	V
		All OUTn = on, LODVTH = 10b	0.82	0.9	0.98	V
		All OUTn = on, LODVTH = 11b	1.12	1.2	1.28	V
$V_{(KNEE)}$	Knee voltage (OUT0 to OUT15)	All OUTn = on, BC = 36h, R_{IREF} = 1.27 kΩ (I_{OUTn} = 10-mA target)		0.3		V
ΔIOLC0	Constant-current error (channel-to-channel)[1]	All OUTn = on, BC = 00h,V_{OUTn} = 1 V, R_{IREF} = 10.7 kΩ (I_{OUTn} = 0.3-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±3.5%	

(1) The deviation of each output from average of all channels constant current. The deviation is calculated by the formula.

$$\Delta(\%) = \left[\frac{\text{IOUTn}}{\frac{\text{IOUT0}+\text{IOUT1}+\ldots+\text{IOUT14}+\text{IOUT15}}{16}} - 1\right] \times 100$$

Electrical Characteristics (continued)

V_{CC} = 3 V to 5.5 V and T_A = –40°C to 85°C; typical values are at V_{CC} = V_{LED} = 3.5 V, T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC1}	Constant-current error (device-to-device)(2)	All OUTn = on, BC = 00h, V_{OUTn} = 1 V, R_{IREF} = 10.7 kΩ (I_{OUTn} = 0.3-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±2%	
ΔI_{OLC2}	Constant-current error (channel-to-channel)(1)	All OUTn = on, BC = 2Ah, V_{OUTn} = 1 V, R_{IREF} = 10.7 kΩ (I_{OUTn} = 1-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±3%	
ΔI_{OLC3}	Constant-current error (device-to-device)(2)	All OUTn = on, BC = 2Ah, V_{OUTn} = 1 V, R_{IREF} = 10.7 kΩ (I_{OUTn} = 1-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±2.5%	
ΔI_{OLC4}	Constant-current error (channel-to-channel)(1)	All OUTn = on, BC = 36h, V_{OUTn} = 1 V, R_{IREF} = 1.27 kΩ (I_{OUTn} = 10-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±2.5%	
ΔI_{OLC5}	Constant-current error (device-to-device)(2)	All OUTn = on, BC = 36h, V_{OUTn} = 1 V, R_{IREF} = 1.27 kΩ (I_{OUTn} = 10-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±2.5%	
ΔI_{OLC6}	Constant-current error (channel-to-channel)(1)	All OUTn = on, BC = 7Eh, V_{OUTn} = 1 V, R_{IREF} = 1.02 kΩ (I_{OUTn} = 25-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±2%	
ΔI_{OLC7}	Constant-current error (device-to-device)(2)	All OUTn = on, BC = 7Eh, V_{OUTn} = 1 V, R_{IREF} = 1.02 kΩ (I_{OUTn} = 25-mA target), T_A = 25°C, includes the V_{IREF} tolerance		±1%	±2%	
ΔI_{OLC8}	Line regulation(3)	All OUTn = on, V_{CC} = 3 V to 5.5 V, V_{OUTn} = 1 V		±1	±2	%/V
ΔI_{OLC9}	Load regulation(4)	All OUTn = on, V_{OUTn} = 1 V to 3 V		±1	±2	%/V
$V_{IL(ISP)}$	IREF resistor short-protection enter threshold		0.15	0.195		V
$V_{IH(ISP)}$	IREF resistor short-protection release threshold			0.325	0.4	V
$T_{(TSD)}$	Thermal shutdown threshold(5)			170		°C
$T_{(HYS)}$	Thermal shutdown hysteresis(5)			15		°C
I_I	SCLK or SIN Input current	V_I = V_{CC} or GND at SCLK or SIN	–1		1	µA

(2) The deviation of the average of constant current from the ideal constant current value.

$$\Delta(\%) = \left[\frac{\frac{IOUT0 + IOUT1 + ... + IOUT14 + IOUT15}{16} - \text{Ideal Output Current}}{\text{Ideal Output Current}}\right] \times 100$$

,Ideal current is calculated by the following equation

$$\text{Ideal Output}(mA) = \text{Gain} \times \left(\frac{V_{IREF}}{R_{IREF(\Omega)}}\right) \times \left(\frac{1}{8} + \frac{BC}{144}\right)$$

(3) Line regulation is calculated by the following equation

$$\Delta(\%V) = \left[\frac{(IOUTn \text{ at } VCC = 5.5V) - (IOUTn \text{ at } VCC = 3V)}{(IOUTn \text{ at } VCC = 3V)}\right] \times \frac{100}{5.5V - 3V}$$

(4) Load regulation is calculated by the following equation

$$\Delta(\%V) = \left[\frac{(IOUTn \text{ at } VOUTn = 3V) - (IOUTn \text{ at } VOUTn = 1V)}{(IOUTn \text{ at } VOUTn = 1V)}\right] \times \frac{100}{3V - 1V}$$

(5) Specified by design

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Electrical Characteristics (continued)

V_{CC} = 3 V to 5.5 V and T_A = –40°C to 85°C; typical values are at V_{CC} = V_{LED} = 3.5 V, T_A = 25°C, over recommended operating conditions (unless otherwise noted)

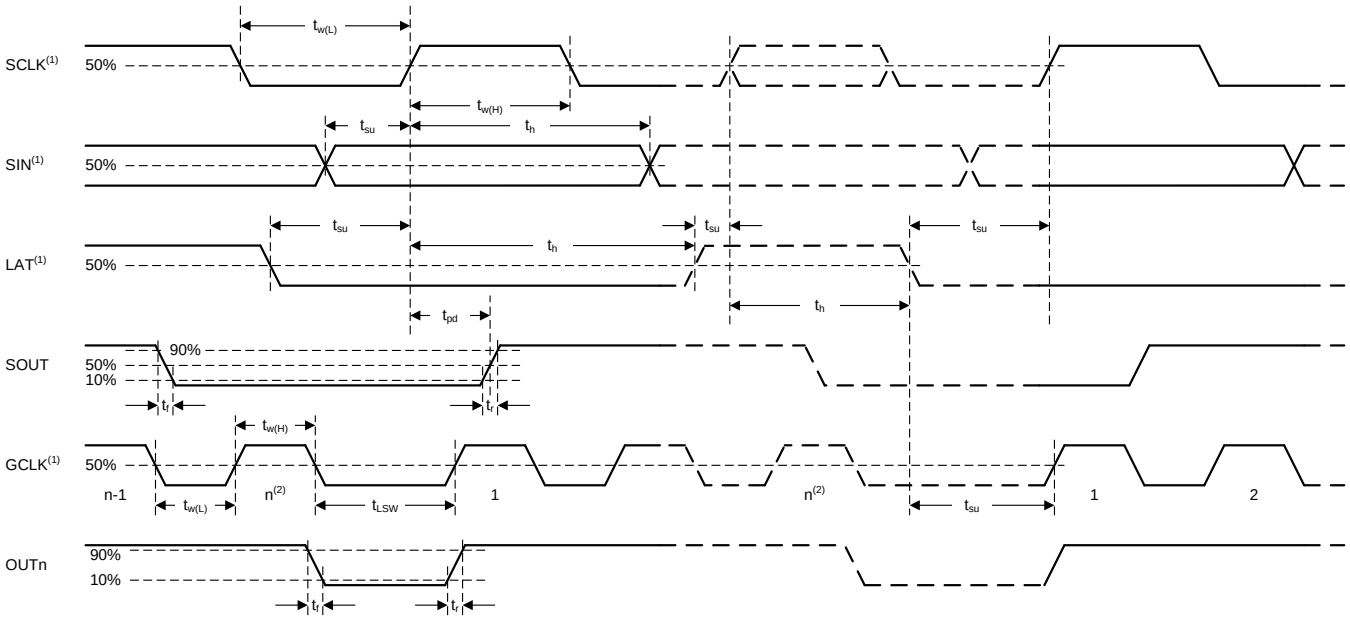
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(0)}$	Supply current(5)	GCLK = LAT = SCLK = SIN = GND, GSn = 0000h, BC = 00h, PCHG_EN = 0, V_{OUTn} = V_{CC}, R_{IREF} = open	3	4.5	6	mA
$I_{CC(1)}$		GCLK = LAT = SCLK = SIN = GND, GSn = 0000h, BC = 36h, PCHG_EN = 0, V_{OUTn} is floating, R_{IREF} = 1.27 kΩ (I_{OUTn} = 10-mA target)	4	6.5	8	mA
$I_{CC(2)}$		GCLK = LAT = SCLK = SIN = GND, GSn = 0000h, BC = 7Eh, PCHG_EN = 0, V_{OUTn} is floating, R_{IREF} = 1.27 kΩ (I_{OUTn} = 20-mA target)	4	7.5	9	mA
$I_{CC(3)}$		LAT = SCLK = SIN = GND, GCLK = 33 MHz, GSn = FFFFh, BC = 36h, PCHG_EN = 0, V_{OUTn} = 1 V, R_{IREF} = 1.27 kΩ (I_{OUTn} = 10-mA target)	4.7	7	10	mA
$I_{CC(4)}$		LAT = SCLK = SIN = GND, GCLK = 33 MHz, GSn = FFFFh, BC = 7Eh, PCHG_EN = 0, V_{OUTn} = 1 V, R_{IREF} = 1.27 kΩ (I_{OUTn} = 20-mA target)	4.7	7.7	10	mA
$I_{CC(6)}$		In power-save mode, PCHG_EN = 0, R_{IREF} = 1.60 kΩ		1	1.5	mA
R_{DW}	Pulldown resistor	LAT	250	480	750	kΩ
		GCLK	250	480	750	

7.6 Switching Characteristics

V_{CC} = 3 V to 5.5 V and T_A = –40°C to85°C; Typical values are at V_{CC} = 3.3 V, T_A = 25°C,V_{LED} = 5 V, over recommended operating conditions (unless otherwisenoted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(0)}$	Rise time(1)	SOUT		2		ns
$t_{r(1)}$		OUTn, BC = 7Eh, V_{OUTn} = 1 V, R_{IREF} = 1.02 kΩ (I_{OUTn} = 25-mA target), T_A = 25°C, R_L = 160 Ω		20		ns
$t_{f(0)}$	Fall time(1)	SOUT		2		ns
$t_{f(1)}$		OUTn, BC = 7Eh, V_{OUTn} = 1 V, R_{IREF} = 1.02 kΩ (I_{OUTn} = 25-mA target), T_A = 25°C, R_L = 160 Ω		15		ns
$t_{pd(0)}$	Propagation delay(1)	SCLK↑ to SOUT↑↓, SEL_TD0 = 00b		5		ns
		SCLK↑ to SOUT↑↓, SEL_TD0 = 01b		10		ns
		SCLK↑ to SOUT↑↓, SEL_TD0 = 10b		20		ns
		SCLK↓ to SOUT↑↓, SEL_TD0 = 11b		5		ns
$t_{pd(1)}$		LAT↓ to SOUT, read LOD information		25	50	ns

(1) Specified by design



(1) Pulse rise and fall times are 1 ns–3 ns

(2) The last GCLK of each display segment in the sub period

Figure 1. Timing Diagram

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7.7 Typical Characteristics

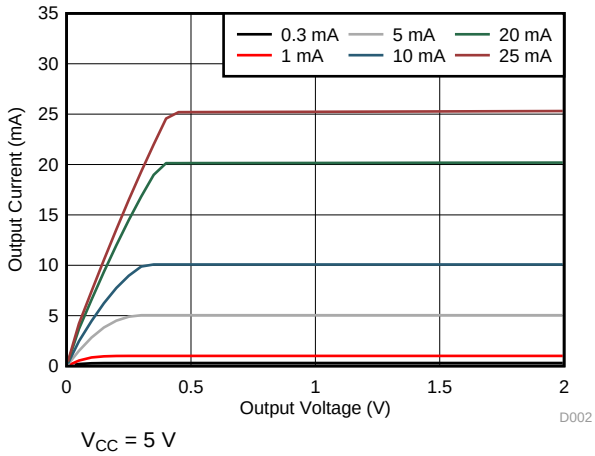


Figure 2. Channel Sink Current vs OUTn Voltage

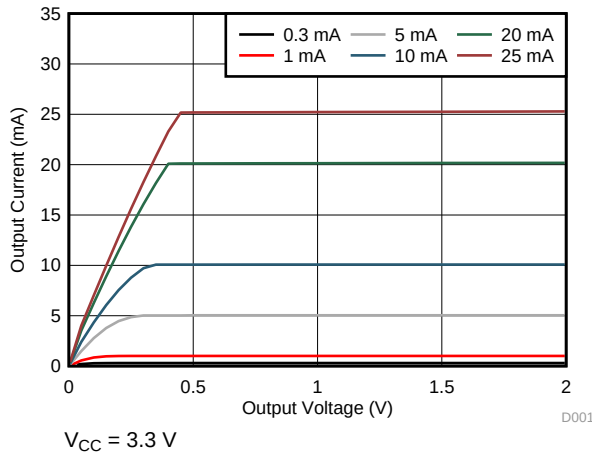


Figure 3. Channel Sink Current vs OUTn Voltage

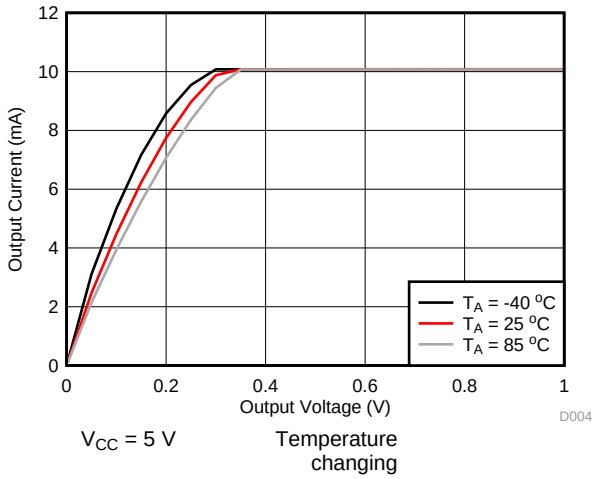


Figure 4. Channel Sink Current vs OUTn Voltage

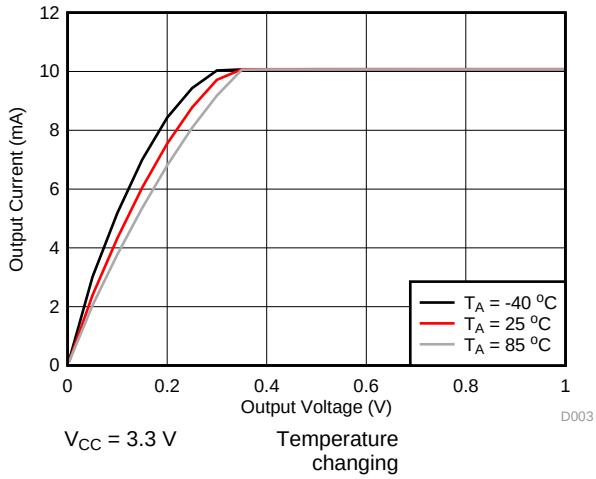


Figure 5. Channel Sink Current vs OUTn Current

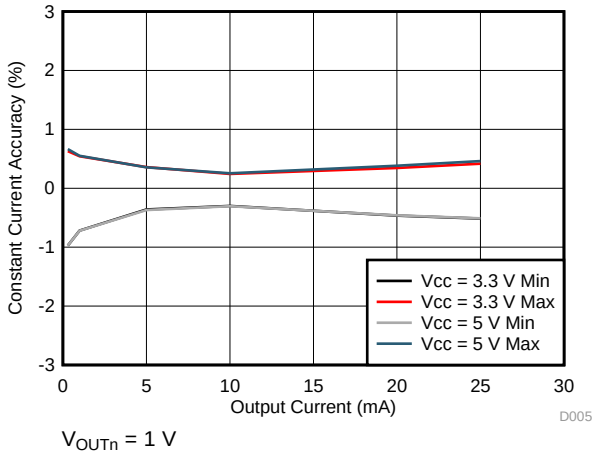


Figure 6. Channel to Channel Accuracy vs OUTn Current

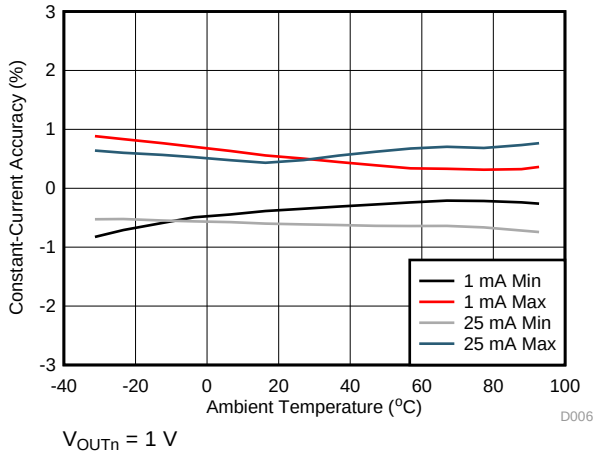
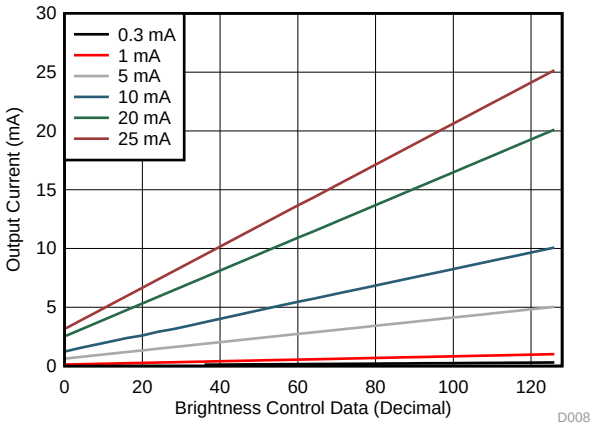


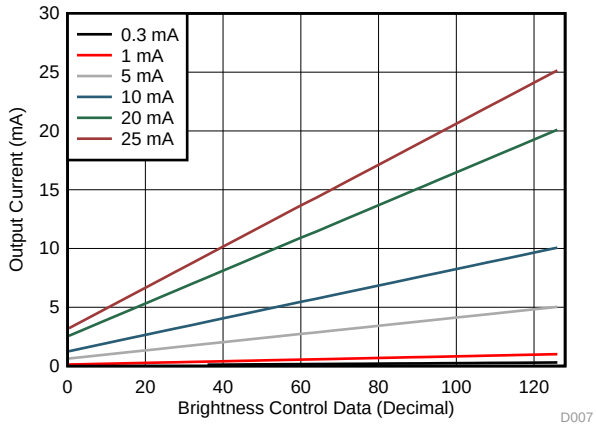
Figure 7. Channel to Channel Accuracy vs Temperature

Typical Characteristics (continued)



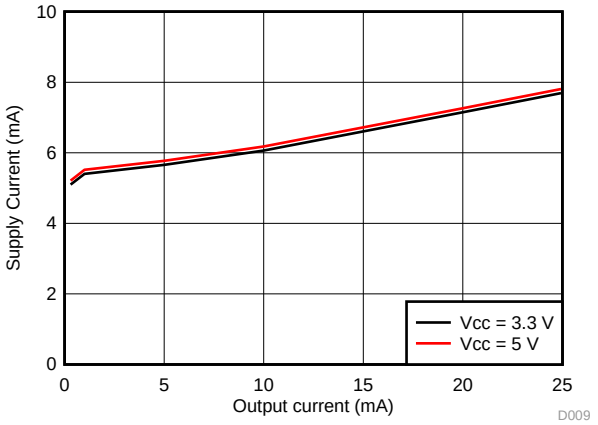
V_{CC} = 5 V V_{OUTn} = 1 V

Figure 8. Channel Sink Current vs Brightness Control (BC)



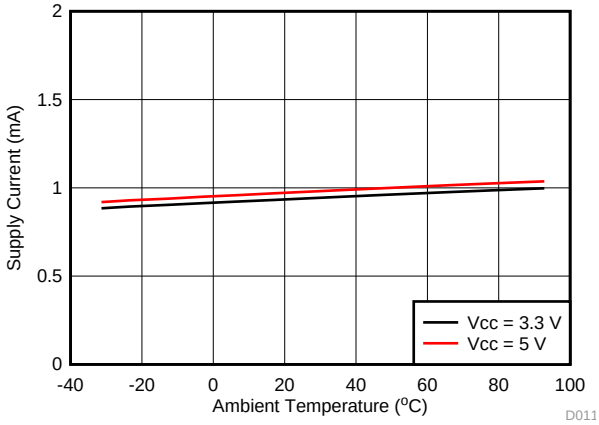
V_{CC} = 3.3 V V_{OUTn} = 1 V

Figure 9. Channel Sink Current vs Brightness Control (BC)



V_{OUTn} = 1 V GCLK = 33 MHz GSn = FFFFh

Figure 10. Supply Current (I_{CC}) vs Channel Sink Current



V_{OUTn} = 1 V GCLK = 33 MHz GSn = 0000h
BC = 36h R_{IREF} = 1.27 kΩ (10-mA target)

Figure 11. Supply Current (I_{CC}) in Power-Save Mode vs Temperature

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8 Parameter Measurement Information

8.1 Pin Equivalent Input and Output Schematic Diagrams

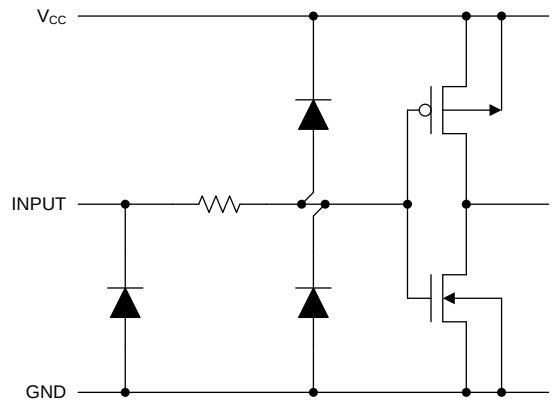

Figure 12. SIN, SCLK

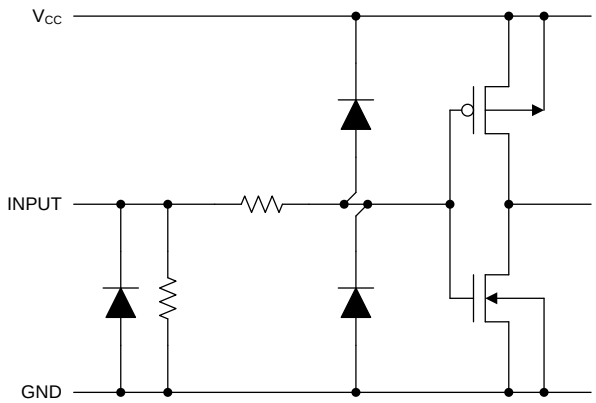

Figure 13. LAT, GCLK

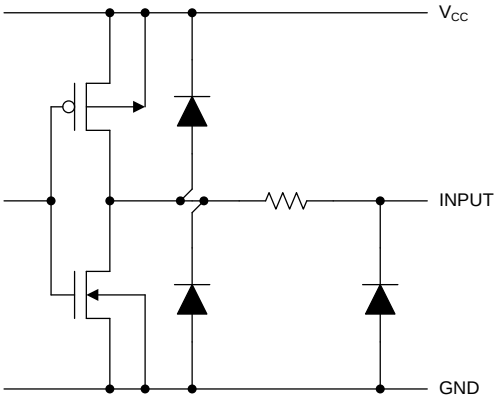

Figure 14. SOUT

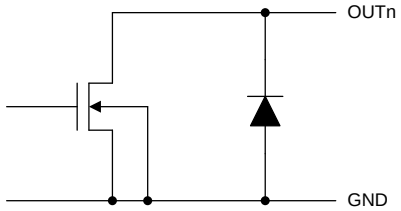

Figure 15. OUT0 Through OUT15

9 Detailed Description

9.1 Overview

The TLC694x device is a 16-channel constant-current-sink LED driver supporting 1- to 32-, 48-multiplexing. Each channel has an individually adjustable 65,536-step pulse-width modulation (PWM) grayscale (GS) control. The TLC6946 device implements 16-Kbit display memory and the TLC6948 device implements 24-Kbit display memory to increase the visual refresh rate and to decrease the grayscale data-writing frequency.

The TLC694x device supports current from 0.3 mA to 25 mA for each channel, with typical 1% channel-to-channel current deviation and typical 1% device-to-device current deviation. The maximum current value of all 16 channels is set by an external IREF resistor and can be adjusted by the 128-step global brightness control (BC). The device also implements low-grayscale enhancement technology to solve the coupling issue and improve the display quality in low-grayscale conditions. These features make the TLC694x device a candidate for high-density-multiplexing LED-matrix-display and LED-panel applications.

The TLC694x device integrates enhanced circuits to solve the various display issues in fine-pitch LED display applications: the low-grayscale uniformity issue, coupling issue, ghosting issue, and caterpillar issue. The TLC694x device features an LED-open detection function, and the error detection results can be read via a serial data-interface port. Thermal shutdown and I_{REF}-resistor short protection ensure a higher system reliability. The TLC694x device also has a smart power-save mode that sets the total current consumption to 1 mA (typical) when all outputs are off.

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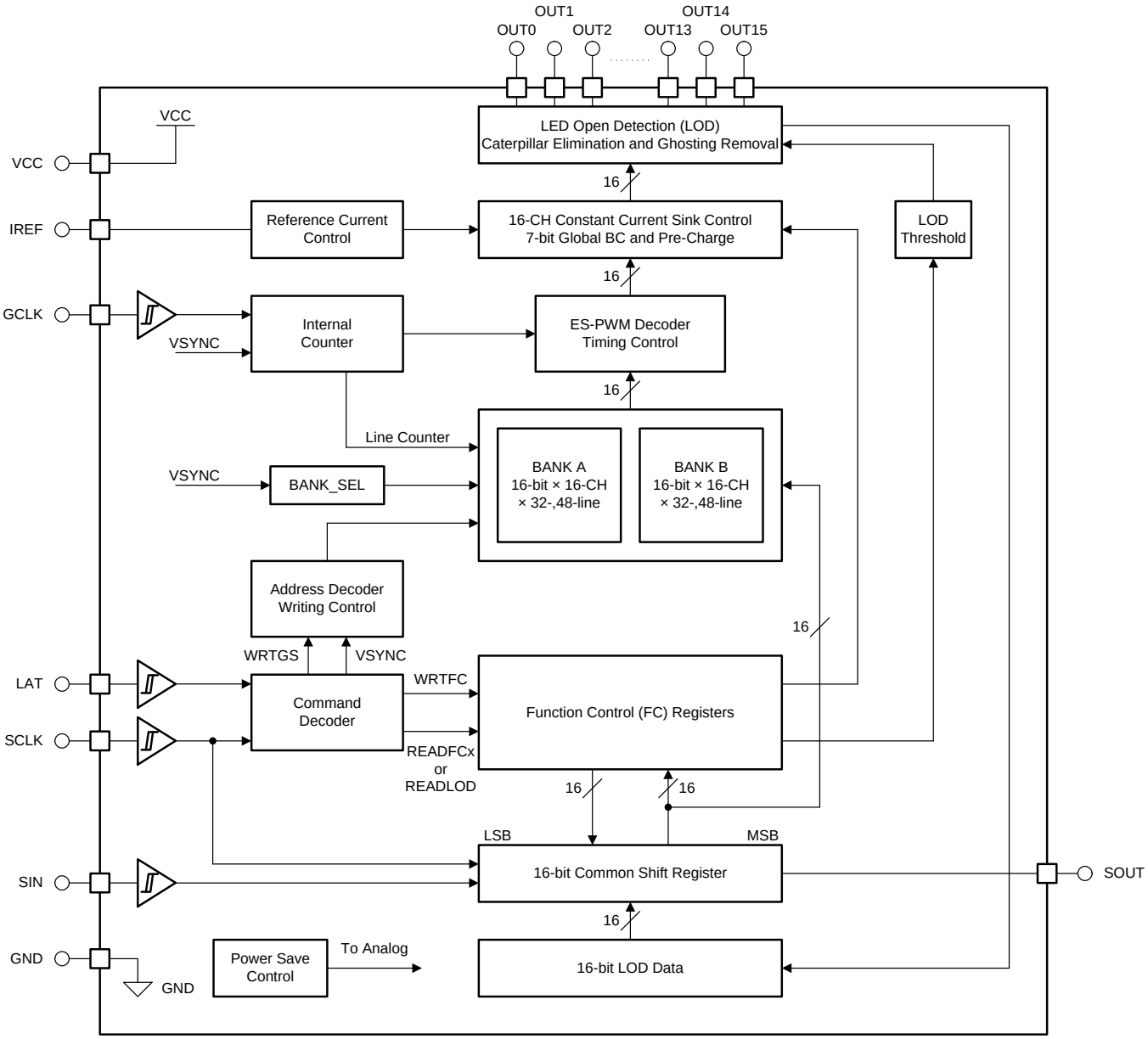
9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Built-In 16Kb Display Memory (SRAM)

The TLC6946 device integrates 16K bits of SRAM to support 1- to 32-multiplexing and the TLC6948 device integrates 24K bits of SRAM to support 1- to 48-multiplexing. SRAM is divided into two BANKs: BANK A and BANK B. While BANK A is displaying, BANK B is ready to receive the data of the next frame. While BANK B is displaying, BANK A is ready to receive the data of next frame.

9.3.2 GCLK Dual-Edge Operation

The TLC694x device uses the rising edge or both edges of GCLK. The selection is made by setting the GCLK_EDGE bit in the function control register. By default, the TLC6946 device uses the GCLK rising edge, and the maximum input GCLK frequency is 33 MHz. By setting GCLK_EDGE = 1, the TLC694x device operates at both GCLK edges (rising and falling), and the maximum internal GCLK frequency is 50 MHz with external 25MHz input.

9.3.3 Programmable Constant-Sink Channel Current

9.3.3.1 Global Brightness Control (BC)

The TLC694x device is able to adjust the output current of all constant-current outputs simultaneously. This function is called global brightness control (BC). The global BC for all outputs is programmed with a 7-bit word, thus all output currents can be adjusted in 128 steps from 12.5% to 100.69% for a given current-programming resistor, R_{IREF} (See Table 1). BC data can be set through the serial interface. When the BC data changes, the output current also changes immediately. When the device is powered on, the BC data in the function control register is set to 36h as the default value.

Table 1. Global BC Data vs Constant-Current Ratio and Set Current Value

BC DATA			GAIN	RATIO OF GAIN / GAIN_MAX (AT MAX BC)	I_{OUT} (mA) (I_{OLCmax}= 25 mA, TYP)	I_{OUT} (mA) (I_{OLCmax}= 2.4 mA, TYP)
BINARY	DECIMAL	HEX				
000 0000	0	00	4	12.5%	3.13	0.3
000 0001	1	01	4.22	13.19%	3.3	0.32
000 0010	2	02	4.44	13.88%	3.47	0.33
...	...	...	...	...	...	...
011 0101	53	35	15.78	49.31%	12.33	1.18
011 0110 (Default)	***54 (Default)***	***36 (Default)***	***16***	***50%***	***12.5***	***1.2***
011 0111	55	37	16.22	50.69%	12.67	1.22
...	...	...	...	...	...	...
111 1101	125	7D	31.78	99.31%	24.83	2.38
111 1110	126	7E	32	100%	25	2.4
111 1111	127	7F	32.22	100.69%	25.17	2.42

9.3.3.2 Select R_{IREF} for a Given BC

The maximum current per channel, I_{OLCmax}, is determined by resistor R_{IREF}, placed between the IREF and GND pins. The voltage on IREF is typically 0.8 V. R_{IREF} can be calculated by Equation 1.

$$R_{IREF}(k\Omega) = \frac{V_{IREF}(V)}{I_{OLCmax}(mA)} \times Gain = \frac{V_{IREF}(V)}{I_{OLCmax}(mA)} \times 32 \times \left(\frac{1}{8} + \frac{BC}{144}\right) \quad (1)$$

where

- V_{IREF} is the internal reference voltage on I_{REF} (0.8 V)
- I_{OLCmax} is the maximum current for each channel
- Gain is the current gain at BC = 7E (See Table 1)

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R_{IREF} must be between 1.02 kΩ and 10.7 kΩ in order to hold the channel sink current I_{OLC} between 25 mA (typical) and 0.3 mA (typical). Otherwise, the output may be unstable.

Table 2. Maximum Constant Current vs External Resistor R_{IREF}

I_{OLCmax} (mA)	R_{IREF} (kΩ, typical)
25	1.02
20	1.28
15	1.71
10	2.56
5	5.12
2.4	10.7

9.3.4 Grayscale (GS) Function (PWM Control)

The TLC694x device can adjust the brightness of each output channel using a pulse-width-modulation (PWM) control scheme. The architecture of 16 bits per channel results in 65536 brightness steps, from 0% up to 100% brightness. The on-time (t_{OUT_ON}) of each output (OUTn) can be calculated by Equation 2.

$$t_{OUT_ON} = t_{GCLK} \times GSn$$

where GSn is the grayscale of channel OUTn (2)

The TLC694x device implements an enhanced spectrum (ES) PWM control. The ES-PWM control can be selected with two different modes: 8-bit MSB + 8-bit LSB (8+8) mode, and 9-bit MSB + 7-bit LSB (9+7) mode. See *TLC6946 Technical Reference Manual* for more details.

9.3.5 Serial Data Interface

The TLC6948 has a flexible serial interface that can be connected to microcontrollers or digital signal processors in various ways. Only three pins are needed to input data into the device. More than two TLC6948s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. The SOUT pin can also be connected to the controller to read back data from the TLC6948 device.

9.3.6 LED-Open Detection (LOD)

The LED-open detection (LOD) function detects faults caused by an open circuit in any LED string or a short from OUTn to ground with low impedance. It does this by comparing the OUTn voltage to the LOD-detection threshold-voltage level set by LODVTH in the function control register. If the OUTn voltage is lower than the programmed voltage, the corresponding output LOD bit is set to 1 to indicate an open LED. Otherwise, the output of that LOD bit is 0. LOD data output by the detection circuit are valid only during the *on* period of that OUTn output channel.

9.3.7 Caterpillar Removal

The TLC694x device implements an internal circuit that can eliminate the caterpillar issue caused by an open LED. The caterpillar effect is a common issue for LED panels. The caterpillar removal function is enabled by setting LODRM_EN to 1 (default value after device powered on) in the function control register. When this function is enabled, the device automatically detects the open LED, and the corresponding channel does not turn on until device reset.

9.3.8 Precharge FET

The TLC694x internal precharge FET can prevent ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current from parasitic capacitance on OUTn through the LED when the supply voltage switches from one common line to the next common line. To prevent this unwanted charging current, the TLC694x device uses an internal FET to pull up OUTn during the common-line switching period. As a result, no charging current flows through LED and ghosting is eliminated.

9.3.9 Thermal Shutdown

The thermal shutdown (TSD) function turns off all device constant-current outputs when the junction temperature (T_J) exceeds 170°C (typical). It resumes normal operation when T_J falls below 155°C (typical).

9.3.10 IREF Resistor Short Protection (ISP)

The IREF resistor short protection (ISP) function prevents unwanted large currents from flowing though the constant-current output when the IREF resistor is shorted accidently. The TLC694x device turns off all output channels when the IREF pin voltage is lower than 0.19 V (typical). When the IREF pin voltage goes higher than 0.325 V (typical), the TLC694x device resumes normal operation.

9.4 Device Functional Modes

9.4.1 Normal Operating Mode

The TLC694x device is fully functional when V_{CC} reaches 3 V and is below 5.5 V. After power on, all OUTn of the TLC694x device are turned off. All the internal counters and function control registers are initialized. Write the proper grayscale data and function control data to enable normal device operation.

9.4.2 Power-Save Mode (PSM)

The power-save mode (PSM) is enabled by setting PSM_EN to 1 in the function control register.

When powered on, the default value of this bit is 0. When this function is enabled, if all the GS data received for the next frame are 0, then device enters power-save mode during the display of the next frame. When the device is in power-save mode, it resumes normal mode when it detects non-zero GS data input. In power-save mode, part of analog circuits are not operational; the device total current consumption, I_{CC}, is 1 mA(typical).

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLC6948 device is a 16-channel constant-current sink LED driver supporting 1- to 48-multiplexing. Each channel has an individually adjustable 65,536-step pulse-width-modulation (PWM) grayscale (GS) control. The TLC6948 device implements 24 Kbits of display memory to increase the visual refresh rate and to decrease the grayscale data writing frequency. This integrated memory makes TLC6948 a potential for high-density, fine-pitch LED matrix applications.

10.2 Typical Application

The TLC6948 is typically connected in series to drive the LED matrix with only a few controller ports. Figure 16 shows a typical application diagram with TLC6948 devices connected in cascade for an LED matrix.

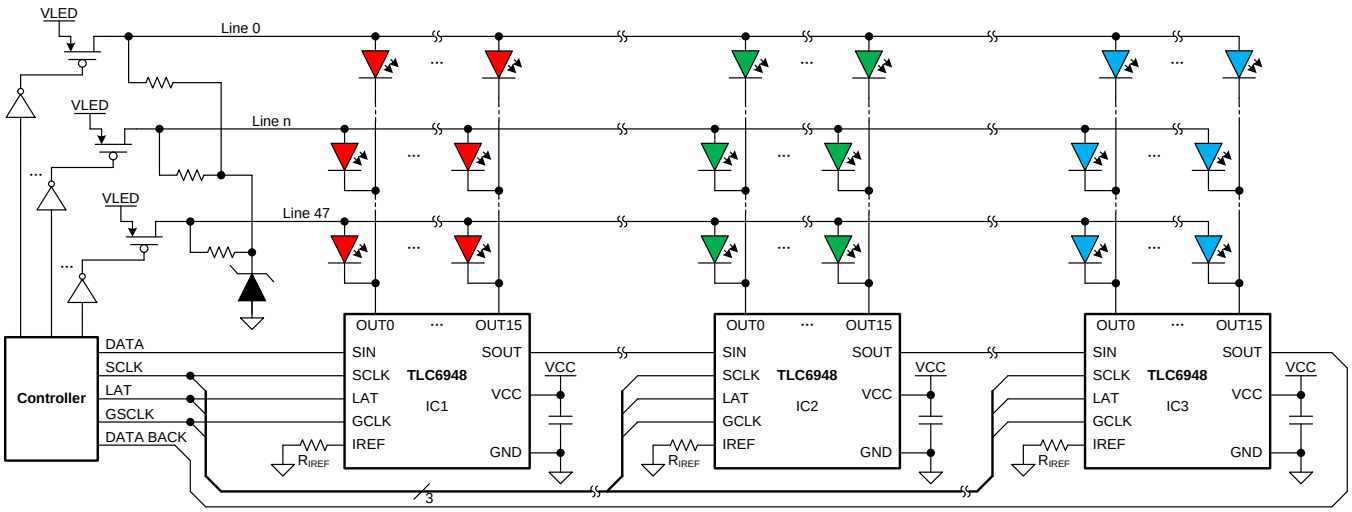

Figure 16. Cascading Three TLC6948 Devices

10.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC} and V_{LED} voltage	3 V to 5.5 V
SIN, SCLK, LAT, and GCLK voltage range	Low level = GND, high level = V_{CC}
The maximum LED forward voltage, $V_{(F)}$	Red LED 2V, green and blue LED 3V
The maximum current for each color LED, I_{OLCmax}	Red LED 10mA, green LED 6mA, blue LED 4mA.

10.2.2 Detailed Design Procedures

10.2.2.1 Power Supply Voltage

The LED power supply voltage V_{LED} must be higher than $V_{(F)}$ + $V_{(KNEE)}$. The device power supply voltage, V_{CC} should be equal or higher than V_{LED}. One example value is V_{LED} = V_{CC}= 3.8 V. See *TLC6946 Technical Reference Manual* for more details.

10.2.2.2 Channel Current and Brightness Control

See *Global Brightness Control (BC)* and *Select R_{IREF} for a Given BC*. Select the reference-current-setting resistor R_{IREF} to set the maximum channel current for each color LED. Select the BC data for the best white balance of the red, green, and blue LED lamp. See *TLC6946 Technical Reference Manual* for more details.

10.2.2.3 SCLK and GCLK Frequency

SCLK is the serial data shift-in clock signal; and GCLK is the PWM-control reference-clock signal. Equation 3 shows the minimum frequency requirement for GCLK and SCLK. See *TLC6946 Technical Reference Manual* for more details.

$$f_{GCLK} = m \times n \times f_{VR}$$
$$f_{SCLK} = N \times n \times 256 \times f_{FPS}$$

where

- f_{GCLK} is the minimum GCLK frequency for single-edge operating mode
- f_{SCLK} is the minimum SCLK frequency
- m is the GCLK number of each sub-period, determined by the PWM mode selected
- f_{VR} is the visual refresh rate of the entire cascading series
- N is the number of cascaded TLC6948 devices
- n is the number of scan lines
- f_{FPS} is the frame rate (3)

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10.2.3 Application Curves

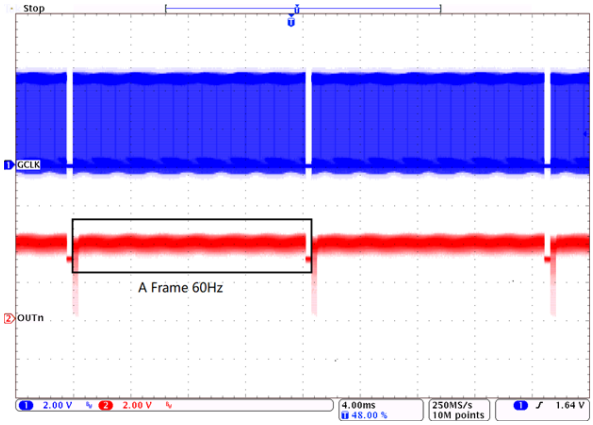

Figure 17. OUTn Waveform for ES-PWM Mode (GSn = 0001h)

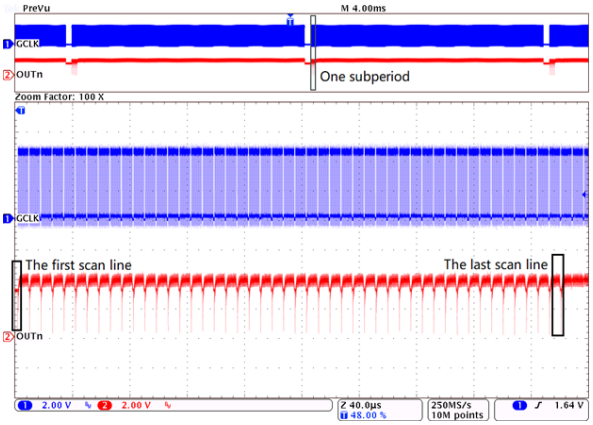

Figure 18. OUTn Waveform for ES-PWM Mode Zooming in One Sub-period (GSn = 0001h)

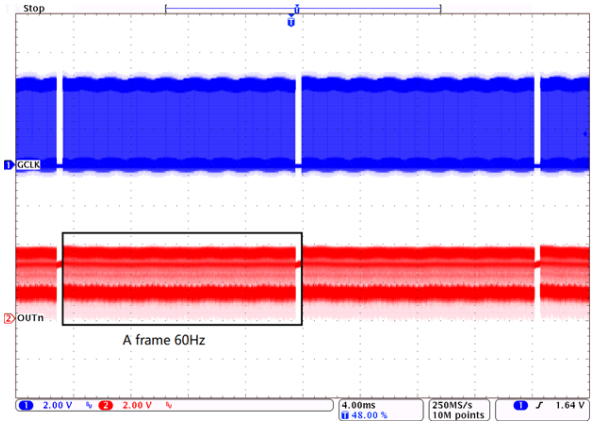

Figure 19. OUTn Waveform for ES-PWM Mode (GSn = FFFFh)

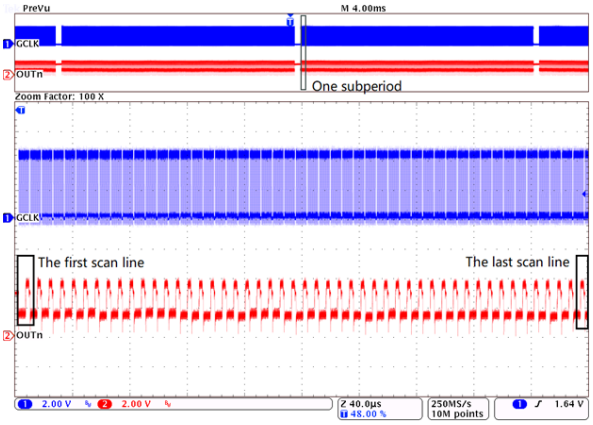

Figure 20. OUTn Waveform for ES-PWM Mode Zooming in One Sub-period (GSn = FFFFh)

11 Power Supply Recommendations

Decouple the V_{CC} power supply voltage by placing a 0.1-µF ceramic capacitor close to the V_{CC} pin and GND plane. Depending on panel size, several equally distributed electrolytic capacitors must be placed on the board for a well-regulated LED supply voltage V_{LED}. V_{LED} voltage ripple must be less than 5% of its nominal value.

12 Layout

12.1 Layout Guidelines

Place the decoupling capacitor near the V_{CC} pin and GND plane.

Place the current-programming resistor, R_{IREF}, close to the IREF pin and the GND pin.

Make the GND trace as wide as possible for large GND currents.

Routing between the LED cathode and the device OUTn pin must be as short and straight as possible to reduce wire inductance.

The thermal pad (QFN package) must be connected to the GND plane. Because the thermal pad is used as a power ground pin internally, there is a large current flow through this pad when all channels turn on. Furthermore, connect the thermal pad to a heat sink layer by thermal vias to reduce device temperature. One suggested thermal via pattern is shown in *Layout Examples*. For more information about suggested thermal via pattern and via size, see *PowerPAD Thermally Enhanced Package*.

MOSFETs must be placed in the in the middle of the board, which should be laid out as symmetrically as possible.

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12.2 Layout Examples

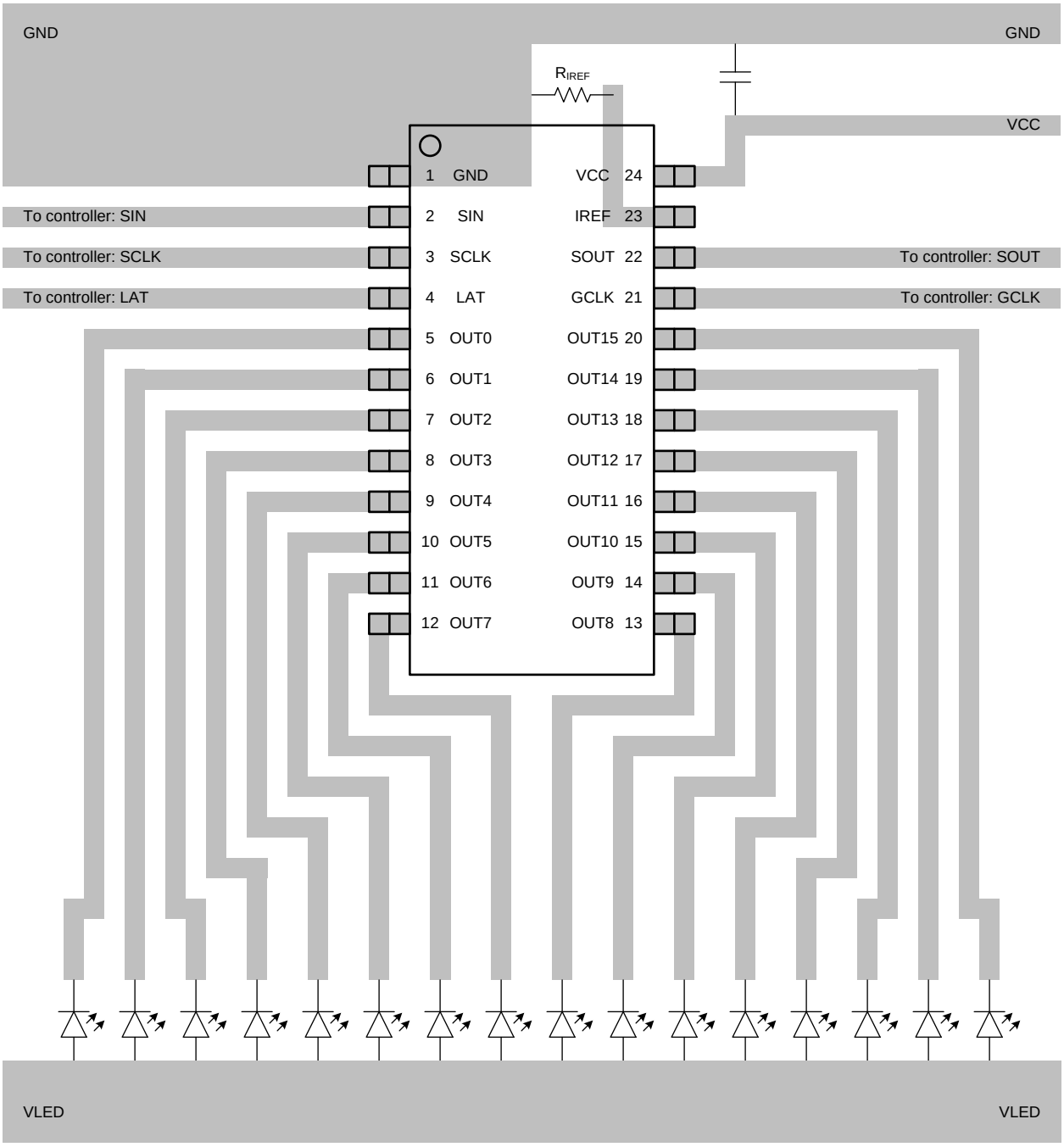

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Figure 21. SSOP-24 Package Layout Example

Layout Examples (continued)

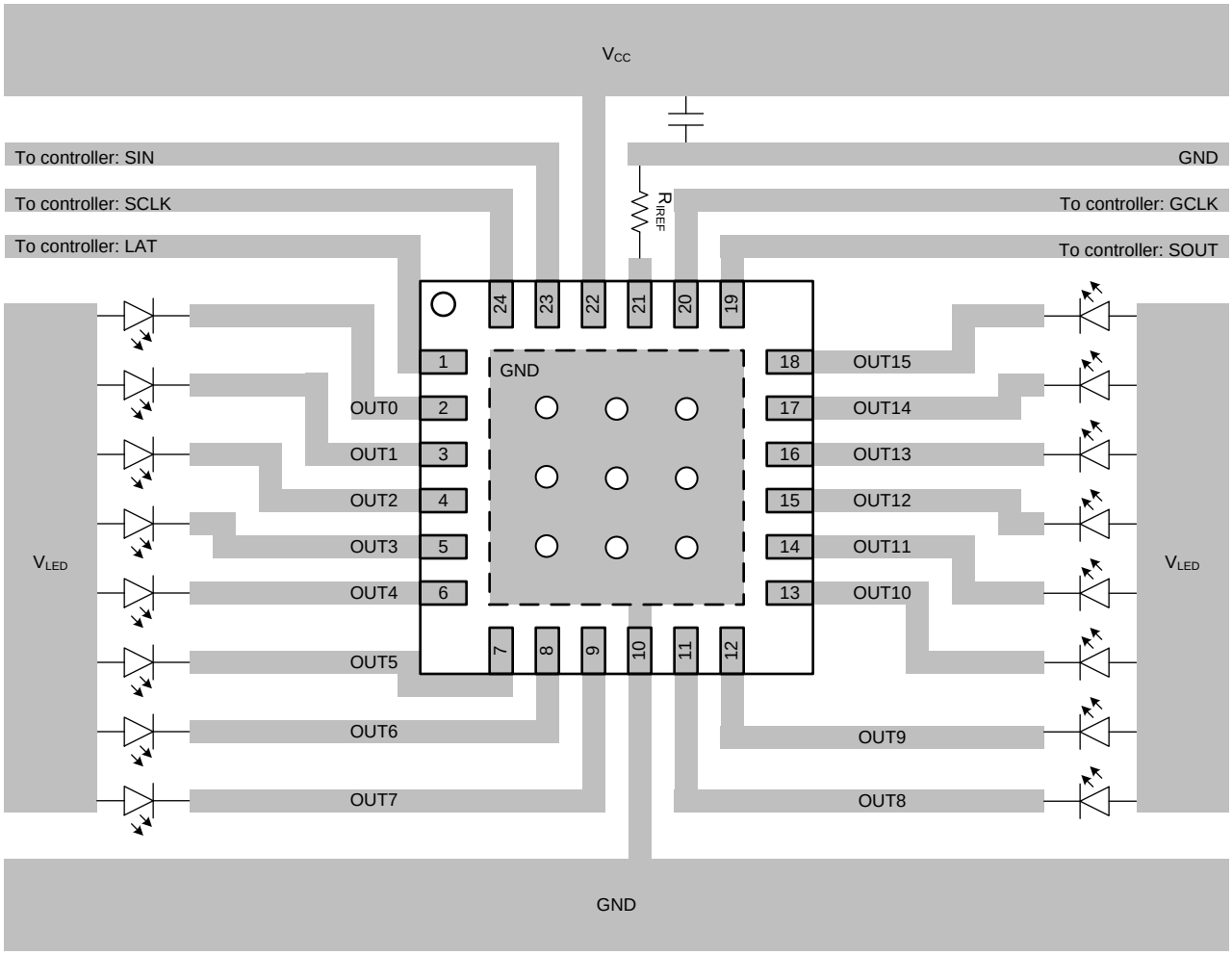

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Figure 22. VQFN-24 Package Layout Example

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *TLC694x 16-Channel LED Driver Technical Reference Manual*
- *Semiconductor and IC Package Thermal Metrics*

13.2 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLC6946	Click here	Click here	Click here	Click here	Click here
TLC6948	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC6946DBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6946
TLC6946DBQR.A	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6946
TLC6946RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 6946
TLC6946RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 6946
TLC6948DBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6948
TLC6948DBQR.A	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC6948
TLC6948RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 6948
TLC6948RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 6948

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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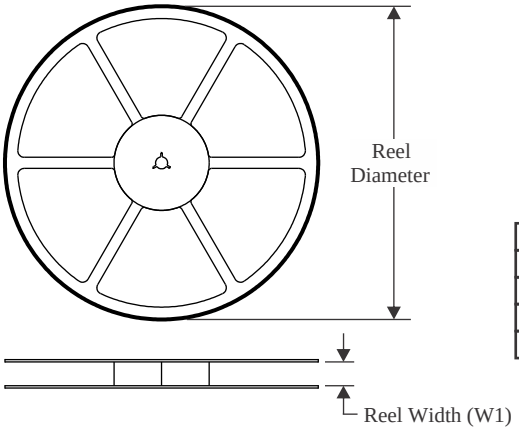
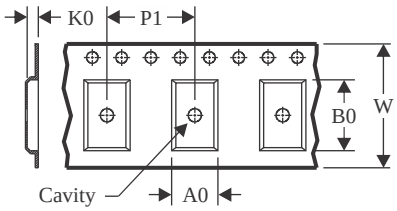
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

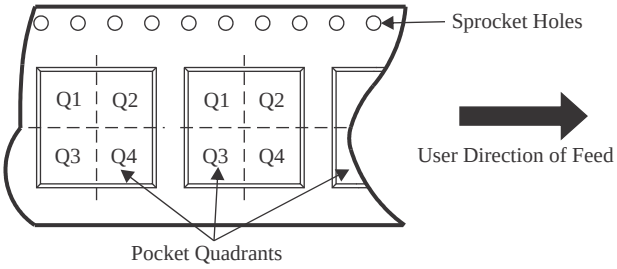


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

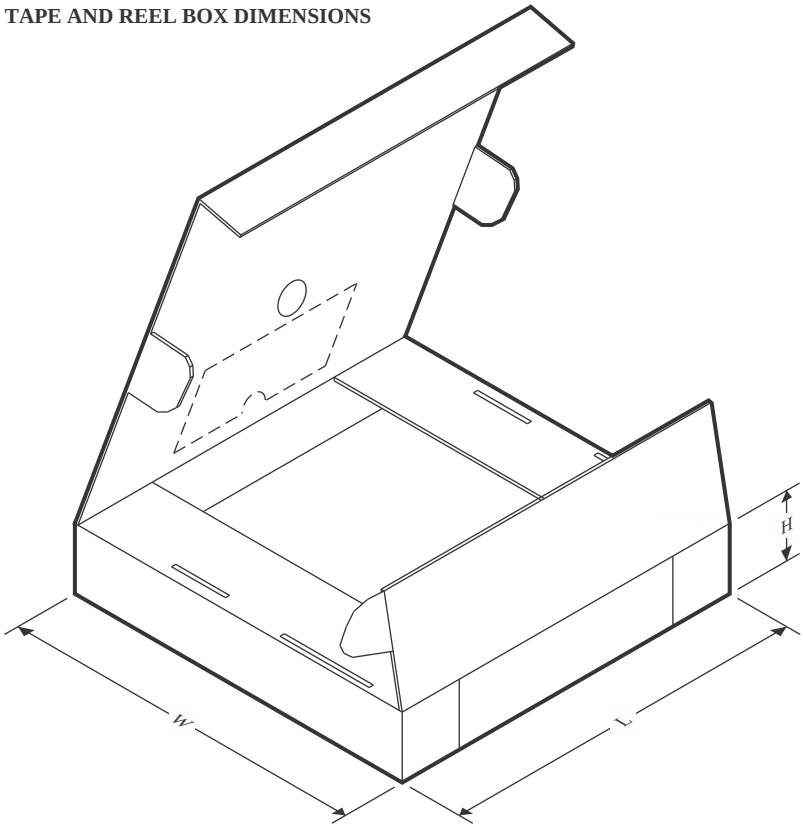
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6946DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC6946RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC6948DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC6948RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

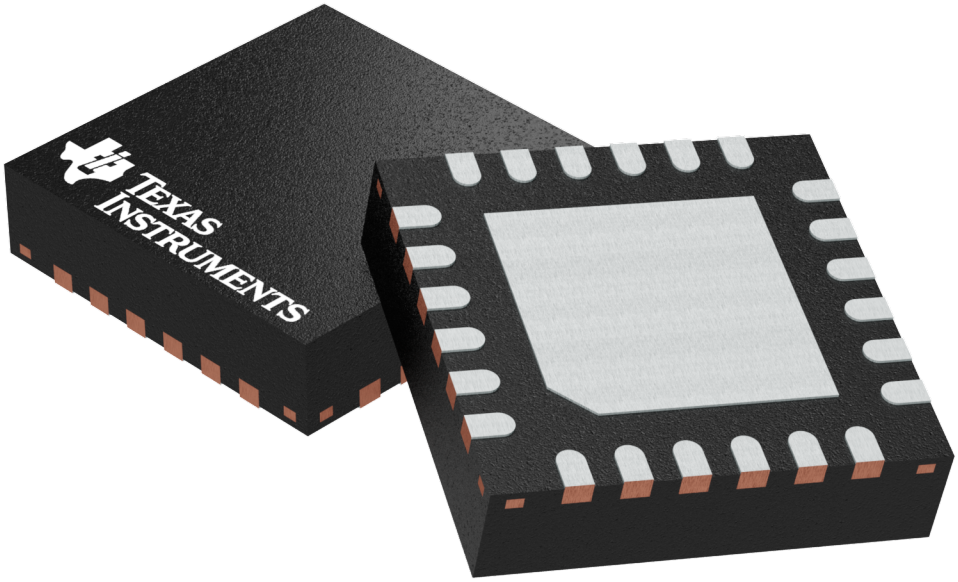


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6946DBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
TLC6946RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TLC6948DBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
TLC6948RGER	VQFN	RGE	24	3000	367.0	367.0	35.0

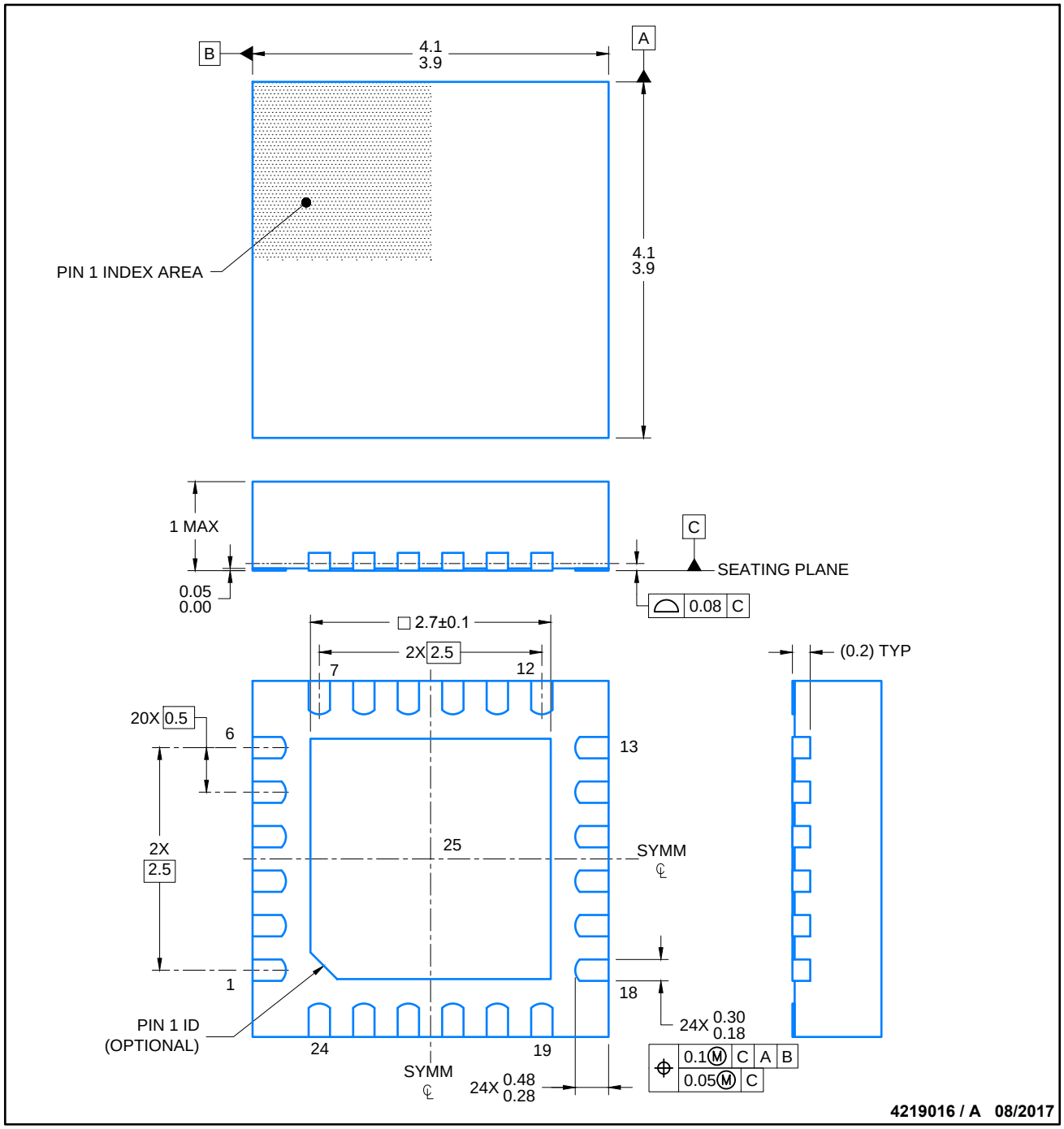
RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



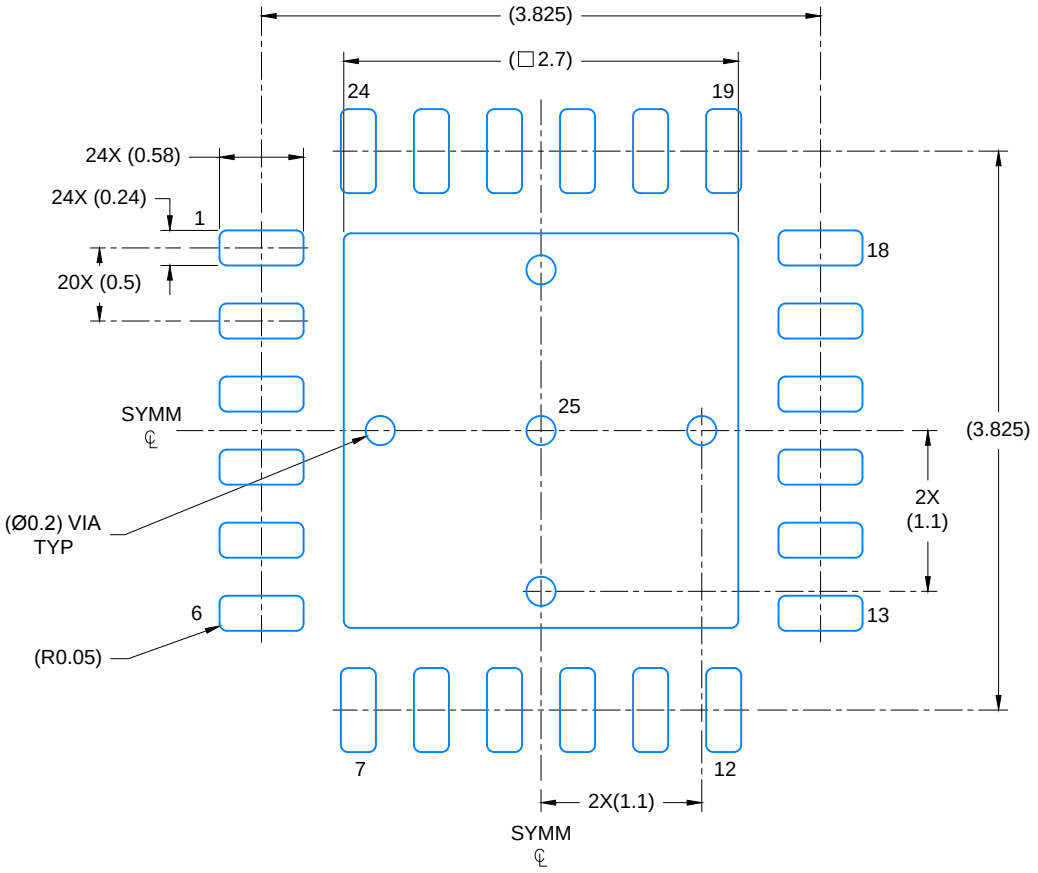
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC QUAD FLATPACK- NO LEAD



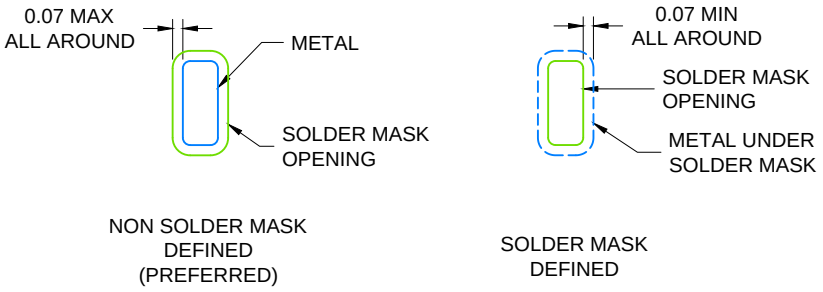
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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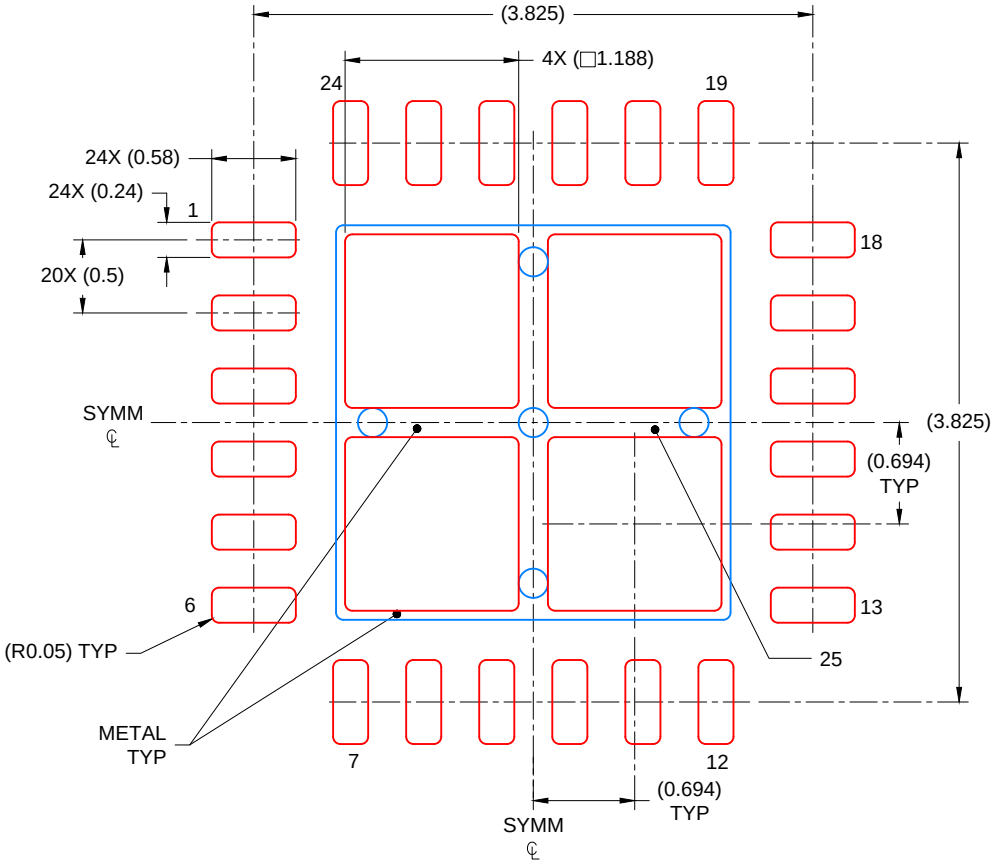
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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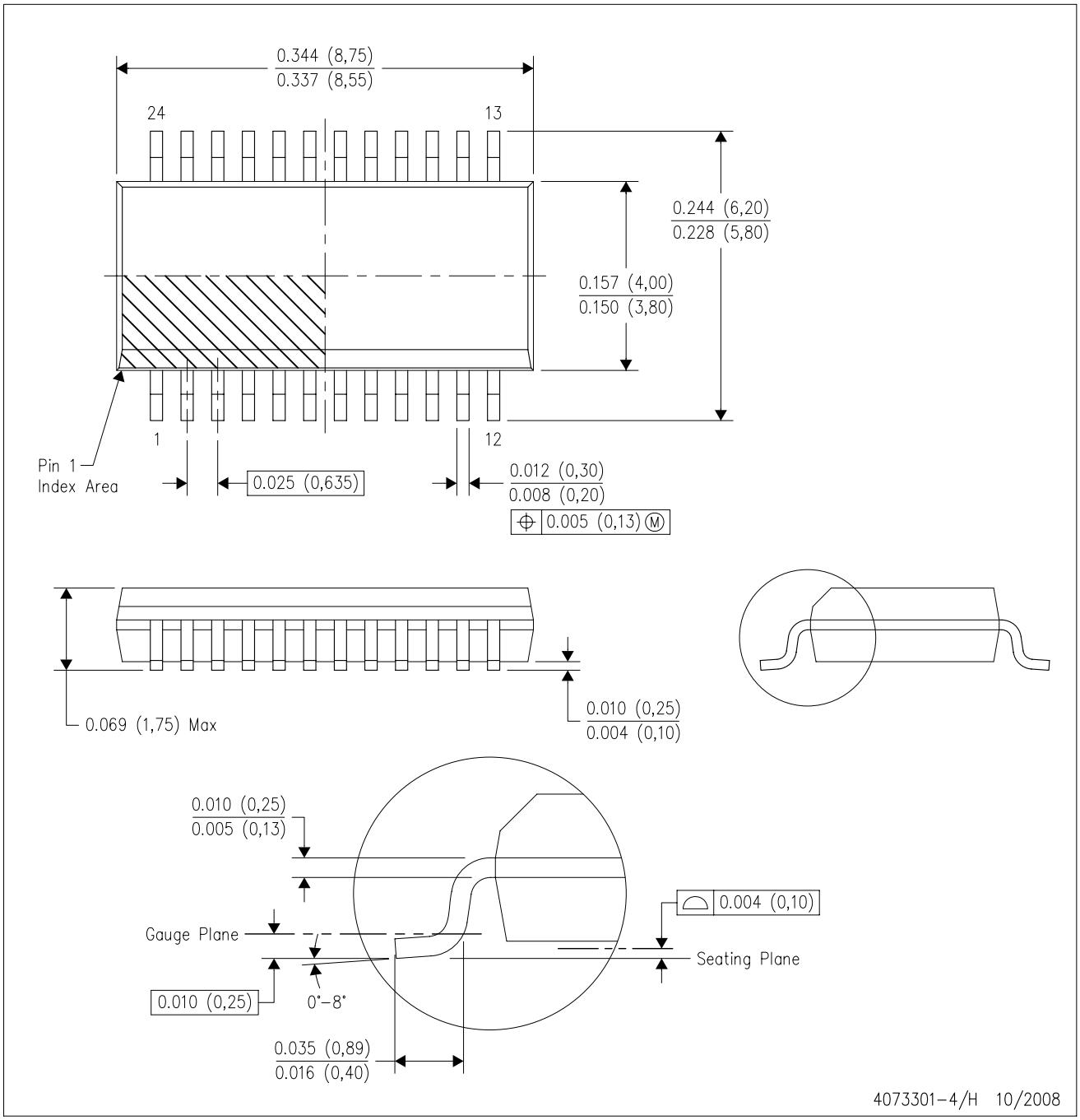
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

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