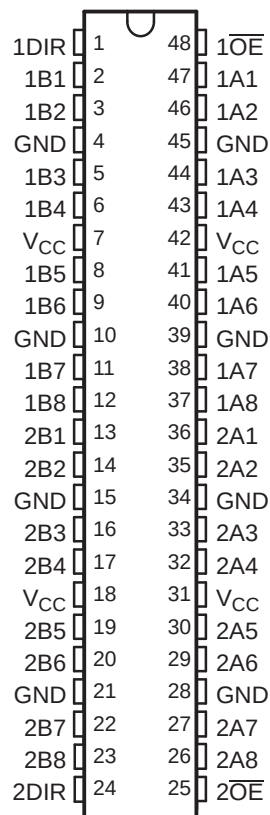


FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Max t_{pd} of 3 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16245-EP is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so that the buses are effectively isolated.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tape and reel	CALVCH16245IDLREP	ALVCH16245
–55°C to 125°C	SSOP – DL	Tape and reel	CALVCH16245MDLREP	ALCH16245M

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN74ALVCH16245-EP

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES608A – SEPTEMBER 2004 – REVISED JUNE 2006

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

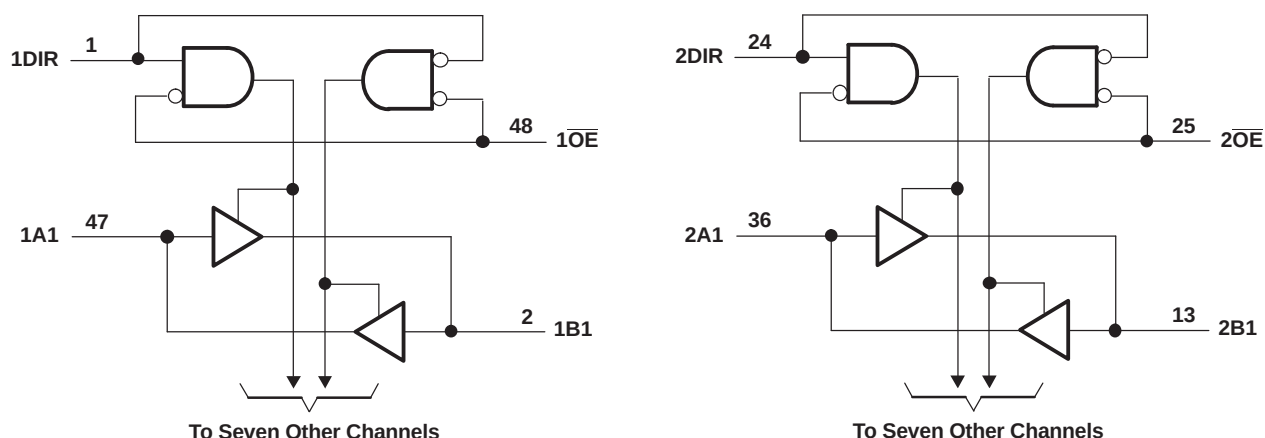
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**FUNCTION TABLE
(EACH 8-BIT SECTION)**

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	4.6	V
V _I	Input voltage range	Except I/O ports ⁽²⁾	−0.5	4.6	V
		I/O ports ⁽²⁾⁽³⁾	−0.5	V _{CC} + 0.5	
V _O	Output voltage range ⁽²⁾⁽³⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±50		mA
	Continuous current through each V _{CC} or GND		±100		mA
θ _{JA}	Package thermal impedance ⁽⁴⁾		63		°C/W
T _{std}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 2.7 V to 3.6 V		0.8	
V _I	Input voltage		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4	mA
		V _{CC} = 2.3 V		–12	
		V _{CC} = 2.7 V		–12	
		V _{CC} = 3 V		–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		12	
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature (I temp)		–40	85	°C
T _A	Operating free-air temperature (M temp)		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH16245-EP

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCES608A – SEPTEMBER 2004 – REVISED JUNE 2006

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = –100 µA	1.65 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –6 mA	2.3 V	2			
	I _{OH} = –12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
	I _{OH} = –24 mA	3 V	2			
V _{OL}	I _{OL} = 100 µA	1.65 V to 3.6 V	0.2			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 6 mA	2.3 V	0.4			
	I _{OL} = 12 mA	2.3 V	0.7			
		2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V	±5			µA
I _{I(hold)}	V _I = 0.58 V	1.65 V	25			µA
	V _I = 1.07 V	1.65 V	–25			
	V _I = 0.7 V	2.3 V	45			
	V _I = 1.7 V	2.3 V	–45			
	V _I = 0.8 V	3 V	75			
	V _I = 2 V	3 V	–75			
	V _I = 0 to 3.6 V ⁽²⁾	3.6 V	±500			
I _{OZ} ⁽³⁾	V _O = V _{CC} or GND	3.6 V	±10			µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V		4	pF
C _{io}	A or B port	V _O = V _{CC} or GND	3.3 V		8	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Switching Characteristics

over recommended operating free-air temperature (–40°C to 85°C) range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	1	3.7	3.6		1	3	ns
t _{en}	$\overline{\text{OE}}$	A or B	1	5.7	5.4		1	4.4	ns
t _{dis}	$\overline{\text{OE}}$	A or B	1	5.2	4.6		1	4.1	ns

Switching Characteristics

over recommended operating free-air M temperature (–55°C to 125°C) range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A	1	4.5	1	4.0	ns
t_{en}	$\overline{OE}$	A or B	1	8.2	1	5.5	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5	1	5.0	ns

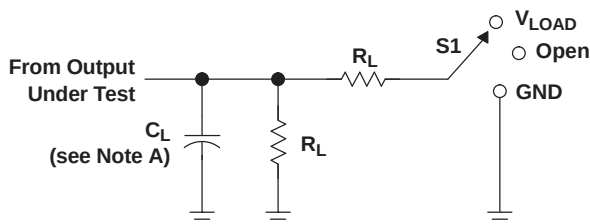
Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}, \quad f = 10\text{ MHz}$	(1)	22	29	pF
	Outputs disabled		(1)	4	5	

(1) This information was not available at the time of publication.

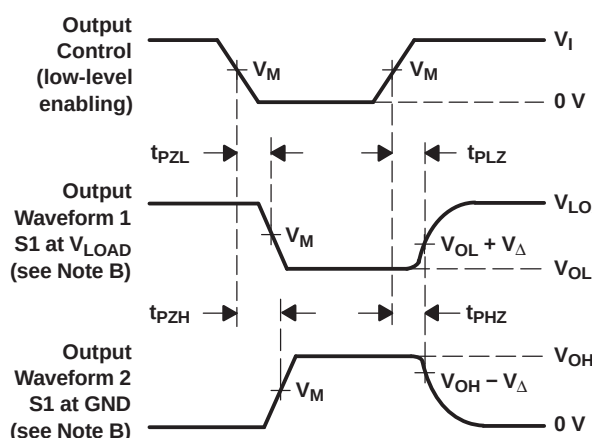
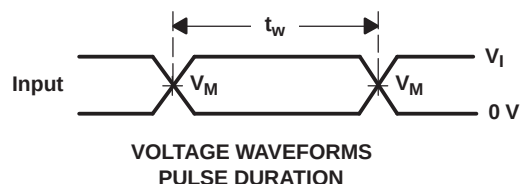
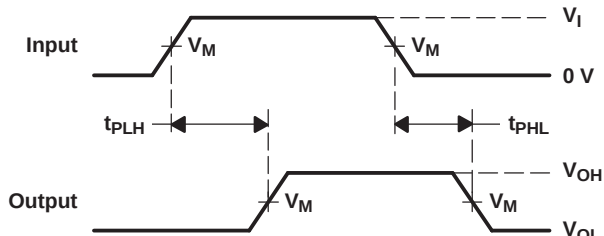
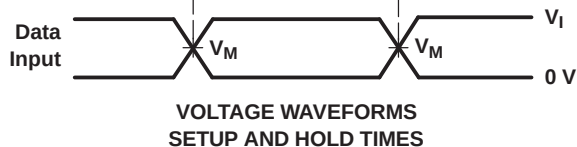
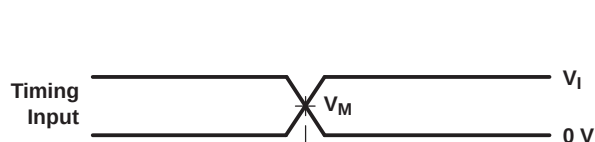
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PHL}	GND

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CALVCH16245IDLREP	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16245
CALVCH16245MDLREP	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ALCH16245M
V62/04763-01XE	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16245
V62/04763-02XE	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ALCH16245M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

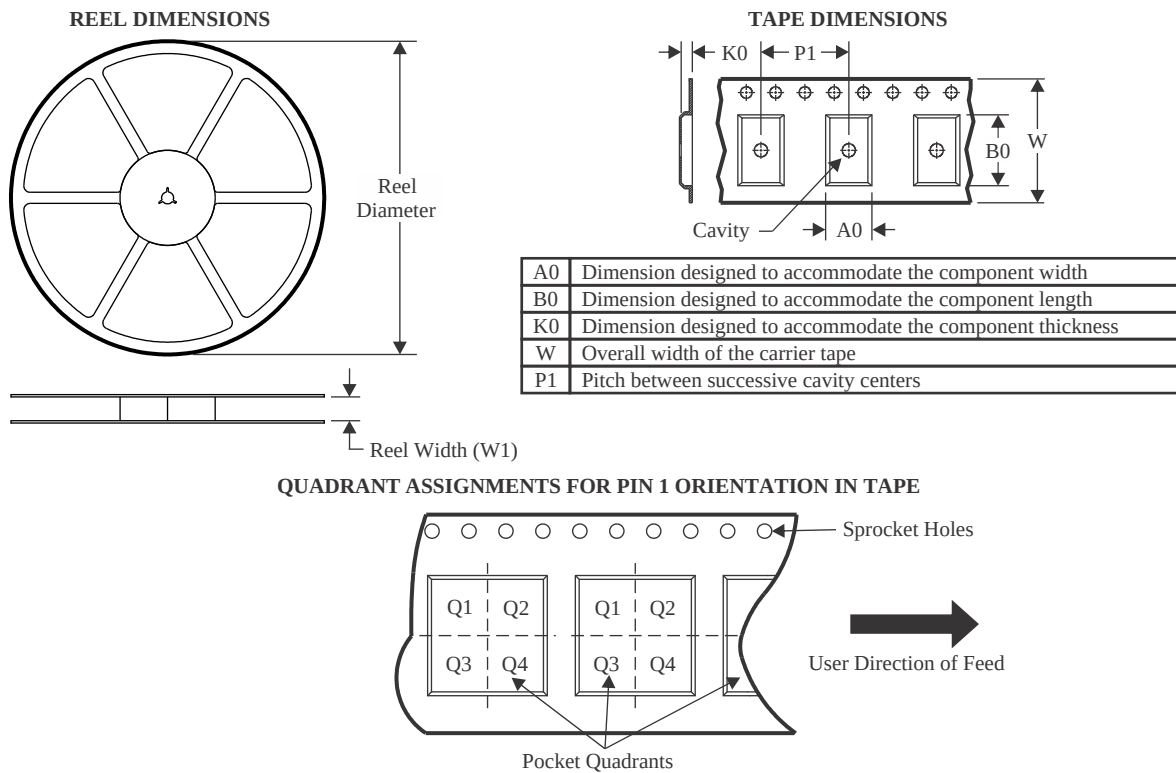
OTHER QUALIFIED VERSIONS OF SN74ALVCH16245-EP :

- Catalog : [SN74ALVCH16245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

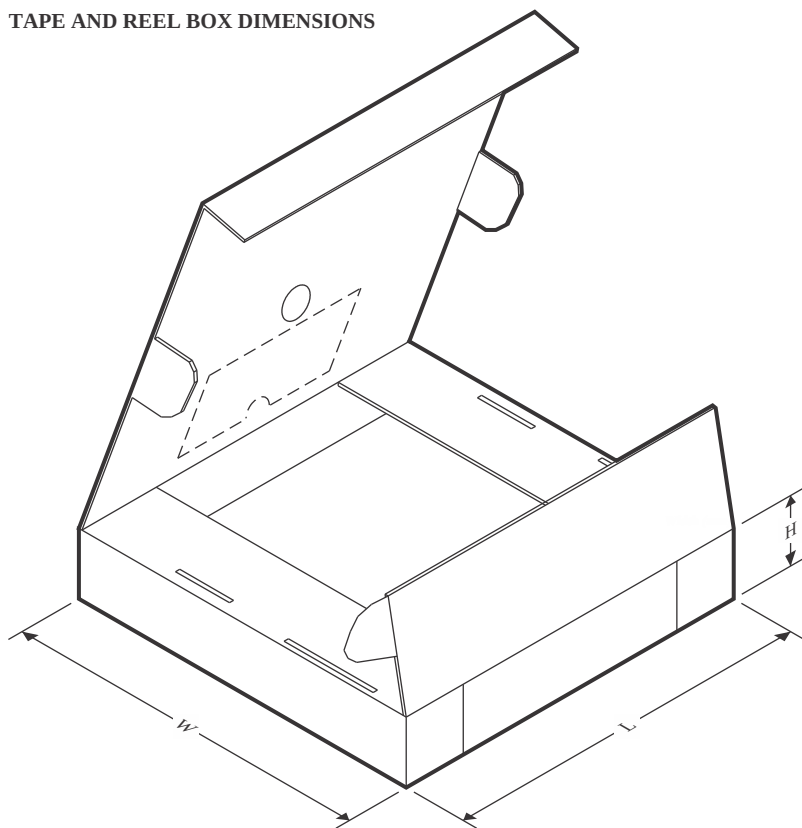
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CALVCH16245IDLREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CALVCH16245MDLREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

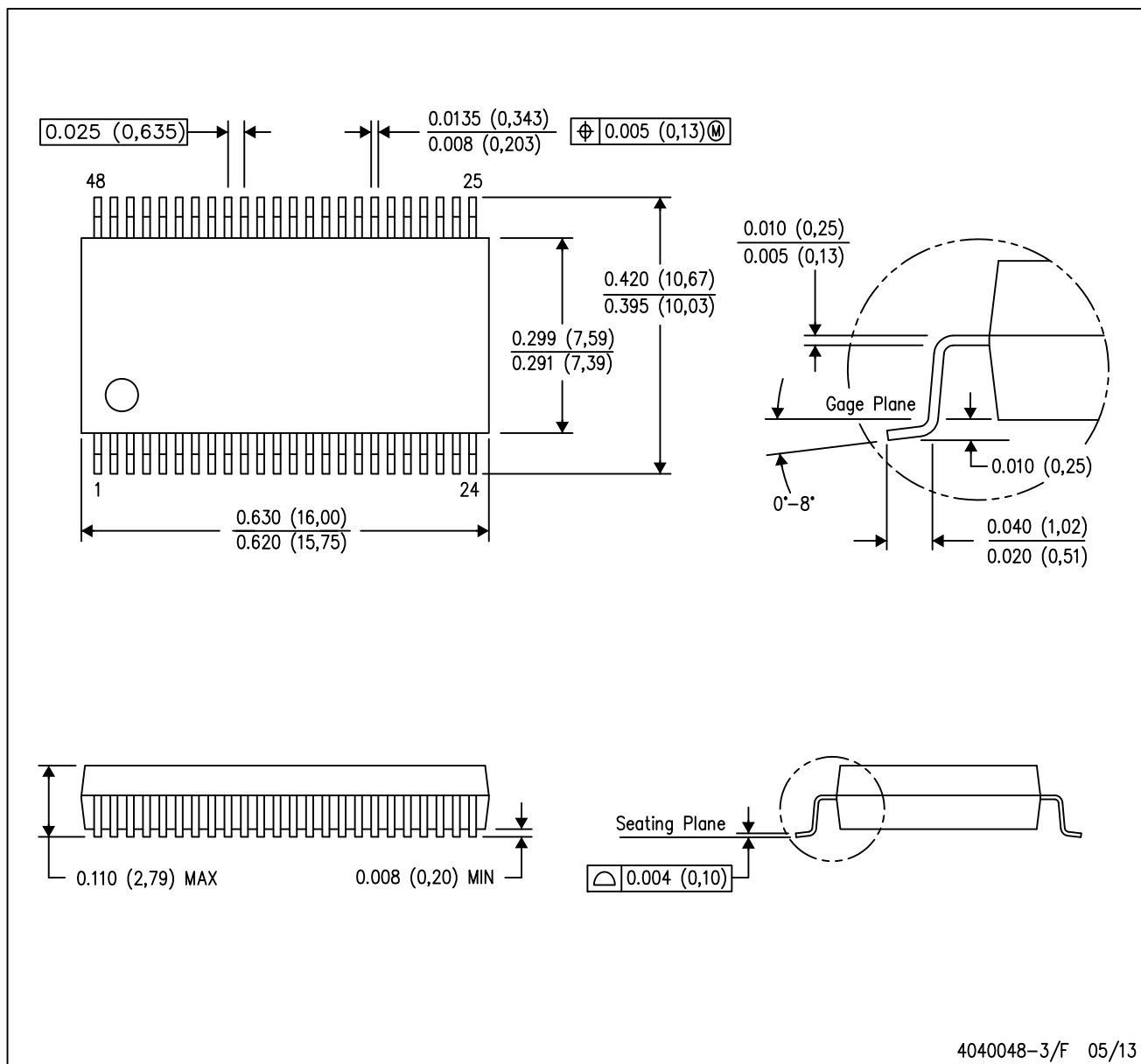


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CALVCH16245IDLREP	SSOP	DL	48	1000	367.0	367.0	55.0
CALVCH16245MDLREP	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated