TPS54361 4.5-V to 60-V Input, 3.5-A, Step-Down DC-DC Converter With Soft-Start and Eco-Mode™

1 Features

- High Efficiency at Light Loads With Pulse-Skipping Eco-Mode™
- 89-mΩ High-Side MOSFET
- 152-μA Operating Quiescent Current and 2-μA Shutdown Current
- 100-kHz to 2.5-MHz Adjustable Switching Frequency
- Synchronizes to External Clock
- Low Dropout at Light Loads With Integrated BOOT Recharge FET
- Adjustable UVLO Voltage and Hysteresis
- UV and OV Power Good Output
- Adjustable Soft Start and Sequencing
- 0.8-V 1% Internal Voltage Reference
- 10-Pin WSON With Thermal Pad Package
- –40°C to 150°C T_J Operating Range
- Create a Custom Design using the TPS54361 with the WEBENCH® Power Designer

2 Applications

- Industrial Automation and Motor Control
- Vehicle Accessories: GPS (see SLVA412), Entertainment
- USB Dedicated Charging Ports and Battery Chargers (see SLVA464)
- 12-V, 24-V, and 48-V Industrial, Automotive, and Communications Power Systems

3 Description

The TPS54361 device is a 60-V, 3.5-A, step-down regulator with an integrated high-side MOSFET. The device survives load dump pulses up to 65 V per ISO 7637. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no-load supply current to 152 μA. Shutdown supply current is reduced to 2 μA when the enable pin is pulled low.

Undervoltage lockout is internally set at 4.3 V but can increase using an external resistor-divider at the enable pin. The output voltage startup ramp is controlled by the soft-start pin that can also be configured for sequencing and tracking. An open-drain power-good signal indicates the output is within 93% to 106% of the nominal voltage.

A wide adjustable switching frequency range allows for optimization of either efficiency or external component size. Cycle-by-cycle current limit, frequency foldback, and thermal shutdown protects internal and external components during an overload condition.

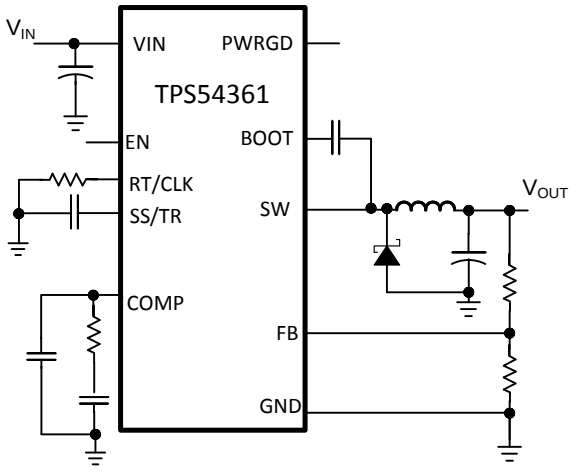
The TPS54361 device is available in a 10-pin 4-mm × 4-mm WSON package.

Device Information

PART NUMBER	PACKAGE (PIN)	BODY SIZE
TPS54361	WSON (10)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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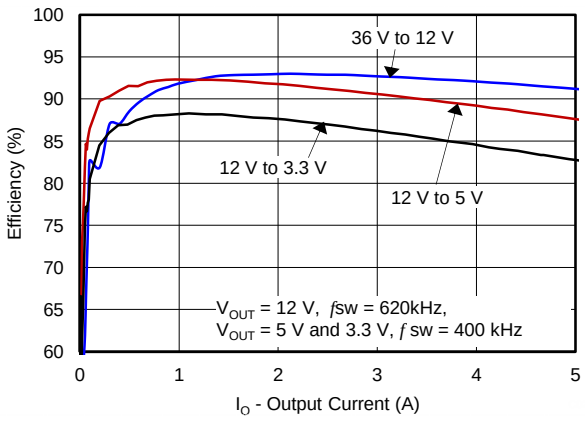
Efficiency vs Load Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2016) to Revision D — **Page**

- Added the WEBENCH information in the *Features*, *Detailed Design Procedure*, and *Device Support* sections ... 1
- Changed Equation 10 and Equation 11 ... 20
- Changed Equation 30 ... 29
- Changed From: "PowerPAD" To: "thermal pad" in the *Layout Guidelines* section ... 42

Changes from Revision B (August 2015) to Revision C — **Page**

- Added SW, 5-ns Transient to the *Absolute Maximum Ratings* ... 4
- Changed text in the *Application Information* From: "iterative design procedure" To: "interactive design procedure" ... 28
- Changed = 47 W To: = 0.444W in Equation 56 ... 35
- Changed = 47 W To: = 0.444W and = 0.616 W To: 0.591 W in Equation 60 ... 36

Changes from Revision A (December 2013) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (November 2013) to Revision A — **Page**

- Changed the device From: Product Preview To: Production ... 1

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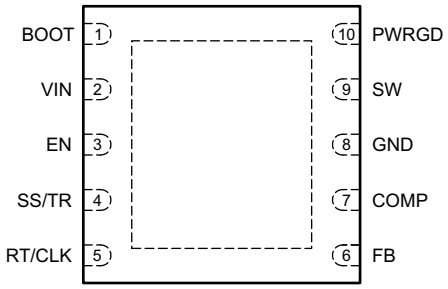
5 Pin Configuration and Functions

DPR Package
10-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	I	A bootstrap capacitor is required between the BOOT and SW pin. If the voltage on this capacitor is below the minimum required to turn on the high-side MOSFET, the gate drive is switched off until the capacitor is refreshed.
COMP	7	I	This pin is the error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
EN	3	I	This pin is the enable pin. An internal pullup current source enables the TPS54361 if the EN pin is floating. Pull EN below 1.2 V to disable. Adjust the input undervoltage lockout with two resistors. See *Enable and Adjusting Undervoltage Lockout*.
FB	6	I	This pin is the inverting input of the transconductance (gm) error amplifier.
GND	8	–	Ground
PWRGD	10	O	The Power Good pin is an open drain output that asserts low if the output voltage is out of regulation because of thermal shutdown, dropout, overvoltage, or EN shutdown.
RT/CLK	5	I	This pin is the resistor timing and external clock pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high-impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
SS/TR	4	I	This pin is the soft start and tracking pin. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, the SS/TR pin can be used for tracking and sequencing.
SW	9	O	The SW pin is the source of the internal high-side power MOSFET and switching node of the converter.
VIN	2	I	Connect to this pin the input voltage supply with a 4.5-V to 60-V operating range.
Thermal Pad		–	The GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	VIN	–0.3	65	V
	EN	–0.3	8.4	
	FB	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.6	
	BOOT-SW	–0.3	8	
	SW	–0.6	65	
	SW, 5-ns Transient	–7	65	
	SW, 10-ns Transient	–2	65	
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	4.5	60	V
V_O	Output voltage	0.8	58.8	V
I_O	Output current	0	3.5	A
T_J	Junction Temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC (1) (2)		TPS54361 DPR (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	35.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	2.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Power rating at a specific ambient temperature T_A must be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See the power dissipation estimate in *Power Dissipation Estimate* for more information.

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6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 4.5 V to 60 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		4.5		60	V
Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
Internal undervoltage lockout threshold hysteresis			325		mV
Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 60 V		2.25	4.5	µA
Operating: nonswitching supply current	FB = 0.9 V, T_A = 25°C		152	200	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
Input current	Enable threshold +50 mV		–4.6		µA
	Enable threshold –50 mV	–0.58	–1.2	–1.8	
Hysteresis current		–2.2	–3.4	–4.5	µA
VOLTAGE REFERENCE					
Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET					
ON-resistance	VIN = 12 V, BOOT-SW = 6 V		89	190	mΩ
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (gm)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		350		µS
Error amplifier transconductance (gm) during soft start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		µS
Error amplifier DC gain	V_{FB} = 0.8 V		10 000		V/V
Min unity gain bandwidth			2500		kHz
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100-mV overdrive		±30		µA
COMP to SW current transconductance			12		A/V
CURRENT LIMIT					
Current limit threshold	All VIN and temperatures, open loop(1)	4.5	5.5	6.8	A
	All temperatures, VIN = 12 V, open loop(1)	4.5	5.5	6.3	
	VIN = 12 V, T_A = 25°C, open loop(1)	5.2	5.5	5.9	
THERMAL SHUTDOWN					
Thermal shutdown			176		°C
Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
RT/CLK high threshold			1.55	2	V
RT/CLK low threshold		0.5	1.2		V

(1) Open Loop current limit measured directly at the SW pin and is independent of the inductor value and slope compensation.

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Electrical Characteristics (continued)

T_J = –40°C to 150°C, VIN = 4.5 V to 60 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START AND TRACKING (SS/TR PIN)					
Charge current	$V_{SS/TR}$ = 0.4 V		1.7		µA
SS/TR-to-FB matching	$V_{SS/TR}$ = 0.4 V		42		mV
SS/TR-to-reference crossover	98% nominal		1.16		V
SS/TR discharge current (overload)	FB = 0 V, $V_{SS/TR}$ = 0.4 V		354		µA
SS/TR discharge voltage	FB = 0 V		54		mV
POWER GOOD (PWRGD PIN)					
FB threshold for PWRGD low	FB falling		90%		
FB threshold for PWRGD high	FB rising		93%		
FB threshold for PWRGD low	FB rising		108%		
FB threshold for PWRGD high	FB falling		106%		
Hysteresis	FB falling		2.5%		
Output high leakage	V_{PWRGD} = 5.5 V, T_A = 25°C		10		nA
ON-resistance	I_{PWRGD} = 3 mA, V_{FB} < 0.79 V		45		Ω
Minimum VIN for defined output	V_{PWRGD} < 0.5 V, I_{PWRGD} = 100 µA		0.9	2	V

6.6 Timing Requirements

T_J = –40°C to 150°C, V_{IN} = 4.5 V to 60 V (unless otherwise noted)

	MIN	NOM	MAX	UNIT
RT/CLK				
Minimum CLK input pulse width		15		ns

6.7 Switching Characteristics

T_J = –40°C to 150°C, V_{IN} = 4.5 V to 60 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW						
t_{on}	Minimum ON-time	V_{IN} = 23.7 V, V_{OUT} = 5 V, I_{OUT} = 3.5 A, R_T = 39.6 kΩ, T_A = 25°C		100		ns
CURRENT LIMIT						
	Current limit threshold delay			60		ns
RT/CLK						
	Switching frequency range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	RT/CLK falling edge to SW rising edge delay	Measured at 500 kHz with an RT resistor in series		55		ns
	PLL lock-in time	Measured at 500 kHz		78		µs
ERROR AMPLIFIER						
	Enable to COMP active	V_{IN} = 12 V, T_A = 25°C		540		µs

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6.8 Typical Characteristics

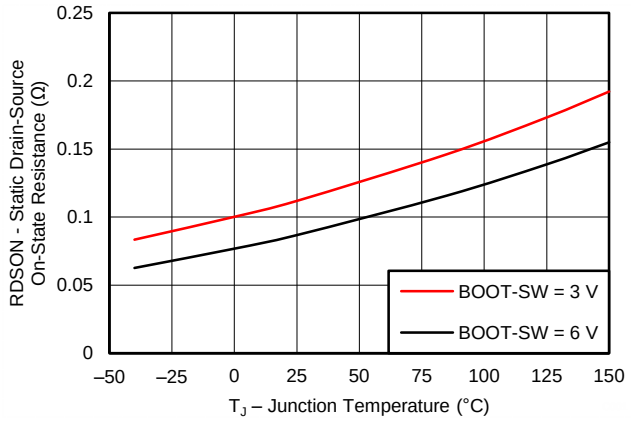

Figure 1. ON-Resistance vs Junction Temperature

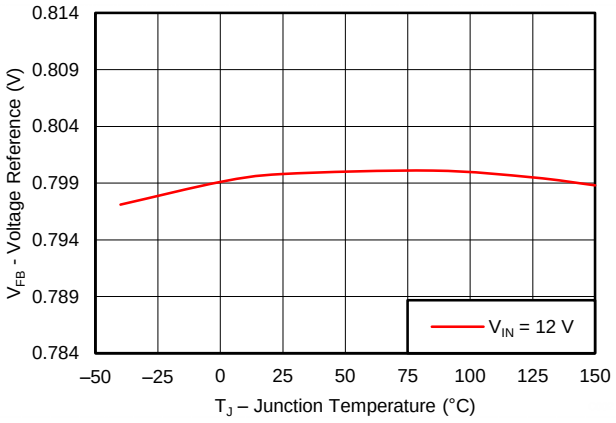

Figure 2. Voltage Reference vs Junction Temperature

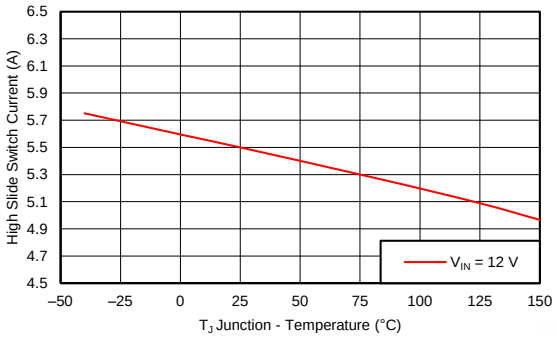

Figure 3. Switch Current Limit vs Junction Temperature

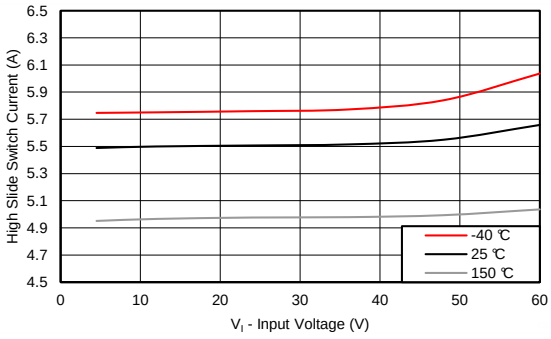

Figure 4. Switch Current Limit vs Input Voltage

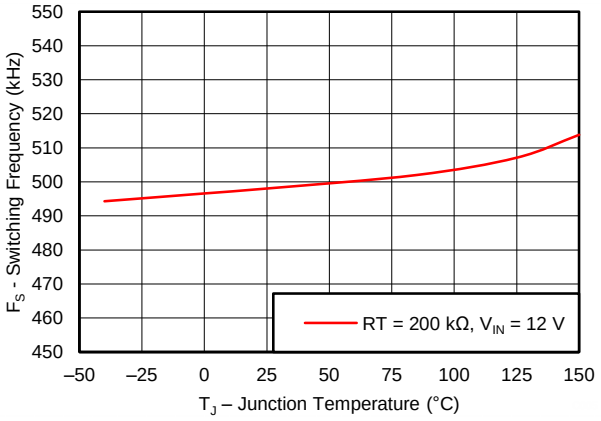

Figure 5. Switching Frequency vs Junction Temperature

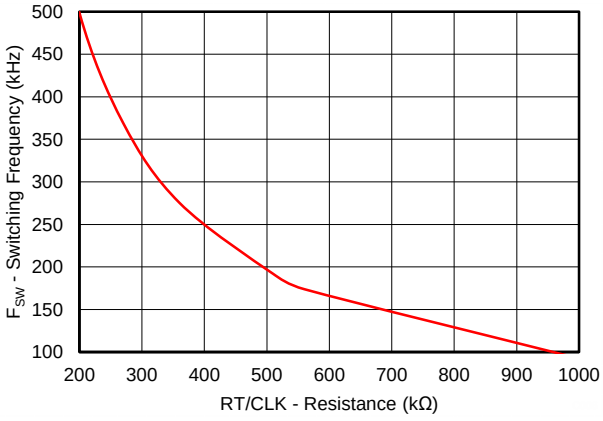

Figure 6. Switching Frequency vs RT/CLK Resistance Low-Frequency Range

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Typical Characteristics (continued)

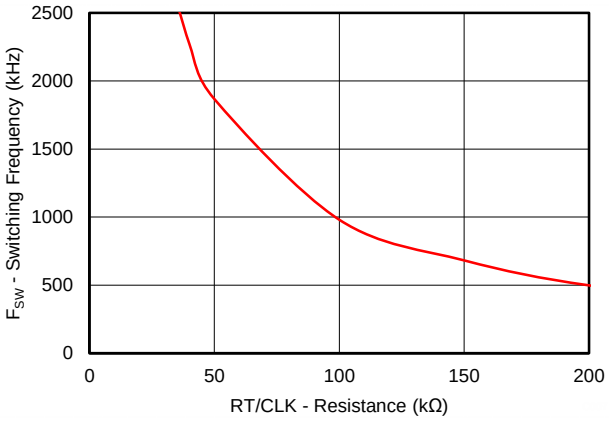

Figure 7. Switching Frequency vs RT/CLK Resistance High-Frequency Range

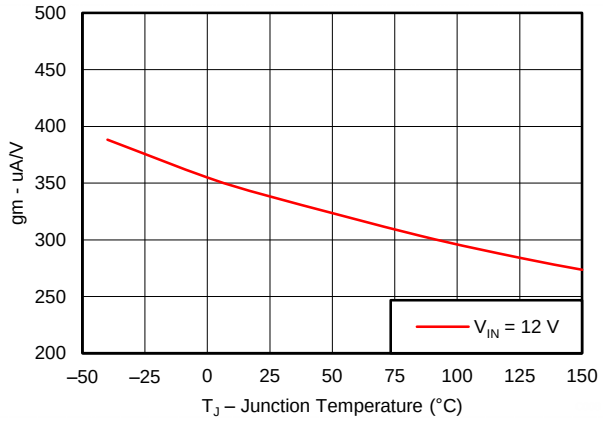

Figure 8. EA Transconductance vs Junction Temperature

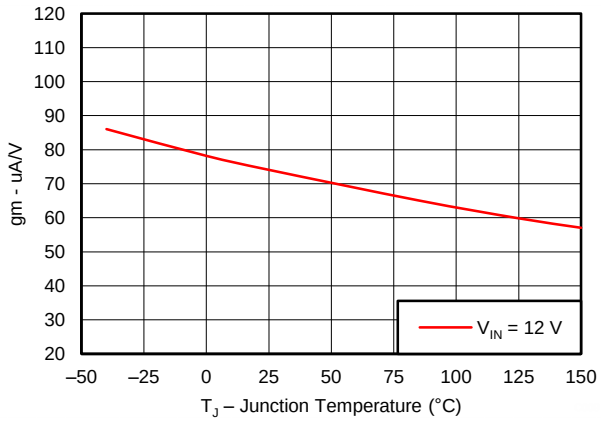

Figure 9. EA Transconductance During Soft Start vs Junction Temperature

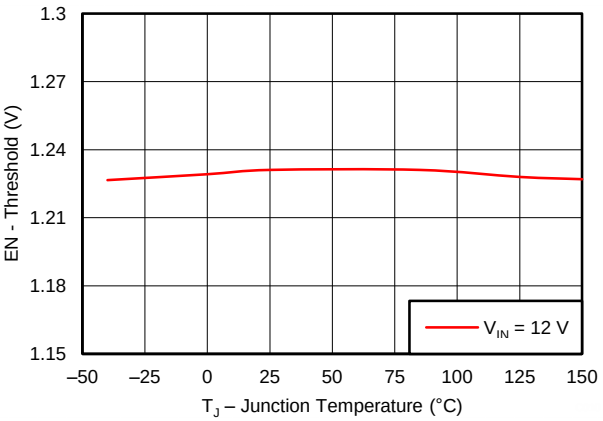

Figure 10. EN Pin Voltage vs Junction Temperature

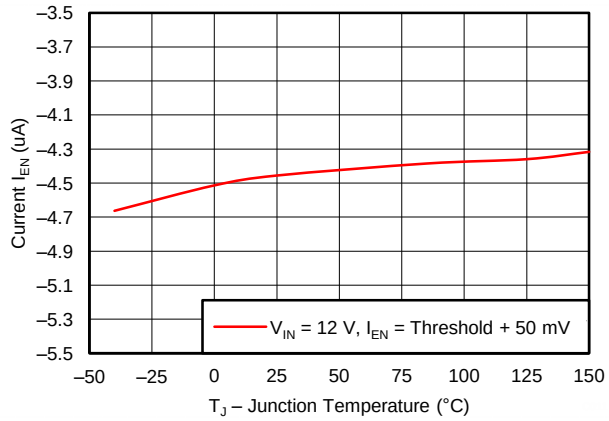

Figure 11. EN Pl Current vs Junction Temperature

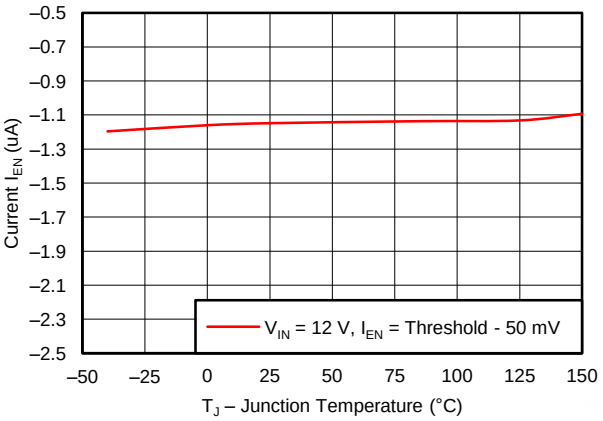

Figure 12. EN Pin Current vs Junction Temperature

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Typical Characteristics (continued)

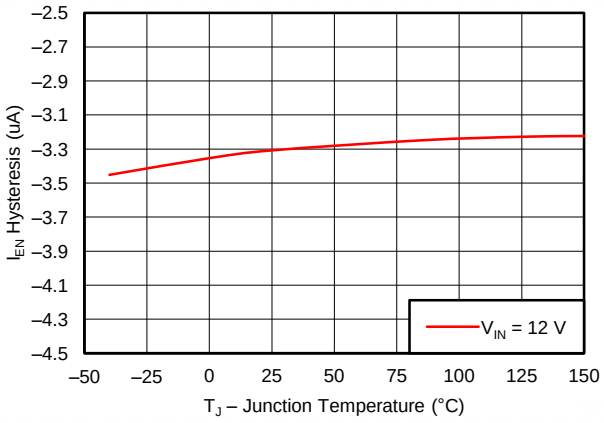

Figure 13. EN Pin Current Hysteresis vs Junction Temperature

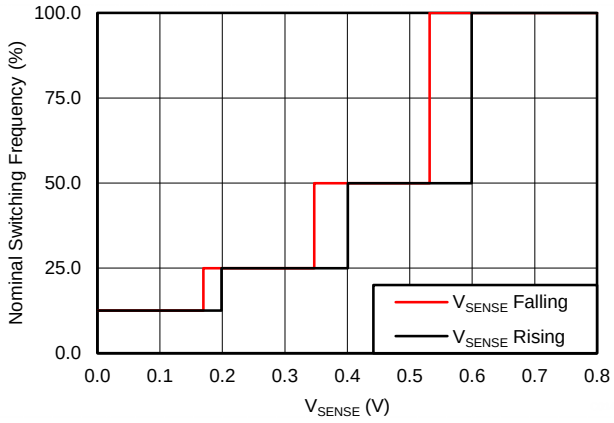

Figure 14. Switching Frequency vs FB

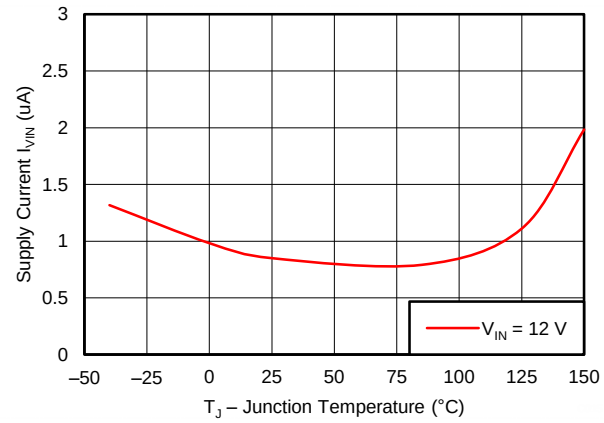

Figure 15. Shutdown Supply Current vs Junction Temperature

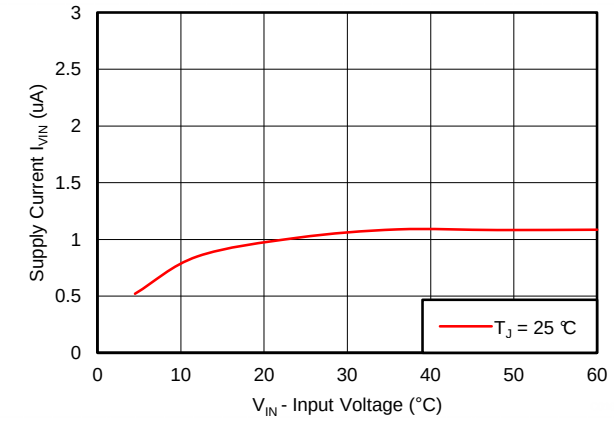

Figure 16. Shutdown Supply Current vs Input Voltage (V_{IN})

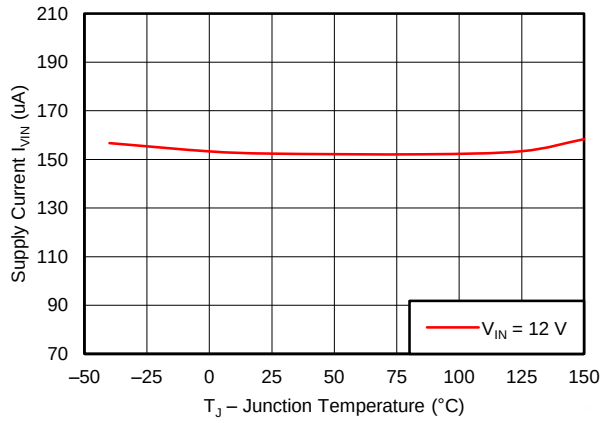

Figure 17. V_{IN} Supply Current vs Junction Temperature

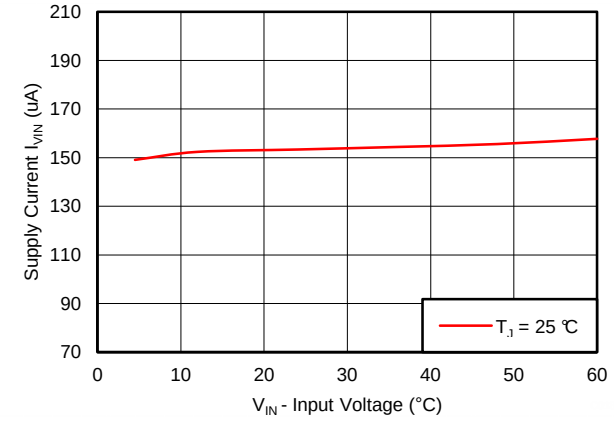

Figure 18. V_{IN} Supply Current vs Input Voltage

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Typical Characteristics (continued)

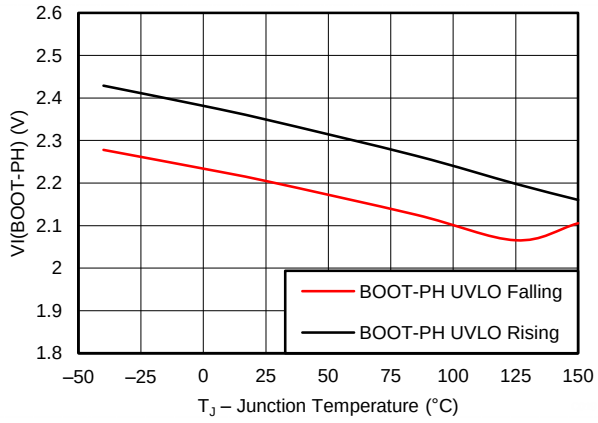

Figure 19. BOOT-SW UVLO vs Junction Temperature

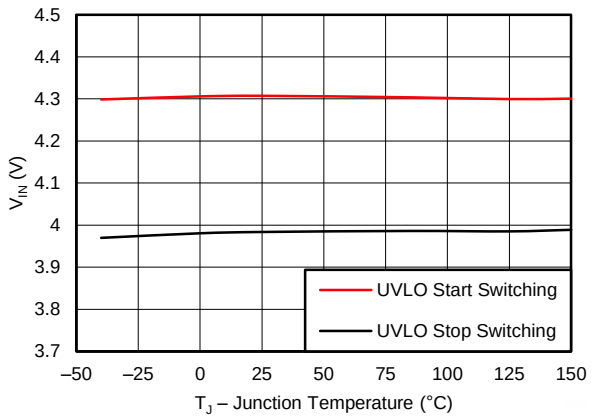

Figure 20. Input Voltage UVLO vs Junction Temperature

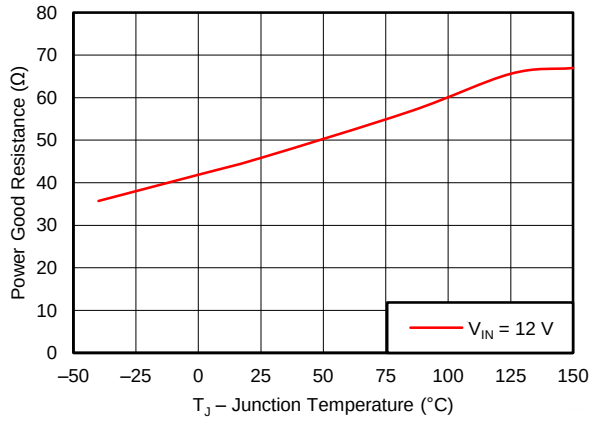

Figure 21. PWRGD ON-Resistance vs Junction Temperature

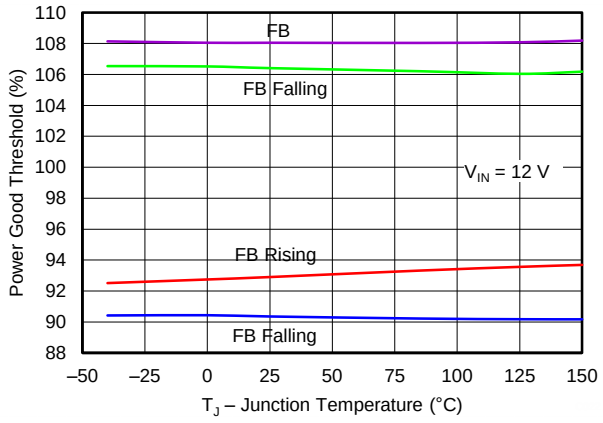

Figure 22. PWRGD Threshold vs Junction Temperature

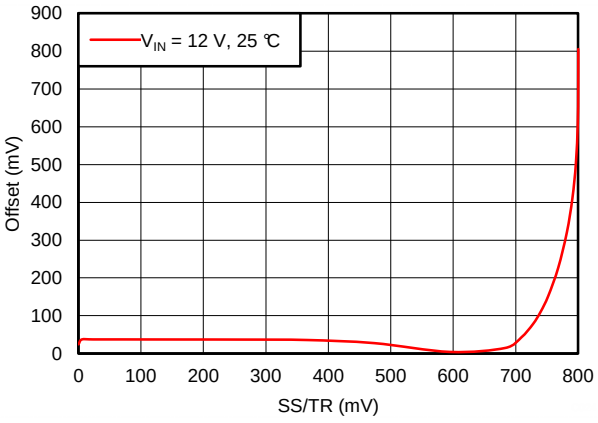

Figure 23. SS/TR to FB Offset vs FB

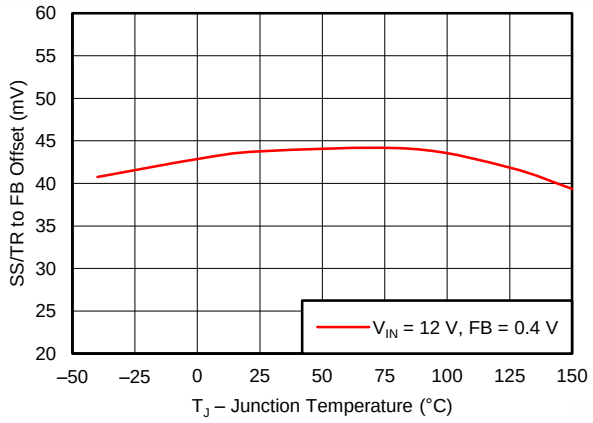

Figure 24. SS/TR to FB Offset vs Temperature

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Typical Characteristics (continued)

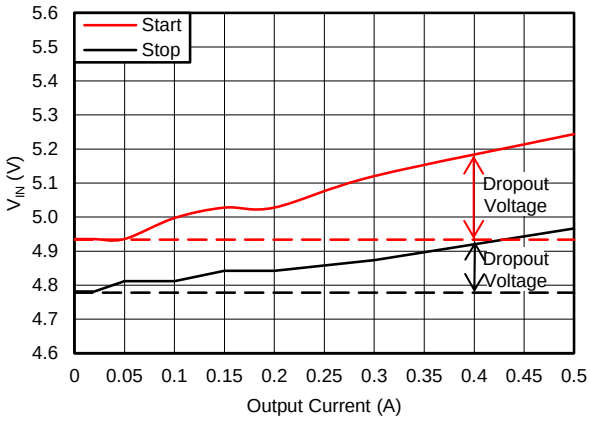

Figure 25. 5-V Start and Stop Voltage
(see *Low Dropout Operation and Bootstrap Voltage (BOOT)*)

7 Detailed Description

7.1 Overview

The TPS54361 device is a 60-V, 3.5-A, step-down (buck) regulator with an integrated high-side N-channel MOSFET. The device implements constant-frequency current-mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 kHz to 2500 kHz allows either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK pin. The device has an internal phase-locked loop (PLL) connected to the RT/CLK pin that synchronizes the power switch turnon to a falling edge of an external clock signal.

The TPS54361 device has a default input start-up voltage of 4.3 V typical. The EN pin adjusts the input voltage undervoltage lockout (UVLO) threshold with two external resistors. An internal pullup current source enables operation when the EN pin is floating. The operating current is 152 μA under no load condition when not switching. When the device is disabled, the supply current is 2 μA.

The integrated 87-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 3.5 A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW pins. The TPS54361 device reduces the external component count by integrating the bootstrap recharge diode. The BOOT pin capacitor voltage is monitored by a UVLO circuit which turns off the high-side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54361 device to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8-V feedback reference.

Output overvoltage transients are minimized by an overvoltage protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET is turned off and remains off until the output voltage is less than 106% of the desired output voltage.

The SS/TR (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor must be connected to the pin to adjust the soft-start time. A resistor-divider can be connected to the pin for critical power supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault, UVLO fault or a disabled condition. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help maintain control of the inductor current.

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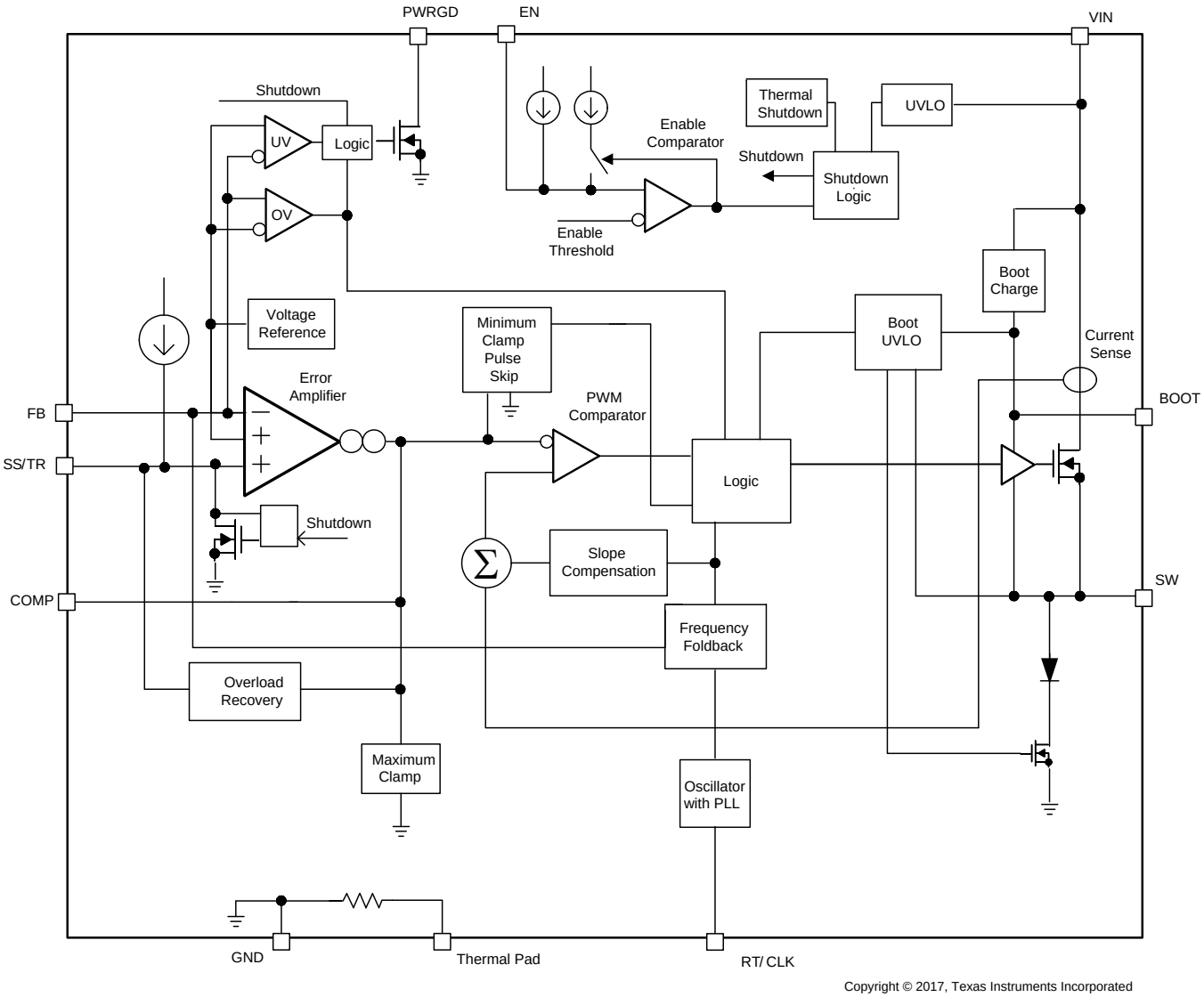
7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The TPS54361 device uses fixed-frequency peak current-mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output at the COMP pin controls the high-side power-switch current. When the high-side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch is turned off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements current-limiting by clamping the COMP pin voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP pin.

7.3.2 Slope Compensation Output Current

The TPS54361 device adds a compensating ramp to the MOSFET switch-current sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty-cycle range.

Feature Description (continued)

7.3.3 Pulse-Skip Eco-Mode

The TPS54361 device operates in a pulse-skipping Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. The device enters Eco-mode if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse-skipping current threshold. The pulse-skipping current threshold is the peak switch-current level corresponding to a nominal COMP voltage of 600 mV.

When in Eco-mode, the COMP pin voltage is clamped at 600 mV and the high-side MOSFET is inhibited. Because the device is not switching, the output voltage begins to decay. The voltage control-loop responds to the falling output voltage by increasing the COMP pin voltage. The high-side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-mode pulse-skipping threshold at which time the device again enters Eco-mode. The internal PLL remains operational when in Eco-mode. When operating at light load currents in Eco-mode, the switching transitions occur synchronously with the external clock signal.

During Eco-mode operation, the TPS54361 device senses and controls the peak switch current and not the average load current. Therefore the load current at which the device enters Eco-mode is dependent on the output inductor value. As the load current approaches zero, the device enters a pulse-skip mode during which it draws only a 152-μA input quiescent current. The circuit in Figure 46 enters Eco-mode at about a 25-mA output current and with no external load has an average input current of 260 μA.

7.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54361 device provides an integrated bootstrap voltage-regulator. A small capacitor between the BOOT and SW pins provides the gate-drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF. A ceramic capacitor with an X7R or X5R-grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the TPS54361 device operates at a 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V. When the voltage from BOOT to SW drops below 2.1 V, the high-side MOSFET turns off and an integrated low-side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low-side MOSFET at high output voltages, the small low-side MOSFET disables at 24-V output and re-enables when the output reaches 21.5 V.

Because the gate-drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode voltage and the printed circuit board (PCB) resistance.

The start and stop voltage for a typical 5-V output application is shown in Figure 25 where the input voltage is plotted versus load current. The start voltage is defined as the input voltage required to regulate the output within 1% of nominal. The stop voltage is defined as the input voltage at which the output drops by 5% or where switching stops.

During high duty-cycle (low-dropout) conditions, inductor current ripple increases when the BOOT capacitor is being recharged which results in an increase in output voltage ripple. Increased ripple occurs when the off time required to recharge the BOOT capacitor is longer than the high-side off time associated with cycle-by-cycle PWM control.

At heavy loads, the minimum input voltage must be increased to ensure a monotonic startup. Equation 1 calculates the minimum input voltage for this condition.

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Feature Description (continued)

$V_O max = Dmax \times (V_{VIN} min - I_O max \times R_{DS(on)} + V_d) - V_d - I_O max \times R_{dc}$

where

- Dmax ≥ 0.9
- V_d = Forward Drop of the Catch Diode
- $R_{DS(on)} = 1 / (-0.3 \times VB2SW^2 + 3.577 \times VB2SW - 4.246)$
- $VB2SW = VBOOT + V_d$
- $VBOOT = (1.41 \times V_{VIN} - 0.554 - V_d \times f_{sw} \times 10^{-6} - 1.847 \times 10^3 \times IB2SW) / (1.41 + f_{sw} \times 10^{-6})$
- $IB2SW = 100 \times 10^{-6}$ A (1)

7.3.5 Error Amplifier

The TPS54361 voltage-regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 350 μS during normal operation. During soft-start operation, the transconductance is reduced to 78 μS and the error amplifier is referenced to the internal soft-start voltage.

The frequency compensation components (capacitor, series resistor, and capacitor) are connected between the error amplifier output COMP pin and GND pin.

7.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8-V ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap reference circuit. The output voltage is set by a resistor divider from the output node to the FB pin. Divider resistors with a 1%-tolerance or better are recommended. Select the low-side resistor R_{LS} for the desired divider current and use Equation 2 to calculate R_{HS}. To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current may become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \quad (2)$$

7.3.7 Enable and Adjust Undervoltage Lockout

The TPS54361 device enables when the VIN pin voltage rises above 4.3 V and the EN pin voltage exceeds the enable threshold of 1.2 V. The TPS54361 device disables when the VIN pin voltage falls below 4 V or when the EN pin voltage is below 1.2 V. The EN pin has an internal pullup current source, I_1, of 1.2 μA that enables operation of the TPS54361 device when the EN pin floats.

If an application requires a higher undervoltage lockout (UVLO) threshold, use the circuit shown in Figure 26 to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, an additional 3.4 μA of hysteresis current, I_{HYS}, is sourced out of the EN pin. When the EN pin is pulled below 1.2 V, the 3-μA I_{HYS} current is removed. This additional current facilitates the adjustable input-voltage UVLO hysteresis. Use Equation 3 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use Equation 4 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (that is, from 4.5 V to 9 V) and withstand high input voltages (that is, from 40 V to 60 V), the EN pin experiences a voltage greater than the absolute maximum voltage of 8.4 V during the high input voltage condition. To avoid exceeding this voltage when using the EN resistors, the EN pin is clamped internally with a 5.8-V Zener diode that sinks up to 150 μA.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (3)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \quad (4)$$

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Feature Description (continued)

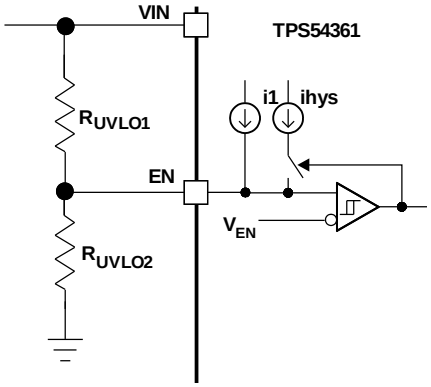

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Figure 26. Adjustable Undervoltage Lockout (UVLO)

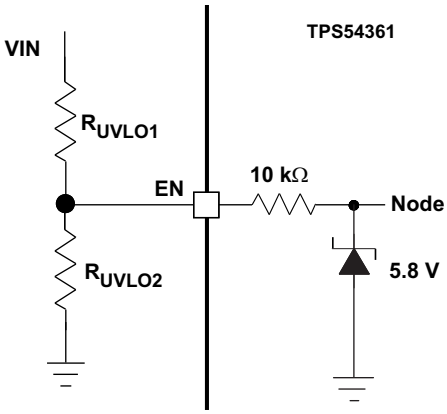

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Figure 27. Internal EN Pin Clamp

7.3.8 Soft-Start/Tracking Pin (SS/TR)

The TPS54361 device effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power-supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a soft-start time. The TPS54361 has an internal pullup current source of 1.7 μA that charges the external soft-start capacitor. The calculations for the soft-start time (10% to 90%) are shown in Equation 5. The voltage reference (V_{REF}) is 0.8 V and the soft-start current (I_{SS}) is 1.7 μA. The soft-start capacitor must remain lower than 0.47 μF and greater than 0.47 nF.

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V) \times 0.8} \quad (5)$$

At power up, the TPS54361 device does not start switching until the soft-start pin is discharged to less than 54 mV to ensure a proper power up, see Figure 28.

Also, during normal operation, the TPS54361 device stops switching and the SS/TR must discharge to 54 mV when one of the following occurs: the VIN UVLO is exceeded, the EN pin pulled below 1.2 V, or a thermal shutdown event occurs.

The FB voltage follows the SS/TR pin voltage with a 42 mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 2.7 V typically as shown in Figure 28.

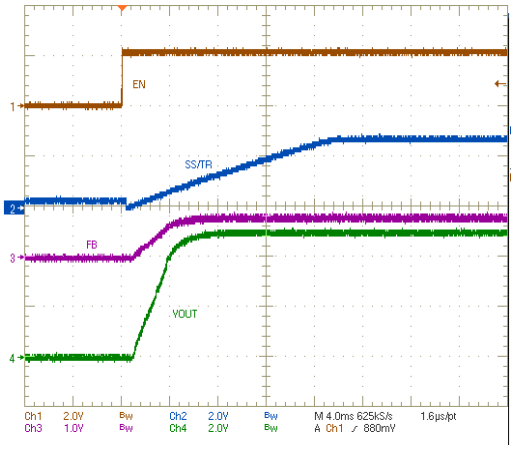

Figure 28. Operation of SS/TR Pin When Starting

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Feature Description (continued)

7.3.9 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins. The sequential method can be implemented using an open drain output of a power on reset pin of another device. The sequential method is illustrated in Figure 29 using two TPS54361 devices. The power good is connected to the EN pin on the TPS54361 which enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms start-up delay. Figure 30 shows the results of Figure 29.

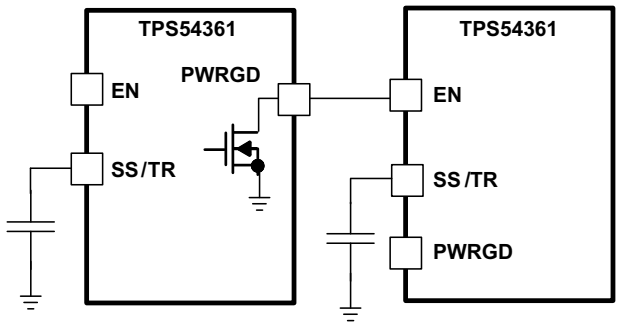

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Figure 29. Schematic for Sequential Start-Up Sequence

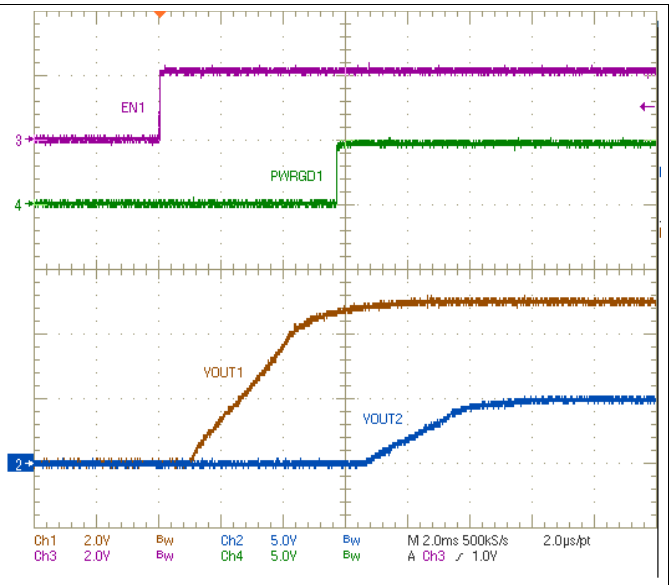

Figure 30. Sequential Startup Using EN and PWRGD

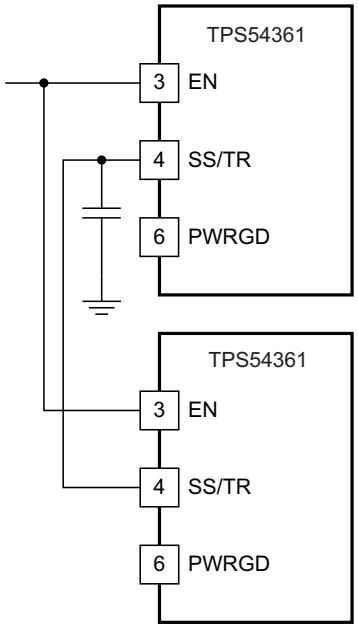

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Figure 31. Schematic for Ratiometric Start-Up Sequence

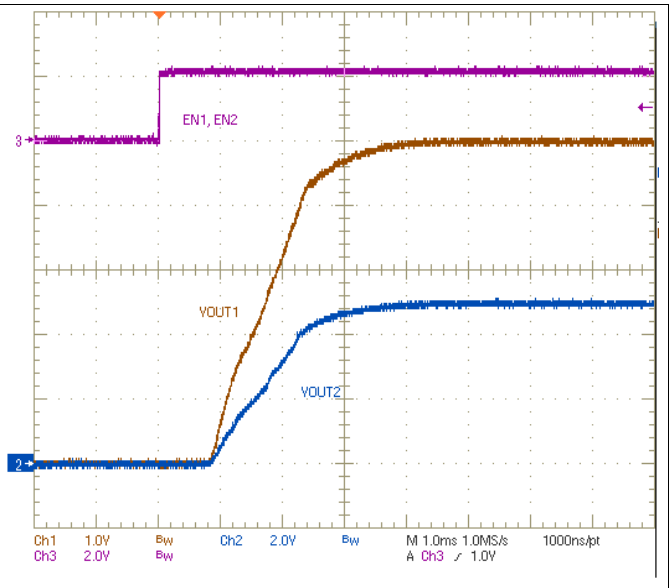

Figure 32. Ratiometric Startup Using Coupled SS/TR pins

Feature Description (continued)

Figure 31 shows a method for ratiometric start up sequence by connecting the SS/TR pins together. The regulator outputs ramps up and reaches regulation at the same time. When calculating the soft-start time the pullup current source must be doubled in Equation 5. Figure 32 shows the results of Figure 31.

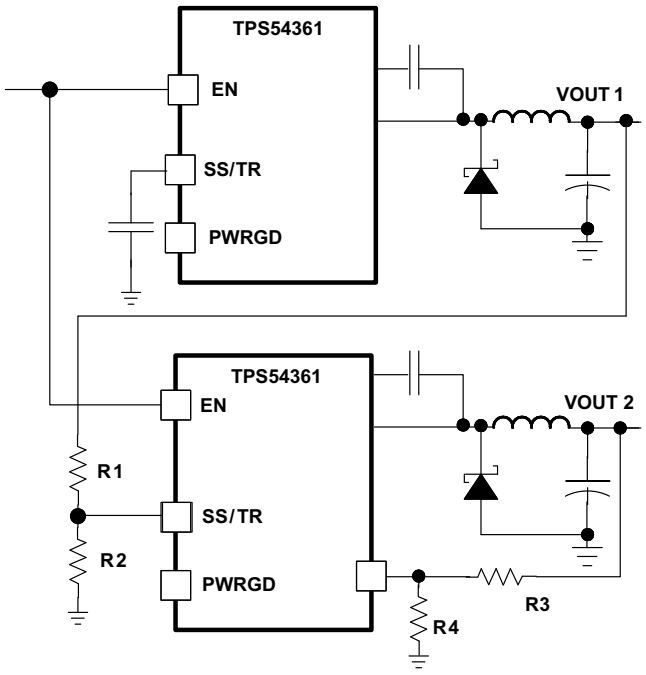

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Figure 33. Schematic for Ratiometric and Simultaneous Start-Up Sequence

Ratiometric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 33 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 6 and Equation 7, the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after or at the same time as V_{OUT1}. Equation 8 is the voltage difference between V_{OUT1} and V_{OUT2} at the 95% of nominal output regulation.

The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to FB offset ($V_{SSoffset}$) in the soft-start circuit and the offset created by the pullup current source (I_{SS}) and tracking resistors, the $V_{SSoffset}$ and I_{SS} are included as variables in the equations.

To design a ratiometric start up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 6 through Equation 8 for ΔV. Equation 8 results in a positive number for applications which the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

Because the SS/TR pin must be pulled below 54 mV before starting after an EN, UVLO or thermal shutdown fault, careful selection of the tracking resistors is needed to ensure the device restarts after a fault. Make sure the calculated R1 value from Equation 6 is greater than the value calculated in Equation 9 to ensure the device can recover from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage the $V_{SSoffset}$ becomes larger as the soft-start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.5 V for a complete handoff to the internal voltage reference as shown in Figure 33.

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSoffset}}{I_{SS}} \quad (6)$$

$$R2 = \frac{V_{REF} \times R1}{V_{OUT2} + \Delta V - V_{REF}} \quad (7)$$

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Feature Description (continued)

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (8)$$

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (9)$$

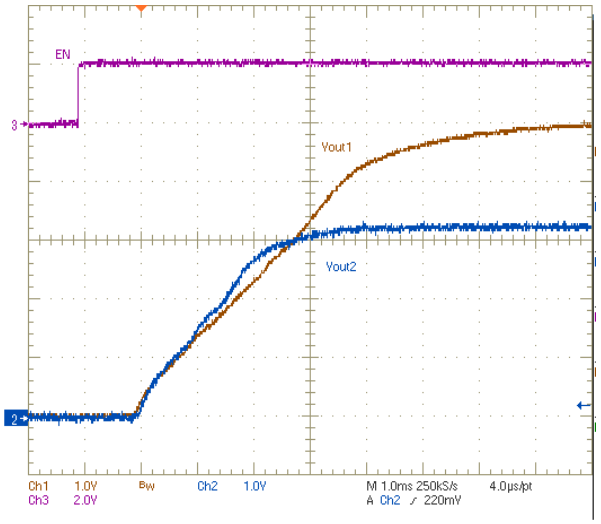

Figure 34. Ratiometric Startup With Tracking Resistors

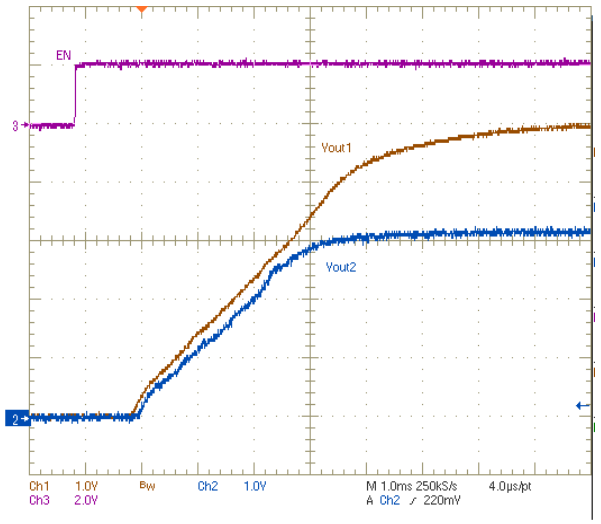

Figure 35. Ratiometric Startup With Tracking Resistors

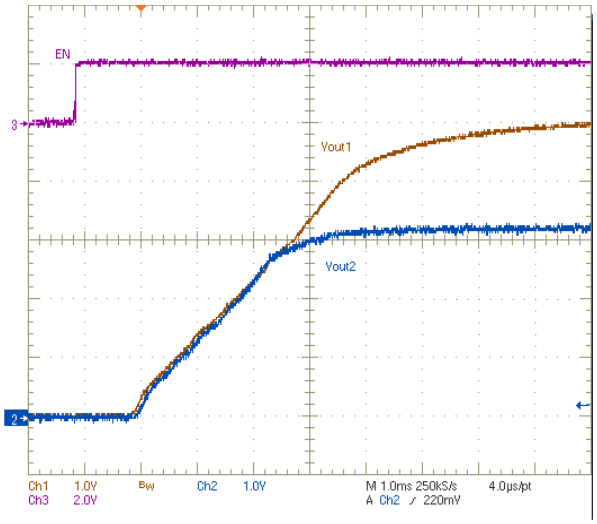

Figure 36. Simultaneous Startup With Tracking Resistor

7.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK) Pin)

The switching frequency of the TPS54361 is adjustable over a wide range from 100 kHz to 2500 kHz by placing a resistor between the RT/CLK pin and GND pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 10 or Equation 11 or the curves in Figure 5 and Figure 6. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time must be considered. The minimum controllable on time is typically 100 ns which limits the maximum operating frequency in applications with high input to output step down ratios. The maximum switching frequency is also limited by the frequency foldback circuit. A more detailed discussion of the maximum switching frequency is provided in *Maximum Switching Frequency*.

$$R_T\ (k\Omega) = \frac{101756}{f\text{sw}\ (kHz)^{1.008}} \quad (10)$$

Feature Description (continued)

$$f\text{sw (kHz)} = \frac{92417}{\text{RT (k}\Omega)^{0.991}} \quad (11)$$

7.3.11 Synchronization to RT/CLK Pin

The RT/CLK pin can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature connect a square wave to the RT/CLK pin through either circuit network shown in Figure 37. The square wave applied to the RT/CLK pin must switch lower than 0.5 V and higher than 2 V and have a pulse width greater than 15 ns. The synchronization frequency range is 160 kHz to 2300 kHz. The rising edge of the SW is synchronized to the falling edge of RT/CLK pin signal. The external synchronization circuit must be designed such that the default frequency set resistor is connected from the RT/CLK pin to ground when the synchronization signal is off. When using a low impedance signal source, the frequency set resistor is connected in parallel with an AC coupling capacitor to a termination resistor (for example, 50 Ω) as shown in Figure 37. The two resistors in series provide the default frequency setting resistance when the signal source is turned off. The sum of the resistance must set the switching frequency close to the external CLK frequency. AC coupling the synchronization signal through a 10-pF ceramic capacitor to RT/CLK pin is recommended.

The first time the RT/CLK is pulled above the PLL threshold the TPS54361 switches from the RT resistor free-running frequency mode to the PLL synchronized mode. The internal 0.5-V voltage source is removed and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and locks onto the external clock frequency within 78 ms. During the transition from the PLL mode to the resistor programmed mode, the switching frequency falls to 150 kHz and then increases or decreases to the resistor programmed frequency when the 0.5-V bias voltage is reapplied to the RT/CLK resistor.

The switching frequency is divided by 8, 4, 2, and 1 as the FB pin voltage ramps from 0 to 0.8 V. The device implements a digital frequency foldback to enable synchronizing to an external clock during normal start-up and fault conditions. Figure 38, Figure 39 and Figure 40 show the device synchronized to an external system clock in continuous conduction mode (CCM), discontinuous conduction (DCM), and pulse-skip mode (Eco-Mode).

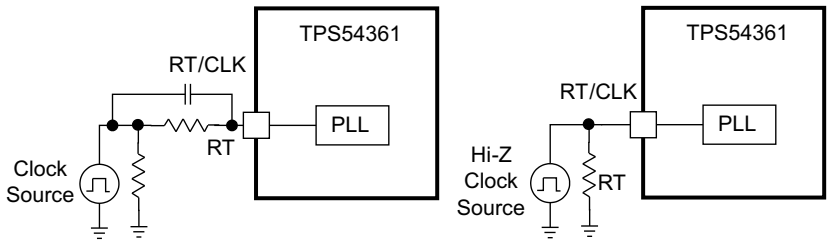

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Figure 37. Synchronizing to a System Clock

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Feature Description (continued)

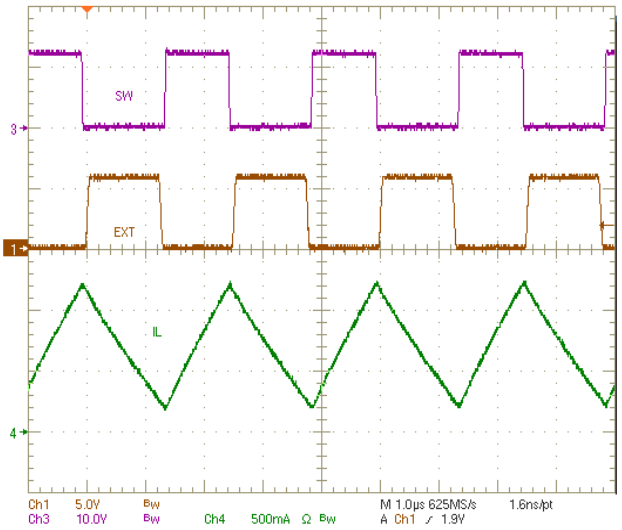

Figure 38. Plot of Synchronizing in CCM

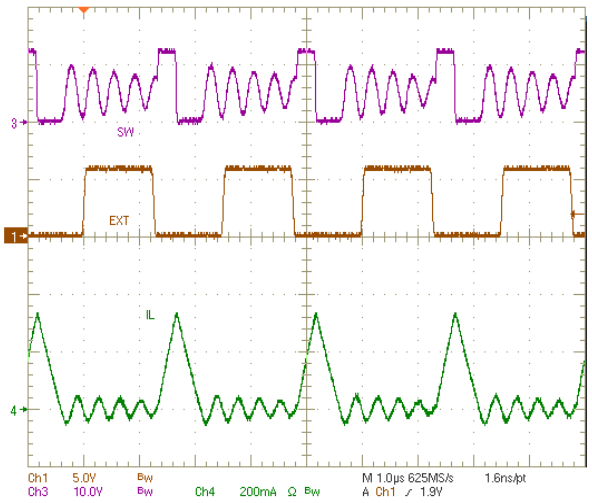

Figure 39. Plot of Synchronizing in DCM

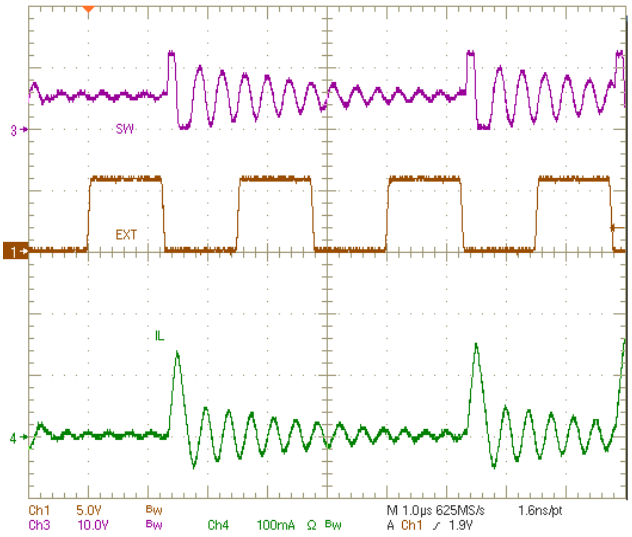

Figure 40. Plot of Synchronizing in Eco-mode

7.3.12 Maximum Switching Frequency

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54361 implements a frequency foldback. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The TPS54361 uses a digital frequency foldback to enable synchronization to an external clock during normal start-up and fault conditions. During short-circuit events, the inductor current may exceed the peak current limit because of the high input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency foldback ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency foldback protection. Equation 13 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to $V_{OUT(SC)}$. The selected operating frequency must not exceed the calculated value.

Feature Description (continued)

Equation 12 calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value causes the regulator to skip switching pulses to achieve the low duty cycle required to regulate the output at maximum input voltage.

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right) \quad (12)$$

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right)$$

where

- I_O is the output current
- I_{CL} is the current limit
- R_{dc} is the inductor resistance
- V_{IN} is the maximum input voltage
- V_{OUT} is the output voltage
- $V_{OUT(SC)}$ is the output voltage during short
- V_d is the diode voltage drop
- $R_{DS(on)}$ is the switch ON-resistance
- t_{ON} is the controllable ON-time
- f_{DIV} is the frequency divide equals (1, 2, 4, or 8) (13)

7.3.13 Accurate Current Limit Operation

The TPS54361 implements peak current mode control in which the COMP pin voltage controls the peak current of the high-side MOSFET. A signal proportional to the high-side switch current and the COMP pin voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP pin high. The error amplifier output is clamped internally at a level which sets the peak switch current limit. The TPS54361 provides an accurate current limit threshold with a typical current limit delay of 60 ns. With smaller inductor values, the delay results in a higher peak inductor current. The relationship between the inductor value and the peak inductor current is shown in Figure 41.

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Feature Description (continued)

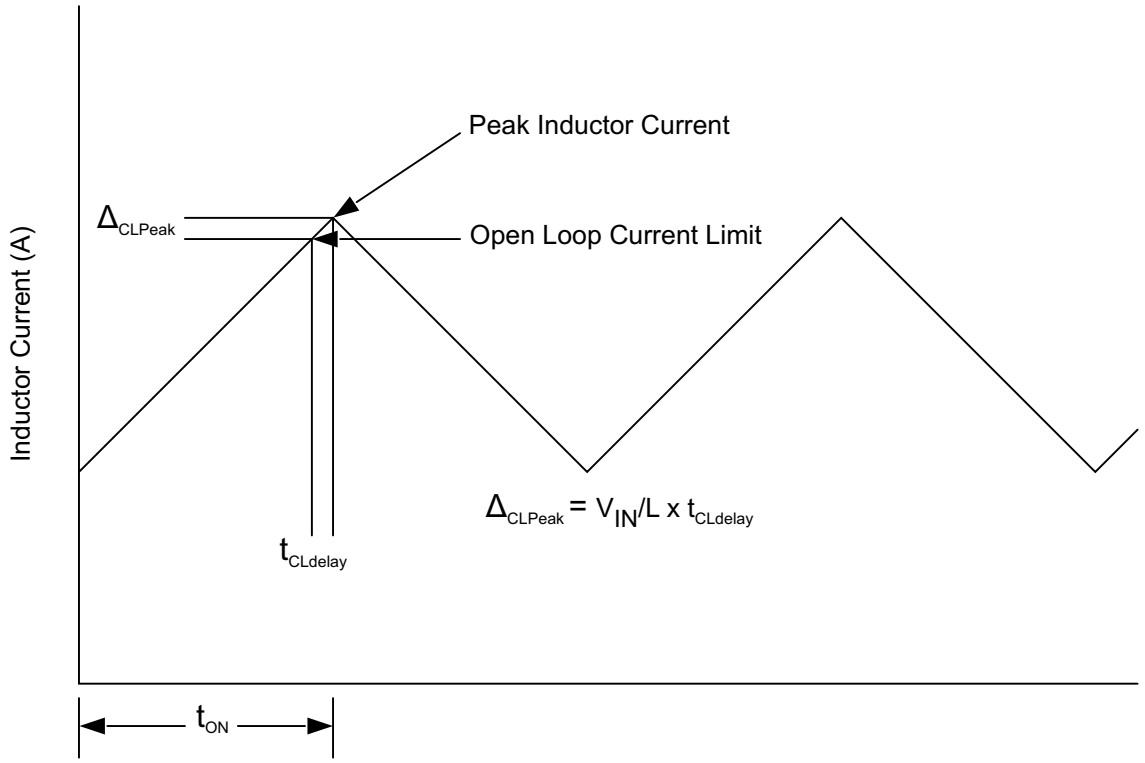

Figure 41. Current Limit Delay

7.3.14 Power Good (PWRGD Pin)

The PWRGD pin is an open-drain output. Once the FB pin is between 93% and 106% of the internal voltage reference the PWRGD pin is deasserted and the pin floats. TI recommends a pullup resistor of 1 kΩ to a voltage source that is 5.5 V or less. A higher pullup resistance reduces the amount of current drawn from the pullup voltage source when the PWRGD pin is asserted low. A lower pullup resistance reduces the switching noise seen on the PWRGD signal. The PWRGD is in a defined state once the VIN input voltage is greater than 2 V but with reduced current sinking capability. The PWRGD achieves full current-sinking capability as VIN input voltage approaches 3 V.

The PWRGD pin is pulled low when the FB is lower than 90% or greater than 108% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the UVLO or thermal shutdown are asserted or the EN pin pulled low.

7.3.15 Overvoltage Protection

The TPS54361 incorporates an output overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier increases to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power supply output voltage can increase faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low value output capacitor by comparing the FB pin voltage to the rising OVP threshold which is nominally 108% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high-side MOSFET is immediately disabled to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high-side MOSFET resumes normal operation.

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Feature Description (continued)

7.3.16 Thermal Shutdown

The TPS54361 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high-side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature falls below 164°C, the device reinitiates the power-up sequence controlled by discharging the SS/TR pin.

7.3.17 Small Signal Model for Loop Response

Figure 42 shows a simplified equivalent model for the TPS54361 control loop which can be simulated to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{ea} of 350 µS. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_O and capacitor C_O model the open loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a provides the small signal response of the frequency compensation. Plotting a/b provides the small signal response of the overall loop. The dynamic loop response can be evaluated by replacing R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous conduction mode (CCM) operation.

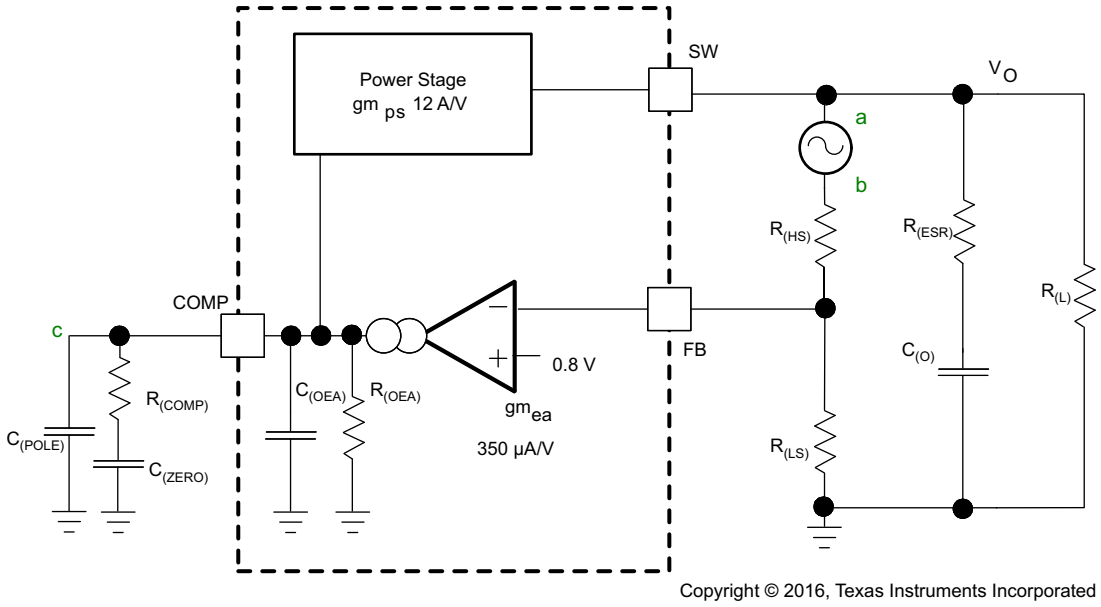

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Figure 42. Small Signal Model for Loop Response

7.3.18 Simple Small Signal Model for Peak Current Mode Control

Figure 43 describes a simple small signal model that can be used to design the frequency compensation. The TPS54361 device power stage can be approximated by a voltage-controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 14 and consists of a DC gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node *c* in Figure 42) is the power stage transconductance, gm_{ps}. The gm_{ps} for the TPS54361 device is 12 A/V. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The combined effect is highlighted by the dashed line in the right half of Figure 43. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin is increased by the ESR zero of the output capacitor (see Equation 17).

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Feature Description (continued)

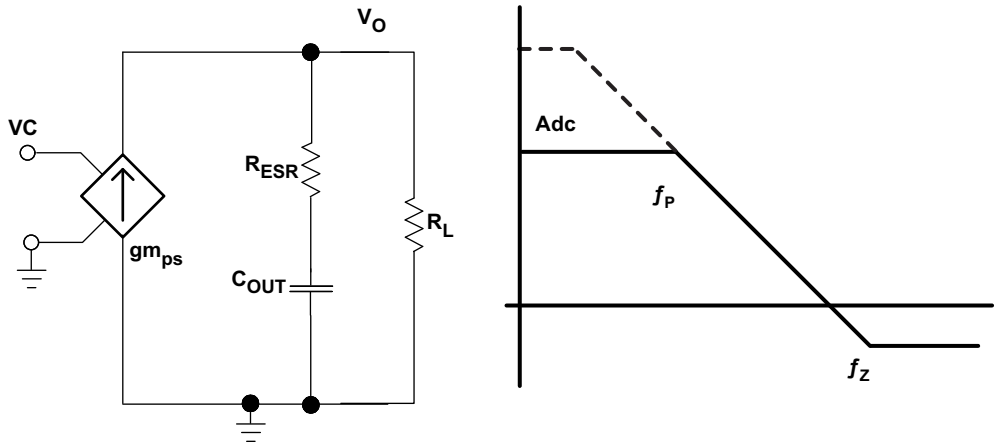

Figure 43. Simple Small Signal Model and Frequency Response for Peak Current Mode Control

$$\frac{V_{OUT}}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

7.3.19 Small Signal Model for Frequency Compensation

The TPS54361 uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 44. Type 2 circuits are typically implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 18 and Equation 19 relate the frequency response of the amplifier to the small signal model in Figure 44. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 44. See the application section for a design example using a Type 2A network with a low ESR output capacitor.

Equation 18 through Equation 27 are provided as a reference. An alternative is to use WEBENCH software tools to create a design based on the power supply requirements.

Feature Description (continued)

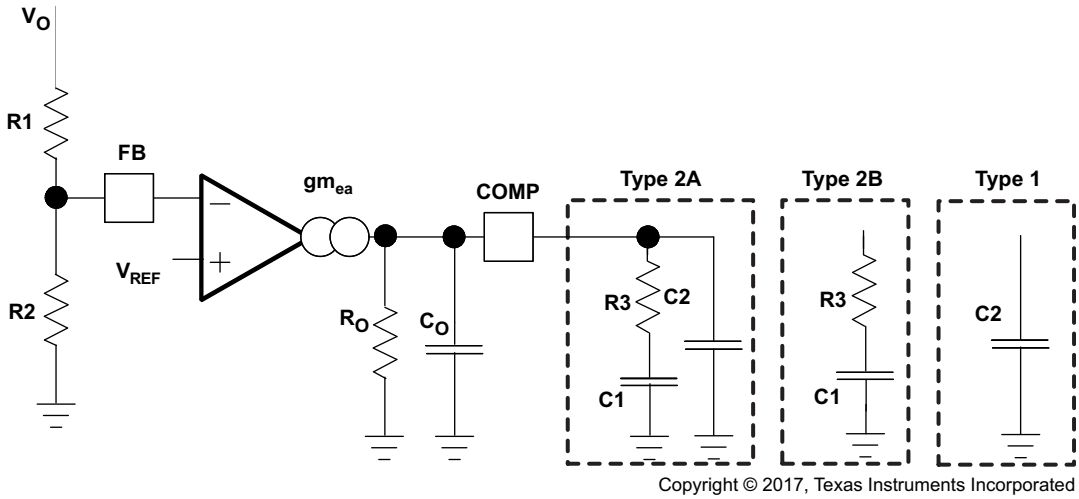

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Figure 44. Types of Frequency Compensation

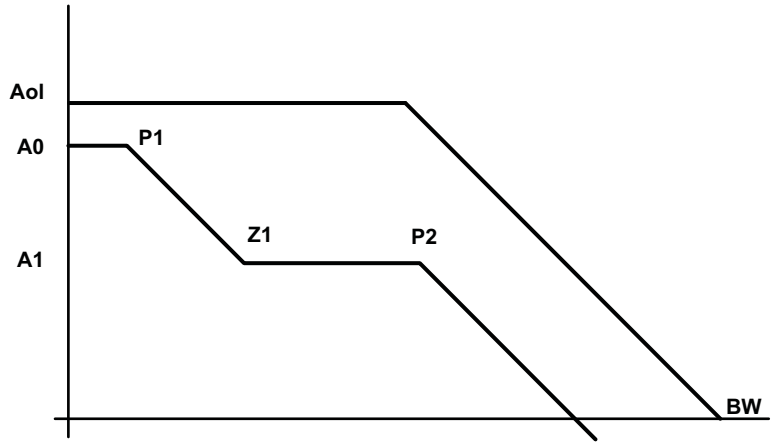

Figure 45. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$R_O = \frac{AoI(V/V)}{gm_{ea}} \quad (18)$$

$$C_O = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \quad (19)$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \left(\frac{s}{2\pi \times f_{P2}}\right)\right)} \quad (20)$$

$$A0 = gm_{ea} \times R_O \times \frac{R2}{R1 + R2} \quad (21)$$

$$A1 = gm_{ea} \times R_O \,||\, R3 \times \frac{R2}{R1 + R2} \quad (22)$$

$$P1 = \frac{1}{2\pi \times R_O \times C1} \quad (23)$$

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Feature Description (continued)

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (24)$$

$$P2 = \frac{1}{2\pi \times R3 || R_O \times (C2 + C_O)} \text{ Type 2A} \quad (25)$$

$$P2 = \frac{1}{2\pi \times R3 || R_O \times C_O} \text{ Type 2B} \quad (26)$$

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{ Type 1} \quad (27)$$

7.4 Device Functional Modes

The TPS54361 is designed to operate with input voltages above 4.5 V. When the VIN voltage is above the 4.3 V typical rising UVLO threshold and the EN voltage is above the 1.2 V typical threshold the device is active. If the VIN voltage falls below the typical 4-V UVLO turnoff threshold, the device stops switching. If the EN voltage falls below the 1.2-V threshold the device stops switching and enters a shutdown mode with low supply current of 2 µA typical.

The TPS54361 will operate in CCM when the output current is enough to keep the inductor current above 0 A at the end of each switching period. As a nonsynchronous converter, it will enter DCM at low output currents when the inductor current falls to 0 A before the end of a switching period. At very low output current the COMP voltage will drop to the pulse-skipping threshold and the device operates in a pulse-skipping Eco-mode. In this mode, the high-side MOSFET does not switch every switching period. This operating mode reduces power loss while keeping the output voltage regulated. For more information on Eco-mode see the *Pulse-Skip Eco-Mode* section.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54361 device is a 60-V, 3.5-A, step-down regulator with an integrated high-side MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3.5 A. Example applications are: 12 V, 24 V, and 48 V industrial, automotive, and communications power systems. Use the following design procedure to select component values for the TPS54361 device. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors. Calculations can be done with the excel spreadsheet (SLVC452) located on the product page. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an interactive design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Applications

8.2.1 Buck Converter With 7-V to 60-V Input and 5-V at 3.5-A Output

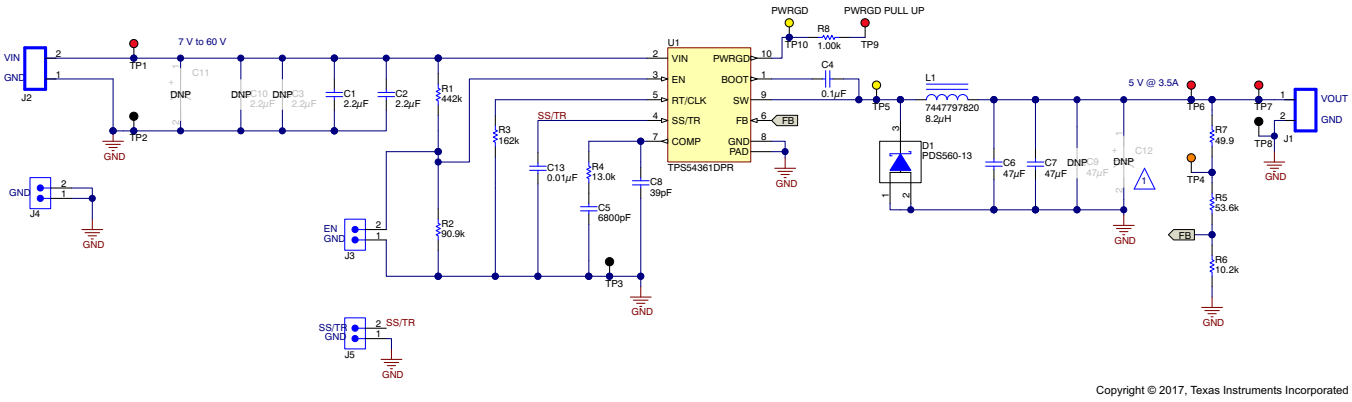

Figure 46. 5-V Output TPS54361 Design Example

8.2.1.1 Design Requirements

A few parameters must be known in order to start the design process. These requirements are typically determined at the system level. This example is designed to the known parameters in Table 1:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output Voltage	5 V
Transient Response 0.875-A to 2.625-A Load Step	ΔV_{OUT} = ±4 %
Maximum Output Current	3.5 A
Input Voltage	12 V nominal 7 V to 60 V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	6.5 V
Stop Input Voltage (falling VIN)	5 V

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8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS54361-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Selecting the Switching Frequency

The first step is to choose a switching frequency for the regulator. Typically, the designer uses the highest switching frequency possible because the highest switching frequency produces the smallest solution size. High switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum ON-time of the internal power switch, the input voltage, the output voltage, and the frequency foldback protection.

Equation 12 and Equation 13 must be used to calculate the upper limit of the switching frequency for the regulator. Choose the lower value result from the two equations. Switching frequencies higher than these values results in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 100 ns for the TPS54361. For this example, the output voltage is 5 V and the maximum input voltage is 60 V, which allows for a maximum switch frequency up to 960 kHz to avoid pulse skipping from Equation 12. To ensure overcurrent runaway is not a concern during short circuits use Equation 13 to determine the maximum switching frequency for frequency foldback protection. With a maximum input voltage of 60 V, assuming a diode voltage of 0.7 V, inductor resistance of 25 mΩ, switch resistance of 89 mΩ, a current limit value of 4.7 A, and short-circuit output voltage of 0.1 V, the maximum switching frequency is 1220 kHz.

For this design, a lower switching frequency of 600 kHz is chosen to operate comfortably below the calculated maximums. To determine the timing resistance for a given switching frequency, use Equation 10 or the curve in Figure 6. The switching frequency is set by resistor R_3 shown in Figure 46. For 600-kHz operation, the closest standard value resistor is 162 kΩ.

$$f_{SW(maxskip)} = \frac{1}{135\ ns} \times \left(\frac{3.5\ A \times 25\ m\Omega + 5\ V + 0.7\ V}{60\ V - 3.5\ A \times 87\ m\Omega + 0.7\ V} \right) = 710\ kHz \quad (28)$$

$$f_{SW(shift)} = \frac{8}{135\ ns} \times \left(\frac{4.7\ A \times 25\ m\Omega + 0.1\ V + 0.7\ V}{60\ V - 4.7\ A \times 87\ m\Omega + 0.7\ V} \right) = 902\ kHz \quad (29)$$

$$RT\ (k\Omega) = \frac{101756}{600\ (kHz)^{1.008}} = 161\ k\Omega \quad (30)$$

8.2.1.2.3 Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 31.

K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however, the following guidelines may be used.

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For designs using low ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 may be desirable. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Because the inductor ripple current is part of the current mode PWM control system, the inductor ripple current must always be greater than 150 mA for stable PWM operation. In a wide input voltage regulator, choosing a relatively large inductor ripple current is best to provide sufficient ripple current with the input voltage at the minimum.

For this design example, K_{IND} = 0.3 and the minimum inductor value is calculated to be 7.3 µH. The nearest standard value is 8.2 µH. The RMS current and saturation current ratings of the inductor must not be exceeded. The RMS and peak inductor current can be found from Equation 33 and Equation 34. For this design, the RMS inductor current is 3.5 A and the peak inductor current is 3.97 A. The chosen inductor is a WE 7447797820, which has a saturation current rating of 5.8 A and an RMS current rating of 5.05 A.

As the equation set demonstrates, lower ripple currents reduce the output voltage ripple of the regulator but require a larger value of inductance. Selecting higher ripple currents increases the output voltage ripple of the regulator but allows for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch current limit of the TPS54361 which is nominally 5.5 A.

$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} = \frac{60\ V - 5\ V}{3.5\ A \times 0.3} \times \frac{5\ V}{60\ V \times 600\ kHz} = 7.3\ \mu H \quad (31)$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} = \frac{5\ V \times (60\ V - 5\ V)}{60\ V \times 8.2\ \mu H \times 600\ kHz} = 0.932\ A \quad (32)$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_O \times f_{SW}} \right)^2} = \sqrt{(3.5\ A)^2 + \frac{1}{12} \times \left(\frac{5\ V \times (60\ V - 5\ V)}{60\ V \times 8.2\ \mu H \times 600\ kHz} \right)^2} = 3.5\ A \quad (33)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 3.5\ A + \frac{0.932\ A}{2} = 3.97\ A \quad (34)$$

8.2.1.2.4 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for 2 clock cycles to maintain the output voltage within the specified range. Equation 35 shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, $f$sw is the regulators switching frequency, and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0.875 A to 2.625 A. Therefore, ΔI_{OUT} is 2.625 A – 0.875 A = 1.75 A and ΔV_{OUT} = 0.04 × 5 = 0.2 V. Using these numbers gives a minimum capacitance of 29.2 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be included in load step calculations.

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The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator can not sink current so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. A typical load step response is shown in Figure 47. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 36 calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where L_O is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the peak output voltage, and Vi is the initial voltage. For this example, the worst-case load step is from 2.625 A to 0.875 A. The output voltage increases during this load transition and the stated maximum in our specification is 4 % of the output voltage which makes $V_f = 1.04 \times 5 = 5.2$. Vi is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 36 yields a minimum capacitance of 25 µF.

Equation 37 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where $f$sw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. Equation 37 yields 7.8 µF.

Equation 38 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 38 indicates the ESR must be less than 27 mΩ.

The most stringent criteria for the output capacitor is 29 µF required to maintain the output voltage within regulation tolerance during a load transient.

Capacitance de-ratings for aging, temperature and dc bias increases this minimum value. For this example, two 47-µF, 10-V ceramic capacitors with 5 mΩ of ESR is used. The derated capacitance is 58 µF, well above the minimum required capacitance of 29 µF.

Capacitors are generally rated for a maximum ripple current that can be filtered without degrading capacitor reliability. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. Equation 39 can be used to calculate the RMS ripple current that the output capacitor must support. For this example, Equation 39 yields 269 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 1.75\ A}{600\ kHz \times 0.2\ V} = 29.2\ \mu F \quad (35)$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_I)^2\right)} = 8.2\ \mu H \times \frac{\left(2.625\ A^2 - 0.875\ A^2\right)}{\left(5.2\ V^2 - 5\ V^2\right)} = 24.6\ \mu F \quad (36)$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{ORIPPLE}}{I_{RIPPLE}}\right)} = \frac{1}{8 \times 600\ kHz} \times \frac{1}{\left(\frac{25\ mV}{0.932\ A}\right)} = 7.8\ \mu F \quad (37)$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} = \frac{25\ mV}{0.932\ A} = 27\ m\Omega \quad (38)$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} = \frac{5\ V \times (60\ V - 5\ V)}{\sqrt{12} \times 60\ V \times 8.2\ \mu H \times 600\ kHz} = 269\ mA \quad (39)$$

8.2.1.2.5 Catch Diode

The TPS54361 requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the TPS54361.

For the example design, the PDS560 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the PDS560 is 0.55 V at 3.5 A.

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The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the OFF-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the AC losses of the diode must be taken into account. The AC losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 40 is used to calculate the total power dissipation, including conduction losses and AC losses of the diode.

The PDS560 diode has a junction capacitance of 90 pF. Using Equation 40, the total loss in the diode is 1.13 W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times Vfd}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + Vfd\right)^2}{2} =$$

$$\frac{(12\ V\ -\ 5\ V) \times 3.5\ A \times 0.55\ V}{12\ V} + \frac{90\ pF \times 600\ kHz \times (12\ V + 0.55\ V)^2}{2} = 1.13\ W \quad (40)$$

8.2.1.2.6 Input Capacitor

The TPS54361 requires a high quality ceramic type X5R or X7R input decoupling capacitor with at least 3 µF of effective capacitance. Some applications benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance due to dc bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54361. The input ripple current can be calculated using Equation 41.

The value of a ceramic capacitor varies significantly with temperature and the dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is more stable over temperature. X5R and X7R ceramic dielectrics are usually selected for switching regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with consideration for the DC bias. The effective value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 60-V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, or 100 V. For this example, two 2.2-µF, 100-V capacitors in parallel are used. Table 2 shows several choices of high voltage capacitors.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 42. Using the design example values, I_{OUT} = 3.5 A, C_{IN} = 4.4 µF, $f$sw = 600 kHz, yields an input voltage ripple of 331 mV and a RMS input ripple current of 1.72 A.

$$I_{CI(rms)} = I_{OUT}\ x \sqrt{\frac{V_{OUT}}{V_{IN(min)}}\ x\ \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 3.5\ A \sqrt{\frac{5\ V}{8.5\ V} \times \frac{(8.5\ V\ -\ 5\ V)}{8.5\ V}} = 1.72\ A \quad (41)$$

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} = \frac{3.5\ A \times 0.25}{4.4\ \mu F \times 600\ kHz} = 331\ mV \quad (42)$$

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Table 2. Capacitor Types

VENDOR	VALUE (µF)	EIA Size	VOLTAGE (V)	DIALECTRIC	COMMENTS
Murata	1 to 2.2	1210	100	X7R	GRM32 series
	1 to 4.7		50		
	1	1206	100		GRM31 series
	1 to 2.2		50		
Vishay	1 to 1.8	2220	50		VJ X7R series
	1 to 1.2		100		
	1 to 3.9	2225	50		
	1 to 1.8		100		
TDK	1 to 2.2	1812	100		C series C4532
	1.5 to 6.8		50		
	1 to 2.2	1210	100		C series C3225
	1 to 3.3		50		
AVX	1 to 4.7	1210	50		X7R dielectric series
	1		100		
	1 to 4.7	1812	50		
	1 to 2.2		100		

8.2.1.2.7 Soft-Start Capacitor

The soft-start capacitor determines the minimum amount of time required for the output voltage to reach its nominal programmed value during power-up. This feature of the soft-start capacitor is useful if a load requires a controlled voltage slew rate. This feature is also used if the output capacitance is large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor can make the TPS54361 device reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The soft-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 43 can be used to find the minimum soft-start time, T_{SS}, necessary to charge the output capacitor, C_{OUT}, from 10% to 90% of the output voltage, V_{OUT}, with an average soft-start current of I_{SSavg}. In the example, to charge the effective output capacitance of 58 µF up to 5 V with an average current of 1 A requires a 0.2-ms soft-start time.

Once the soft-start time is known, the soft-start capacitor value can be calculated using Equation 5. For the example circuit, the soft-start time is not too critical because the output capacitor value is 2 × 47 µF which does not require much current to charge to 5 V. The example circuit has the soft-start time set to an arbitrary value of 3.5 ms which requires a 9.3-nF soft start capacitor calculated by Equation 44. For this design, the next larger standard value of 10 nF is used.

$$T_{SS} > \frac{C_{OUT} \times V_{OUT} \times 0.8}{I_{SSavg}} \quad (43)$$

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V) \times 0.8} = \frac{3.5\ ms \times 1.7\ \mu A}{(0.8\ V \times 0.8)} = 9.3\ nF \quad (44)$$

8.2.1.2.8 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor must have a 10-V or higher voltage rating.

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8.2.1.2.9 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54361 device. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply must turn on and start switching once the input voltage increases above 6.5 V (UVLO start). After the regulator starts switching, it must continue to do so until the input voltage falls below 5 V (UVLO stop).

Programmable UVLO threshold voltages are set using the resistor-divider of R_{UVLO1} and R_{UVLO2} between VIN and ground connected to the EN pin. Equation 3 and Equation 4 calculate the resistance values necessary. For the example application, a 442 kΩ between V_{IN} and EN (R_{UVLO1}) and a 90.9 kΩ between EN and ground (R_{UVLO2}) are required to produce the 6.5-V and 5-V start and stop voltages.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} = \frac{6.5\ V - 5\ V}{3.4\ \mu A} = 441\ k\Omega \quad (45)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} = \frac{1.2\ V}{\frac{6.5\ V - 1.2\ V}{442\ k\Omega} + 1.2\ \mu A} = 90.9\ k\Omega \quad (46)$$

8.2.1.2.10 Output Voltage and Feedback Resistors Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, 10.2 kΩ was selected for R6. Using Equation 2, R5 is calculated as 53.5 kΩ. The nearest standard 1% resistor is 53.6 kΩ. Due to the input current of the FB pin, the current flowing through the feedback network must be greater than 1 µA to maintain the output voltage accuracy. This requirement is satisfied if the value of R6 is less than 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - 0.8\ V}{0.8\ V} = 10.2\ k\Omega \times \left(\frac{5\ V - 0.8\ V}{0.8\ V}\right) = 53.5\ k\Omega \quad (47)$$

8.2.1.2.11 Compensation

There are several methods to design compensation for DC-DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Because the slope compensation is ignored, the actual crossover frequency is lower than the crossover frequency used in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least ten-times greater the modulator pole.

To get started, the modulator pole, $f_{p(mod)}$, and the ESR zero, f_{z1} must be calculated using Equation 48 and Equation 49. For C_{OUT}, use a derated value of 58.3 µF. Use equations Equation 50 and Equation 51 to estimate a starting point for the crossover frequency, $f$co. For the example design, $f_{p(mod)}$ is 1912 Hz and $f_{z(mod)}$ is 1092 kHz. Equation 49 is the geometric mean of the modulator pole and the ESR zero and Equation 51 is the mean of modulator pole and the switching frequency. Equation 50 yields 45.7 kHz and Equation 51 gives 23.9 kHz. Use the lower value of Equation 50 or Equation 51 for an initial crossover frequency. For this example, the target $f$co is 23.9 kHz.

Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{3.5\ A}{2 \times \pi \times 5\ V \times 58.3\ \mu F} = 1912\ Hz \quad (48)$$

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2 \times \pi \times 2.5\ m\Omega \times 58.3\ \mu F} = 1092\ kHz \quad (49)$$

$$f_{co} = \sqrt{f_{p(mod)} \times f_{z(mod)}} = \sqrt{1912\ Hz \times 1092\ kHz} = 45.7\ kHz \quad (50)$$

$$f_{co} = \sqrt{f_{p(mod)} \times \frac{f_{SW}}{2}} = \sqrt{1912\ Hz \times \frac{600\ kHz}{2}} = 23.9\ kHz \quad (51)$$

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To determine the compensation resistor, R4, use Equation 52. Assume the power stage transconductance, gm_{ps}, is 12 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 5 V, 0.8 V, and 350 μS, respectively. R4 is calculated to be 13 kΩ, which is a standard value. Use Equation 53 to set the compensation zero to the modulator pole frequency. Equation 53 yields 6404 pF for compensating capacitor C5. 6800 pF is used for this design.

$$R4 = \left(\frac{2 \times \pi \times f_{co} \times C_{OUT}}{gm_{ps}}\right) \times \left(\frac{V_{OUT}}{V_{REF} \text{ x } gm_{ea}}\right) = \left(\frac{2 \times \pi \times 23.9 \text{ kHz} \times 58.3 \text{ µF}}{12 \text{ A / V}}\right) \times \left(\frac{5 \text{ V}}{0.8 \text{ V} \times 350 \text{ µA / V}}\right) = 13 \text{ k}\Omega \quad (52)$$

$$C5 = \frac{1}{2 \times \pi \times R4 \text{ x } f_{p(mod)}} = \frac{1}{2 \times \pi \times 13 \text{ k}\Omega \text{ x } 1912 \text{ Hz}} = 6404 \text{ pF} \quad (53)$$

A compensation pole can be implemented if desired by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from Equation 54 and Equation 55 for C8 to set the compensation pole. The selected value of C8 is 39 pF for this design example.

$$C8 = \frac{C_{OUT} \text{ x } R_{ESR}}{R4} = \frac{58.3 \text{ µF x } 2.5 \text{ m}\Omega}{13 \text{ k}\Omega} = 11.2 \text{ pF} \quad (54)$$

$$C8 = \frac{1}{R4 \times f_{sw} \times \pi} = \frac{1}{13 \text{ k}\Omega \times 600 \text{ kHz} \times \pi} = 40.8 \text{ pF} \quad (55)$$

8.2.1.2.12 Power Dissipation Estimate

The following formulas show how to estimate the TPS54361 power dissipation under continuous conduction mode (CCM) operation. These equations must not be used if the device is operating in discontinuous conduction mode (DCM).

The power dissipation of the IC includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}), and supply current (P_Q). Example calculations are shown with the 12-V typical input voltage of the design example.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}}\right) = 3.5 \text{ A}^2 \times 87 \text{ m}\Omega \times \frac{5 \text{ V}}{12 \text{ V}} = 0.444 \text{ W} \quad (56)$$

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times t_{rise} = 12 \text{ V} \times 600 \text{ kHz} \times 3.5 \text{ A} \times 4.9 \text{ ns} = 0.123 \text{ W} \quad (57)$$

$$P_{GD} = V_{IN} \times Q_G \times f_{SW} = 12 \text{ V} \times 3\text{nC} \times 600 \text{ kHz} = 0.022 \text{ W} \quad (58)$$

$$P_Q = V_{IN} \times I_Q = 12 \text{ V} \times 146 \text{ µA} = 0.0018 \text{ W}$$

where

- I_{OUT} is the output current (A)
- $R_{DS(on)}$ is the ON-resistance of the high-side MOSFET (Ω)
- V_{OUT} is the output voltage (V)
- V_{IN} is the input voltage (V)
- f_{SW} is the switching frequency (Hz)
- t_{rise} is the SW pin voltage rise time and can be estimated by trise = V_{IN} × 0.16 ns/V + 3 ns
- Q_G is the total gate charge of the internal MOSFET
- I_Q is the operating nonswitching supply current (59)

Therefore,

$$P_{TOT} = P_{COND} + P_{SW} + P_{GD} + P_Q = 0.444\ W\ +\ 0.123\ W\ +\ 0.022\ W\ +\ 0.0018\ W = 0.591\ W \quad (60)$$

For given T_A,

$$T_J = T_A + R_{TH} \times P_{TOT} \quad (61)$$

For given $T_{J(MAX)}$ = 150°C

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT}$$

where

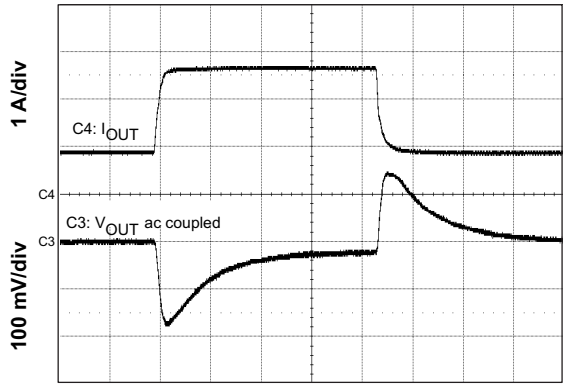
- P_{TOT} is the total device power dissipation (W)
- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- R_{TH} is the thermal resistance from junction to ambient for a given PCB layout (°C/W)
- $T_{J(MAX)}$ is maximum junction temperature (°C)
- $T_{A(MAX)}$ is maximum ambient temperature (°C) (62)

Additional power losses occur in the regulator circuit because of the inductor AC and DC losses, the catch diode, and PCB trace resistance impacting the overall efficiency of the regulator.

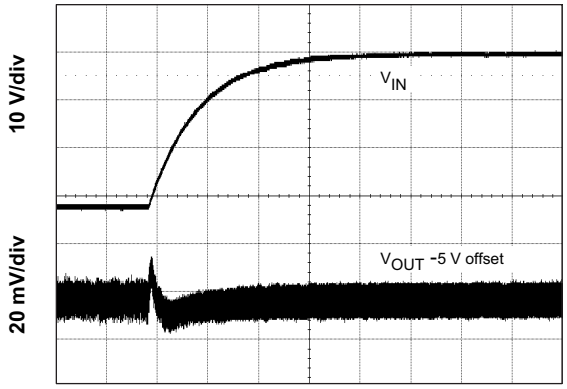
8.2.1.2.13 Discontinuous Conduction Mode and Eco-Mode Boundary

With an input voltage of 12 V, the power supply enters discontinuous conduction mode when the output current is less than 300 mA. The power supply enters Eco-mode when the output current is lower than 24 mA. The input current draw is 260 μA with no load.

8.2.1.3 Application Curves



Time = 100 μs/div
Figure 47. Load Transient



Time = 5 ms/div
Figure 48. Line Transient (8 V to 40 V)

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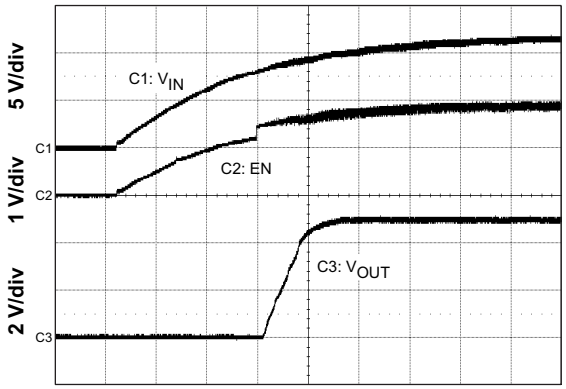
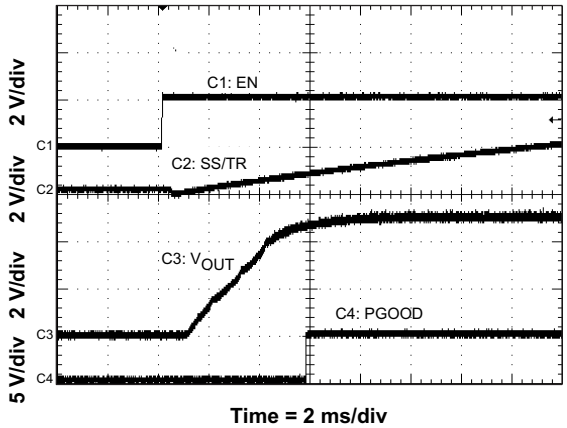
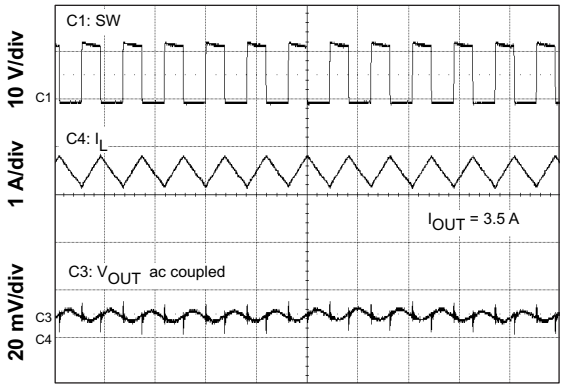


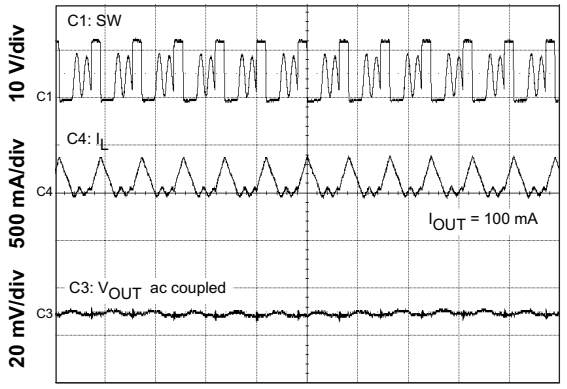
Time = 2 ms/div
Figure 49. Start-Up With VIN



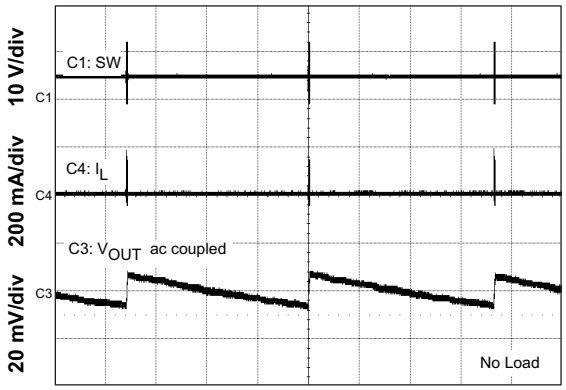
Time = 2 ms/div
Figure 50. Start-Up With EN



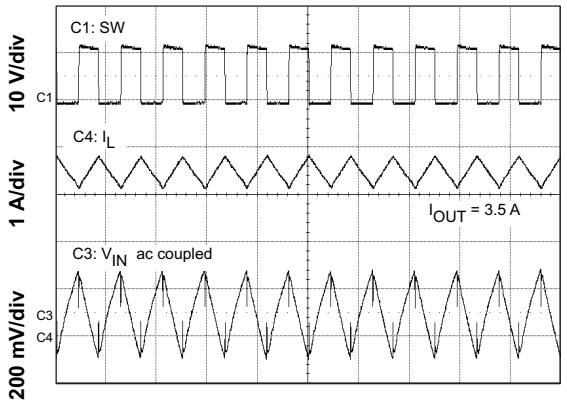
Time = 2 µs/div
Figure 51. Output Ripple CCM



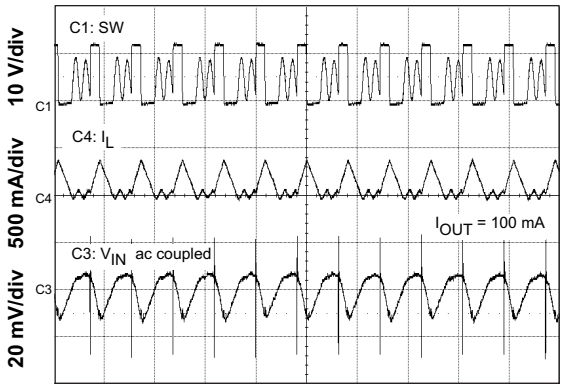
Time = 2 µs/div
Figure 52. Output Ripple DCM



Time = 2 ms/div
Figure 53. Output Ripple PSM

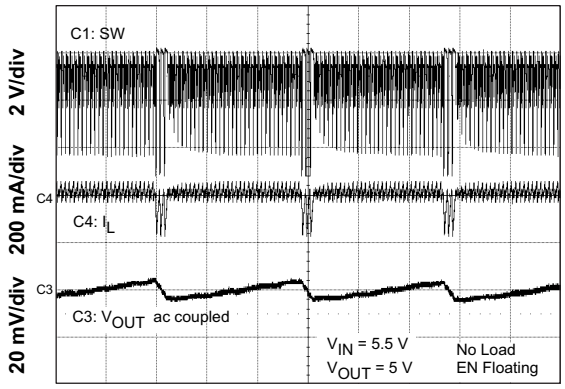


Time = 2 µs/div
Figure 54. Input Ripple CCM



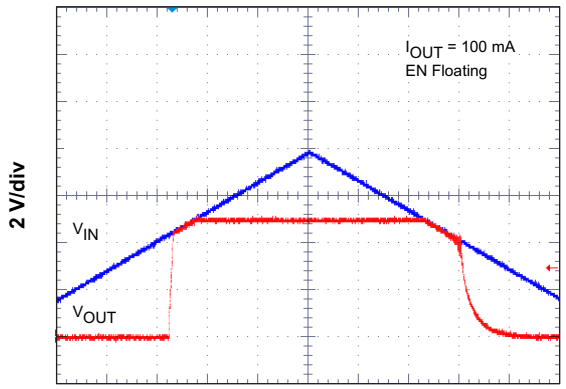
Time = 2 μs/div

Figure 55. Input Ripple DCM



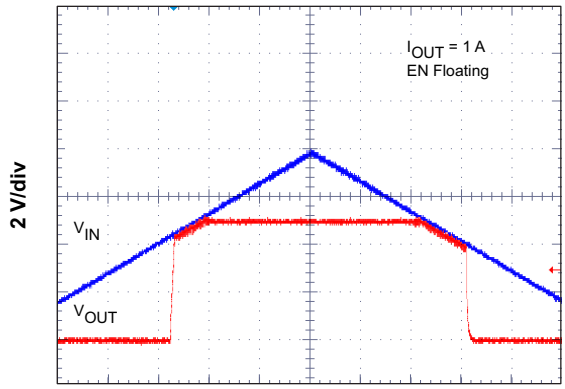
Time = 20 μs/div

Figure 56. Low-Dropout Operation



Time = 40 μs/div

Figure 57. Low-Dropout Operation



Time = 40 μs/div

Figure 58. Low-Dropout Operation

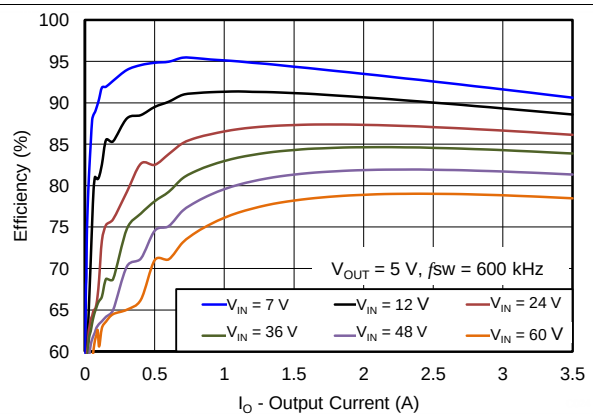


Figure 59. Efficiency Versus Load Current

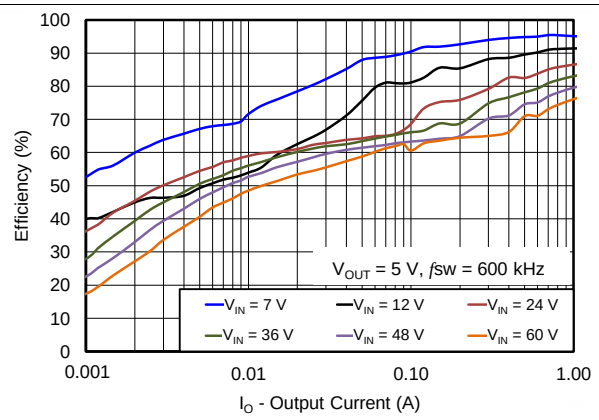


Figure 60. Light-Load Efficiency

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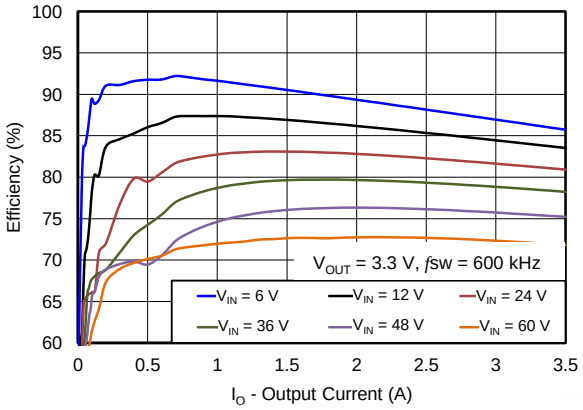

Figure 61. Efficiency Versus Load Current

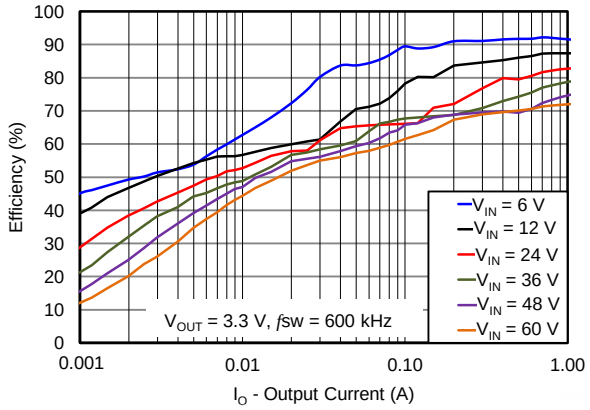

Figure 62. Light-Load Efficiency

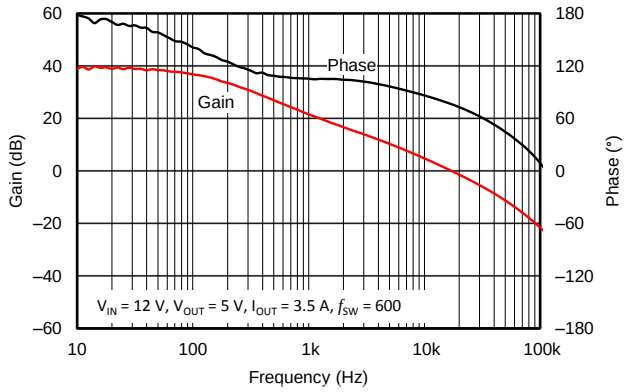

Figure 63. Overall Loop-Frequency Response

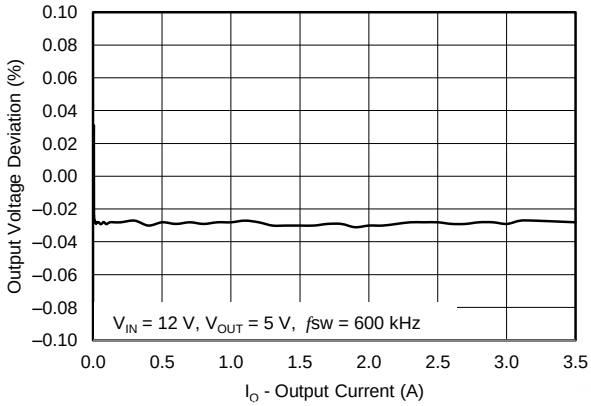

Figure 64. Regulation Versus Load Current

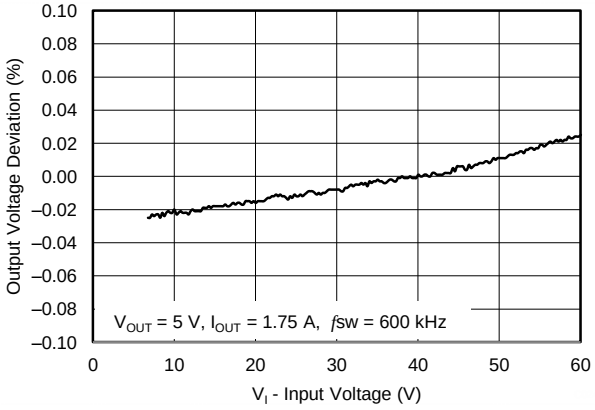

Figure 65. Regulation Versus Input Voltage

8.2.2 Inverting Power Supply

The TPS54361 can be used to convert a positive input voltage to a negative output voltage. Example applications are amplifiers requiring a negative power supply. For a more detailed example, see SLVA317.

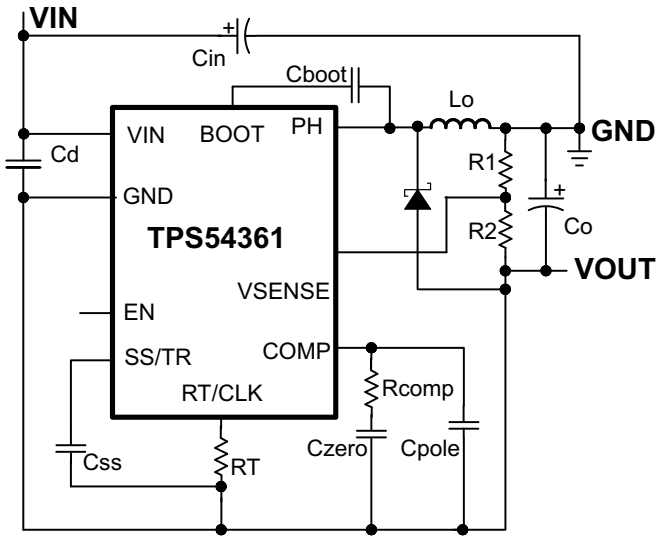

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Figure 66. TPS54361 Inverting Power Supply Based on the Application Note, SLVA317

8.2.3 Split-Rail Power Supply

The TPS54361 can be used to convert a positive input voltage to a split-rail positive and negative output voltage by using a coupled inductor. Example applications are amplifiers requiring a split-rail positive and negative voltage power supply. For a more detailed example, see SLVA369.

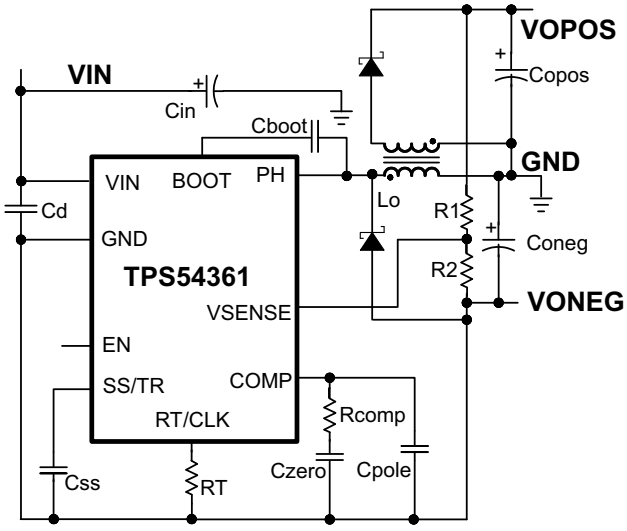

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Figure 67. TPS54361 Split Rail Power Supply Based on the Application Note, SLVA369

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 4.5 V to 60 V. This input supply must remain within this range. If the input supply is located more than a few inches from the TPS54361 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

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10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. See Figure 68 for a PCB layout example.

- To reduce parasitic effects, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Care must be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. The SW pin should be routed to the cathode of the catch diode and to the output inductor. Since the SW connection is the switching node, the catch diode and output inductor should be located close to the SW pin, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The GND pin should be tied directly to the thermal pad under the IC. The thermal pad should be connected to internal PCB ground planes using multiple vias directly under the IC.
- For operation at full rated load, the top side ground area must provide adequate heat dissipating area.
- The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
- The additional external components can be placed approximately as shown.
- It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

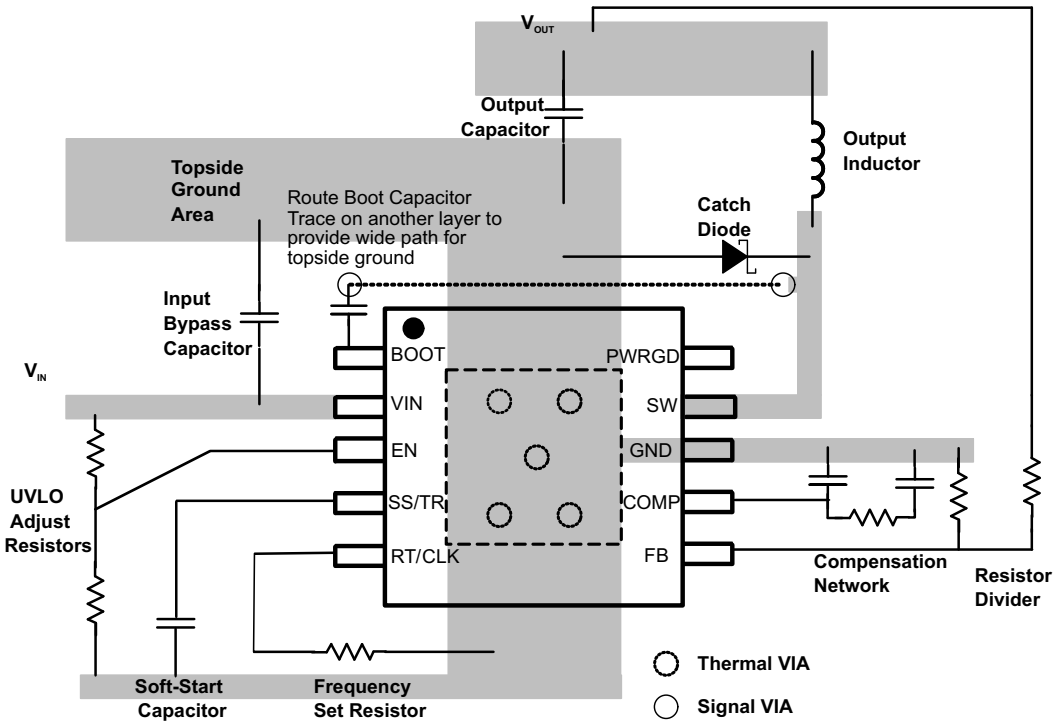

Figure 68. PCB Layout Example

10.3 Estimated Circuit Area

Boxing in the components in the design of Figure 46, the estimated printed circuit board surface area is 1.025 in^2 (661 mm^2). This area does not include test points or connectors. If the area needs to be reduced, this can be done by using a two sided assembly and replacing the 0603 sized passives with a smaller sized equivalent.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For the TPS54360, TPS54361, and TPS54361-Q1 family Excel design tool, see SLVC452.

For the WEBENCH Design Center, go to www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Create an Inverting Power Supply From a Step-Down Regulator,* SLVA317
- *Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator,* SLVA369
- *Evaluation Module for the TPS54361 Step-Down Converter,* SLVU992
- *Creating a Universal Car Charger for USB Devices From the TPS54240 and TPS2511,* SLVA464
- *Creating GSM /GPRS Power Supply from TPS54260,* SLVA412

11.2.2 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS54361-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance
   - Run thermal simulations to understand the thermal performance of your board
   - Export your customized schematic and layout into popular CAD formats
   - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the Alert me button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and

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Community Resources (continued)

contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54361DPRR	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRR.A	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRR.B	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRRG4	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRRG4.A	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRRG4.B	Active	Production	WSON (DPR) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRT	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRT.A	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361
TPS54361DPRT.B	Active	Production	WSON (DPR) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS 54361

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54361 :

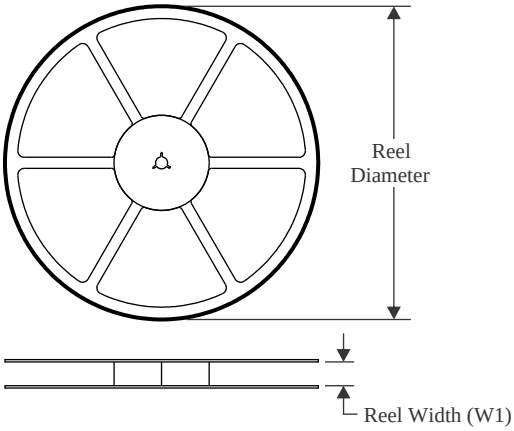
- Automotive : TPS54361-Q1

NOTE: Qualified Version Definitions:

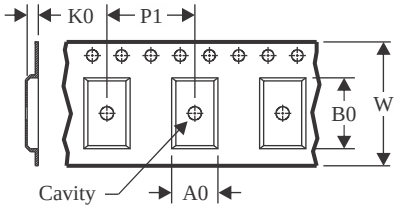
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

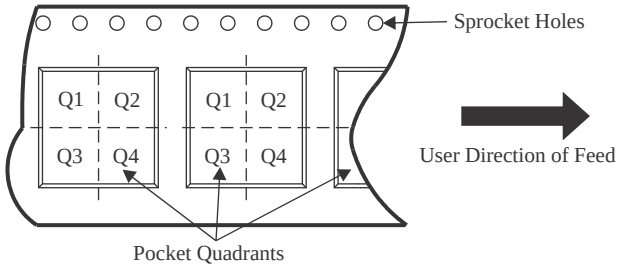


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

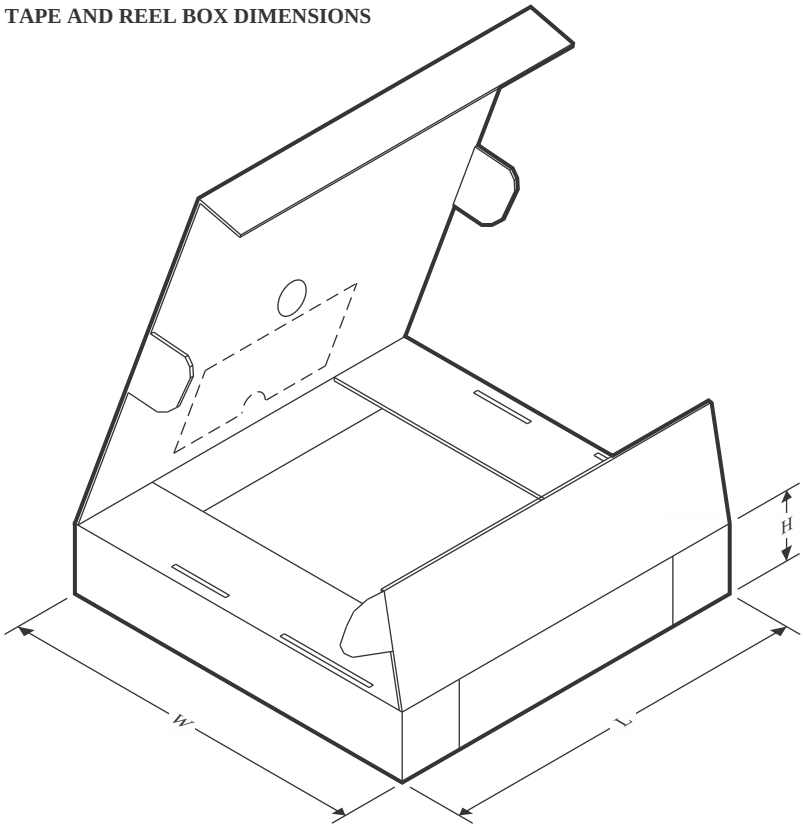
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54361DPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54361DPRRG4	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54361DPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

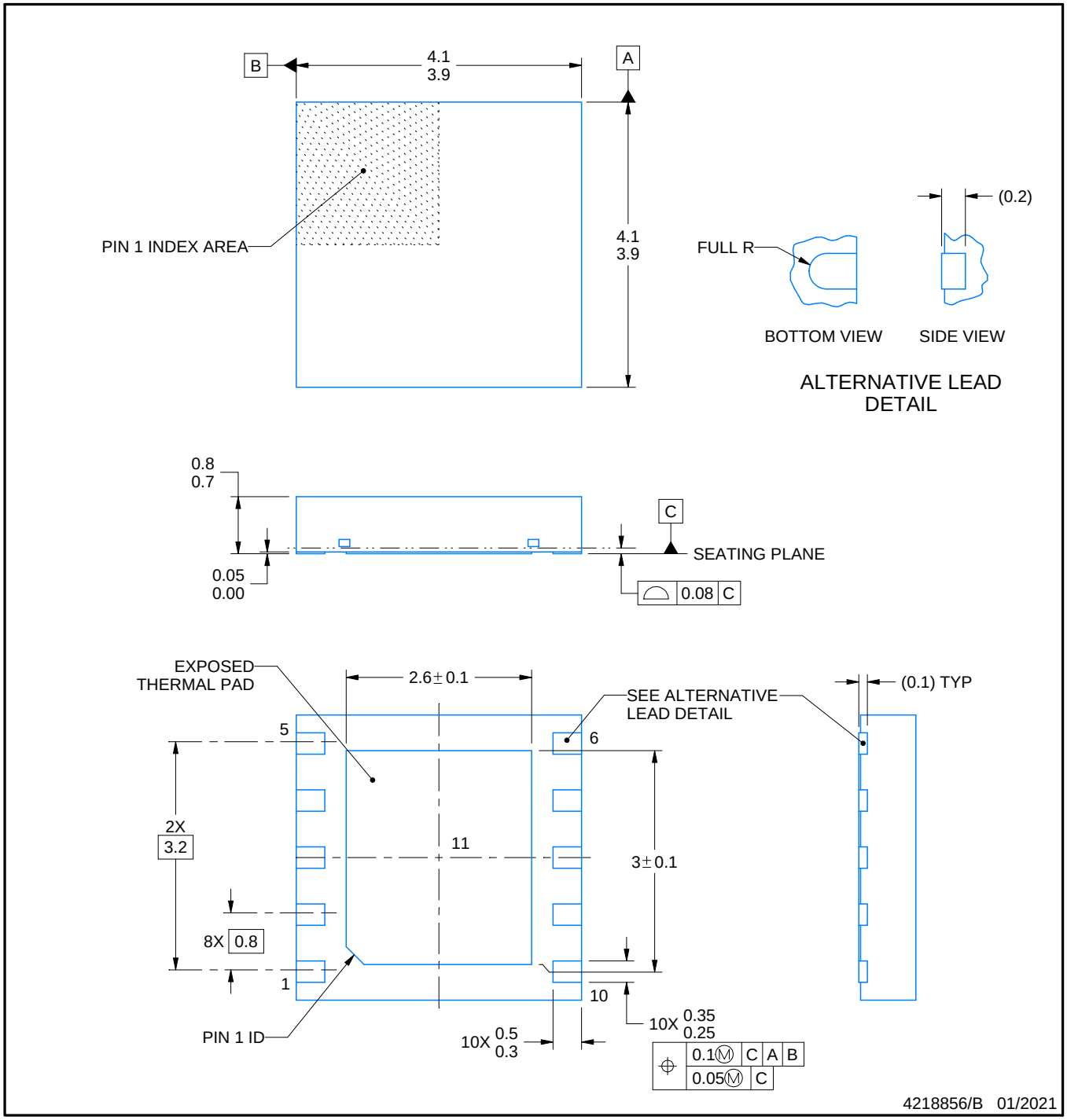
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54361DPRR	WSON	DPR	10	3000	346.0	346.0	33.0
TPS54361DPRRG4	WSON	DPR	10	3000	346.0	346.0	33.0
TPS54361DPRT	WSON	DPR	10	250	182.0	182.0	20.0

PACKAGE OUTLINE

DPR0010A

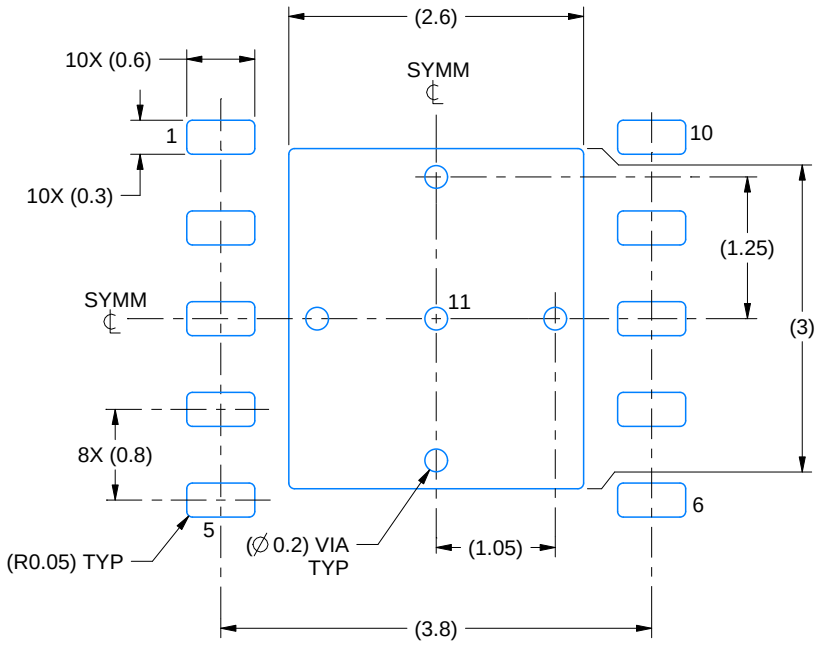
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

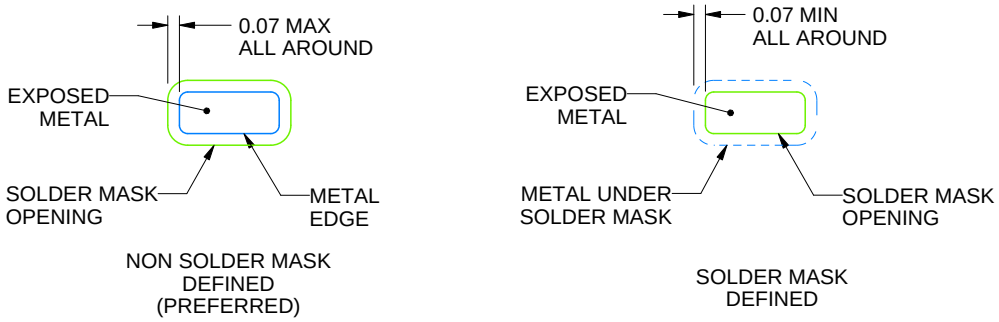


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

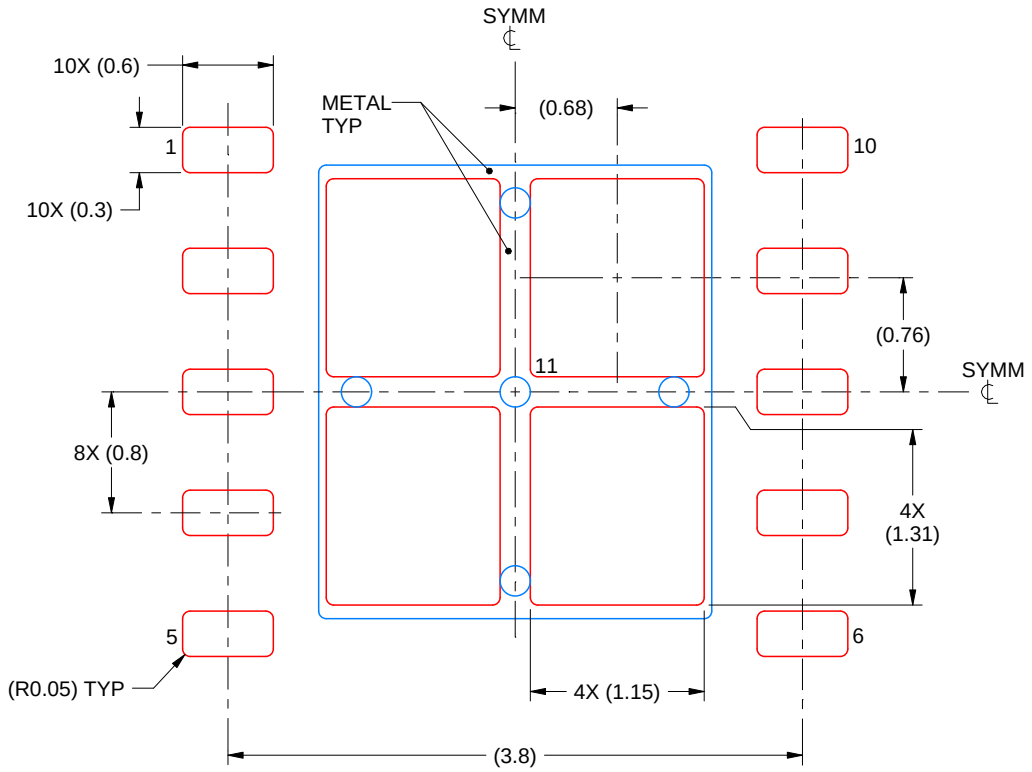


SOLDER MASK DETAILS

4218856/B 01/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218856/B 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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