

# LM2653 1.5A High Efficiency Synchronous Switching Regulator

**Check for Samples:** [LM2653](#)

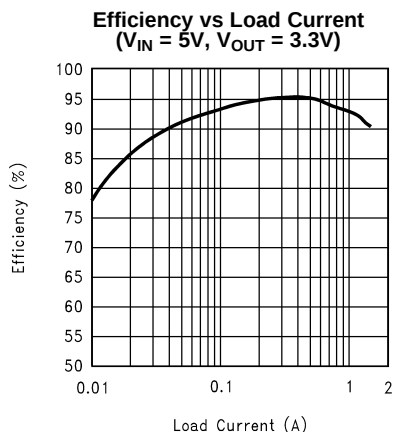
## FEATURES

- **Efficiency up to 97%**
- **4V to 14V Input Voltage Range**
- **1.5V to 5.0V Adjustable Output Voltage**
- **0.1Ω Switch On Resistance**
- **300 kHz Fixed Frequency Internal Oscillator**
- **7 μA Shutdown Current**
- **Patented Current Sensing for Current Mode Control**
- **Input Undervoltage Lockout**
- **Output Overvoltage Shutdown Protection**
- **Output Undervoltage Shutdown Protection**
- **Adjustable Soft-Start**
- **Adjustable PGOOD Delay**
- **Current Limit and Thermal Shutdown**

## APPLICATIONS

- **Webpad**
- **Personal Digital Assistants (PDAs)**
- **Computer Peripherals**
- **Battery-Powered Devices**
- **Notebook Computer Video Supply**
- **Handheld Scanners**
- **GXM I/O and Core Voltage**
- **High Efficiency 5V Conversion**

## Typical Application



**Figure 1.**

## DESCRIPTION

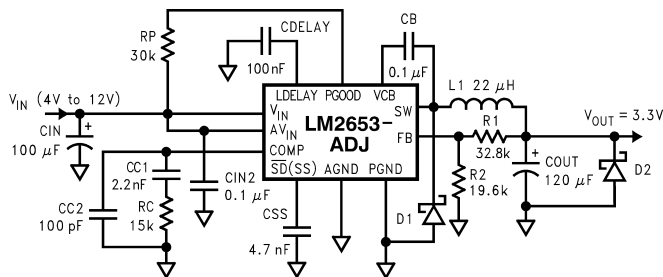
The LM2653 switching regulator provides high efficient power conversion over a 100:1 load range (1.5A to 15 mA). This feature makes the LM2653 an ideal fit in battery-powered applications.

Synchronous rectification is used to achieve up to 97% efficiency. At light loads, the LM2653 enters a low power hysteretic or “sleep” mode to keep the efficiency high. In many applications, the efficiency still exceeds 80% at 15 mA load. A shutdown pin is available to disable the LM2653 and reduce the supply current to 7µA.

All the power, control, and drive functions are integrated within the ICs. The ICs contain patented current sensing circuitry for current mode control. This feature eliminates the external current sensing resistor required by other current-mode DC-DC converters.

The ICs have a 300 kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low profile components.

Protection features include thermal shutdown, input undervoltage lockout, adjustable soft-start, cycle by cycle current limit, output overvoltage and undervoltage protections.



**Figure 2.**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

|                                                         |            |                                 |                                            |
|---------------------------------------------------------|------------|---------------------------------|--------------------------------------------|
| Input Voltage                                           |            |                                 | 15V                                        |
| PGOOD Pin Voltage                                       |            |                                 | 15V                                        |
| Feedback Pin Voltage                                    |            |                                 | $-0.4V \leq V_{FB} \leq 5V$                |
| Power Dissipation (T <sub>A</sub> =25°C) <sup>(4)</sup> |            |                                 | 893 mW                                     |
| Junction Temperature Range                              |            |                                 | $-40^{\circ}C \leq T_J \leq +125^{\circ}C$ |
| Storage Temperature Range                               |            |                                 | $-65^{\circ}C$ to $+150^{\circ}C$          |
| Lead Temperature                                        | PW Package | Vapor Phase (60 sec.)           | 215°C                                      |
|                                                         |            | Infrared (15 sec.)              | 220°C                                      |
| Maximum Junction Temperature                            |            |                                 | 150°C                                      |
| ESD Susceptibility                                      |            | Human Body Model <sup>(3)</sup> | 1 kV                                       |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be specified under these conditions. For specified specifications and test conditions, see [Electrical Characteristics](#).
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
- (4) The maximum allowable power dissipation is calculated by using  $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$ , where  $T_{JMAX}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction-to-ambient thermal resistance of the specified package. The 893 mW rating results from using  $150^\circ\text{C}$ ,  $25^\circ\text{C}$ , and  $140^\circ\text{C/W}$  for  $T_{JMAX}$ ,  $T_A$ , and  $\theta_{JA}$  respectively. A  $\theta_{JA}$  of  $140^\circ\text{C/W}$  represents the worst-case condition of no heat sinking of the 16-pin TSSOP package. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation must be derated by 7.14 mW per  $^\circ\text{C}$  above  $25^\circ\text{C}$  ambient. The LM2653 actively limits its junction temperatures to about  $165^\circ\text{C}$ .

### Operating Ratings<sup>(1)</sup>

|                |                           |
|----------------|---------------------------|
| Supply Voltage | $4V \leq V_{IN} \leq 14V$ |
|----------------|---------------------------|

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be specified under these conditions. For specified specifications and test conditions, see [Electrical Characteristics](#).

### Electrical Characteristics

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$ , and those in **boldface type** apply over full **Operating Temperature Range**.  $V_{IN} = 10V$  unless otherwise specified.

| Symbol         | Parameter                                       | Conditions                                            | Typical <sup>(1)</sup> | Limit <sup>(2)</sup>         | Units                 |
|----------------|-------------------------------------------------|-------------------------------------------------------|------------------------|------------------------------|-----------------------|
| $V_{FB}$       | Feedback Voltage                                | $I_{LOAD} = 900\text{ mA}$                            | 1.238                  | <b>1.200</b><br><b>1.263</b> | V<br>V(min)<br>V(max) |
| $V_{OUT}$      | Output Voltage Line Regulation                  | $V_{IN} = 4V$ to $12V$<br>$I_{LOAD} = 900\text{ mA}$  | 0.2                    |                              | %                     |
|                | Output Voltage Load Regulation                  | $I_{LOAD} = 10\text{ mA}$ to $1.5A$<br>$V_{IN} = 5V$  | 1.3                    |                              | %                     |
|                | Output Voltage Load Regulation                  | $I_{LOAD} = 200\text{ mA}$ to $1.5A$<br>$V_{IN} = 5V$ | 0.3                    |                              | %                     |
| $V_{INUV}$     | $V_{IN}$ Undervoltage Lockout Threshold Voltage | Rising Edge                                           | 3.8                    | <b>3.95</b>                  | V<br>V(max)           |
| $V_{UV\_HYST}$ | Hysteresis for the Input Undervoltage Lockout   |                                                       | 210                    |                              | mV                    |
| $I_{CL}$       | Switch Current Limit                            | $V_{IN} = 5V$<br>$V_{OUT} = 2.5V$                     | 2.0                    | <b>1.55</b><br><b>2.60</b>   | A<br>A(min)<br>A(max) |
| $I_{SM}$       | Sleep Mode Threshold Current                    | $V_{IN} = 5V$ , $V_{OUT} = 2.5V$                      | 100                    |                              | mA                    |

- (1) All limits specified at room temperature (standard typeface) and at **temperature extremes (bold typeface)**. All room temperature limits are 100% production tested. All limits at **temperature extremes** are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) Typical numbers are at  $25^\circ\text{C}$  and represent the most likely norm.

## Electrical Characteristics (continued)

Specifications with standard typeface are for  $T_j = 25^\circ\text{C}$ , and those in **boldface type** apply over full **Operating Temperature Range**.  $V_{IN} = 10\text{V}$  unless otherwise specified.

| Symbol              | Parameter                                                                                   | Conditions                                                                | Typical <sup>(1)</sup> | Limit <sup>(2)</sup>     | Units                                                                   |
|---------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|------------------------|--------------------------|-------------------------------------------------------------------------|
| $V_{HYST}$          | Sleep Mode Feedback Voltage Hysteresis                                                      |                                                                           | 24                     |                          | mV                                                                      |
| $I_Q$               | Quiescent Current                                                                           |                                                                           | 1.7                    | <b>2.0</b>               | mA<br>mA(max)                                                           |
| $I_{QSD}$           | Quiescent Current in Shutdown Mode                                                          | Shutdown Pin Pulled Low                                                   | 7                      | <b>12/20</b>             | $\mu\text{A}$<br>$\mu\text{A}(\text{max})$                              |
| $R_{DS(ON)}$        | High-Side or Low-Side MOSFET ON Resistance                                                  | $I_{SWITCH} = 1\text{A}$                                                  | 75                     | <b>130</b>               | $\text{m}\Omega$<br>$\text{m}\Omega(\text{max})$                        |
| $R_{SW(ON)}$        | High-Side or Low-Side Switch On Resistance (MOSFET ON Resistance + Bonding Wire Resistance) | $I_{SWITCH} = 1\text{A}$                                                  | 110                    |                          | $\text{m}\Omega$                                                        |
| $I_L$               | Switch Leakage Current—High Side                                                            |                                                                           | 130                    |                          | nA                                                                      |
|                     | Switch Leakage Current—Low Side                                                             |                                                                           | 130                    |                          | nA                                                                      |
| $V_{BOOT}$          | Bootstrap Regulator Voltage                                                                 | $I_{BOOT} = 1\text{mA}$                                                   | 6.75                   | 6.45/6.40<br>6.95/7.00   | V<br>V(min)<br>V(max)                                                   |
| $G_M$               | Error Amplifier Transconductance                                                            |                                                                           | 1250                   |                          | $\mu\text{mho}$                                                         |
| $A_V$               | Error Amplifier Voltage Gain                                                                |                                                                           | 100                    |                          |                                                                         |
| $I_{EA\_SOURCE}$    | Error Amplifier Source Current                                                              | $V_{IN} = 3.6\text{V}$ , $V_{FB} = 1.17\text{V}$ , $V_{COMP} = 2\text{V}$ | 40                     | <b>25/15</b>             | $\mu\text{A}$<br>$\mu\text{A}(\text{min})$                              |
| $I_{EA\_SINK}$      | Error Amplifier Sink Current                                                                | $V_{IN} = 3.6\text{V}$ , $V_{FB} = 1.31\text{V}$ , $V_{COMP} = 2\text{V}$ | 65                     | <b>30</b>                | $\mu\text{A}$<br>$\mu\text{A}(\text{min})$                              |
| $V_{EAH}$           | Error Amplifier Output Swing Upper Limit                                                    | $V_{IN} = 4\text{V}$ , $V_{FB} = 1.17\text{V}$                            | 2.70                   | <b>2.50/2.40</b>         | V<br>V(min)                                                             |
| $V_{EAL}$           | Error Amplifier Output Swing Lower Limit                                                    | $V_{IN} = 4\text{V}$ , $V_{FB} = 1.31\text{V}$                            | 1.25                   | <b>1.35/1.50</b>         | V<br>V(max)                                                             |
| $V_D$               | Body Diode Voltage                                                                          | $I_{DIODE} = 1.5\text{A}$                                                 | 1                      |                          | V                                                                       |
| $F_{OSC}$           | Oscillator Frequency                                                                        | Measured at Switch Pin<br>$V_{IN} = 4\text{V}$                            | 300                    | 280/255<br>330/345       | kHz<br>kHz(min)<br>kHz(max)                                             |
| $D_{MAX}$           | Maximum Duty Cycle                                                                          | $V_{IN} = 4\text{V}$                                                      | 95                     | <b>92</b>                | %<br>%(min)                                                             |
| $I_{SS}$            | Soft-Start Current                                                                          | Voltage at the SS Pin = 1.4V                                              | 11                     | <b>7</b><br><b>14</b>    | $\mu\text{A}$<br>$\mu\text{A}(\text{min})$<br>$\mu\text{A}(\text{max})$ |
| $V_{OUTUV}$         | $V_{OUT}$ Undervoltage Lockout Threshold Voltage                                            |                                                                           | 81                     | <b>76</b><br><b>84</b>   | % $V_{OUT}$<br>% $V_{OUT}(\text{min})$<br>% $V_{OUT}(\text{max})$       |
|                     | Hysteresis for $V_{OUTUV}$                                                                  |                                                                           | 5                      |                          | % $V_{OUT}$                                                             |
| $V_{OUTOV}$         | $V_{OUT}$ Overvoltage Lockout Threshold Voltage                                             |                                                                           | 108                    | <b>106</b><br><b>114</b> | % $V_{OUT}$<br>% $V_{OUT}(\text{min})$<br>% $V_{OUT}(\text{max})$       |
|                     | Hysteresis for $V_{OUTOV}$                                                                  |                                                                           | 3                      |                          | % $V_{OUT}$                                                             |
| $I_{LDELAY-SOURCE}$ | LDELAY Pin Source Current                                                                   |                                                                           | 5                      |                          | $\mu\text{A}$                                                           |
| $I_{PGOOD-SINK}$    | PGOOD Pin Sink Current                                                                      | $V_{PGOOD} = 0.4\text{V}$                                                 |                        | <b>15</b>                | mA(max)                                                                 |
| $I_{PGOOD-LEAKAGE}$ | PGOOD Pin Leakage Current                                                                   | $V_{PGOOD} = 5\text{V}$                                                   | 50                     |                          | nA                                                                      |
| $I_{SHUTDOWN}$      | Shutdown Pin Current                                                                        | Shutdown Pin Pulled Low                                                   | 2.2                    | 0.8/0.5<br>3.7/4.0       | $\mu\text{A}$<br>$\mu\text{A}(\text{min})$<br>$\mu\text{A}(\text{max})$ |

## Electrical Characteristics (continued)

Specifications with standard typeface are for  $T_j = 25^\circ\text{C}$ , and those in **boldface type** apply over full **Operating Temperature Range**.  $V_{IN} = 10\text{V}$  unless otherwise specified.

| Symbol                | Parameter                               | Conditions  | Typical <sup>(1)</sup> | Limit <sup>(2)</sup>     | Units                 |
|-----------------------|-----------------------------------------|-------------|------------------------|--------------------------|-----------------------|
| $V_{\text{SHUTDOWN}}$ | Shutdown Pin Threshold Voltage          | Rising Edge | 0.6                    | <b>0.3</b><br><b>0.9</b> | V<br>V(min)<br>V(max) |
| $T_{\text{SD}}$       | Thermal Shutdown Temperature            |             | 165                    |                          | $^\circ\text{C}$      |
| $T_{\text{SD\_HYST}}$ | Thermal Shutdown Hysteresis Temperature |             | 25                     |                          | $^\circ\text{C}$      |

## Typical Performance Characteristics

Efficiency vs Load Current ( $V_{IN} = 5V$ ,  $V_{OUT} = 2.5V$ )

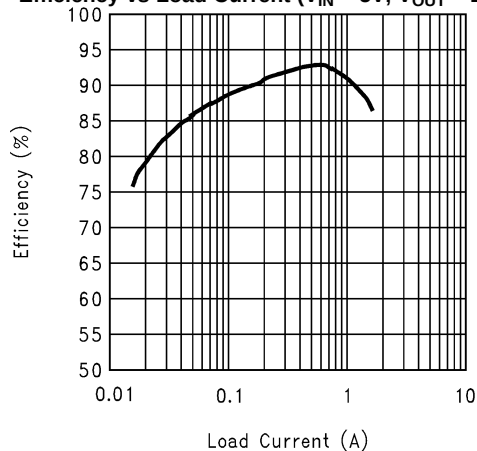


Figure 3.

$I_Q$  vs  $V_{IN}$

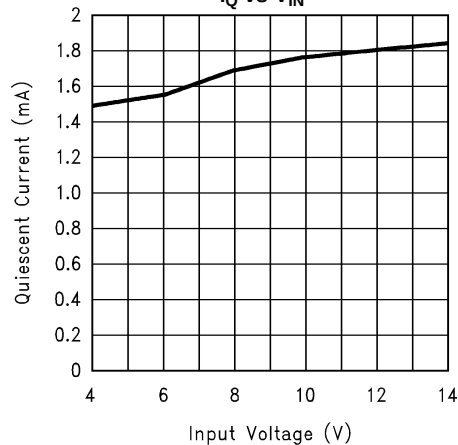


Figure 4.

$I_{QSD}$  vs Input Voltage

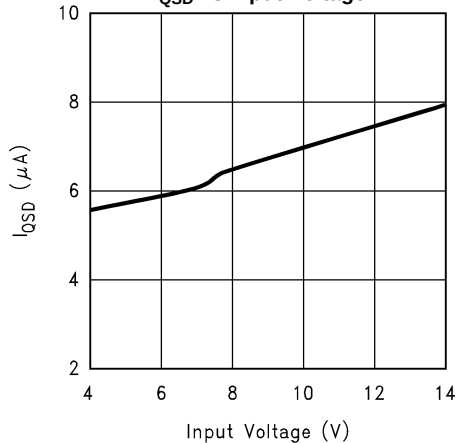


Figure 5.

$I_{QSD}$  vs Junction Temperature

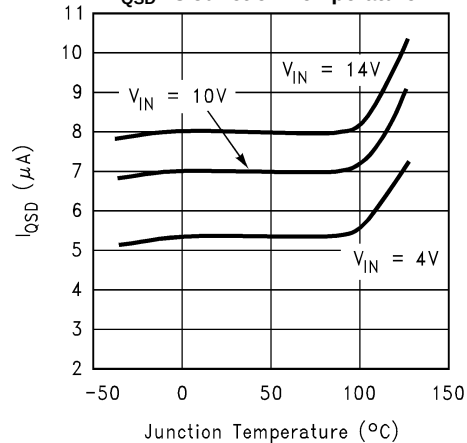


Figure 6.

Frequency vs Junction Temperature

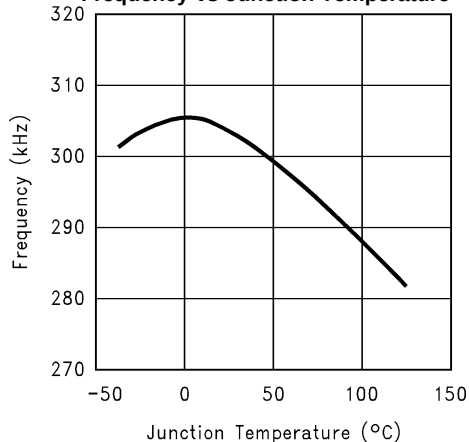


Figure 7.

$R_{SW(ON)}$  vs Input Voltage

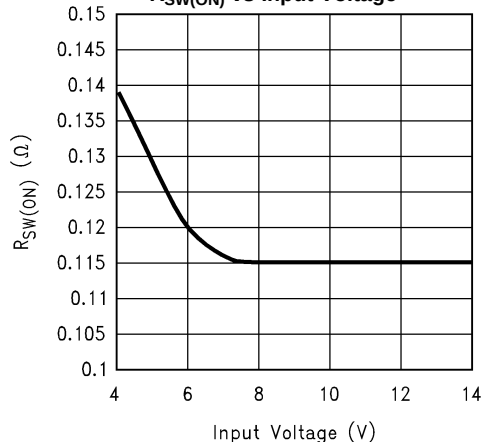


Figure 8.

### Typical Performance Characteristics (continued)

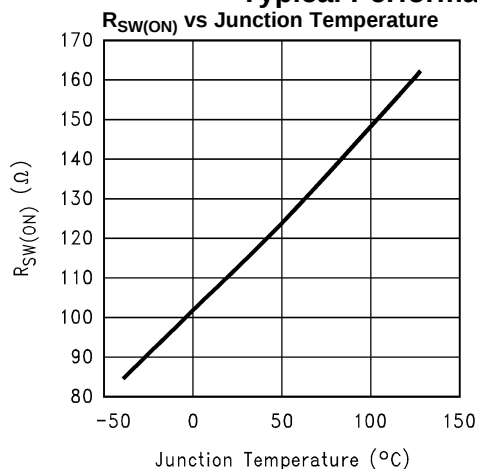


Figure 9.

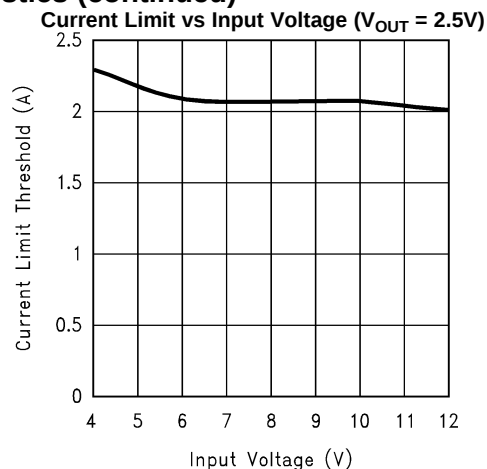


Figure 10.

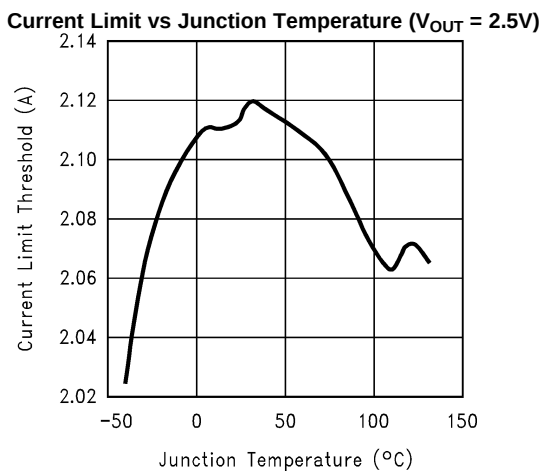


Figure 11.

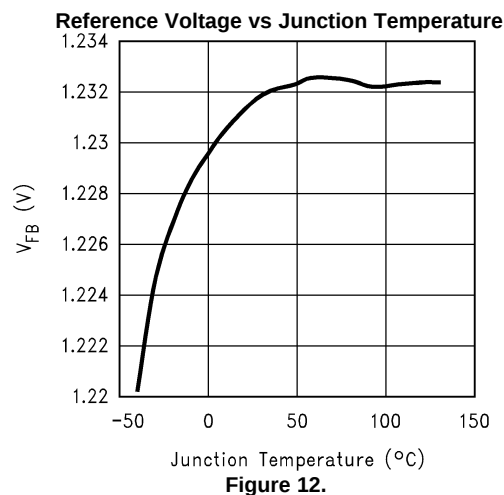


Figure 12.

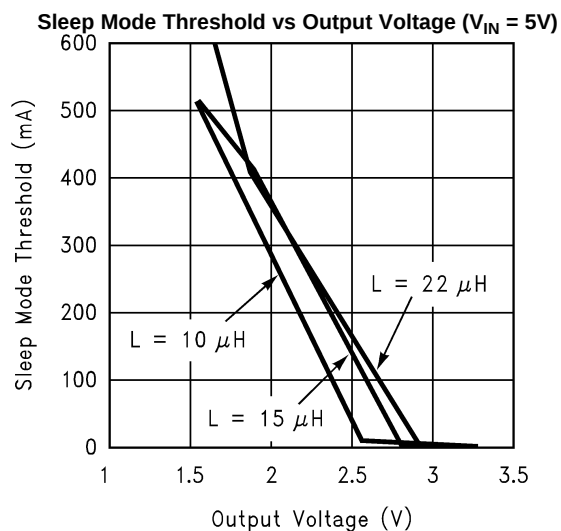
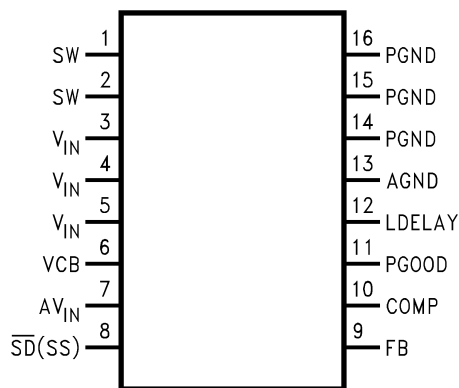


Figure 13.

## CONNECTION DIAGRAM



**Figure 14. 16-Lead TSSOP (PW)**  
**See Package Number PW0016A**

## PIN DESCRIPTIONS

| Pin   | Name                              | Function                                                                                                                                                                                                                                                               |
|-------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1-2   | SW                                | Switched-node connection, which is connected with the source of the internal high-side MOSFET.                                                                                                                                                                         |
| 3-5   | V <sub>IN</sub>                   | Main power supply input pin. Connected to the drain of the high-side MOSFET.                                                                                                                                                                                           |
| 6     | V <sub>CB</sub>                   | Bootstrap capacitor connection for high-side gate drive.                                                                                                                                                                                                               |
| 7     | A V <sub>IN</sub>                 | Input voltage for control and driver circuits.                                                                                                                                                                                                                         |
| 8     | $\overline{\text{SD}}(\text{SS})$ | Shutdown and Soft-start control pin. Pulling this pin below 0.3V shuts off the regulator. A capacitor connected from this pin to ground provides a control ramp of the input current. Do not drive this pin with an external source or erroneous operation may result. |
| 9     | FB                                | Output voltage feedback input. Connected to the output voltage.                                                                                                                                                                                                        |
| 10    | COMP                              | Compensation network connection. Connected to the output of the voltage error amplifier.                                                                                                                                                                               |
| 11    | PGOOD                             | A constant monitor on the output voltage. PGOOD will go low if the output voltage exceeds 110% or goes below 80% of its nominal.                                                                                                                                       |
| 12    | LDELAY                            | A capacitor between this pin to ground sets the delay from the output voltage reaches 80% of its nominal to when the undervoltage latch protection is enabled and PGOOD pin goes low.                                                                                  |
| 13    | AGND                              | Low-noise analog ground.                                                                                                                                                                                                                                               |
| 14-16 | PGND                              | Power ground.                                                                                                                                                                                                                                                          |

## Block Diagram

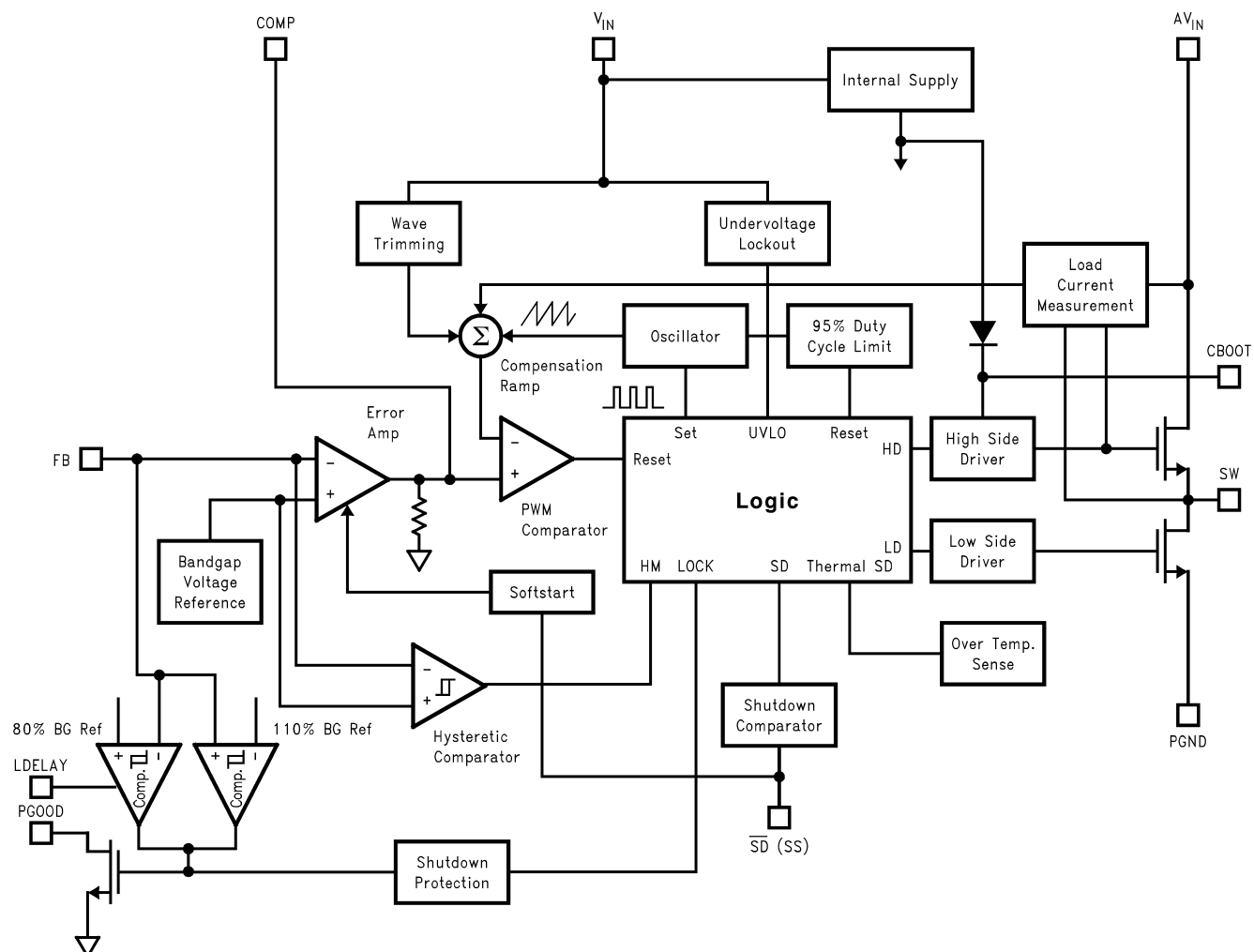


Figure 15.

## OPERATION

The LM2653 operates in a constant frequency (300 kHz), current-mode PWM for moderate to heavy loads; and it automatically switches to hysteretic mode for light loads. In hysteretic mode, the switching frequency is reduced to keep the efficiency high.

### MAIN OPERATION

When the load current is higher than the sleep mode threshold, the part is always operating in PWM mode. At the beginning of each switching cycle, the high-side switch is turned on, the current from the high-side switch is sensed and compared with the output of the error amplifier (COMP pin). When the sensed current reaches the COMP pin voltage level, the high-side switch is turned off; after 40 ns (deadtime), the low-side switch is turned on. At the end of the switching cycle, the low-side switch is turned off; and the same cycle repeats.

The current of the top switch is sensed by a patented internal circuitry. This unique technique gets rid of the external sense resistor, saves cost and size, and improves noise immunity of the sensed current. A feedforward from the input voltage is added to reduce the variation of the current limit over the input voltage range.

When the load current decreases below the sleep mode threshold, the output voltage will rise slightly, this rise is sensed by the hysteretic mode comparator which makes the part go into the hysteretic mode with both the high and low side switches off. The output voltage starts to drop until it hits the low threshold of the hysteretic comparator, and the part immediately goes back to the PWM operation. The output voltage keeps increasing until it reaches the top hysteretic threshold, then both the high and low side switches turn off again, and the same cycle repeats.

### PROTECTIONS

The cycle-by-cycle current limit circuitry turns off the high-side MOSFET whenever the current in MOSFET reaches 2A. A second level current limit is accomplished by the undervoltage protection: if the load pulls the output voltage down below 80% of its nominal value, the undervoltage latch protection will wait for a period of time (set by the capacitor at the LDELAY pin, see [LDELAY CAPACITOR](#) for more information). If the output voltage is still below 80% of its nominal after the waiting period, the latch protection will be enabled. In the latch protection mode, the low-side MOSFET is on and the high-side MOSFET is off. The latch protection will also be enabled immediately whenever the output voltage exceeds the overvoltage threshold (110% of its nominal). Both protections are disabled during start-up. (See [SOFT-START CAPACITOR](#) and [LDELAY CAPACITOR](#) for more information.) Toggling the input supply voltage or the shutdown pin can reset the device from the latched protection mode.

### PGOOD FLAG

The PGOOD flag goes low whenever the overvoltage or undervoltage latch protection is enabled.

### Design Procedure

This section presents guidelines for selecting external components.

#### INPUT CAPACITOR

A low ESR aluminum, tantalum, or ceramic capacitor is needed between the input pin and power ground. This capacitor prevents large voltage transients from appearing at the input. The capacitor is selected based on the RMS current and voltage requirements. The RMS current is given by:

$$I_{\text{RMS}} = I_{\text{OUT}} \times \frac{\sqrt{V_{\text{OUT}}(V_{\text{IN}} - V_{\text{OUT}})}}{V_{\text{IN}}} \quad (1)$$

The RMS current reaches its maximum ( $I_{\text{OUT}}/2$ ) when  $V_{\text{IN}}$  equals  $2V_{\text{OUT}}$ . For an aluminum or ceramic capacitor, the voltage rating should be at least 25% higher than the maximum input voltage. If a tantalum capacitor is used, the voltage rating required is about twice the maximum input voltage. The tantalum capacitor should be surge current tested by the manufacturer to prevent shorted by the inrush current. It is also recommended to put a small ceramic capacitor (0.1  $\mu\text{F}$ ) between the input pin and ground pin to reduce high frequency spikes.

## INDUCTOR

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages:

$$L = \frac{(V_{IN} - V_{OUT}) V_{OUT}}{V_{IN} \times I_{RIPPLE} \times 300 \text{ kHz}} \quad (2)$$

A higher value of ripple current reduces inductance, but increases the conduction loss, core loss, current stress for the inductor and switch devices. It also requires a bigger output capacitor for the same output voltage ripple requirement. A reasonable value is setting the ripple current to be 30% of the DC output current. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. The DC resistance of the inductor is a key parameter for the efficiency. Lower DC resistance is available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal 2% of the output power.

## OUTPUT CAPACITOR

The selection of  $C_{OUT}$  is driven by the maximum allowable output voltage ripple. The output ripple in the constant frequency, PWM mode is approximated by:

$$V_{RIPPLE} = I_{RIPPLE} \left( ESR + \frac{1}{8 f_s C_{OUT}} \right) \quad (3)$$

The ESR term usually plays the dominant role in determining the voltage ripple. A low ESR aluminum electrolytic or tantalum capacitor (such as Nichicon PL series, Sanyo OS-CON, Sprague 593D, 594D, AVX TPS, and CDE polymer aluminum) is recommended. An electrolytic capacitor is not recommended for temperatures below  $-25^{\circ}\text{C}$  since its ESR rises dramatically at cold temperature. A tantalum capacitor has a much better ESR specification at cold temperature and is preferred for low temperature applications.

The output voltage ripple in constant frequency mode has to be less than the sleep mode voltage hysteresis to avoid entering the sleep mode at full load:

$$V_{RIPPLE} < 20\text{mV} \times V_{OUT} / V_{FB} \quad (4)$$

## BOOST CAPACITOR

A 0.1  $\mu\text{F}$  ceramic capacitor is recommended for the boost capacitor. The typical voltage across the boost capacitor is 6.7V.

## SOFT-START CAPACITOR

A soft-start capacitor is used to provide the soft-start feature. When the input voltage is first applied, or when the  $\overline{\text{SD}}(\text{SS})$  pin is allowed to go high, the soft-start capacitor is charged by a current source (approximately 2  $\mu\text{A}$ ). When the  $\overline{\text{SD}}(\text{SS})$  pin voltage reaches 0.6V (shutdown threshold), the internal regulator circuitry starts to operate. The current charging the soft-start capacitor increases from 2  $\mu\text{A}$  to approximately 10  $\mu\text{A}$ . With the  $\overline{\text{SD}}(\text{SS})$  pin voltage between 0.6V and 1.3V, the level of the current limit is zero, which means the output voltage is still zero. When the  $\overline{\text{SD}}(\text{SS})$  pin voltage increases beyond 1.3V, the current limit starts to increase. The switch duty cycle, which is controlled by the level of the current limit, starts with narrow pulses and gradually gets wider. At the same time, the output voltage of the converter increases towards the nominal value, which brings down the output voltage of the error amplifier. When the output of the error amplifier is less than the current limit voltage, it takes over the control of the duty cycle. The converter enters the normal current-mode PWM operation. The  $\overline{\text{SD}}(\text{SS})$  pin voltage is eventually charged up to about 2V.

The soft-start time can be estimated as:

$$T_{SS} = C_{SS} \times 0.6\text{V} / 2 \mu\text{A} + C_{SS} \times (2\text{V} - 0.6\text{V}) / 10 \mu\text{A} \quad (5)$$

During start-up, the internal circuit is monitoring the soft-start voltage. When the softstart voltage reaches 2V, the undervoltage and overvoltage protections are enabled.

If the output voltage doesn't rise above 80% of the normal value before the soft-start reaches 2V. The undervoltage protection will kick in and shut the device down. You can avoid this by either increasing the value of the soft-start capacitor, or using a LDELAY capacitor.

## LDELAY CAPACITOR

As mentioned in the [Operation](#) section, the LDELAY capacitor sets the time delay between the output voltage goes below 80% of its nominal value and the undervoltage latch protection is enabled.

Charging the CDELAY by a 5  $\mu\text{A}$  current source up to 2V sets the delay time. Therefore,  $T_{\text{DELAY}} = C_{\text{DELAY}} * 2\text{V}/5\mu\text{A}$ .

The undervoltage protection is disabled by tying the LDELAY pin to the ground.

## R<sub>1</sub> and R<sub>2</sub> (PROGRAMMING OUTPUT VOLTAGE)

Use the following formula to select the appropriate resistor values:

$$V_{\text{OUT}} = V_{\text{REF}}(1 + R_1/R_2)$$

where

- $V_{\text{REF}} = 1.238\text{V}$  (6)

Select resistors between 10k $\Omega$  and 100k $\Omega$ . (1% or higher accuracy metal film resistors for R<sub>1</sub> and R<sub>2</sub>.)

## COMPENSATION COMPONENTS

In the control to output transfer function, the first pole  $F_{p1}$  can be estimated as  $1/(2\pi R_{\text{OUT}} C_{\text{OUT}})$ ; The ESR zero  $F_{z1}$  of the output capacitor is  $1/(2\pi \text{ESR} C_{\text{OUT}})$ ; Also, there is a high frequency pole  $F_{p2}$  in the range of 45kHz to 150kHz:

$$F_{p2} = F_s/(\pi n(1-D))$$

where

- $D = V_{\text{OUT}}/V_{\text{IN}}$
- $n = 1 + 0.348L/(V_{\text{IN}} - V_{\text{OUT}})$  (L is in  $\mu\text{H}$ s and  $V_{\text{IN}}$  and  $V_{\text{OUT}}$  in volts) (7)

The total loop gain G is approximately  $500/I_{\text{OUT}}$  where  $I_{\text{OUT}}$  is in amperes.

A Gm amplifier is used inside the LM2653. The output resistor  $R_o$  of the Gm amplifier is about 80k $\Omega$ .  $C_{c1}$  and  $R_c$  together with  $R_o$  give a lag compensation to roll off the gain:

$$F_{pc1} = 1/(2\pi C_{c1}(R_o + R_c)), F_{zc1} = 1/2\pi C_{c1} R_c. \quad (8)$$

In some applications, the ESR zero  $F_{z1}$  cannot be cancelled by  $F_{p2}$ . Then,  $C_{c2}$  is needed to introduce  $F_{pc2}$  to cancel the ESR zero,  $F_{p2} = 1/(2\pi C_{c2} R_o \parallel R_c)$ .

The rule of thumb is to have more than 45° phase margin at the crossover frequency ( $G=1$ ).

If  $C_{\text{OUT}}$  is higher than 68 $\mu\text{F}$ ,  $C_{c1} = 2.2\text{nF}$ , and  $R_c = 15\text{k}\Omega$  are good choices for most applications. If the ESR zero is too low to be cancelled by  $F_{p2}$ , add  $C_{c2}$ .

If the transient response to a step load is important, choose  $R_c$  to be higher than 10k $\Omega$ .

## EXTERNAL SCHOTTKY DIODE

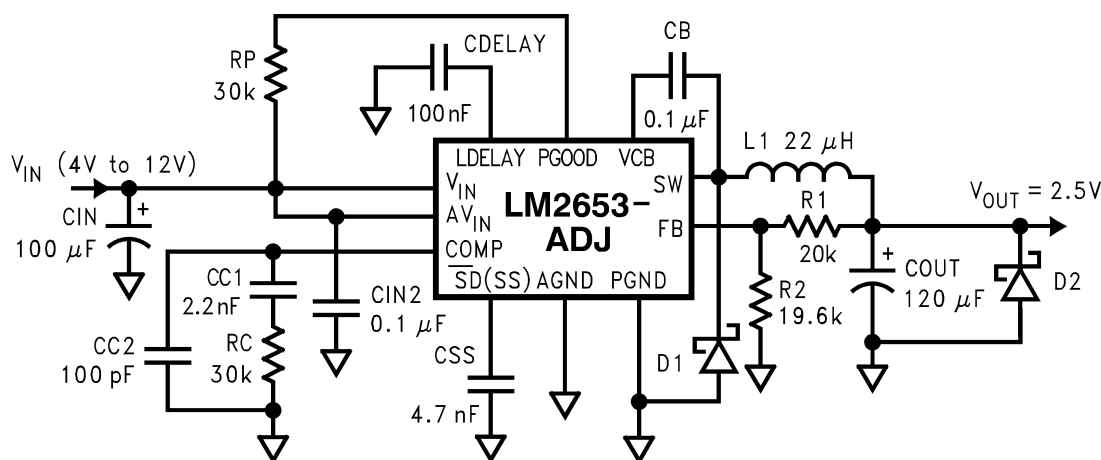
A Schottky diode  $D_1$  is recommended to prevent the intrinsic body diode of the low-side MOSFET from conducting during the deadtime in PWM operation and hysteretic mode when both MOSFETs are off. If the body diode turns on, there is extra power dissipation in the body diode because of the reverse-recovery current and higher forward voltage; the high-side MOSFET also has more switching loss since the negative diode reverse-recovery current appears as the high-side MOSFET turn-on current in addition to the load current. These losses degrade the efficiency by 1-2%. The improved efficiency and noise immunity with the Schottky diode become more obvious with increasing input voltage and load current.

The breakdown voltage rating of  $D_1$  is preferred to be 25% higher than the maximum input voltage. Since  $D_1$  is only on for a short period of time, the average current rating for  $D_1$  only requires being higher than 30% of the maximum output current. It is important to place  $D_1$  very close to the drain and source of the low-side MOSFET, extra parasitic inductance in the parallel loop will slow the turn-on of  $D_1$  and direct the current through the body diode of the low-side MOSFET.

## PCB Layout Considerations

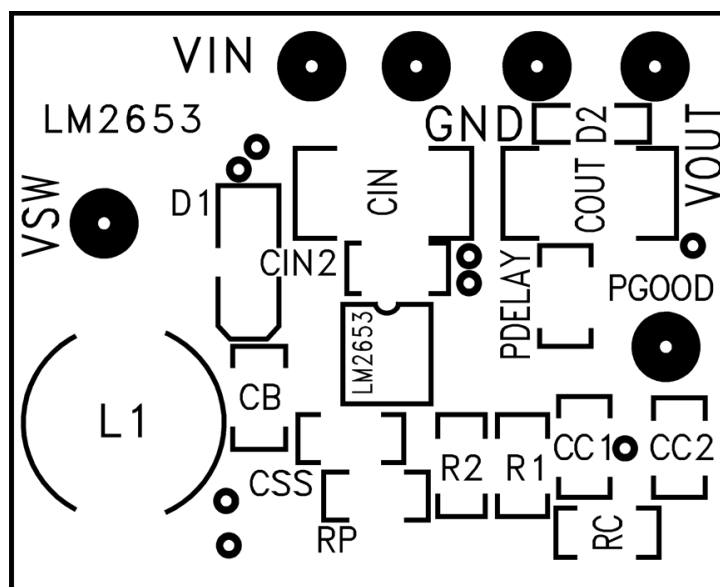
Layout is critical to reduce noises and ensure specified performance. The important guidelines are listed as follows:

1. Minimize the parasitic inductance in the loop of input capacitors and the internal MOSFETs by connecting the input capacitors to  $V_{IN}$  and PGND pins with short and wide traces. This is important because the rapidly switching current, together with wiring inductance can generate large voltage spikes that may result in noise problems.
2. Minimize the trace from the center of the output resistor divider to the FB pin and keep it away from noise sources to avoid noise pick up. For applications require tight regulation at the output, a dedicated sense trace (separated from the power trace) is recommended to connect the top of the resistor divider to the output.
3. If the Schottky diode  $D_1$  is used, minimize the traces connecting  $D_1$  to SW and PGND pins.



**Figure 16. Schematic for the Typical Board Layout**

### Typical PC Board Layout: (2X Size)



### Figure 17. Component Placement Guide

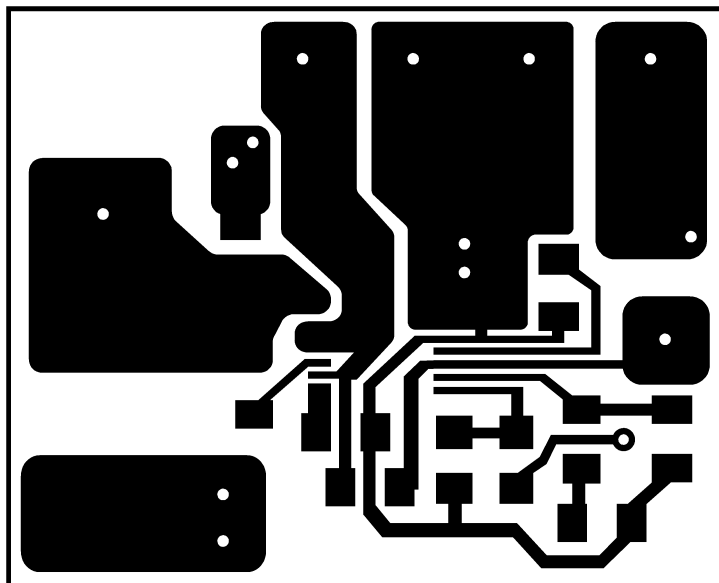


Figure 18. Component Side PC Board Layout

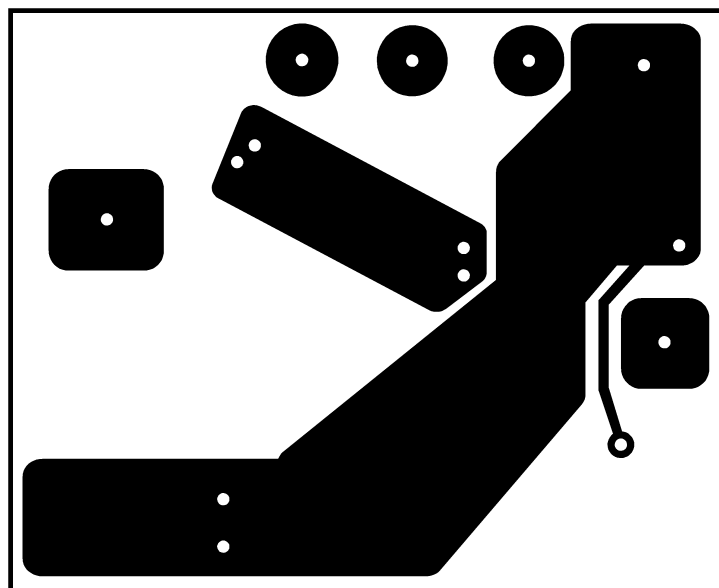


Figure 19. Solder Side PC Board Layout

## REVISION HISTORY

### Changes from Revision D (April 2013) to Revision E

### Page

- Changed layout of National Data Sheet to TI format ..... [13](#)

## PACKAGING INFORMATION

| Orderable part number               | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LM2653MTC-ADJ/NOPB</a>  | Active        | Production           | TSSOP (PW)   16 | 92   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | 2653MT<br>C-ADJ     |
| LM2653MTC-ADJ/NOPB.A                | Active        | Production           | TSSOP (PW)   16 | 92   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | 2653MT<br>C-ADJ     |
| LM2653MTC-ADJ/NOPB.B                | Active        | Production           | TSSOP (PW)   16 | 92   TUBE             | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | 2653MT<br>C-ADJ     |
| LM2653MTCX-ADJ/NO.A                 | Active        | Production           | TSSOP (PW)   16 | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | 2653MT<br>C-ADJ     |
| <a href="#">LM2653MTCX-ADJ/NOPB</a> | Active        | Production           | TSSOP (PW)   16 | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | 2653MT<br>C-ADJ     |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device              | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM2653MTCX-ADJ/NOPB | TSSOP        | PW              | 16   | 2500 | 330.0              | 12.4               | 6.95    | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

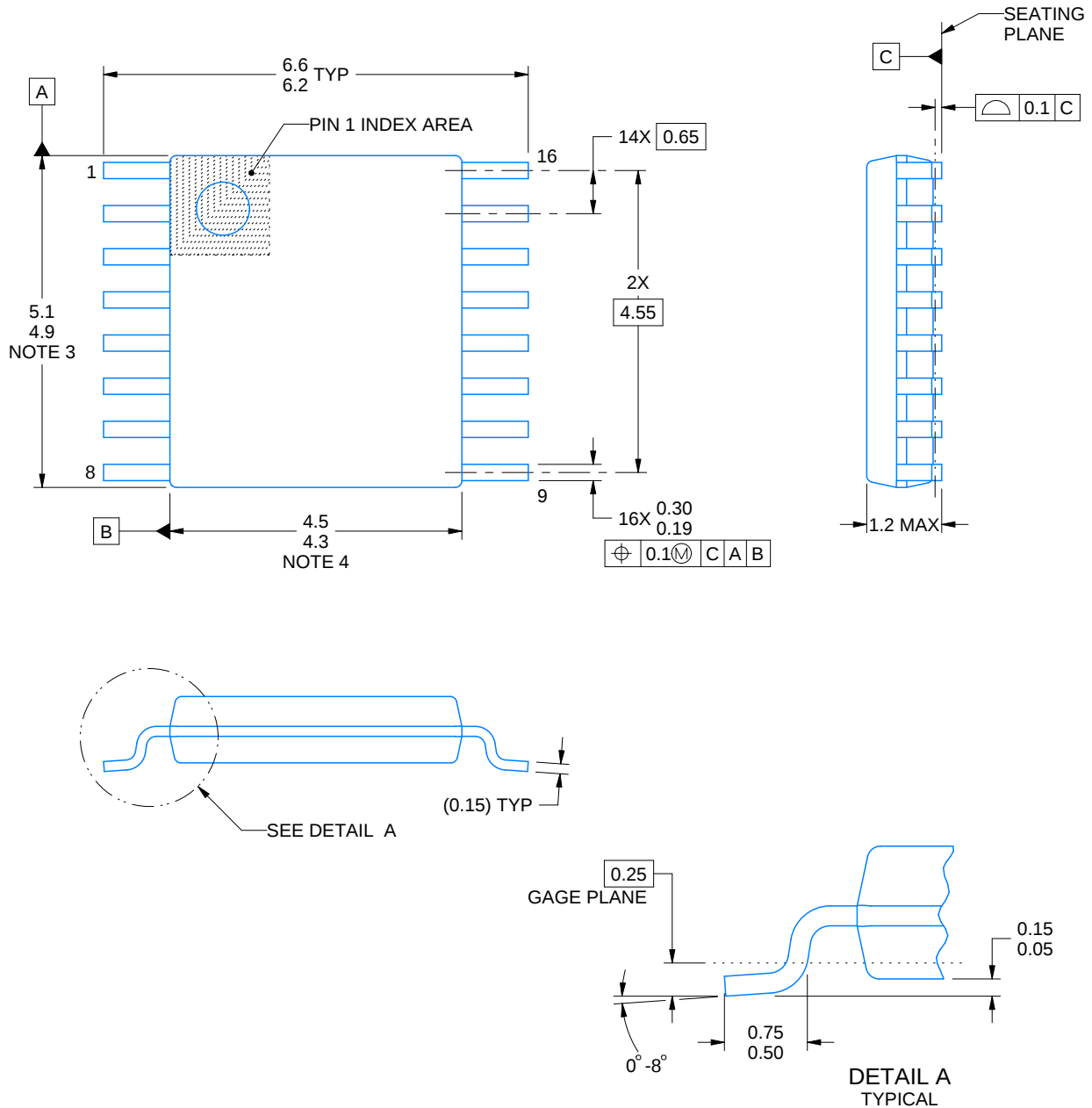
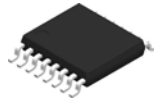
| Device              | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM2653MTCX-ADJ/NOPB | TSSOP        | PW              | 16   | 2500 | 367.0       | 367.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device               | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LM2653MTC-ADJ/NOPB   | PW           | TSSOP        | 16   | 92  | 495    | 8      | 2514.6 | 4.06   |
| LM2653MTC-ADJ/NOPB.A | PW           | TSSOP        | 16   | 92  | 495    | 8      | 2514.6 | 4.06   |
| LM2653MTC-ADJ/NOPB.B | PW           | TSSOP        | 16   | 92  | 495    | 8      | 2514.6 | 4.06   |



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## NOTES:

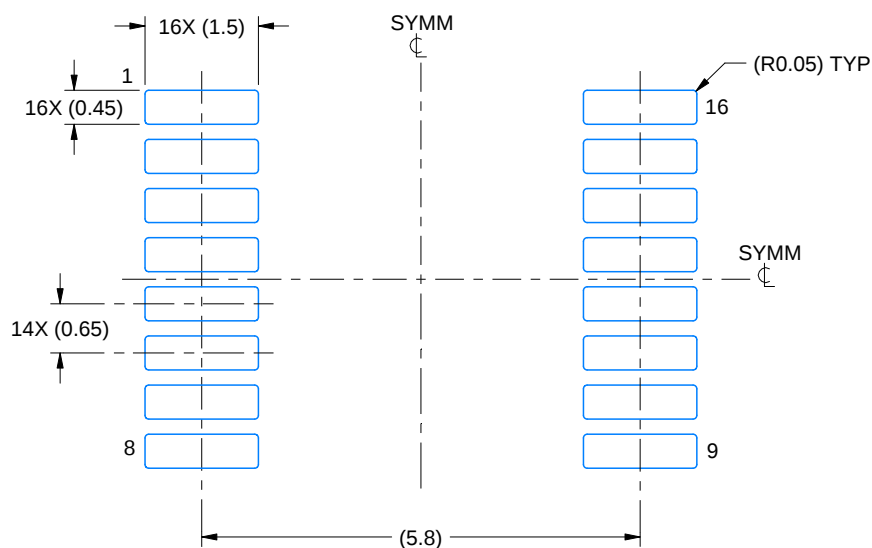
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

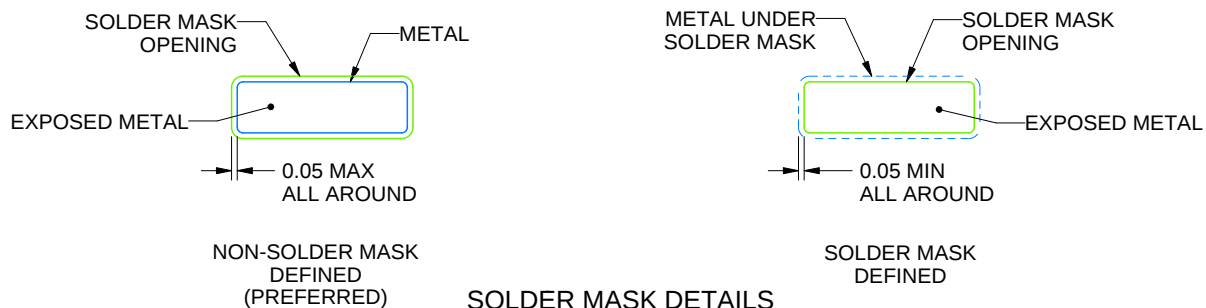
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

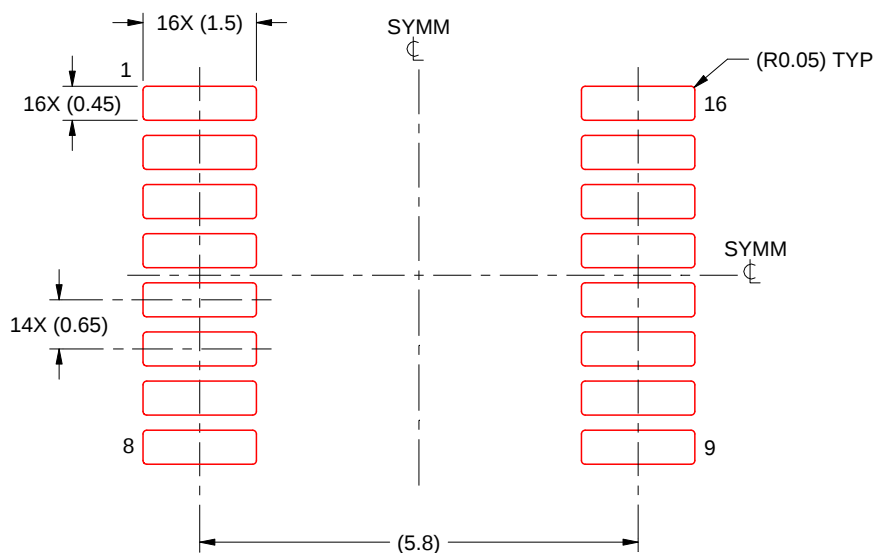
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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