TAS5729MD 12-W I²S Input Class-D Amplifier With Digital Audio Processor and DirectPath™ HP and Line Driver

1 Features

- Audio I/O Configuration:
  - Single Stereo I²S Input
  - Stereo BTL or Mono PBTL Operation
  - 8-kHz to 48-kHz Sample Rates
  - Headphone Amplifier and Line Driver
- Audio Digital Signal Processing:
  - Digital Equalization
  - Two-Band Automatic Gain Limiting
  - Coarse and Fine Volume Control
  - PWM Level Meter
- General Operational Features:
  - I²C Software Control With Programmable I²C Address (101010[R/W] or 101011[R/W])
  - AD, BD, Ternary Modulation
  - Overtemperature, Undervoltage, Clock, and Overcurrent Protection
- Audio Performance (PVDD = 18 V, R_{LOAD} = 8 Ω)
  - Idle Channel Noise = 56 µVrms
  - THD+N at 1 W, 1 kHz, = 0.15%
  - SNR = 105 dB (reference to 0 dBFS)

2 Applications

- LCD/LED TV and Multipurpose Monitors
- Sound Bars, Docking Stations, PC Audio
- Consumer Audio Equipment

3 Description

The TAS5729MD is a stereo I²S input device which includes a digital auto processor with two-band automatic gain limiting (AGL), digital equalization, course and fine volume control, and PWM level meter. The AGL is an enhanced dynamic range compression (DRC) function. The device can operate from a wide PVDD power supply range to enable use in numerous applications. The TAS5729MD operates with a nominal supply voltage from 4.5 to 24 VDC. The device is controlled by an I²C control port. The device has an integrated DirectPath™ headphone amplifier and line driver to increase system-level integration and reduce total solution costs.

An optimal mix of thermal performance and device cost is provided in the 200-mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced HTSSOP provides excellent operation in the elevated ambient temperatures found in today's modern consumer electronic devices.

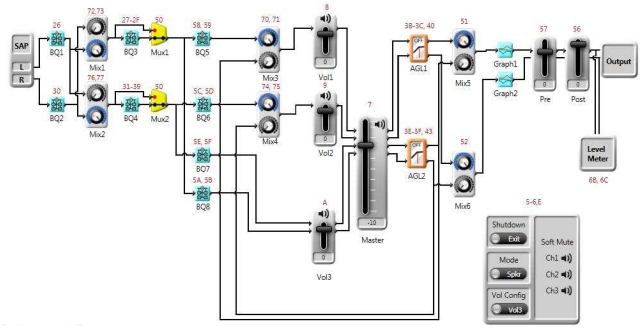
The entire TAS5729xx family is pin-to-pin compatible allowing a single hardware solution to be used across several end application platforms. Additionally, the I²C register map in the entire TAS5729xx family is identical to ensure low development overhead to choose between devices based upon system level requirements.

Device Information(1)

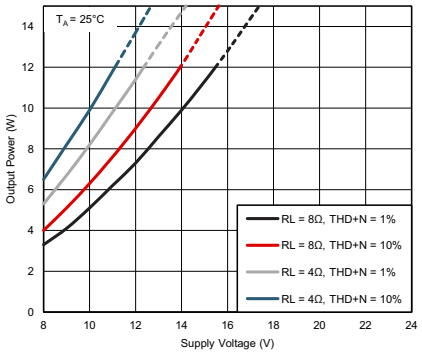
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5729MD	HTSSOP (48)	12.50 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Signal Processing Flow



Power at 10% THD+N vs PVDD



NOTE: Dashed lines represent thermally limited region.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2016) to Revision E — **Page**

- Changed *Features* From: "Address (1010100[R/W] or 1010101[R/W])" To: Address (101010[R/W] or 101011[R/W])" ... 1
- Changed I2C adress From: 1010101[R/W] To: 101011[R/W]) and (1010100[R/W] To: 101010[R/W]) in the *ADR/SPK_FAULT* section ... 17

Changes from Revision C (March 2015) to Revision D — **Page**

- Added the *Recommended Start-Up and Shutdown Procedures* section to the *Detailed Design Procedure* section ... 50

Changes from Revision B (September 2014) to Revision C — **Page**

- Changed the minimum load that the TAS5729MD can drive in BTL mode to 4 Ohms. Updated plots to reflect this change ... 11

Changes from Revision A (June 2013) to Revision B — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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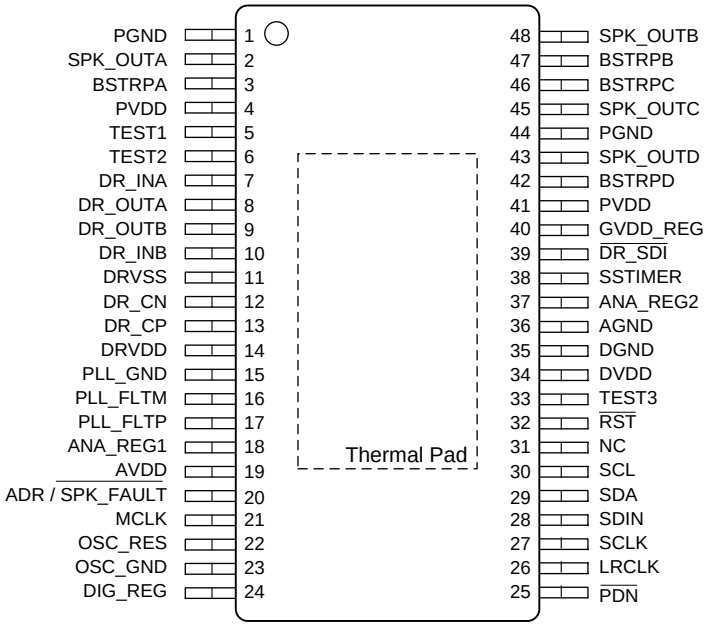
5 Related Devices

DEVICE NAME	DESCRIPTION
TAS5729MD	12-W I²S Input Class-D Amplifier with Digital Audio Processor and DirectPath HP and Line Driver
TAS5707	20-W Stereo I^2S Audio Power Amplifier with Speaker EQ and DRC
TAS5721	15-W Stereo (2.1) Class-D Audio Amp with Integrated HP Amplifier Audio Processing

6 Pin Configuration and Functions

DCA Package
48-Pin HTSSOP With PowerPAD™
Top View



Pin Functions

PIN		TYPE(1)	TERMINATION	DESCRIPTION
NAME	NUMBER			
ADR/SPK_FAULT	20	DI/DO	—	Dual-function pin which sets the LSB of the 7-bit I^2C address to 0 if pulled to GND, 1 if pulled to DVDD. If configured to be a fault output via the System Control Register 2 (0x05), this pin is pulled low when an internal fault with the speaker amplifier occurs. A pullup or pulldown resistor is required, as is shown in the *Typical Applications*.
AGND	36	P	—	Ground for analog circuitry(2)
AVDD	19	P	—	Power supply for internal analog circuitry
ANA_REG1	18	P	—	Linear voltage regulator output derived from AVDD supply which is used for internal analog circuitry. Nominal 1.8-V output.(3)
ANA_REG2	37	P	—	Linear voltage regulator output derived from AVDD supply which is used for internal analog circuitry. Nominal 3.3-V output.(3)
BSTRPx	3, 42, 46, 47	P	—	Connection points for the bootstrap capacitors which are used to create a power supply for the high-side gate drive of the device.
DGND	35	P	—	Ground for digital circuitry(2)
DIG_REG	24	P	—	Linear voltage regulator output derived from the DVDD supply which is used for internal digital circuitry.(3)

(1) TYPE: AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, P = Power, G = Ground (0 V)
(2) This pin should be connected to the system ground.
(3) This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.

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Pin Functions (continued)

PIN		TYPE(1)	TERMINATION	DESCRIPTION
NAME	NUMBER			
DR_CN	12	P	—	Negative pin for capacitor connection used in headphone amplifier and line driver charge pump
DR_CP	13	P	—	Positive pin for capacitor connection used in headphone amplifier and line driver charge pump
DR_INx	7, 10	AI	—	Input for channel A or B of headphone amplifier or line driver
DR_OUTx	8, 9	AO	—	Output for channel A or B of headphone amplifier or line driver
$\overline{\text{DR_SDI}}$	39	DI	—	Places the headphone amplifier/line driver in shutdown when pulled low.
DRVSS	11	P	—	Negative supply generated by charge pump for ground centered headphone and line driver output
DRVDD	14	P	—	Power supply for internal headphone and line driver circuitry
DVDD	34	P	—	Power supply for the internal digital circuitry
GVDD_REG	40	P	—	Voltage regulator derived from PVDD supply(3)
LRCLK	26	DI	Pulldown	Word select clock of the serial audio port.
MCLK	21	DI	Pulldown	Master clock used for internal clock tree and sub-circuit and state machine clocking
NC	31	—	—	Not connected inside the device (all NC terminals should be connected to ground for optimal thermal performance)
OSC_GND	23	P	—	Ground for oscillator circuitry (this terminal should be connected to the system ground)
OSC_RES	22	AO	—	Connection point for oscillator trim resistor
$\overline{\text{PDN}}$	25	DI	Pullup	Quick powerdown of the device that is used upon an unexpected loss of the PVDD or DVDD power supply to quickly transition the outputs of the speaker amplifier to Hi-Z. This quick powerdown feature avoids the audible anamolies that would occur as a result of loss of either of the supplies.
PGND	1, 44	P	—	Ground for power device circuitry(2)
PLL_FLTM	16	AI/AO	—	Negative connection point for the PLL loop filter components
PLL_FLTP	17	AI/AO	—	Positive connection point for the PLL loop filter components
PLL_GND	15	P	—	Ground for PLL circuitry (this terminal should be connected to the system ground)
PowerPAD™	—	P	—	Thermal and ground pad that provides both an electrical connection to the ground plane and a thermal path to the PCB for heat dissipation. This pad must be grounded to the system ground. (2)
PVDD	4, 41	P	—	Power supply for internal power circuitry
$\overline{\text{RST}}$	32	DI	Pullup	Places the device in reset when pulled low
SCL	30	DI	—	I^2C serial control port clock
SCLK	27	DI	Pulldown	Bit clock of the serial audio port
SDA	29	DI/DO	—	I^2C serial control port data
SDIN	28	DI	Pulldown	Data line to the serial data port
SPK_OUTx	2, 43, 45, 48	AO	—	Speaker amplifier outputs
SSTIMER	38	AI	—	Controls ramp time of SPK_OUTx to minimize pop. Leave this pin floating for BD mode. Requires capacitor to GND in AD mode, as is shown in *Typical Applications*. The capacitor determines the ramp time.
TEST1	5	DO	—	Used for testing during device production (this terminal must be left floating)
TEST2	6	DO	—	Used for testing during device production (this terminal must be left floating)
TEST3	33	DI	—	Used for testing during device production (this terminal must be connected to GND)

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7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Temperature	Ambient operating temperature, T_A	0	85	°C
Supply voltage	DVDD, DRVDD, AVDD	–0.3	4.2	V
	PVDD	–0.3	30	V
Input voltage	DVDD referenced digital inputs	–0.5	DVDD + 0.5	V
	5-V tolerant digital inputs (2)	–0.5	DVDD + 2.5(3)	V
	DR_INx	DRVSS – 0.3	DRVDD + 0.3	V
HP Load	R_{LOAD}(HP)	12.8	N/A	Ω
Line Driver Load	R_{LOAD}(LD)	600	N/A	Ω
Voltage at speaker output pins	SPK_OUTx	–0.03	32	V
Voltage at BSTRPx pins	BSTRPx	–0.03	39	V
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) 5-V tolerant inputs are $\overline{PDN}$, $\overline{RESET}$, SCLK, LRCLK, MCLK, SDIN, SDA, and SCL.
(3) Maximum pin voltage should not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Ambient operating temperature	0	85	°C
VDD	DVDD, DRVDD, and AVDD supply	2.97	3.63	V
PVDD	PVDD supply	4.5	26.4(1)	V
V_{IH}	Input logic high	2		V
V_{IL}	Input logic low		0.8	V
R_{HP}	Minimum HP load	16		Ω
R_{LD}	Minimum line driver load	600		Ω
$R_{SPK(BTL)}$	Minimum speaker load in BTL mode	4		Ω
$R_{SPK(PBTL)}$	Minimum speaker load in post-filter PBTL mode	4		Ω
L_{FILT}	Minimum output inductance under short-circuit condition	10		µH

(1) For operation at PVDD levels greater than 18 V, the modulation limit must be set to 93.8% via the control port register 0x10.

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7.4 Thermal Information

THERMAL METRIC(1)		TAS5729MD		UNIT
		DCA(2)	DCA(3)	
		48 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.6	32.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (bottom) thermal resistance	17.9	16.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	14.3	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (top) thermal resistance	1.5	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metricsapplication report.
(2) JEDEC Standard 2 Layer Board
(3) JEDEC Standard 4 Layer Board

7.5 Digital I/O Pins

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|I_{IH}\|$	Input logic high current level	All digital pins			75	µA
V_{IH}	Input logic high threshold for DVDD referenced digital inputs	All digital pins	2			V
$\|I_{IL}\|$	Input logic low current level	All digital pins			75	µA
V_{IL}	Input logic low threshold for DVDD referenced digital inputs	All digital pins			0.8	V
V_{OH}	Output logic high voltage level	I_{OH} = 4 mA, VDD = 3 V	2.4			V
V_{OL}	Output logic low voltage level	I_{OH} = –4 mA, VDD = 3 V			0.5	V

7.6 Master Clock

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
D_{MCLK}	Allowable MCLK duty cycle	40%	50%	60%	
f_{MCLK}	Supported MCLK frequencies	2.8224		24.576	MHz
t_r t_f	Rise or fall time for MCLK			5	ns

7.7 Serial Audio Port

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK}	Supported SCLK frequencies	Values include 32, 48, and 64	32		64	× f_S
D_{SCLK}	Allowable SCLK duty cycle		40%	50%	60%	
t_{su2}	Required SDIN setup time before SCLK rising edge		10			ns
t_{h2}	Required SDIN hold time after SCLK rising edge		10			ns
f_S	Supported input sample rates		8		48	kHz
D_{LRCLK}	Allowable LRCLK duty cycle		40%	50%	60%	
t_{su1}	Required LRCLK to SCLK rising edge 10					ns
t_{h1}	Required LRCLK to SCLK rising edge		10			ns
t_r, t_f	Rise or fall time for SCLK and LRCLK				8	ns
	Allowable LRCLK drift before LRCLK reset				4	MCLKs

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7.8 Protection Circuitry

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OCE_{THRES}	Overcurrent threshold for each BTL output	PVDD = 15 V, T_A = 25°C		4.5		A
$UVE_{THRES(PVDD)}$	Undervoltage error (UVE) threshold	PVDD falling		4		V
$UVE_{THRES(AVDD)}$	Undervoltage error (UVE) threshold	AVDD falling		4.1		V
$UVE_{HYST(PVDD)}$	UVE recovery threshold	PVDD rising		4.5		V
$UVE_{HYST(AVDD)}$	UVE recovery threshold	AVDD rising		2.7		V
OTE_{THRES}	Overtemperature error (OTE) threshold			150		°C
OTE_{HYST}	OTE recovery threshold			30		°C

7.9 Speaker Amplifier in All Modes

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SPK_AMP}	Speaker amplifier switching frequency	11.025-, 22.05-, or 44.1-kHz data rate ±2%		352.8		kHz
		48-, 24-, 12-, 8-, 16-, or 32-kHz data rate ±2%		384		kHz
$R_{DS(ON)}$	On resistance of output MOSFET (both high-side and low-side)	PVDD = 15 V, T_A = 25°C, die only		200		mΩ
		PVDD = 15 V, T_A = 25°C, includes: die, bond wires, leadframe		240		mΩ
R_{PD}	Internal pulldown resistor at output of each half-bridge making up the full bridge outputs	Connected when drivers are hi-Z to provide bootstrap capacitor charge		3		kΩ

7.10 Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode

T_A = 25°C, PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal = 1-kHz sine wave, BTL, AD mode, f_S = 48 kHz, RSPK = 8 Ω, AES17 filter, f_{PWM} = 384 kHz, external components per *Typical Characteristics*, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ICN_{(SPK)}$	Idle channel noise	PVDD = 18 V, A-Weighted		56		µVrms
$P_{O(SPK)}$	Maximum continuous output power per channel	PVDD = 13 V, 10% THD, 1-kHz input signal		10.5		W
		PVDD = 8 V, 10% THD, 1-kHz input signal		4		W
		PVDD = 18 V, 10% THD, 1-kHz input signal		12		W
$SNR_{(SPK)}$	Signal-to-noise ratio (referenced to 0dBFS input signal)	PVDD = 18 V, A-weighted, f = 1 kHz, maximum power at THD < 1%		105		dB
$THD+N_{(SPK)}$	Total harmonic distortion and noise	PVDD = 18 V; P_O = 1 W		0.15%		
		PVDD = 13 V; P_O = 1 W		0.13%		
		PVDD = 8 V; P_O = 1 W		0.2%		
$X\text{-}Talk_{(SPK)}$	Crosstalk (worst case between L- to-R and R-to-L coupling)	P_O = 1 W, f = 1 kHz (BD mode)		–70		dB
		P_O = 1 W, f = 1 kHz (AD mode)		–48		dB

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7.11 Speaker Amplifier in Stereo Post-Filter Parallel Bridge Tied Load (Post-Filter PBTL) Mode

T_A = 25°C, PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal = 1-kHz sine wave, BTL, AD mode, f_S = 48 kHz, RSPK = 4 Ω, AES17 filter, f_{PWM} = 384 kHz, external components per *Typical Characteristics*, and in accordance with recommended operating conditions (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ICN_{(SPK)}$	Idle channel noise	PVDD = 18 V, A-Weighted		42		µVrms
$P_{O(SPK)}$	Maximum continuous output power per channel	PVDD = 13 V, 10% THD, 1-kHz input signal		18.9		W
		PVDD = 8 V, 10% THD, 1-kHz input signal		7.2		W
		PVDD = 18 V, 10% THD, 1-kHz input signal		24		W
$SNR_{(SPK)}$	Signal-to-noise ratio (referenced to 0dBFS input signal)	PVDD = 18 V, A-weighted, f = 1 kHz, maximum power at THD < 1%		105		dB
$THD+N_{(SPK)}$	Total harmonic distortion and noise	PVDD = 18 V; P_O = 1 W		0.06%		
		PVDD = 13 V; P_O = 1 W		0.03%		
		PVDD = 8 V; P_O = 1 W		0.15%		

7.12 Headphone Amplifier and Line Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CP}	Charge pump switching frequency		200	300	400	kHz
$P_{O(HP)}$	Headphone amplifier output power	R_{LOAD}(HP) = 32 Ω, THD+N = 1%, outputs in phase		55		mW
$SNR_{(HP)}$	Signal-to-noise ratio	(Referenced to 55-mW output signal), R_{LOAD}(HP) = 32 Ω, A-Weighted		101		dB
$SNR_{(LD)}$	Signal-to-noise ratio	(Referenced to 2-Vrms output signal), R_{LOAD}(LD) = 10 kΩ, A-Weighted		105		dB

7.13 Reset Timing

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{w(RESET)}$	Pulse duration required to reset the device	100			µs

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7.14 I²C Control Port

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{L(I^2C)}$	Allowable load capacitance for each I²C line				400	pF
f_{SCL}	Supported SCL frequency	No wait states	100		400	kHz
t_{buf}	Bus free time between stop and start conditions		1.3			µs
$t_{f(I^2C)}$	Rise time, SCL and SDA				300	ns
$t_{h1(I^2C)}$	Hold time, SCL to SDA		0			ns
$t_{h2(I^2C)}$	Hold time, start condition to SCL		0.6			µs
$t_{I^2C(start)}$	I²C startup time	Time to enable I²C from RST release	12			ms
$t_{r(I^2C)}$	Rise time, SCL and SDA				300	ns
$t_{su1(I^2C)}$	Setup time, SDA to SCL		100			ns
$t_{su2(I^2C)}$	Setup time, SCL to start condition		0.6			µs
$t_{su3(I^2C)}$	Setup time, SCL to stop condition		0.6			µs
$T_{w(H)}$	Required pulse duration, SCL high		0.6			µs
$T_{w(L)}$	Required pulse duration, SCL low		1.3			µs

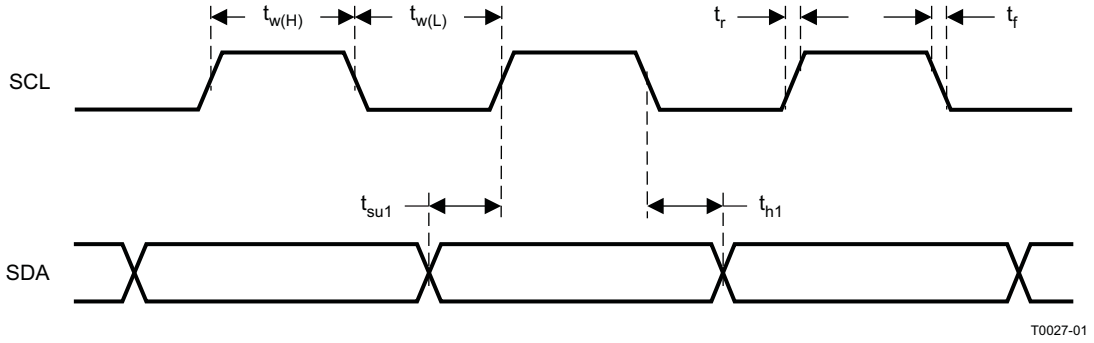

Figure 1. SCL and SDA Timing for I²C Control Port

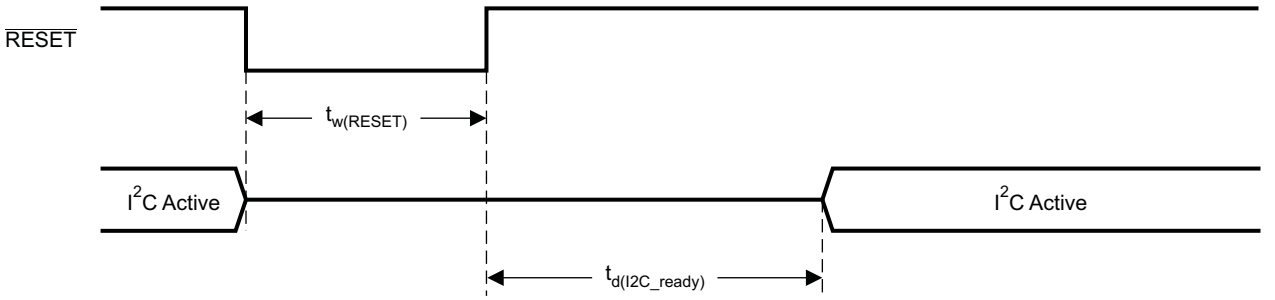

Figure 2. Start and Stop Timing Conditions

7.15 Typical Electrical Power Consumption

over operating free-air temperature range (unless otherwise noted), with DVDD = DRVDD = 3.3 V and AVDD = PVDD, external components as specified on the EVM.

SPEAKER AMPLIFIER STATE		CONFIGURATION SETTINGS	V_{PVDD} [V]	I_{PVDD} [mA]	I_{VDD} [mA]	P_{DISS} (From all Supplies) [W]
f_{SPK_AMP}	OPERATIONAL STATE					
384kHz	Idle	$\overline{RST}$ pulled high, speaker amplifier outputs at 50/50 mute	18	20	48	0.51
	Reset	$\overline{RST}$ pulled low, $\overline{PDN}$ pulled high		5	21	0.16

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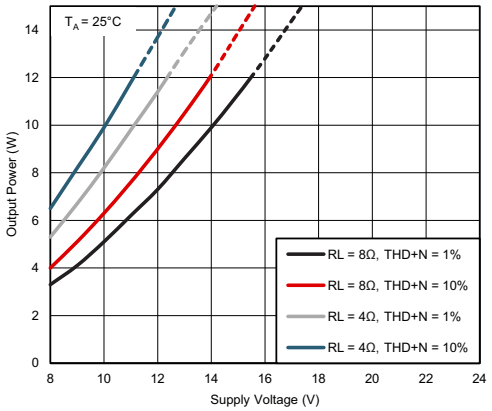
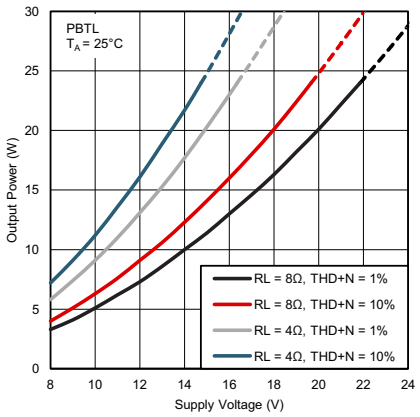
7.16 Typical Characteristics

7.16.1 Speaker Amplifier



Dashed lines represent thermally limited region.

Figure 3. Output Power vs PVDD in BTL Mode



Dashed lines represent thermally limited region.

Figure 4. Output Power vs PVDD in Post-Filter PBTL Mode

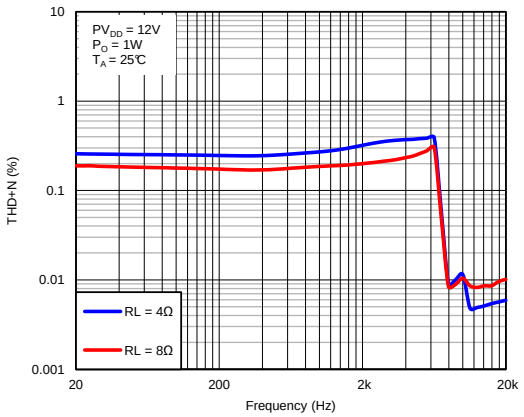


Figure 5. Total Harmonic Distortion + Noise vs Frequency in BTL Mode With PVDD = 12 V

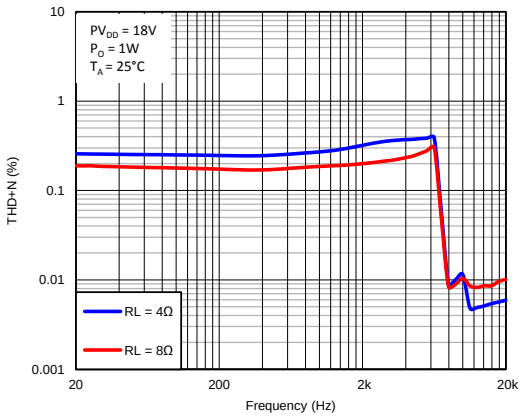


Figure 6. Total Harmonic Distortion + Noise vs Frequency in BTL Mode With PVDD = 18 V

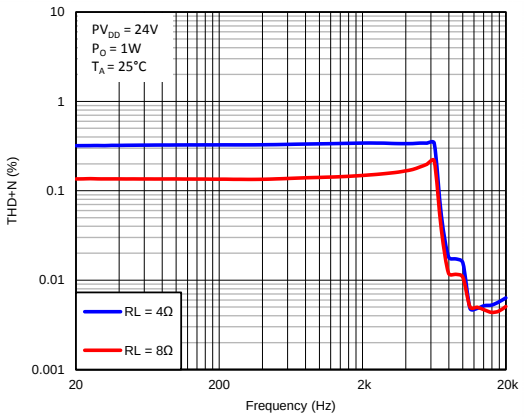


Figure 7. Total Harmonic Distortion + Noise vs Frequency in BTL Mode With PVDD = 24 V

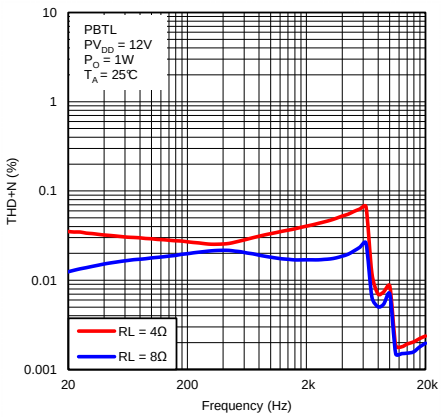


Figure 8. Total Harmonic Distortion + Noise vs Frequency in Post-Filter PBTL Mode With PVDD = 12 V

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Speaker Amplifier (continued)

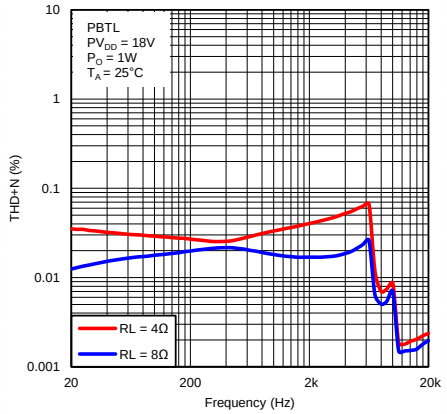

Figure 9. Total Harmonic Distortion + Noise vs Frequency in Post-Filter PBTL Mode With PVDD = 18 V

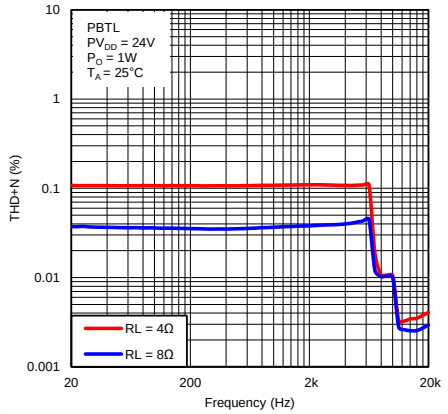

Figure 10. Total Harmonic Distortion + Noise vs Frequency in Post-Filter PBTL Mode With PVDD = 24 V

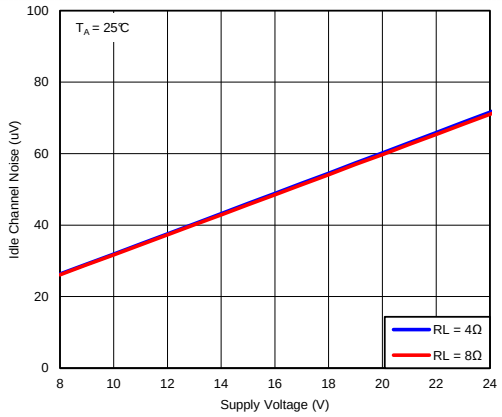

Figure 11. Stereo BTL Idle Channel Noise vs PVDD

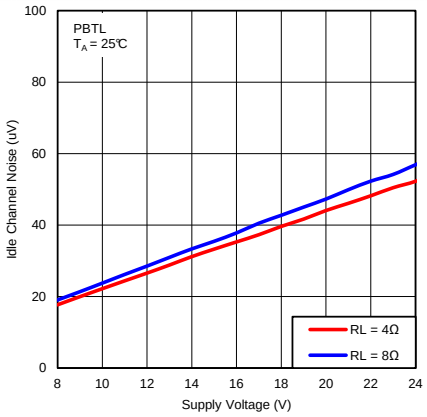

Figure 12. Post-Filter PBTL Idle Channel Noise vs PVDD

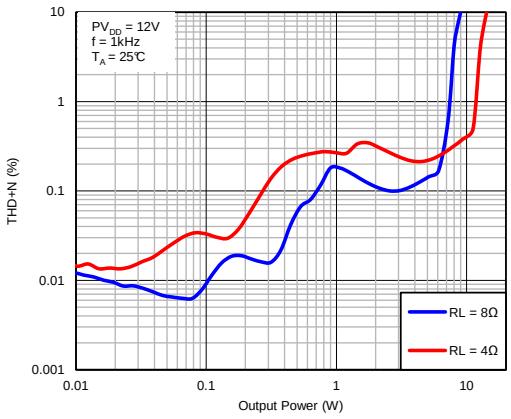

Figure 13. Total Harmonic Distortion + Noise vs Output Power in BTL Mode With PVDD = 12 V

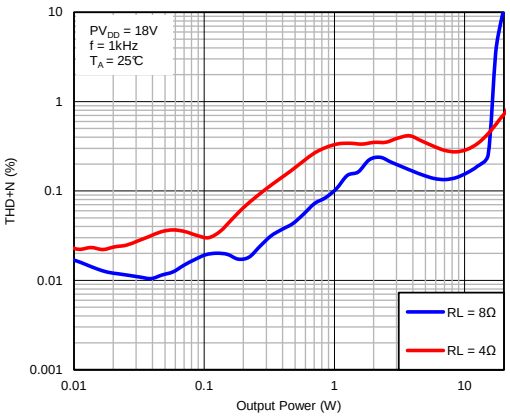

Figure 14. Total Harmonic Distortion + Noise vs Output Power in BTL Mode With PVDD = 18 V

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Speaker Amplifier (continued)

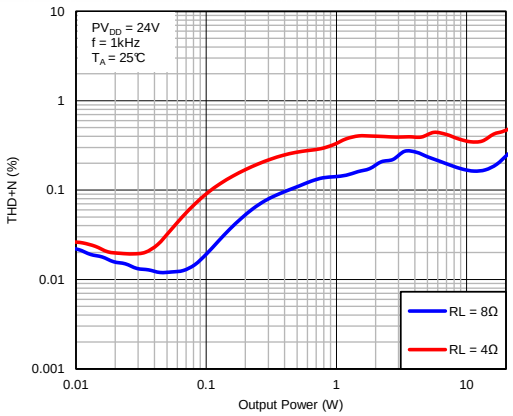


Figure 15. Total Harmonic Distortion + Noise vs Output Power in BTL Mode With PVDD = 24 V

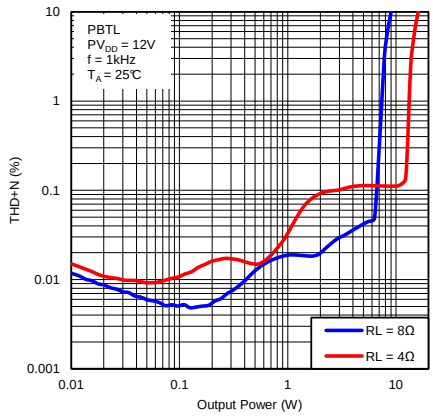


Figure 16. Total Harmonic Distortion + Noise vs Output Power in Post-Filter PBTL Mode With PVDD = 12 V

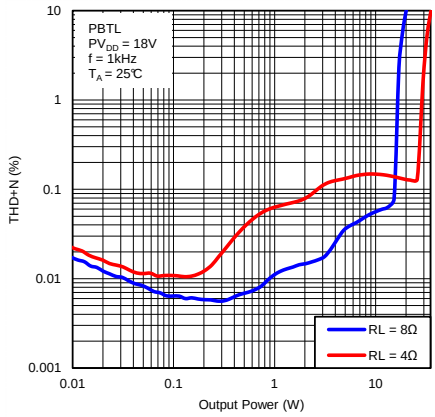


Figure 17. Total Harmonic Distortion + Noise vs Output Power in Post-Filter PBTL Mode With PVDD = 18 V

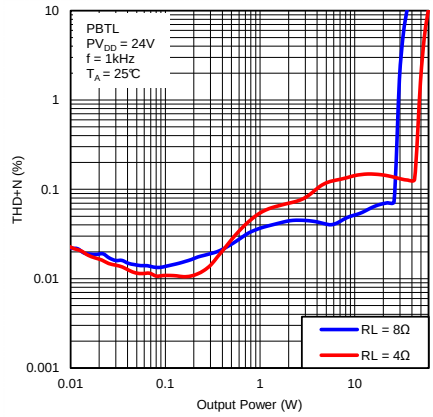
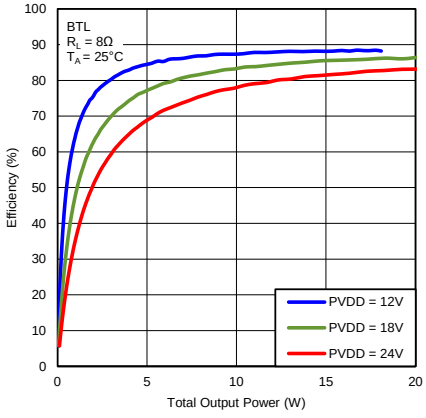
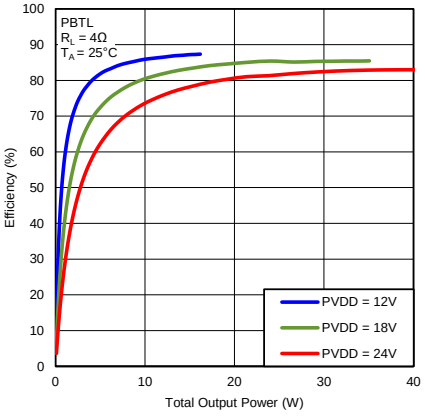


Figure 18. Total Harmonic Distortion + Noise vs Output Power in Post-Filter PBTL Mode With PVDD = 24 V



All channels driven

Figure 19. Efficiency vs Output Power in BTL Mode



All channels driven

Figure 20. Efficiency vs Output Power in Post-Filter PBTL Mode

Speaker Amplifier (continued)

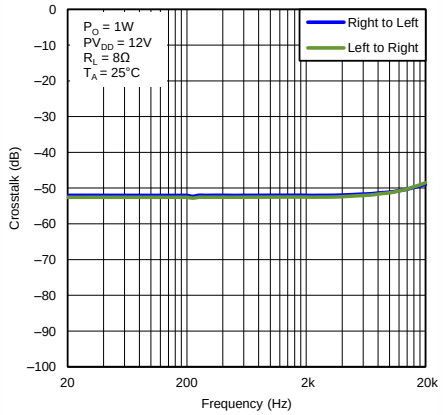


Figure 21. 8-Ohm Load Crosstalk vs Frequency in BTL Mode With PVDD = 12 V

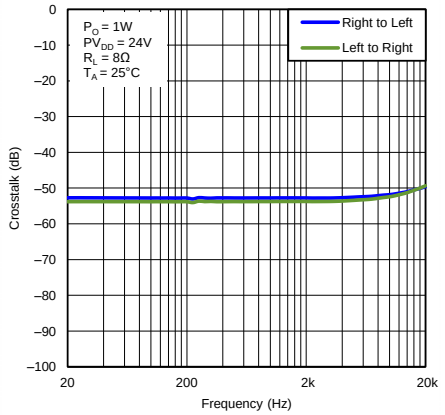


Figure 22. 8-Ohm Load Crosstalk vs Frequency in BTL Mode With PVDD = 24 V

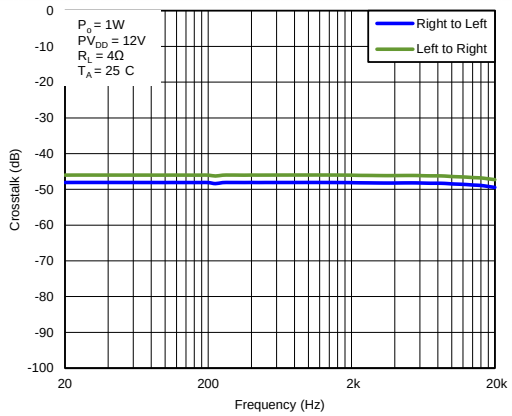


Figure 23. 4-Ohm Load Crosstalk vs Frequency in BTL Mode With PVDD = 12 V

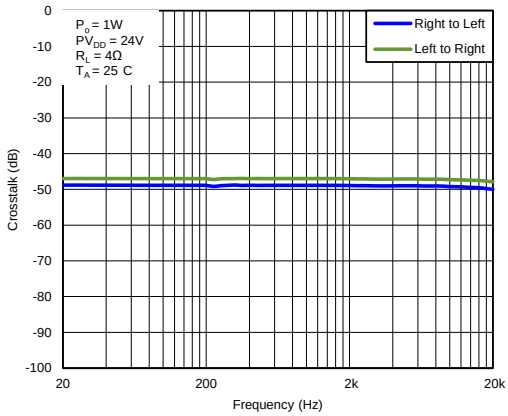


Figure 24. 4-Ohm Load Crosstalk vs Frequency in BTL Mode With PVDD = 24 V

7.16.2 Headphone Amplifier

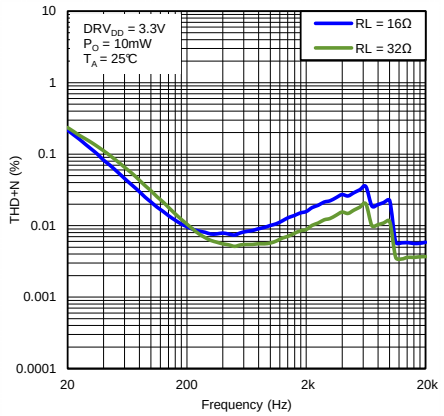


Figure 25. Headphone Total Harmonic Distortion + Noise vs Frequency With DRVDD = 3.3 V

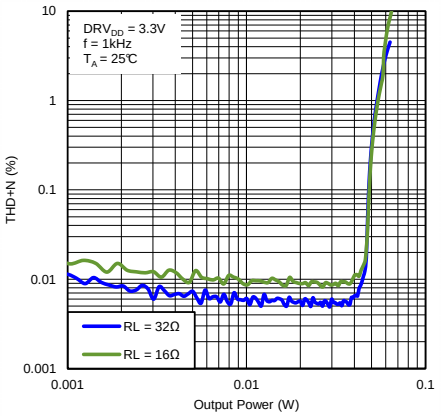


Figure 26. Headphone Total Harmonic Distortion + Noise vs Output Power With DRVDD = 3.3 V

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Headphone Amplifier (continued)

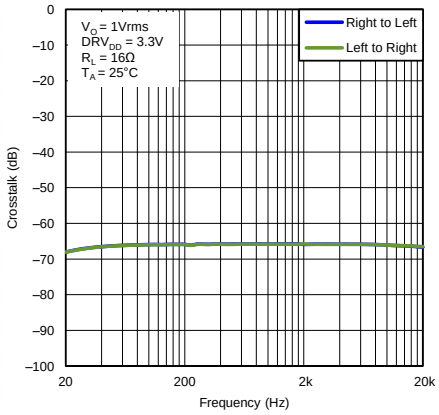


Figure 27. Headphone Crosstalk vs Frequency with DRVDD = 3.3 V and R_{HP} = 16 Ω

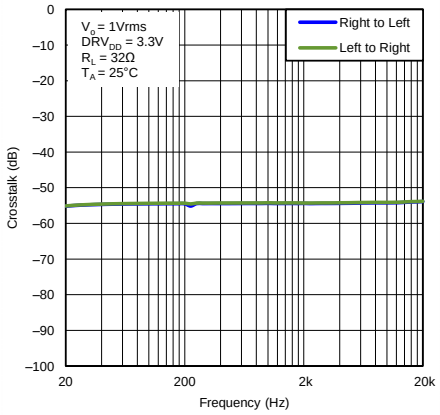


Figure 28. Headphone Crosstalk vs Frequency with DRVDD = 3.3 V and R_{HP} = 32 Ω

7.16.3 Line Driver

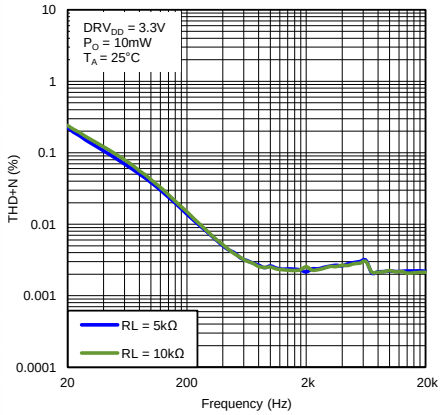


Figure 29. Line Driver Total Harmonic Distortion + Noise vs Frequency With DRVDD = 3.3 V

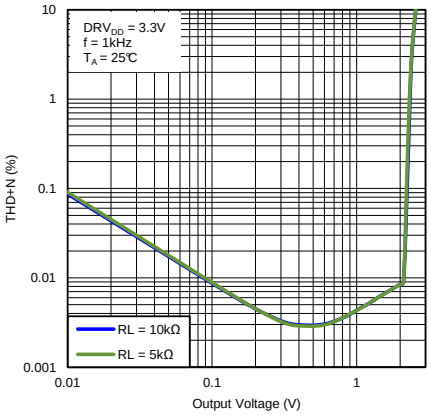


Figure 30. Line Driver THD+N vs Output Voltage With DRVDD = 3.3 V

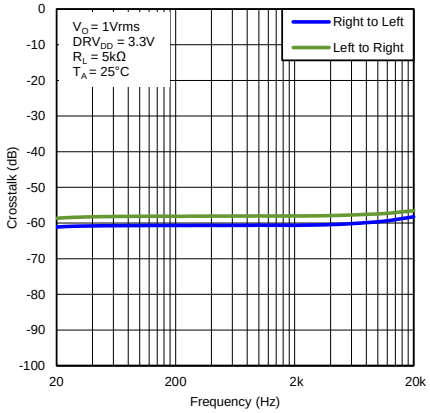


Figure 31. Line Driver Crosstalk vs Frequency With DRVDD = 3.3 V

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

9 Detailed Description

9.1 Overview

The TAS5729MD is a stereo I^2S input Class-D amplifier with a digital audio processor and a DirectPath™ headphone/line driver.

Digital auto processor features two-band advanced automatic gain limiting (AGL), digital equalization, course and fine volume control, and PWM Level meter. The AGL is an enhanced dynamic range compression (DRC) function.

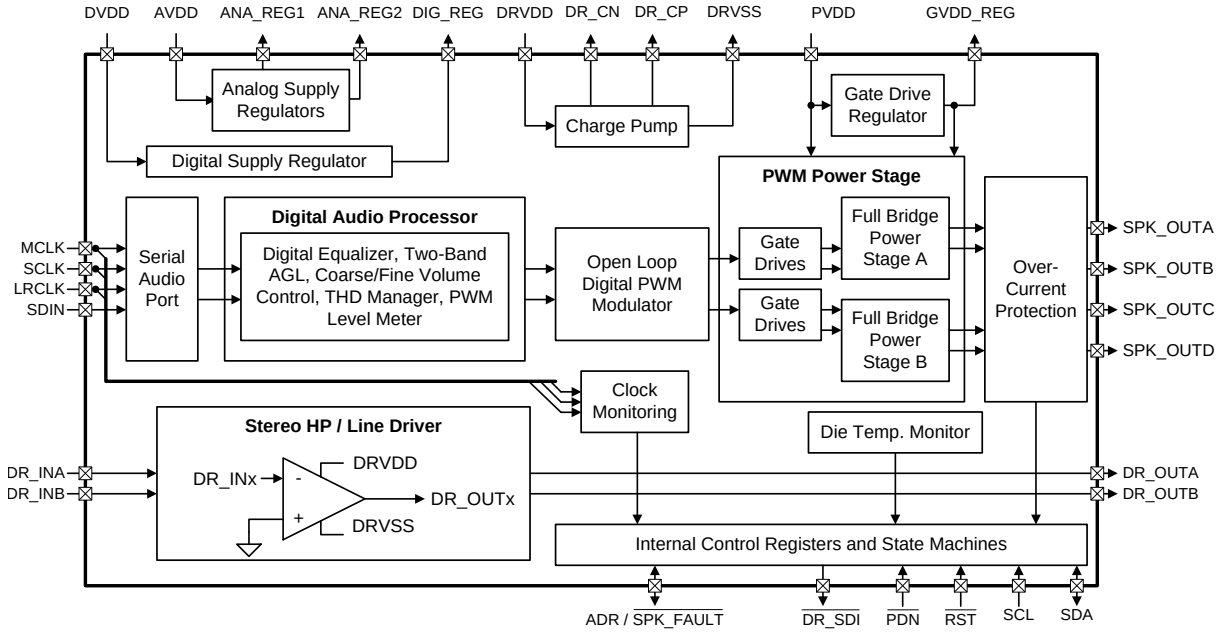
The device requires only a single DVDD supply in addition to the higher-voltage PVDD power supply. The wide PVDD power supply range of the device enables its use in a multitude of applications.

The TAS5729MD is a slave-only device that is controlled by a bidirectional I^2C interface that supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This control interface is used to program the registers of the device and read the device status.

The device has an integrated DirectPath headphone amplifier / line driver to increase system level integration and reduce total solution costs. DirectPath architecture eliminates the requirement for external dc-blocking output capacitors.

An optimal mix of thermal performance and device cost is provided in the 200-mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced 48-pin HTSSOP provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Power Supply

To facilitate system design, the TAS5729MD requires only a single low-voltage DVDD supply in addition to the higher-voltage PVDD power supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply (for example, the high-side gate drive) is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

To provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges that operate in pairs to produce the full-bridge outputs capable of driving BTL loads. For this reason, each half-bridge has separate bootstrap pins (BSTRPx) and power-stage supply pins (PVDD). The gate drive voltage (GVDD_REG) is derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSTRPx) to the power-stage output pin (SPK_OUTx). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD_REG) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each pair of half-bridges has independent power-stage supply pins (PVDD). For optimal electrical performance, EMI compliance, and system reliability, each PVDD pin must be decoupled with a ceramic capacitor placed as close as possible to each supply pin, as shown in *Typical Applications*.

9.3.2 ADR/$\overline{\text{SPK_FAULT}}$

The ADR/$\overline{\text{SPK_FAULT}}$ pin is an input pin during power-up, and can be pulled high or low through a pullup or pulldown resistor, as shown in *Typical Applications*. High sets an I^2C address of 101011[$^R/_W$], and low sets an address of 101010[$^R/_W$]. Additionally, via the control port, the ADR/$\overline{\text{SPK_FAULT}}$ pin can be configured to serve as the fault indicator for the speaker amplifier.

9.3.3 Device Protection System

9.3.3.1 Overcurrent (OC) Protection With Current Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by a protection system. If a high-current condition persists, that is, the power stage is being overloaded, a protection system triggers a shutdown resulting in the power stage being set in the high-impedance (Hi-Z) state. The device retries to start-up based on the retry time set in the BKDN_ERR register and returns to normal operation once the fault condition (that is, a short-circuit on the output) is removed. Current limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shutdown. An overcurrent fault error is reported in the ERROR STATUS register, and a fault error signal can be monitored on the SPK_FAULT pin if configured in the system control register.

9.3.3.2 Overtemperature Protection

The TAS5729MD has an overtemperature-protection system. If the device junction temperature exceeds the amount specified by OTE_{THRES} in the *Protection Circuitry* table, the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state. The TAS5729MD recovers automatically once the temperature drops by the amount specified by OTE_{HYST}. An overtemperature fault error is reported in the ERROR STATUS register, and a fault error signal can be monitored on the SPK_FAULT pin if configured in the system control register.

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Feature Description (continued)

9.3.3.3 Undervoltage Error (UVE) and Power-On Reset (POR)

The UVE and POR circuits of the TAS5729MD fully protect the device in any power-up, powerdown, or brownout situation. While powering up, the POR circuit ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach their respective UVE_{THRES} levels as specified in the *Protection Circuitry* table. Although PVDD and AVDD are independently monitored, a supply voltage drop below the UVE threshold for AVDD or either of the PVDD pins results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state. An undervoltage fault error is reported in the ERROR STATUS register, and a fault error signal can be monitored on the $\overline{\text{SPK_FAULT}}$ pin if configured in the system control register.

9.3.4 Clock, Auto Detection, and PLL

The TAS5729MD is an I^2S slave device that requires a valid master clock (MCLK), bit clock (SCLK), and word clock (LRCLK) to play audio. The digital audio processor (DAP) supports all of the sample rates and MCLK rates that are defined in the *Clock Control Register (0x00)*. The TAS5729MD checks to verify that SCLK is a specific value of 32 × f_S, 48 × f_S, or 64 × f_S. The DAP only supports a 1 × f_S LRCLK.

The device has robust clock error handling that uses a built-in auto detect block to quickly detect changes or errors. When the system detects a clock change or error, it mutes the audio (through a single-step mute) and forces PLL to limp, where output PWMs continue to switch in idle but the device cannot play audio. Once the clocks are valid and stable, the system auto detects the new rate and reverts to normal operation. During this process, the volume is restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x0E).

Table 1 shows the valid MCLK rates across different f_S rates. For 44.1-kHz or 48-kHz f_S rates, a 64 × f_S MCLK rate is supported. If a 64 × f_S SCLK rate is used, a common 64 × f_S clock can be used for both MCLK and SCLK.

Table 1. Supported LRCLK, SCLK, and MCLK Ratios in the TAS5729MD

LRCLK Rate [kHz]	MCLK Rate [× f_S]					
	64	128	192	256	384	512
8	—	—	—	—	Y	Y
11.025 or 12	—	—	—	Y	Y	Y
16	—	—	—	Y	Y	Y
22.05 or 24	—	—	—	Y	Y	Y
32	—	—	Y	Y	Y	Y
44.1 or 48	Y	Y	Y	Y	Y	Y

9.3.5 Serial Data Interface

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5729MD DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, or I^2S serial data format.

9.3.6 PWM Section

The TAS5729MD DAP device uses noise-shaping and sophisticated nonlinear correction algorithms to achieve high-power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has internal dc-blocking filters that can be enabled and disabled using the *System Control Register 1 (0x03)*. The controls for the dc-blocking filters are ganged together and enabling or disabling will affect both channels simultaneously. The filter cutoff frequency is less than 1 Hz. Individual-channel de-emphasis filters for 44.1 kHz and 48 kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

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9.3.7 I²C Compatible Serial Control Interface

The TAS5729MD DAP has an I²C serial control slave interface to receive commands from a system controller. The serial control interface supports both normal-speed (100 kHz) and high-speed (400 kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent.

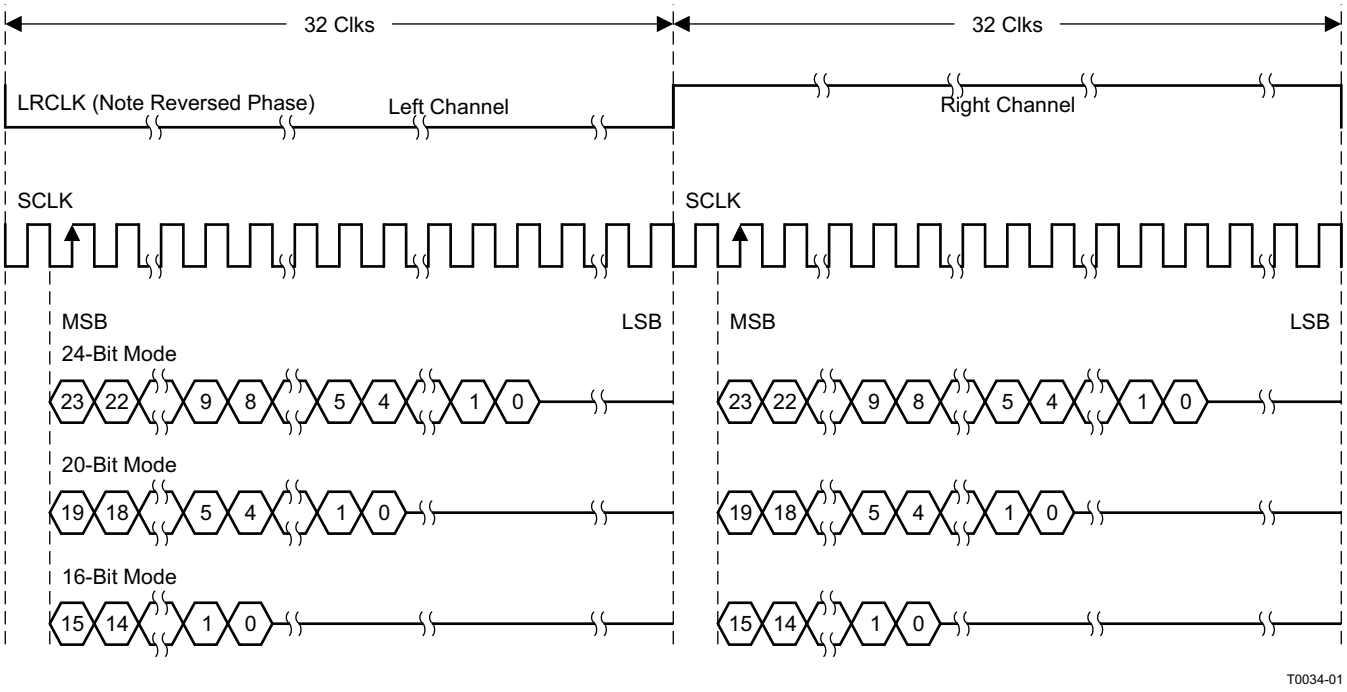
The serial control interface supports both single-byte and multiple-byte read and write operations for status registers and the general control registers associated with the PWM.

9.3.8 Serial Interface Control And Timing

9.3.8.1 I²S Timing

I²S timing uses LRCLK to define when the data being transmitted is for the left channel and when the data is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. A delay of one bit clock exists from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused trailing data-bit positions.

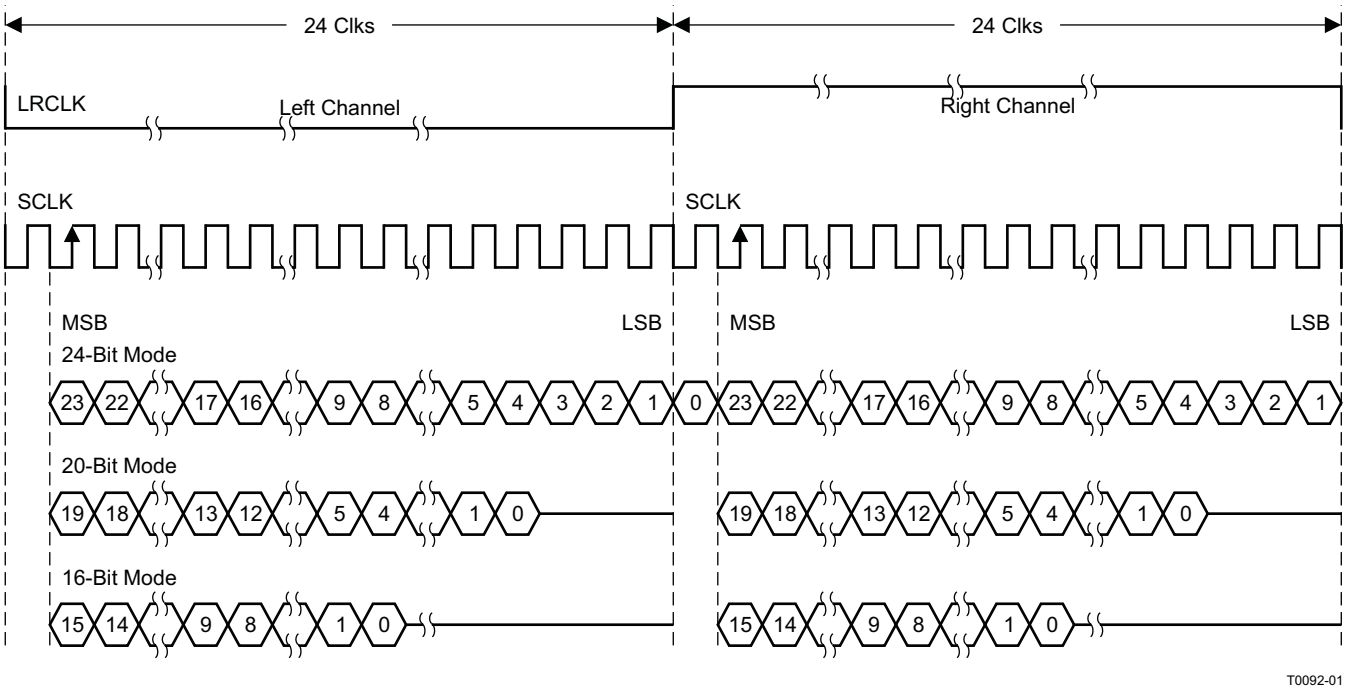
2-Channel I²S (Philips Format) Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 32. I²S 64 × f_S Format

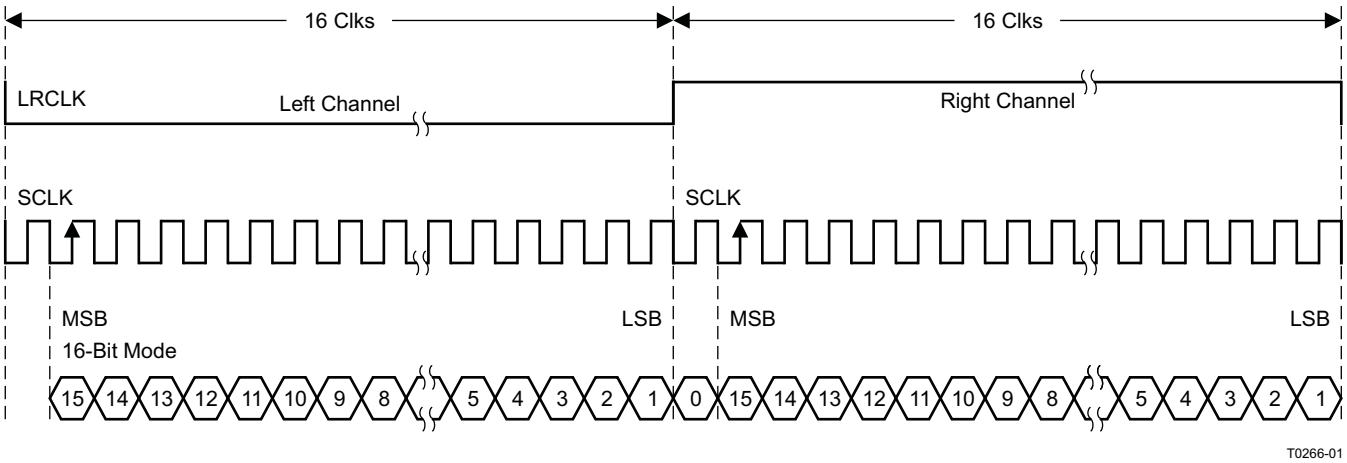
2-Channel I²S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)



NOTE: All data presented in 2s-complement form with MSB first.

Figure 33. I²S 48 × f_S Format

2-Channel I²S (Philips Format) Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 34. I²S 32 × f_S Format

9.3.8.2 Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when the data is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data-bit positions.

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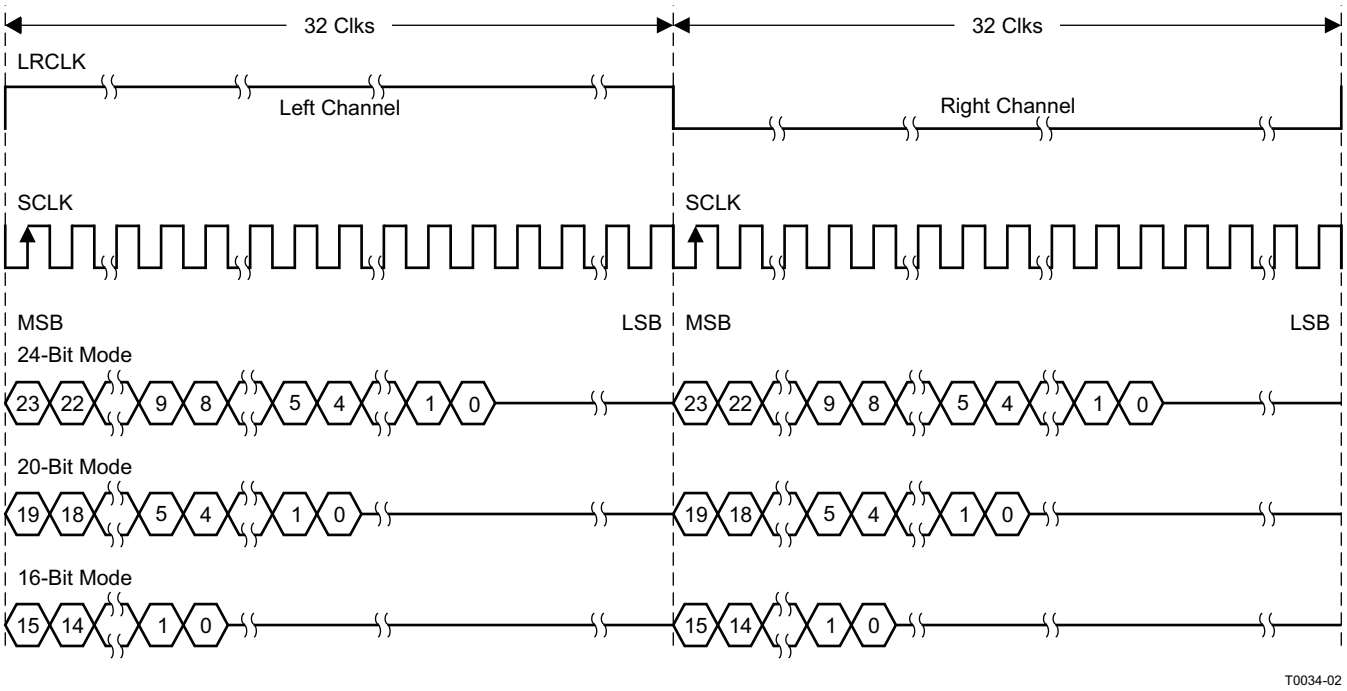
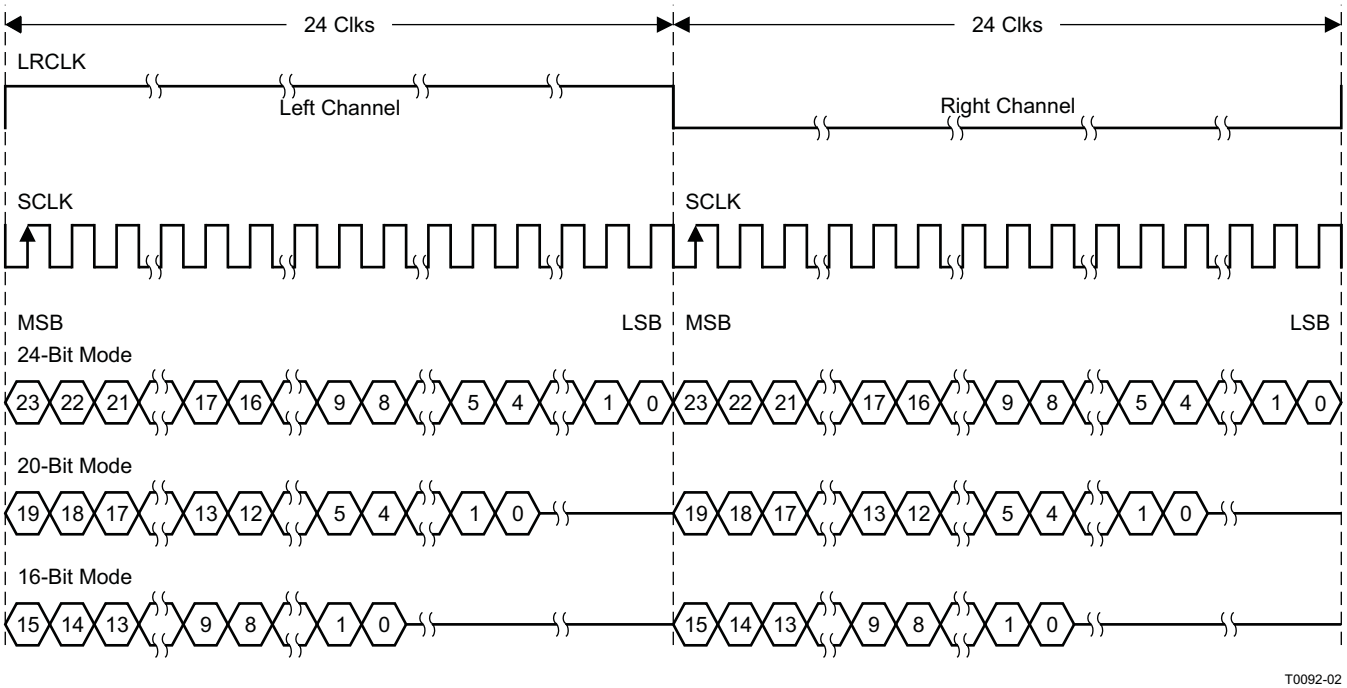
2-Channel Left-Justified Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 35. Left-Justified 64 × f_S Format

2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)



NOTE: All data presented in 2s-complement form with MSB first.

Figure 36. Left-Justified 48 × f_S Format

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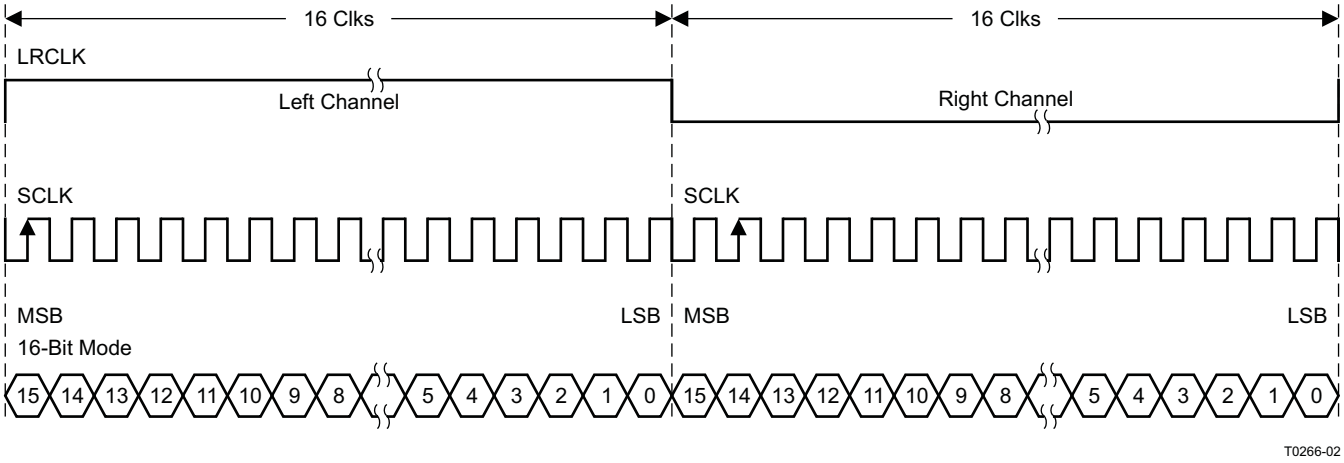
2-Channel Left-Justified Stereo Input



NOTE: All data presented in 2s-complement form with MSB first.

Figure 37. Left-Justified 32 × f_S Format

9.3.8.3 Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when the data is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The DAP masks unused leading data-bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

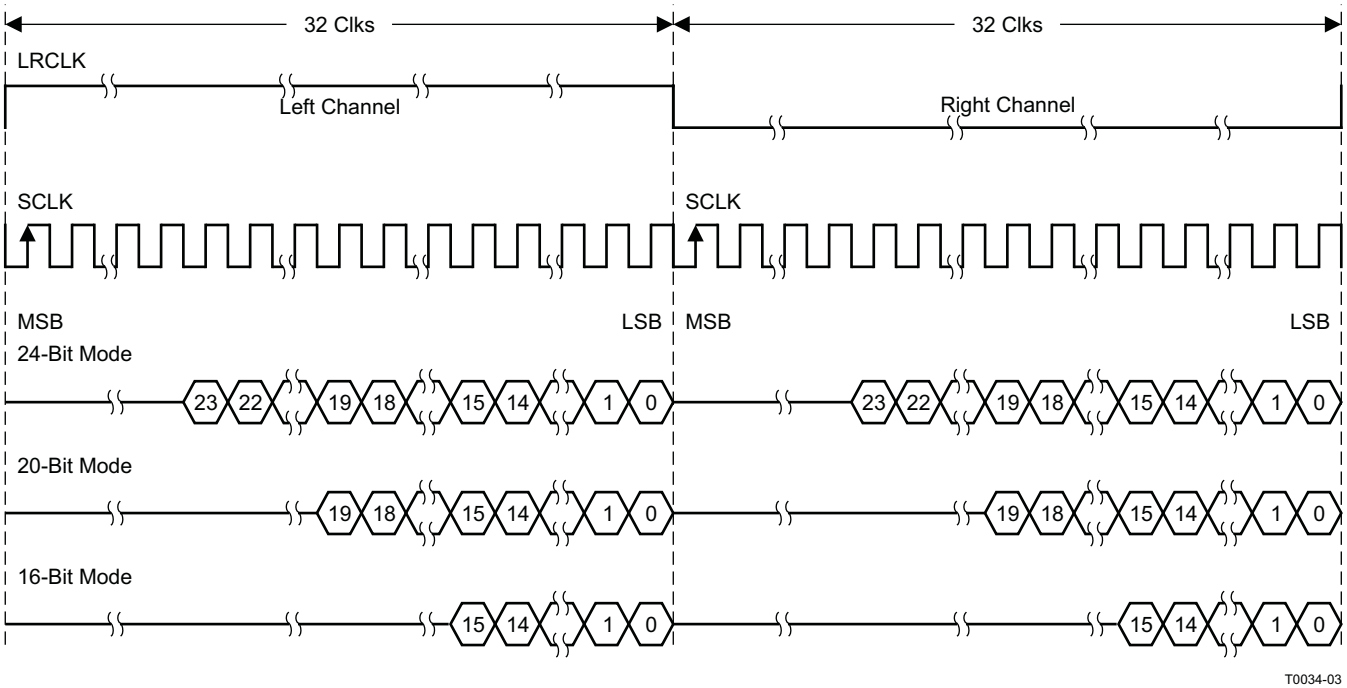


Figure 38. Right-Justified 64 × f_S Format

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2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

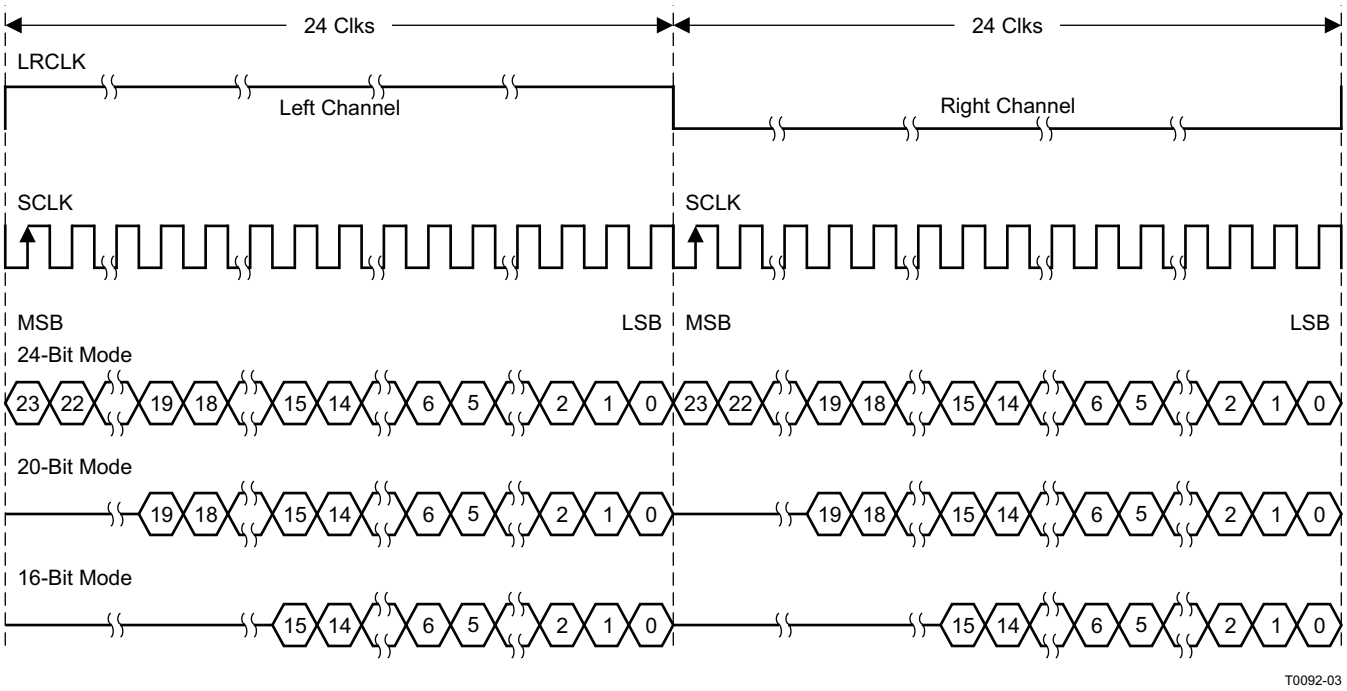


Figure 39. Right-Justified 48 × f_S Format

2-Channel Right-Justified (Sony Format) Stereo Input

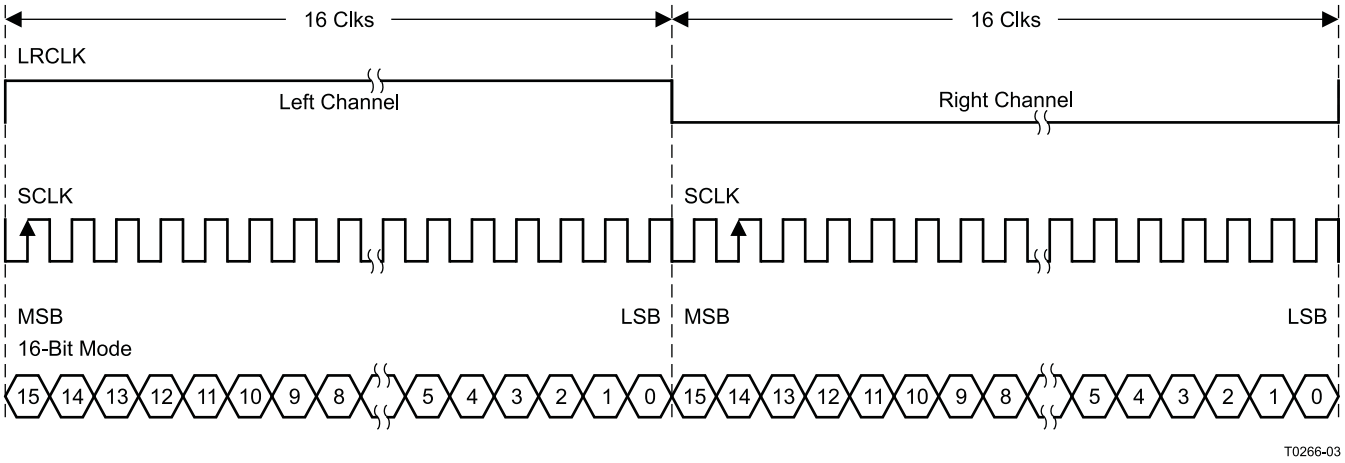
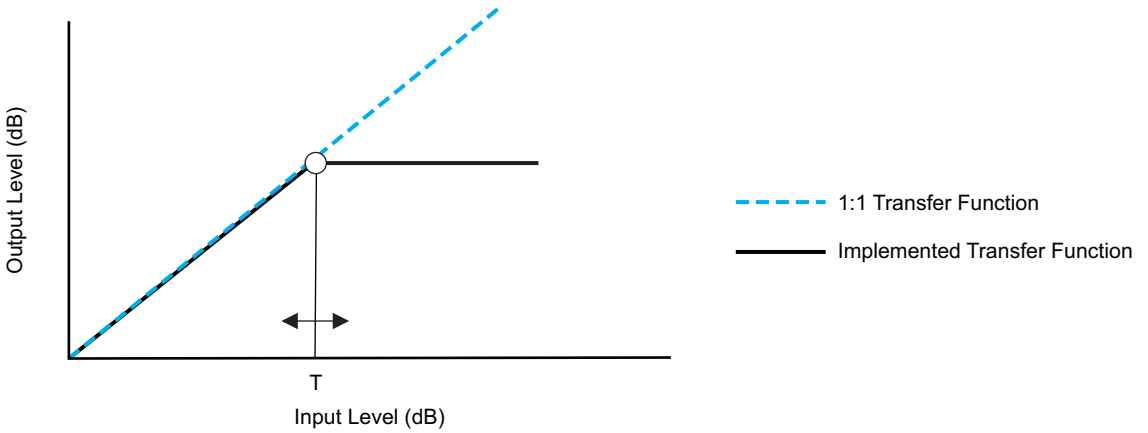


Figure 40. Right-Justified 32 × f_S Format

9.3.9 Automatic Gain Limiting (AGL)

The AGL scheme has two AGL blocks. The high-band left/right channels have one ganged AGL and the low-band left/right channels have the other AGL.

The AGL input/output diagram is shown in Figure 41.

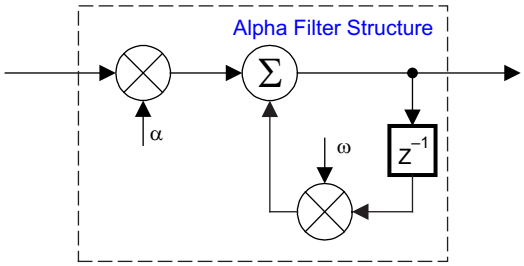


Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- Each AGL has adjustable threshold levels.
- Programmable attack and release rate
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

Figure 41. Automatic Gain Limiting

	α, ω	T	α_a, ω_a / α_d, φ_d
AGL1	0x3B	0x40	0x3C
AGL2	0x3E	0x43	0x3F



T = 9.23 format, all other AGL coefficients are 3.23 format

Figure 42. AGL Structure

9.3.10 PWM Level Meter

The structure in Figure 43 shows the PWM level meter that can be used to study the power profile.

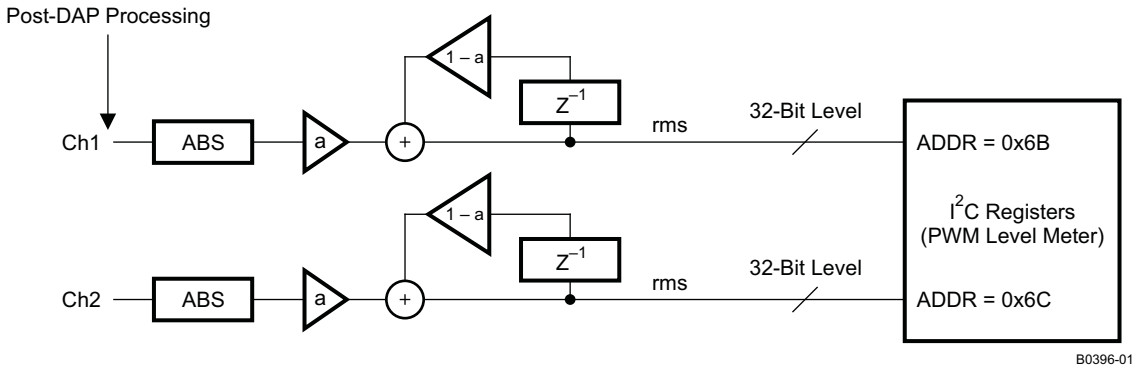


Figure 43. PWM Level Meter Structure

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9.4 Device Functional Modes

9.4.1 Device Protection Mode

The TAS5729MD contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to overcurrent, overtemperature, and undervoltage. Any of these errors are reported in the ERROR STATUS register, and a fault error signal can be monitored on the SPK_FAULT pin if configured in the system control register. If any of the protection circuits is activated, all half-bridge outputs are immediately set in the high-impedance (hi-Z) state.

9.4.2 Speaker Amplifier Mode

The TAS5729MD can be configured in different amplifier configurations:

- Stereo BTL mode
- Monaural PBTL mode

9.4.2.1 Stereo Mode

The classic stereo mode of operation uses the TAS5729MD device to amplify two independent signals that represent the left and right portions of a stereo signal. These amplified left and right audio signals are presented on differential output pairs shown as SPK_OUTA and SPK_OUTB for channel 1 and SPK_OUTC and SPK_OUTD for channel 2. The routing of the audio data that is presented on the SPK_OUTx outputs can be changed according to the PWM Output Mux Register (0x25). By default, the TAS5729MD device is configured to output channel 1 to the SPK_OUTA and SPK_OUTB outputs, and channel 2 to the SPK_OUTC and SPK_OUTD outputs. Stereo mode operation outputs are shown in Figure 44.

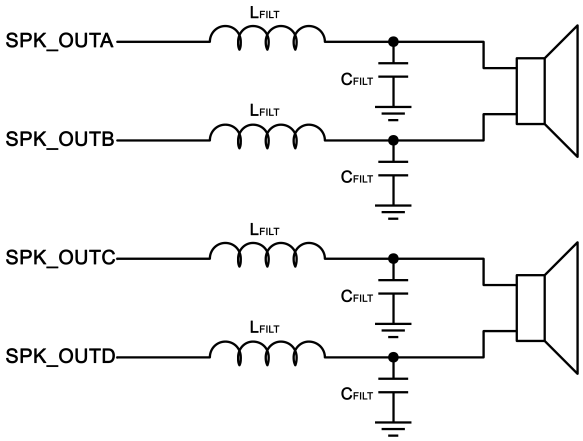

Figure 44. Stereo BTL Mode

9.4.2.2 Monaural Mode

When this mode of operation is used, the two stereo outputs of the device are placed in parallel, one with another to increase the power sourcing capabilities of the device. On the output side of the TAS5729MD device, the merging of the two output channels is done after the inductor portion of the output filter. Doing so requires two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. This process is called post-filter PBTL, and the monaural operation is shown in Figure 45.

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Device Functional Modes (continued)

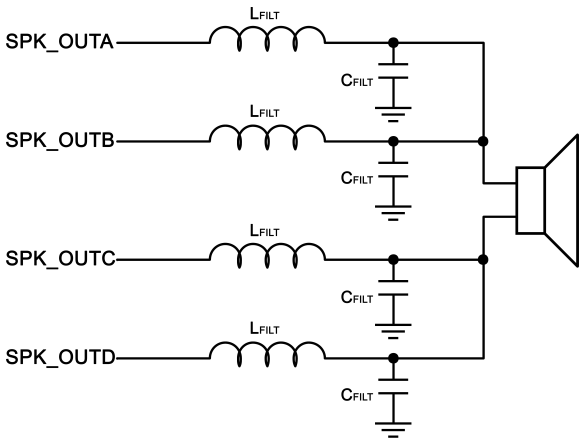

Figure 45. Post-Filter PBTL

On the input side of the TAS5729MD device, the input signal to the monaural amplifier can be selected from a mix, left, or right frame from an I²S, LJ, or RJ signal. The routing of the audio data which is presented on the SPK_OUTx outputs must be configured with the PWM Output Mux Register (0x25).

9.4.3 Headphone/Line Amplifier

An integrated ground centered DirectPath combination headphone amplifier and line driver is integrated in the TAS5729MD. This headphone/line amplifier can be used independently from the device speaker amplifier modes, with analog single-ended inputs DR_INA and DR_INB, linked to the respective analog outputs DR_OUTA, and DR_OUTB. A basic diagram of the headphone/line amplifier is shown in Figure 46.

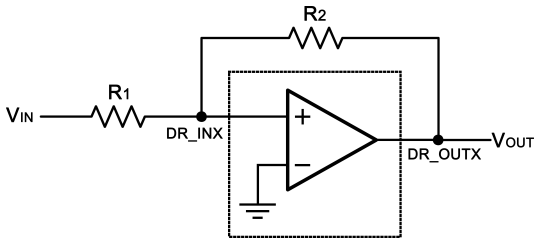

Figure 46. Headphone/Line Amplifier

The $\overline{\text{DR_SDI}}$ pin can be used to turn on or off the headphone amplifier and line driver. The DirectPath amplifier makes use of the provided positive and negative supply rails generated by the IC. The output voltages are centered at zero volts with the capability to swing to the positive rail or negative rail; combining this capability with the built-in click and pop reduction circuit, the DirectPath amplifier requires no output dc blocking capacitors.

9.5 Programming

9.5.1 I²C Serial Control Interface

The TAS5729MD DAP has a bidirectional I²C interface that is compatible with the I²C bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. The DAP is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

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Programming (continued)

9.5.1.1 General I²C Operation

The I²C bus employs two signals: SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit.

Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 47.

The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5729MD holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

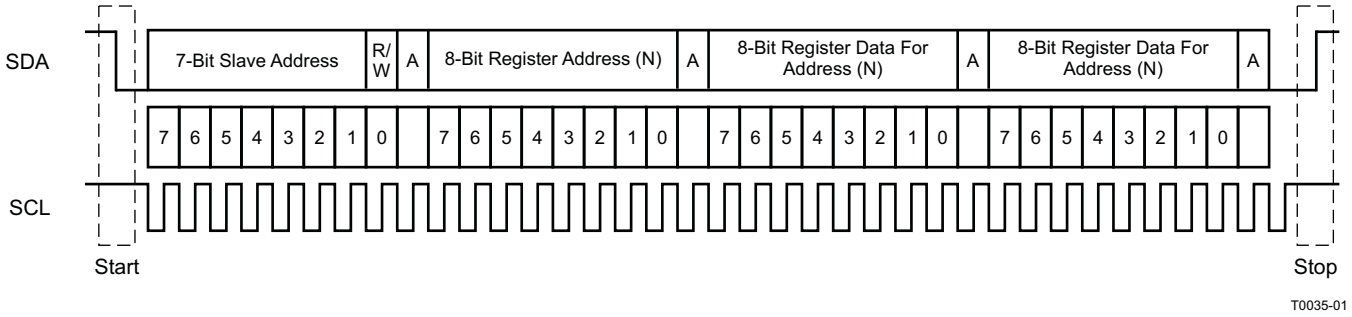

Figure 47. Typical I²C Sequence

An unlimited number of bytes can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 47.

9.5.1.2 Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5729MD also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5729MD. For I²C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

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Programming (continued)

9.5.1.3 Single-Byte Write

As shown in Figure 48, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is 0. After receiving the correct I^2C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5729MD internal memory address being accessed. After receiving the address byte, the TAS5729MD again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5729MD again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

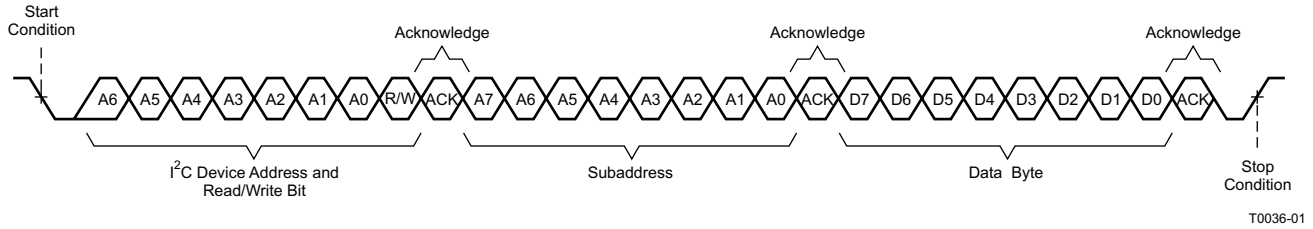

Figure 48. Single-Byte Write Transfer

9.5.1.4 Multiple-Byte Write

A multiple-byte data-write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 49. After receiving each data byte, the TAS5729MD responds with an acknowledge bit.

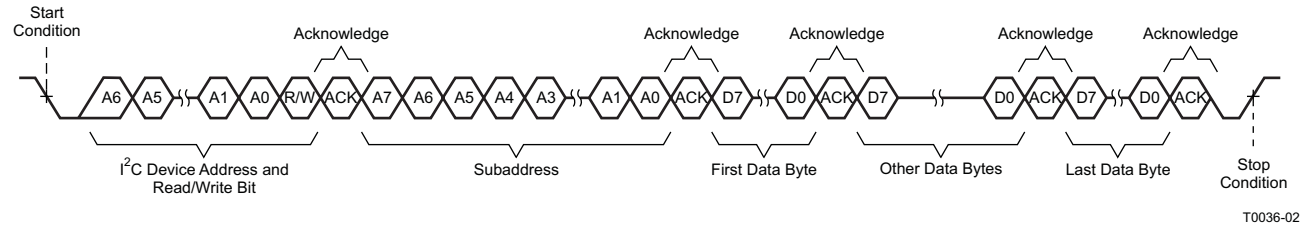

Figure 49. Multiple-Byte Write Transfer

9.5.1.5 Single-Byte Read

As shown in Figure 50, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5729MD address and the read/write bit, TAS5729MD responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5729MD address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5729MD again responds with an acknowledge bit. Next, the TAS5729MD transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

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Programming (continued)

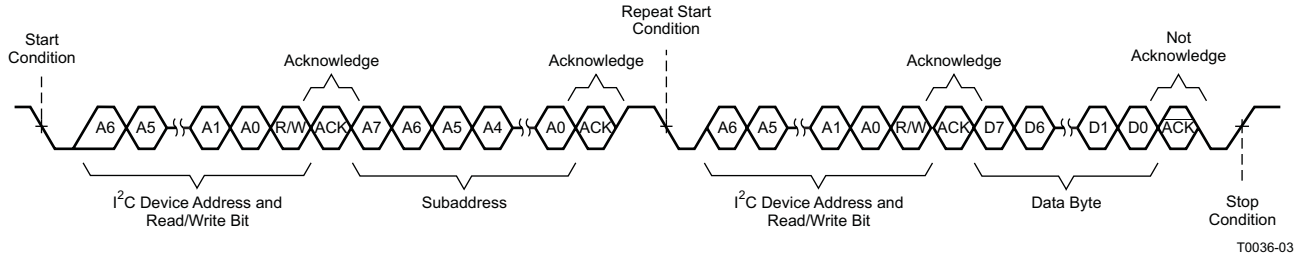

Figure 50. Single-Byte Read Transfer

9.5.1.6 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS5729MD to the master device as shown in Figure 51. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

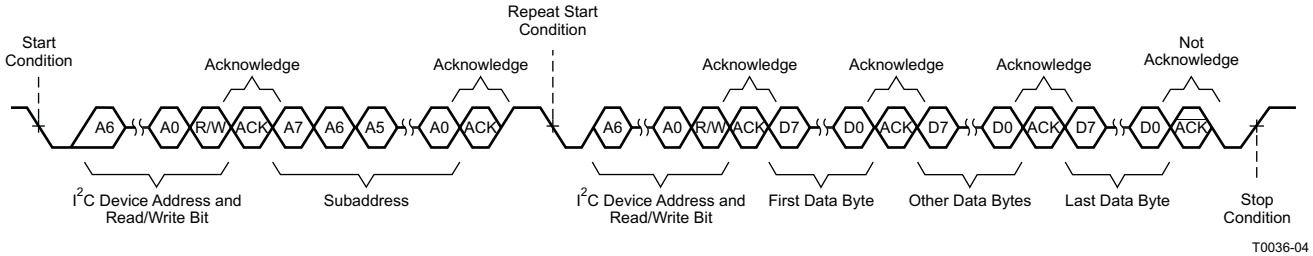

Figure 51. Multiple-Byte Read Transfer

9.5.2 26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. A number formatted as a 3.23 number means that the binary point has three bits to the left and 23 bits to the right. This configuration is shown in Figure 52.

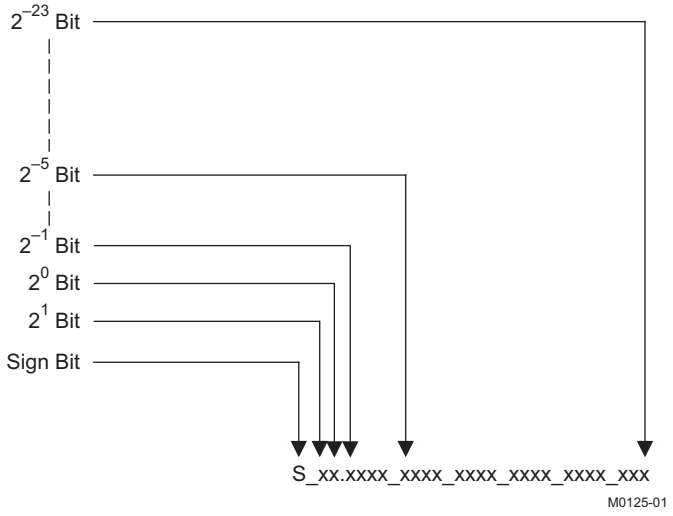

Figure 52. 3.23 Format

Programming (continued)

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 52. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 53 applied to obtain the magnitude of the negative number.

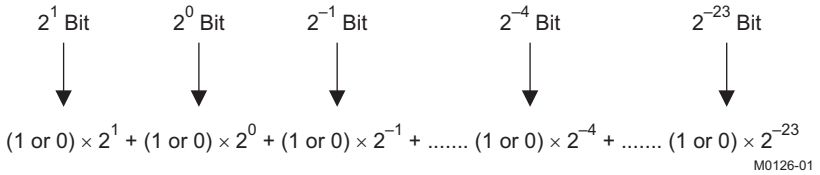

Figure 53. Conversion Weighting Factors—3.23 Format to Floating Point

Gain coefficients, entered via the I^2C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 54.

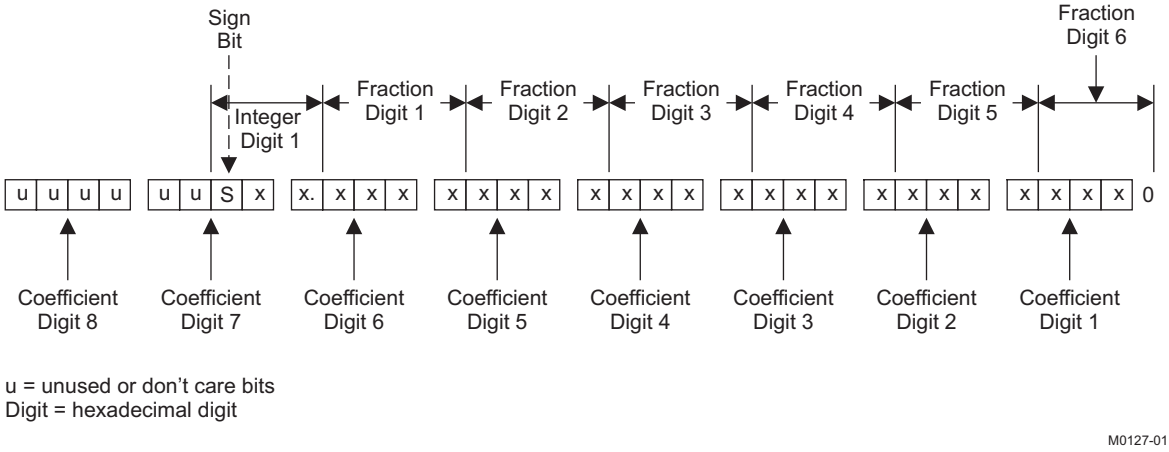

Figure 54. Alignment of 3.23 Coefficient in 32-Bit I^2C Word

Table 2. Sample Calculation for 3.23 Format

dB	LINEAR	DECIMAL	HEX (3.23 FORMAT)
0	1	8,388,608	80 0000
5	1.77	14,917,288	00E3 9EA8
–5	0.56	4,717,260	0047 FACC
X	$L = 10^{(X/20)}$	D = 8388608 × L	H = dec2hex (D, 8)

Table 3. Sample Calculation for 9.17 Format

dB	LINEAR	DECIMAL	HEX (9.17 FORMAT)
0	1	131,072	20 000
5	1.77	231,997	38 A3D
–5	0.56	73,400	11 EB8
X	$L = 10^{(X/20)}$	D = 131,072 × L	H = dec2hex (D, 8)

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9.6 Register Maps

Table 4. Serial Control Interface Register Summary

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
			A u indicates unused bits.	
0x00	Clock control register	1	Description shown in subsequent section	0x6C
0x01	Device ID register	1	Description shown in subsequent section	0xC1
0x02	Error status register	1	Description shown in subsequent section	0x00
0x03	System control register 1	1	Description shown in subsequent section	0xA0
0x04	Serial data interface register	1	Description shown in subsequent section	0x05
0x05	System control register 2	1	Description shown in subsequent section	0x40
0x06	Soft mute register	1	Description shown in subsequent section	0x00
0x07	Master volume	2	Description shown in subsequent section	0x03FF (mute)
0x08	Channel 1 vol	2	Description shown in subsequent section	0x00C0 (0 dB)
0x09	Channel 2 vol	2	Description shown in subsequent section	0x00C0 (0 dB)
0x0A	Channel 3 vol	2	Description shown in subsequent section	0x00C0 (0 dB)
0x0B–0x0D		1	Reserved(1)	
0x0E	Volume configuration register	1	Description shown in subsequent section	0xF0
0x0F		1	Reserved(1)	
0x10	Modulation limit register	1	Description shown in subsequent section	0x01
0x11	IC delay channel 1	1	Description shown in subsequent section	0xAC
0x12	IC delay channel 2	1	Description shown in subsequent section	0x54
0x13	IC delay channel 3	1	Description shown in subsequent section	0xAC
0x14	IC delay channel 4	1	Description shown in subsequent section	0x54
0x15–0x18		1	Reserved(1)	
0x19	PWM Shutdown Group Register	1	Description shown in subsequent section	0x30
0x1A	Start/stop period register	1		0x68
0x1B	Oscillator trim register	1		0x82
0x1C	BKND_ERR register	1		0x57
0x1D–0x1F		1	Reserved(1)	
0x20	Input MUX register	4	Description shown in subsequent section	0x0001 7772
0x21	Ch 4 source select register	4	Description shown in subsequent section	0x0000 4303
0x22–0x24		4	Reserved(1)	
0x25	PWM MUX register	4	Description shown in subsequent section	0x0102 1345
0x26	ch1_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x27	ch1_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

(1) Reserved registers should not be accessed.

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Register Maps (continued)

Table 4. Serial Control Interface Register Summary (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x28	ch1_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x29	ch1_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2A	ch1_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2B	ch1_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2C	ch1_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2D	ch1_bq[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2E	ch1_bq[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x2F	ch1_bq[9]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x30	ch2_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

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Register Maps (continued)

Table 4. Serial Control Interface Register Summary (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x31	ch2_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x32	ch2_bq[2]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x33	ch2_bq[3]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x34	ch2_bq[4]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x35	ch2_bq[5]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x36	ch2_bq[6]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x37	ch2_bq[7]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x38	ch2_bq[8]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x39	ch2_bq[9]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

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Register Maps (continued)

Table 4. Serial Control Interface Register Summary (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x3A		4	Reserved(1)	
0x3B	AGL1 softening filter alpha	8	u[31:26], ae[25:0]	0x0008 0000
	AGL1 softening filter omega		u[31:26], oe[25:0]	0x0078 0000
0x3C	AGL1 attack rate	8		0x0000 0100
	AGL1 release rate			0xFFFF FF00
0x3D		8	Reserved(1)	
0x3E	AGL2 softening filter alpha	8	u[31:26], ae[25:0]	0x0008 0000
	AGL2 softening filter omega		u[31:26], oe[25:0]	0x0078 0000
0x3F	AGL2 attack rate	8	u[31:26], at[25:0]	0x0008 0000
	AGL2 release rate		u[31:26], rt[25:0]	0xFFF8 0000
0x40	AGL1 attack threshold	4	T1[31:0] (9.23 format)	0x0800 0000
0x41–0x42		4	Reserved(1)	
0x43	AGL2 attack threshold	4	T2[31:0] (9.23 format)	0x0074 0000
0x44–0x45		4	Reserved(1)	
0x46	AGL control	4	Description shown in subsequent section	0x0002 0000
0x47–0x4E		4	Reserved(1)	
0x4F	PWM switching rate control	4	u[31:4], src[3:0]	0x0000 0008
0x50	EQ control	4	Description shown in subsequent section	0x0F70 8000
0x51	Ch 1 output mixer	8	Ch 1 output mix1[1]	0x0080 0000
			Ch 1 output mix1[0]	0x0000 0000
0x52	Ch 2 output mixer	8	Ch 2 output mix2[1]	0x0080 0000
			Ch 2 output mix2[0]	0x0000 0000
0x53		16	Reserved(1)	
0x54		16	Reserved(1)	
0x56	Output post-scale	4	u[31:26], post[25:0]	0x0080 0000
0x57	Output pre-scale	4	u[31:26], pre[25:0] (9.17 format)	0x0002 0000
0x58	ch1_bq[10]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x59	ch1_bq[11]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5A	ch4_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000

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Register Maps (continued)

Table 4. Serial Control Interface Register Summary (continued)

SUBADDRESS	REGISTER NAME	NO. OF BYTES	CONTENTS	DEFAULT VALUE
0x5B	ch4_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5C	ch2_bq[10]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5D	ch2_bq[11]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5E	ch3_bq[0]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x5F	ch3_bq[1]	20	u[31:26], b0[25:0]	0x0080 0000
			u[31:26], b1[25:0]	0x0000 0000
			u[31:26], b2[25:0]	0x0000 0000
			u[31:26], a1[25:0]	0x0000 0000
			u[31:26], a2[25:0]	0x0000 0000
0x60–0x61		4	Reserved (1)	
0x62	IDF post scale	4		0x0000 0080
0x63–0x6A			Reserved (1)	
0x6B	Left channel PWM level meter	4	Data[31:0]	0x0000 0000
0x6C	Right channel PWM level meter	4	Data[31:0]	0x0000 0000
0x6D–0x6F			Reserved (1)	
0x70	ch1 inline mixer	4	u[31:26], in_mix1[25:0]	0x0080 0000
0x71	inline_AGL_en_mixer_ch1	4	u[31:26], in_mixAGL_1[25:0]	0x0000 0000
0x72	ch1 right_channel mixer	4	u[31:26], right_mix1[25:0]	0x0000 0000
0x73	ch1 left_channel_mixer	4	u[31:26], left_mix_1[25:0]	0x0080 0000
0x74	ch2 inline mixer	4	u[31:26], in_mix2[25:0]	0x0080 0000
0x75	inline_AGL_en_mixer_ch2	4	u[31:26], in_mixAGL_2[25:0]	0x0000 0000
0x76	ch2 left_chanel mixer	4	u[31:26], left_mix1[25:0]	0x0000 0000
0x77	ch2 right_channel_mixer	4	u[31:26], right_mix_1[25:0]	0x0080 0000
0x78–0xF7			Reserved (1)	
0xF8	Update dev address key	4	Dev Id Update Key[31:0] (Key = 0xF9A5A5A5)	0x0000 0000
0xF9	Update dev address reg	4	u[31:8],New Dev Id[7:0] (New Dev Id = 0x38 for TAS5729MD)	0x0000 0056
0xFA–0xFF		4	Reserved (1)	

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All DAP coefficients are 3.23 format unless specified otherwise.

Registers 0x3B through 0x46 should be altered only during the initialization phase.

9.6.1 Clock Control Register (0x00)

The clocks and data rates are automatically determined by the TAS5729MD. The clock control register contains the autodetected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency.

Table 5. Clock Control Register (0x00)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–	–	–	f_S = 32-kHz sample rate
0	0	1	–	–	–	–	–	Reserved
0	1	0	–	–	–	–	–	Reserved
0	**1**	**1**	**–**	**–**	**–**	**–**	**–**	**f_S = 44.1- or 48-kHz sample rate**(1)
1	0	0	–	–	–	–	–	f_S = 16-kHz sample rate
1	0	1	–	–	–	–	–	f_S = 22.05- or 24-kHz sample rate
1	1	0	–	–	–	–	–	f_S = 8-kHz sample rate
1	1	1	–	–	–	–	–	f_S = 11.025- or 12-kHz sample rate
–	–	–	0	0	0	–	–	MCLK frequency = 64 × f_S(2)
–	–	–	0	0	1	–	–	MCLK frequency = 128 × f_S(2)
–	–	–	0	1	0	–	–	MCLK frequency = 192 × f_S(3)
–	**–**	**–**	**0**	**1**	**1**	**–**	**–**	**MCLK frequency = 256 × f_S** (1)(4)
–	–	–	1	0	0	–	–	MCLK frequency = 384 × f_S
–	–	–	1	0	1	–	–	MCLK frequency = 512 × f_S
–	–	–	1	1	0	–	–	Reserved
–	–	–	1	1	1	–	–	Reserved
–	–	–	–	–	–	**0**	–	**Reserved**(1)
–	**–**	**–**	–	**–**	**–**	**–**	**0**	**Reserved**(1)

(1) Default values are in **bold**.
(2) Only available for 44.1-kHz and 48-kHz rates
(3) Rate only available for 32-, 44.1-, and 48-kHz sample rates
(4) Not available at 8 kHz

9.6.2 Device ID Register (0x01)

The device ID register contains the ID code for the firmware revision.

Table 6. General Status Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	**1**	0	0	0	0	0	**1**	**Identification code**(1)

(1) Default values are in **bold**.

9.6.3 Error Status Register (0x02)

The error bits are sticky and are not cleared by the hardware, which means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error definitions:

- MCLK error: MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK error: The number of SCLKs per LRCLK is changing.
- LRCLK error: LRCLK frequency is changing.
- Frame slip: LRCLK phase is drifting with respect to internal frame sync.

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Table 7. Error Status Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	MCLK error
–	1	–	–	–	–	–	–	PLL autolock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip
–	–	–	–	–	1	–	–	Clip indicator
–	–	–	–	–	–	1	–	Overcurrent, overtemperature, overvoltage, or undervoltage error
0	0	0	0	0	0	0	0	Reserved
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**No errors** (1)

(1) Default values are in **bold**.

9.6.4 System Control Register 1 (0x03)

System control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.
If 1, the dc-blocking filter (–3 dB cutoff < 1 Hz) for each channel is enabled.

Bit D5: If 0, use soft unmute on recovery from a clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E.
If 1, use hard unmute on recovery from clock error. This is fast recovery, single-step volume ramp.

Bits D1–D0: Select de-emphasis

Table 8. System Control Register 1 (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	PWM high-pass (dc blocking) disabled
1	–	–	–	–	–	–	–	**PWM high-pass (dc blocking) enabled** (1)
–	**0**	–	–	–	–	–	–	**Reserved**(1)
–	–	**0**	–	–	–	–	–	**Soft unmute on recovery from clock error or exit all channel shutdown.**(1)
–	–	1	–	–	–	–	–	Hard unmute on recovery from clock error or exit all channel shutdown.
–	–	–	**0**	–	–	–	–	**Reserved**(1)
–	–	–	–	**0**	–	–	–	**Reserved**(1)
–	–	–	–	–	**0**	–	–	**Reserved**(1)
–	–	–	–	–	–	**0**	**0**	**No de-emphasis**(1)
–	–	–	–	–	–	0	1	De-emphasis for f_S = 32 kHz
–	–	–	–	–	–	1	0	De-emphasis for f_S = 44.1 kHz
–	–	–	–	–	–	1	1	De-emphasis for f_S = 48 kHz

(1) Default values are in **bold**.

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9.6.5 Serial Data Interface Register (0x04)

As shown in Table 9, the TAS5729MD supports nine serial data modes. The default is 24-bit, I^2S mode.

Table 9. Serial Data Interface Control Register (0x04) Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTH	D7–D4	D3	D2	D1	D0
Right-justified	16	0000	0	0	0	0
Right-justified	20	0000	0	0	0	1
Right-justified	24	0000	0	0	1	0
I^2S	16	0000	0	0	1	1
I^2S	20	0000	0	1	0	0
I^2S(1)	**24**	**0000**	**0**	**1**	**0**	**1**
Left-justified	16	0000	0	1	1	0
Left-justified	20	0000	0	1	1	1
Left-justified	24	0000	1	0	0	0
Reserved		0000	1	0	0	1
Reserved		0000	1	0	1	0
Reserved		0000	1	0	1	1
Reserved		0000	1	1	0	0
Reserved		0000	1	1	0	1
Reserved		0000	1	1	1	0
Reserved		0000	1	1	1	1

(1) Default values are in **bold**.

9.6.6 System Control Register 2 (0x05)

When bit D6 is set low, the system exits all-channel shutdown and starts playing audio; otherwise, the outputs are shutdown (hard mute).

Table 10. System Control Register 2 (0x05)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	**–**	**–**	**–**	**–**	**–**	–	**Reserved**(1)
–	0	–	–	–	–	–	–	Exit all-channel shutdown (normal operation)(2)
–	**1**	–	–	–	–	–	–	**Enter all-channel shutdown (hard mute)**(1)
–	–	**0**	**–-**	**–**	**–**	**–**	–	**Reserved** (1)
–	–	–	**0**	**–**	**–**	**–**	**–**	**Reserved** (1)
–	–	–	–	1	–	–	**–**	In speaker mode, a value of 1 means device is in ternary modulation.
–	–	–	–	**0**	–	–	**–**	**In speaker mode, a value of 0 means device is in not in ternary modulation (AD or BD as defined in register 0x25).** (1)
–	–	–	–	–	**0**	–	–	**Reserved** (1)
–	–	–	–	–	–	**0**	–	ADR/$\overline{\text{SPK_FAULT}}$ configured as input for address select.
–	–	–	–	–	–	1	–	ADR/$\overline{\text{SPK_FAULT}}$ configured as output for $\overline{\text{SPK_FAULT}}$
.–	–	–	–	–	–	–	**0**	**Reserved**(1)

(1) Default values are in **bold**.
(2) When exiting all-channel shutdown, a soft or hard unmute is determined by register 0x03, bit 5.

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9.6.7 Soft Mute Register (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

Table 11. Soft Mute Register (0x06)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	–	–	–	**Reserved**(1)
–	–	–	–	–	1	–	–	Soft mute channel 3
–	–	–	–	–	**0**	–	–	**Soft unmute channel 3**(1)
–	–	–	–	–	–	1	–	Soft mute channel 2
–	–	–	–	–	–	**0**	–	**Soft unmute channel 2**(1)
–	–	–	–	–	–	–	1	Soft mute channel 1
–	–	–	–	–	–	–	**0**	**Soft unmute channel 1**(1)

(1) Default values are in **bold**.

9.6.8 Volume Registers (0x07, 0x08, 0x09)

Step size is 0.125 dB and volume registers are 2 bytes.

Master volume:	0x07 (default is mute)
Channel-1 volume:	0x08 (default is 0 dB)
Channel-2 volume:	0x09 (default is 0 dB)

Volume Range: +24dB to –103.75dB

Step-Size: 0.125dB

Formula:

Target Volume Level (dB) = 'V'

- Step-1: Calculate (24 – V)/0.125
- Step-2: Convert calculated decimal value to 2-byte hexadecimal to get the register hex-value

Examples:

Target Volume = 12dB

- (24 – 12)/0.125 = 96
- Converting decimal value 96 to 2-byte hexadecimal gives x0060

Target Volume = 0dB

- (24 – 0)/0.125 = 192
- Converting decimal value 192 to 2-byte hexadecimal gives x00C0

Target Volume = –12dB

- (24 – (–12))/0.125 = 36/0.125 = 288
- Converting decimal value 288 to 2-byte hexadecimal gives x0120

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9.6.9 Volume Configuration Register (0x0E)

Bits D2–D0: Volume slew rate (used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I^2S data as follows:

Sample rate (kHz)	Approximate ramp rate
8, 16, or 32	125 µs/step
11.025, 22.05, or 44.1	90.7 µs/step
12, 24, or 48	83.3 µs/step

Table 12. Volume Configuration Register (0x0E)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	1	1	**1**	**0**	–	–	–	**Reserved**(1)
–	–	–	–	–	**0**	**0**	**0**	**Volume slew 512 steps (43-ms volume ramp time at 48 kHz)**(1)
–	–	–	–	–	0	0	1	Volume slew 1024 steps (85-ms volume ramp time at 48 kHz)
–	–	–	–	–	0	1	0	Volume slew 2048 steps (171-ms volume ramp time at 48 kHz)
–	–	–	–	–	0	1	1	Volume slew 256 steps (21-ms volume ramp time at 48 kHz)
–	–	–	–	–	1	X	X	Reserved

(1) Default values are in **bold**.

9.6.10 Modulation Limit Register (0x10)

Table 13. Modulation Limit Register (0x10)

D7	D6	D5	D4	D3	D2	D1	D0	MODULATION LIMIT
0	0	0	0	0	–	–	–	Reserved
–	–	–	–	–	0	0	0	99.2%
–	–	–	–	–	**0**	**0**	**1**	**98.4%** (1)
–	–	–	–	–	0	1	0	97.7%
–	–	–	–	–	0	1	1	96.9%
–	–	–	–	–	1	0	0	96.1%
–	–	–	–	–	1	0	1	95.3%
–	–	–	–	–	1	1	0	94.5%
–	–	–	–	–	1	1	1	93.8%

(1) Default values are in **bold**.

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9.6.11 Interchannel Delay Registers (0x11, 0x12, 0x13, and 0x14)

Internal PWM channels 1, 2, $\overline{1}$, and $\overline{2}$ are mapped into registers 0x11, 0x12, 0x13, and 0x14.

Table 14. Channel Interchannel Delay Register Format

BITS DEFINITION	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	–	–	Minimum absolute delay, 0 DCLK cycles
	0	1	1	1	1	1	–	–	Maximum positive delay, 31 × 4 DCLK cycles
	1	0	0	0	0	0	–	–	Maximum negative delay, –32 × 4 DCLK cycles
							0	0	Reserved
SUBADDRESS	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Delay = (value) × 4 DCLKs**
0x11	**1**	**0**	**1**	**0**	**1**	**1**	–	–	**Default value for channel 1**(1)
0x12	**0**	**1**	**0**	**1**	**0**	**1**	–	–	**Default value for channel 2**(1)
0x13	**1**	**0**	**1**	**0**	**1**	**1**	–	–	**Default value for $\overline{\text{channel 1}}$**(1)
0x14	**0**	**1**	**0**	**1**	**0**	**1**	–	–	**Default value for $\overline{\text{channel 2}}$**(1)

(1) Default values are in **bold**.

ICD settings have high impact on audio performance (for example, dynamic range, THD, crosstalk, and so on). Therefore, appropriate ICD settings must be used. By default, the device has ICD settings for the AD mode. If used in BD mode, then update these registers before coming out of all-channel shutdown.

MODE	AD MODE	BD MODE
0x11	AC	B8
0x12	54	60
0x13	AC	A0
0x14	54	48

9.6.12 PWM Shutdown Group Register (0x19)

Settings of this register determine which PWM channels are active. The value should be 0x30 for BTL mode and 0x3A for post-filter PBTL mode. The default value of this register is 0x30. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

Table 15. PWM Shutdown Group Register (0x19)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–	–	**Reserved**(1)
–	**0**	–	–	–	–	–	–	**Reserved**(1)
–	–	**1**	–	–	–	–	–	**Reserved**(1)
–	–	–	**1**	–	–	–	–	**Reserved**(1)
–	–	–	–	**0**	–	–	–	**PWM channel 4 does not belong to shutdown group.**(1)
–	–	–	–	1	–	–	–	PWM channel 4 belongs to shutdown group.
–	–	–	–	–	**0**	–	–	**PWM channel 3 does not belong to shutdown group.**(1)
–	–	–	–	–	1	–	–	PWM channel 3 belongs to shutdown group.
–	–	–	–	–	–	**0**	–	**PWM channel 2 does not belong to shutdown group.**(1)
–	–	–	–	–	–	1	–	PWM channel 2 belongs to shutdown group.
–	–	–	–	–	–	–	**0**	**PWM channel 1 does not belong to shutdown group.**(1)
–	–	–	–	–	–	–	1	PWM channel 1 belongs to shutdown group.

(1) Default values are in **bold**.

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9.6.13 Start/Stop Period Register (0x1A)

This register is used to control the soft-start and soft-stop period following an enter or exit all-channel shutdown command or change in the $\overline{PDN}$ state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I^2S clock stability.

Table 16. Start/Stop Period Register (0x1A)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**–**	**–**	–	–	–	–	–	**SSTIMER enabled**(1)
1	–	–	–	–	–	–	–	SSTIMER disabled
–	**1**	**1**	–	–	–	–	–	**Reserved**(1)
–	–	–	0	0	–	–	–	No 50% duty cycle start/stop period
–	–	–	**0**	**1**	**0**	**0**	**0**	**16.5-ms 50% duty cycle start/stop period**(1)
–	–	–	0	1	0	0	1	23.9-ms 50% duty cycle start/stop period
–	–	–	0	1	0	1	0	31.4-ms 50% duty cycle start/stop period
–	–	–	0	1	0	1	1	40.4-ms 50% duty cycle start/stop period
–	–	–	0	1	1	0	0	53.9-ms 50% duty cycle start/stop period
–	–	–	0	1	1	0	1	70.3-ms 50% duty cycle start/stop period
–	–	–	0	1	1	1	0	94.2-ms 50% duty cycle start/stop period
–	–	–	0	1	1	1	1	125.7-ms 50% duty cycle start/stop period
–	–	–	1	0	0	0	0	164.6-ms 50% duty cycle start/stop period
–	–	–	1	0	0	0	1	239.4-ms 50% duty cycle start/stop period
–	–	–	1	0	0	1	0	314.2-ms 50% duty cycle start/stop period
–	–	–	1	0	0	1	1	403.9-ms 50% duty cycle start/stop period
–	–	–	1	0	1	0	0	538.6-ms 50% duty cycle start/stop period
–	–	–	1	0	1	0	1	703.1-ms 50% duty cycle start/stop period
–	–	–	1	0	1	1	0	942.5-ms 50% duty cycle start/stop period
–	–	–	1	0	1	1	1	1256.6-ms 50% duty cycle start/stop period
–	–	–	1	1	0	0	0	1728.1-ms 50% duty cycle start/stop period
–	–	–	1	1	0	0	1	2513.6-ms 50% duty cycle start/stop period
–	–	–	1	1	0	1	0	3299.1-ms 50% duty cycle start/stop period
–	–	–	1	1	0	1	1	4241.7-ms 50% duty cycle start/stop period
–	–	–	1	1	1	0	0	5655.6-ms 50% duty cycle start/stop period
–	–	–	1	1	1	0	1	7383.7-ms 50% duty cycle start/stop period
–	–	–	1	1	1	1	0	9897.3-ms 50% duty cycle start/stop period
–	–	–	1	1	1	1	1	13,196.4-ms 50% duty cycle start/stop period

(1) Default values are in **bold**.

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9.6.14 Oscillator Trim Register (0x1B)

The TAS5729MD PWM processor contains an internal oscillator to support autodetect of the I^2S clock rates. This reduces system cost because an external reference is not required. Currently, TI recommends a reference resistor value of 18.2 kΩ (1%). This should be connected between OSC_RES and DVSSO.

Writing 0x00 to register 0x1B enables the trim that was programmed at the factory.

Note that trim must always be run following reset of the device.

Table 17. Oscillator Trim Register (0x1B)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	**Reserved**(1)
–	**0**	–	–	–	–	–	–	**Oscillator trim not done (read-only)**(1)
–	1	–	–	–	–	–	–	Oscillator trim done (read only)
–	–	**0**	**0**	**0**	**0**	–	–	**Reserved**(1)
–	–	–	–	–	–	0	–	Select factory trim (Write a 0 to select factory trim; default is 1.)
–	–	–	–	–	–	**1**	–	**Factory trim disabled**(1)
–	–	–	–	–	–	–	**0**	**Reserved**(1)

(1) Default values are in **bold**.

9.6.15 BKND_ERR Register (0x1C)

When a back-end error signal is received from the internal power stage, the power stage is reset, stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in Table 18 before attempting to re-start the power stage.

Table 18. BKND_ERR Register (0x1C)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**1**	**0**	**1**	–	–	–	–	**Reserved**(1)
–	–	–	–	0	0	1	0	Set back-end reset period to 299 ms
–	–	–	–	0	0	1	1	Set back-end reset period to 449 ms
–	–	–	–	0	1	0	0	Set back-end reset period to 598 ms
–	–	–	–	0	1	0	1	Set back-end reset period to 748 ms
–	–	–	–	0	1	1	0	Set back-end reset period to 898 ms
–	–	–	–	**0**	**1**	**1**	**1**	**Set back-end reset period to 1047 ms**(1)
–	–	–	–	1	0	0	0	Set back-end reset period to 1197 ms
–	–	–	–	1	0	0	1	Set back-end reset period to 1346 ms
–	–	–	–	1	0	1	X	Set back-end reset period to 1496 ms
–	–	–	–	1	1	X	X	Set back-end reset period to 1496 ms

(1) Default values are in **bold**.

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9.6.16 Input Multiplexer Register (0x20)

This register controls the modulation scheme (AD or BD mode) as well as the routing of I^2S audio to the internal channels.

Table 19. Input Multiplexer Register (0x20)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	–	–	–	–	–	–	–	**Channel-1 AD mode**(1)
1	–	–	–	–	–	–	–	Channel-1 BD mode
–	**0**	**0**	**0**	–	–	–	–	**SDIN-L to channel 1**(1)
–	0	0	1	–	–	–	–	SDIN-R to channel 1
–	0	1	0	–	–	–	–	Reserved
–	0	1	1	–	–	–	–	Reserved
–	1	0	0	–	–	–	–	Reserved
–	1	0	1	–	–	–	–	Reserved
–	1	1	0	–	–	–	–	Ground (0) to channel 1
–	1	1	1	–	–	–	–	Reserved
–	–	–	–	**0**	–	–	–	**Channel 2 AD mode**(1)
–	–	–	–	1	–	–	–	Channel 2 BD mode
–	–	–	–	–	0	0	0	SDIN-L to channel 2
–	–	–	–	–	**0**	**0**	**1**	**SDIN-R to channel 2**(1)
–	–	–	–	–	0	1	0	Reserved
–	–	–	–	–	0	1	1	Reserved
–	–	–	–	–	1	0	0	Reserved
–	–	–	–	–	1	0	1	Reserved
–	–	–	–	–	1	1	0	Ground (0) to channel 2
–	–	–	–	–	1	1	1	Reserved
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**Reserved**(1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**Reserved**(1)

(1) Default values are in **bold**.

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9.6.17 Channel 4 Source Select Register (0x21)

This register selects the channel 4 source.

Table 20. Subchannel Control Register (0x21)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**1**	**0**	**0**	**0**	**0**	**1**	**–**	**Reserved**(1)
–	–	–	–	–	–	**–**	0	(L + R) / 2
–	–	–	–	–	–	–	**1**	**Left-channel post-BQ**(1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Reserved**(1)

(1) Default values are in **bold**.

9.6.18 PWM Output MUX Register (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20: Selects which PWM channel is output to OUT_A
Bits D17–D16: Selects which PWM channel is output to OUT_B
Bits D13–D12: Selects which PWM channel is output to OUT_C
Bits D09–D08: Selects which PWM channel is output to OUT_D

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 4 = 0x03.

Table 21. PWM Output Mux Register (0x25)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	–	–	–	–	–	–	**Reserved**(1)
–	**–**	**0**	**0**	–	–	–	–	**Multiplex channel 1 to OUT_A**(1)
–	–	0	1	–	–	–	–	Multiplex channel 2 to OUT_A
–	–	1	0	–	–	–	–	Multiplex $\overline{\text{channel 1}}$ to OUT_A
–	–	1	1	–	–	–	–	Multiplex $\overline{\text{channel 2}}$ to OUT_A
–	–	–	–	**0**	**0**	–	–	**Reserved**(1)
–	–	–	–	–	–	0	0	Multiplex channel 1 to OUT_B
–	–	–	–	–	–	0	1	Multiplex channel 2 to OUT_B
–	–	–	–	–	–	**1**	**0**	**Multiplex $\overline{\text{channel 1}}$ to OUT_B**(1)
–	–	–	–	–	–	1	1	Multiplex $\overline{\text{channel 2}}$ to OUT_B
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	–	–	–	–	–	–	**Reserved**(1)
–	–	0	0	–	–	–	–	Multiplex channel 1 to OUT_C
–	–	**0**	**1**	–	–	–	–	**Multiplex channel 2 to OUT_C**(1)
–	–	1	0	–	–	–	–	Multiplex $\overline{\text{channel 1}}$ to OUT_C

(1) Default values are in **bold**.

Table 21. PWM Output Mux Register (0x25) (continued)

–	–	1	1	–	–	–	–	Multiplex $\overline{\text{channel 2}}$ to OUT_C
–	–	–	–	**0**	**0**	–	–	**Reserved**(1)
–	–	–	–	–	–	0	0	Multiplex channel 1 to OUT_D
–	–	–	–	–	–	0	1	Multiplex channel 2 to OUT_D
–	–	–	–	–	–	1	0	Multiplex $\overline{\text{channel 1}}$ to OUT_D
–	–	–	–	–	–	**1**	**1**	**Multiplex channel 2 to OUT_D**(1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**Reserved**(1)

9.6.19 AGL Control Register (0x46)

Table 22. AGL Control Register (0x46)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**Reserved**(1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	**0**	**–**	**–**	–	–	–	–	**Reserved**(1)
–	–	0	–	–	–	–	–	Reserved
–	–	1	–	–	–	–	–	Reserved
–	–	–	**0**	–	–	–	–	**Reserved**(1)
–	–	**–**	**–**	**0**	–	–	–	**Reserved**(1)
–	–	–	–	–	**0**	–	–	**Reserved**(1)
–	–	–	–	–	–	**0**	–	**AGL2 turned OFF**(1)
–	–	–	–	–	–	1	–	AGL2 turned ON
–	–	–	–	–	–	–	**0**	**AGL1 turned OFF**(1)
–	–	–	–	–	–	–	1	AGL1 turned ON

(1) Default values are in **bold**.

9.6.20 PWM Switching Rate Control Register (0x4F)

The output PWM switching frequency is configurable as a multiple of the input sample rate (f_S). The PWM frequency can be set to one of 6 × f_S, 7 × f_S, 8 × f_S, or 9 × f_S. PWM switching rate should be selected through the register 0x4F before coming out of all-channel shutdown.

Table 23. PWM Switching Rate Control Register (0x4F)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
–	–	**0**	**0**	–	–	–	–	**Reserved**(1)
–	–	–	–	0	1	1	0	PWM SRC = 6 × f_S

(1) Default values are in **bold**.

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Table 23. PWM Switching Rate Control Register (0x4F) (continued)

–	–	–	–	0	1	1	1	PWM SRC = 7 x f_S
–	–	–	–	**1**	**0**	**0**	**0**	**PWM SRC = 8 × f_S**(1)
–	–	–	–	1	0	0	1	PWM SRC = 9 × f_S
–	–	–	–	1	0	1	0	Reserved
–	–	–	–	1	1	–	–	Reserved

9.6.21 EQ Control (0x50)

Table 24. EQ Command (0x50)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	**1**	**1**	**1**	**1**	**Reserved**(1)
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**1**	**1**	**1**	0	0	0	0	**Reserved**(1)
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**FUNCTION**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Reserved**(1)
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	–	–	–	–	–	–	–	**EQ ON**(1)
1	–	–	–	–	–	–	–	EQ OFF (bypass BQ 0–7 of channels 1 and 2)
–	**0**	–	–	–	–	–	–	**Reserved**(1)
–	–	**0**	–	–	–	–	–	**Reserved**(1)
–	–	1	–	–	–	–	–	**Reserved**(1)
–	–	–	**0**	–	–	–	–	**L and R can be written independently.**(1)
–	–	–	1	–	–	–	–	L and R are ganged for EQ biquads; a write to the left-channel biquad is also written to the right-channel biquad. (0x29–0x2F is ganged to 0x30–0x36. Also, 0x58–0x5B is ganged to 0x5C–0x5F.
–	–	**–**	**–**	**0**	–	–	–	**Reserved**(1)
–	–	–	–	–	**0**	**0**	**0**	**Reserved**(1)
–	–	–	–	–	0	0	1	**Reserved**
–	–	–	–	–	0	1	X	Reserved
–	–	–	–	–	1	X	X	Reserved

(1) Default values are in **bold**.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Applications

These application circuits detail the recommended component selection and board configurations for the TAS5729MD device.

For further information regarding component selection, see *TAS5721xx, TAS5723xx, and TAS5729xx Evaluation Module* (SLOU367).

10.2.1 Stereo BTL Configuration With Headphone and Line Driver Amplifier

A stereo system generally refers to a system in which are two full range speakers without a separate amplifier path for the speakers that reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel.

This configuration also has a DirectPath headphone stereo amplifier which can be used independently from the speaker channels.

The Stereo BTL Configuration with Headphone and Line Driver Amplifier application is shown in Figure 55.

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Typical Applications (continued)

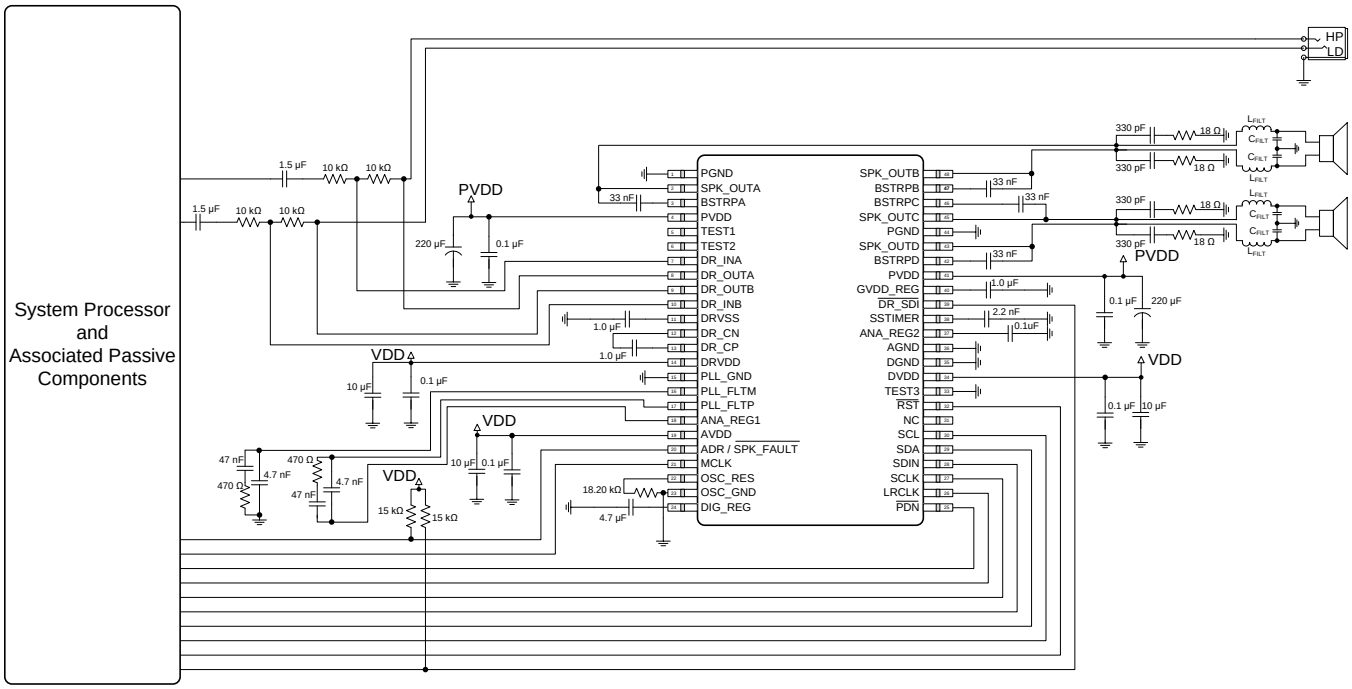

Figure 55. Stereo BTL Configuration With Headphone and Line Driver Amplifier

10.2.1.1 Design Requirements

Power supplies:

- 3.3-V power supply for internal digital, analog, and headphone/line driver circuitry.
- 4.5-V to 25-V power supply for internal power circuitry

Communication:

- System controller with I^2C control interface serving a compliant master

Audio digital input:

- Serial data in 16-, 20-, or 24-bit left-justified, right-justified, or I^2S format

Headphone/line driver input:

- Analog single-ended line input

Output components:

- 2 × 8-Ω speakers (recommended).
- 16-Ω headphones (recommended) / 5-kΩ line driver load

Output filter:

- 4 × 15-µH Inductors
- 4 × 0.33-µF Capacitors

Components required:

- 4 × 10-kΩ Resistor
- 2 × 470-Ω Resistor
- 2 × 15-kΩ Resistor
- 1 × 18.2-kΩ Resistor
- 4 × 18-Ω Resistor
- 2 × 1.5-µF Capacitor
- 4 × 4.7-nF Capacitor

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Typical Applications (continued)

- 3 × 10-µF Capacitor
- 3 × 1-µF Capacitor
- 6 × 0.1-µF Capacitor
- 4 × 33-nF Capacitor
- 2 × 220-µF Capacitor
- 1 × 4.7-µF Capacitor
- 1 × 2.2-µF Capacitor
- 4 × 330-pF Capacitor

10.2.1.2 Detailed Design Procedure

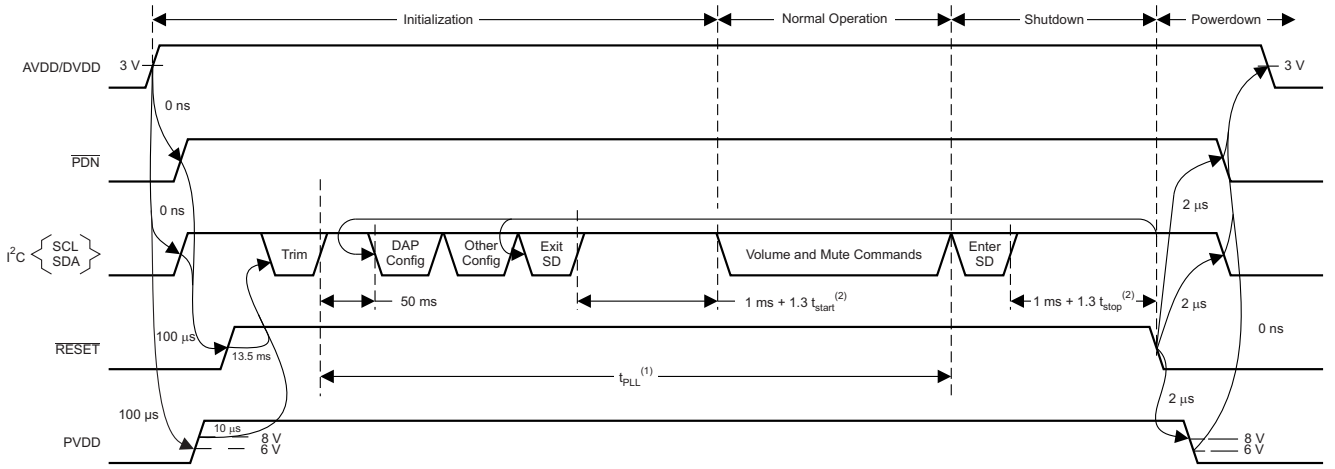
10.2.1.2.1 Hardware Integration

- Using the Typical Application Schematic as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, schematic layout and routing given in the layout example below, integrate the device and its supporting components into the system PCB file.
  - The most critical sections of the circuit are the power supply inputs, the amplifier output signals, and the high-frequency signals which go to the serial audio port. These sections should be constructed to ensure they are given precedent as design trade-offs are made.
  - For questions and support go to the E2E forums (e2e.ti.com). If the user must deviate from the recommended layout, please visit the E2E forum to request a layout review.

10.2.1.2.2 Control and Software Integration

Use TAS5729 EVM and the Purepath Console GUI for device control and configuration. Prior approval is required to download the GUI. Please request access at http://www.ti.com/tool/purepathconsole.

10.2.1.2.3 Recommended Start-Up and Shutdown Procedures



(1) t_{PLL} has to be greater than 240 ms + 1.3 t_{start}.
This constraint only applies to the first trim command following AVDD/DVDD power-up.
It does not apply to trim commands following subsequent resets.
(2) t_{start}/t_{stop} = PWM start/stop time as defined in register 0X1A

T0419-06

Figure 56. Recommended Command Sequence

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Typical Applications (continued)

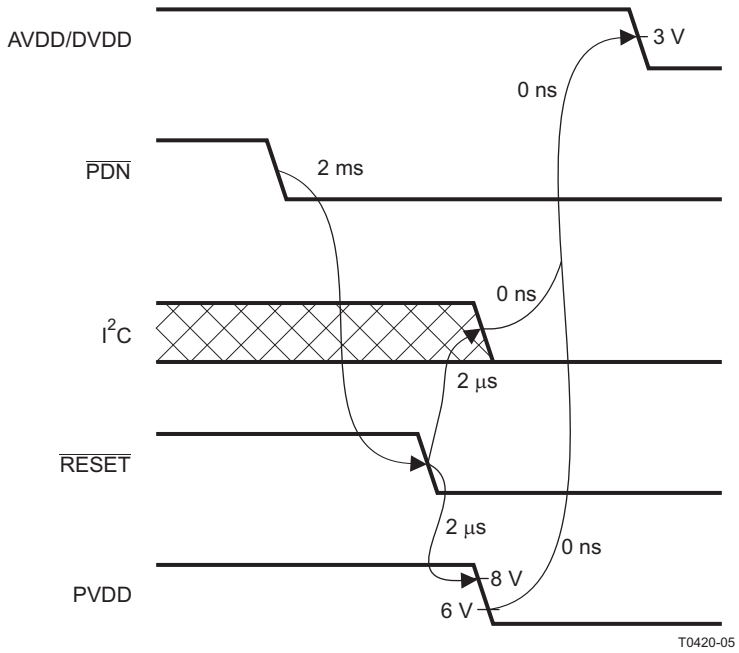

Figure 57. Power-Loss Sequence

10.2.1.2.3.1 Initialization Sequence

Use the following sequence to power up and initialize the TAS5729MD device:

1. Hold all digital inputs low and ramp up AVDD/DVDD to at least 3 V.
2. Initialize digital inputs and PVDD supply as follows:
   - Drive RESET = 0, PDN = 1, and other digital inputs to their desired state while ensuring that all are never more than 2.5 V above AVDD/DVDD. Wait at least 100 µs, drive RESET = 1, and wait at least another 13.5 ms.
   - Ramp up PVDD to at least 8 V while ensuring that it remains below 6 V for at least 100 µs after AVDD/DVDD reaches 3 V. Then wait at least another 10 µs.
3. Trim oscillator (write 0x00 to register 0x1B) and wait at least 50 ms.
4. Configure the DAP via I2C, see the TAS5731EVM Evaluation Module User's Guide (SLOU331) for typical values.
5. Configure remaining registers.
6. Exit shutdown (sequence defined in *Shutdown Sequence*).

10.2.1.2.3.2 Normal Operation

The following are the only events supported during normal operation:

1. Writes to master/channel volume registers
2. Writes to soft-mute register
3. Enter and exit shutdown (sequence defined in *Shutdown Sequence*)

10.2.1.2.3.3 Shutdown Sequence

Enter:

1. Write 0x40 to register 0x05.
2. Wait at least 1 ms + 1.3 × tstop (where tstop is specified by register 0x1A).
3. If desired, reconfigure by returning to step 4 of initialization sequence.

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Typical Applications (continued)

Exit:

1. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240 ms after trim following AVDD/DVDD power-up ramp).
2. Wait at least 1 ms + 1.3 × tstart (where tstart is specified by register 0x1A).
3. Proceed with normal operation.

10.2.1.2.3.4 Power-Down Sequence

Use the following sequence to power down the device and its supplies:

1. If time permits, enter shutdown (sequence defined in *Shutdown Sequence*); else, in case of sudden power loss, assert PDN = 0 and wait at least 2 ms.
2. Assert RESET = 0.
3. Drive digital inputs low and ramp down PVDD supply as follows:
   – Drive all digital inputs low after RESET has been low for at least 2 µs.
   – Ramp down PVDD while ensuring that it remains above 8 V until RESET has been low for at least 2 µs.
4. Ramp down AVDD/DVDD while ensuring that it remains above 3 V until PVDD is below 6 V and that it is never more than 2.5 V below the digital inputs.

10.2.1.3 Application Curves for Stereo BTL Configuration with Headphone and Line Driver Amplifier

Table 25. Stereo BTL Configuration with Headphone and Line Driver Amplifier Application Curves

PLOT TITLE	FIGURE
Output Power vs PVDD	Figure 3
THD+N vs Frequency, V_{PVDD} = 12 V	Figure 5
THD+N vs Frequency, V_{PVDD} = 18 V	Figure 6
THD+N vs Frequency, V_{PVDD} = 24 V	Figure 7
Idle Channel Noise vs PVDD	Figure 11
THD+N vs Output Power, V_{PVDD} = 12 V	Figure 13
THD+N vs Output Power, V_{PVDD} = 18 V	Figure 14
THD+N vs Output Power, V_{PVDD} = 24 V	Figure 15
Efficiency vs Output Power	Figure 19
Crosstalk vs Frequency, V_{PVDD} = 12 V	Figure 21
Headphone THD+N vs Frequency, V_{DRVDD} = 3.3 V	Figure 25
Headphone THD+N vs Output Power, V_{DRVDD} = 3.3 V	Figure 26
Headphone Crosstalk vs Frequency, V_{DRVDD} = 3.3 V, RHP = 16 Ω	Figure 27
Headphone Crosstalk vs Frequency, V_{DRVDD} = 3.3 V, RHP = 32 Ω	Figure 28
Line Driver THD+N vs Frequency, V_{DRVDD} = 3.3 V	Figure 29
Line Driver THD+N vs Output Voltage, V_{DRVDD} = 3.3 V	Figure 30
Line Driver Crosstalk vs Frequency, V_{DRVDD} = 3.3 V	Figure 31

10.2.2 Mono PBTL Configuration with Headphone and Line Driver Amplifier

A mono system refers to a system in which the amplifier is used to drive a single loudspeaker. Parallel Bridge Tied Load (PBTL) indicates that the two full-bridge channels of the device are placed in parallel and drive the loudspeaker simultaneously using an identical audio signal. The primary benefit of operating the TAS5729MD device in PBTL operation is to reduce the power dissipation and increase the current sourcing capabilities of the amplifier output. In this mode of operation, the current limit of the audio amplifier is approximately doubled while the on-resistance is approximately halved.

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The loudspeaker can be a full-range transducer or one that only reproduces the low-frequency content of an audio signal, as in the case of a powered subwoofer. Often in this use case, two stereo signals are mixed together and sent through a low-pass filter to create a single audio signal which contains the low-frequency information of the two channels.

This configuration also has a DirectPath headphone stereo amplifier which can be used independently from the speaker channel.

The Mono PBTL Configuration with Headphone and Line Driver Amplifier application is shown in Figure 58.

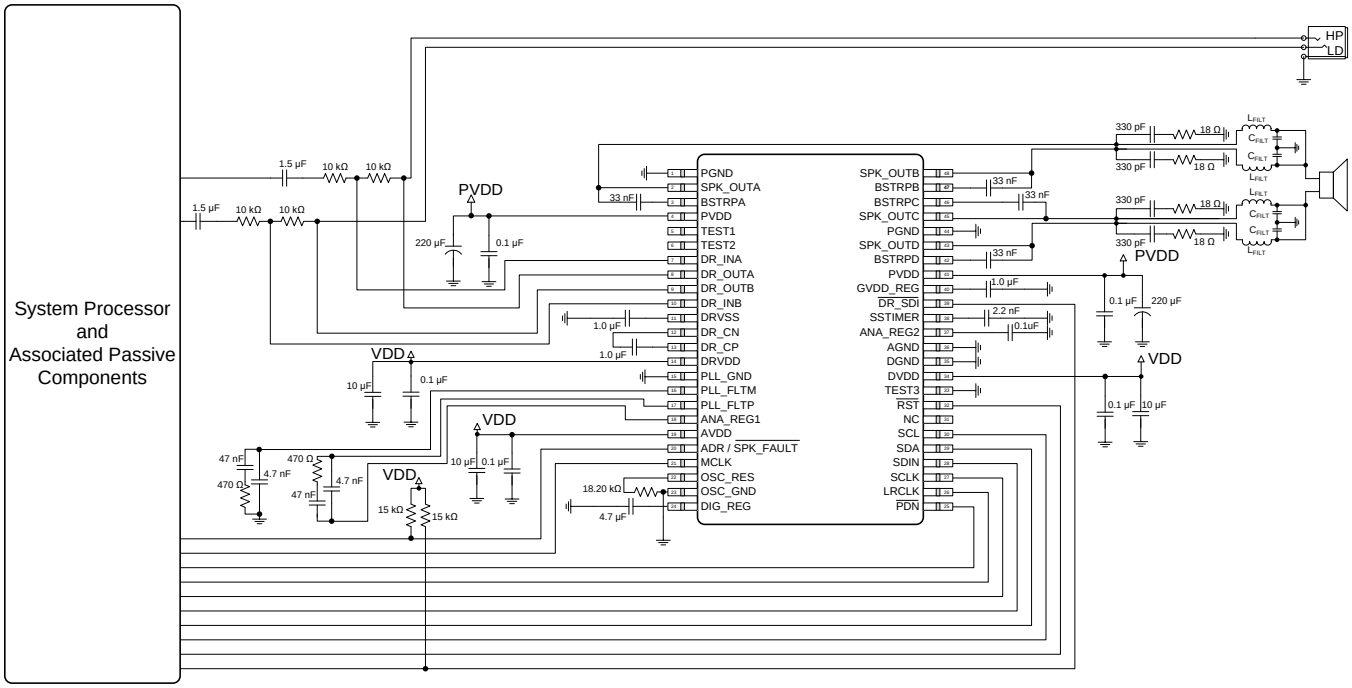

Figure 58. Mono PBTL Configuration with Headphone and Line Driver Amplifier

10.2.2.1 Design Requirements

Power supplies:

- 3.3-V power supply for internal digital, analog, and headphone/line driver circuitry.
- 4.5-V to 26-V power supply for internal power circuitry

Communication:

- System controller with I^2C control interface serving a compliant master

Audio digital input:

- Serial data in 16-, 20-, or 24-bit left-justified, right-justified, or I^2S format

Headphone/line driver input:

- Analog single-ended line input

Output components:

- 1 × 4-Ω speaker (recommended).
- 16-Ω headphones (recommended) / 5-kΩ line driver load

Output filter:

- 4 × 15-µH Inductors
- 4 × 0.33-µF Capacitors

Components required:

- 4 × 10-kΩ Resistor
- 2 × 470-Ω Resistor

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- 2 × 15-kΩ Resistor
- 1 × 18.2-kΩ Resistor
- 4 × 18-Ω Resistor
- 2 × 1.5-µF Capacitor
- 4 × 4.7-nF Capacitor
- 3 × 10-µF Capacitor
- 3 × 1-µF Capacitor
- 6 × 0.1-µF Capacitor
- 4 × 33-nF Capacitor
- 2 × 220-µF Capacitor
- 1 × 4.7-µF Capacitor
- 1 × 2.2-µF Capacitor
- 4 × 330-pF Capacitor

10.2.2.2 Detailed Design Procedure

See Stereo BTL Configuration With Headphone and Line Driver Amplifier.

10.2.2.3 Application Curves

Table 26. Mono PBTL Configuration with Headphone and Line Driver Amplifier Application Curves

PLOT TITLE	FIGURE
Output Power vs PVDD	Figure 4
THD+N vs Frequency, V_{PVDD} = 12 V	Figure 8
THD+N vs Frequency, V_{PVDD} = 18 V	Figure 9
THD+N vs Frequency, V_{PVDD} = 24 V	Figure 10
Idle Channel Noise vs PVDD	Figure 12
THD+N vs Output Power, V_{PVDD} = 12 V	Figure 16
THD+N vs Output Power, V_{PVDD} = 18 V	Figure 17
THD+N vs Output Power, V_{PVDD} = 24 V	Figure 18
Efficiency vs Output Power	Figure 20
Crosstalk vs Frequency, V_{PVDD} = 12 V	Figure 22
Headphone THD+N vs Frequency, V_{DRVDD} = 3.3 V	Figure 25
Headphone THD+N vs Output Power, V_{DRVDD} = 3.3 V	Figure 26
Headphone Crosstalk vs Frequency, V_{DRVDD} = 3.3 V, RHP = 16 Ω	Figure 27
Headphone Crosstalk vs Frequency, V_{DRVDD} = 3.3 V, RHP = 32 Ω	Figure 28
Line Driver THD+N vs Frequency, V_{DRVDD} = 3.3 V	Figure 29
Line Driver THD+N vs Output Voltage, V_{DRVDD} = 3.3 V	Figure 30
Line Driver Crosstalk vs Frequency, V_{DRVDD} = 3.3 V	Figure 31

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11 Power Supply Recommendations

The TAS5729MD requires two power supplies; a low-voltage 3.3-V nominal for the pins DVDD, AVDD, and DRVDD and a high-voltage power supply, 4.5 V to 26 V for the pin PVDD. The low-voltage and high-voltage power supplies have no required sequencing for power-up; however, the $\overline{\text{PDN}}$ pin should be put to low before removing the low-voltage power supplies to protect the outputs.

11.1 DVDD, AVDD, and DRVDD Supplies

The AVDD supply is used to power the analog internal circuit of the device, and requires a well-regulated and filtered 3.3-V supply voltage. The DVDD supply is used to power the digital circuitry, and also requires a well-regulated and filtered 3.3-V supply voltage. The DRVDD supply is used to power the DirectPath™ headphone/line driver.

11.2 PVDD Power Supply

The TAS5729MD class-D audio amplifier requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) and noise is as low as possible. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device PVDD leads works best. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier is recommended.

12 Layout

12.1 Layout Guidelines

Class-D switching edges are fast and switched currents are high, therefore the user must take care when planning the layout of the printed-circuit board. The following suggestions will help to meet audio, thermal, and EMC requirements:

- TAS5729MD uses the PCB for heat sinking; therefore, the PowerPAD must be soldered to the PCB and adequate copper area and copper vias connecting the top, bottom, and internal layers should be used.
- Decoupling capacitors: the high-frequency decoupling capacitors should be placed as close to the supply pins as possible; on the TAS5729MD a 1-µF high-quality ceramic capacitor is used. Large (10 µF or greater) bulk power supply decoupling capacitors should be placed near the TAS5729MD on the PVDD supply.
- Keep the current loop from each of the outputs through the output inductor and the small filter capacitor and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding: a big common GND plane is recommended. The PVDD decoupling capacitors should connect to GND. The TAS5729MD PowerPAD should be connected to GND.
- Crosstalk: it is recommended to have a width separation between analog traces, like headphone input or outputs, to avoid possible crosstalk.
- Output filter: remember to select inductors that can handle the high short-circuit current of the device. The LC filter should be placed close to the outputs. The capacitors used should be grounded.

The EVM product folder and User's Guide available on www.ti.com shows schematic, bill of material, gerber files, and more detailed layout plots.

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12.2 Layout Example

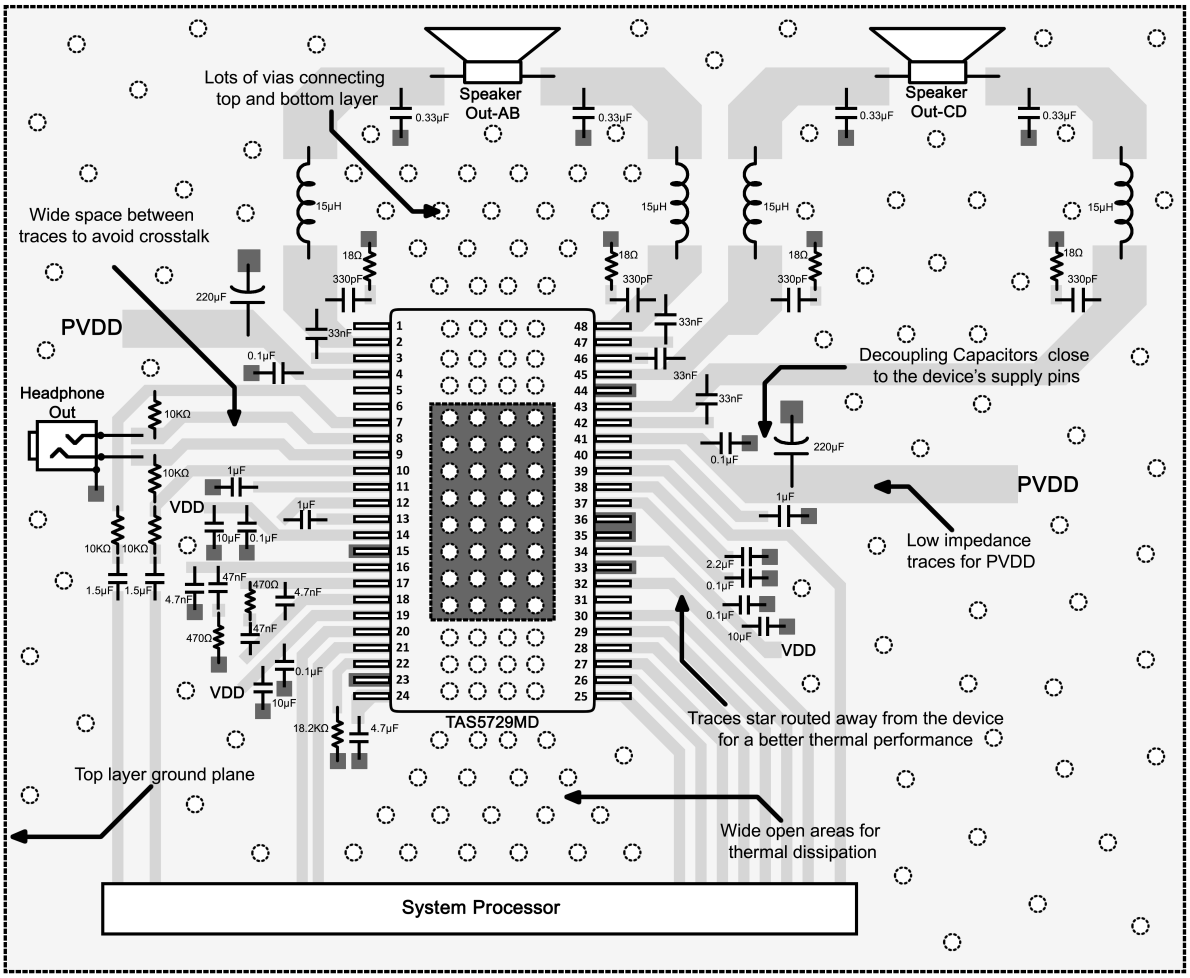

Figure 59. TAS5729MD Layout Example

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

TAS5721xx, TAS5723xx, and TAS5729xx Evaluation Module (SLOU367)

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

DirectPath, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5729MDDCA	Active	Production	HTSSOP (DCA) | 48	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5729MD
TAS5729MDDCA.A	Active	Production	HTSSOP (DCA) | 48	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5729MD
TAS5729MDDCA.B	Active	Production	HTSSOP (DCA) | 48	40 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5729MD
TAS5729MDDCAR	Active	Production	HTSSOP (DCA) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5729MD
TAS5729MDDCAR.A	Active	Production	HTSSOP (DCA) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5729MD
TAS5729MDDCAR.B	Active	Production	HTSSOP (DCA) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	TAS5729MD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

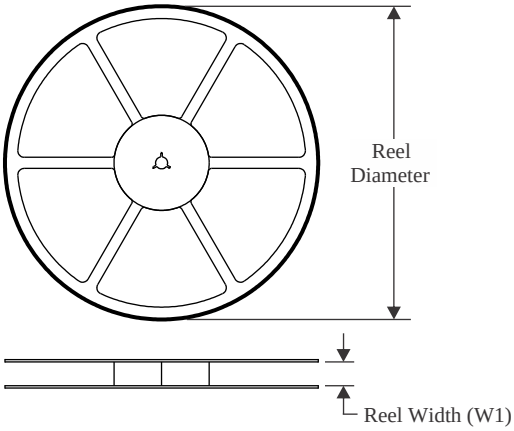
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

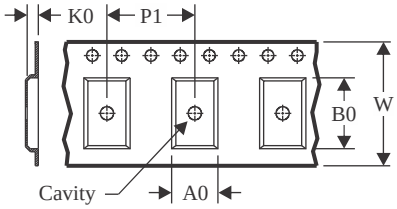
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

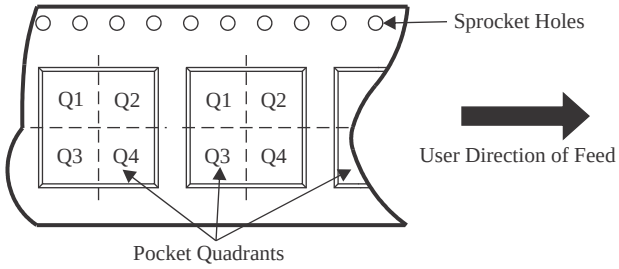


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

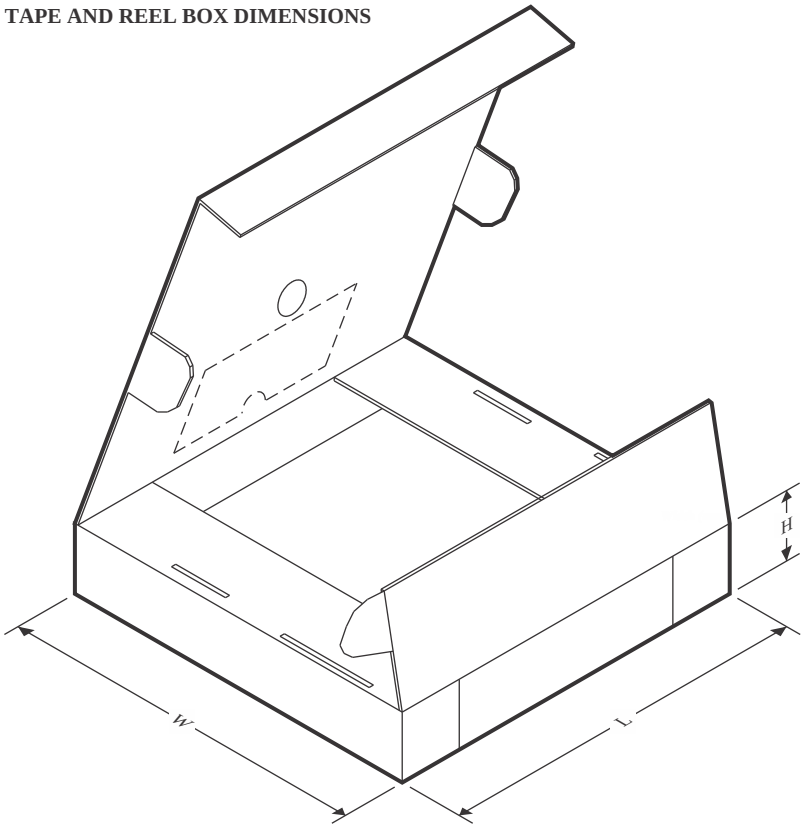
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5729MDDCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

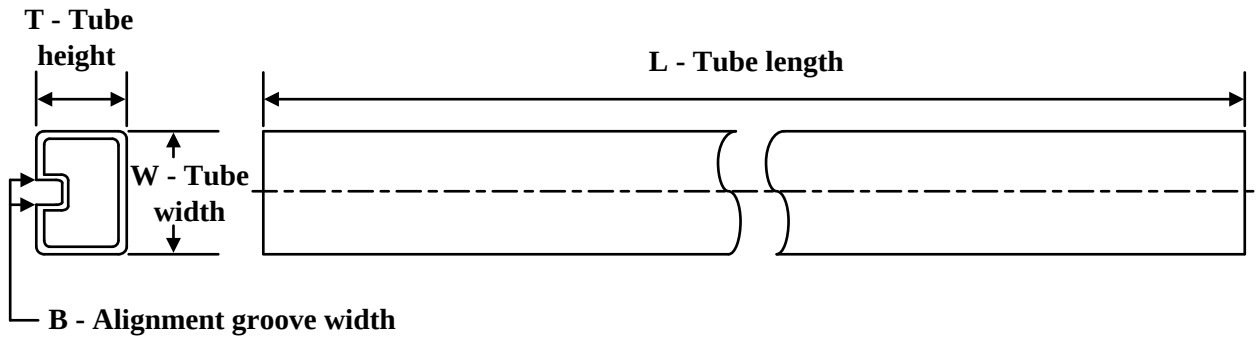
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5729MDDCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5729MDDCA	DCA	HTSSOP	48	40	530	11.89	3600	4.9
TAS5729MDDCA.A	DCA	HTSSOP	48	40	530	11.89	3600	4.9
TAS5729MDDCA.B	DCA	HTSSOP	48	40	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

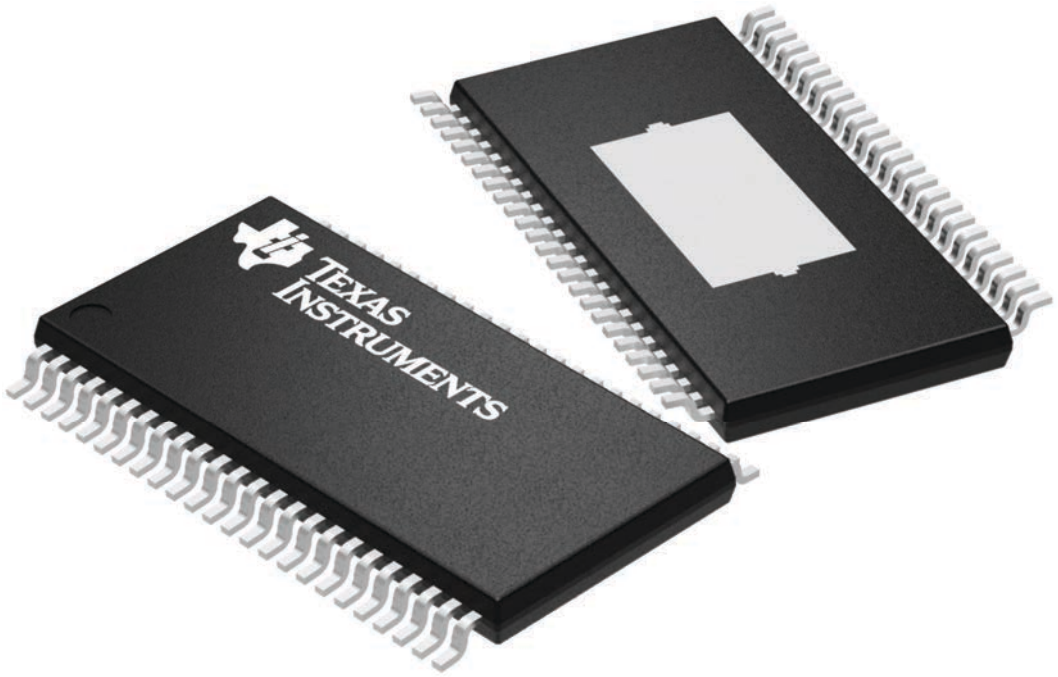
DCA 48

HTSSOP - 1.2 mm max height

12.5 x 6.1, 0.5 mm pitch

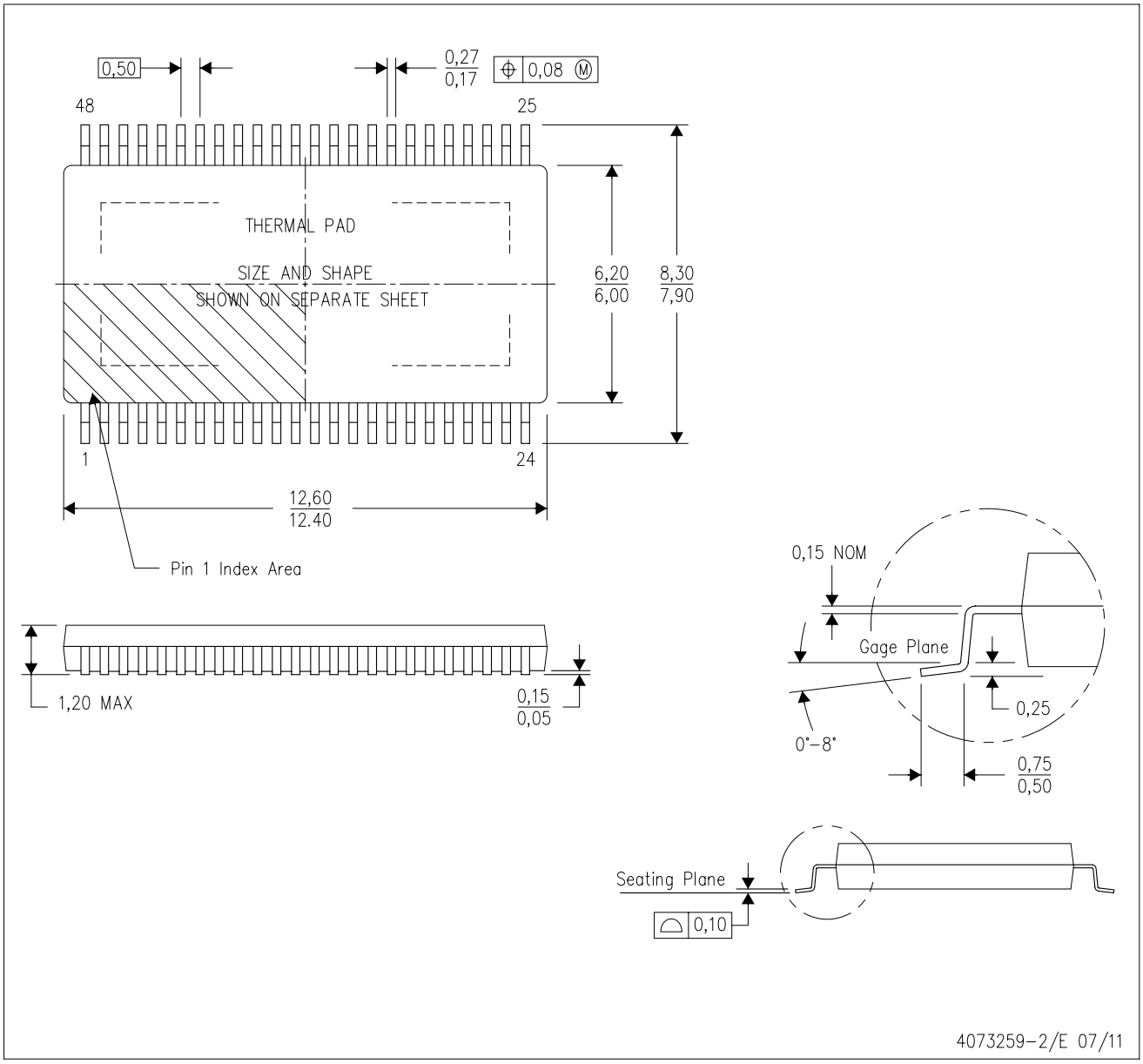
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224608/A

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

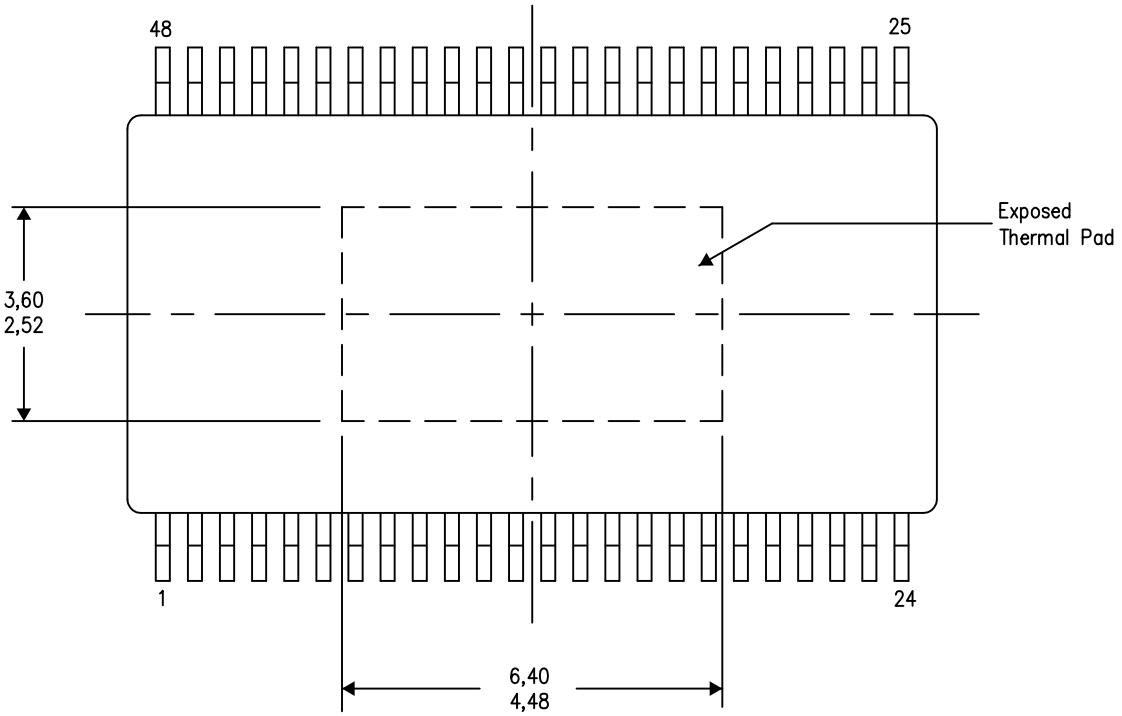
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

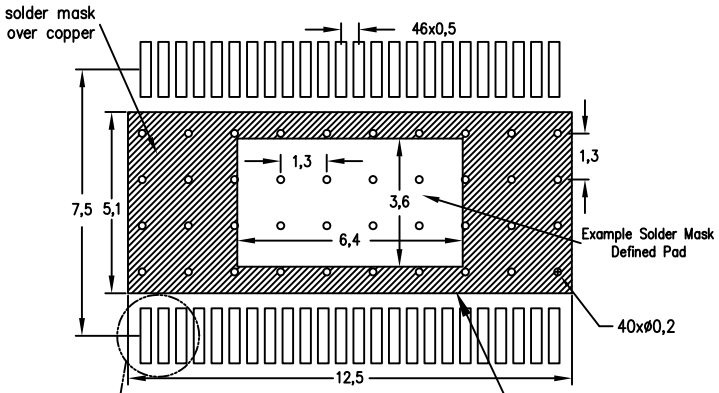
4206320–4/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

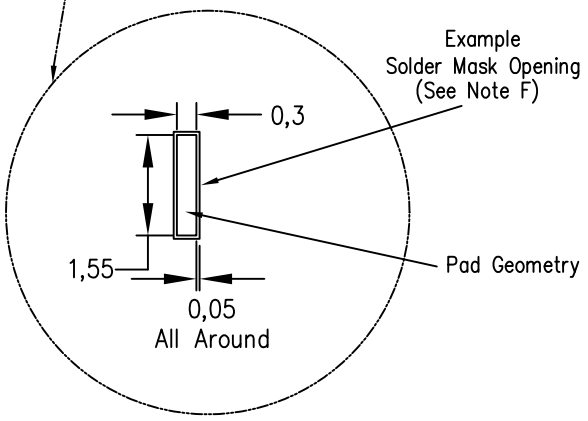
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

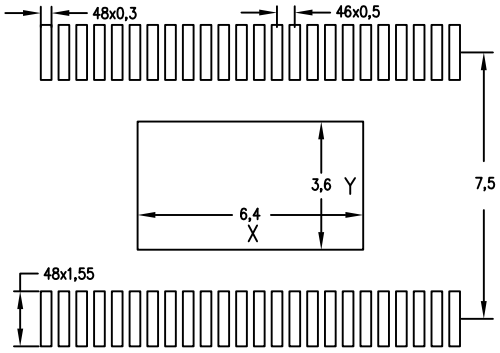


Increasing copper area will
enhance thermal performance
(See Note D)

Example
Non Soldermask Defined Pad



Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



(See Note E)

Center PowerPAD Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.21	4.06
0.127mm	6.40	3.60
0.152mm	5.85	3.29
0.178mm	5.41	3.04

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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