# SN74AVCH4T245 4-Bit Dual-Supply Bus Transceiver With Configurable Level-Shifting, Voltage Translation, and 3-State Outputs

## 1 Features

- Control inputs $V_{IH}/V_{IL}$ levels are referenced to $V_{CCA}$ voltage
- Fully configurable dual-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range
- I/Os Are 4.6V Tolerant
- $I_{off}$ supports partial power-down-mode operation
- Bus hold on data inputs eliminates the need for external pull-up/pull-down resistors
- Supports data rate up to:
  - 380Mbps (1.8V to 3.3V Translation)
  - 200Mbps (<1.8V to 3.3V Translation)
  - 200Mbps (Translate to 2.5V or 1.8V)
  - 150Mbps (Translate to 1.5V)
  - 100Mbps (Translate to 1.2V)
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22:
  - 8000V Human Body Model (A114-A)
  - 200V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)

## 2 Applications

- Personal electronics
- Industrial
- Enterprise
- Telecom

## 3 Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track $V_{CCA}$. $V_{CCA}$ accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track $V_{CCB}$. $V_{CCB}$ accepts any supply voltage from 1.2V to 3.6V. The SN74AVCH4T245 is optimized to operate with $V_{CCA}/V_{CCB}$ set at 1.2V to 3.6V. It is operational with $V_{CCA}/V_{CCB}$ as low as 1.2V. This allows for universal low voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The SN74AVCH4T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess $I_{CC}$ and $I_{CCZ}$.

The SN74AVCH4T245 device control pins (1DIR, 2DIR, 1OE, and 2OE) are supplied by $V_{CCA}$.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The $V_{CC}$ isolation feature is designed so that if either $V_{CC}$ input is at GND, then both ports are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry on the powered-up side always stays active.

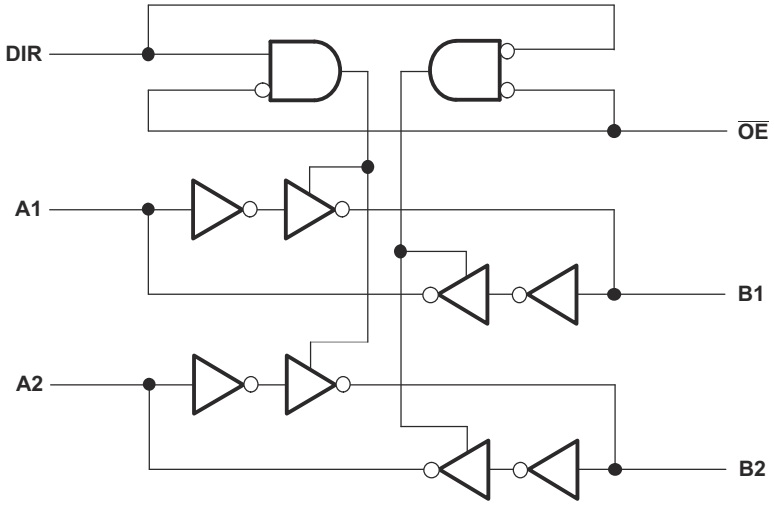
To put the device in the high-impedance state during power up or power down, tie the $\overline{OE}$ pin to $V_{CC}$ through a pull-up resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| SN74AVCH4T245 | D (SOIC, 16) | 9.9mm × 6mm |
| | PW (TSSOP, 16) | 5mm × 6.4mm |
| | DGV (TVSOP, 16) | 3.6mm × 6.4mm |
| | RSV (UQFN, 16) | 2.6mm × 1.8mm |
| | RGY (VQFN, 16) | 4mm × 3.5mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.




**Logic Diagram (Positive Logic) for 1/2 of SN74AVCH4T245**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## 4 Pin Configuration and Functions

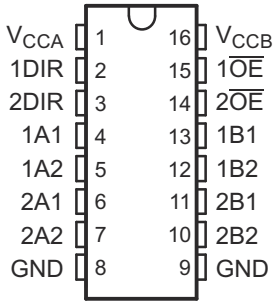


**Figure 4-1. D, DGV, or PW Packages 16-Pin SOIC, TVSOP, or TSSOP Top View**

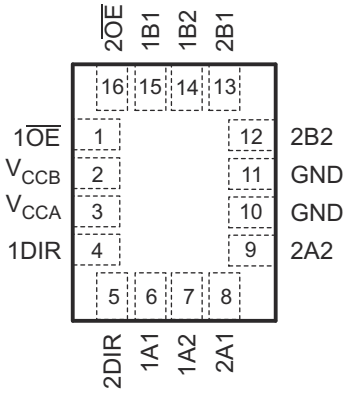


**Figure 4-2. RSV Package 16-Pin UQFN Top View**

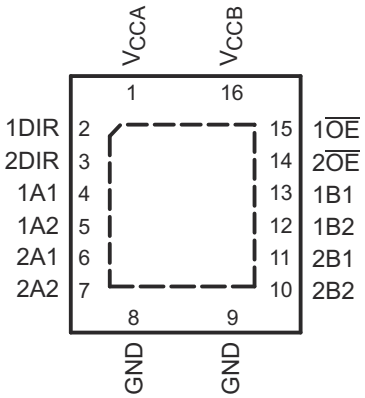


**Figure 4-3. RGY Package 16-Pin VQFN Top View**


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**Table 4-1. Pin Functions**

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, TVSOP, TSSOP, VQFN | UQFN | | |
| 1A1 | 4 | 6 | I/O | Input/output 1A1. Referenced to $V_{CCA}$. |
| 1A2 | 5 | 7 | I/O | Input/output 1A2. Referenced to $V_{CCA}$. |
| 1B1 | 13 | 15 | I/O | Input/output 1B1. Referenced to $V_{CCA}$. |
| 1B2 | 12 | 14 | I/O | Input/output 1B2. Referenced to $V_{CCA}$. |
| 1DIR | 2 | 4 | I | Direction-control input for 1 ports. |
| $1\overline{OE}$ | 15 | 1 | I | 3-state output-mode enables. Pull OE high to place ‘1’ outputs in 3-state mode. Referecend to $V_{CCA}$. |
| 2A1 | 6 | 8 | I/O | Input/output 2A1. Referenced to $V_{CCA}$. |
| 2A2 | 7 | 9 | I/O | Input/output 2A2. Referenced to $V_{CCA}$. |
| 2B1 | 11 | 13 | I/O | Input/output 2B1. Referenced to $V_{CCA}$. |
| 2B2 | 10 | 12 | I/O | Input/output 2B2. Referenced to $V_{CCA}$. |
| 2DIR | 3 | 5 | I | Direction-control input for 2 ports. |
| $2\overline{OE}$ | 14 | 16 | I | 3-state output-mode enables. Pull OE high to place ‘2’ outputs in 3-state mode. Referecend to $V_{CCA}$. |
| GND | 8, 9 | 10, 11 | - | Ground. |
| $V_{CCA}$ | 1 | 3 | - | A-port power supply voltage. 1.2V ≤ VCCA ≤ 3.6V. |
| $V_{CCB}$ | 16 | 2 | - | B-port power supply voltage. 1.2V ≤ VCCA ≤ 3.6V. |

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage A | | –0.5 | 4.6 | V |
| $V_{CCB}$ | Supply voltage B | | –0.5 | 4.6 | V |
| $V_I$ | Input Voltage [2] | I/O Ports (A Port) | –0.5 | 4.6 | V |
| | | I/O Ports (B Port) | –0.5 | 4.6 | |
| | | Control Inputs | –0.5 | 4.6 | |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state [2] | A Port | –0.5 | 4.6 | V |
| | | B Port | –0.5 | 4.6 | |
| $V_O$ | Voltage applied to any output in the high or low state [2] [3] | A Port | –0.5 | $V_{CCA}$ + 0.5 | V |
| | | B Port | –0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $T_j$ | Junction Temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±8000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |
| | | Machine model, per A115-A | 200 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.


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## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4) (5)

| | | | $V_{CCI}$ | $V_{CCO}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage A | | | | 1.2 | 3.6 | V |
| $V_{CCB}$ | Supply voltage B | | | | 1.2 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | Data inputs (4) | 1.2V to 1.95V | | $V_{CCI}$ x 0.65 | | V |
| | | | 1.95V to 2.7V | | 1.6 | | V |
| | | | 2.7V to 3.6V | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | Data inputs (4) | 1.2V to 1.95V | | | $V_{CCI}$ x 0.35 | V |
| | | | 1.95V to 2.7V | | | 0.7 | V |
| | | | 2.7V to 3.6V | | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | DIR (refrenced to $V_{CCA}$) (5) | 1.2V to 1.95V | | $V_{CCA}$ x 0.65 | | V |
| | | | 1.95V to 2.7V | | 1.6 | | |
| | | | 2.7V to 3.6V | | 2 | | |
| $V_{IL}$ | Low-level input voltage | DIR (refrenced to $V_{CCA}$) (5) | 1.2V to 1.95V | | | $V_{CCA}$ x 0.35 | V |
| | | | 1.95V to 2.7V | | | 0.7 | |
| | | | 2.7V to 3.6V | | | 0.8 | |
| $V_I$ | Input voltage | | | | 0 | 3.6 | V |
| $V_O$ | Output voltage | Active state | | | 0 | $V_{CCO}$ | V |
| | | 3-state | | | 0 | 3.6 | |
| $I_{OH}$ | High-level output current | | | 1.2V | | –3 | mA |
| | | | | 1.4V to 1.6V | | –6 | |
| | | | | 1.65V to 1.95V | | –8 | |
| | | | | 2.3V to 2.7V | | –9 | |
| | | | | 3V to 3.6V | | -12 | |
| $I_{OL}$ | Low-level output current | | | 1.2V | | 3 | mA |
| | | | | 1.4V to 1.6V | | 6 | |
| | | | | 1.65V to 1.95V | | 8 | |
| | | | | 2.3V to 2.7V | | 9 | |
| | | | | 3V to 3.6V | | 12 | |
| Δt/Δv | Input transition rise and fall time | | | | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | | | –40 | 85 | °C |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(3) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.
(4) For $V_{CCI}$ values not specified in the data sheet, $V_{IH}$ min = $V_{CCI}$ × 0.7V, $V_{IL}$ max = $V_{CCI}$ × 0.3V
(5) For $V_{CCA}$ values not specified in the data sheet, $V_{IH}$ min = $V_{CCA}$ × 0.7V, $V_{IL}$ max = $V_{CCI}$ × 0.3V

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## 5.4 Thermal Information

| THERMAL METRIC[1] | | SN74AVCH4T245 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DGV (TVSOP) | PW (TSSOP) | RGY (VQFN) | RSV (UQFN) | |
| | | 6 PINS | 6 PINS | 6 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 85.5 | 126 | 102.8 | 68.8 | 146.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 46.9 | 50.8 | 35.9 | 70.6 | 53.6 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 43 | 57.7 | 57.5 | 45 | 75.6 | |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 13.4 | 5.7 | 1.6 | 11.9 | 13.5 | |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 42.7 | 57.2 | 56.9 | 44.7 | 75.6 | |
| $R_{\theta JC(bottom)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | 28.2 | N/A | |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1] [2]

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature (TA) –40°C to 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –100µA | $V_I = V_{IH}$ | 1.2V to 3.6V | 1.2V to 3.6V | $V_{CCO}$ – 0.2 | | | V |
| | | $I_{OH}$ = –3mA | | 1.2V | 1.2V | | 0.95 | | |
| | | $I_{OH}$ = –6mA | | 1.4V | 1.4V | 1.05 | | | |
| | | $I_{OH}$ = –8mA | | 1.65V | 1.65V | 1.2 | | | |
| | | $I_{OH}$ = –9mA | | 2.3V | 2.3V | 1.75 | | | |
| | | $I_{OH}$ = –12mA | | 3V | 3V | 2.3 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100µA | $V_I = V_{IL}$ | 1.2V to 3.6V | 1.2V to 3.6V | | | 0.2 | V |
| | | $I_{OL}$ = 3mA | | 1.2V | 1.2V | | 0.15 | | |
| | | $I_{OL}$ = 6mA | | 1.4V | 1.4V | | | 0.35 | |
| | | $I_{OL}$ = 8mA | | 1.65V | 1.65V | | | 045 | |
| | | $I_{OL}$ = 9mA | | 2.3V | 2.3V | | | 0.55 | |
| | | $I_{OL}$ = 12mA | | 3V | 3V | | | 0.7 | |
| $I_I$ | DIR | VI = $V_{CCA}$ or GND | | 1.2V to 3.6V | 1.2V to 3.6V | –1 | 0.025 | 1 | µA |
| $I_{BHL}$ | Bus-hold low sustaining current Port A or Port B [6] | $V_I$ = 0.42V | | 1.2V | 1.2V | | 25 | | µA |
| | | $V_I$ = 0.49V | | 1.4V | 1.4V | 15 | | | |
| | | $V_I$ = 0.58V | | 1.65V | 1.65V | 25 | | | |
| | | $V_I$ = 0.7V | | 2.3V | 2.3V | 45 | | | |
| | | $V_I$ = 0.8V | | 3V | 3V | 100 | | | |
| $I_{BHH}$ | Bus-hold high sustaining current Port A or Port B [7] | $V_I$ = 0.78V | | 1.2V | 1.2V | | –25 | | µA |
| | | $V_I$ = 0.91V | | 1.4V | 1.4V | –15 | | | |
| | | $V_I$ = 1.07V | | 1.65V | 1.65V | –25 | | | |
| | | $V_I$ = 1.6V | | 2.3V | 2.3V | –45 | | | |
| | | $V_I$ = 2V | | 3V | 3V | –100 | | | |


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over operating free-air temperature range (unless otherwise noted)[1] [2]

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | Operating free-air temperature (TA) –40°C to 85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| $I_{BHLO}$ | Bus-hold low overdrive current [8] | Ramp input up $V_I$ = 0 to $V_{CCI}$ | | 1.2 | 1.2 | | 50 | | μA |
| | | | | 1.6 | 1.6 | 125 | | | |
| | | | | 1.95V | 1.95V | 200 | | | |
| | | | | 2.7V | 2.7V | 300 | | | |
| | | | | 3.6V | 3.6V | 500 | | | |
| $I_{BHHO}$ | Bus-hold high overdrive current [9] | Ramp input down $V_I$ = $V_{CCI}$ to 0 | | 1.2 | 1.2 | | -50 | | μA |
| | | | | 1.6 | 1.6 | –125 | | | |
| | | | | 1.95V | 1.95V | –200 | | | |
| | | | | 2.7V | 2.7V | –300 | | | |
| | | | | 3.6V | 3.6V | –500 | | | |
| $I_{off}$ | A port | $V_I$ or $V_O$ = 0V - 3.6V | | 0V | 0V to 3.6V | –5 | 0.1 | 5 | μA |
| | B port | | | 0V to 3.6V | 0V | –5 | 0.1 | 5 | |
| $I_{OZ}$ | B port | $V_I$ = or $V_O$ = 0 to 3.6V | | 0V | 3.6V | –5 | 0.5 | 5 | μA |
| | A port | | | 3.6V | 0V | –5 | 0.5 | 5 | |
| $I_{CCA}$ | | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 1.2V to 3.6V | 1.2V to 3.6V | | | 8 | μA |
| | | | | 0V | 3.6V | | | –2 | |
| | | | | 3.6V | 0V | | | 8 | |
| $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 1.2V to 3.6V | 1.2V to 3.6V | | | 8 | μA |
| | | | | 0V | 3.6V | | | 8 | |
| | | | | 3.6V | 0V | | | –2 | |
| $I_{CCA}$ + $I_{CCB}$ | | $V_I$ = $V_{CCI}$ or GND | $I_O$ = 0 | 1.2V to 3.6V | 1.2V to 3.6V | | | 16 | μA |
| $C_i$ | Control Input | $V_I$ = 3.3V or GND | | 3.3V | 3.3V | | 3.5 | 4.5 | pF |
| $C_{io}$ | A or B port | $V_O$ = 3.3V or GND | | 3.3V | 3.3V | | 6 | 7 | pF |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port.

## 5.6 Switching Characteristics, $V_{CCA}$ = 1.2V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.2V (see Figure 6-1)

| PARAMETER | FROM | TO | B-Port Supply Voltage ($V_{CCB}$) | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| | | | TYP | TYP | TYP | TYP | TYP | |
| $t_{PLH}$ | A | B | 3.4 | 2.9 | 2.7 | 2.6 | 2.8 | ns |
| $t_{PHL}$ | | | 3.4 | 2.9 | 2.7 | 2.6 | 2.8 | |
| $t_{PLH}$ | B | A | 3.6 | 3.1 | 2.8 | 2.6 | 2.6 | |
| $t_{PHL}$ | | | 3.6 | 3.1 | 2.8 | 2.6 | 2.6 | |
| $t_{PHZ}$ | $\overline{OE}$ | A | 5.6 | 4.7 | 4.3 | 3.9 | 3.7 | ns |
| $t_{PLZ}$ | | | 5.6 | 4.7 | 4.3 | 3.9 | 3.7 | |
| $t_{PHZ}$ | $\overline{OE}$ | B | 5 | 4.3 | 3.9 | 3.6 | 3.6 | |
| $t_{PLZ}$ | | | 5 | 4.3 | 3.9 | 3.6 | 3.6 | |
| $t_{PZH}$ | $\overline{OE}$ | A | 6.2 | 5.2 | 5.2 | 4.3 | 4.8 | ns |
| $t_{PZL}$ | | | 6.2 | 5.2 | 5.2 | 4.3 | 4.8 | |
| $t_{PZH}$ | $\overline{OE}$ | B | 5.9 | 5.1 | 5 | 4.7 | 5.5 | |
| $t_{PZL}$ | | | 5.9 | 5.1 | 5 | 4.7 | 5.5 | |

## 5.7 Switching Characteristics, $V_{CCA}$ = 1.5 ± 0.1V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.5 ± 0.1V (see Figure 6-1)

| PARAMETER | FROM | TO | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2V | | | 1.5 ± 0.1V | | | 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | B | | 3.2 | | 0.3 | | 6.3 | 0.3 | | 5.2 | 0.4 | | 4.2 | 0.4 | | 4.2 | ns |
| $t_{PHL}$ | | | | 3.2 | | 0.3 | | 6.3 | 0.3 | | 5.2 | 0.4 | | 4.2 | 0.4 | | 4.2 | |
| $t_{PLH}$ | B | A | | 3.3 | | 0.7 | | 6.3 | 0.5 | | 6 | 0.4 | | 5.7 | 0.3 | | 5.6 | |
| $t_{PHL}$ | | | | 3.3 | | 0.7 | | 6.3 | 0.5 | | 6 | 0.4 | | 5.7 | 0.3 | | 5.6 | |
| $t_{PHZ}$ | $\overline{OE}$ | A | | 4.9 | | 1.4 | | 9.6 | 1.1 | | 9.5 | 0.7 | | 9.4 | 0.4 | | 9.4 | ns |
| $t_{PLZ}$ | | | | 4.9 | | 1.4 | | 9.6 | 1.1 | | 9.5 | 0.7 | | 9.4 | 0.4 | | 9.4 | |
| $t_{PHZ}$ | $\overline{OE}$ | B | | 4.5 | | 1.4 | | 9.6 | 1.1 | | 7.7 | 0.9 | | 5.8 | 0.9 | | 5.6 | |
| $t_{PLZ}$ | | | | 4.5 | | 1.4 | | 9.6 | 1.1 | | 7.7 | 0.9 | | 5.8 | 0.9 | | 5.6 | |
| $t_{PZH}$ | $\overline{OE}$ | A | | 5.6 | | 1.8 | | 10.2 | 1.5 | | 10.2 | 1.3 | | 10.2 | 1.6 | | 10.2 | ns |
| $t_{PZL}$ | | | | 5.6 | | 1.8 | | 10.2 | 1.5 | | 10.2 | 1.3 | | 10.2 | 1.6 | | 10.2 | |
| $t_{PZH}$ | $\overline{OE}$ | B | | 5.2 | | 1.9 | | 10.3 | 1.9 | | 9.1 | 1.4 | | 7.4 | 1.2 | | 7.6 | |
| $t_{PZL}$ | | | | 5.2 | | 1.9 | | 10.3 | 1.9 | | 9.1 | 1.4 | | 7.4 | 1.2 | | 7.6 | |


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## 5.8 Switching Characteristics, $V_{CCA}$ = 1.8 ± 0.15V

over recommended operating free-air temperature range, $V_{CCA}$ = 1.8V ± 0.15V (see Figure 6-1)

| PARAMETER | FROM | TO | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2V | | | 1.5 ± 0.1V | | | 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | B | | 2.9 | | 0.1 | | 6 | 0.1 | | 4.9 | 0.1 | | 3.9 | 0.1 | | 3.9 | ns |
| $t_{PHL}$ | | | | 2.9 | | 0.1 | | 6 | 0.1 | | 4.9 | 0.1 | | 3.9 | 0.1 | | 3.9 | |
| $t_{PLH}$ | B | A | | 3 | | 0.6 | | 5.3 | 0.5 | | 4.9 | 0.3 | | 4.6 | 0.3 | | 4.5 | |
| $t_{PHL}$ | | | | 3 | | 0.6 | | 5.3 | 0.5 | | 4.9 | 0.3 | | 4.6 | 0.3 | | 4.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | A | | 4.4 | | 1 | | 7.4 | 1 | | 7.3 | 0.6 | | 7.3 | 0.4 | | 7.2 | ns |
| $t_{PLZ}$ | | | | 4.4 | | 1 | | 7.4 | 1 | | 7.3 | 0.6 | | 7.3 | 0.4 | | 7.2 | |
| $t_{PHZ}$ | $\overline{OE}$ | B | | 4.1 | | 1.2 | | 9.2 | 1 | | 7.4 | 0.8 | | 5.3 | 0.8 | | 4.6 | |
| $t_{PLZ}$ | | | | 4.1 | | 1.2 | | 9.2 | 1 | | 7.4 | 0.8 | | 5.3 | 0.8 | | 4.6 | |
| $t_{PZH}$ | $\overline{OE}$ | A | | 5.4 | | 1.6 | | 8.6 | 1.8 | | 8.7 | 1.3 | | 8.7 | 1.6 | | 8.7 | ns |
| $t_{PZL}$ | | | | 5.4 | | 1.6 | | 8.6 | 1.8 | | 8.7 | 1.3 | | 8.7 | 1.6 | | 8.7 | |
| $t_{PZH}$ | $\overline{OE}$ | B | | 5 | | 1.7 | | 9.9 | 1.6 | | 8.7 | 1.2 | | 6.9 | 1 | | 6.9 | |
| $t_{PZL}$ | | | | 5 | | 1.7 | | 9.9 | 1.6 | | 8.7 | 1.2 | | 6.9 | 1 | | 6.9 | |

## 5.9 Switching Characteristics, $V_{CCA}$ = 2.5 ± 0.2V

over recommended operating free-air temperature range, $V_{CCA}$ = 2.5 ± 0.2V (see Figure 6-1)

| PARAMETER | FROM | TO | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2V | | | 1.5 ± 0.1V | | | 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | B | | 2.8 | | 0.1 | | 5.7 | 0.1 | | 4.6 | 0.2 | | 3.5 | 0.1 | | 3.6 | ns |
| $t_{PHL}$ | | | | 2.8 | | 0.1 | | 5.7 | 0.1 | | 4.6 | 0.2 | | 3.5 | 0.1 | | 3.6 | |
| $t_{PLH}$ | B | A | | 2.7 | | 0.6 | | 4.2 | 0.4 | | 3.9 | 0.2 | | 3.4 | 0.2 | | 3.3 | |
| $t_{PHL}$ | | | | 2.7 | | 0.6 | | 4.2 | 0.4 | | 3.9 | 0.2 | | 3.4 | 0.2 | | 3.3 | |
| $t_{PHZ}$ | $\overline{OE}$ | A | | 4 | | 0.7 | | 6.5 | 0.7 | | 5.2 | 0.6 | | 4.8 | 0.4 | | 4.8 | ns |
| $t_{PLZ}$ | | | | 4 | | 0.7 | | 6.5 | 0.7 | | 5.2 | 0.6 | | 4.8 | 0.4 | | 4.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | B | | 3.8 | | 0.9 | | 8.8 | 0.8 | | 7 | 0.6 | | 4.8 | 0.6 | | 4 | |
| $t_{PLZ}$ | | | | 3.8 | | 0.9 | | 8.8 | 0.8 | | 7 | 0.6 | | 4.8 | 0.6 | | 4 | |
| $t_{PZH}$ | $\overline{OE}$ | A | | 4.7 | | 1 | | 8.4 | 1 | | 8.4 | 1 | | 6.2 | 1 | | 6.6 | ns |
| $t_{PZL}$ | | | | 4.7 | | 1 | | 8.4 | 1 | | 8.4 | 1 | | 6.2 | 1 | | 6.6 | |
| $t_{PZH}$ | $\overline{OE}$ | B | | 4.5 | | 1.5 | | 9.4 | 1.3 | | 8.2 | 1.1 | | 6.2 | 0.9 | | 5.2 | |
| $t_{PZL}$ | | | | 4.5 | | 1.5 | | 9.4 | 1.3 | | 8.2 | 1.1 | | 6.2 | 0.9 | | 5.2 | |

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## 5.10 Switching Characteristics, $V_{CCA}$ = 3.3 ± 0.3V

over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 ± 0.3V (see Figure 6-1)

| PARAMETER | FROM | TO | B-Port Supply Voltage ($V_{CCB}$) | | | | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2V | | | 1.5 ± 0.1V | | | 1.8 ± 0.15V | | | 2.5 ± 0.2V | | | 3.3 ± 0.3V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | B | | 2.9 | | 0.1 | | 5.6 | 0.1 | | 4.5 | 0.1 | | 3.3 | 0.1 | | 2.9 | ns |
| $t_{PHL}$ | | | | 2.9 | | 0.1 | | 5.6 | 0.1 | | 4.5 | 0.1 | | 3.3 | 0.1 | | 2.9 | |
| $t_{PLH}$ | B | A | | 2.6 | | 0.6 | | 4.2 | 0.4 | | 3.4 | 0.2 | | 3 | 0.1 | | 2.8 | |
| $t_{PHL}$ | | | | 2.6 | | 0.6 | | 4.2 | 0.4 | | 3.4 | 0.2 | | 3 | 0.1 | | 2.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | A | | 3.8 | | 0.6 | | 8.7 | 0.6 | | 5.2 | 0.6 | | 3.8 | 0.4 | | 3.8 | ns |
| $t_{PLZ}$ | | | | 3.8 | | 0.6 | | 8.7 | 0.6 | | 5.2 | 0.6 | | 3.8 | 0.4 | | 3.8 | |
| $t_{PHZ}$ | $\overline{OE}$ | B | | 3.7 | | 0.8 | | 8.7 | 0.6 | | 6.8 | 0.5 | | 4.7 | 0.5 | | 3.8 | |
| $t_{PLZ}$ | | | | 3.7 | | 0.8 | | 8.7 | 0.6 | | 6.8 | 0.5 | | 4.7 | 0.5 | | 3.8 | |
| $t_{PZH}$ | $\overline{OE}$ | A | | 4.8 | | 0.7 | | 9.3 | 0.7 | | 8.3 | 0.7 | | 5.6 | 0.7 | | 6.6 | ns |
| $t_{PZL}$ | | | | 4.8 | | 0.7 | | 9.3 | 0.7 | | 8.3 | 0.7 | | 5.6 | 0.7 | | 6.6 | |
| $t_{PZH}$ | $\overline{OE}$ | B | | 5.3 | | 1.4 | | 9.3 | 1.2 | | 8.1 | 1 | | 6.4 | 0.8 | | 6.2 | |
| $t_{PZL}$ | | | | 5.3 | | 1.4 | | 9.3 | 1.2 | | 8.1 | 1 | | 6.4 | 0.8 | | 6.2 | |

## 5.11 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | B-Port Supply Voltage (VCCB) | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| | | | | TYP | TYP | TYP | TYP | TYP | |
| $C_{pdA}$ (1) | A-port input, B-port output | Outputs enabled | $C_L$ = 0pF, f = 10MHz, $t_r = t_f$ = 1ns | 1 | 1 | 1 | 1.5 | 2 | pF |
| | | Outputs disabled | | 1 | 1 | 1 | 1 | 1 | |
| | B-port input, A-port output | Outputs enabled | | 12 | 12.5 | 13 | 14 | 15 | |
| | | Outputs disabled | | 1 | 1 | 1 | 1 | 1 | |
| $C_{pdB}$ (1) | A-port input, B-port output | Outputs enabled | $C_L$ = 0pF, f = 10MHz, $t_r = t_f$ = 1ns | 12 | 12.5 | 13 | 14 | 15 | pF |
| | | Outputs disabled | | 1 | 1 | 1 | 1 | 1 | |
| | B-port input, A-port output | Outputs enabled | | 1 | 1 | 1 | 1 | 2 | |
| | | Outputs disabled | | 1 | 1 | 1 | 1 | 1 | |

(1) Power dissipation capacitance per transceiver


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## 5.12 Typical Characteristics

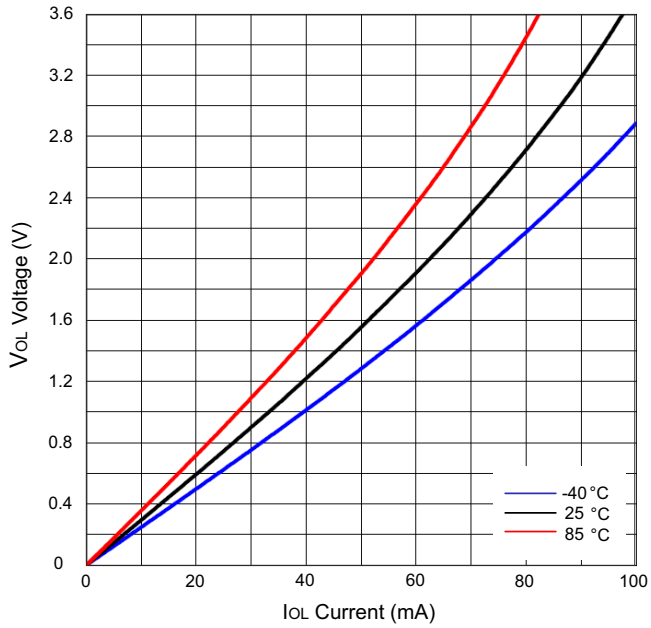



**Figure 5-1. Low-Level Output Voltage ($V_{OL}$) vs Low-Level Current ($I_{OL}$)**

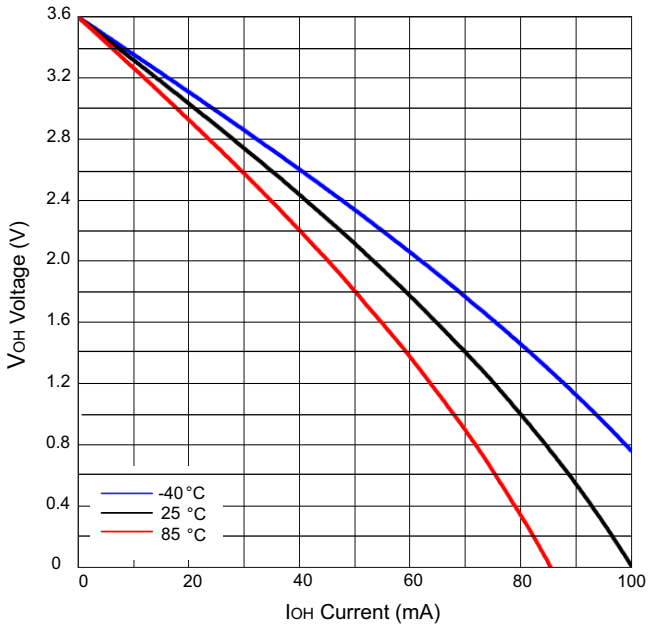
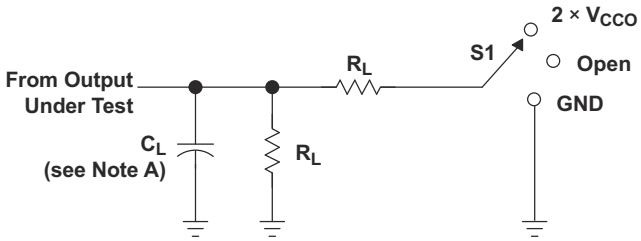



**Figure 5-2. High-Level Output Voltage ($V_{OH}$) vs High-Level Current ($I_{OH}$)**

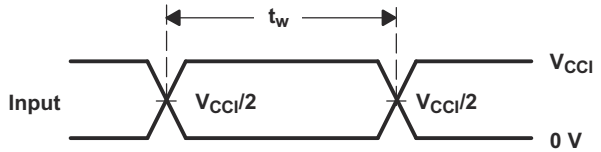
## 6 Parameter Measurement Information



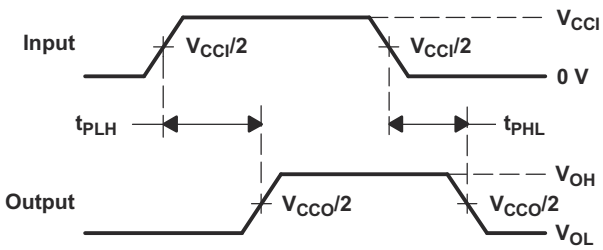

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CCO}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

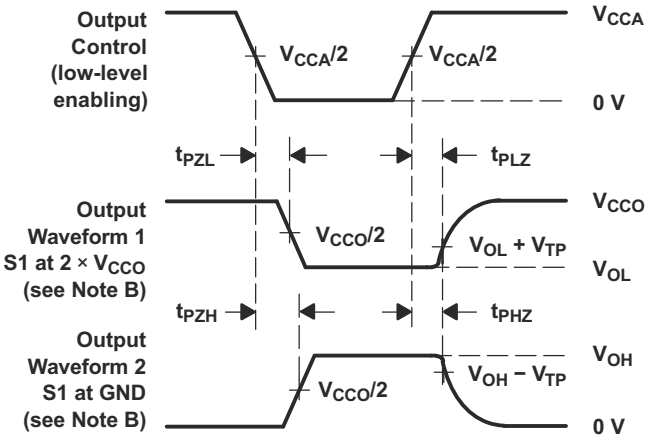
| $V_{CCO}$ | $C_L$ | $R_L$ | $V_{TP}$ |
|---|---|---|---|
| 1.2 V | 15 pF | 2 kΩ | 0.1 V |
| 1.5 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | 15 pF | 2 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 15 pF | 2 kΩ | 0.15 V |
| 3.3 V ± 0.3 V | 15 pF | 2 kΩ | 0.3 V |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, $Z_O$ = 50 Ω, dv/dt ≥ 1 V/ns, dv/dt ≥1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. $V_{CCI}$ is the $V_{CC}$ associated with the input port.
I. $V_{CCO}$ is the $V_{CC}$ associated with the output port.

**Figure 6-1. Load Circuit and Voltage Waveforms**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# 7 Detailed Description

## 7.1 Overview

The SN74AVCH4T245 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR,1 $\overline{OE}$, and 2 $\overline{OE}$) are supported by $V_{CCA}$, and Bx pins are supported by $V_{CCB}$. The A port can accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.2V to 3.6V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state. For more information, refer to the *AVC Logic Family Technology and Applications* application report.

## 7.2 Functional Block Diagram

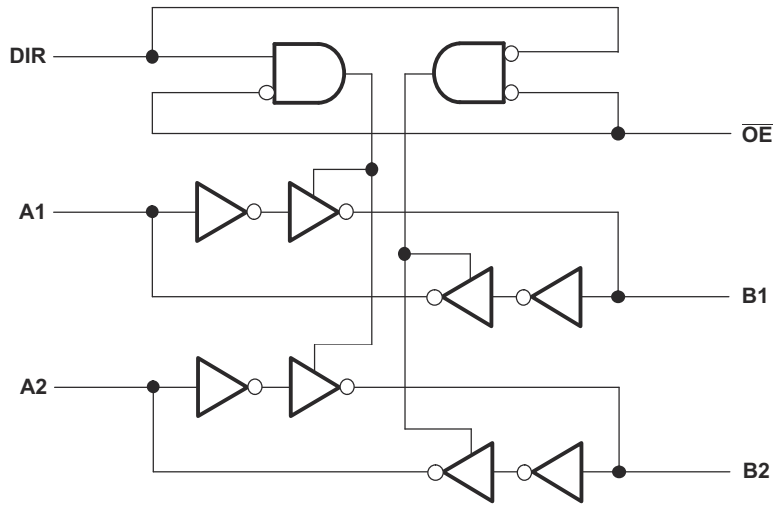


**Figure 7-1. Logic Diagram (Positive Logic) for 1/2 of SN74AVCH4T245**

## 7.3 Feature Description

### *7.3.1 Fully Configurable Dual-Rail Design*

Fully configurable dual-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range.

Both $V_{CCA}$ and $V_{CCB}$ can be supplied at any voltage between 1.2V and 3.6V; thus, making the device an excellent choice for translating between any of the low voltage nodes (1.2V, 1.8V, 2.5V, and 3.3V).

### *7.3.2 Supports High Speed Translation*

The SN74AVCH4T245 device can support high data rate applications. The translated signal data rate can be up to 380Mbps when the signal is translated from 1.8V to 3.3V.

### *7.3.3 $I_{off}$ Supports Partial-Power-Down Mode Operation*

$I_{off}$ will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

### *7.3.4 Bus-Hold Circuitry*

This device has active bus-hold circuitry that holds unused or undriven inputs at a valid logic state. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended (Refer to the *Bus-Hold Circuit* application report). Pullup and pulldown resistors are not recommended on the inputs of devices with bus-hold. Unused inputs can be left floating.

### *7.3.5 Vcc Isolation Feature*

The VCC isolation feature is designed so that if either $V_{CCA}$ or $V_{CCB}$ are at GND (or < 0.4V), both ports will be in a high-impedance state ($I_{OZ}$ shown in *Section 5.5*). This prevents false logic levels from being presented to either bus.

## 7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AVCH4T245.

**Table 7-1. Function Table (Each 2-Bit Section)**

| CONTROL INPUTS[1] | | OUTPUT CIRCUITS | | OPERATION |
|---|---|---|---|---|
| $\overline{OE}$ | DIR | A PORT | B PORT | |
| L | L | Enabled | Hi-Z | B data to A bus |
| L | H | Hi-Z | Enabled | A data to B bus |
| H | X | Hi-Z | Hi-Z | Isolation |

(1) Input circuits of the data I/Os are always active.


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# 8 Application and Implementation

## Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The SN74AVCH4T245 device can be used in level-shifting applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVCH4T245 device is an excellent choice for applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 380Mbps when device translates a signal from 1.8V to 3.3V.

## 8.2 Typical Application

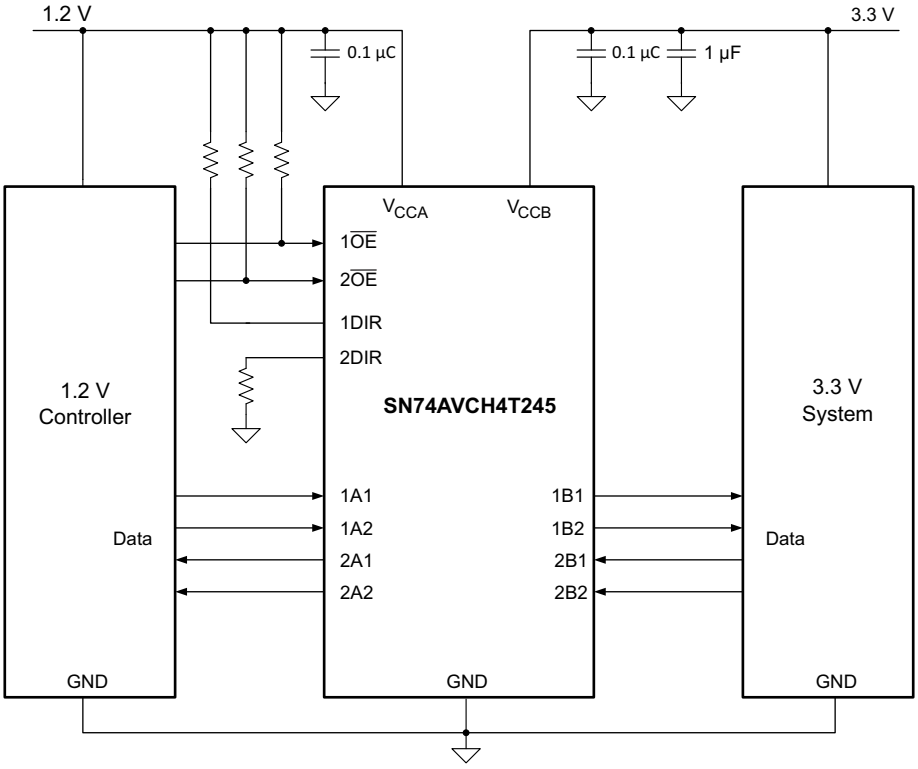


**Figure 8-1. Typical Application Diagram**

### 8.2.1 Design Requirements

For the design example shown in Section 8.2 use the parameters listed in Table 8-1.

**Table 8-1. Desgin Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 1.2V to 3.6V |
| Output voltage range | 1.2V to 3.6V |

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVCH4T245 device to determine the input voltage range. For a valid logic high, the value must exceed the $V_{IH}$ of the input port. For a valid logic low, the value must be less than the $V_{IL}$ of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVCH4T245 device is driving to determine the output voltage range.

### 8.2.3 Application Curve

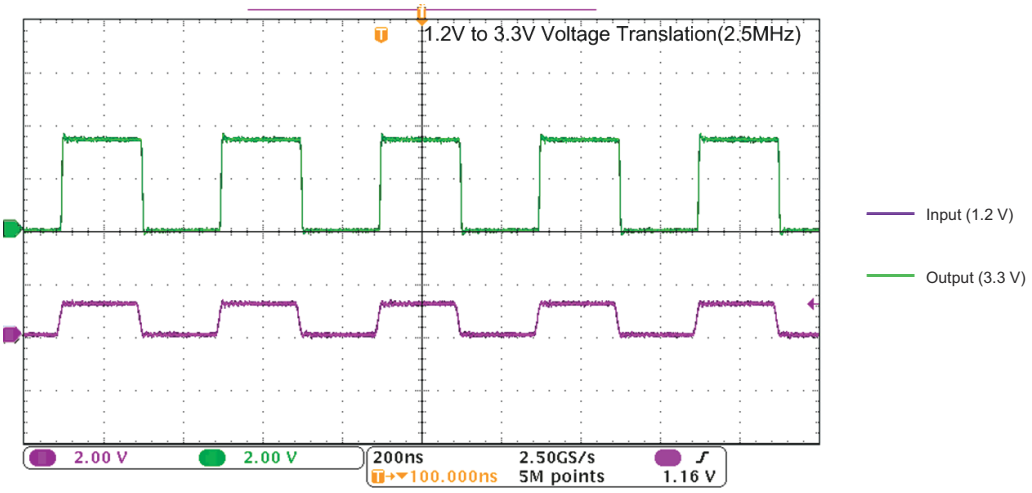


**Figure 8-2. Translation Up (1.2V to 3.3V) at 2.5MHz**

## 8.3 Power Supply Recommendations

The SN74AVCH4T245 device uses two separate configurable power-supply rails, $V_{CCA}$ and $V_{CCB}$. $V_{CCA}$ accepts any supply voltage from 1.2V to 3.6V, and $V_{CCB}$ accepts any supply voltage from 1.2V to 3.6V. The A port and B port are designed to track $V_{CCA}$ and $V_{CCB}$ respectively allowing for low voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by $V_{CCA}$, and all outputs are placed in the high-impedance state when the $\overline{OE}$ input is high. To put the outputs in the high-impedance state during power up or power down, the $\overline{OE}$ input pin must be tied to $V_{CCA}$ through a pull-up resistor and must not be enabled until $V_{CCA}$ and $V_{CCB}$ are fully ramped and stable. The current-sinking capability of the driver determines the minimum value of the pull-up resistor to $V_{CCA}$.

$V_{CCA}$ or $V_{CCB}$ can be powered up first. If the SN74AVCH4T245 is powered up in a permanently enabled state, pull-up resistors are recommended at the input. This allows for proper or glitch-free power-up. For more information, refer to *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters* application note.


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## 8.4 Layout

### 8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pull-up resistors to help adjust rise and fall times of signals, depending on the system requirements.

### 8.4.2 Layout Example

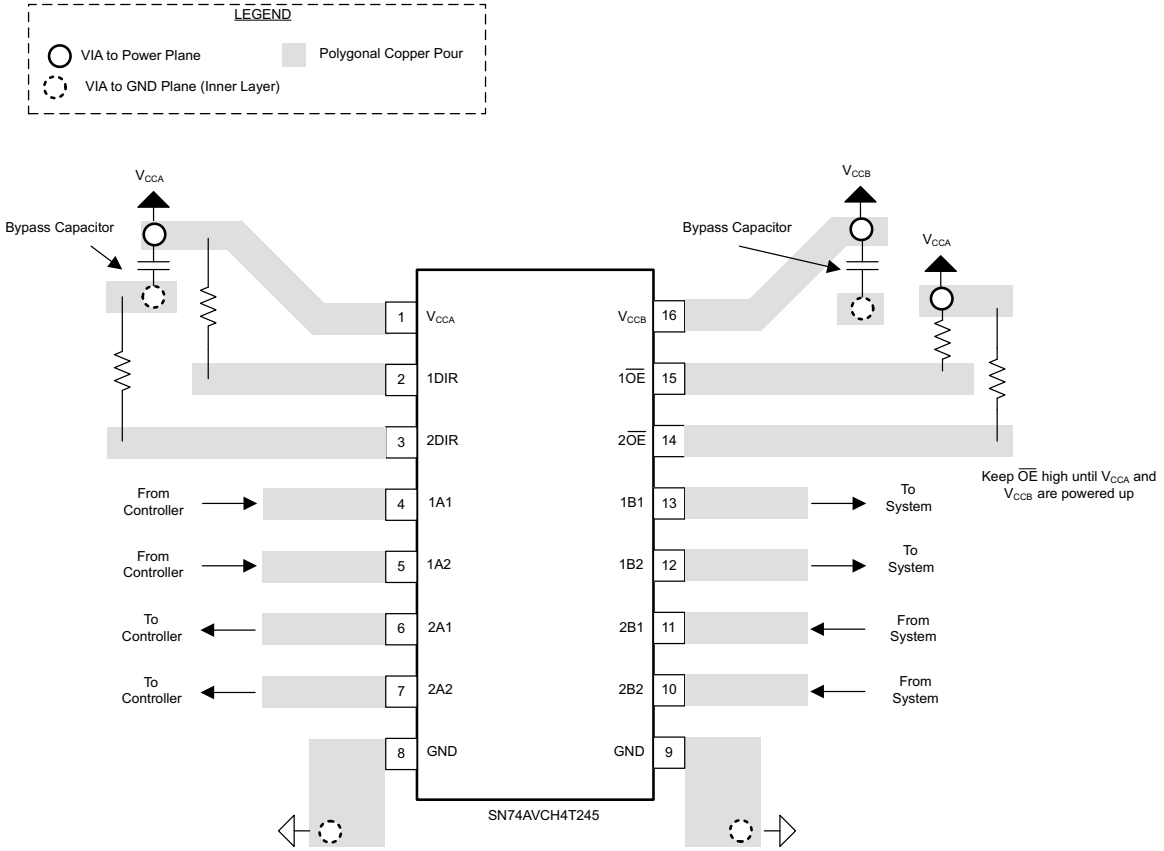


**Figure 8-3. Layout Recommendation**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters*
- Texas Instruments, *Bus-Hold Circuit*
- Texas Instruments, *AVC Logic Family Technology and Applications*

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (November 2015) to Revision F (February 2025) | Page |
|---|---|
| • Updated PW and RGY *Thermal Information* | 8 |

| Changes from Revision D (June 2007) to Revision E (November 2015) | Page |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Changed *Pin Functions* table | 4 |


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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 74AVCH4T245PWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| 74AVCH4T245PWTE4 | Active | Production | TSSOP (PW) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| 74AVCH4T245PWTG4 | Active | Production | TSSOP (PW) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| 74AVCH4T245RGYRG4 | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WS245 |
| 74AVCH4T245RGYRG4.A | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WS245 |
| 74AVCH4T245RGYRG4.B | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WS245 |
| 74AVCH4T245RSVR-NT | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| 74AVCH4T245RSVR-NT.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| 74AVCH4T245RSVR-NT.B | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| 74AVCH4T245RSVRG4 | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| 74AVCH4T245RSVRG4.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| 74AVCH4T245RSVRG4.B | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| SN74AVCH4T245D | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AVCH4T245 |
| SN74AVCH4T245D.B | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AVCH4T245 |
| SN74AVCH4T245DGVR | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245DGVR.B | Active | Production | TVSOP (DGV) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AVCH4T245 |
| SN74AVCH4T245DR.B | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AVCH4T245 |
| SN74AVCH4T245DT | Active | Production | SOIC (D) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AVCH4T245 |
| SN74AVCH4T245DT.B | Active | Production | SOIC (D) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AVCH4T245 |
| SN74AVCH4T245PW | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245PW.B | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245PWE4 | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245PWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245PWR.B | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245PWT | Active | Production | TSSOP (PW) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245PWT.B | Active | Production | TSSOP (PW) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WS245 |
| SN74AVCH4T245RGYR | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WS245 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AVCH4T245RGYR.A | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WS245 |
| SN74AVCH4T245RGYR.B | Active | Production | VQFN (RGY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WS245 |
| SN74AVCH4T245RSVR | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| SN74AVCH4T245RSVR.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |
| SN74AVCH4T245RSVR.B | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ZWV |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AVCH4T245 :**

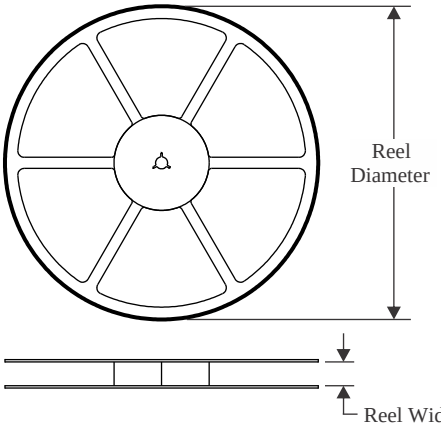
- Automotive : SN74AVCH4T245-Q1
- Enhanced Product : SN74AVCH4T245-EP

NOTE: Qualified Version Definitions:

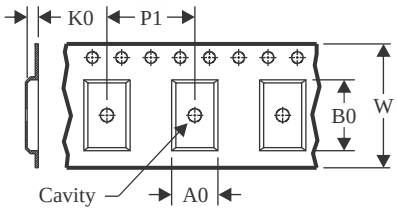
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

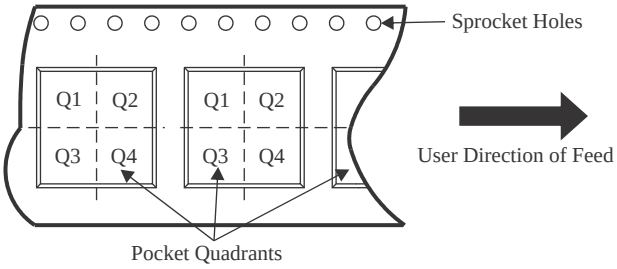



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

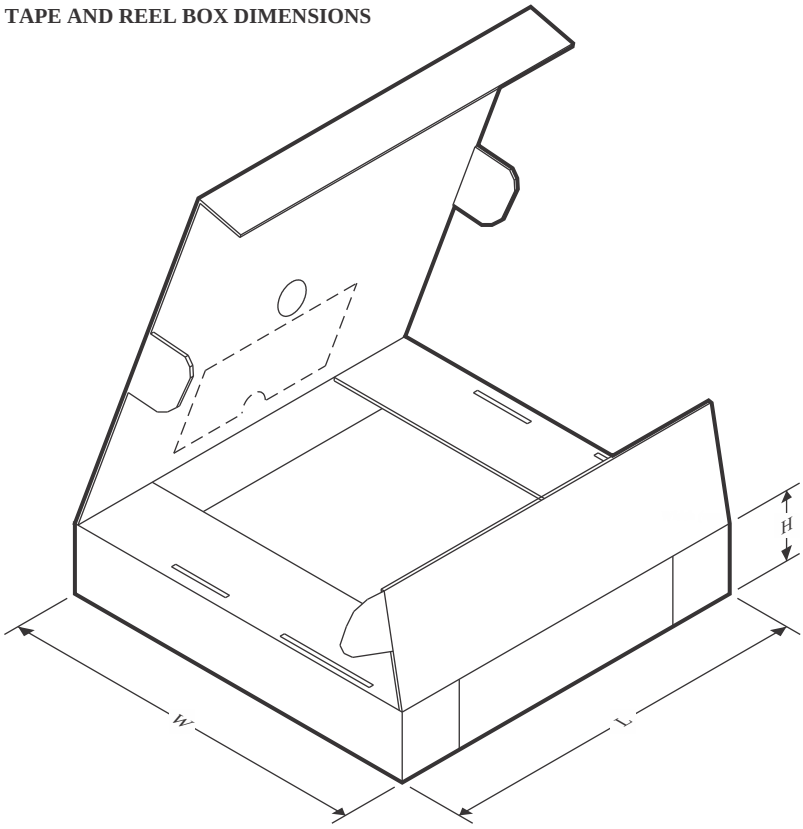
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AVCH4T245RGYRG4 | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| 74AVCH4T245RSVR-NT | UQFN | RSV | 16 | 3000 | 180.0 | 8.4 | 2.0 | 2.8 | 0.7 | 4.0 | 8.0 | Q1 |
| 74AVCH4T245RSVRG4 | UQFN | RSV | 16 | 3000 | 180.0 | 12.4 | 2.1 | 2.9 | 0.75 | 4.0 | 12.0 | Q1 |
| SN74AVCH4T245DGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AVCH4T245DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AVCH4T245PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AVCH4T245PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AVCH4T245RGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |
| SN74AVCH4T245RSVR | UQFN | RSV | 16 | 3000 | 180.0 | 12.4 | 2.1 | 2.9 | 0.75 | 4.0 | 12.0 | Q1 |

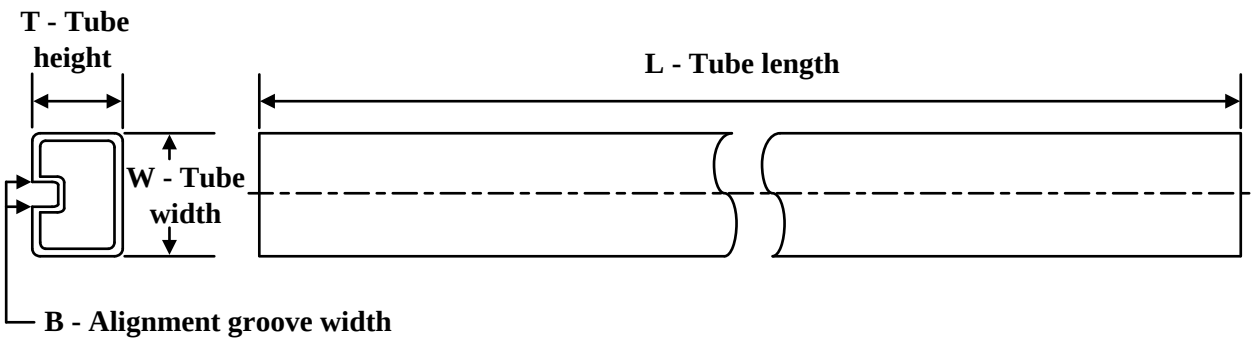
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74AVCH4T245RGYRG4 | VQFN | RGY | 16 | 3000 | 356.0 | 356.0 | 35.0 |
| 74AVCH4T245RSVR-NT | UQFN | RSV | 16 | 3000 | 200.0 | 183.0 | 25.0 |
| 74AVCH4T245RSVRG4 | UQFN | RSV | 16 | 3000 | 200.0 | 183.0 | 25.0 |
| SN74AVCH4T245DGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AVCH4T245DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74AVCH4T245PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AVCH4T245PWT | TSSOP | PW | 16 | 250 | 356.0 | 356.0 | 35.0 |
| SN74AVCH4T245RGYR | VQFN | RGY | 16 | 3000 | 356.0 | 356.0 | 35.0 |
| SN74AVCH4T245RSVR | UQFN | RSV | 16 | 3000 | 200.0 | 183.0 | 25.0 |

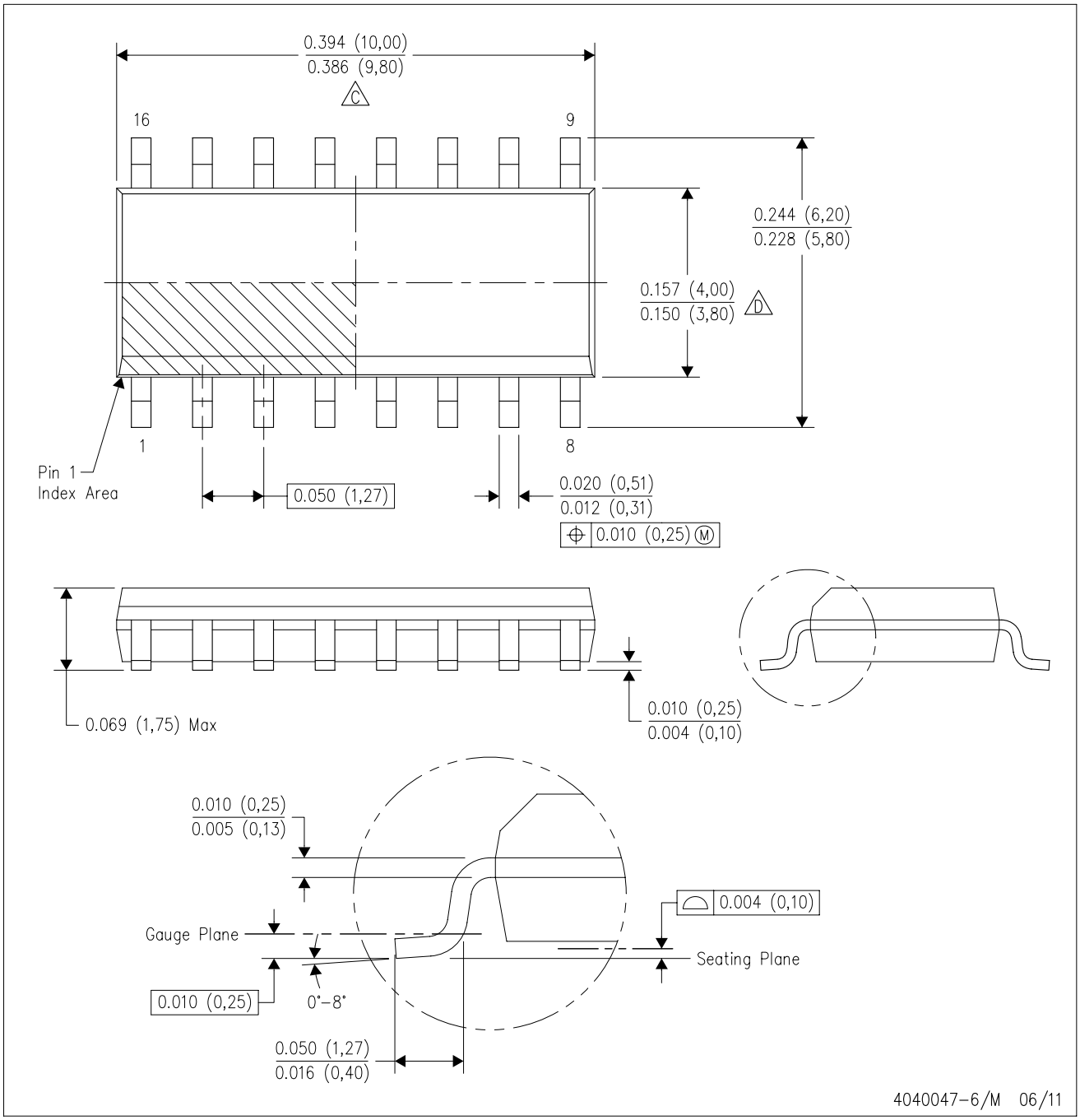
## TUBE




*All dimensions are nominal

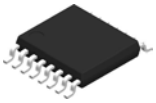
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74AVCH4T245D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74AVCH4T245D.B | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74AVCH4T245PW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74AVCH4T245PW.B | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74AVCH4T245PWE4 | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

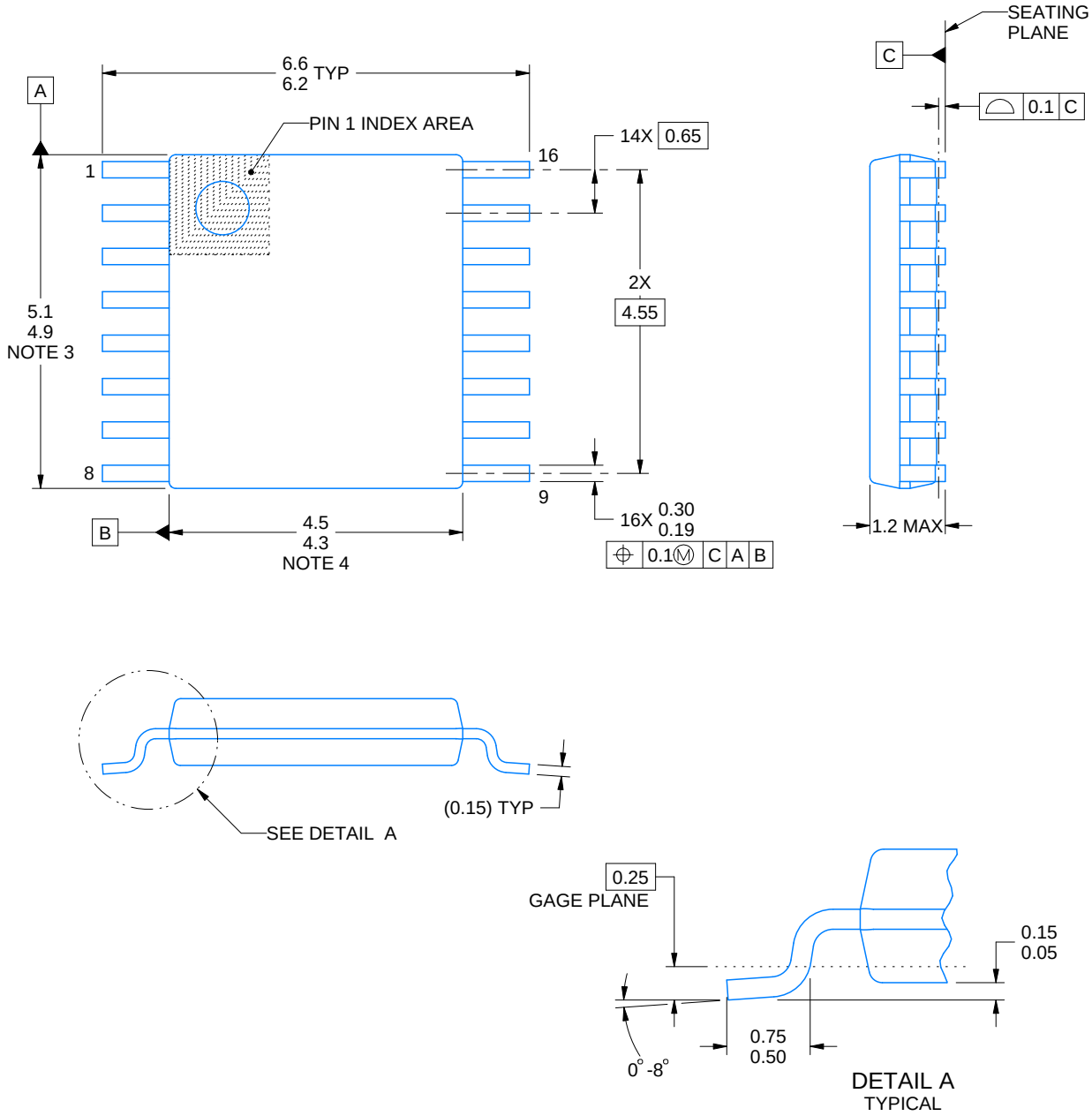
# PW0016A



# PACKAGE OUTLINE

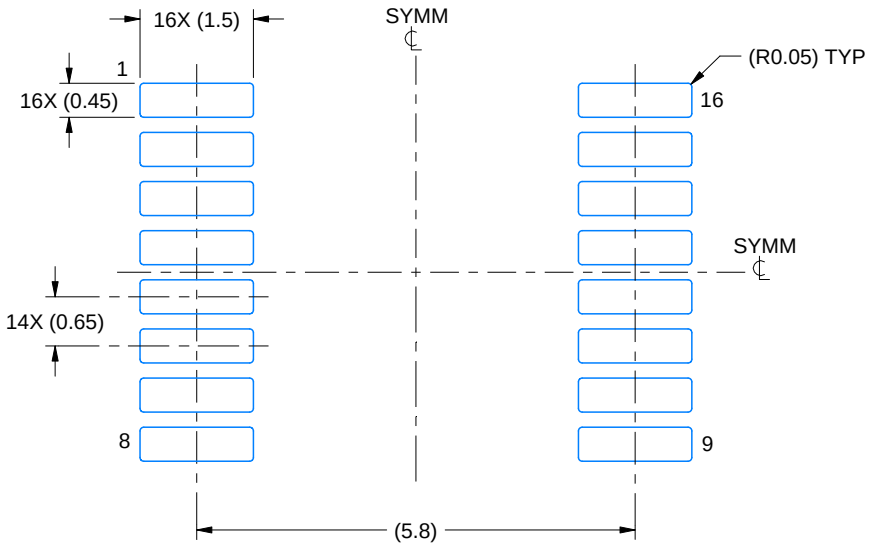
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

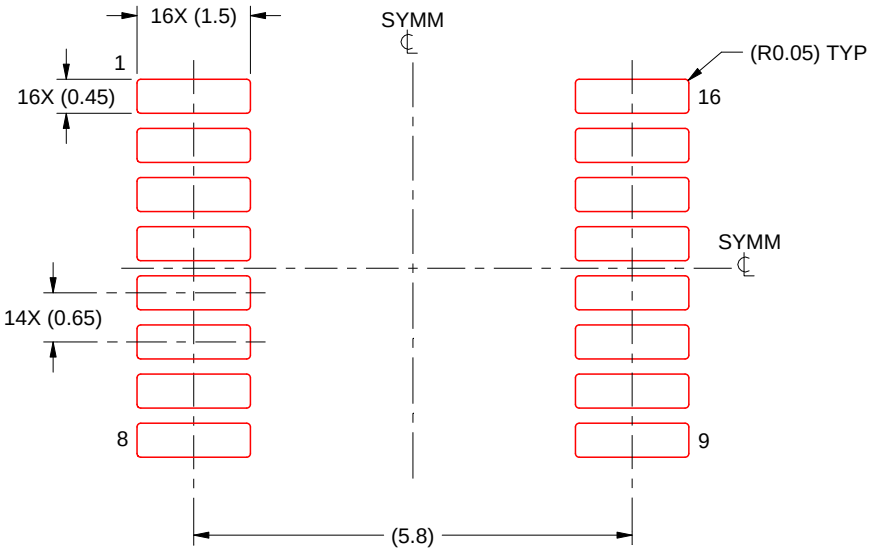
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

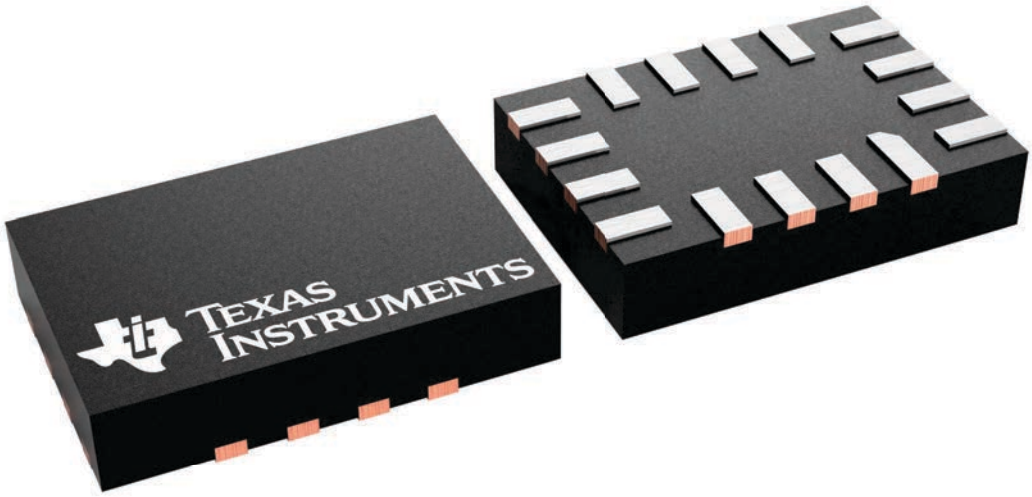
## RSV 16

## UQFN - 0.55 mm max height

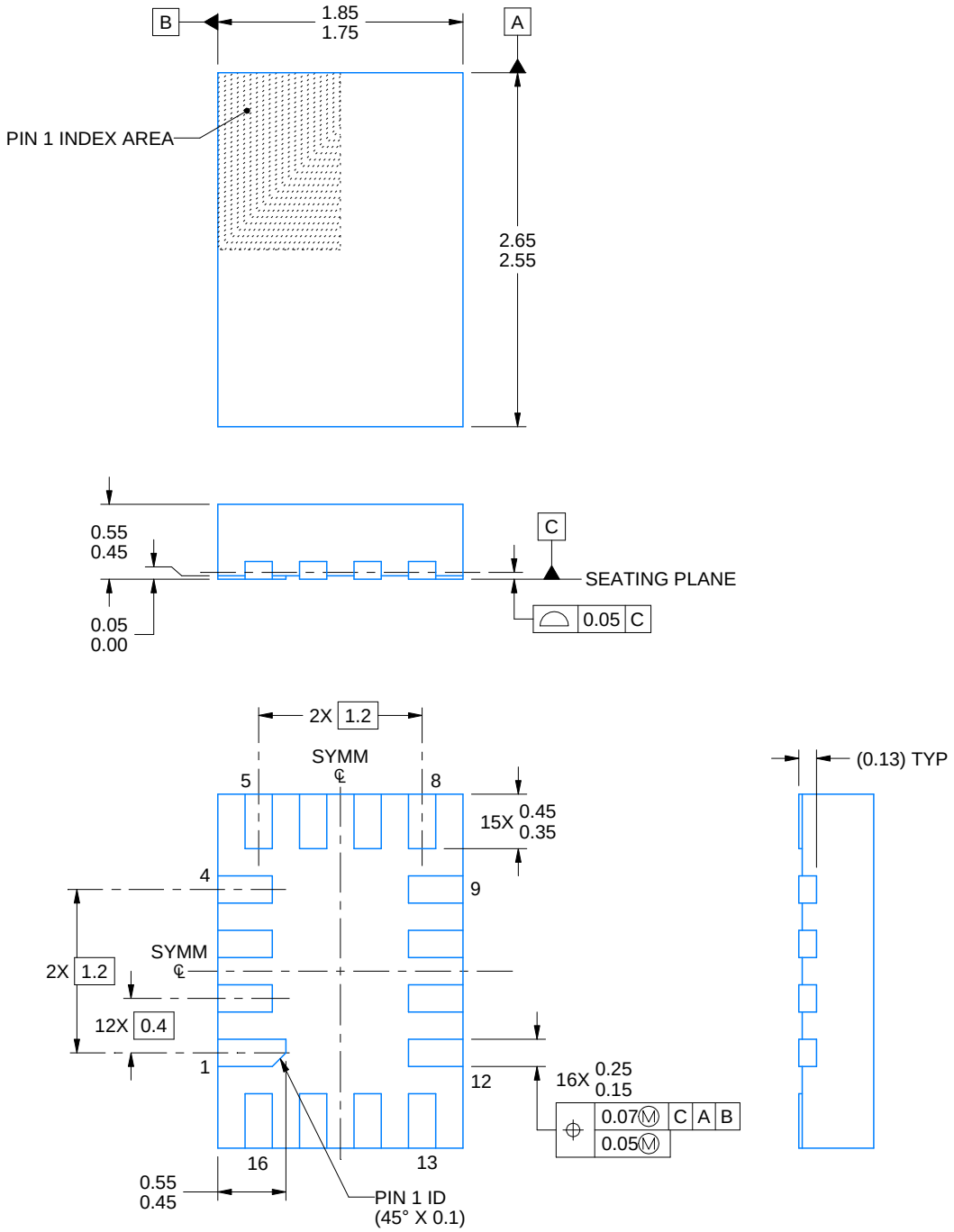
**1.8 x 2.6, 0.4 mm pitch**

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

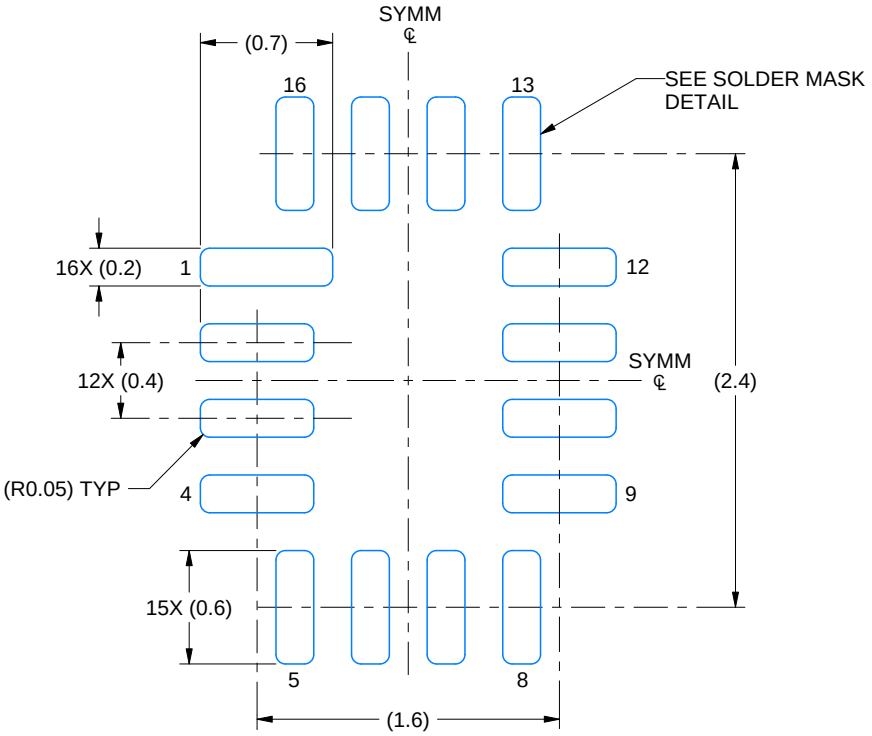



4231225/A

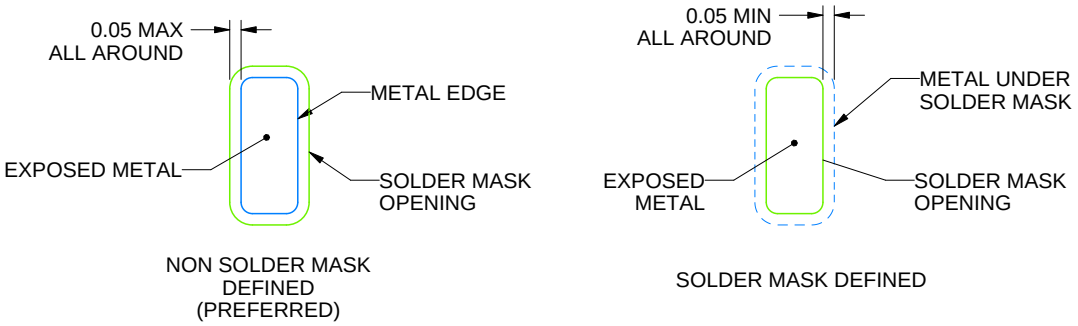



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

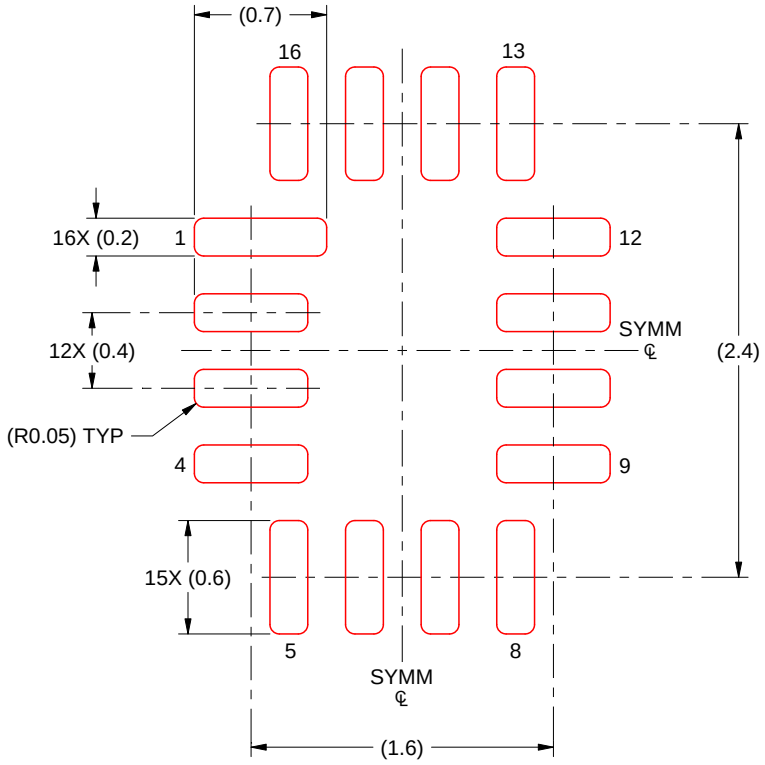



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



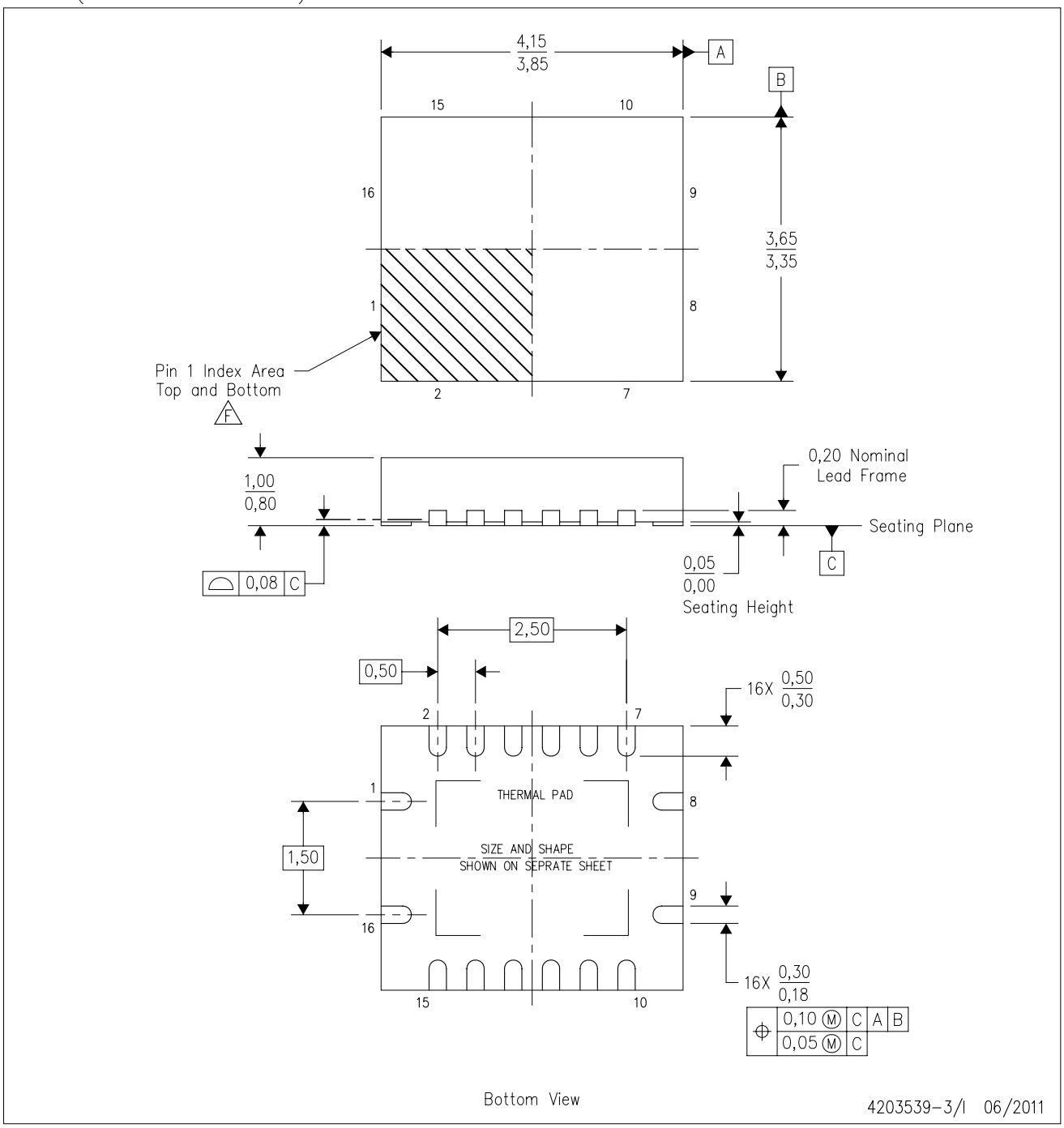

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD




NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

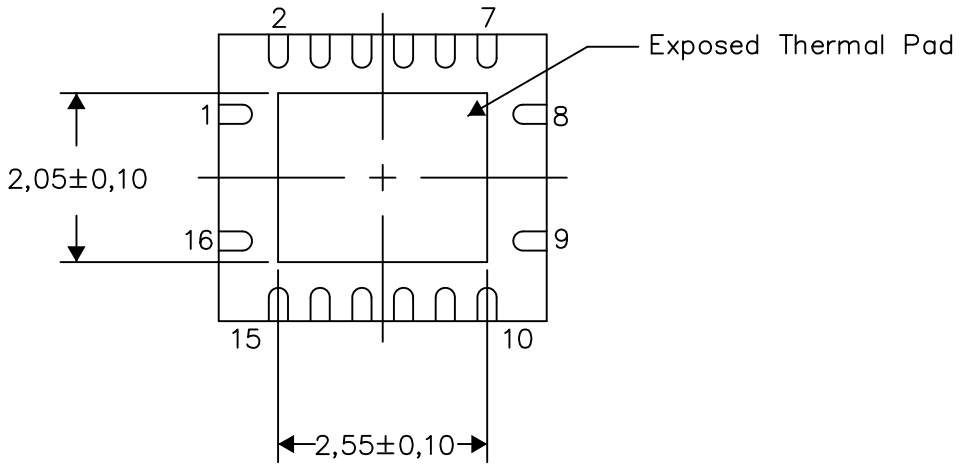
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



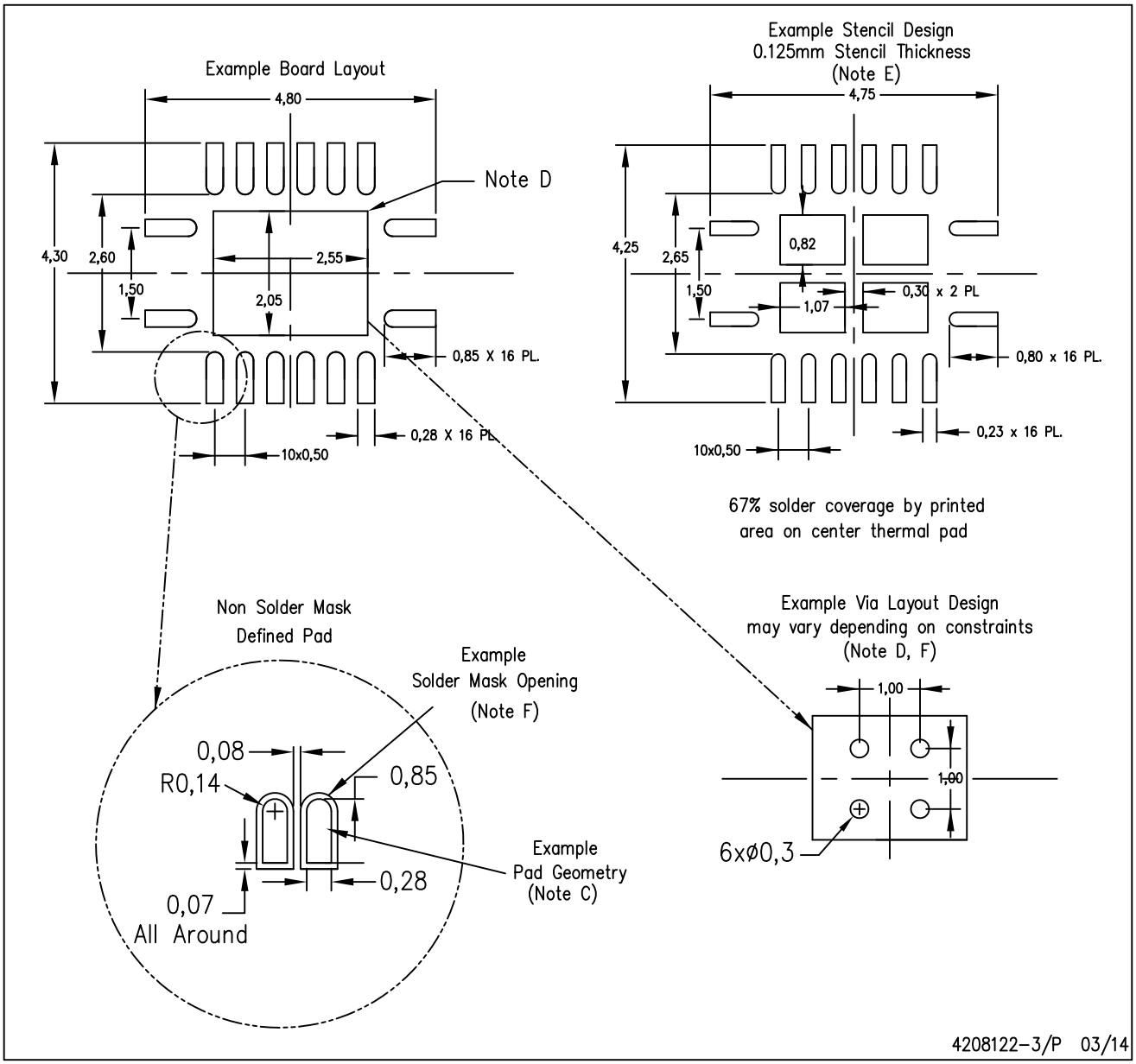

Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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