ADS5294 Octal-Channel 14-Bit 80-MSPS High-SNR and Low-Power ADC

1 Features

- Maximum Sample Rate: 80 MSPS/14-Bit
- High Signal-to-Noise Ratio
  - 75.5-dBFS SNR at 5 MHz / 80 MSPS
  - 78.2-dBFS SNR at 5 MHz / 80 MSPS and Decimation Filter Enabled
  - 84-dBc SFDR at 5 MHz / 80 MSPS
- Low Power Consumption
  - 58 mW/CH at 50 MSPS
  - 77 mW/CH at 80 MSPS (2-LVDS Wire Per Channel)
- Digital Processing Block
  - Programmable FIR Decimation Filter and Oversampling to Minimize Harmonic Interference
  - Programmable IIR High-Pass Filter to Minimize DC Offset
  - Programmable Digital Gain: 0 dB to 12 dB
  - 2-Channel or 4-Channel Averaging
- Flexible Serialized LVDS Outputs:
  - One or Two Wires of LVDS Output Lines Per Channel Depending on ADC Sampling Rate
  - Programmable Mapping Between ADC Input Channels and LVDS Output Pins-Eases Board Design
  - Variety of Test Patterns to Verify Data Capture by FPGA/Receiver
- Internal and External References
- 1.8-V Operation for Low Power Consumption
- Low-Frequency Noise Suppression
- Recovery From 6-dB Overload Within 1 Clock Cycle
- Package: 12-mm × 12-mm 80-Pin QFP

2 Applications

- Ultrasound and Sonar Imaging
- Communication Applications
- Multi-channel Data Acquisition

3 Description

The ADS5294 is a low-power 80-MSPS 8-Channel ADC that uses CMOS process technology and innovative circuit techniques. Low power consumption, high SNR, low SFDR, and consistent overload recovery allow users to design high-performance systems.

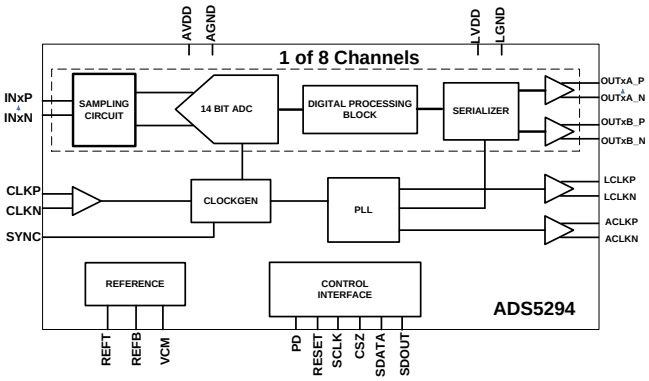
The digital processing block of the ADS5294 integrates several commonly used digital functions for improving system performance. The device includes a digital filter module that has built-in decimation filters (with lowpass, highpass and bandpass characteristics). The decimation rate is also programmable (by 2, by 4, or by 8). This rate is useful for narrow-band applications, where the filters are used to conveniently improve SNR and knock-off harmonics, while at the same time reducing the output data rate. The device includes an averaging mode where two channels (or even four channels) are averaged to improve SNR.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS5294	HTQFP (80)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2015) to Revision E	Page
• Added *The maximum limit used for the LVDD current at –40°C is 132 mA* table note	12
• Added bypass decimation values to the DATA_RATE, FILTERn_RATE, and FILTERn_COEFF_SET columns	33
• Changed D15 value of ADDR. (HEX) 28 to X	41
• Changed *this* to *the byte-wise* for clarification	41
• Changed *this* to *the word-wise* for clarification	41
• Changed D15 value to *1* in *Bit-Byte-Word Wise Output* table	48
• Added DATA_RATE>, FILTERn_RATE, and FILTERn_COEFF_SET values to the bypass decimation row in the *Digital Filters* table	55

Changes from Revision C (September 2013) to Revision D	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added "Sonar Imaging" in Applications	1
• Updated Pinout.	7
• Added text note 2 to Figure 1	17
• Added a text note to Figure 44.	30

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- Corrected typo in Table 1 33
- Added note to EN_2WIRE bit. 44
- Corrected typo in Table 17 55

Changes from Revision B (July 2012) to Revision C **Page**

- Added cross-reference link for VCM pin. 7
- Added note for REFB pin under INT/EXT reference modes. 8
- Added note for REFT pin under INT/EXT reference modes. 8
- Changed the maximum rating of digital input pins RESET, SCLK, SDATA, SYNC, PD, CSZ to 3.6V. 9
- Added test condition "Digital Filter Disabled" and changed "LVDS output rate" to "ADC CLK Frequency" in LVDS Timing at Different Sampling Frequencies — 2-Wire Interface, 7x-Serialization, Digital Filter Disabled 14
- Added test condition "Digital Filter Disabled" and changed "LVDS output rate" to "ADC CLK Frequency" in LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Digital Filter Disabled 14
- Added note after LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Digital Filter Disabled : *The above LVDS timing spec is only valid when digital filters are disabled*... 14
- Added LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 2 Filter Enabled 16
- Added LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 4 Filter Enabled 16
- Added LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 8 Filter Enabled 16
- Added a note related to EN_CUSTOM_FILT and changed formats in Table 9. 33
- Added PLL Operation Versus LVDS Timing before *APPLICATION INFORMATION* section 35
- Added a note link to Reg.0x38 44
- Changed 0xF[15] to 0xF0[15] in the description of Reg.0x42. 44
- Changed the Reg.0x46[11:8] formatting. 44
- Corrected the EN_RAMP address from 0x24 to 0x25 in the section of LVDS test patterns. 47
- Changed "Note that these bits are functional only when the GLOBAL_EN_FILTER gets set to 1" to " Note that these bits are functional only when the GLOBAL_EN_FILTER gets set to 1 and USE_FILTERn bit is set to 1” in the section of Decimation Filter,. 54
- Added a note related to EN_CUSTOM_FILT and changed formats inTable 17 55
- Changed Equation (5). 59
- Added register address in Table 23. 59
- Revised Figure 63 and moved the 2pF cap to the left hand side of the resistors. 66
- Added a note regarding the location of LVDS Rterm in the section of Input clock. 67

Changes from Revision A (November 2011) to Revision B **Page**

- Changed the location of OUT A and OUT B in Figure 5 and Figure 6. 20
- Added Figure 45 31
- Replaced Table 9 (Decimation Filter Modes) with new Table 1 - Digital Filters. 33
- Deleted section: Synchronization Pulse 35
- Added EN_HIGH_ADDRS to Table 3. 40
- Moved EN_EXT_REF From: 0x0F To: 0xF0 in Table 3 45
- Added the section BIT-BYTE-WORD WISE OUTPUT. Added Figure 53 and Figure 54. 48
- Added section DIGITAL PROCESSING BLOCKS 49
- Replaced Table 5 and Table 6 with new Table 17 - Digital Filters. 55
- Changed the SYNCHRONIZATION PULSE section 58

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- Added the External Reference Mode of Operation section 59

Changes from Original (November 2011) to Revision A **Page**

- Changed From: Product Preview To: Production 1

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5 Description (continued)

Serial LVDS outputs reduce the number of interface lines and enable the highest system integration. The digital data from each channel ADC is output over one or two wires of LVDS output lines depending on the ADC sampling rate. This 2-wire interface maintains a low serial-data rate, allowing low-cost FPGA-based receivers to be used even at a high sample rate. The ADC resolution is programmed to 12-bit or 14-bit through registers. A unique feature is the programmable-mapping module that allows flexible mapping between the input channels and the LVDS output pins. This module greatly reduces the complexity of LVDS-output routing, and by reducing the number of PCB layers, potentially results in cheaper system boards.

The device integrates an internal reference trimmed to accurately match across devices. Internal reference mode achieves the best performance. External references can also drive the device.

The device is available in a 12-mm × 12-mm 80-pin QFP package. The device is specified over a –40°C to 85°C operating temperature range. ADS5294 is completely pin-to-pin and register compatible to ADS5292.

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6 Device Comparison Table

DEVICE	DESCRIPTION	PACKAGE	BODY SIZE (NOM)
ADS5294	Octal-channel, 14-bit, 80-MSPS ADC, 75-dBFS SNR, 77 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5292	Octal-channel, 12-bit, 80-MSPS ADC, 70-dBFS SNR, 66 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5295	Octal-channel, 12-bit, 100-MSPS ADC, 70.6-dBFS SNR, 80 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
ADS5296A	10-bit, 200-MSPS, 4-channel, 61-dBFS SNR, 150-mW/ch and 12-bit, 80-MSPS, 8-channel, 70-dBFS SNR, 65-mW/ch ADC	VQFN (64)	9.00 mm × 9.00 mm
AFE5801	8-channel variable-gain amplifier (VGA) with octal high-speed ADC, 5.5 nV/√Hz, 12 bits, 65 MSPS, 65 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
AFE5803	8-channel AFE, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5804	8-channel AFE, 1.23 nV/√Hz, 12 bits, 50 MSPS, 101 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5805	8-channel AFE, 0.85 nV/√Hz, 12 bits, 50 MSPS, 122 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5807	8-channel AFE with passive CW mixer, 1.05 nV/√Hz, 12 bits, 80 MSPS, 117 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5808A	8-channel AFE with passive CW mixer, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5809	8-channel AFE with passive CW mixer, and digital I/Q demodulator, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 158 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5812	Fully integrated, 8-channel AFE with passive CW mixer, and digital I/Q demodulator, 0.75 nV/√Hz, 14 and 12 bits, 65 MSPS, 180 mW/ch	NFBGA (135)	15.00 mm × 9.00 mm
AFE5818	16-Channel AFE with 124-mW/Channel, 0.75-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer	NFBGA (289)	15.00 mm × 15.00 mm
AFE5816	16-channel AFE with 90-mW/channel, 1-nV/√Hz noise, 14-bit, 65-MSPS or 12-bit, 80-MSPS ADC and passive CW mixer	NFBGA (289)	15.00 mm × 15.00 mm
AFE5851	16-channel VGA with high-speed ADC, 5.5 nV/√Hz, 12 bits, 32.5 MSPS, 39 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
VCA8500	8-channel, ultralow-power VGA with low-noise pre-amp, 0.8 nV/√Hz, 65 mW/ch	VQFN (64)	9.00 mm × 9.00 mm
VCA5807	8-channel voltage-controlled amplifier with passive CW mixer, 0.75 nV/√Hz, 99 mW/ch	HTQFP (80)	14.00 mm × 14.00 mm
PGA5807A	Integrated 8-channel AFE with LNA, PGA, and LPF,2.1 nV/√Hz, 60 mW/ch	VQFN (64)	9.00 mm × 9.00 mm

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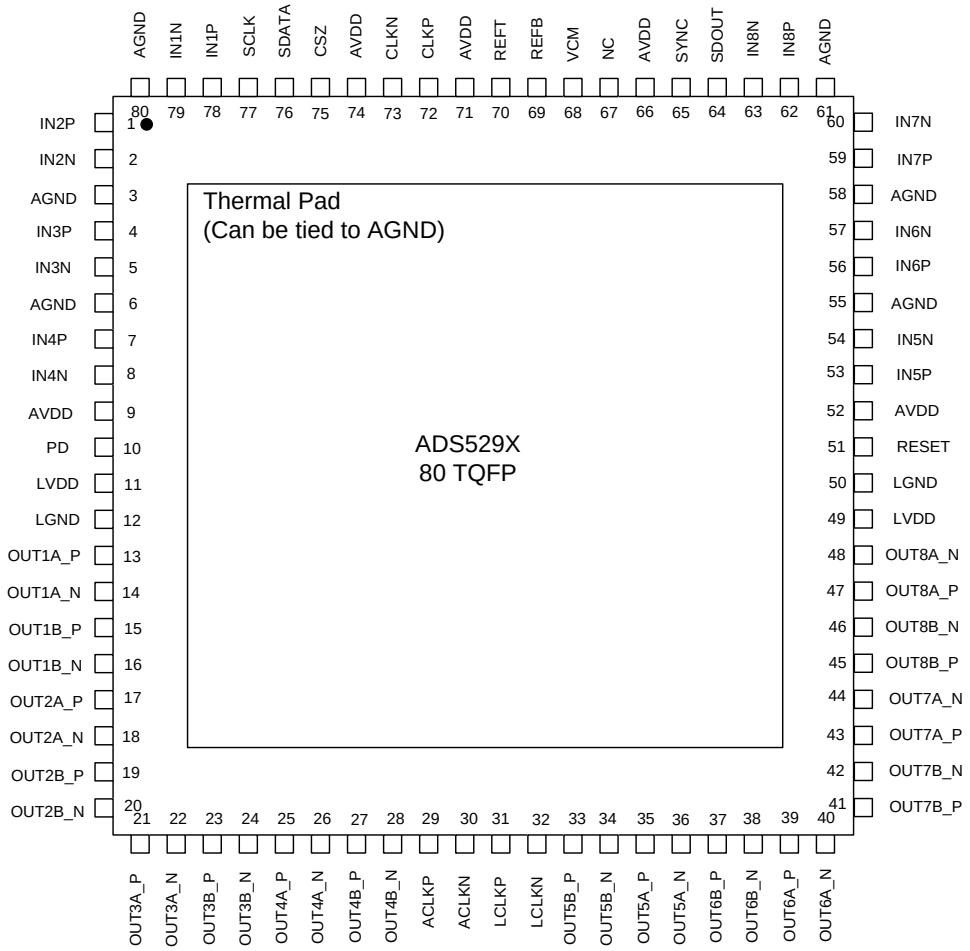
7 Pin Configuration and Functions

PFP Package
80-PIN TQFP With Thermal Pad
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AVDD	9, 52, 66, 71, 74	Analog power supply, 1.8 V
AGND	3, 6, 55, 58, 61, 80	Analog ground
VCM	68	Common-mode output pin, 0.95-V output. This pin can be configured as the external reference voltage (1.5 V) input pin as well. See Reg 0x42 and *External Reference Mode of Operation*.
CLKN	73	Negative differential clock –Tie CLKN to GND for single-ended clock
CLKP	72	Positive differential clock
IN1P, IN1N	78, 79	Differential input signal, Channel 1
IN2P, IN2N	1, 2	Differential input signal, Channel 2
IN3P, IN3N	4, 5	Differential input signal, Channel 3
IN4P, IN4N	7, 8	Differential input signal, Channel 4
IN5P, IN5N	53, 54	Differential input signal, Channel 5
IN6P, IN6N	56, 57	Differential input signal, Channel 6
IN7P, IN7N	59, 60	Differential input signal, Channel 7
IN8P, IN8N	62, 63	Differential input signal, Channel 8
LCLKP, LCLKN	31, 32	Differential LVDS bit clock (7X)
ACLKP, ACLKN	29, 30	Differential LVDS frame clock (1X)

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Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
OUT1A_P, OUT1A_N	13, 14	Differential LVDS data output, wire 1, channel 1
OUT1B_P, OUT1B_N	15, 16	Differential LVDS data output, wire 2, channel 1
OUT2A_P, OUT2A_N	17, 18	Differential LVDS data output, wire 1, channel 2
OUT2B_P, OUT2B_N	19, 20	Differential LVDS data output, wire 2, channel 2
OUT3A_P, OUT3A_N	21, 22	Differential LVDS data output, wire 1, channel 3
OUT3B_P, OUT3B_N	23, 24	Differential LVDS data output, wire 2, channel 3
OUT4A_P, OUT4A_N	25, 26	Differential LVDS data output, wire 1, channel 4
OUT4B_P, OUT4B_N	27, 28	Differential LVDS data output, wire 2, channel 4
OUT5A_P, OUT5A_N	35, 36	Differential LVDS data output, wire 1, channel 5
OUT5B_P, OUT5B_N	33, 34	Differential LVDS data output, wire 2, channel 5
OUT6A_P, OUT6A_N	39, 40	Differential LVDS data output, wire 1, channel 6
OUT6B_P, OUT6B_N	37, 38	Differential LVDS data output, wire 2, channel 6
OUT7A_P, OUT7A_N	43, 44	Differential LVDS data output, wire 1, channel 7
OUT7B_P, OUT7B_N	41, 42	Differential LVDS data output, wire 2, channel 7
OUT8A_P, OUT8A_N	47, 48	Differential LVDS data output, wire 1, channel 8
OUT8B_P, OUT8B_N	45, 46	Differential LVDS data output, wire 2, channel 8
PD	10	Power-down control input. Active High. The pin has an internal 220-kΩ pulldown resistor.
REFB	69	Negative reference input and output. Internal reference mode: Reference bottom voltage (0.45 V) is output on this pin. A decoupling capacitor is not required on this pin. External reference mode: Reference bottom voltage (0.45 V) must be externally applied to this pin. Please see *External Reference Mode of Operation*.
REFT	70	Positive reference input and output. Internal reference mode: Reference top voltage (1.45 V) is output on this pin. A decoupling capacitor is not required on this pin. External reference mode: Reference top voltage (1.45 V) must be externally applied to this pin. Please see *External Reference Mode of Operation*.
RESET	51	Active HIGH RESET input. The pin has an internal 220-kΩ pulldown resistor.
SCLK	77	Serial clock input. The pin has an internal 220-kΩ pulldown resistor.
SDATA	76	Serial data input. The pin has an internal 220-kΩ pulldown resistor.
SDOUT	64	Serial data readout. This pin is in the high-impedance state after reset. When the <READOUT> bit is set, the SDOUT pin becomes active. SDOUT is a CMOS digital output running from the AVDD supply.
CSZ	75	Serial enable chip select – active-low digital input
SYNC	65	Input signal to synchronize channels and chips when used with reduced output data rates. If it is not used, add a ≤ 10-KΩ pulldown resistor.
LVDD	11, 49	Digital and I/O power supply, 1.8 V
LGND	12, 50	Digital ground
NC	67	No Connection. Must leave floated

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	AVDD	–0.3	2.2	V
	LVDD	–0.3	2.2	V
Voltage	Between AGND and LGND	–0.3	0.3	V
	At analog inputs	–0.3	min[2.2, AVDD+0.3]	V
	At digital inputs, RESET, SCLK, SDATA, SYNC, PD, CSZ	–0.3	3.6	V
	At CLKN, CLKP[2],	–0.3	min[2.2, AVDD+0.3]	V
	At digital outputs	–0.3	min[2.2, LVDD+0.3]	V
Maximum junction temperature (T_J), any condition			105	°C
Operating temperature		–40	85	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) When AVDD is turned off, TI recommends to switch off the input clock (or ensure the voltage on CLKP, CLKN is < |0.3V|). This prevents the ESD protection diodes at the clock input pins from turning on.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
LVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS/OUTPUTS						
	Differential input voltage range			2		V_{PP}
	Input common-mode voltage			0.95 ± 0.05		V
REF_T	External reference mode			1.45		V
REF_B	External reference mode			0.45		V
VCM	Common-mode voltage output			0.95		V
	External Reference mode Input			1.5		V
	Maximum Input Frequency (1)	2 V_{PP} amplitude		80		MHz
CLOCK INPUTS						
	ADC Clock input sample rate		10		80	MSPS
	Input Clock amplitude differential ($V_{(CLKP)}$ – $V_{(CLKN)}$) peak-to-peak	Sine wave, AC-coupled	0.2	1.5		V_{PP}
		LVPECL, AC-coupled	0.2	1.6		
		LVDS, AC-coupled	0.2	0.7		
V_{IL}	Input Clock CMOS single-ended ($V_{(CLKP)}$)			<0.3		V
V_{IH}				>1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
	ACLKP and ACLKN outputs (LVDS), 1-wire interface			1x (sample rate)		MSPS
	LCLKP and LCLKN outputs (LVDS), 1-wire interface			7x (sample rate)		MSPS
	ACLKP and ACLKN outputs (LVDS), 2-wire interface			0.5x (sample rate)		MSPS
	LCLKP and LCLKN outputs (LVDS), 2-wire interface			3.5x (sample rate)		MSPS
	Maximum data rate, 2-wire interface			560		Mbps
	Maximum data rate, 1-wire interface			700		Mbps
C_{LOAD}	Maximum external capacitance from each output pin to LGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs			100		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) See the *Large and Small Signal Input Bandwidth* section.

8.4 Thermal Information

THERMAL METRIC (1)		ADS5294 PFP (HTQFP) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics Dynamic Performance

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, Sample rate = 80 MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SNR	Signal-to-noise ratio	f_{in} = 10 MHz, 65 MSPS			75.6		dBFS
		f_{in} = 5 MHz, T_A = 25°C		72.8	75.5		dBFS
		f_{in} = 5 MHz, Across temperatures		71.8			dBFS
		f_{in} = 5 MHz, -60 dBFS Input signal amplitude			77.3		dBFS
		f_{in} = 5 MHz, Decimation by two enabled			78.2		dBFS
		f_{in} = 30 MHz			74.2		dBFS
		f_{in} = 65 MHz			71.7		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{in} = 5 MHz			74.8		dBFS
		f_{in} = 30 MHz			73.4		dBFS
		f_{in} = 65 MHz			70		dBFS
ENOB	Effective number of bits	f_{in} = 5 MHz			12.2		Bits
DNL	Differential nonlinearity	f_{in} = 5 MHz		–0.96	±0.5	1.7	LSB
INL	Integral nonlinearity	f_{in} = 5 MHz			2.2	5.5	LSB
SFDR	Spurious-free dynamic range	f_{in} = 5 MHz		72	84		dBc
		f_{in} = 30 MHz			81		dBc
		f_{in} = 65 MHz			74		dBc
THD	Total harmonic distortion	f_{in} = 5 MHz		70.5	82		dBc
		f_{in} = 30 MHz			80		dBc
		f_{in} = 65 MHz			73.5		dBc
HD2	Second-harmonic distortion	f_{in} = 5 MHz		73	93		dBc
		f_{in} = 30 MHz			88		dBc
		f_{in} = 65 MHz			85		dBc
HD3	Third-harmonic distortion	f_{in} = 5 MHz		72	84		dBc
		f_{in} = 30 MHz			81		dBc
		f_{in} = 65 MHz			74		dBc
	Worse spur excluding HD2, HD3	f_{in} = 5 MHz			91		dBc
		f_{in} = 30 MHz			83		dBc
		f_{in} = 65 MHz			76		dBc
IMD3	Intermodualtion distortion	f_{in} = 8 MHz at –7 dBFS, f_2 = 10 MHz at –7 dBFS			84.5		dBc
	Overload recovery	Recovery to within 1% of full-scale for 6-dB overload with sine wave input			1		Clock Cycle
XTALK	Cross-talk	f_{in} = 10 MHz, –1-dBFS signal applied on aggressor channel no signal applied on victim channel	far channel		90		dBc
			near channel		85		dBc
	Phase noise	5 MHz, 1-kHz off carrier			–138		dBc/Hz
ANALOG INPUT / OUTPUT							
	Differential input voltage range (0-dB gain)				2		V_{PP}
R_{IN}	Differential Input Resistance	At DC			2		kΩ
C_{IN}	Differential Input Capacitance	At DC			3.2		pF
	Analog input bandwidth	With a 50-Ω source impedance			550		MHz
	Analog input common-mode current (per input pin)				1.6		µA/MSPS
	VCM common-mode output voltage				0.95		V
	VCM output current capability				5		mA

Electrical Characteristics Dynamic Performance (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, Sample rate = 80 MSPS, ADC is configured in internal reference mode (unless otherwise noted). MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V.

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Offset error	Across devices and across channels within a device	–15		15	mV
	Temperature coefficient of offset error			< 0.01		mV/ °C
$E_{(GREF)}$	Gain error due to internal reference inaccuracy alone	Across devices	–2		2	%FS
$E_{(GCHAN)}$	Gain error of channel alone			0.5		%FS
	Temperature coefficient of $E_{(GCHAN)}$			< 0.01		%FS/ °C
POWER SUPPLY						
	Power consumption	80 MSPS, 14 Bit, 2-wire LVDS		77		mW/CH
		50 MSPS, 1 wire LVDS		58		mW/CH
		40 MSPS, 14 Bit, 1-wire LVDS		52		mW/CH
		10 MSPS, 14 Bit, 1-wire LVDS		33		mW/CH
		f_{in} = 10 MHz, 80 MSPS, 14 Bit, Decimation filter = 2, 1-wire LVDS		100		mW/CH
AVDD		14 Bit, 80 MSPS		230	265	mA
		14 Bit, 65 MSPS		200		mA
		14 Bit, 40 MSPS		155		mA
LVDD		80 MSPS, 14 Bit, 2-wire LVDS (1)		111	122	mA
		50 MSPS, 14 Bit, 1-wire LVDS		80		mA
		40 MSPS, 14 Bit, 1-wire LVDS		73		mA
		80 MSPS, 1 Bit, Decimation filter = 2, 1-wire LVDS		210		mA
	Power-down power consumption	Partial Power Down (80 MSPS, 2-wire)		175		mW
		Complete Power Down			60	mW
	Power supply modulation ratio	Carrier = 5 MHz, $f_{(PSRR)}$ = 10 kHz, 50 mVpp on AVDD		35		dB
	Power supply rejection ratio	AC power supply rejection ratio f = 10 kHz		55		dB

(1) The maximum limit used for the LVDD current at –40°C is 132 mA.

8.6 Digital Characteristics

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 1.8 V, LVDD = 1.8 V

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage	All digital inputs support 1.8-V and 3.3-V CMOS logic levels.	1.3			V
V_{IL}	Logic low input voltage				0.4	V
I_{IH}	Logic high input current	V_{HIGH} = 1.8 V		6		µA
I_{IL}	Logic low input current	V_{LOW} = 0 V		< 0.1		µA
V_{OH}	Logic high output voltage			AVDD - 0.1		V
V_{OL}	Logic low output voltage			0.2		V
LVDS OUTPUTS (see Figure 2)						
V_{ODH}	High-level output differential voltage	100-Ω external termination	245	350	405	mV
V_{ODL}	Low-level output differential voltage	100-Ω external termination	–245	–350	–405	mV
V_{OCM}	Output common-mode voltage		900	1100	1300	mV

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8.7 Timing Requirements

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, sampling frequency = 80 MSPS, 14-bit, sine wave input clock = 1.5 Vpp clock amplitude, C_{LOAD} = 5 pF, R_{LOAD} = 100 Ω, unless otherwise noted. MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.7 V to 1.9 V(1)(2)(3)

			MIN	TYP	MAX	UNIT
t_a	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs		4		ns
	Aperture delay variation	Across channels within the same device		±175		ps
		Across devices at the same temperature and LVDD supply		2.5		ns
t_j	Aperture jitter RMS			320		fs rms
t_d	Data latency	1-wire LVDS output interface		11		Clock cycles
		2-wire LVDS output interface		15		Clock cycles
t_{SU}	Data set-up time	80 MSPS, 2-wire LVDS, 7x-serialization	0.34	0.57		ns
t_H	Data hold time	80 MSPS, 2-wire LVDS, 7x-serialization	0.55	0.8		ns
t_{PROP}	Clock propagation delay	Input clock rising edge (zero cross) to frame clock rising edge (zero cross)	See LVDS Timing at Different Sampling Frequencies — 2-Wire Interface, 7x-Serialization, Digital Filter Disabled and LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Digital Filter Disabled			
	Variation of t_{PROP}	Between two devices at same temperature and LVDD supply		±0.75		ns
	LVDS bit clock duty cycle			48%		
t_{RISE}	Data rise time	Rise time is from –100 mV to + 100 mV, 10 ≤ Fs ≤ 80 MSPS		0.24		ns
t_{FALL}	Data fall time	Fall time is from +100 mV to –100 mV, 10 ≤ Fs ≤ 80 MSPS		0.24		ns
$t_{CLKRISE}$	Output clock rise time	Rise time is from –100 mV to +100 mV, 10 ≤ Fs ≤ 80 MSPS		0.20		ns
$t_{CLKFALL}$	Output clock fall time	Fall time is from +100 mV to –100 mV, 10 ≤ Fs ≤ 80 MSPS		0.20		ns
t_{WAKE}	Wake-up Time	Time to valid data after coming out of COMPLETE POWER-DOWN mode		100		µs
		Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)		5		µs

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Set-up and hold time specifications take into account the effect of jitter on the output data and clock.
(3) Data valid refers to logic HIGH of 100 mV and logic LOW of –100 mV.

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8.8 LVDS Timing at Different Sampling Frequencies — 2-Wire Interface, 7x-Serialization, Digital Filter Disabled

See [1]

ADC CLK Frequency (MSPS)	Set-up Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (6 / 7) × T + t_{delay}, ns[2]		
Fs = 1 / T	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from Input clock zero-cross rising edge to frame clock zero cross (rising edge)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	0.34	0.57		0.55	0.8		8	9.5	11
65	0.35	0.64		0.8	1.1		8	9.5	11
50	0.7	0.9		1.2	1.5		8	9.5	11
40	1	1.3		1.6	1.85		8	9.5	11
30	1.7	2		2	2.3		8	9.5	11
20	2.9	3.2		3.2	3.5		8	9.5	11
10	6.5	6.7		6.7	7		8	9.5	11

(1) Bit clock and Frame clock jitter has been included in the Set-up and hold timing.
(2) Values below correspond to tdelay, NOT t_{PROG}

8.9 LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Digital Filter Disabled

See [1]

ADC CLK Frequency (MSPS)	Set-up Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (5 / 7) × T + t_{delay}, ns[2]		
Fs = 1 / T	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from Input clock zero-cross rising edge to frame clock zero cross (rising edge)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
50	0.28	0.48		0.28	0.6		7.5	9	10.5
40	0.5	0.68		0.54	0.8		7.5	9	10.5
30	0.62	0.8		1	1.25		7.5	9	10.5
20	1.2	1.4		1.6	1.9		7.5	9	10.5
10	3.1	3.3		3.3	3.5		7.5	9	10.5

(1) Bit clock and Frame clock jitter has been included in the Set-up and hold timing.
(2) Values below correspond to tdelay, NOT t_{PROG}

NOTE

The LVDS timing specification is only valid when digital decimation filters are disabled. When digital filters are enabled, the set-up time decreases as the corresponding hold time increases as shown in *LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 2 Filter Enabled* to *LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 8 Filter Enabled* . The change on LVDS timing also depends on the internal PLL setting of the ADS5294. See *PLL Operation Versus LVDS Timing* for more information.

At the highest sampling frequency, 80-MSPS, and decimation of 2 (for example: effective data rate = 560 Mbps in 1-wire mode), the set-up time is reduced by 70 ps, (for example: set-up time, min = 0.43 ns; hold time, min = 0.54 ns). scenario assumes that the recommended PLL settings are configured as shown in *PLL Operation Versus LVDS Timing*

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8.10 Serial Interface Timing Requirements

The table shows typical values at 25°C. MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, LVDD = 1.8 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1 / t_{SCLK})	> DC		15	MHz
t_{SLOADS}	$\overline{CS}$ to SCLK set-up time	33			ns
t_{SLOADH}	SCLK to $\overline{CS}$ hold time	33			ns
t_{DS}	SDATA set-up time	33			ns
t_{DH}	SDATA hold time	33			ns

8.11 Reset Timing

The table shows typical values at 25°C. MIN and MAX values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C (unless otherwise noted). See Figure 1

			MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power up of AVDD and LVDD to RESET pulse active		1		ms
t_2	Reset pulse duration	Pulse duration of active RESET signal	50			ns
t_3	Register write delay	Delay from RESET disable to CSZ active		100		ns

8.12 LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 2 Filter Enabled

See (1)(2)(3)

ADC CLK Frequency (MSPS)	Set-up Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (6 / 7) × T + t_{delay}, ns(4)		
Fs = 1 / T	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from input clock zero-cross rising edge to frame clock zero cross (rising edge)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	0.43			0.54			7.5	9	10.5
60	0.54			0.9			7.5	9	10.5
40	1.1			1.45			7.5	9	10.5

(1) Bit clock and Frame clock jitter has been included in the Set-up and hold timing.
(2) The LVDS timing depends on the state of the internal PLL. Use Table 3 to configure the PLL when decimation by two is enabled..
(3) For any given ADC input clock frequency, TI recommends to use the highest PLL state to get the best set-up time. The timing numbers are specified under this condition. For example, for a 40-MSPS input clock frequency, use PLL state 3 to get set-up time ≥ 1.1 ns. PLL state 2 can also be used at 40 MSPS, however, the set-up time degrades by 100 to 200 ps (while the hold time improves by a similar amount).
(4) Values below correspond to t_{delay}, not t_{PROG}

8.13 LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 4 Filter Enabled

See (1)(2)(3)

ADC CLK Frequency (MSPS)	Set-up Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (8 / 7) × T + t_{delay}, ns(4)		
Fs = 1 / T	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from input clock zero-cross rising edge to frame clock zero cross (rising edge)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	1			1.5			7.5	9	10.5
60	1.7			1.7			7.5	9	10.5

(1) Bit clock and Frame clock jitter has been included in the Set-up and hold timing.
(2) The LVDS timing depends on the state of the internal PLL. Use Table 4 to configure the PLL when decimation by 4 is enabled
(3) For any given ADC input clock frequency, TI recommends to use the highest PLL state to get best set-up time. The timing numbers are specified under this condition.
(4) Values below correspond to t_{delay}, not t_{PROG}

8.14 LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 8 Filter Enabled

See (1)(2)(3)

ADC CLK Frequency (MSPS)	Set-up Time (t_{su}), ns			Hold Time (t_H), ns			t_{PROG} = (5 / 7) × T + t_{delay}, ns(4)		
Fs = 1 / T	Data Valid to Zero-Crossing of LCLKP (both edges)			Zero-Crossing of LCLKP to Data Becoming Invalid (both edges)			t_{PROG} = delay from Input clock zero-cross rising edge to frame clock zero cross (rising edge)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	2.9			3.2			7.5	9	10.5

(1) Bit clock and Frame clock jitter has been included in the Set-up and hold timing.
(2) The LVDS timing depends on the state of the internal PLL. Use Table 5 to configure the PLL when decimation by 8 is enabled
(3) For any given ADC input clock frequency, TI recommends using the highest PLL state to get best set-up time. The timing numbers are specified under this condition.
(4) Values below correspond to t_{delay}, not t_{PROG}

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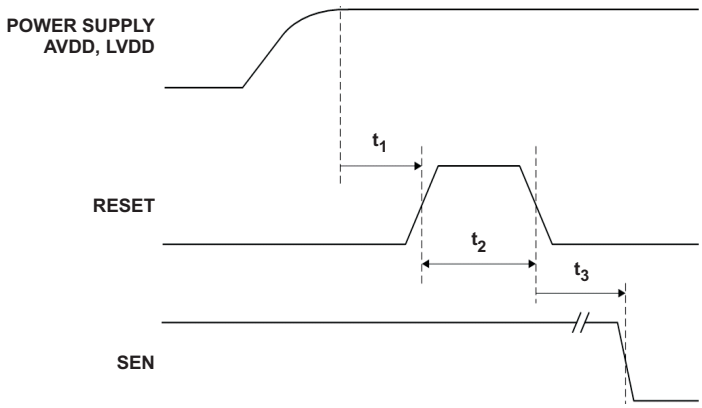

(1) A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. Tie RESET permanently HIGH for parallel interface operation.

(2) SEN refers to the CSZ pin.

Figure 1. Reset Timing Diagram

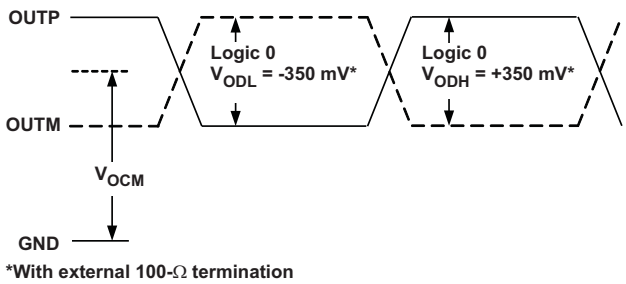

Figure 2. LVDS Output Voltage Levels

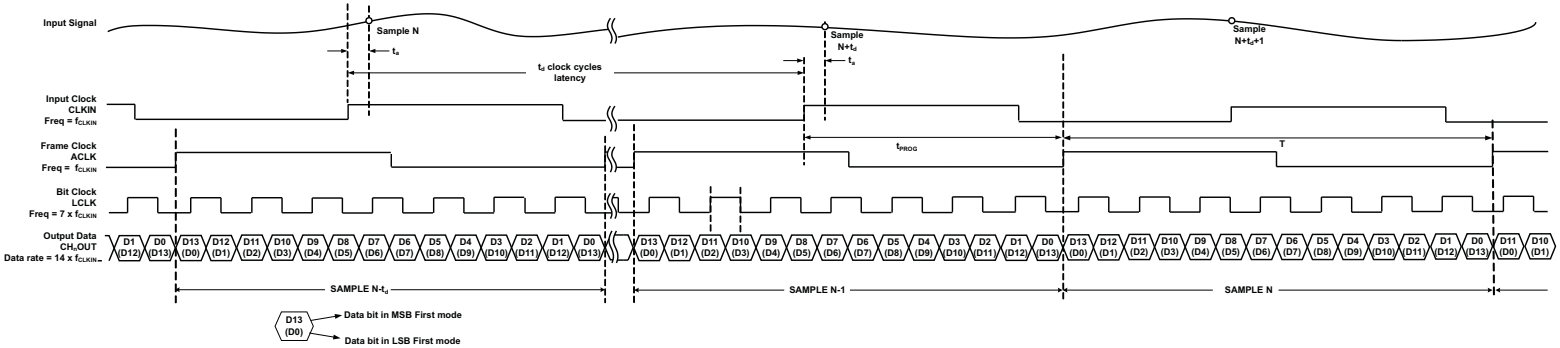

Figure 3. 14-Bit 1-Wire LVDS Timing Diagram

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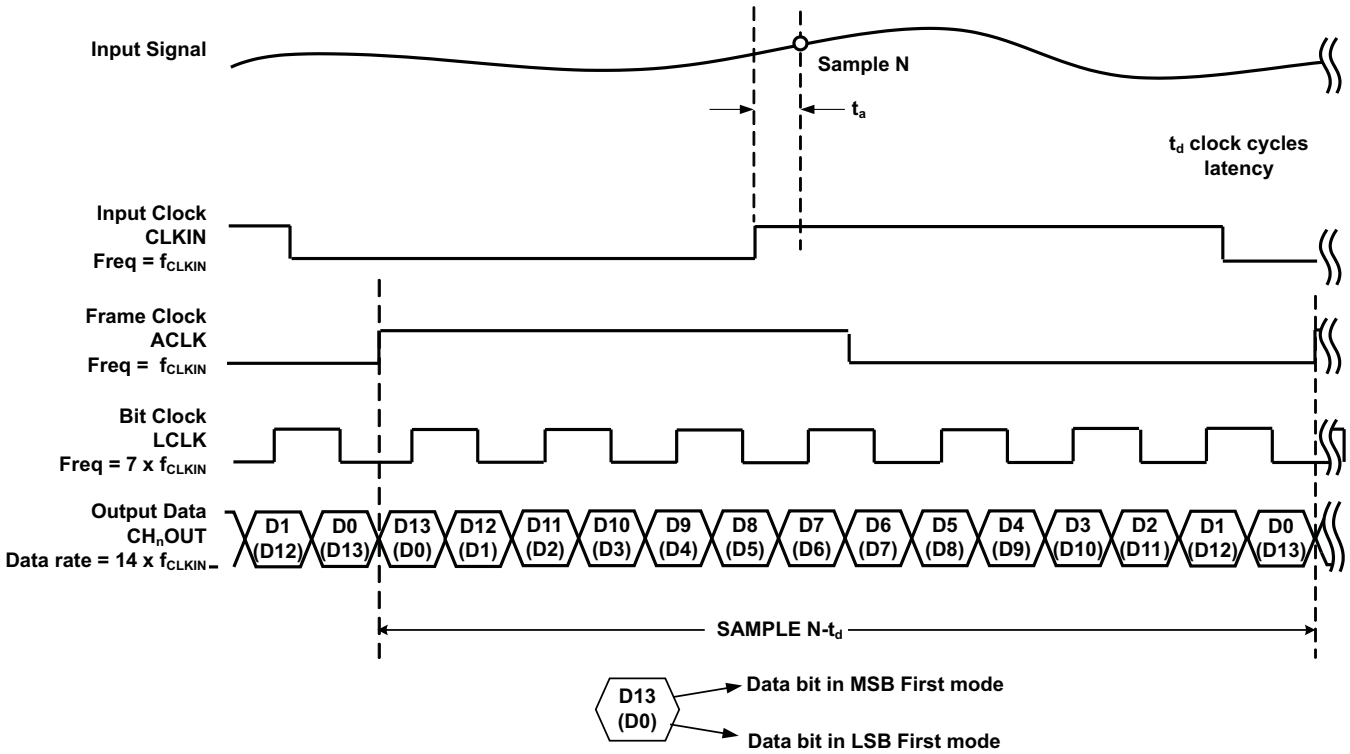

Figure 4. Enlarged 1-Wire LVDS Timing Diagram (14 bit)

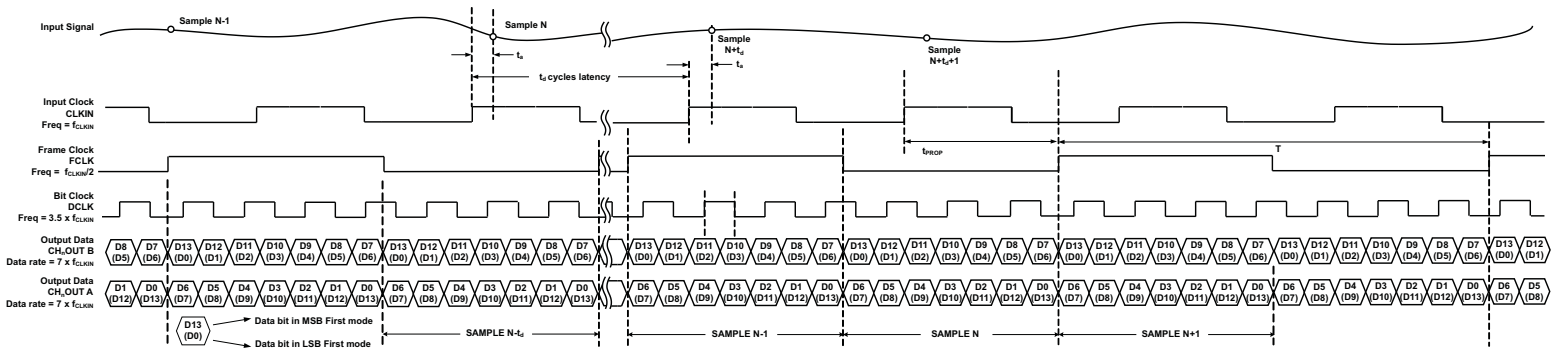

Figure 5. 14-Bit 2-Wire LVDS Timing Diagram

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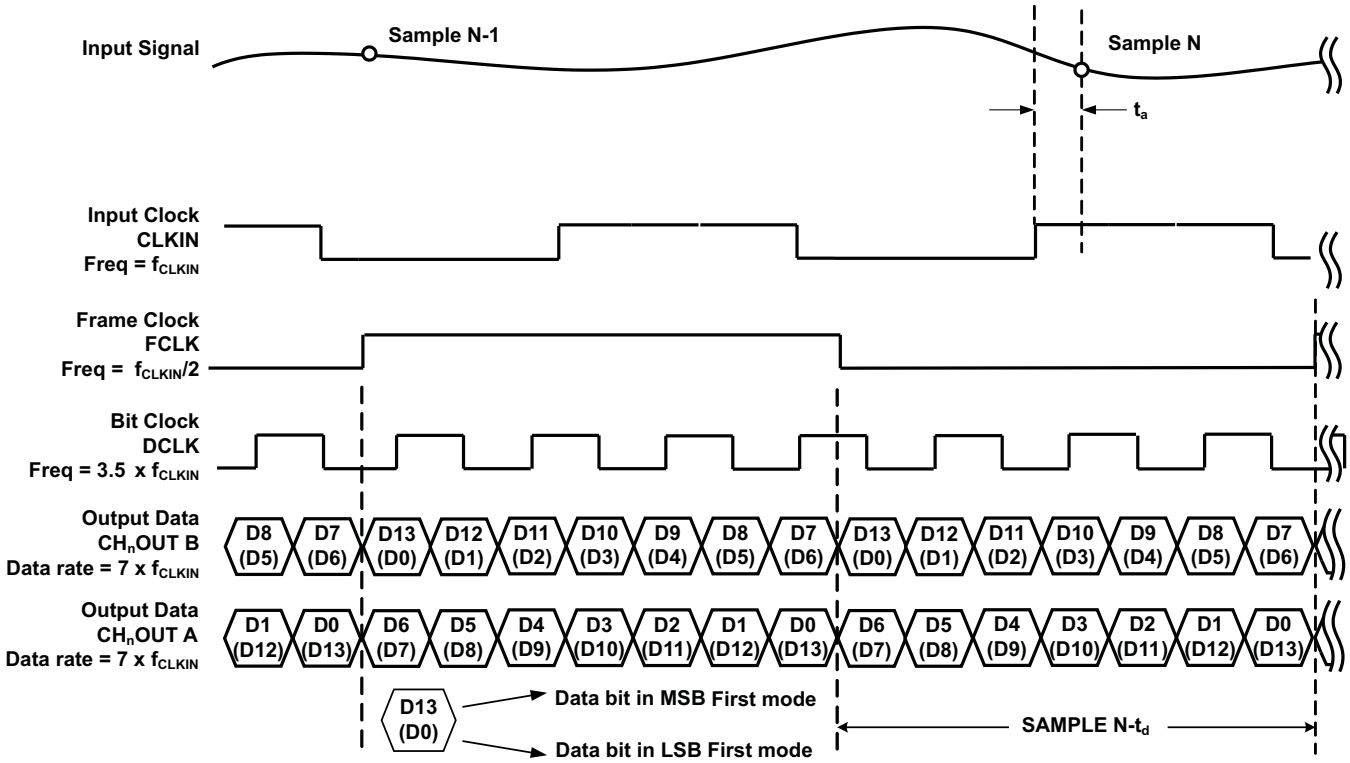

Figure 6. Enlarged 2-Wire LVDS Timing Diagram (14 bit)

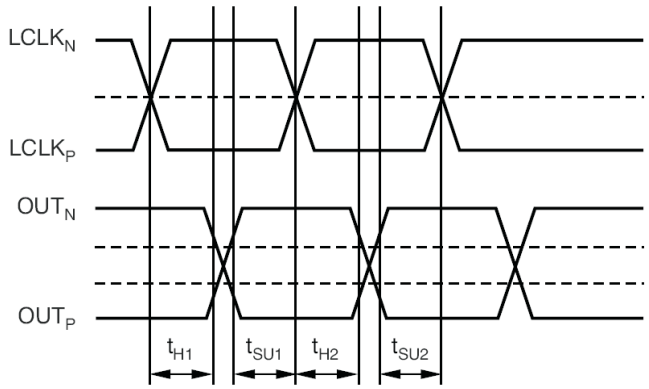

Figure 7. Definition of Setup and Hold Times t_{SU} = min(t_{SU1}, t_{SU2}); t_H = min(t_{H1}, t_{H2})

8.15 Typical Characteristics

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 14 Bit/ 80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

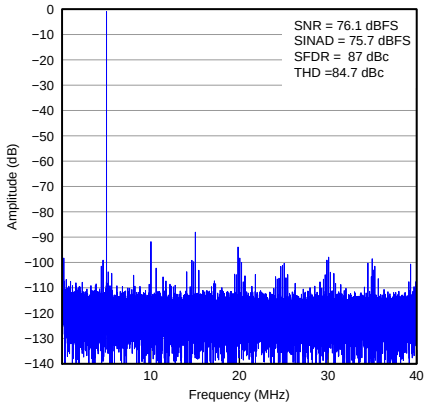

Figure 8. FFT for 5-MHz Input Signal, Sample Rate = 80 MSPS

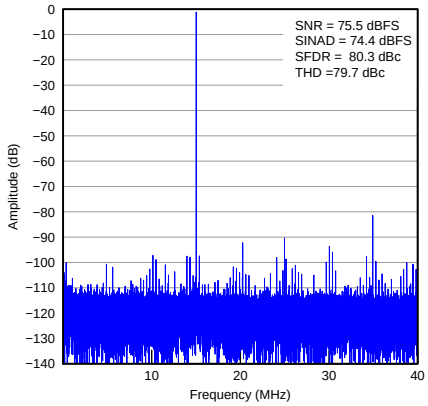

Figure 9. FFT for 15-MHz Input Signal, Sample Rate = 80 MSPS

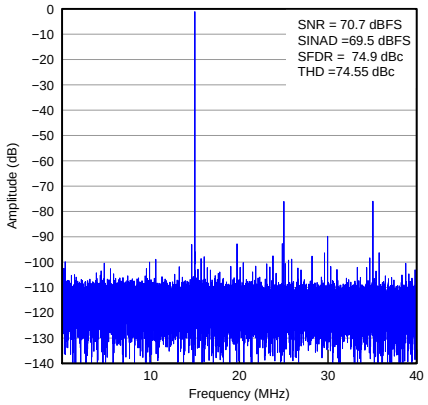

Figure 10. FFT for 65-MHz Input Signal, Sample Rate = 80 MSPS

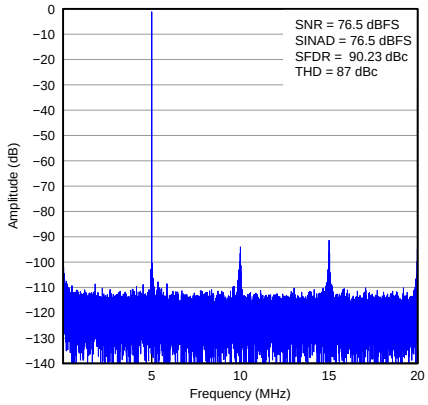

Figure 11. FFT for 5-MHz Input Signal, Sample Rate = 40 MSPS

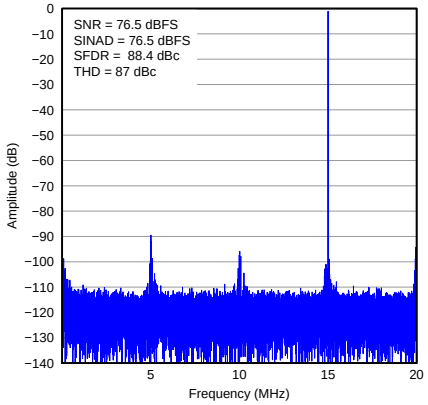

Figure 12. FFT for 15-MHz Input Signal, Sample Rate = 40 MSPS

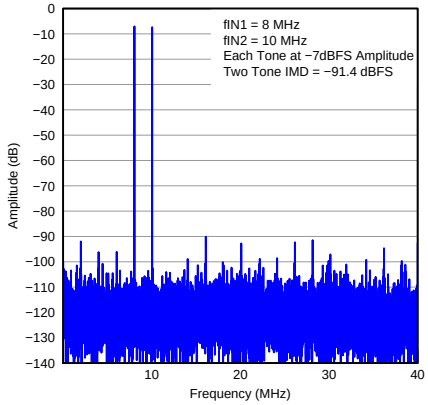

Figure 13. Two-Tone Intermodulation

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Typical Characteristics (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 14 Bit/ 80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

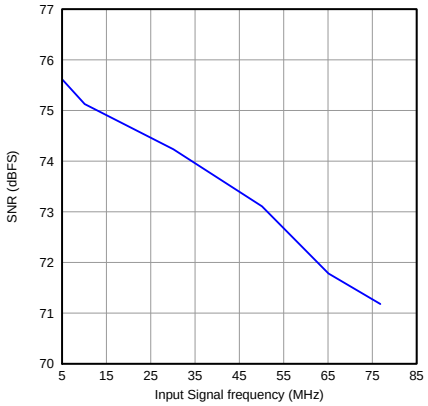

Figure 14. Signal-To-Noise Ratio vs Input Signal Frequency

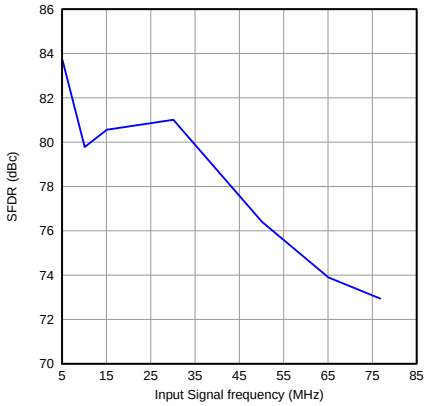

Figure 15. Spurious-Free Dynamic Range vs Input Signal Frequency

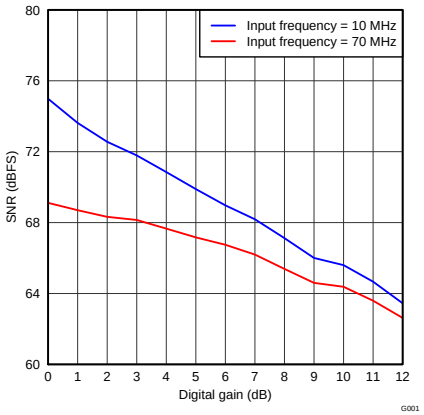

Figure 16. SNR vs Digital Gain

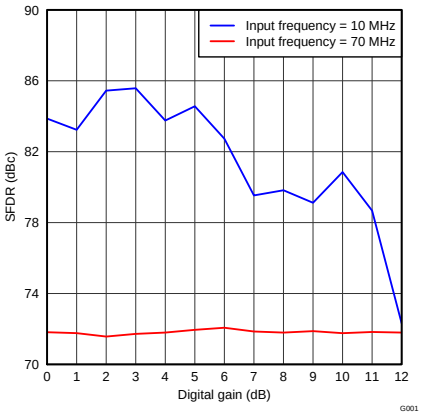

Figure 17. SFDR vs Digital Gain

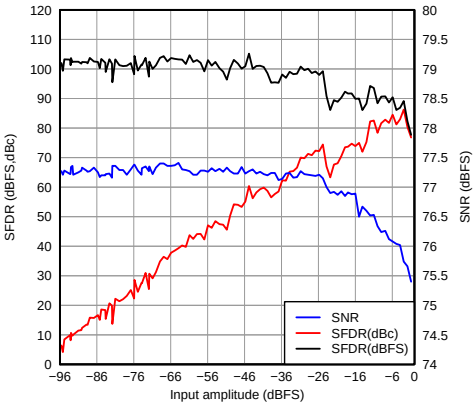

Figure 18. Performance vs Input Amplitude

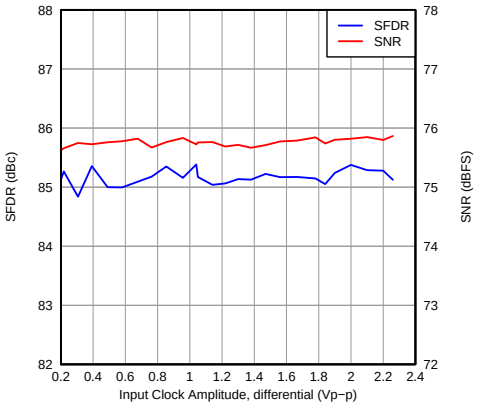

Figure 19. Performance vs Clock Input Amplitudes

Typical Characteristics (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 14 Bit/ 80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

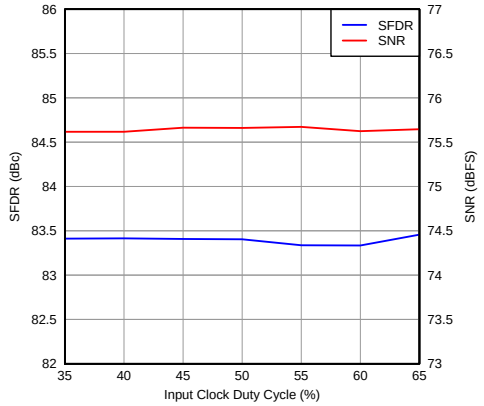

Figure 20. Performance vs Input Clock Duty CyclePerformance vs Input Clock Duty Cycle

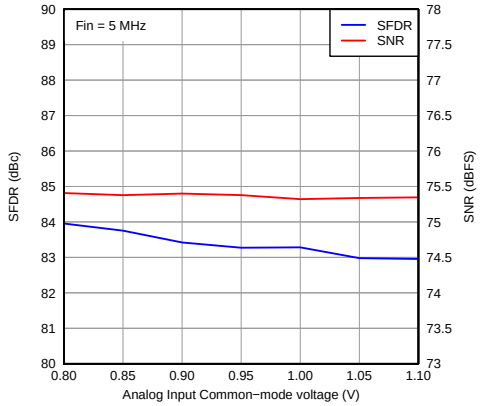

Figure 21. Performance vs Input VCM

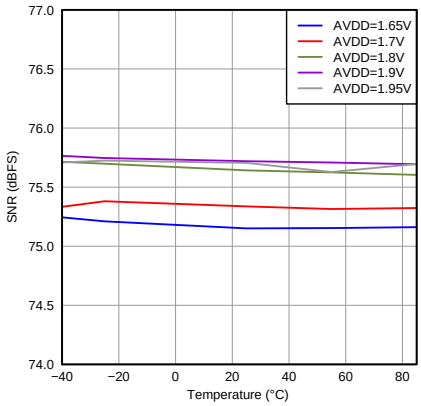

Figure 22. Signal-To-Noise Ratio vs Temperature

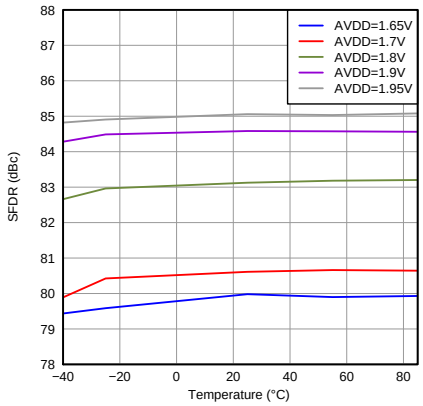

Figure 23. Spurious-Free Dynamic Range vs Temperature

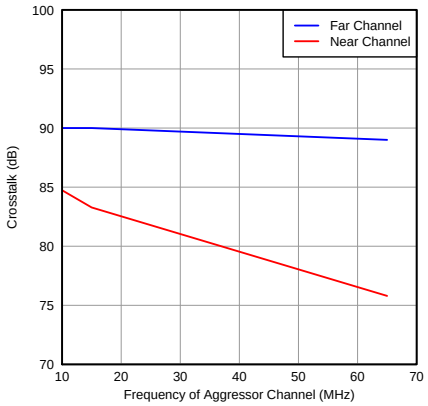

Figure 24. Crosstalk vs Frequency

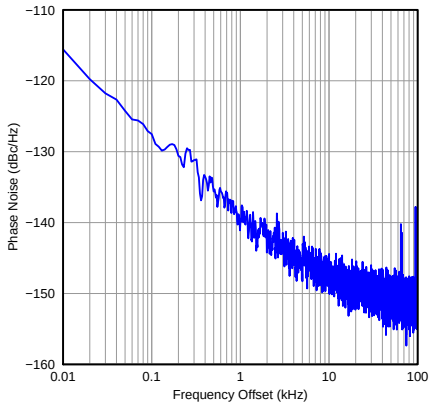

Figure 25. Phase Noise for 5-MHz Input Signal, Sample Rate = 80 MSPS

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Typical Characteristics (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 14 Bit/ 80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

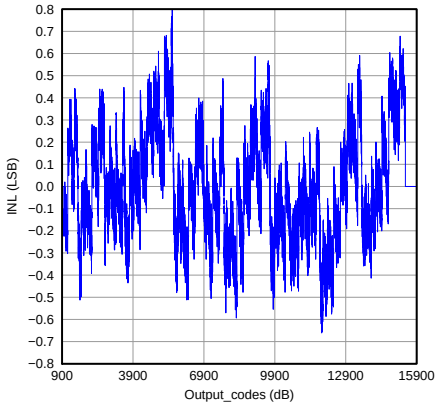

Figure 26. Integral Non-Linearity

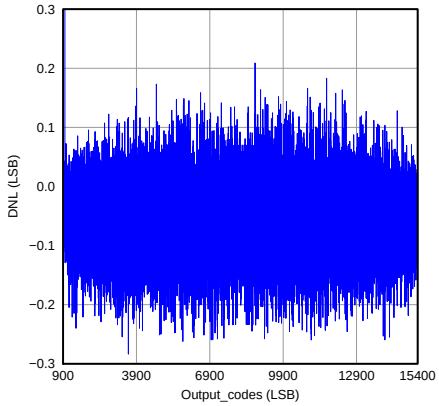

Figure 27. Differential Non-Linearity

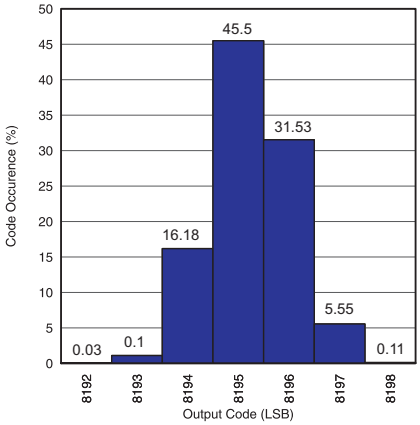

Figure 28. Histogram of Output Code With Analog Inputs Shorted (RMS Noise = 96.4 uV) a note "RMS Noise = 96.4 uV" to Figure 28

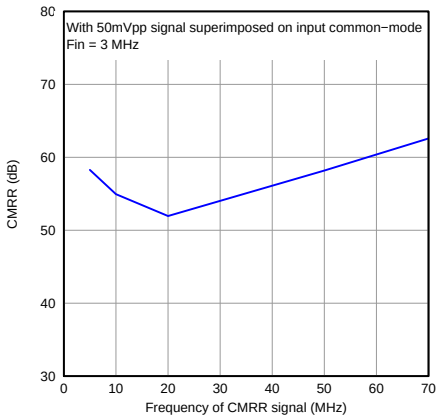

Figure 29. Common Mode Rejection Ratio vs Frequency

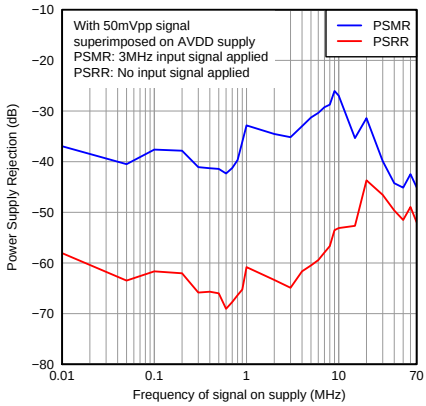

Figure 30. Power-Supply Rejection Ratio vs Frequency

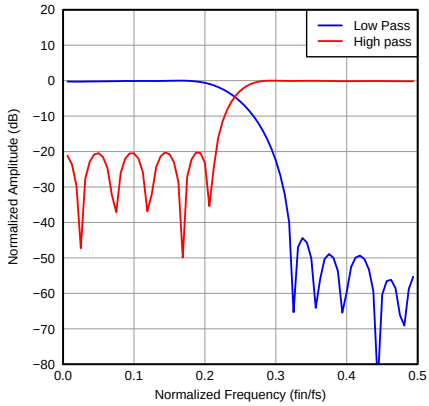

Figure 31. Filter Response, Decimate by 2

Typical Characteristics (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 14 Bit/ 80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

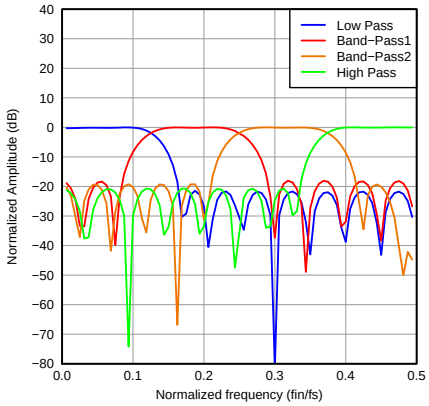

Figure 32. Filter Response, Decimate by 4

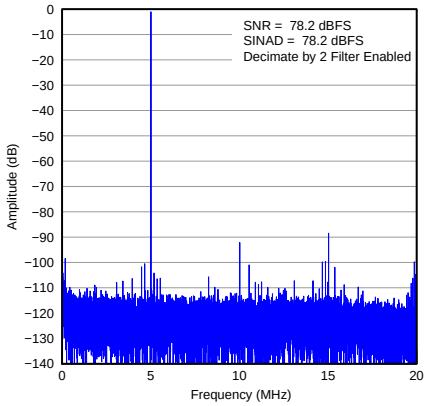

Figure 33. FFT for 5-MHz Input Signal, Sample Rate = 80 MSPS with Decimation Filter = 2

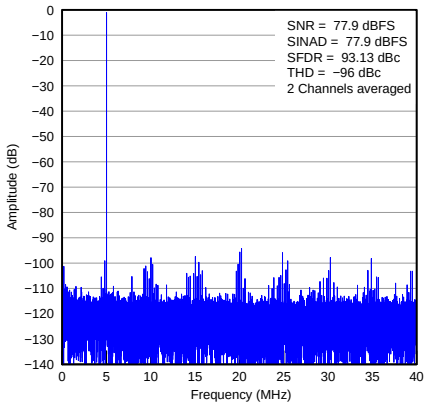

Figure 34. FFT for 5-MHz Input Signal, Sample Rate = 80 MSPS by Averaging 2 Channels

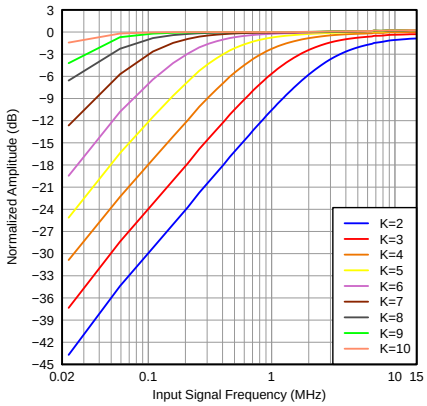

Figure 35. Digital High-Pass Filter Response

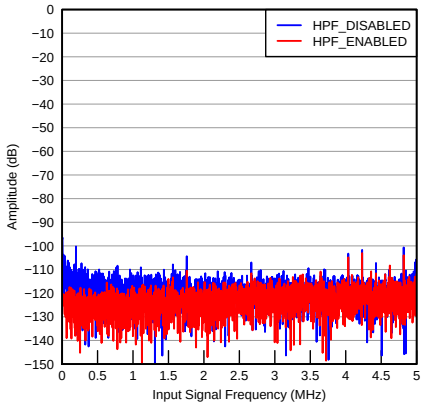

Figure 36. FFT with HPF Enabled and Disabled, No Signal

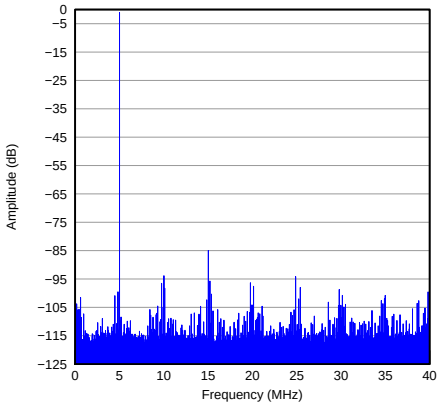

Figure 37. FFT (Full-Band) for 5-MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

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Typical Characteristics (continued)

Typical values are at 25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 14 Bit/ 80 MSPS, ADC is configured in the internal reference mode, unless otherwise noted.

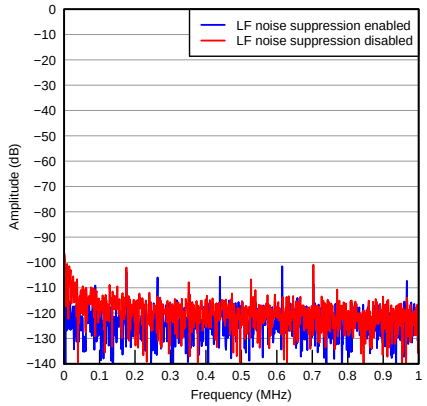

Figure 38. FFT (0 to 1 MHz) for 5-MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

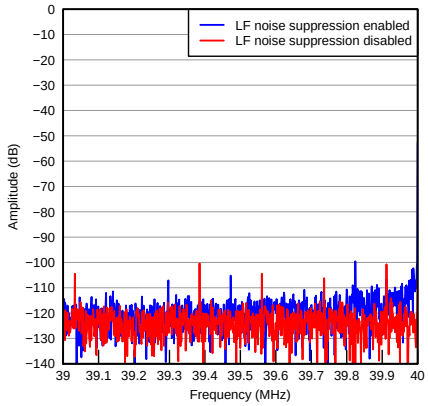

Figure 39. FFT (39 MHz to 40 MHz) for 5-MHz Input Signal, Sample Rate = 80 MSPS with Low Frequency Noise Suppression Enabled

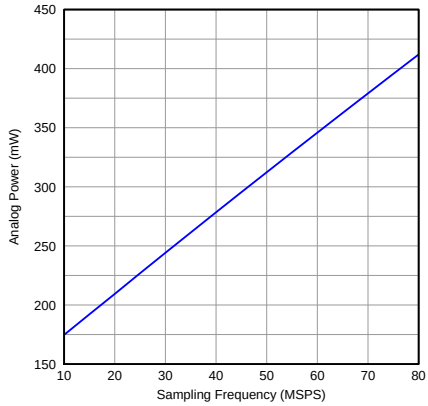

Figure 40. Power Consumption on Analog Supply

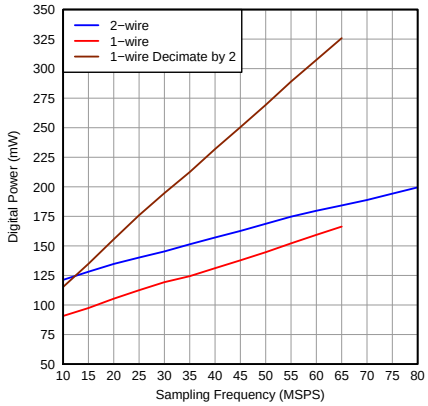

Figure 41. Power Consumption on Digital Supply

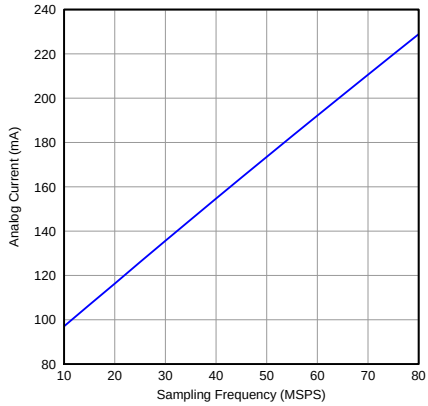

Figure 42. Supply Current on Analog Supply

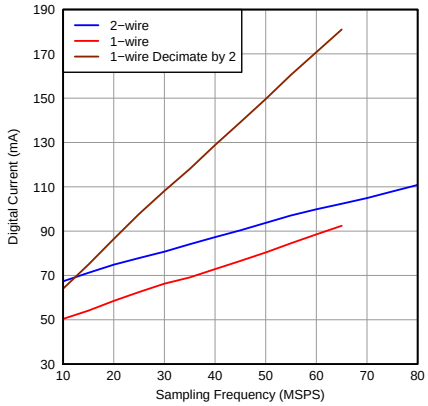

Figure 43. Supply Current on Digital Supply

9 Detailed Description

9.1 Overview

The ADS5294 is an octal-channel, 14-bit, high-speed ADC with a sample rate of up to 80 MSPS that runs off a single 1.8-V supply. All eight channels of the ADS5294 simultaneously sample the respective analog inputs at the rising edge of the input clock. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock, edge the sample propagates through the pipeline resulting in a data latency of 11 clock cycles.

The 14 data bits of each channel are serialized and sent out in either 1-wire mode (one pair of LVDS pins are used) or 2-wire mode (two pairs of LVDS pins are used), depending on the LVDS output rate. When the data is output in the 2-wire mode, it reduces the serial data rate of the outputs, especially at higher sampling rates. Low-cost FPGAs are used to capture 80 MSPS / 14-bit data. Alternately, at lower sample rates, the 14-bit data is output as a single data stream over one pair of LVDS pins (1-wire mode). The device outputs a bit clock at 7x and frame clock at 1x the sample frequency in the 14-bit mode.

This 14-bit ADC achieves approximately 76-dBFS SNR at 80 MSPS. Its output resolution can be configured as 12-bit and 10-bit, if necessary. When the output resolution of the ADS5294 is 12-bit and 10-bit, SNR of 72 dBFS and 61 dBFS (respectively) is achieved.

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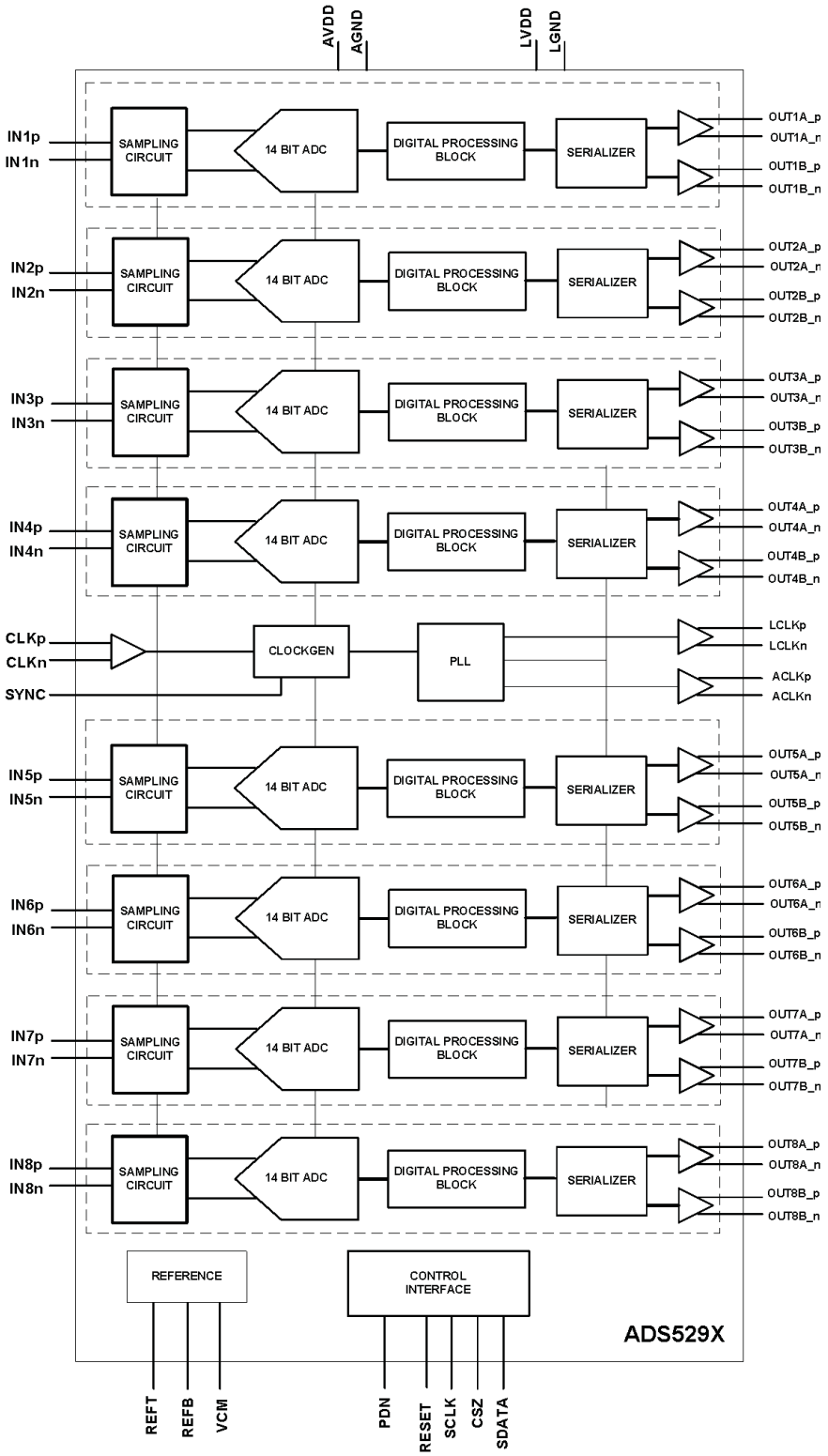
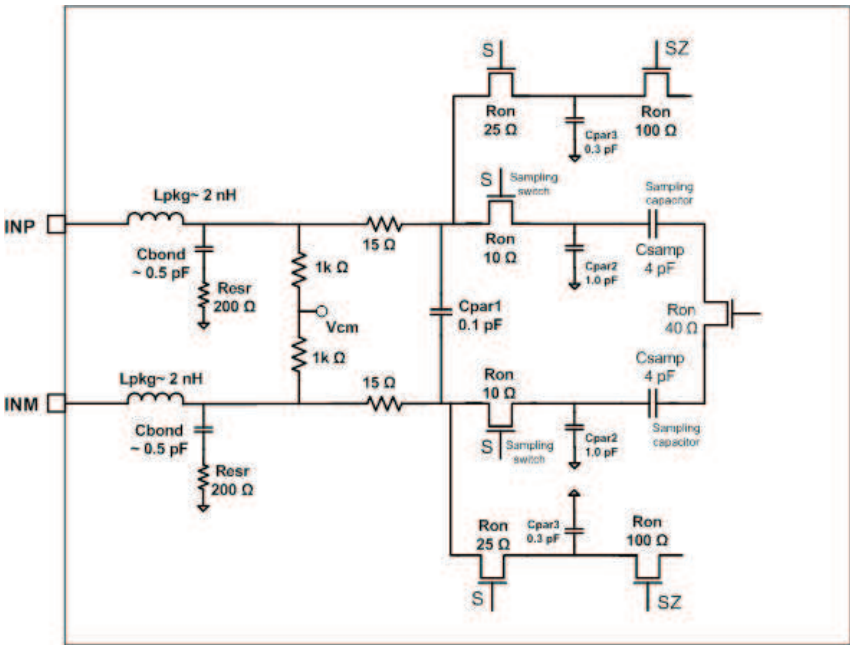
9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Analog Input

The analog inputs consist of a switched-capacitor-based differential sample and hold architecture. This differential topology results in good AC performance even for high input frequencies at high sampling rates. The INP and INM pins are internally biased around a common-mode voltage of Vcm (0.95 V). For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between Vcm + 0.5 V and Vcm – 0.5 V, resulting in a 2 V_{PP} differential input swing. Figure 44 shows the equivalent circuit of the input sampling circuit.



(1) SZ MOSFETs' open ends connect to common mode potential, while they don't impact the inputs' loading. Users may treat the open ends as high impedance nodes.

Figure 44. Analog Input Circuit Model

9.3.2 Input Clock

Figure 45 shows the clock equivalent circuit of the ADS5294. The ADS5294 is configured by default to operate with a single-ended input clock. CLKP is driven by a CMOS clock and CLKM is tied to GND. The device automatically detects a single-ended or differential clock. If CLKM is grounded, the device treats clock as a single-ended clock. Operating with a low-jitter differential clock usually gives better SNR performance, especially at input frequencies greater than 30 MHz.

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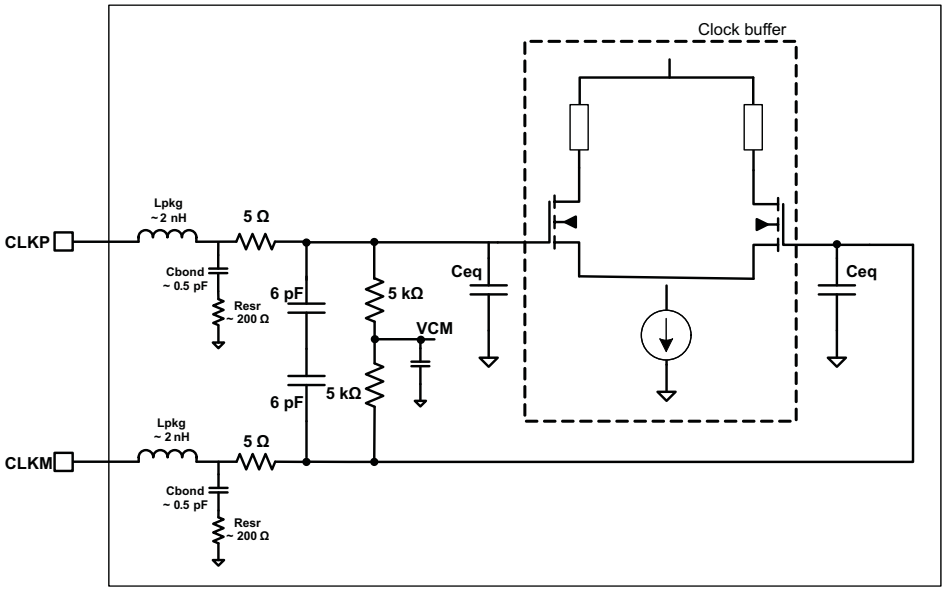
Feature Description (continued)



Ceq is approximately 1 to 3 pF, equivalent input capacitance of clock buffer.

Figure 45. Equivalent Circut of the Input Clock Circuit

Feature Description (continued)

9.3.3 Digital Highpass IIR Filter

DC offset is often observed at ADC input signals. For example, in ultrasound applications, the DC offset from variable-gain amplifier (VGA) varies at different gains. Such a variable offset can introduce artifacts in ultrasound images especially in Doppler modes. Analog filter between ADC and VGA can be used with added noise and power. Digital filter achieves the same performance as analog filters and has more flexibility in fine tuning multiple characteristics.

ADS5294 includes optional first-order digital high-pass (HP) IIR filter. Figure 46 shows the device block diagram and transfer function.

$$y(n) = \frac{2^k}{2^k+1}[x(n) - x(n-1) + y(n-1)] \tag{1}$$

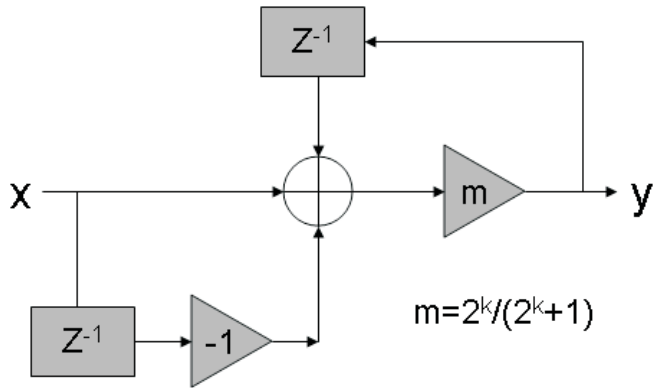


Figure 46. HP Filter Block Diagram

Figure 47 shows the characteristics at k=2 to 10.

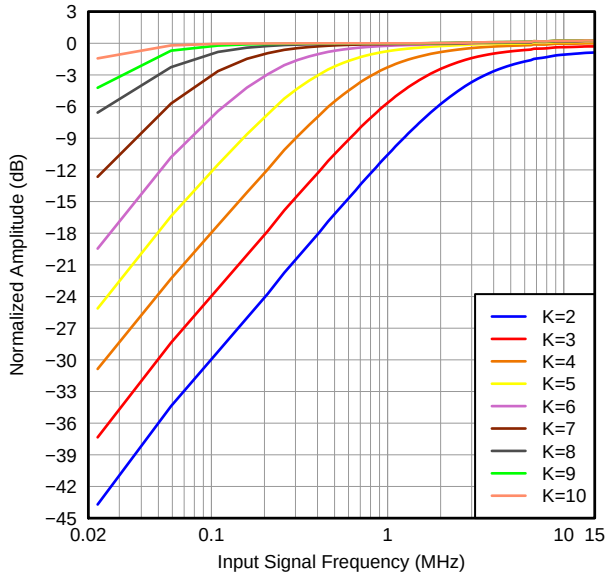


Figure 47. HP Filter Amplitude Response at K = 2 to 10

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Feature Description (continued)

9.3.4 Decimation Filter

ADS5294 includes an option to decimate the ADC output data using filters. Once the decimation is enabled, the decimation rate, frequency band of the filter can be programmed. In addition, the user can select either the pre-defined or custom coefficients.

Table 1. Digital Filters(1)

DECIMATION	TYPE OF FILTER	DATA _RATE	FILTERn _RATE	FILTERn _COEFF_SET	ODD_TAP	USE _FILTER _CHn	EN_CUSTOM _FILT
Decimate by 2	Built-in **low-pass odd-tap** filter (pass band = 0 to f_S / 4)	01	000	000	1	1	0
	Built-in **high-pass odd-tap** filter (pass band = f_S / 4 to f_S /2)	01	000	001	1	1	0
Decimate by 4	Built-in **low-pass even-tap** filter (pass band = 0 to f_S / 8)	10	001	010	0	1	0
	Built-in first **band pass even tap** filter (pass band = f_S / 8 to f_S / 4)	10	001	011	0	1	0
	Built-in second **band pass even tap** filter (pass band = f_S / 4 to 3 f_S / 8)	10	001	100	0	1	0
	Built-in **high pass odd tap** filter (pass band = 3 f_S / 8 to f_S / 2)	10	001	101	1	1	0
Decimate by 2	Custom filter (user-programmable coefficients)	01	000	000	0 and 1	1	1
Decimate by 4	Custom filter (user-programmable coefficients)	10	001	000	0 and 1	1	1
Decimate by 8	Custom filter (user-programmable coefficients)	11	100	000	0 and 1	1	1
Bypass decimation	Custom filter (user-programmable coefficients)	00	011	000	0 and 1	1	1

(1) EN_CUSTOM_FILT is the D15 of register 5A (Hex) to B9 (Hex).

9.3.5 Decimation Filter Equation

In the default setting, the decimation filter is implemented as a 24-tap FIR filter with symmetrical coefficients (each coefficient is 12-bit signed). By setting the register bit **ODD_TAPn** = 1, a 23-tap FIR is implemented

9.3.5.1 Pre-defined Coefficients

The built-in filters (lowpass, highpass, and bandpass) use pre-defined coefficients. The frequency responses of the build-in decimation filters with different decimation factors are shown in Figure 48.

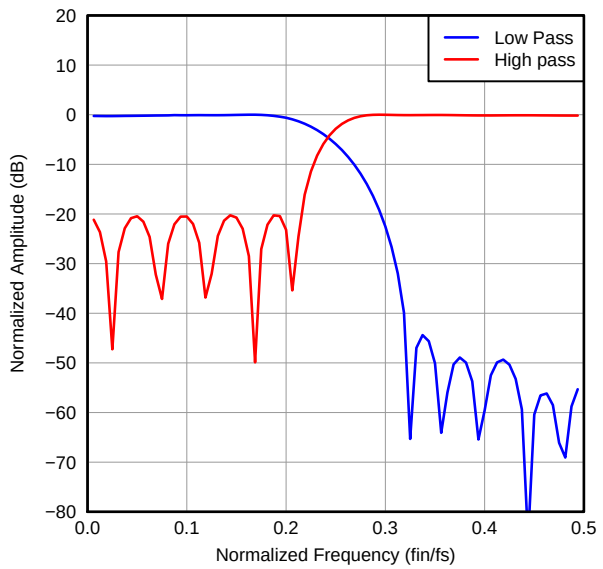

Figure 48. Decimation Filter Responses (Decimate by 2)

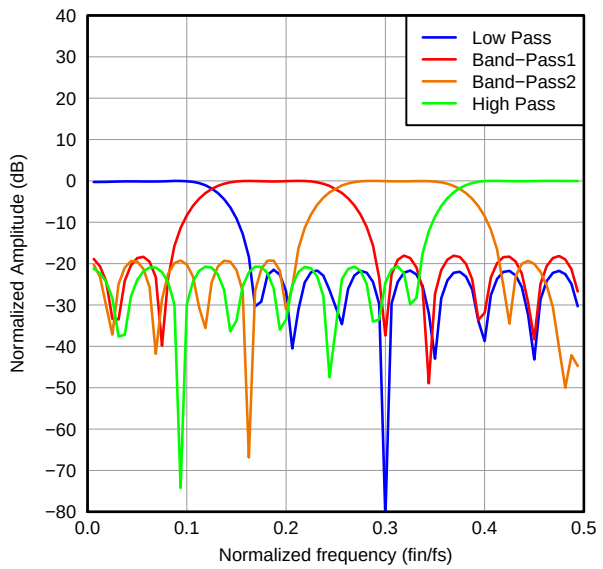

Figure 49. Decimation Filter Responses (Decimate by 4)

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9.3.5.2 Custom Filter Coefficients

The filter coefficients are also programmed, or customized, by the user. For custom coefficients, set the register bit **<FILTER COEFF SELECT>** and load the coefficients (h_0 to h_{11}) in registers 0x5A to 0xB9, using the serial interface as:

Register content = real coefficient value × 211, 12-bit signed representation of real coefficient.

9.3.6 PLL Operation Versus LVDS Timing

The ADS5294 uses a PLL that automatically changes configuration to one of four states depending on the sampling clock frequency. The clock frequency detection is automatic and each time the sampling frequency crosses a threshold, the PLL changes configuration to a new state. The PLL remains in the new state for a range of clock frequencies. To prevent unwanted toggling of PLL state around a threshold, the circuit has an built-in hysteresis. The ADS5294 has three thresholds over the sampling clock frequency range from 10 MHz to 80 MHz and can be in one of four states as shown by Figure 50.

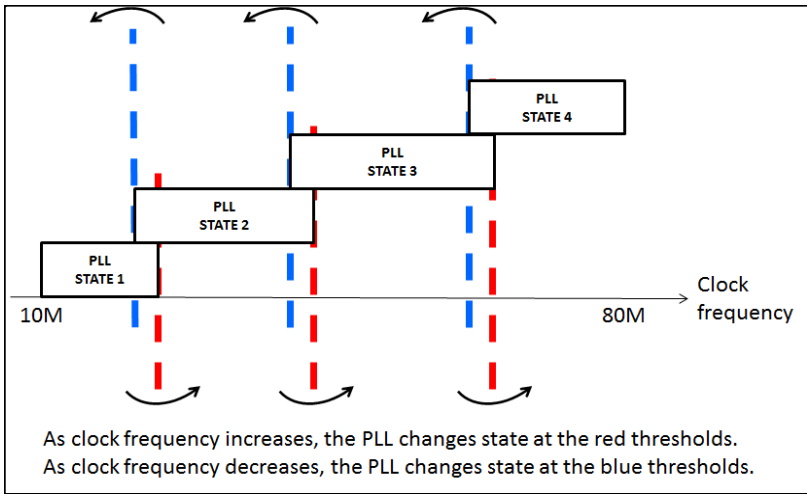

Figure 50. PLL States Versus ADC Fs

Each threshold shifts by a small amount across temperature. On power up, depending on the clock frequency, the PLL settles in one of four states. Later, as the system warms up, the PLL changes state once due to the shift in the threshold across temperature.

9.3.6.1 Effect on Output Timings

The PLL state change has an effect on the output LVDS timings. In some settings, the set-up time decreases by 100 ps typically with a corresponding increase in the hold time.

In applications where a timing calibration occurs at the system level once after power-up, this subsequent change of the PLL state is undesirable. The ADS5294 has register options to disable the automatic switch of the PLL state based on frequency detected. To prevent this variation in output timing, disable the PLL from switching states.

In addition to disabling the auto-switching, setting the PLL to the correct state is also required, depending on the sample clock frequency used in the system. The following sequence of register writes must be followed exactly:

- Step 1: Enable test-mode access by writing register data = 0x0010 in address 0x01 (for example: enable the access to registers with address higher than 0xF0).
- Step 2: Configure the PLL to the correct state depending on the clock frequency of operation and the decimation factor, as per the following tables.

NOTE

For certain sampling frequencies, there are two PLL states possible, both of which are stable. In such cases, the higher PLL state results in a better set-up time compared to a lower PLL state. For example, at 80 MSPS, with decimation by 2 enabled, the PLL may be in states 3 or 4. However, the set-up time value specified in *LVDS Timing at Different Sampling Frequencies — 1-Wire Interface, 14x-Serialization, Decimation by 2 Filter Enabled* (0.43 ns minimum) is in PLL state 4. In state 3, the set-up time is reduced further by 100 ps typically, with a corresponding increase in the hold time.

Table 2. PLL Configuration When Decimation is Disabled

ADC Fs (MSPS)	FUNCTION	REGISTER ADDRESS	REGISTER DATA
Fs ≤ 12	Disable PLL auto state switch and put PLL in state 1	0xD1	0x0040
9 ≤ Fs ≤ 24	Disable PLL auto state switch and put PLL in state 2	0xD1	0x00C0
18 ≤ Fs ≤ 42	Disable PLL auto state switch and put PLL in state 3	0xD1	0x0140
Fs ≥ 28	Disable PLL auto state switch and put PLL in state 4	0xD1	0x0240

Table 3. PLL Configuration When Decimation by 2 is Used

ADC Fs	FUNCTION	REGISTER ADDRESS	REGISTER DATA
Fs ≤ 24	Disable PLL auto state switch and put PLL in state 1	0xD1	0x0040
18 ≤ Fs ≤ 48	Disable PLL auto state switch and put PLL in state 2	0xD1	0x00C0
36 ≤ Fs ≤ 80	Disable PLL auto state switch and put PLL in state 3	0xD1	0x0140
Fs ≥ 56	Disable PLL auto state switch and put PLL in state 4	0xD1	0x0240

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Table 4. PLL Configuration When Decimation by 4 is Used

ADC Fs	FUNCTION	REGISTER ADDRESS	REGISTER DATA
Fs ≤ 48	Disable PLL auto state switch and put PLL in state 1	0xD1	0x0040
36 ≤ Fs ≤ 80	Disable PLL auto state switch and put PLL in state 2	0xD1	0x00C0
Fs ≥ 72	Disable PLL auto state switch and put PLL in state 3	0xD1	0x0140

Table 5. PLL Configuration When Decimation by 8 is Used

ADC Fs	FUNCTION	REGISTER ADDRESS	REGISTER DATA
Fs ≤ 80	Disable PLL auto state switch and put PLL in state 1	0xD1	0x0040
72 ≤ Fs ≤ 80	Disable PLL auto state switch and put PLL in state 2	0xD1	0x00C0

9.4 Device Functional Modes

ADC Output Resolution and LVDS Serialization Rate Modes: The LVDS serialization rate can be programmed as 10, 12, 14, or 16 bits by the EN_BIT_SER register bit.

Output Data Rate Modes: The density of output data payload can be set to 1X or 2X mode by using the EN_SDR register bit. The maximum data rate (in bits per sec) of the LVDS interface is limited. In addtion, the LVDS data can be distributed by one pair LVDS data lane or two pairs of LVDS data lanes. Please see the description of Registers 0x50 to 0x55 in the *Programmable Mapping Between Input Channels and Output Pins* section. When the decimation feature is used, the LVDS output rate can be reduced to 1/2, 1/4, and 1/8 of ADC sampling rate as *Output Data Rate Control* shows. The flexible output data rate modes give users a wide selection of different speed FPGAs.

Power Modes: The device can be configured via SPI or pin settings to a complete power-down mode and via pin settings to a partial power-down (standby mode). During these two modes (complete and partial power-down), different internal functions stay powered up, resulting in different power consumption and wake-up times. In the partial power-down mode, all LVDS data lanes are powered down. The bit clock and frame clock lanes remain enabled to save time to sync again on the receiver side. However, in the complete power-down mode all lanes are powered down and thus this mode requires more time to wake-up because the bit clock and frame clock lanes must sync again with the receiver device.

LVDS Test Pattern Mode: The ADC data coming out of the LVDS outputs can be replaced by different kinds of test patterns. Note that the test patterns replace the data streaming out of the ADCs. The different test patterns are described in *LVDS Test Patterns*.

9.5 Programming

9.5.1 Serial Interface

ADS5294 has a set of internal registers that can be accessed by the serial interface formed by pins CSZ (Serial interface Enable – Active Low), SCLK (Serial Interface Clock), and SDATA (Serial Interface Data).

When CSZ is low,

- Serial shift of bits into the device is enabled
- Serial data (SDATA) is latched at every rising edge of SCLK
- SDATA is loaded into the register at every 24th SCLK rising edge.

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active CSZ pulse. The first eight bits form the register address and the remaining 16 bits form the register data. The interface works with SCLK frequencies from 15 MHz down to very low speeds (a few Hertz) and also with non-50% SCLK duty cycle.

Programming (continued)

9.5.1.1 Register Initialization

After power-up, initialize the internal registers to the respective default values. Initialization occurs in one of two ways:

1. Through a hardware reset, by applying a high pulse on the RESET pin.
2. Through a software reset: using the serial interface, set the RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the bit low. In this case, the RESET pin stays low (inactive).

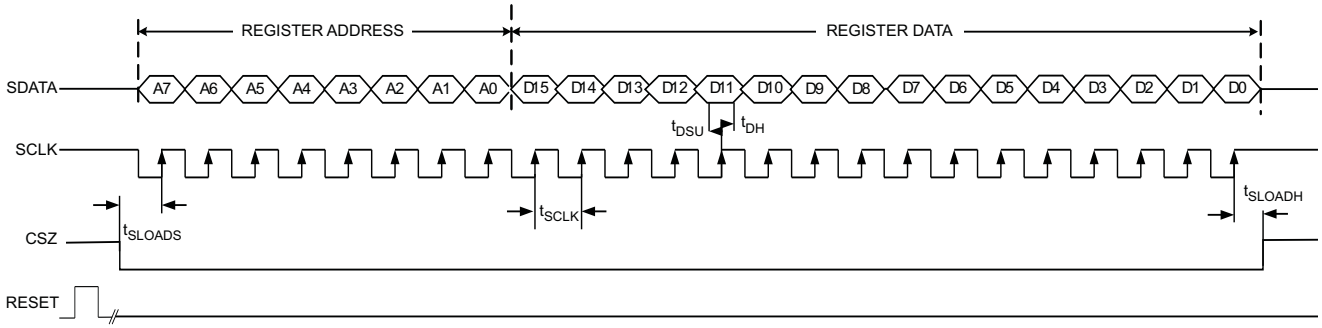

Figure 51. Serial Interface Timing

Please refer to *Serial Interface Timing Requirements* for more details.

9.5.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back on the SDOUT pin. This mode is useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

By default, after power up and device reset, the SDOUT pin is in the high-impedance state. When the readout mode is enabled using the register bit <READOUT>, SDOUT outputs the contents of the selected register serially, described as follows.

- Set register bit <READOUT> = 1 to put the device in serial readout mode. This setting disables any further writes into the internal registers, EXCEPT the register at address 1.
  - Note that the <READOUT> bit itself is also located in register 1.

  The device can exit readout mode by writing <READOUT> to 0.

  Only the contents of register at address 1 cannot be read in the register readout mode.
- Initiate a serial interface cycle specifying the address of the register (A7–A0) whose content is to be read.
- The device serially outputs the contents (D15–D0) of the selected register on the SDOUT pin.
- The external controller can latch the contents at the rising edge of SCLK.
- To exit the serial readout mode, reset register bit <READOUT> = 0, which enables writes into all registers of the device. At this point, the SDOUT pin enters the high-impedance state.

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Programming (continued)

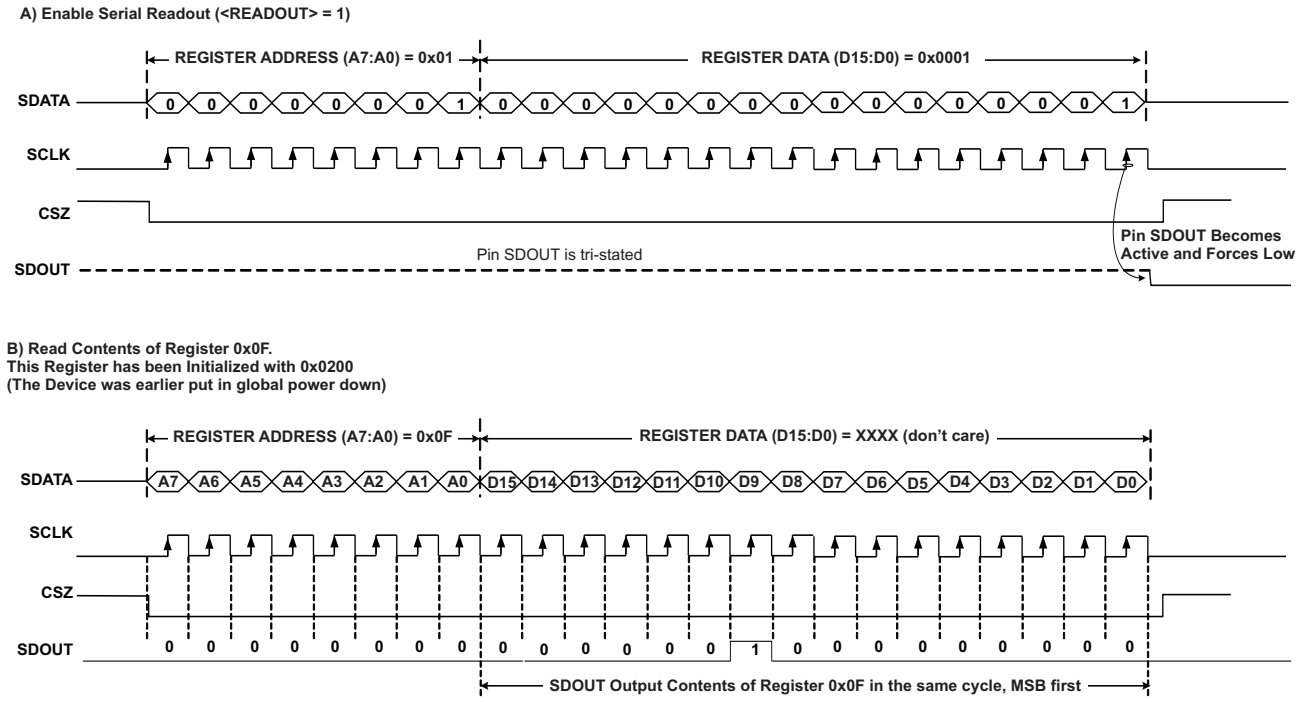

Figure 52. Serial Readout Timing

9.5.1.3 Default States After Reset

- Device is in normal operation mode with 14-bit ADC enabled for all channels
- Output interface is 1-wire, 14×-serialization with 7×-bit clock and 1×-frame clock frequency
- Serial readout is disabled
- PDN pin is configured as global power-down pin
- Digital gain is set to 0 dB
- Digital modes such as LFNS and digital filters are disabled

9.6 Register Maps

Table 6. Summary of Functions Supported by Serial Interface (1)(2)(3)(4)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
00																X	RST	1: Self-clearing software RESET; . After reset, this bit is set to 0 0: Normal operation.
01																X	EN_READOUT	1: READOUT of registers mode;0: Normal operation
												X					EN_HIGH_ADDRS	0 – Disable access to register at address 0xF0 1 – Enable access to register at address 0xF0
02			X														EN_SYNC	1:Enable SYNC feature to synchronize the test patterns; 0: Normal operation, SYNC feature is disabled for the test patterns. Note: this bit needs to be set as 1 when software or hardware SYNC feature is used. see Reg.0x25[8] and 0x25[15]
0A	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RAMP_PAT_RESET_VAL	Ramp pattern reset value
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>	1:Channel-specific ADC power-down mode; 0: Normal operation
								X									PDN_PARTIAL	1:Partial power-down mode - fast recovery from power-down; 0: Normal operation
							X										PDN_COMPLETE	1:Register mode for complete power-down - slower recovery; 0: Normal operation
						X											PDN_PIN_CFG	1:Configures PD pin for partial power-down mode; 0:Configures PD pin for complete power-down mode
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>	1: Channel-specific low-frequency noise suppression mode enable; 0: LFNS disabled
1C		X															EN_FRAME_PAT	1: Enables output frame clock to be programmed through a pattern; 0: Normal operation on frame clock
			X	X	X	X	X	X	X	X	X	X	X	X	X	X	ADCLKOUT<13:0>	14-bit pattern for frame clock on ADCLKP and ADCLKN pins
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>	PRBS pattern starting seed value lower 16 bits
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>	1: Swaps the polarity of the analog input pins electrically; 0: Normal configuration
	X	X	X	X	X	X	X										PRBS_SEED<22:16>	PRBS seed starting value upper 7 bits

(1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.
(2) X = Register bit referenced by the corresponding name and description
(3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.
(4) Multiple functions in a register can be programmed in a single write operation.

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Register Maps (continued)

Table 6. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
25										X	0	0					EN_RAMP	1: Enables a repeating full-scale ramp pattern on the outputs; 0: Normal operation
										0	X	0					DUALCUSTOM_PAT	1:Enables mode wherein output toggles between two defined codes; 0: Normal operation
										0	0	X					SINGLE_CUSTOM_PAT	1: Enables mode wherein output is a constant specified code; 0: Normal operation
															X	X	BITS_CUSTOM1<13:12>	2 MSBs for single custom pattern (and for the first code of the dual custom patterns)
													X	X			BITS_CUSTOM2<13:12>	2 MSBs for second code of the dual custom patterns
								X									TP_SOFT_SYNC	1: Software sync bit for test patterns on all 8 CHs; 0: No sync. Note: in order to synchronize the digital filters using the SYNC pin, this bit must be set as 0.
				X													PRBS_TP_EN	1: PRBS test pattern enable bit; 0: PRBS test pattern disabled
			X														PRBS_MODE_2	PRBS 9 bit LFSR (23bit LFSR is default)
		X															PRBS_SEED_FROM_REG	1: Enable PRBS seed to be chosen from register 0x23 and 0x24; 0: Disabled
	X																TP_HARD_SYNC	1: Enable the external SYNC feature for syncing test patterns. 0: Inactive. Note: in order to synchronize the digital filters using the SYNC pin, this bit must be set as 0.
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>	12 lower bits for single custom pattern (and for the first code of the dual custom pattern).
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>	12 lower bits for second code of the dual custom pattern
28	X																EN_BITORDER	Enables the bit order output. 0 = byte-wise, 1 = word-wise or bit-wise
	X							X									BIT_WISE	Selects between byte-wise and bit-wise 1: bit-wise, odd bits come out on one wire and even bits come out on other wire. D15 must be set to '1' for the bit-wise mode. 0: byte-wise, upper bits on one wire and lower bits on other wire D15 must be set to '0' for the byte-wise mode.
	1								X	X	X	X	X	X	X	X	EN_WORDWISE__BY_CH<7:0>	1: Output format is one sample on one LVDS wire and next sample on other LVDS wire. 0: Data comes out in 2-wire mode with upper set of bits on one channel and lower set of bits on the other. Note: D15 must set to '1' for the word-wise mode.
29															X		GLOBAL_EN_FILTER	1: Enables filter blocks - global control; 0: Inactive
																X	EN_CHANNEL_AVG	1: Enables channel averaging mode; 0: Inactive
2A													X	X	X	X	GAIN_CH1<3:0>	Programmable gain - Channel 1
									X	X	X	X					GAIN_CH2<3:0>	Programmable gain - Channel 2
					X	X	X	X									GAIN_CH3<3:0>	Programmable gain - Channel 3
	X	X	X	X													GAIN_CH4<3:0>	Programmable gain - Channel 4

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Register Maps (continued)

Table 6. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain - Channel 5
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain - Channel 6
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain - Channel 7
													X	X	X	X	GAIN_CH8<3:0>	Programmable gain - Channel 8
2C						X	X										AVG_CTRL4<1:0>	Averaging control for what comes out on LVDS output OUT4
									X	X							AVG_CTRL3<1:0>	Averaging control for what comes out on LVDS output OUT3
												X	X				AVG_CTRL2<1:0>	Averaging control for what comes out on LVDS output OUT2
															X	X	AVG_CTRL1<1:0>	Averaging control for what comes out on LVDS output OUT1
2D						X	X										AVG_CTRL8<1:0>	Averaging control for what comes out on LVDS output OUT8
									X	X							AVG_CTRL7<1:0>	Averaging control for what comes out on LVDS output OUT7
												X	X				AVG_CTRL6<1:0>	Averaging control for what comes out on LVDS output OUT6
															X	X	AVG_CTRL5<1:0>	Averaging control for what comes out on LVDS output OUT5
2E							X	X	X								FILTER1_COEFF_SET<2:0>	Select stored coefficient set for filter 1
										X	X	X					FILTER1_RATE<2:0>	Set decimation factor for filter 1
														X			ODD_TAP1	Use odd tap filter 1
																X	USE_FILTER1	1: Enables filter for channel 1; 0: Disables
			X	X	X	X											HPF_CORNER _CH1	HPF corner in values k from 2 to 10
		X															HPF_EN_CH1	1: HPF filter enable for the channel; 0: Disables
2F							X	X	X								FILTER2_COEFF_SET<2:0>	Select stored coefficient set for filter 2
										X	X	X					FILTER2_RATE<2:0>	Set decimation factor for filter 2
														X			ODD_TAP2	Use odd tap filter 2
																X	USE_FILTER2	1: Enables filter for channel 2; 0: Disables
			X	X	X	X											HPF_CORNER _CH2	HPF corner in values k from 2 to 10
		X															HPF_EN_CH2	1: HPF filter enabled for the channel; 0: Disabled
30							X	X	X								FILTER3_COEFF_SET<2:0>	Select stored coefficient set for filter 3
										X	X	X					FILTER3_RATE<2:0>	Set decimation factor for filter 3
														X			ODD_TAP3	Use odd tap filter 3
																X	USE_FILTER3	1: Enables filter for channel 3; 0: Disables
			X	X	X	X											HPF_CORNER _CH3	HPF corner in values k from 2 to 10
		X															HPF_EN_CH3	1: HPF filter enabled for the channel; 0: Disabled

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Register Maps (continued)

Table 6. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
31							X	X	X								FILTER4_COEFF_SET<2:0>	Select stored coefficient set for filter 4
										X	X	X					FILTER4_RATE<2:0>	Set decimation factor for filter 4
														X			ODD_TAP4	Use odd tap filter 4
																X	USE_FILTER4	1: Enables filter for channel 4; 0: Disables
			X	X	X	X											HPF_CORNER _CH4	HPF corner in values k from 2 to 10
		X															HPF_EN_CH4	1: HPF filter enabled for the channel; 0: Disabled
32							X	X	X								FILTER5_COEFF_SET<2:0>	Select stored coefficient set for filter 5
										X	X	X					FILTER5_RATE<2:0>	Set decimation factor for filter 5
														X			ODD_TAP5	Use odd tap filter 5
																X	USE_FILTER5	1: Enables filter for channel 5; 0: Disables
			X	X	X	X											HPF_CORNER _CH5	HPF corner in values k from 2 to 10
		X															HPF_EN_CH5	1: HPF filter enabled for the channel; 0: Disabled
33							X	X	X								FILTER_TYPE6<2:0>	Select stored coefficient set for filter 6
										X							DECBY8_6	Enables decimate by 8 filter 6
											X	X					FILTER_MODE6<1:0>	Set decimation factor for filter 6
														X			ODD_TAP6	Use odd tap filter 6
																X	USE_FILTER6	Enables filter for channel 6
			X	X	X	X											HPF_CORNER _CH6	HPF corner in values k from 2 to 10
		X															HPF_EN_CH6	HPF filter enable for the channel
34							X	X	X								FILTER_TYPE7<2:0>	Select stored coefficient set for filter 7
										X							DECBY8_7	Enables decimate by 8 filter 7
											X	X					FILTER_MODE7<1:0>	Set decimation factor for filter 7
														X			ODD_TAP7	Use odd tap filter 7
																X	USE_FILTER7	Enables filter for channel 7
			X	X	X	X											HPF_CORNER _CH7	HPF corner in values k from 2 to 10
		X															HPF_EN_CH7	HPF filter enable for the channel
35							X	X	X								FILTER_TYPE8<2:0>	Select stored coefficient set for filter 8
										X							DECBY8_8	Enables decimate by 8 filter 8
											X	X					FILTER_MODE8<1:0>	Set decimation factor for filter 8
														X			ODD_TAP8	Use odd tap filter 8
																X	USE_FILTER8	1: Enables filter for channel 8; 0: Disables
			X	X	X	X											HPF_CORNER_CH8	HPF corner in values k from 2 to 10
		X															HPF_EN_CH8	1: HPF filter enable for the channel; 0: Disables

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Register Maps (continued)

Table 6. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
38															X	X	DATA_RATE<1:0>	Select output frame clock rate. Please see *Output Data Rate Control*.
42	X												X				EXT_REF_VCM	Drive external reference mode through: D15 = D3 = 1: the VCM pin; D15 = D3 = 0: REFT and REFB pins. Note: 0xF0[15] should be set as '1' to enable the external reference mode.
										X	X						PHASE_DDR<1:0>	Controls phase of LCLK output relative to data
45															0	X	PAT_DESKEW	1: Enable deskew pattern mode; 0: Inactive
															X	0	PAT_SYNC	1: Enable sync pattern mode; 0: Inactive
46	1															X	EN_2WIRE	1: 2-wire LVDS output; 0: 1-wire LVDS output. Note: ~250us PLL settling time is required after programming the EN_2WIRE bit from *Default States After Reset*.
	1													X			BTC_MODE	1: 2s complement; (ADC data output format) 0: Binary Offset (ADC data output format)
	1												X				MSB_FIRST	1: MSB First; 0: LSB First
	1											X					EN_SDR	1:SDR Bit Clock; 0: DDR Bit Clock
	1				X	X	X	X									EN_BIT_SER	Output serialization mode. 0001: 10 bit (EN_10BIT) 0010: 12 bit (EN_12BIT) 0100: 14 bit (EN_14BIT) 1000: 16 bit (EN_16BIT)
	1		X														FALL_SDR	1: Controls LCLK rising or falling edge comes in the middle of data window when operating in SDR output mode; 0: At the edge of data window.
50	1												X	X	X	X	MAP_Ch1234_to_OUT1A	OUT1A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT1B	OUT1B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT2A	OUT2A Pin pair to channel data mapping selection
51	1												X	X	X	X	MAP_Ch1234_to_OUT2B	OUT2B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT3A	OUT3A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch1234_to_OUT3B	OUT3B Pin pair to channel data mapping selection
52	1												X	X	X	X	MAP_Ch1234_to_OUT4A	OUT4A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch1234_to_OUT4B	OUT4B Pin pair to channel data mapping selection
53	1												X	X	X	X	MAP_Ch5678_to_OUT5B	OUT5B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT5A	OUT5A Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT6B	OUT6B Pin pair to channel data mapping selection
54	1												X	X	X	X	MAP_Ch5678_to_OUT6A	OUT6A Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT7B	OUT7B Pin pair to channel data mapping selection
	1				X	X	X	X									MAP_Ch5678_to_OUT7A	OUT7A Pin pair to channel data mapping selection

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Register Maps (continued)

Table 6. Summary of Functions Supported by Serial Interface (1)(2)(3)(4) (continued)

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
55	1												X	X	X	X	MAP_Ch5678_to_OUT8B	OUT8B Pin pair to channel data mapping selection
	1								X	X	X	X					MAP_Ch5678_to_OUT8A	OUT8A Pin pair to channel data mapping selection
F0	X																EN_EXT_REF	1: Enable external reference mode. the voltage reference can be applied on either REFP and REFB pins or VCM pin. 0: Default: internal reference mode.

9.6.1 Description Of Serial Registers

9.6.1.1 Power-Down Modes

Table 7. Power-Down Mode Register

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>
								X									PDN_PARTIAL
							X										PDN_COMPLETE
						X											PDN_PIN_CFG

Each of the eight channels can be individually powered down. PDN_CH<N> controls the power-down mode for ADC channel <N>. In addition to channel-specific power-down, the ADS5294 also has two global power-down modes:

1. The partial power-down mode partially powers down the chip. Recovery time from the partial power-down mode is about 10 µs provided that the clock has been running for at least 50 µs before exiting this mode.
2. The complete power-down mode completely powers down the chip This mode involves a much longer recovery time 100 µs.

In addition to programming the chip in either of these two power-down modes (through either the PDN_PARTIAL or PDN_COMPLETE bits), the PD pin itself can be configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN_PIN_CFG=0 (default), when the PD pin is high, the device enters complete power-down mode. However, if PDN_PIN_CFG=1, when the PD pin is high, the device enters partial power-down mode.

9.6.1.2 Low Frequency Noise Suppression Mode

Table 8. Low Frequency Noise Suppression Mode Register

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14									X	X	X	X	X	X	X	X	LFNS_CH<8:1>

The low-frequency noise suppression mode is useful in applications where good noise performance is desired in the frequency band of 0 to 1 MHz (around DC). Setting this mode shifts the low-frequency noise of the ADS5294 to approximately Fs / 2, thereby, moving the noise floor around DC to a much lower value. LFNS_CH<8:1> enables this mode individually for each channel. See Figure 38 and Figure 39.

9.6.1.3 Analog Input Invert

Table 9. Analog Input Invert Register

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
24									X	X	X	X	X	X	X	X	INVERT_CH<8:1>

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Generally, IN_P pin represents the positive analog input pin, and INN represents the complementary negative input. Setting the bits marked INVERT_CH<8:1> (individual control for each channel) causes the inputs to be swapped. IN_N now represents the positive input, and IN_P the negative input.

9.6.1.4 LVDS Test Patterns

Table 10. LVDS Test Patterns

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
23	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	PRBS_SEED<15:0>
24	X	X	X	X	X	X	X										PRBS_SEED<22:16>
25										X	0	0					EN_RAMP
										0	X	0					DUALCUSTOM_PAT
										0	0	X					SINGLE_CUSTOM_PAT
															X	X	BITS_CUSTOM1<13:12>
													X	X			BITS_CUSTOM2<13:12>
								X									TP_SOFT_SYNC
				X													PRBS_TP_EN
			X														PRBS_MODE_2
		X															PRBS_SEED_FROM_REG
	X																TP_HARD_SYNC
26	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM1<11:0>
27	X	X	X	X	X	X	X	X	X	X	X	X					BITS_CUSTOM2<11:0>
45															0	X	PAT_DESKEW
															X	0	PAT_SYNC

The ADS5294 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. All these patterns can be synchronized across devices by the sync function either through the hardware SYNC pin or the software sync bit TP_SOFT_SYNC bit in register 0x25. When set, the TP_HARD_SYNC bit enables the test patterns to be synchronized by the hardware SYNC Pin. When the software sync bit TP_SOFT_SYNC is set, special timing is needed.

- Setting EN_RAMP to '1' causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1 LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.
- The device can also be programmed to output a constant code by setting SINGLE_CUSTOM_PAT to '1', and programming the desired code in BITS_CUSTOM1<13:0>. In this mode, BITS_CUSTOM1<13:0> take the place of the 14-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes the same way as normal ADC data are controlled.
- The device can also toggle between two consecutive codes, by programming DUAL_CUSTOM_PAT to '1'. The two codes are represented by the contents of BITS_CUSTOM1<13:0> and BITS_CUSTOM2<13:0>.
- In addition to custom patterns, the device may also be made to output two preset patterns:
  - **Deskew patten –** Set using PAT_DESKEW, this mode replaces the 14-bit ADC output D<13:0> with the 0101010101010101 word.
  - **Sync pattern –** Set using PAT_SYNC, the normal ADC word is replaced by a fixed 11111110000000 word.
  - **PRBS patterns –** The device can give 9-bit or 23-bit LFSR Pseudo random pattern on the channel outputs that are controlled by the register 0x25. To enable the PRBS pattern **PRBS_TP_EN** bit in the register 0x25 needs to be set. The default is the 23-bit LFSR. To select the 9-bit LFSR, set the **PRBS_MODE_2** bit. The seed value for the PRBS patterns can be chosen by enabling the **PRBS_SEED_FROM_REG** bit to 1 and the value written to the PRBS_SEED registers in 0x24 and 0x23.

NOTE

Only one of these patterns should be active at any given instant.

9.6.1.5 Bit-Byte-Word Wise Output

Table 11. Bit-Byte-Word Wise Output

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
28	x																EN_BITORDER
	1							x									BIT_WISE
	1								X	X	X	X	X	X	X	X	EN_WORDWISE_BY_CH<7:>

Register 0x28 selects the LVDS ADC output as bit-wise, byte-wise, or word-wise in the 2-wire mode. Figure 53 and Figure 54 show the details.

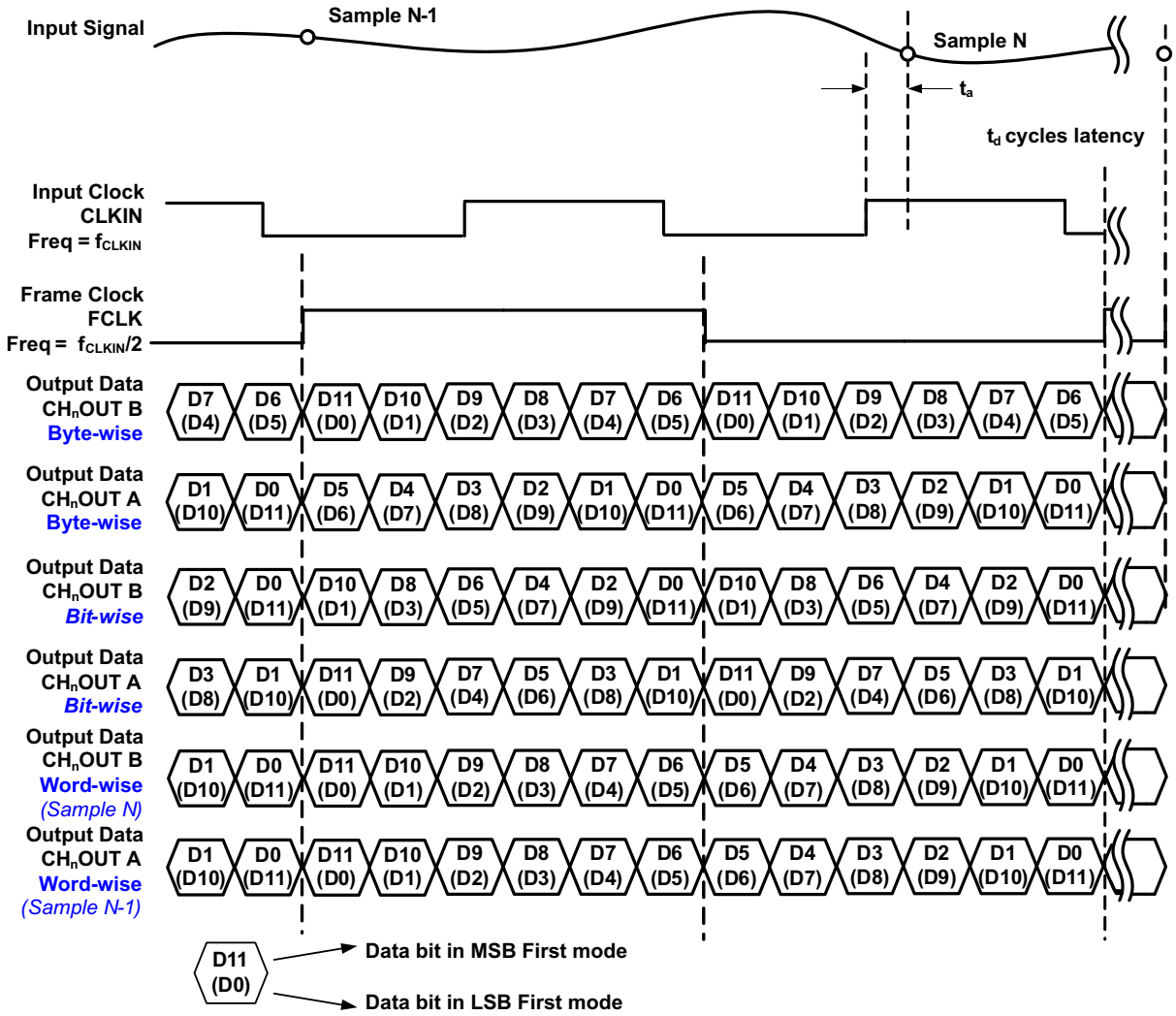

Figure 53. 12-Bit Word Wise

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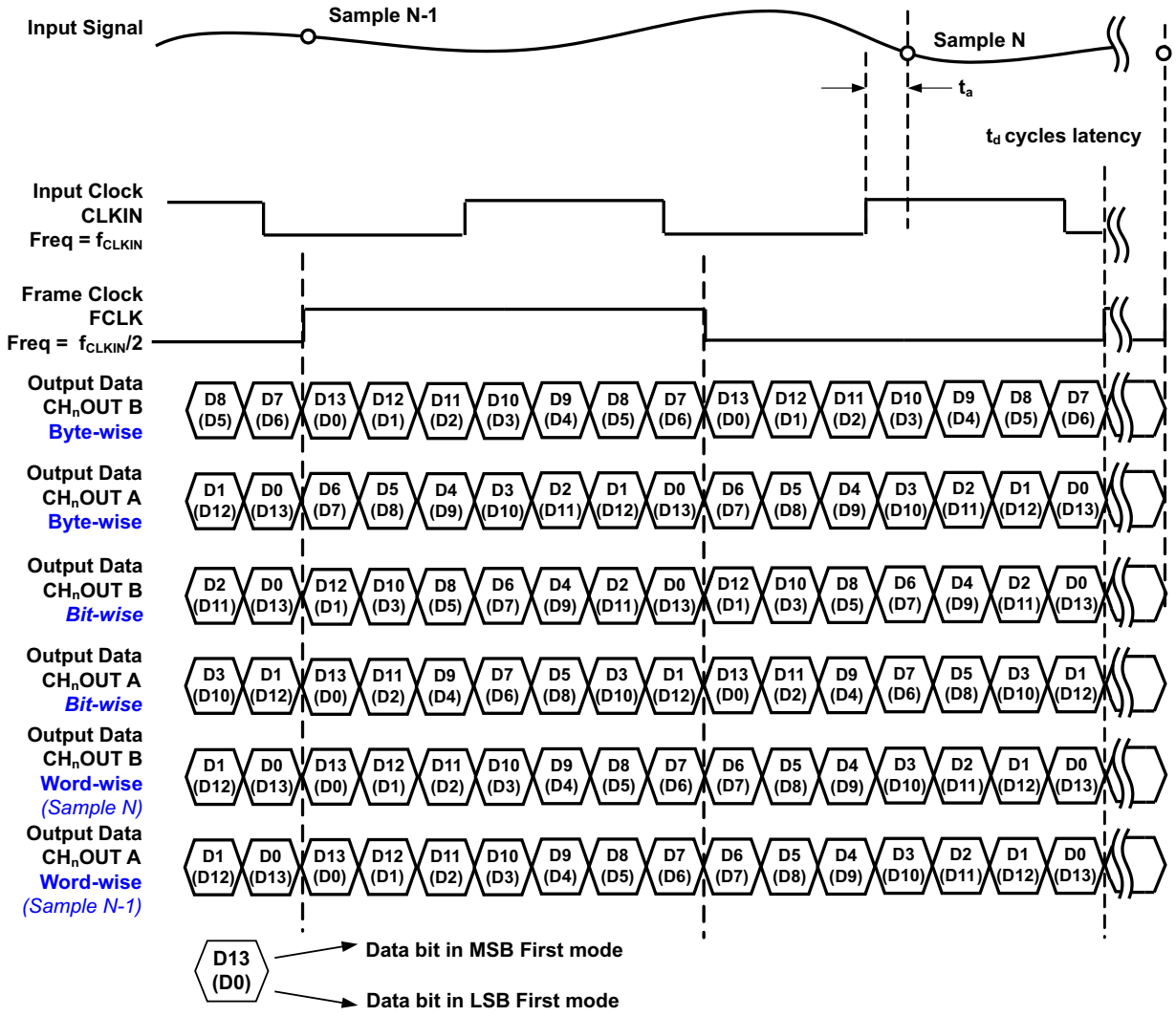

Figure 54. 14-Bit Word Wise

9.6.1.6 Digital Processing Blocks

The ADS5294 integrates a set of commonly-used digital functions to ease system design. These functions are shown in the digital block diagram of Figure 55 and described in the following sections.

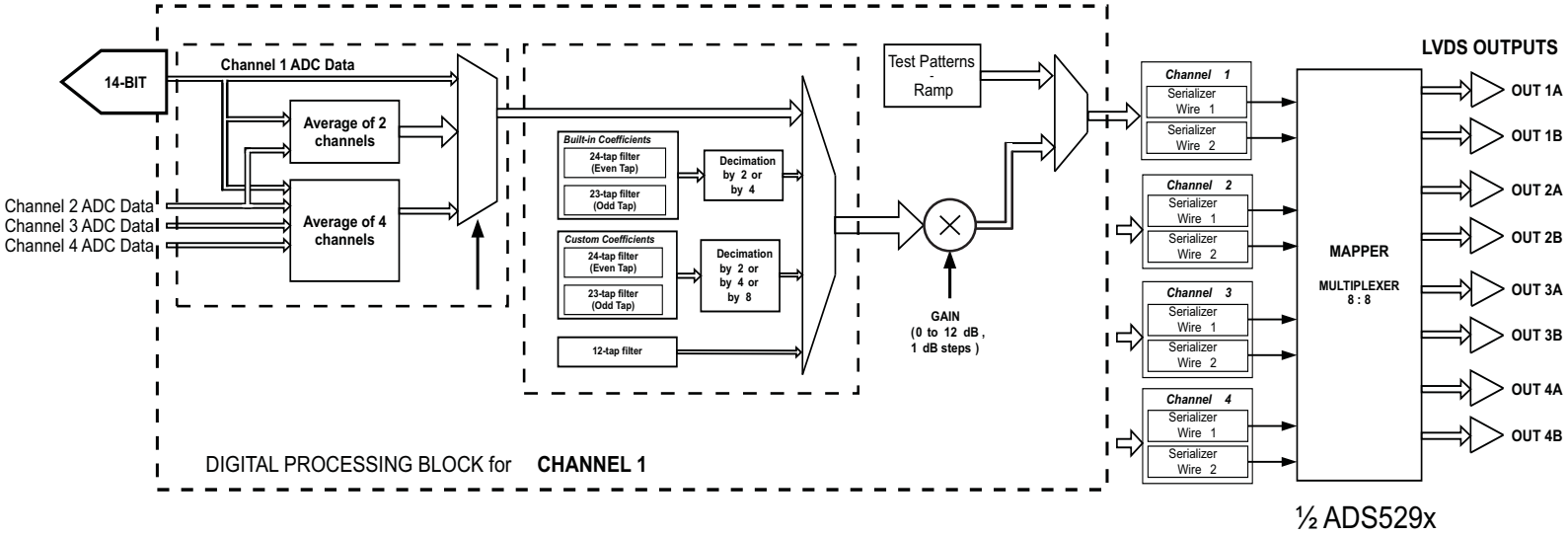

Figure 55. Digital Processing Block Diagram

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9.6.1.7 Programmable Digital Gain

Table 12. Programmable Digital Gain

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A													X	X	X	X	GAIN_CH1<3:0>
									X	X	X	X					GAIN_CH2<3:0>
					X	X	X	X									GAIN_CH3<3:0>
	X	X	X	X													GAIN_CH4<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

In applications where the full-scale swing of the analog input signal is much less than the 2 V_{PP} range supported by the ADS5294, a programmable gain is set to achieve the full-scale output code even with a lower analog input swing. The programmable gain for each channel is set individually using a set of four bits, indicated as GAIN_CHN<3:0> for Channel N. The gain setting is coded in binary from 0 to 12 dB as shown in Table 13.

Table 13. Gain Setting for Channel N

GAIN_CHN<3>	GAIN_CHN<2>	GAIN_CHN<1>	GAIN_CHN<0>	CHANNEL N GAIN SETTING
0	0	0	0	0 dB
0	0	0	1	1 dB
0	0	1	0	2 dB
0	0	1	1	3 dB
0	1	0	0	4 dB
0	1	0	1	5 dB
0	1	1	0	6 dB
0	1	1	1	7 dB
1	0	0	0	8 dB
1	0	0	1	9 dB
1	0	1	0	10 dB
1	0	1	1	11 dB
1	1	0	0	12 dB
1	1	0	1	Do not use
1	1	1	0	Do not use
1	1	1	1	Do not use

9.6.1.8 Channel Averaging

Table 14. Channel Averaging

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29																X	EN_CHANNEL_AVG
2C						X	X										AVG_CTRL4<1:0>
									X	X							AVG_CTRL3<1:0>
												X	X				AVG_CTRL2<1:0>
															X	X	AVG_CTRL1<1:0>
2D						X	X										AVG_CTRL8<1:0>
									X	X							AVG_CTRL7<1:0>
												X	X				AVG_CTRL6<1:0>
															X	X	AVG_CTRL5<1:0>

In the default mode of operation, the LVDS outputs <8..1> contain the data of the ADC Channels <8..1>. By setting the EN_CHANNEL_AVG bit to '1', the outputs from multiple channels can be averaged. The resulting outputs from the Channel averaging block (which is bypassed in the default mode) are referred to as Bins. The contents of the Bins <8..1> come out on the LVDS outputs <8..1>. The contents of each of the eight Bins are determined by the register bits marked AVG_CTRL*n*<1:0> where *n* stands for the Bin number. The different settings are shown in the following table:

Table 15. Channel Averaging

AVG_CTRL1<1>	AVG_CTRL1<0>	Contents of Bin 1
0	0	Zero
0	1	ADC Channel 1
1	0	Average of ADC Channel 1, 2
1	1	Average of ADC Channel 1, 2, 3, 4
AVG_CTRL2<1>	**AVG_CTRL2<0>**	**Contents of Bin 2**
0	0	Zero
0	1	ADC Channel 2
1	0	ADC Channel 3
1	1	Average of ADC Channel 3, 4
AVG_CTRL3<1>	**AVG_CTRL3<0>**	**Contents of Bin 3**
0	0	Zero
0	1	ADC Channel 3
1	0	ADC Channel 2
1	1	Average of ADC Channel 1, 2
AVG_CTRL4<1>	**AVG_CTRL4<0>**	**Contents of Bin 4**
0	0	Zero
0	1	ADC Channel 4
1	0	Average of ADC Channel 3, 4
1	1	Average of ADC Channel 1, 2, 3, 4
AVG_CTRL5<1>	**AVG_CTRL5<0>**	**Contents of Bin 5**
0	0	Zero
0	1	ADC Channel 5
1	0	Average of ADC Channel 5, 6
1	1	Average of ADC Channel 5, 6, 7, 8
AVG_CTRL6<1>	**AVG_CTRL6<0>**	**Contents of Bin 6**
0	0	Zero
0	1	ADC Channel 6
1	0	ADC Channel 7
1	1	Average of ADC Channel 7, 8
AVG_CTRL7<1>	**AVG_CTRL7<0>**	**Contents of Bin 7**
0	0	Zero
0	1	ADC Channel 7
1	0	ADC Channel 6
1	1	Average of ADC Channel 6, 5
AVG_CTRL8<1>	**AVG_CTRL8<0>**	**Contents of Bin 8**
0	0	Zero
0	1	ADC Channel 8
1	0	Average of ADC Channel 7, 8
1	1	Average of ADC Channel 5, 6, 7, 8

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When the contents of a particular Bin is set to zero, then the LVDS buffer corresponding to that Bin gets automatically powered down.

9.6.1.9 Decimation Filter

Table 16. Decimation Filter

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
29															X		GLOBAL_EN_FILTER
2E							X	X	X								FILTER1_COEFF_SET<2:0>
										X	X	X					FILTER1_RATE<2:0>
														X			ODD_TAP1
																X	USE_FILTER1
2F							X	X	X								FILTER2_COEFF_SET<2:0>
										X	X	X					FILTER2_RATE<2:0>
														X			ODD_TAP2
																X	USE_FILTER2
30							X	X	X								FILTER3_COEFF_SET<2:0>
										X	X	X					FILTER3_RATE<2:0>
														X			ODD_TAP3
																X	USE_FILTER3
31							X	X	X								FILTER4_COEFF_SET<2:0>
										X	X	X					FILTER4_RATE<2:0>
														X			ODD_TAP4
																X	USE_FILTER4
32							X	X	X								FILTER5_COEFF_SET<2:0>
										X	X	X					FILTER5_RATE<2:0>
														X			ODD_TAP5
																X	USE_FILTER5
33							X	X	X								FILTER6_COEFF_SET<2:0>
										X	X	X					FILTER6_RATE<2:0>
														X			ODD_TAP6
																X	USE_FILTER6
34							X	X	X								FILTER7_COEFF_SET<2:0>
										X	X	X					FILTER7_RATE<2:0>
														X			ODD_TAP7
																X	USE_FILTER7
35							X	X	X								FILTER8_COEFF_SET<2:0>
										X	X	X					FILTER8_RATE<2:0>
														X			ODD_TAP8
																X	USE_FILTER8

The decimation filter is implemented as 24-tap FIR with symmetrical coefficients (each coefficient is 12-bit signed). The filter equation is:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times \left[(h_0 \times x(n) + h_1 \times x(n-1) + h_2 \times x(n-2) + \ldots + h_{11} \times x(n-11) + h_{11} \times x(n-12) \ldots + h_1 \times x(n-22) + h_0 \times x(n-23)\right] \quad (2)$$

By setting the register bit <ODD_TAPn> = 1, a 23-tap FIR is implemented:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times \left[(h_0 \times x(n) + h_1 \times x(n-1) + h_2 \times x(n-2) + \ldots + h_{10} \times x(n-10) + h_{11} \times x(n-11) + h_{10} \times x(n-12) \ldots + h_1 \times x(n-21) + h_0 \times x(n-22)\right] \quad (3)$$

In Equation 2 and Equation 3, *h0, h1 …*h_{11} are 12-bit signed representation of the coefficients, *x(n)* is the input data sequence to the filter and *y(n)* is the filter output sequence.

A decimation filter can be introduced at the output of each channel. To enable this feature, the GLOBAL_EN_FILTER should be set to ‘1’. Setting this bit to ‘1’ increases the overall latency of each channel to 20 clock cycles irrespective of whether the filter for that particular channel has been chosen or not (using the USE_FILTER bit). The bits marked FILTER*n*_COEFF_SET<2:0>, FILTER*n*_RATE<2:0>, ODD_TAP*n* and USE_FILTER*n* represent the controls for the filter for Channel *n*. Note that these bits are functional only when the GLOBAL_EN_FILTER gets set to '1' and USE_FILTERn bit is set to '1'. For illustration, the controls for channel 1 are listed in Table 17:

The USE_FILTER1 bit determines whether the filter for Channel 1 is used or not. When this bit is set to ‘1’, the filter for channel 1 is enabled. When this bit is set to ‘0’, the filter for channel 1 is disabled but the channel data passes through a dummy delay so that the overall latency of channel 1 is 20 clock cycles. With the USE_FILTER1 bit set to ‘1’, the characteristics of the filter can be set by using the other sets of bits.

The ADS5294 has six sets of filter coefficients stored in memory. Each of these sets define a unique pass band in the frequency domain and contain 12 coefficients (each coefficient is 12-bit long). These 12 coefficients are used to implement either a symmetric 24-tap (even-tap) filter, or a symmetric 23-tap (odd-tap) filter. Setting the register bit ODD_TAP1 to ‘1’ enables the odd-tap configuration (the default is even tap with this bit set to ‘0’) for Channel 1. The bits FILTER1_COEFF_SET<2:0> are used to choose the required set of coefficients for Channel 1.

The passbands corresponding to of each of these filter coefficient sets is shown in Figure 56

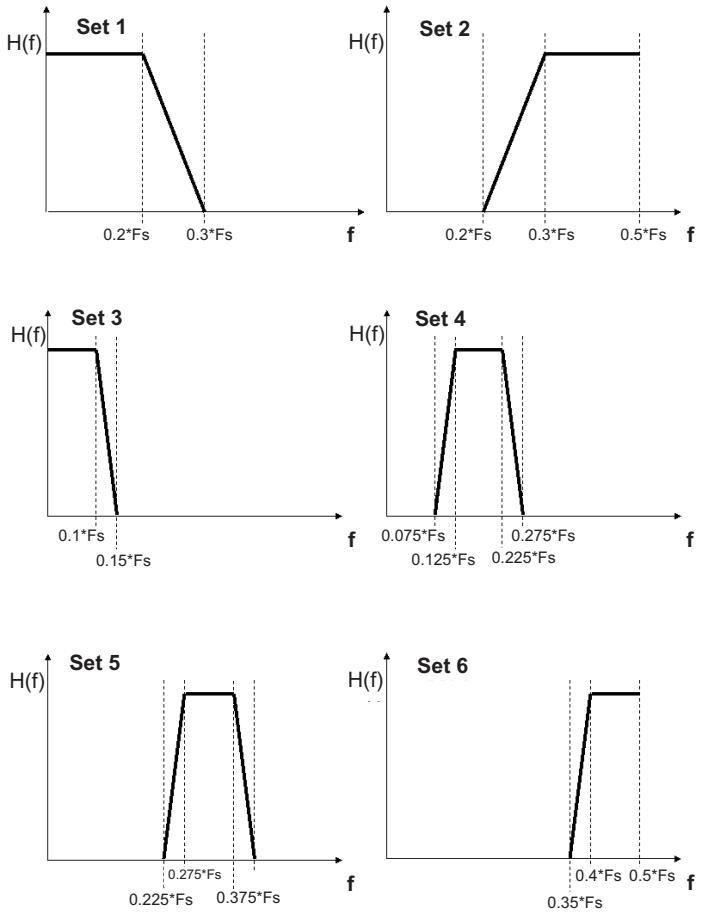

Figure 56. Filter Types

Coefficient Sets 1 and 2 are the most appropriate when decimation by a factor of 2 is required, whereas Coefficient Sets 3, 4, 5, and 6 are appropriate when decimation by a factor of 4 is desired. The computation rate of the filter output is set independently using the bits FILTERn_RATE<2:0>. The settings are shown in Table 17.

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Table 17. Digital Filters

DECIMATION	TYPE OF FILTER	DATA_RATE>	FILTERn_RATE	FILTERn_COEFF_SET	ODD_TAP	USE_FILTER_CHn	EN_CUSTOM_FILT
Decimate by 2	Built-in **low-pass odd-tap** filter (pass band = 0 to $f_S/4$)	01	000	000	1	1	0
	Built-in **highpass odd-tap** filter (pass band = $f_S/4$ to $f_S/2$)	01	000	001	1	1	0
Decimate by 4	Built-in **lowpass even-tap** filter (pass band = 0 to $f_S/8$)	10	001	010	0	1	0
	Built-in first **bandpass even tap** filter(pass band = $f_S/8$ to $f_S/4$)	10	001	011	0	1	0
	Built-in second **bandpass even tap** filter(pass band = $f_S/4$ to 3 $f_S/8$)	10	001	100	0	1	0
	Built-in **highpass odd tap** filter (pass band = 3 $f_S/8$ to $f_S/2$)	10	001	101	1	1	0
Decimate by 2	Custom filter (user-programmable coefficients)	01	000	000	0 and 1	1	1
Decimate by 4	Custom filter (user-programmable coefficients)	10	001	000	0 and 1	1	1
Decimate by 8	Custom filter (user-programmable coefficients)	11	100	000	0 and 1	1	1
Bypass decimation	Custom filter (user-programmable coefficients)	00	011	000	0 and 1	1	1
Note: EN_CUSTOM_FILT is the D15 of register 5A (Hex) to B9 (Hex).							

The choice of the odd or even tap setting, filter coefficient set, and the filter rate uniquely determines the filter to be used. In addition to the preset filter coefficients, the coefficients for each of the eight filter channels can be programmed by the user. Each of the eight channels has 12 programmable coefficients, each 12-bit long. The 96 registers with addresses from 5A (Hex) to B9 (Hex) are used to program these eight sets of 12 programmable coefficients. Registers 5A to 65 are used to program the first filter, with the first coefficient occupying the bits D11..D0 of register 5A, the second coefficient occupying the bits D11..D0 of register 5B, and so on. Similarly registers 66 (Hex) to 71 (Hex) are used to program the second filter, and so on.

When programming the filter coefficients, the D15 bit, EN_CUSTOM_FILT, of each of the 12 registers corresponding to that filter should be set to ‘1’. If the D15 bit of these 12 registers is set to ‘0’, then the preset coefficient (as programmed by FILTERn_COEFF_SET<2:0>) is used even if the bits D11..D0 get programmed. By setting or not setting the D15 bits of individual filter channels to ‘1’, some filters can be made to operate with preset coefficient sets, and some others can be made to simultaneously operate with programmed coefficient sets.

9.6.1.10 Highpass Filter

Table 18. Highpass Filter

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2E			X	X	X	X											HPF_corner_CH1
2E		X															HPF_EN_CH1
2F			X	X	X	X											HPF_corner_CH2
2F		X															HPF_EN_CH2
30			X	X	X	X											HPF_corner_CH3
30		X															HPF_EN_CH3
31			X	X	X	X											HPF_corner_CH4
31		X															HPF_EN_CH4
32			X	X	X	X											HPF_corner_CH5
32		X															HPF_EN_CH5
33			X	X	X	X											HPF_corner_CH6
33		X															HPF_EN_CH6
34			X	X	X	X											HPF_corner_CH7
34		X															HPF_EN_CH7
35			X	X	X	X											HPF_corner_CH8
35		X															HPF_EN_CH8

This group of registers controls the characteristics of a digital highpass transfer function applied to the output data, using Equation 4:

$$y(n) = \frac{2^k}{2^k+1}[x(n) - x(n-1) + y(n-1)]$$

where

- k is set as described by the HPF_corner registers (one for each channel). (4)

The HPF_EN bit in each register must be set to enable the HPF feature for each channel.

9.6.1.11 Bit-Clock Programmability

Table 19. Bit-Clock Programmability

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42										X	X						PHASE_DDR<1:0>
46	1											X					EN_SDR
46	1		X														FALL_SDR

The output interface of the ADS5294 is normally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. This default phase is shown in Figure 57.

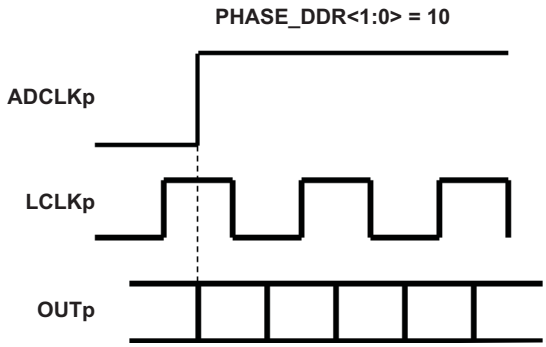

Figure 57. Default Phase of LCLK

The phase of LCLK is programmed relative to the output frame clock and data using bits PHASE_DDR<1:0>. The LCLK phase modes are shown in Figure 58.

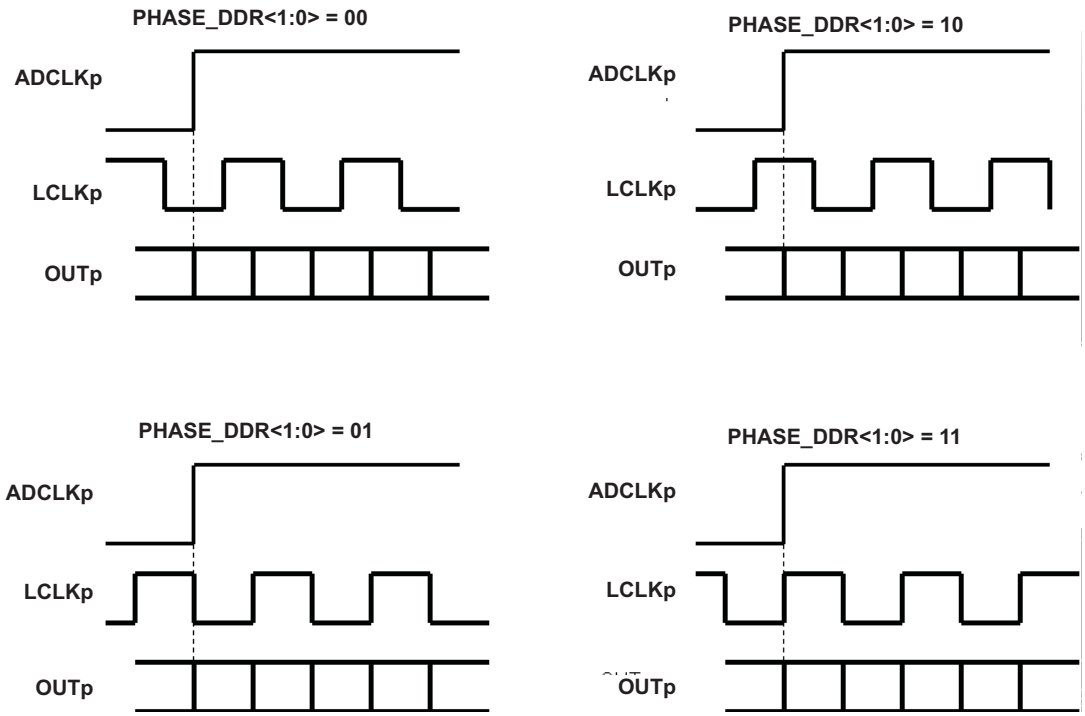

Figure 58. Phase Programmability Modes for LCLK

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In addition to programming the phase of the LCLK in the DDR mode, the device also operates in SDR mode by setting bit EN_SDR to 1. In SDR mode, the bit clock (LCLK) is output at 14-times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL_SDR, the LCLK may be output in either of the two manners shown in Figure 59. As can be seen in Figure 59, only the LCLK rising (or falling edge) is used to capture the output data in SDR mode. The SDR mode does not work well beyond 40 MSPS because the LCLK frequency will become very high.

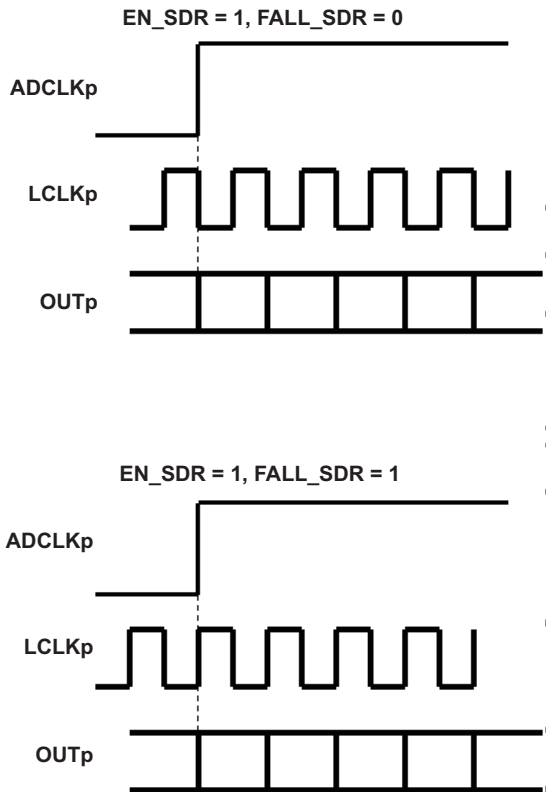

Figure 59. SDR Interface Modes

9.6.1.12 Output Data Rate Control

Table 20. Output Data Rate Control

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38															DATA_RATE<1>	DATA_RATE<0>

In the default mode of operation, the data rate at the output of the ADS5294 is at the sampling rate of the ADC which is true even when the custom pattern generator is enabled. In addition, both output data rate and sampling rate can be configured to a sub-multiple of the input clock rate.

With the DATA_RATE<1:0> control, the output data rate is programmed to be a sub-multiple of the ADC sampling rate. This feature is used to lower the output data rate, for example, when the decimation filter is used. Without enabling the decimation filter, the sub-multiple ADC sampling rate feature is used.

The different settings are listed in Table 21.

Table 21. Output Data Rates

DATA_RATE<1>	DATA_RATE<0>	OUTPUT DATA RATE
0	0	Same as ADC sampling rate
0	1	1 / 2 of ADC sampling rate
1	0	1 / 4 of ADC sampling rate

Table 21. Output Data Rates (continued)

DATA_RATE<1>	DATA_RATE<0>	OUTPUT DATA RATE
1	1	1 / 8 of ADC sampling rate

9.6.1.13 Synchronization Pulse

Table 22. Synchronization Pulse

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
25	TP_HARD_SYNC															
02			EN_SYNC													

The SYNC pin synchronizes the data output from channels within the same chip or from channels across chips when decimation filters are used with reduced output data rate.

When the decimation filters are used (for example, the decimate-by-two filter is enabled), then, effectively, the device outputs one digital code for every two analog input samples. If the SYNC function is not enabled, then the filters are not synchronized (even within a chip) which means that one channel is sending out codes corresponding to input samples N, N + 1 and so on, while another may be sending out code corresponding to N + 1, N + 2, and so on.

To achieve synchronization, the SYNC pulse must arrive at all the ADS529x chips at the same time instant (as shown in the timing diagram of Figure 60

The ADS5294 generates an internal synchronization signal which is used to reset the internal clock dividers used by the decimation filter.

Using the SYNC signal in this way ensures that all channels will output digital codes corresponding to the same set of input samples.

SYNC Timings:

Synchronizing the filters using the SYNC pin is enabled by default. No register bits are required to be written. Even EN_SYNC bit is not required.It is important for register bit TP_HARD_SYNC to be 0 for this mode to work. As shown by Figure 60, the SYNC rising edge can be positioned anywhere within the window. The width of the SYNC must be at least one clock cycle.

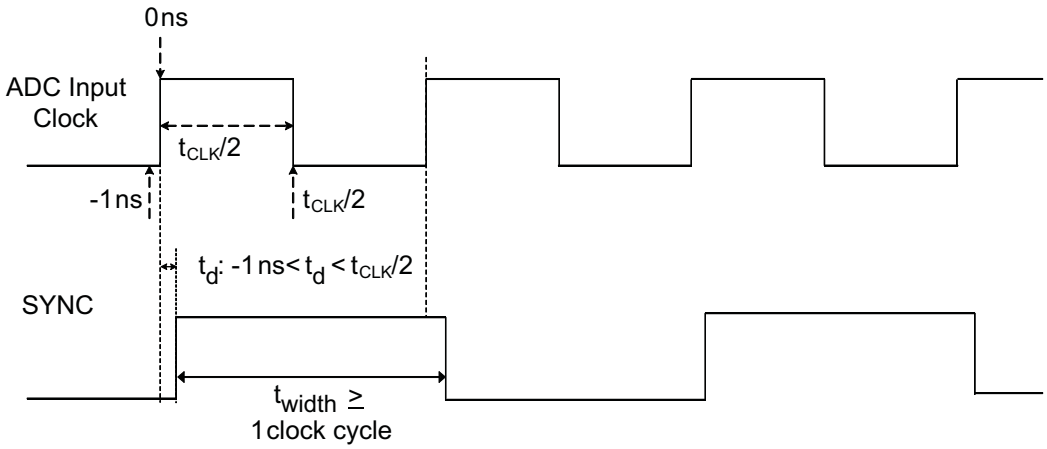

Figure 60. Synchronization Pulse Timing

Note that the SYNC DOES NOT synchronize the sampling instants of the ADC across chips. All channels within a single chip sample their analog inputs simultaneously. The input clock needs to be routed to both chips with identical length to ensure that channels across two chips will sample their analog inputs simultaneously. Taking this step ensures that the input clocks arrive at both of the chips at the same time. This should be handled in the board design and routing. The SYNC pin cannot be used to synchronize the sampling instants.

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In addition to the above, the SYNC also synchronizes the RAMP test patterns across channels. In order to synchronize the test patterns, TP_HARD_SYNC must be set as '1'. Setting TP_HARD_SYNC = 1 actually disables the sync of the filters.

9.6.1.14 External Reference Mode of Operation

The ADS5294 supports an external reference mode of operation in one of two ways:

a. By forcing the reference voltages on the REFT and REFB pins.
b. By applying the reference voltage on VCM pin.

This mode can be used to operate multiple ADS5294 chips with the same (externally applied) reference voltage.

Using the REF pins:

For normal operation, the device requires two reference voltages: REFT and REFB. By default, the device generates these two voltages internally. To enable the external reference mode, set the register bits as shown in Table 23 which powers down the internal reference amplifier and the two reference voltages are forced directly on the REFT and REFB pins as VREFT = 1.45 V ± 50 mV and VREFB = 0.45 V ±50 mV.

Note that the relation between the ADC full-scale input voltage and the applied reference voltages is

$$\text{Full-scale input voltage} = 2 \times (\text{VREFT} - \text{VREFB}) \quad (5)$$

Using the VCM pin:

In this mode, an external reference voltage VREFIN can be applied to the VCM pin such that

$$\text{Full-scale input voltage} = 2 \times \text{VREFIN} \times (2 / 3) \quad (6)$$

To enable this mode, set the register bits as shown in Table 23 which changes the function of the VCM pin to an external reference input pin. The voltage applied on VCM must be 1.5 V ±50 mV.

Table 23. External Reference Function

Function	EN_HIGH_ADDRS (0x1[4])	EN_EXT_REF (0xF0[15])	EXT_REF_VCM (0x42[15,3])
External reference using REFT and REFB pins	1	1	00
External reference using VCM pin	1	1	11

9.6.1.15 Data Output Format Modes

Table 24. Data Output Format Modes

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
46	1													X			BTC_MODE
46	1												X				MSB_FIRST

By default, the ADC output is in straight-offset binary mode. Programming the BTC_MODE bit to '1' inverts the MSB, and the output becomes Binary 2s-complement mode. Also by default, the first bit of the frame (following the rising edge of CLKP) is the LSB of the ADC output. Programming the MSB_FIRST mode inverts the bit order in the word, and the MSB is output as the first bit following CLKP rising edge.

9.6.1.16 Programmable Mapping Between Input Channels and Output Pins

Table 25. Mapping Between Input Channels and Output Pins

ADDR. (HEX)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
50	1												X	X	X	X	MAP_CH1234_TO_OUT1A
	1								X	X	X	X					MAP_CH1234_TO_OUT1B
	1				X	X	X	X									MAP_CH1234_TO_OUT2A
51	1												X	X	X	X	MAP_CH1234_TO_OUT2B
	1								X	X	X	X					MAP_CH1234_TO_OUT3A
	1				X	X	X	X									MAP_CH1234_TO_OUT3B
52	1								X					X	X	X	MAP_CH1234_TO_OUT4A
	1								X	X	X	X					MAP_CH1234_TO_OUT4B
53	1												X	X	X	X	MAP_CH5678_TO_OUT5B
	1								X	X	X	X					MAP_CH5678_TO_OUT5A
	1				X	X	X	X									MAP_CH5678_TO_OUT6B
54	1												X	X	X	X	MAP_CH5678_TO_OUT6A
	1								X	X	X	X					MAP_CH5678_TO_OUT7B
	1				X	X	X	X									MAP_CH5678_TO_OUT7A
55	1												X	X	X	X	MAP_CH5678_TO_OUT8B
	1								X	X	X	X					MAP_CH5678_TO_OUT8A

The ADS5294 has 16 pairs of LVDS channel outputs. The mapping of ADC channels to LVDS output channels is programmable to allow for flexibility in board layout. The 16 LVDS channel outputs are split into two groups of eight LVDS pairs. Within each group four ADC input channels are multiplexed into the eight LVDS pairs depending on the modes of operation whether it is in 1-wire mode or 2-wire mode.

Input channels 1 to 4 map to any of the LVDS outputs OUT1A or OUT1B to OUT4A or OUT4B (using the MAP_CH1234_TO_OUTnA or OUTnB). Similarly, input channels 5 to 8 can be mapped to any of the LVDS outputs OUT5A or OUT5B to OUT8A or OUT8B (using the MAP_CH5678_TO_OUTnA or OUTnB). The block diagram of the mapping is listed in Figure 61.

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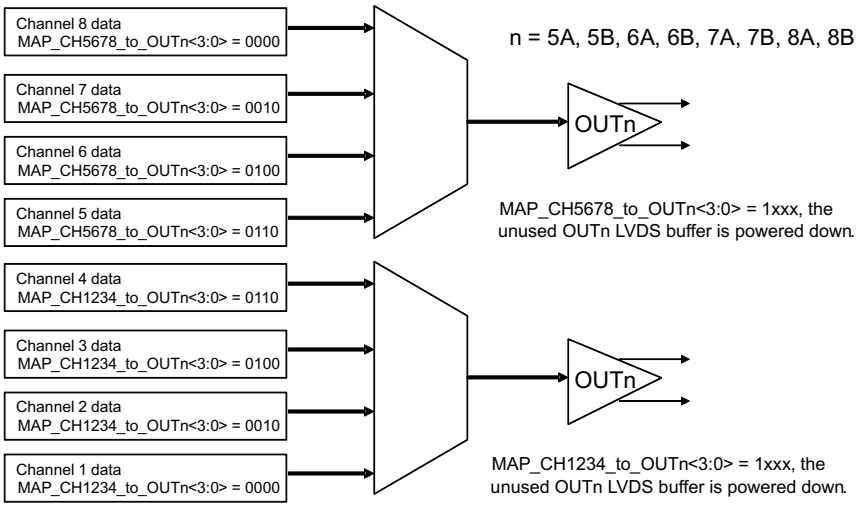
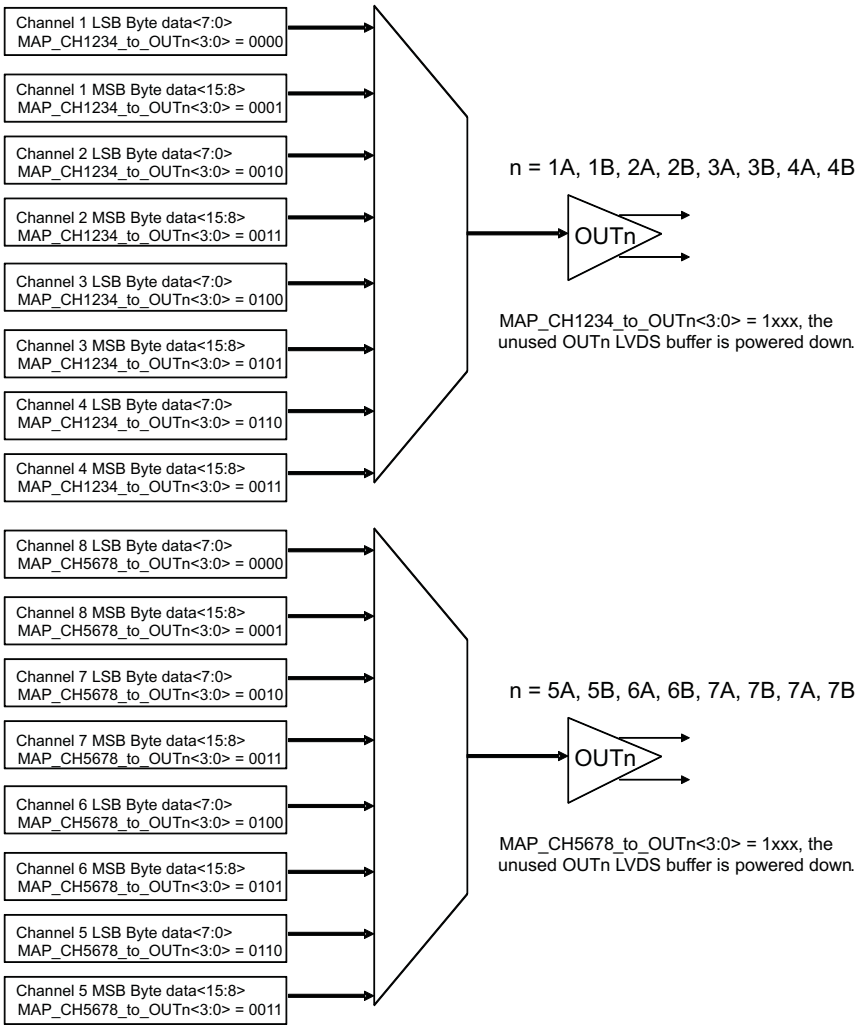


(a) 1-wire mode



(b) 2-wire mode

Figure 61. Input and Output Channel Mapping

Registers 0x50 to 0x55 control the multiplexing options as shown in Table 26 and Table 27.

Table 26. Multiplexing Options

MAP_CH1234_to_OUTn<3:0>	MAPPING	USED IN 1-WIRE MODE?	USED IN 2-WIRE MODE?
0000	ADC input channel IN1 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN1 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN2 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN2 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN3 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN3 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN4 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN4 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

Table 27. Multiplexing Options

MAP_CH5678_to_OUTn<3:0>	MAPPING	USED IN 1-WIRE MODE?	USED IN 2-WIRE MODE?
0000	ADC input channel IN8 to OUTn	Y	Y, for LSB byte
0001	ADC input channel IN8 to OUTn (2-wire only)	N	Y, for MSB byte
0010	ADC input channel IN7 to OUTn	Y	Y, for LSB byte
0011	ADC input channel IN7 to OUTn (2-wire only)	N	Y, for MSB byte
0100	ADC input channel IN6 to OUTn	Y	Y, for LSB byte
0101	ADC input channel IN6 to OUTn (2-wire only)	N	Y, for MSB byte
0110	ADC input channel IN5 to OUTn	Y	Y, for LSB byte
0111	ADC input channel IN5 to OUTn (2-wire only)	N	Y, for MSB byte
1xxx	LVDS output buffer OUTn is powered down		

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The default mapping for 1-wire and 2-wire modes is shown in Table 28 and Table 29.

Table 28. Mapping for 1-Wire Mode(1)

ANALOG INPUT CHANNEL	LVDS OUTPUT
Channel IN1	OUT1A
Channel IN2	OUT2A
Channel IN3	OUT3A
Channel IN4	OUT4A
Channel IN5	OUT5A
Channel IN6	OUT6A
Channel IN7	OUT7A
Channel IN8	OUT8A

(1) 3In the single wire mode with default register settings, ADC data is available only on OUTnA.

Table 29. Mapping for 2-Wire Mode(1)

ANALOG INPUT CHANNEL	LVDS OUTPUT
Channel IN1	OUT1A, OUT1B
Channel IN2	OUT2A, OUT2B
Channel IN3	OUT3A, OUT3B
Channel IN4	OUT4A, OUT4B
Channel IN5	OUT5A, OUT5B
Channel IN6	OUT6A, OUT6B
Channel IN7	OUT7A, OUT7B
Channel IN8	OUT8A, OUT8B

(1) In the 2-wire mode, the ADC data is available on both OUTnA and OUTnB.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The design procedures are discussed in the following sections. *Device Comparison Table* shows related devices suitable for high-speed, multi-channel data acquisition. Figure 62 lists a typical application circuit diagram.

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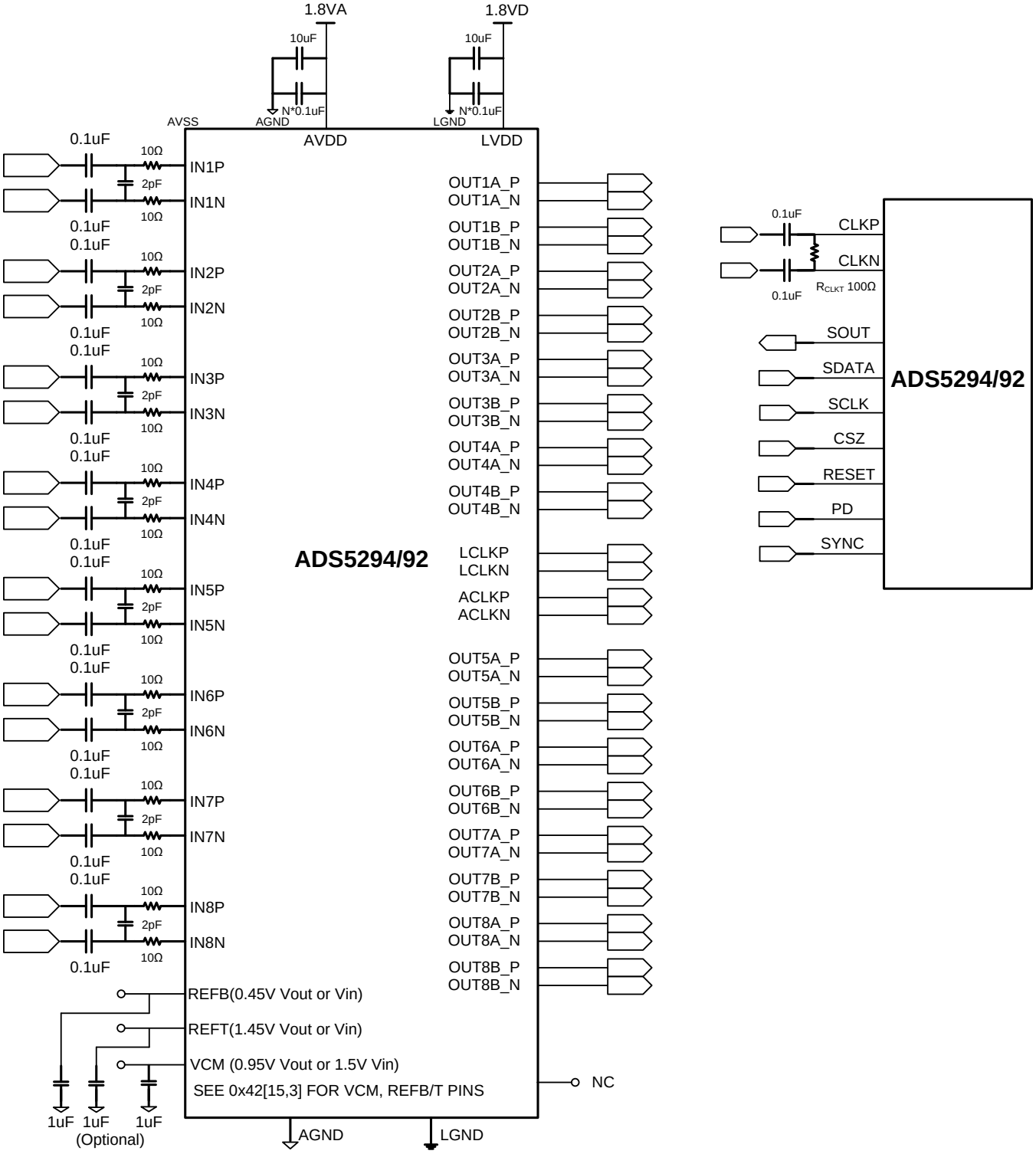
10.2 Typical Application



(1) REFB, REFT pins can be left floating in the internal reference mode, i.e. EN_EXT_REF=0.

Figure 62. Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

The ADS5294 is a high-speed, multi-channel ADC suitable for medical imaging, communication systems, multi-channel data acquisition, and so on. In all applications, the signal dynamic range, center frequency, and bandwidth are the key requirements for the ADC selection.

The ADS5294 has a noise level of approximately 20 nV/√Hz referred to its input, assuming of a sampling rate of 80 MHz, a 2-Vpp input, and 75.5-dBFS SNR. Suitable ADS5294 driver circuit shall be designed to achieve better than 20 nV/√Hz output referred noise.

10.2.2 Detailed Design Procedure

Use the following steps to design a typical data acquistion system:

1. Use the signal center frequency and signal bandwidth to select an appropriate ADC sampling frequency.
2. Use the transducer or sensor noise level and maximum input signal amplitude to select appropriate pre-driver amplifiers.
3. Select appropriate low jitter clock for the ADC.
4. Determine whether to use the on-chip digital filters or decimation filters based on required SNR and pass band shaping.

10.2.2.1 Large and Small Signal Input Bandwidth

The small signal bandwidth of the analog input circuit is high, around 550 MHz. When using an amplifier to drive the ADS5294, consider the total noise of the amplifier up to the small signal bandwidth. The large signal bandwidth of the device depends on the amplitude of the input signal. The ADS5294 supports 2 V_{PP} amplitude for input signal frequency up to 80 MHz. For higher frequencies (80 MHz), the amplitude of the input signal must be decreased proportionally. For example, at 160 MHz, the device supports a maximum of 1 V_{PP} signal.

10.2.2.2 Drive Circuit

For optimum performance, the analog inputs must be driven differentially which improves the common-mode noise immunity and even order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp-out ringing caused by package parasitic.

The drive circuit shows an R-C filter across the analog input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors.

The output of the driver circuit referred noise shall be considered in order to maximize SNR of the ADS5294.

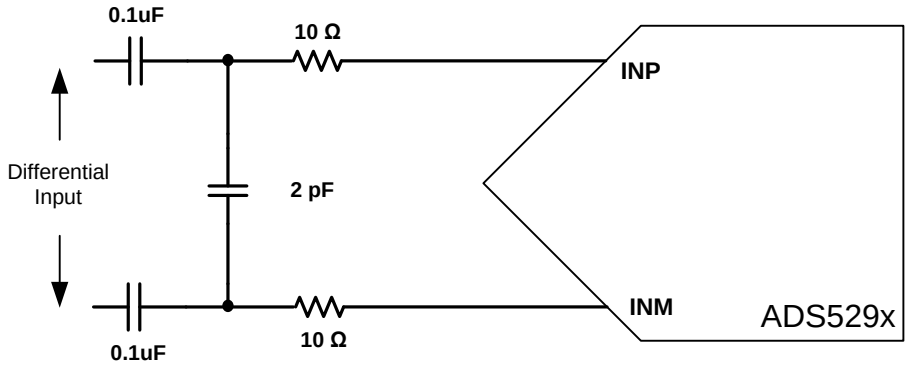


Figure 63. Analog Input Drive Circuit

10.2.2.3 Clock Selection

To ensure that the aperture delay and jitter are the same for all channels, the ADS5294 uses a clock tree network to generate individual sampling clocks for each channel. The clock, for all the channels, are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the aperture delay parameter of the output interface timing. Its variation is given by the aperture jitter number of the same table.

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Typical Application (continued)

The ADS5294 clock input can be driven by either a differential clocks (sine wave, LVPECL, or LVDS) or a singled clock(LVCMOS). In the single-ended case, TI recommends that the use of low jitter square signals (LVCMOS levels, 1.8-V amplitude). See TI document SLYT075 for further details on the theory.

The jitter cleaner CDCM7005 SCAS793, CDCE72010 SLAS490, LMK04803 SNAS489 is suitable to generate the ADC clock of the ADS5294 and ensure the performance for the14-bit ADC with >75-dBFS SNR. Please note that the location of LVDS Rterm depends on the LVDS clock driver. Some clock devices require the Rterm at the left side of AC coupling capacitors.

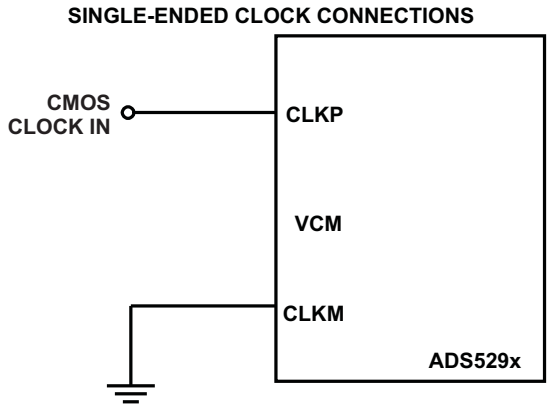


Figure 64. Single-Ended Clock Drive Circuit

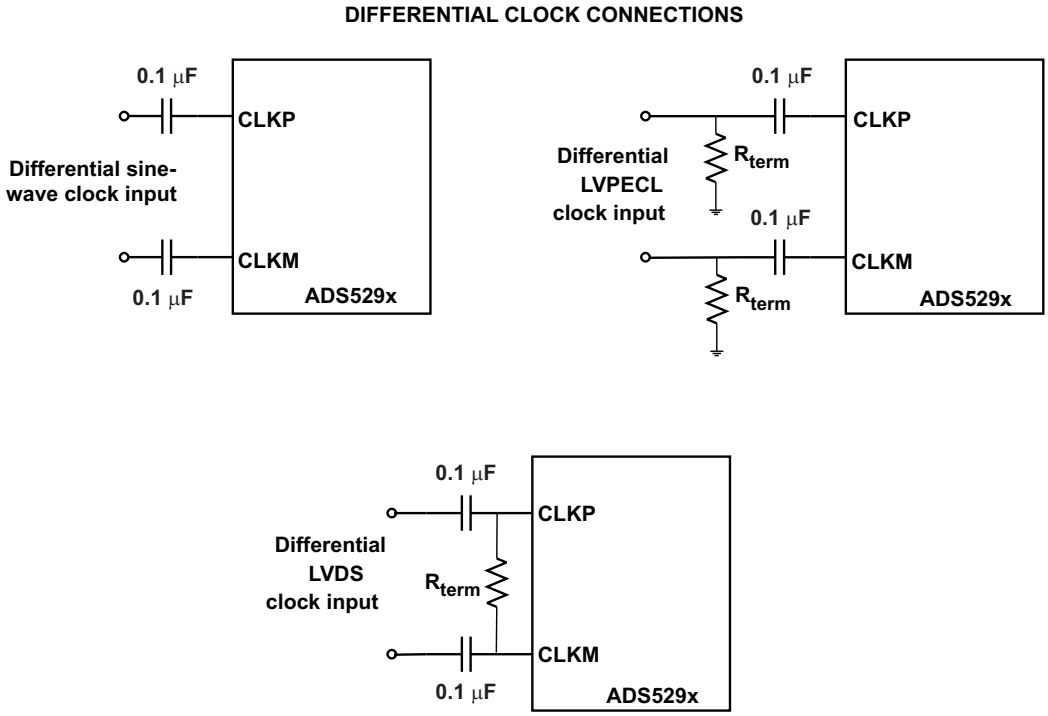
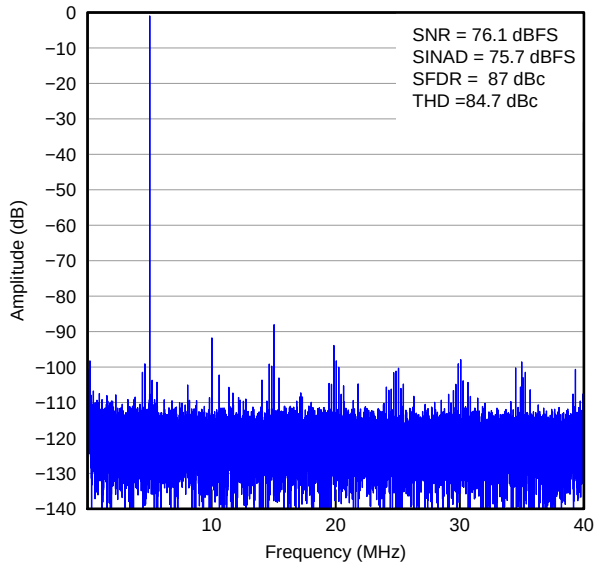


Figure 65. Differential Clock Drive Circuit

Typical Application (continued)

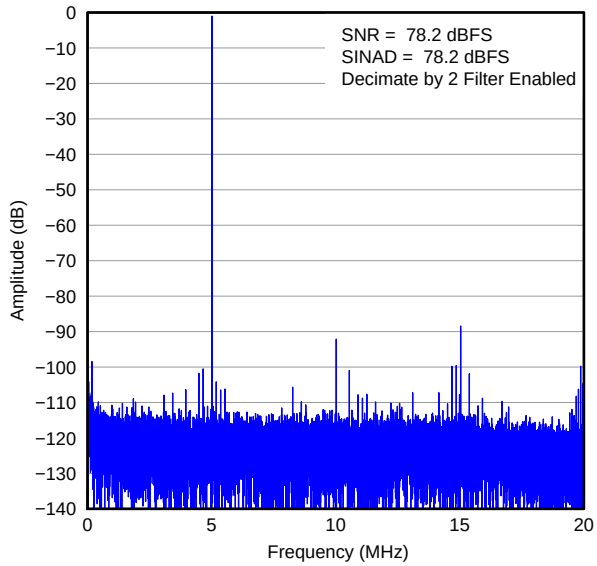
10.2.3 Application Curves

The ADS5294 is a low-power 80-MSPS 8-Channel ADC. The digital processing block of the ADS5294 integrates several commonly used digital features for improving system performance. The device includes a digital filter module that has built-in decimation filters (with lowpass, highpass and bandpass characteristics). The decimation rate is programmable (by 2, by 4, or by 8). This rate is useful for narrow-band applications, where the filters are used to conveniently improve SNR and knock-off harmonics, while at the same time reducing the output data rate. The device also includes an averaging mode where two channels (or even four channels) are averaged to improve SNR. The below application curves show that about 2 dB SNR improvment can be achieved by either enabling 2X decimation or 2-CH averaging features.



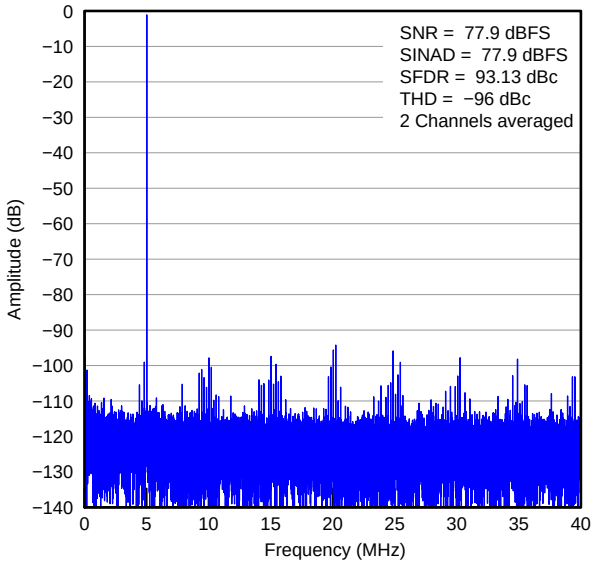
Fs = 80 MSPS

Figure 66. SNR without Decimation Enabled



Fs = 80 MSPS

Figure 67. SNR With Decimation Enabled



Fs = 80 MSPS

Figure 68. SNR With 2-CH Average Enabled

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11 Power Supply Recommendations

The device requires three supplies in order to operate properly. These supplies are AVDD and LVDD. All supplies must be driven with low-noise sources to be able to achieve the best performance from the device. When determining the drive current needed to drive each of the supplies of the device, a margin of 50-100% over the typical current might be needed to account for the current consumption across different modes of operation. Please also refer to *Reset Timing* after power up.

12 Layout

12.1 Layout Guidelines

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS5294VM Evaluation Module* (SLAU355) for placement of components, routing, and grounding.

Because the ADS5294 already includes internal decoupling, minimal external decoupling can be used without loss in performance. For example, the ADS5294EVM uses a single 0.1-µF decoupling capacitor for each supply, placed close to the device supply pins.

The exposed pad at the bottom of the package is the main path for heat dissipation. Solder the pad to a ground plane on the PCB for best thermal performance. The pad must be connected to the ground plane through the optimum number of vias.

See TI's thermal Web site at www.ti.com/thermal for additional information.

12.2 Layout Example

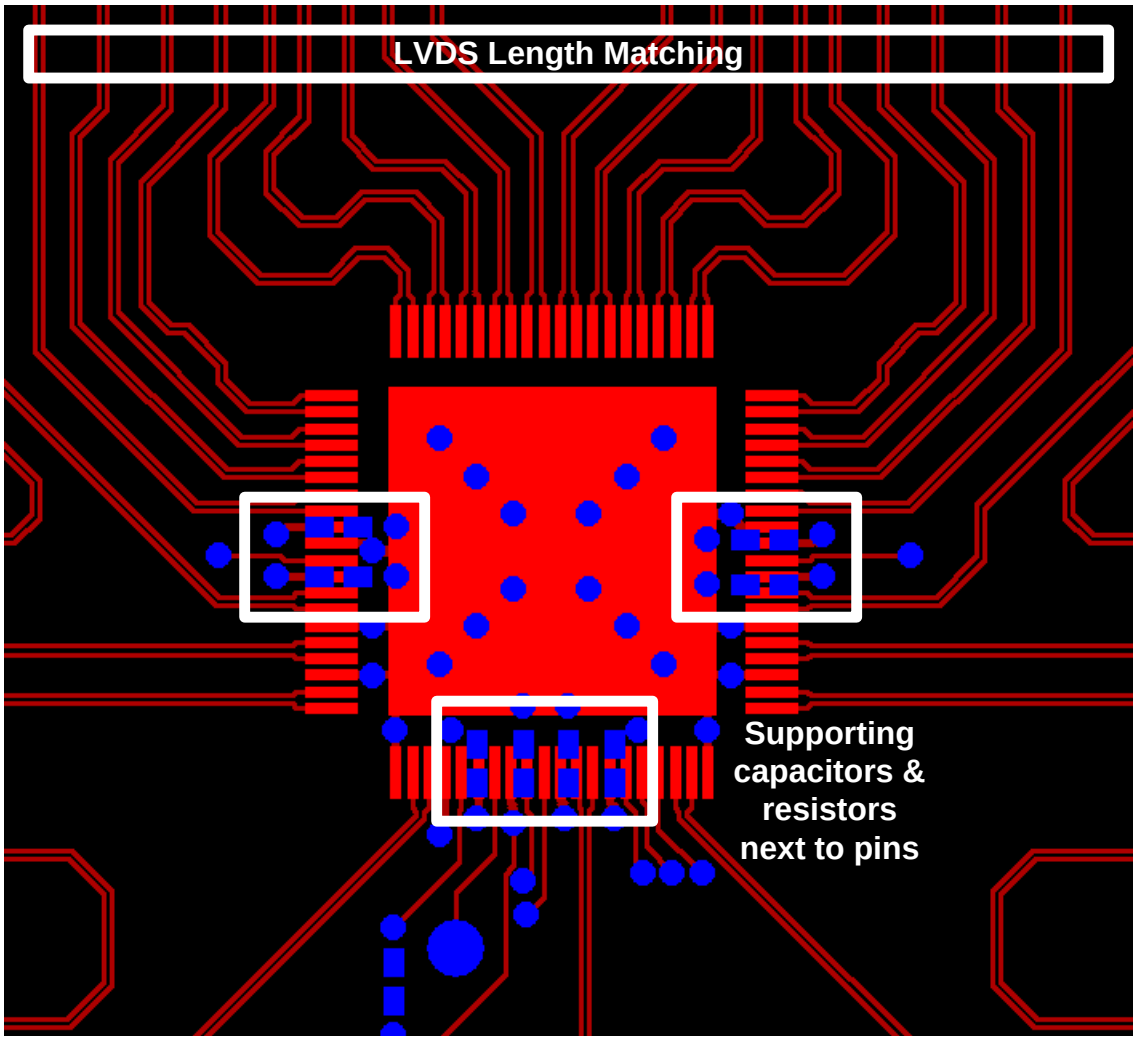

Figure 69. Layout Recommendations

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Nomenclature

13.1.1.1 Definition Of Specifications

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Width and Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions.

Differential Non-Linearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.
To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.
For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5 / 100) \times FS_{ideal}$ to $(1 + 0.5 / 100) \times FS_{ideal}$.

Offset Error The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. Temperature drift is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} - T_{MIN}$.

Signal-to-Noise Ratio SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \tag{7}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding DC.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \tag{8}$$

Device Support (continued)

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{9}$$

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10} \frac{P_S}{P_N} \tag{10}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \tag{11}$$

Voltage Overload Recovery The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. Voltage overload recovery is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \tag{12}$$

Crosstalk (only for multi-channel ADCs) Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc.

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- *Clocking High-Speed Data Converters*, SLYT075
- *CDCM7005 3.3-V High Performance Clock Synchronizer and Jitter Cleaner*, SCAS793
- *CDCE72010 16-Bit, 2-MSPS, LVDS Serial Interface, SAR ADC*, SLAS490
- *LMK04800 Family Low-Noise Clock Jitter Cleaner with Dual Loop PLLs*, SNAS489
- *ADS5294VM Evaluation Module*, SLAU355

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5294IPFP	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5294
ADS5294IPFP.A	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5294
ADS5294IPFPG4.A	Active	Production	HTQFP (PFP) | 80	96 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5294
ADS5294IPFPR	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5294
ADS5294IPFPR.A	Active	Production	HTQFP (PFP) | 80	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5294
ADS5294IPFPT	Active	Production	HTQFP (PFP) | 80	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5294
ADS5294IPFPT.A	Active	Production	HTQFP (PFP) | 80	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS5294

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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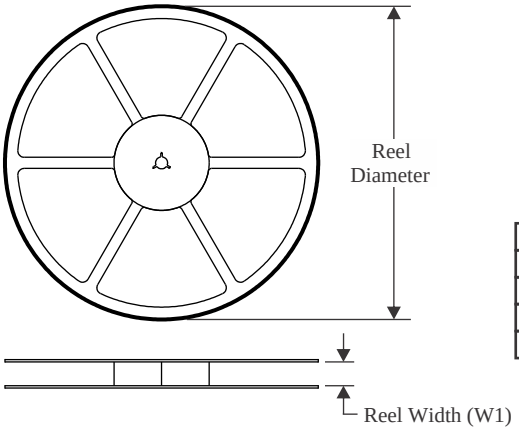
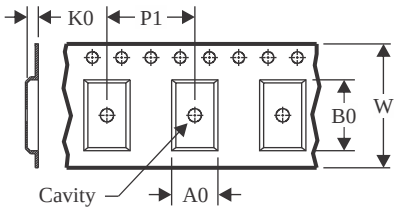
TAPE AND REEL INFORMATION

REEL DIMENSIONS

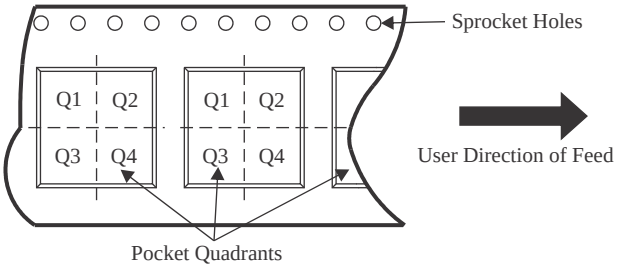


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

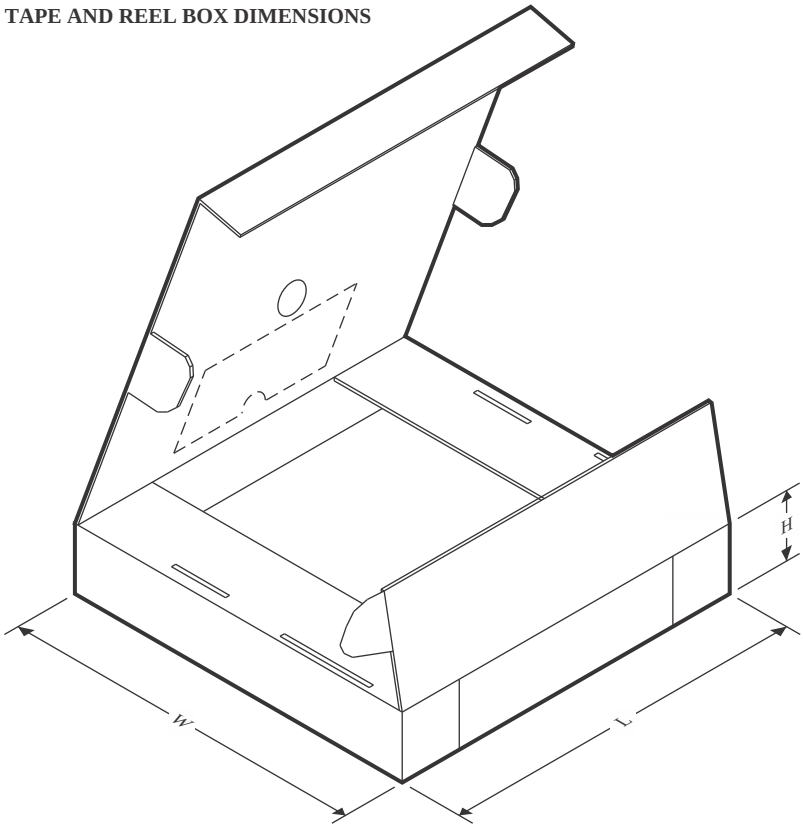
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS5294IPFPR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
ADS5294IPFPT	HTQFP	PFP	80	250	180.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

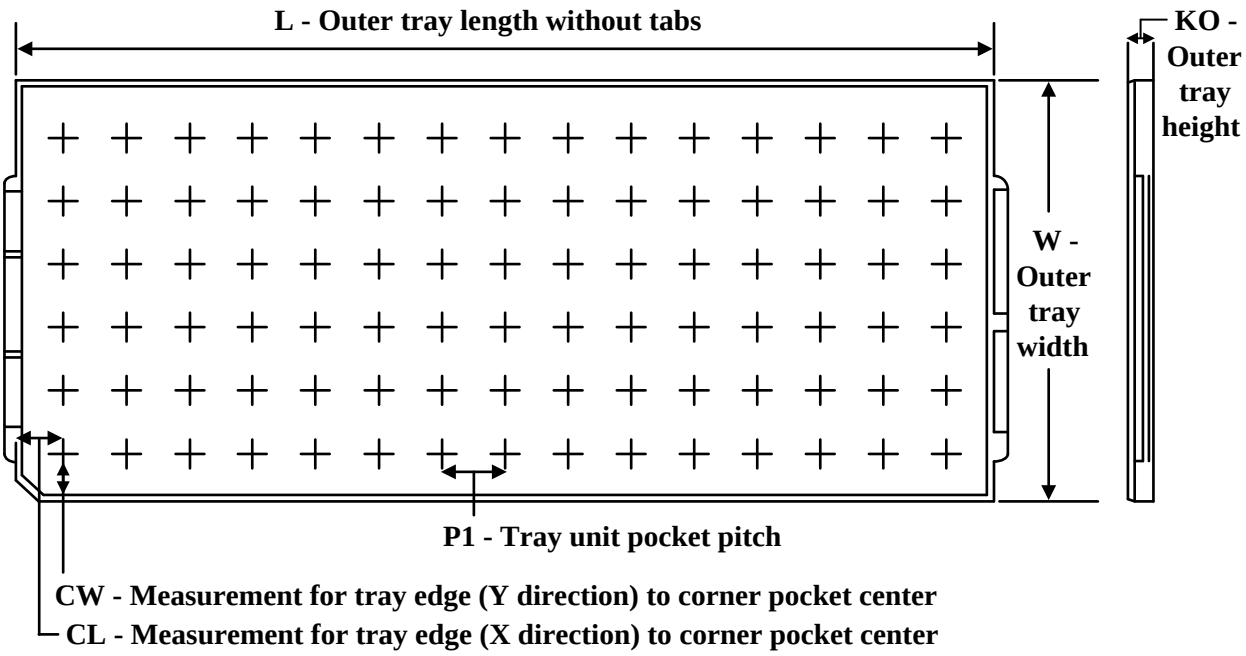
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS5294IPFPR	HTQFP	PFP	80	1000	350.0	350.0	43.0
ADS5294IPFPT	HTQFP	PFP	80	250	213.0	191.0	55.0

TRAY

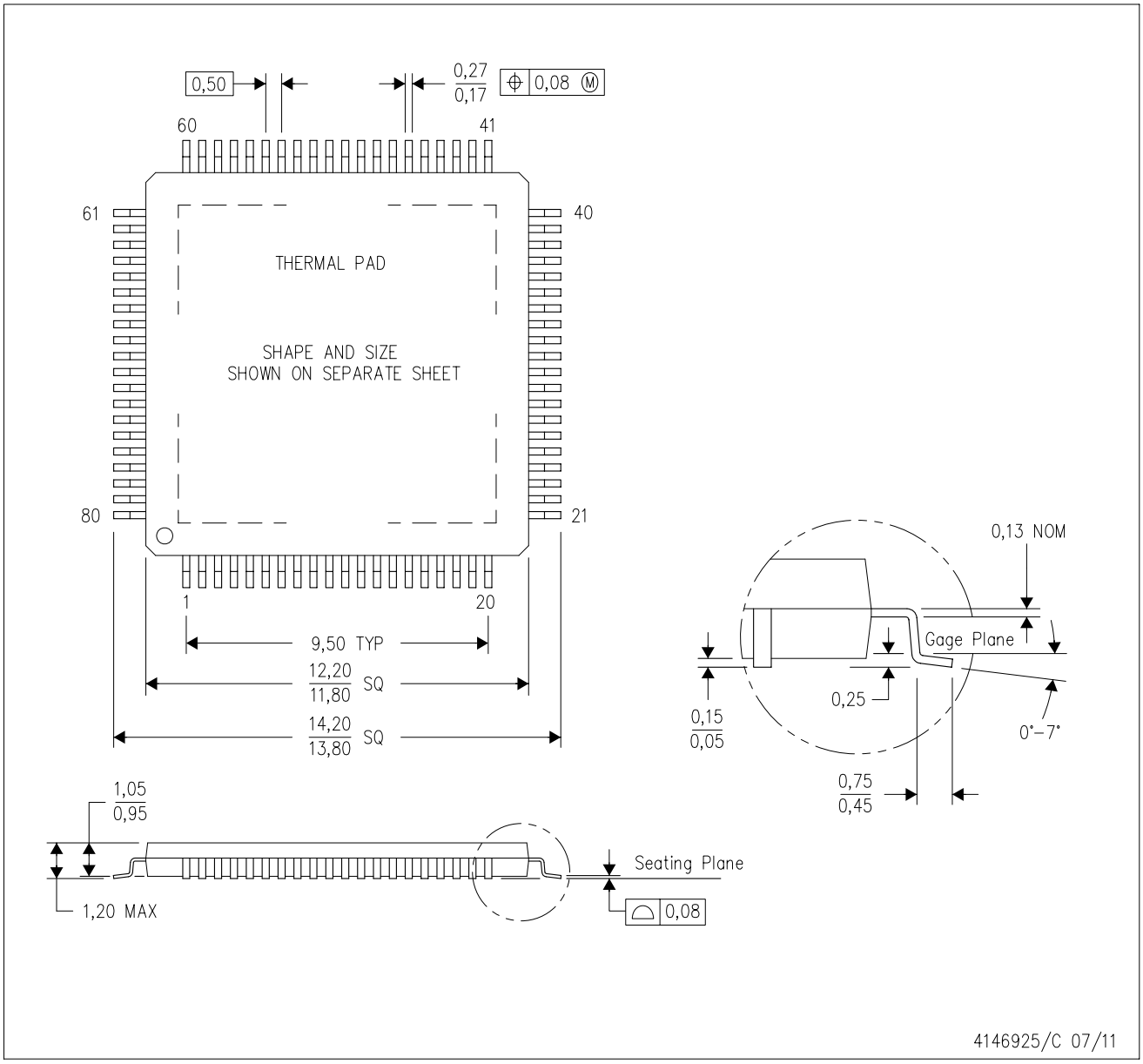


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5294IPFP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
ADS5294IPFP.A	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
ADS5294IPFPG4.A	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS-026

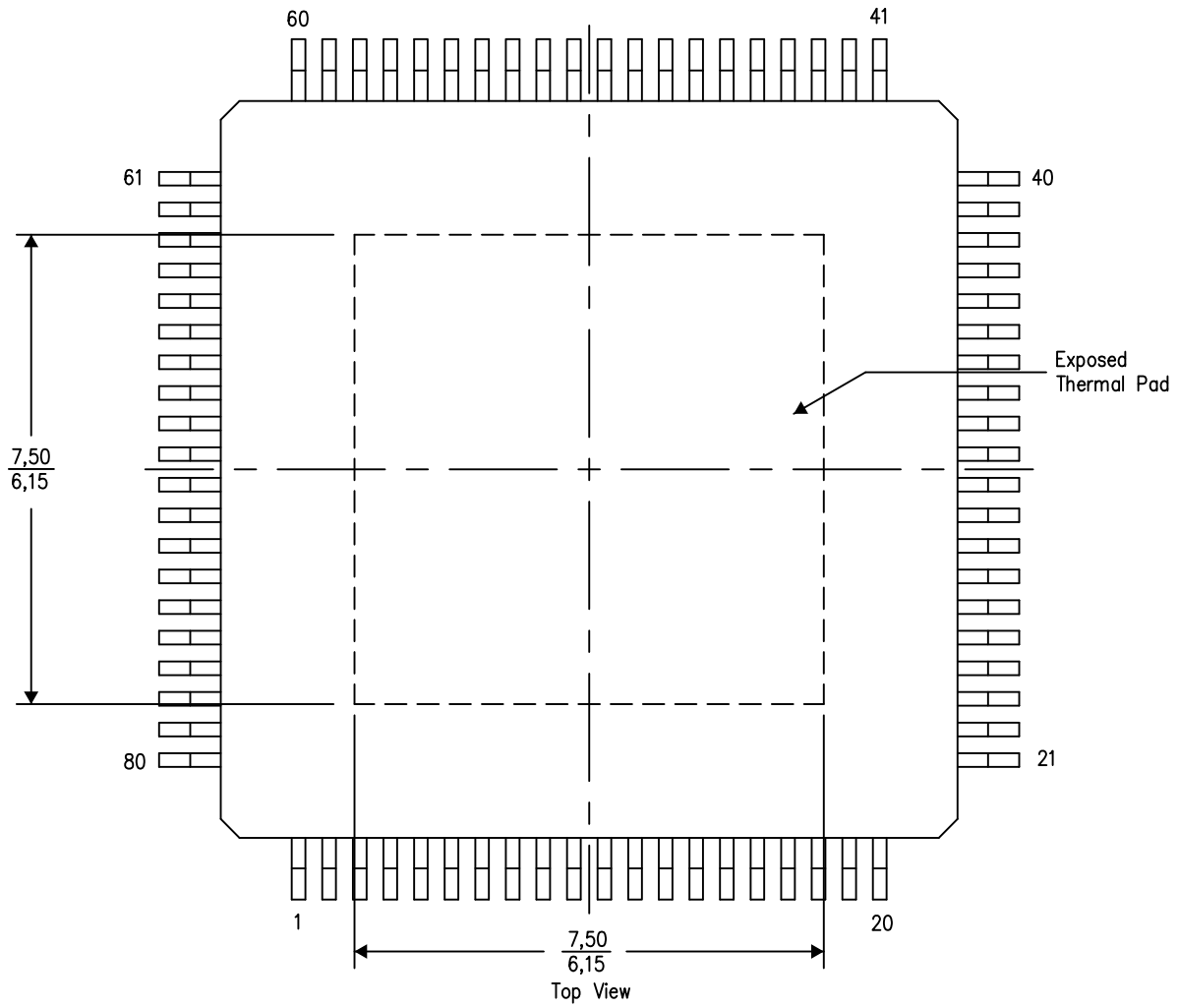
PowerPAD is a trademark of Texas Instruments.

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).
For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



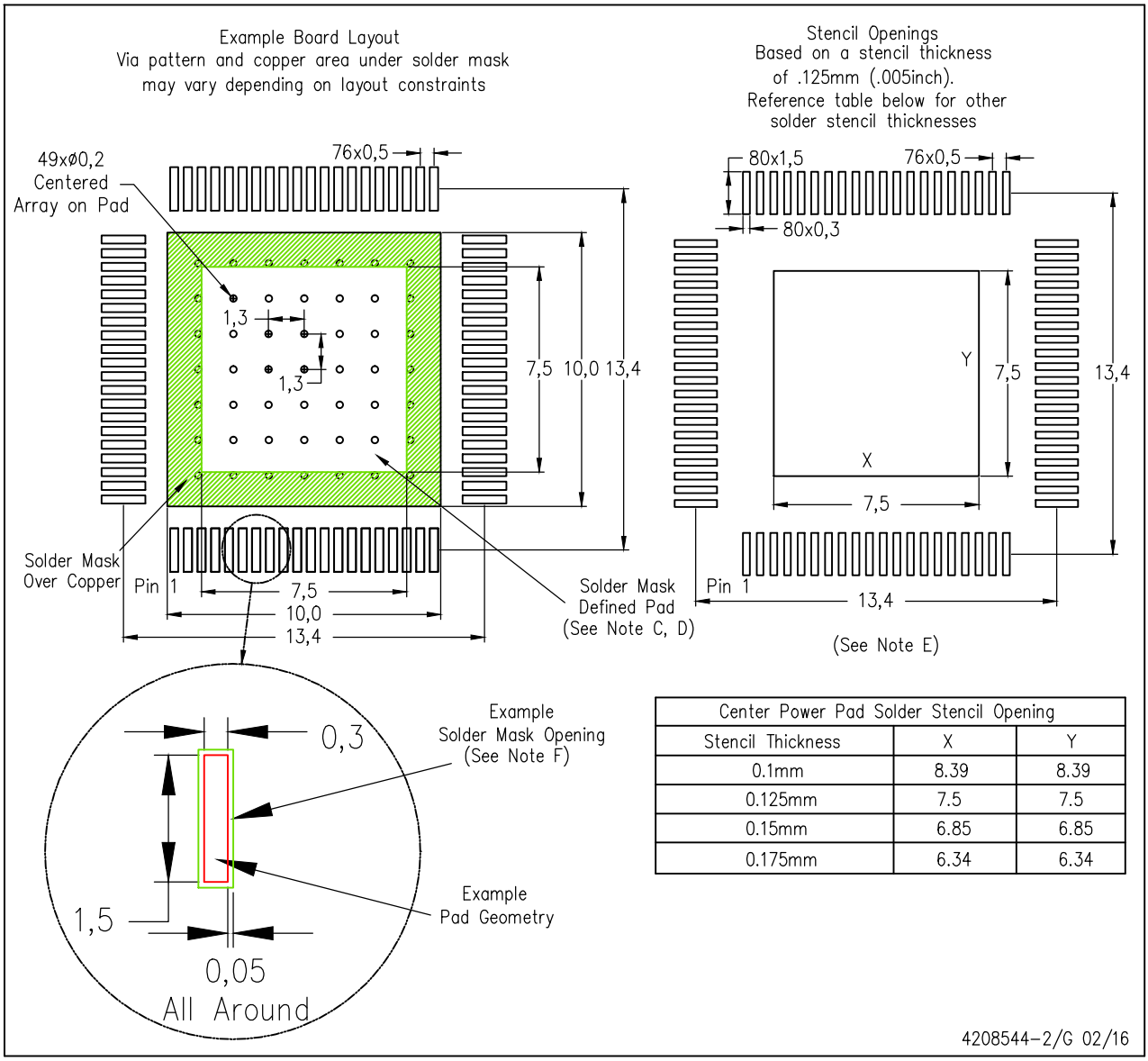
Exposed Thermal Pad Dimensions

4206327-2/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.39	8.39
0.125mm	7.5	7.5
0.15mm	6.85	6.85
0.175mm	6.34	6.34

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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