# SNx4HC132 Quadruple 2-Input NAND Gates with Schmitt-Trigger Inputs

## 1 Features

- Buffered inputs
- Wide operating temperature range: –40°C to +85°C
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

## 2 Applications

- Alarm / tamper detect circuit
- S-R latch

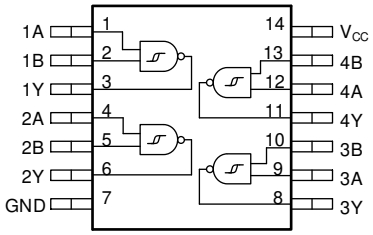
## 3 Description

This device contains four independent 2-input NAND gates. Each gate performs the Boolean function $Y = \overline{A \bullet B}$ in positive logic.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| SN74HC132D | SOIC (14) | 8.65 mm × 3.90 mm |
| SN74HC132DB | SSOP (14) | 6.20 mm × 5.30 mm |
| SN74HC132N | PDIP (14) | 19.30 mm × 6.40 mm |
| SN74HC132NS | SO (14) | 10.20 mm × 5.30 mm |
| SN74HC132PW | TSSOP (14) | 5.00 mm × 4.40 mm |
| SN54HC132J | CDIP (14) | 19.94 mm × 7.62 mm |
| SN54HC132W | CDIP (14) | 9.20 mm × 6.29 mm |
| SN54HC132FK | LCCC (20) | 8.89 mm × 8.89 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Device functional pinout**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (January 2016) to Revision H (January 2021) | Page |
|---|---|
| • Updated data sheet to new template | 1 |
| • Thermal values changed for all packages | 4 |

| Changes from Revision F (November 2004) to Revision G (January 2016) | Page |
|---|---|
| • Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section | 1 |
| • Removed Ordering Information table, see POA at the end of the data sheet | 1 |


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## 5 Pin Configuration and Functions

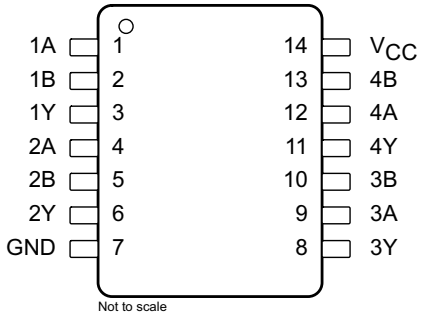


**Figure 5-1. D, DB, N, NS, J, W, or PW Package 14-Pin SOIC, SSOP, PDIP, SO, or TSSOP Top View**

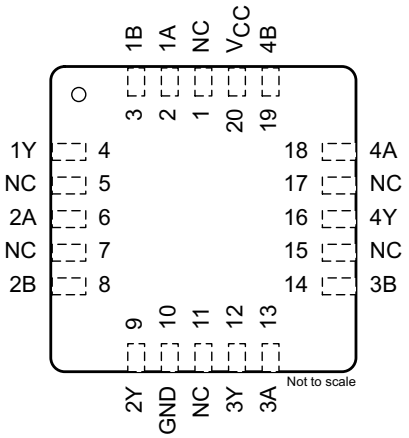


**Figure 5-2. FK Package 20-Pin LCCC Top View**

### Pin Functions [(1)]

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, SSOP, PDIP, SO, TSSOP | LCCC | | |
| 1A | 1 | 2 | I | 1A Input |
| 1B | 2 | 3 | I | 1B Input |
| 1Y | 3 | 4 | O | 1Y Output |
| 2A | 4 | 6 | I | 2A Input |
| 2B | 5 | 8 | I | 2B Input |
| 2Y | 6 | 9 | O | 2Y Output |
| 3A | 9 | 13 | I | 3A Input |
| 3B | 10 | 14 | I | 3B Input |
| 3Y | 8 | 12 | O | 3Y Output |
| 4A | 12 | 18 | I | 4A Input |
| 4B | 13 | 19 | I | 4B Input |
| 4Y | 11 | 16 | O | 4Y Output |
| GND | 7 | 10 | — | Ground Pin |
| NC | — | 1, 5, 7, 11, 15, 17 | — | No Connection |
| $V_{CC}$ | 14 | 20 | — | Power Pin |

(1) NC – no connection

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current[2] | $V_I$ < –0.5 V or $V_I$ > $V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current[2] | $V_O$ < –0.5 V or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature[3] | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $T_A$ | Ambient temperature | SN54HC132 | –55 | | 125 | °C |
| | | SN74HC132 | –40 | | 85 | |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74HC132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 133.6 | 106.8 | 61.5 | 122.6 | 151.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 89 | 56.4 | 49.3 | 81.8 | 79.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 89.5 | 57.0 | 41.3 | 83.8 | 94.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 45.5 | 16.9 | 28.9 | 45.4 | 25.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 89.1 | 56.3 | 41.1 | 83.4 | 94.1 | °C/W |


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| THERMAL METRIC[1] | | SN74HC132 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics - Commercial (74xx)

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | -40°C to 85°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{T+}$ | Positive switching threshold | | | 2 V | 0.7 | 1.2 | 1.5 | 0.7 | | 1.5 | V |
| | | | | 4.5 V | 1.55 | .5 | 3.15 | 1.55 | | 3.15 | |
| | | | | 6 V | 2.1 | 3.3 | 4.2 | 2.1 | | 4.2 | |
| $V_{T-}$ | Negative switching threshold | | | 2 V | 0.3 | 0.6 | 1.0 | 0.3 | | 1.0 | V |
| | | | | 4.5 V | 0.9 | 1.6 | 2.45 | 0.9 | | 2.45 | |
| | | | | 6 V | 1.2 | 2.0 | 3.2 | 1.2 | | 3.2 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$) | | | 2 V | 0.2 | 0.6 | 1.2 | 0.2 | | 1.2 | V |
| | | | | 4.5 V | 0.4 | 0.9 | 2.1 | 0.4 | | 2.1 | |
| | | | | 6 V | 0.5 | 1.3 | 2.5 | 0.5 | | 2.5 | |
| $V_{OH}$ | High-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | | V |
| | | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | | |
| | | | | 6 V | 5.9 | 5.999 | | 5.9 | | | |
| | | | $I_{OH}$ = -4 mA | 4.5 V | 3.98 | 4.3 | | | | 3.84 | |
| | | | $I_{OH}$ = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.34 | | | |
| $V_{OL}$ | Low-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V | | 0.002 | 0.1 | | | 0.1 | V |
| | | | | 4.5 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | | 6 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | | 0.33 | |
| | | | $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | | 0.33 | |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or 0 | | 6 V | | ±0.1 | ±100 | | | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I = V_{CC}$ or 0 | $V_I = V_{CC}$ or 0 | 6 V | | | 2 | | | 20 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | 3 | 10 | | | 10 | pF |
| $C_{pd}$ | Power dissipation capacitance per gate | No load | | 2 V to 6 V | | 20 | | | | | pF |

## 6.6 Electrical Characteristics - Military (54xx)

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | -55°C to 125°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{T+}$ | Positive switching threshold | | | 2 V | 0.7 | 1.2 | 1.5 | 0.7 | | 1.5 | V |
| | | | | 4.5 V | 1.55 | .5 | 3.15 | 1.55 | | 3.15 | |
| | | | | 6 V | 2.1 | 3.3 | 4.2 | 2.1 | | 4.2 | |
| $V_{T-}$ | Negative switching threshold | | | 2 V | 0.3 | 0.6 | 1.0 | 0.3 | | 1.0 | V |
| | | | | 4.5 V | 0.9 | 1.6 | 2.45 | 0.9 | | 2.45 | |
| | | | | 6 V | 1.2 | 2.0 | 3.2 | 1.2 | | 3.2 | |
| $\Delta V_T$ | Hysteresis ($V_{T+}$ - $V_{T-}$) | | | 2 V | 0.2 | 0.6 | 1.2 | 0.2 | | 1.2 | V |
| | | | | 4.5 V | 0.4 | 0.9 | 2.1 | 0.4 | | 2.1 | |
| | | | | 6 V | 0.5 | 1.3 | 2.5 | 0.5 | | 2.5 | |
| $V_{OH}$ | High-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | | V |
| | | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | | |
| | | | | 6 V | 5.9 | 5.999 | | 5.9 | | | |
| | | | $I_{OH}$ = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | | |
| | | | $I_{OH}$ = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | | |
| $V_{OL}$ | High-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V | | 0.002 | 0.1 | | | 0.1 | V |
| | | | | 4.5 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | | 6 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | | 0.4 | |
| | | | $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | | 0.4 | |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or 0 | | 6 V | | ±0.1 | ±100 | | | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I = V_{CC}$ or 0 | $V_I = V_{CC}$ or 0 | 6 V | | | 2 | | | 40 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | 3 | 10 | | | 10 | pF |
| $C_{pd}$ | Power dissipation capacitance per gate | No load | | 2 V to 6 V | | 20 | | | | | pF |

## 6.7 Switching Characteristics - Commercial (74xx)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM | TO | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | –40°C to 85°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | A or B | Y | 2 V | | 60 | | | | 156 | ns |
| | | | | 4.5 V | | 18 | | | | 31 | |
| | | | | 6 V | | 14 | | | | 27 | |
| $t_t$ | Transition-time | | Any | 2 V | | 28 | | | | 95 | ns |
| | | | | 4.5 V | | 8 | | | | 19 | |
| | | | | 6 V | | 6 | | | | 16 | |


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## 6.8 Switching Characteristics - Military (54xx)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM | TO | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | –55°C to 125°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | A or B | Y | 2 V | | 60 | | | | 186 | ns |
| | | | | 4.5 V | | 18 | | | | 37 | |
| | | | | 6 V | | 14 | | | | 32 | |
| $t_t$ | Transition-time | | Any | 2 V | | 28 | | | | 110 | ns |
| | | | | 4.5 V | | 8 | | | | 22 | |
| | | | | 6 V | | 6 | | | | 19 | |

## 6.9 Typical Characteristics

$T_A$ = 25°C

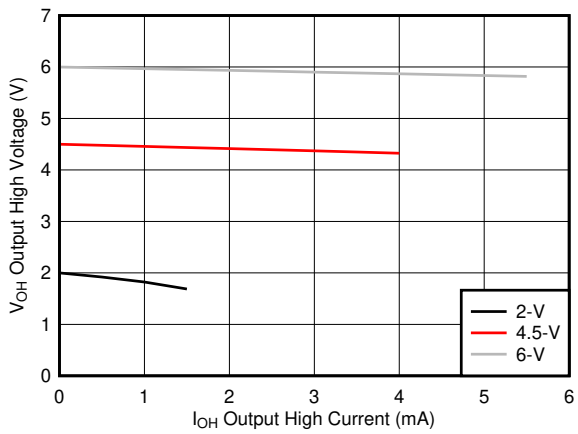



**Figure 6-1. Typical output voltage in the high state ($V_{OH}$)**

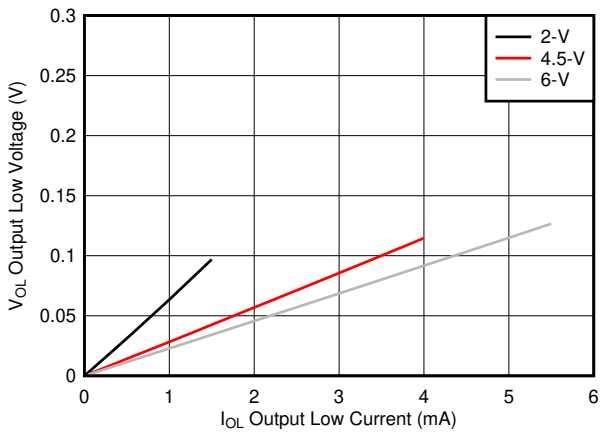


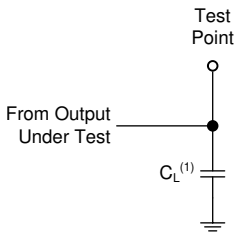

**Figure 6-2. Typical output voltage in the low state ($V_{OL}$)**

## 7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 6 ns.

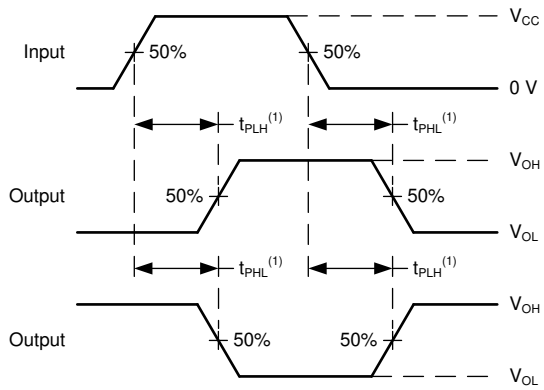
For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



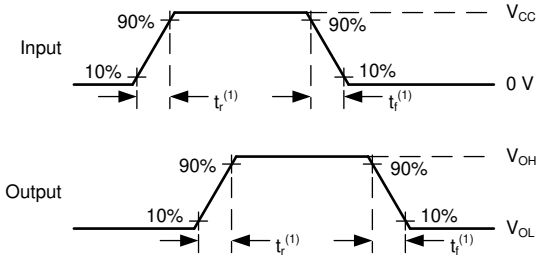

(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 7-1. Load Circuit for Push-Pull Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

**Figure 7-2. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

**Figure 7-3. Voltage Waveforms, Input and Output Transition Times**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# 8 Detailed Description

## 8.1 Overview

This device contains four independent 2-input NAND gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = \overline{A \bullet B}$ in positive logic.

## 8.2 Functional Block Diagram

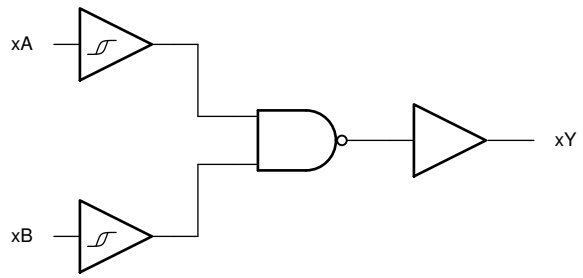


**Figure 8-1. Logic Diagram (Positive Logic) for the SN74HC132**

## 8.3 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

## 8.4 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

## 8.5 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Electrical Placement of Clamping Diodes for Each Input and Output.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

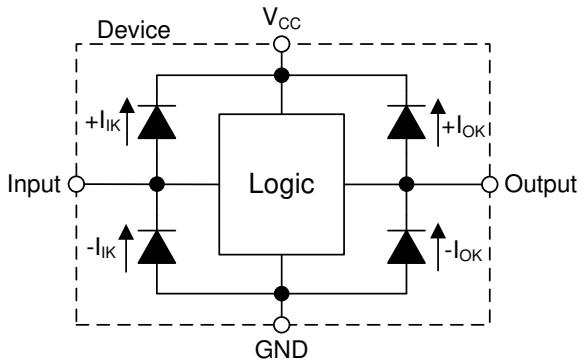


**Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.6 Device Functional Modes

**Table 8-1. Function Table**

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | H | L |
| L | X | H |
| X | L | H |


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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

In this application, the SN74HC132 is used to create an active-low SR latch. The two additional gates can be used for a second active-low SR latch, individually used for their logic function, or the inputs can be grounded and both channels left unused. This device is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

## 9.2 Typical Application

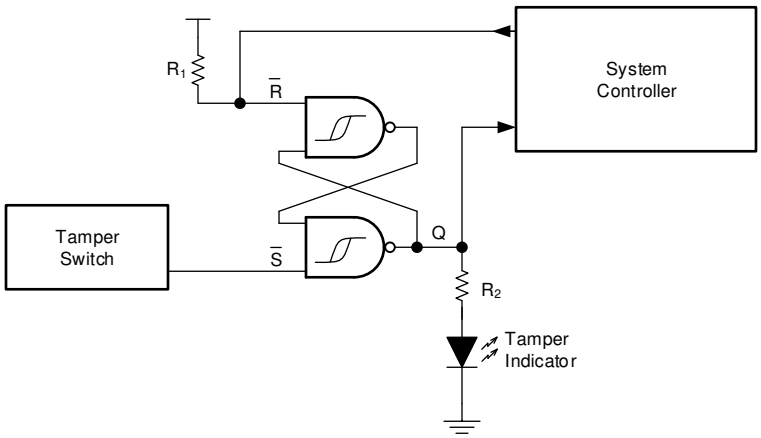


**Figure 9-1. Typical application diagram**

### 9.2.1 Design Requirements

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC132 plus the maximum static supply current, $I_{CC}$, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HC132 plus the maximum supply current, $I_{CC}$, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HC132 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HC132 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the high state, the

output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and Cpd Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### *9.2.1.2 Input Considerations*

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC132, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HC132 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

#### *9.2.1.3 Output Considerations*

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.


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2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC132 to the receiving device(s).
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

### 9.2.3 Application Curve

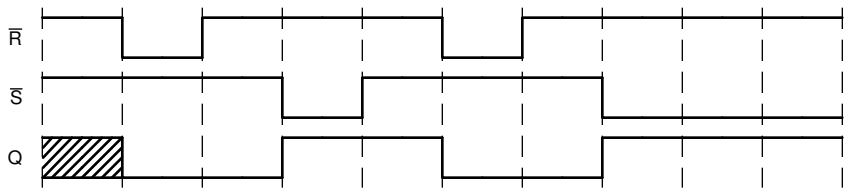


**Figure 9-2. Application timing diagram**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

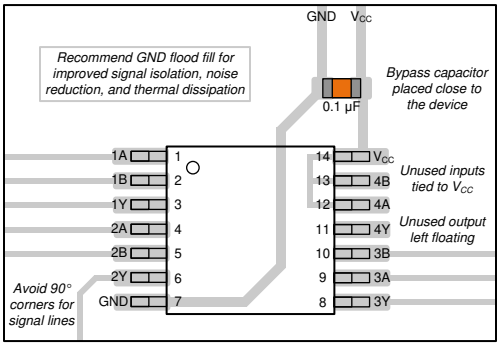


**Figure 11-1. Example layout for the SN74HC132.**


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# 12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 12.1 Documentation Support

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-89845022A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-89845022A SNJ54HC132FK |
| 5962-8984502CA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502CA SNJ54HC132J |
| 5962-8984502DA | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502DA SNJ54HC132W |
| 5962-8984502VCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502VCA SNV54HC132J |
| 5962-8984502VCA.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502VCA SNV54HC132J |
| 5962-8984502VDA | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502VDA SNV54HC132W |
| 5962-8984502VDA.A | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502VDA SNV54HC132W |
| SN54HC132J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC132J |
| SN54HC132J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC132J |
| SN74HC132D | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 85 | HC132 |
| SN74HC132DBR | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132DBR.A | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132DR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132DR1G4 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC132 |
| SN74HC132DR1G4.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC132 |
| SN74HC132DT | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 85 | HC132 |
| SN74HC132N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC132N |
| SN74HC132N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC132N |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74HC132NE4 | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC132N |
| SN74HC132NSR | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132NSR.A | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132NSRG4 | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132PW | Obsolete | Production | TSSOP (PW) \| 14 | - | - | Call TI | Call TI | -40 to 85 | HC132 |
| SN74HC132PWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132PWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC132 |
| SN74HC132PWR1G4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC132 |
| SN74HC132PWR1G4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC132 |
| SN74HC132PWT | Obsolete | Production | TSSOP (PW) \| 14 | - | - | Call TI | Call TI | -40 to 85 | HC132 |
| SN74HCS132DYYR | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS132 |
| SN74HCS132DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HCS132 |
| SNJ54HC132FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-89845022A SNJ54HC 132FK |
| SNJ54HC132FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-89845022A SNJ54HC 132FK |
| SNJ54HC132J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502CA SNJ54HC132J |
| SNJ54HC132J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502CA SNJ54HC132J |
| SNJ54HC132W | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502DA SNJ54HC132W |
| SNJ54HC132W.A | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8984502DA SNJ54HC132W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54HC132, SN54HC132-SP, SN74HC132 :**

- Catalog : SN74HC132, SN54HC132
- Automotive : SN74HC132-Q1, SN74HC132-Q1
- Military : SN54HC132
- Space : SN54HC132-SP

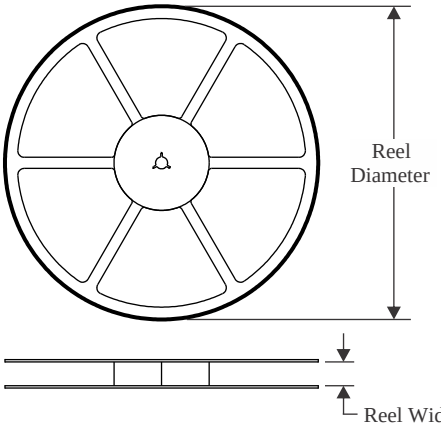
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

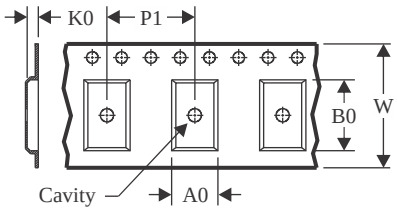
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

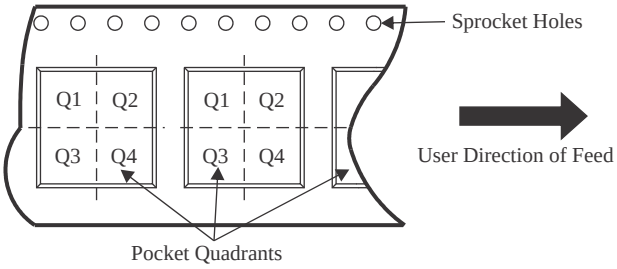



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

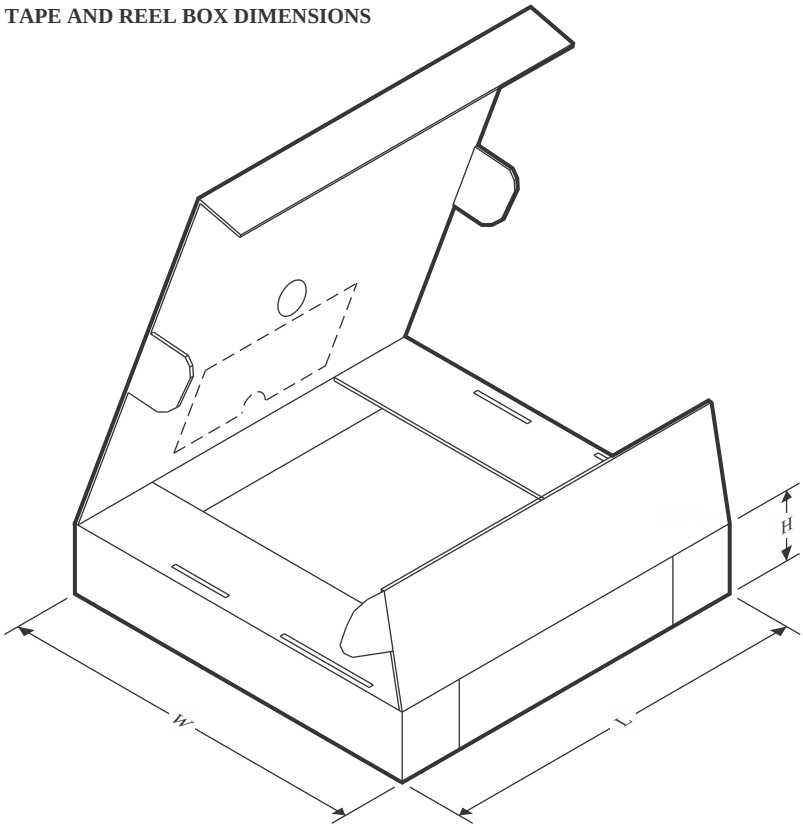
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC132DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74HC132DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC132DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.6 | 9.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC132DR1G4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC132NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |
| SN74HC132PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC132PWR1G4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HCS132DYYR | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |

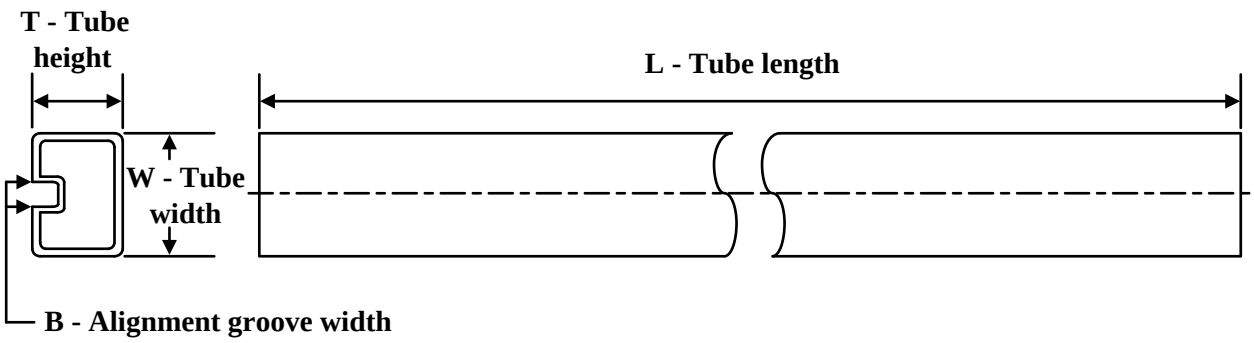
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC132DBR | SSOP | DB | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC132DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC132DR | SOIC | D | 14 | 2500 | 366.0 | 364.0 | 50.0 |
| SN74HC132DR1G4 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74HC132NSR | SOP | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC132PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HC132PWR1G4 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCS132DYYR | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |

## TUBE

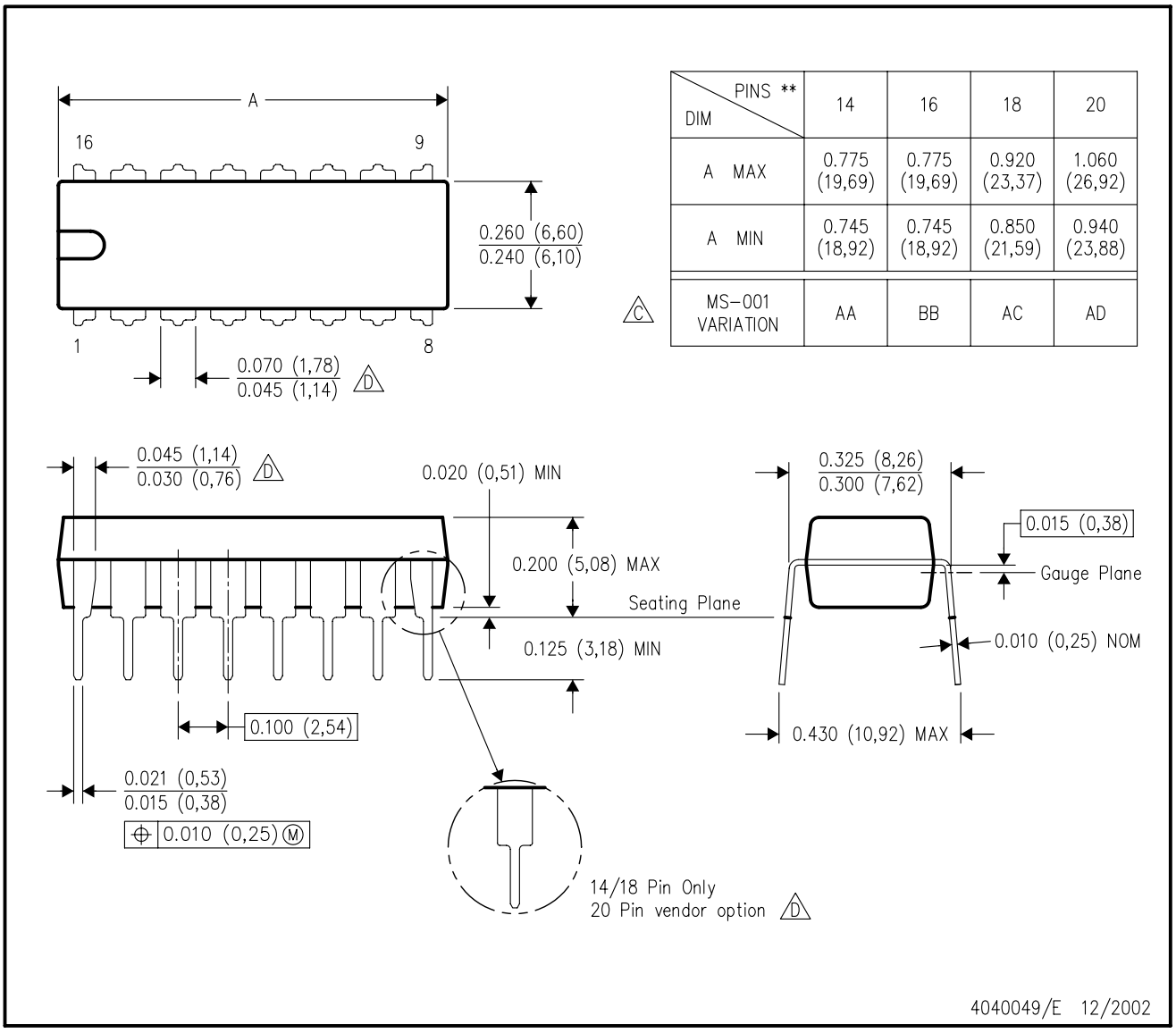



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-89845022A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8984502DA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-8984502VDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-8984502VDA.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HC132N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC132N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC132N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC132N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC132NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC132NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC132FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC132FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC132W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54HC132W.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

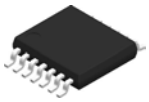
16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

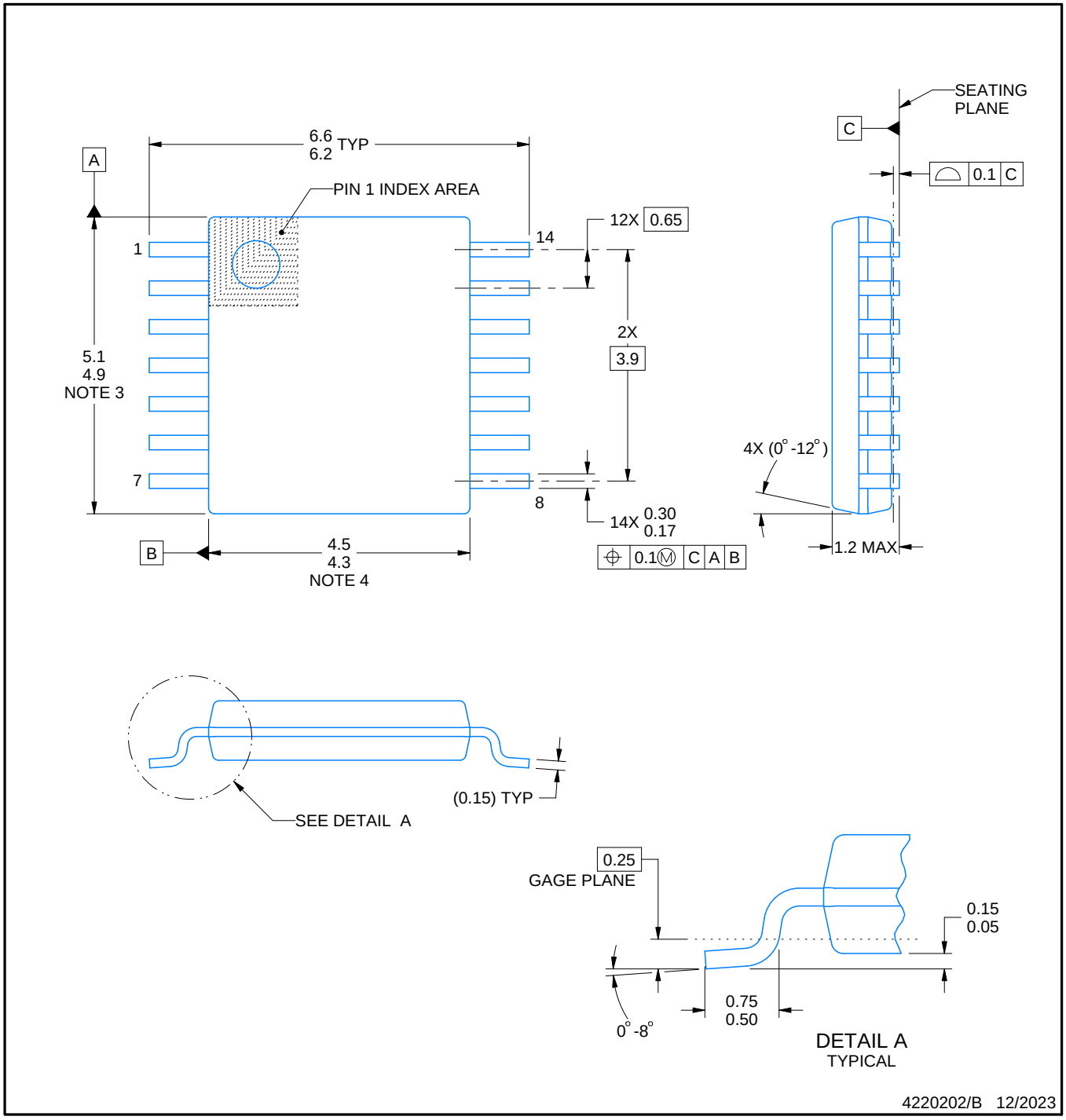
# PW0014A



# PACKAGE OUTLINE

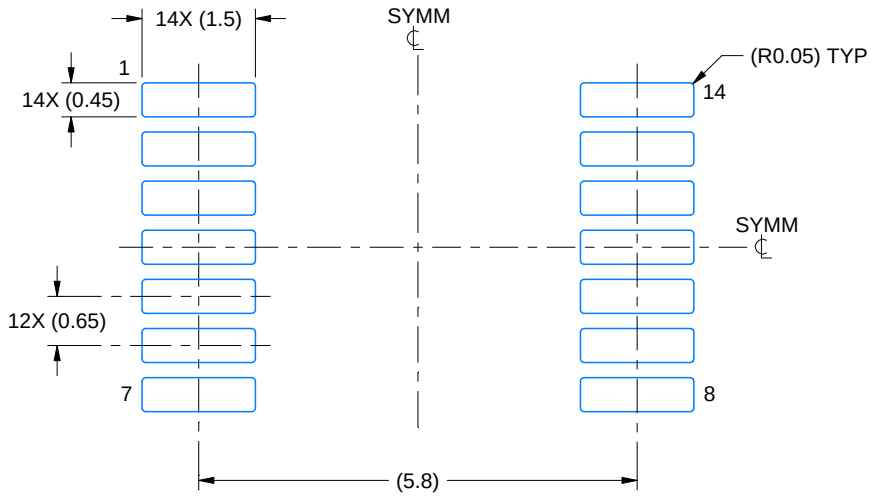
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

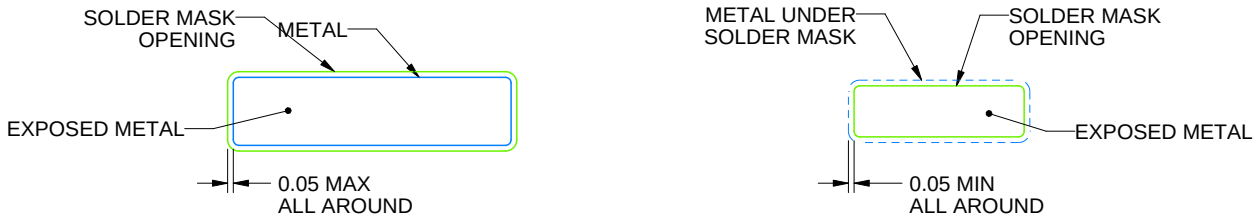



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

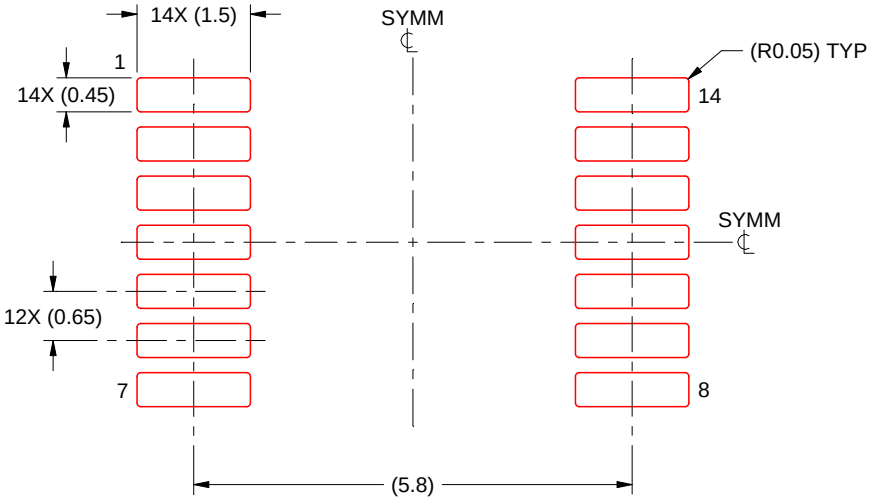
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

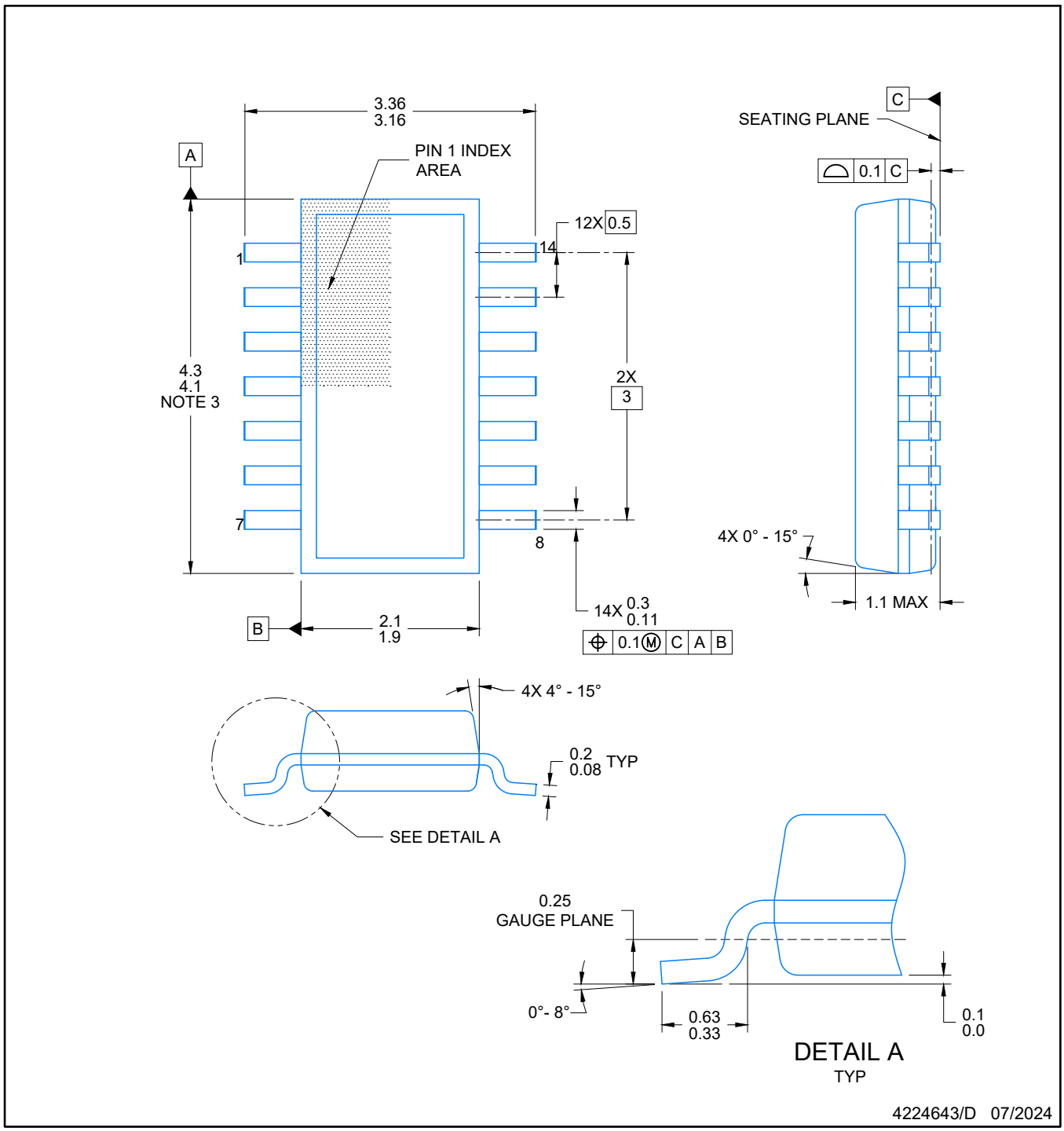



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

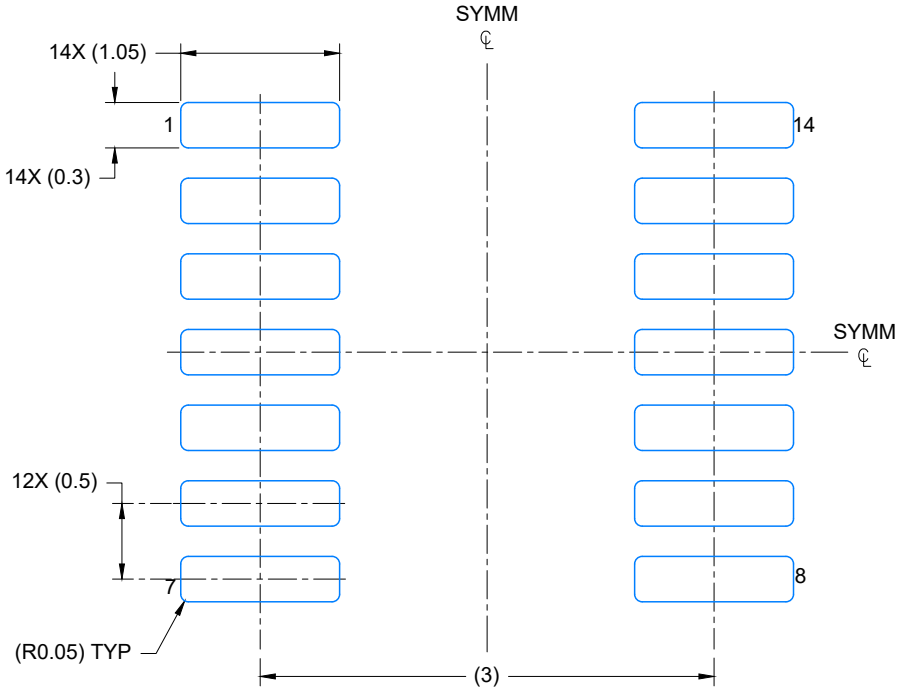
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

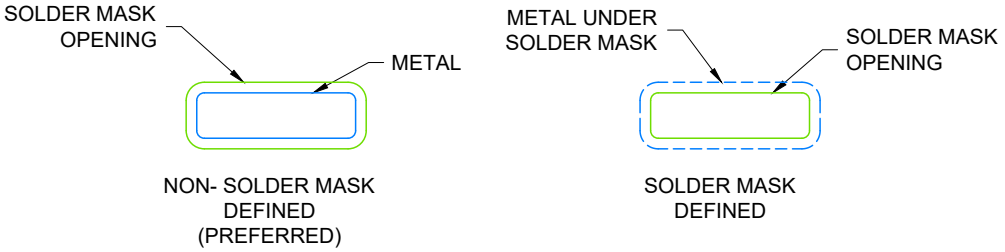



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

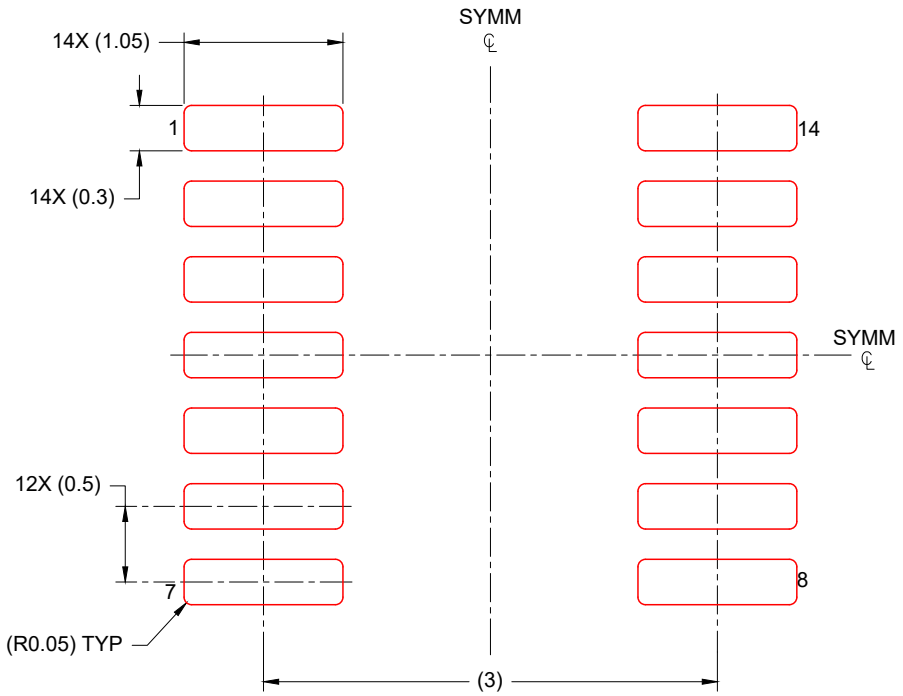



SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

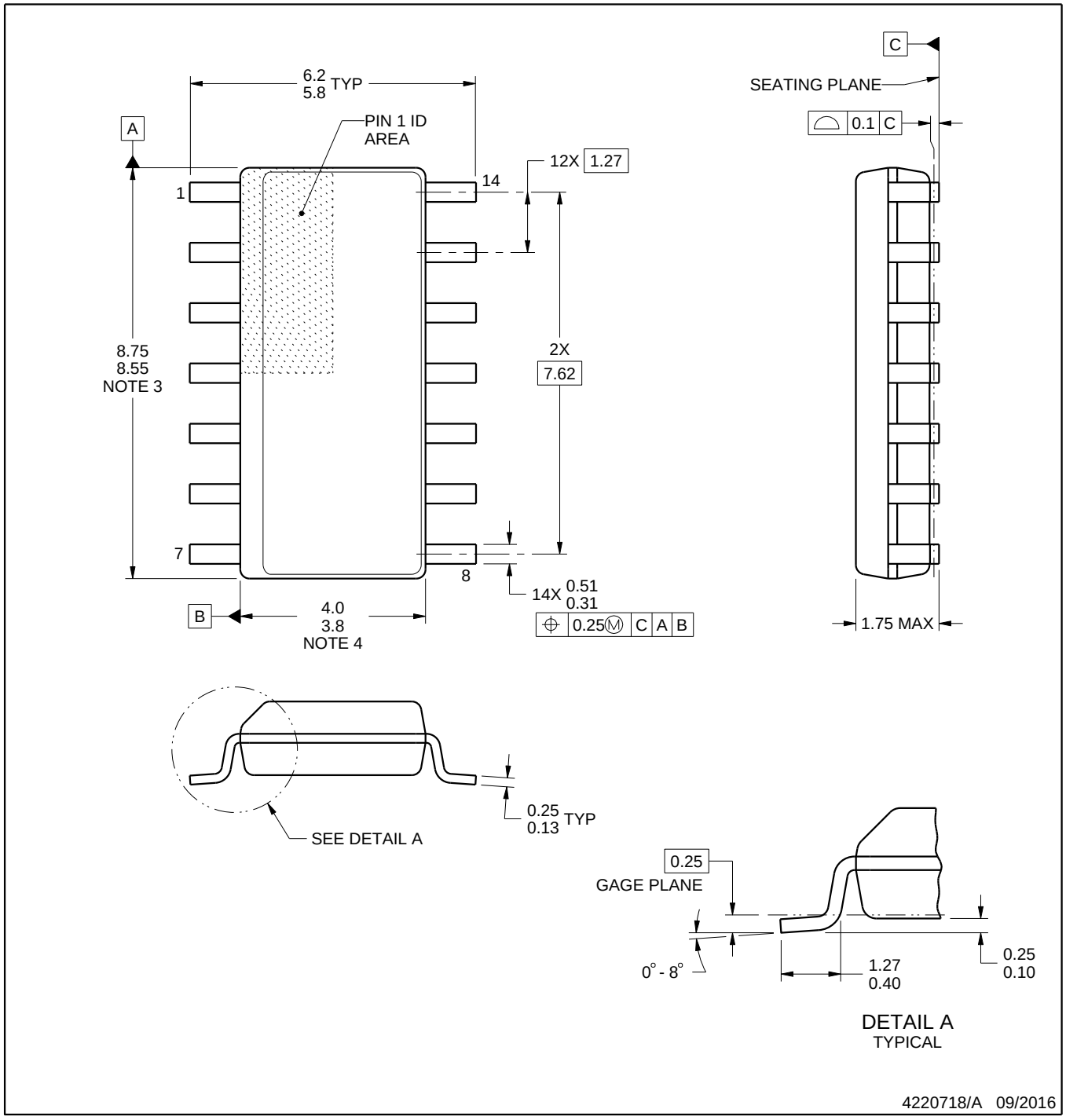



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

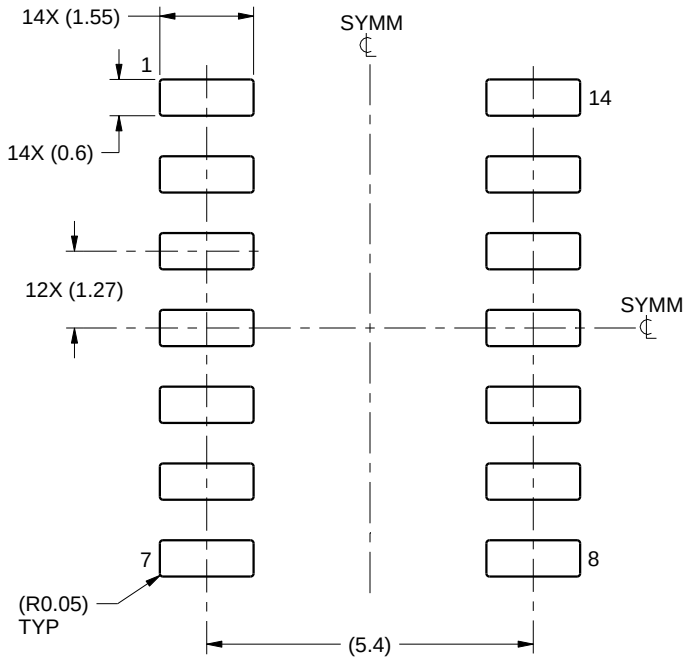
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

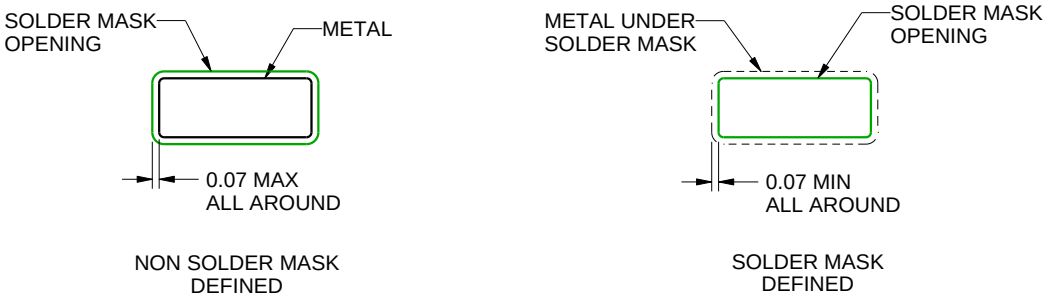



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X

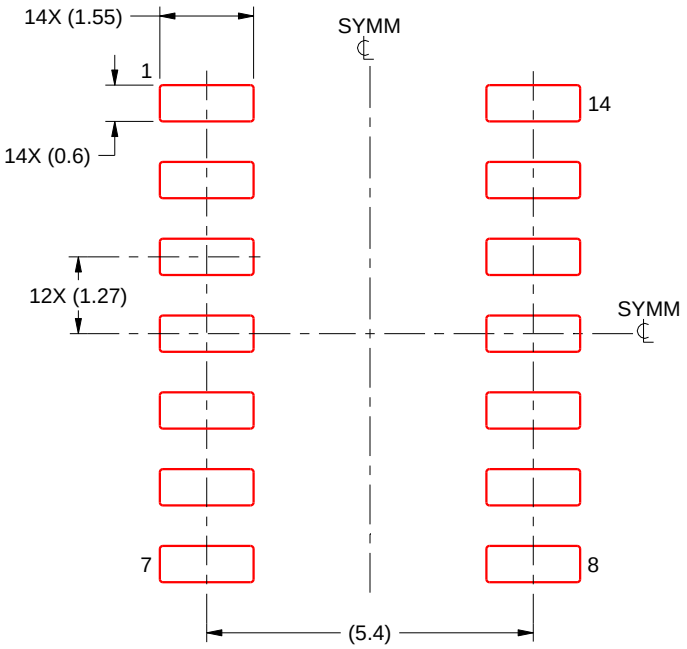



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

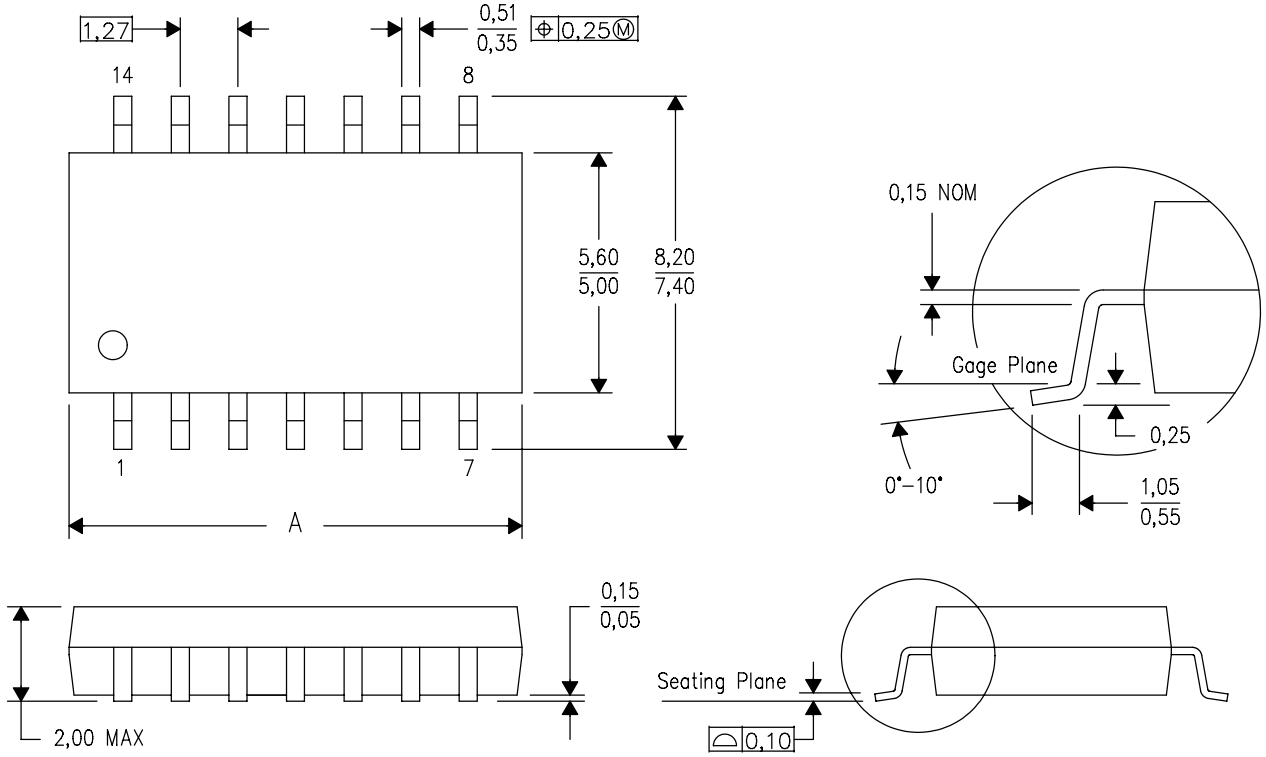
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

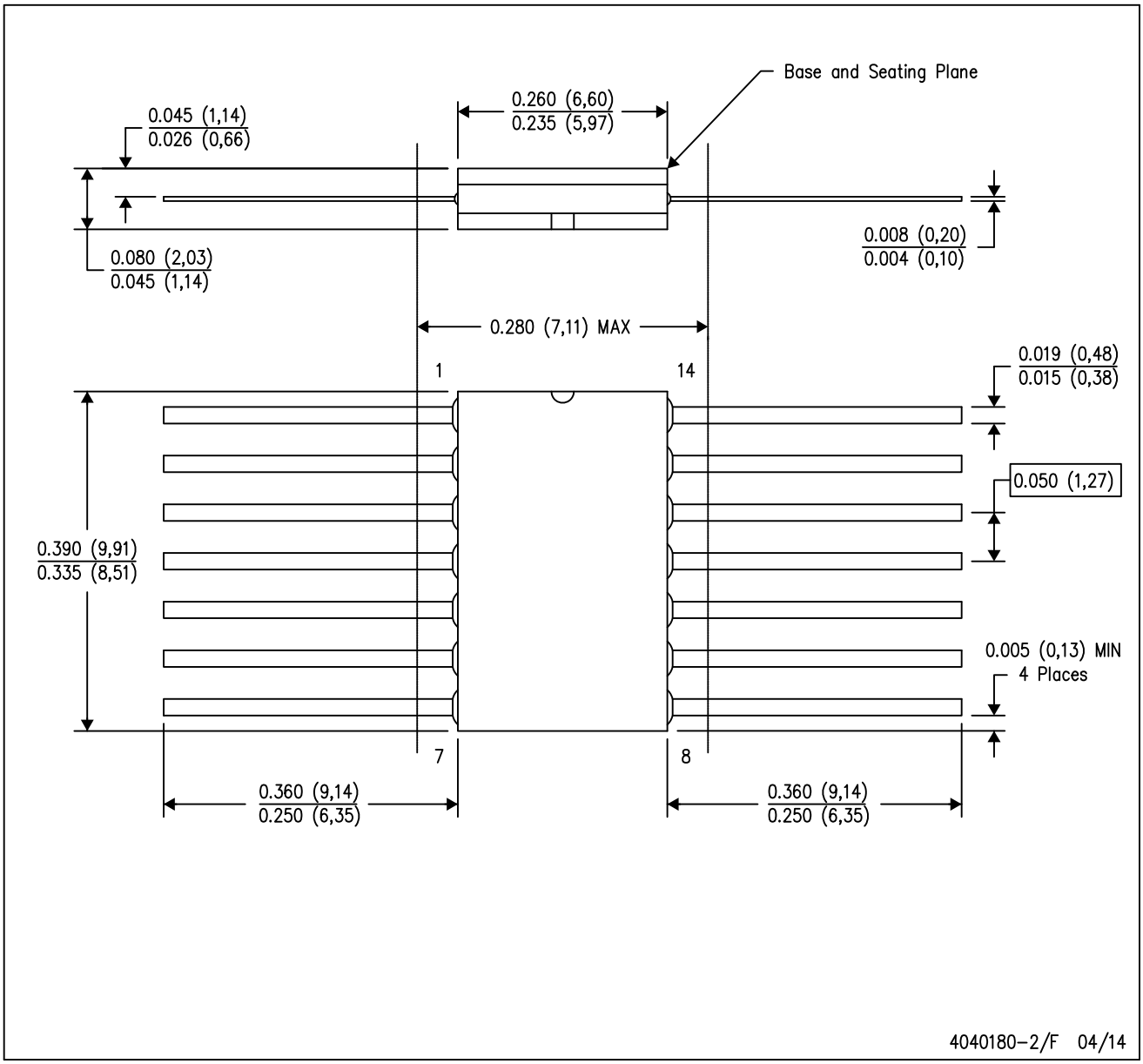



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

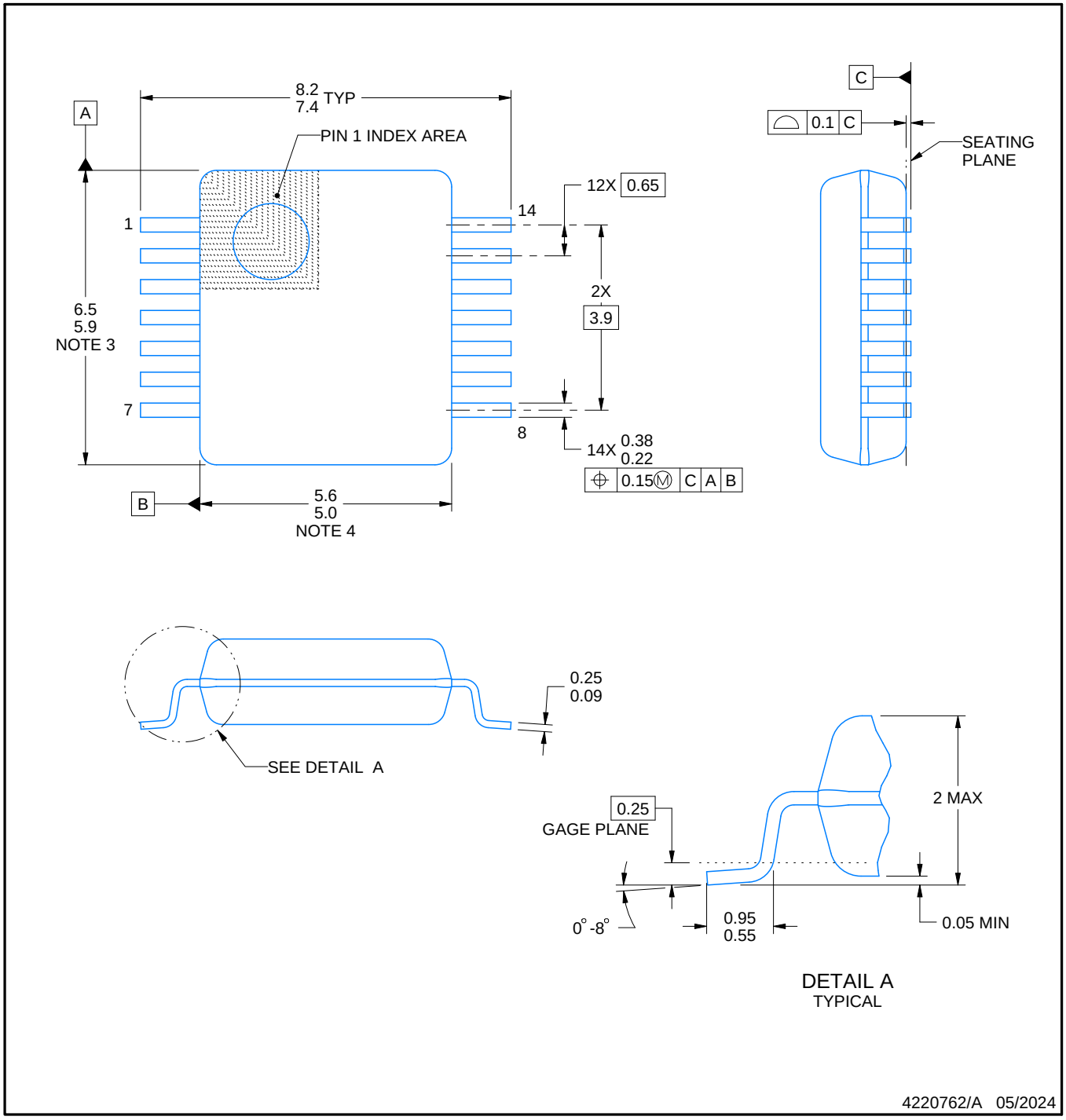
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

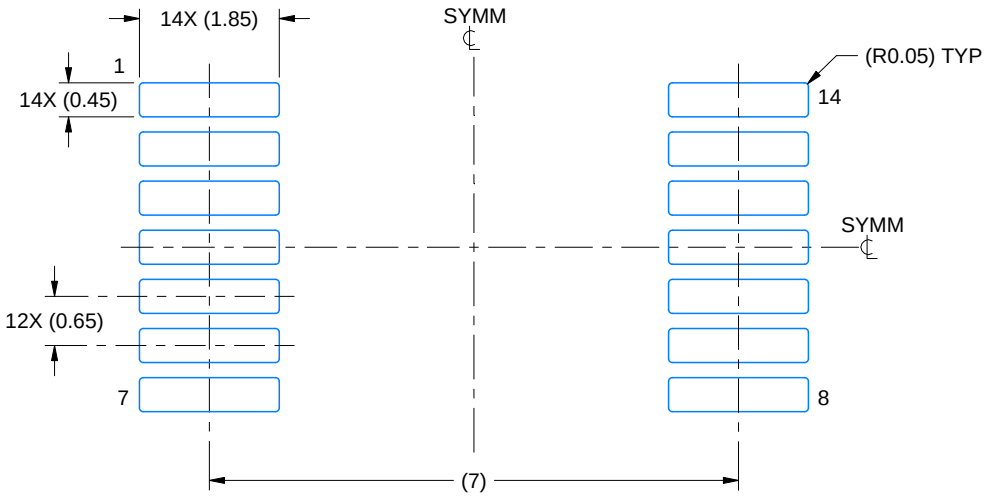



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

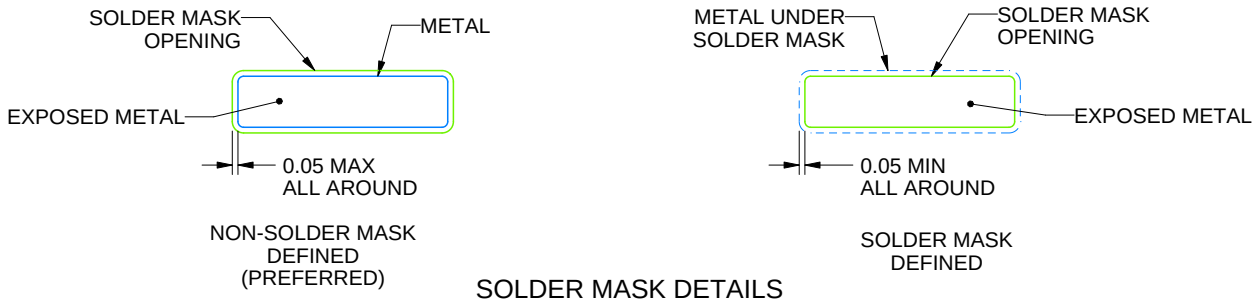



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

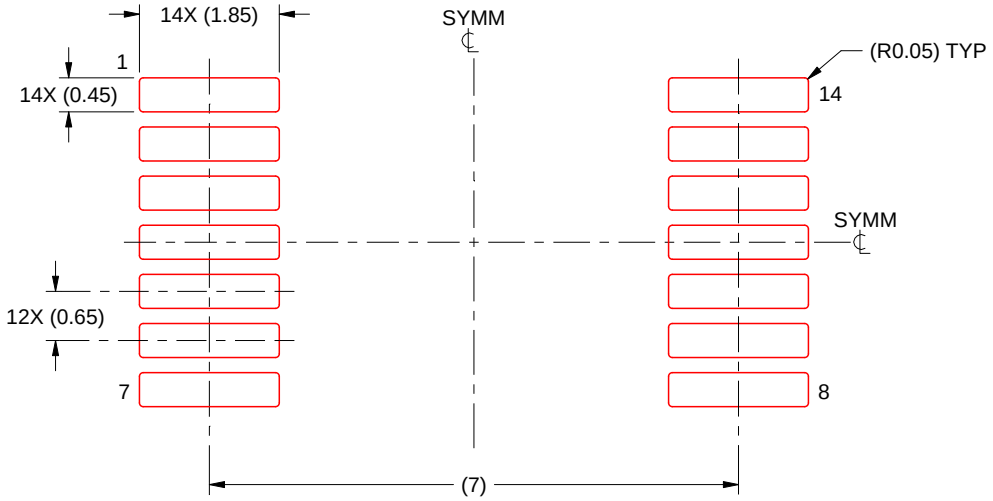



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

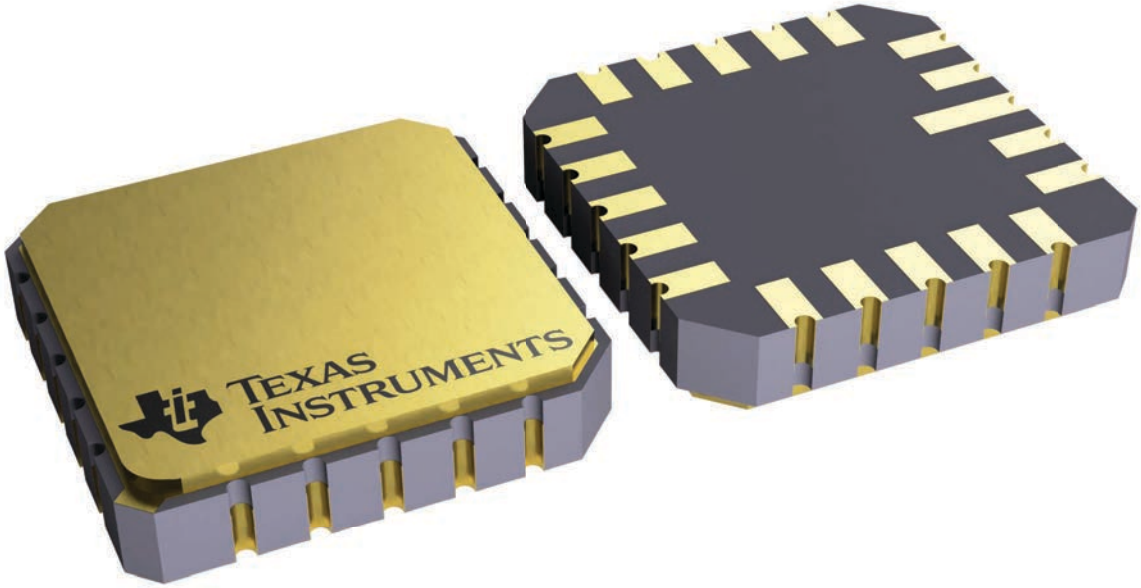
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

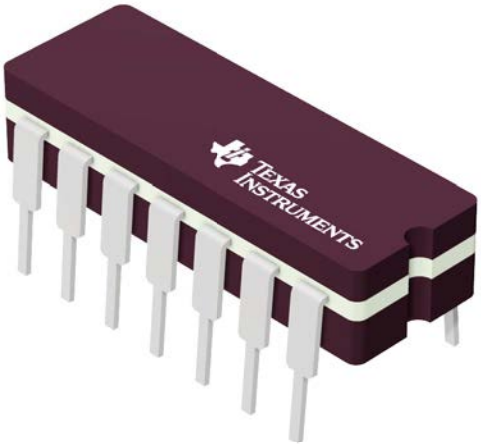
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4229370VA\

# J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

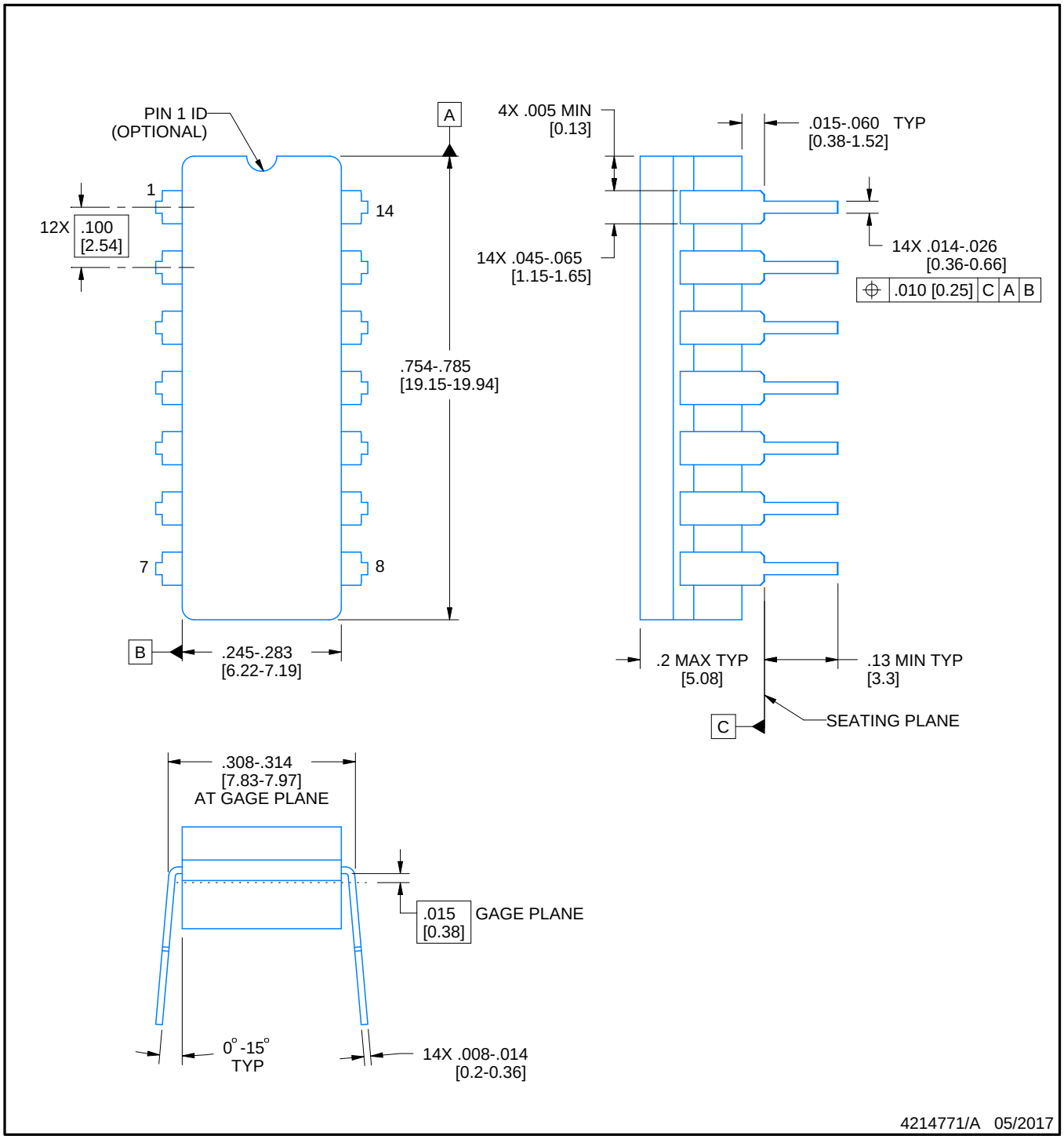
4040083-5/G

# PACKAGE OUTLINE

## J0014A

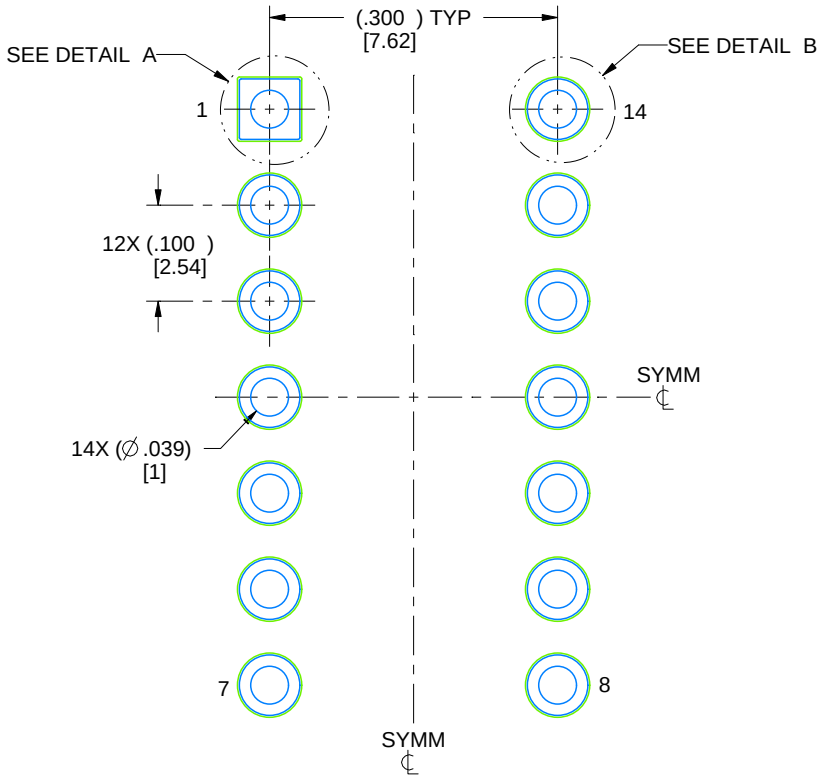
## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

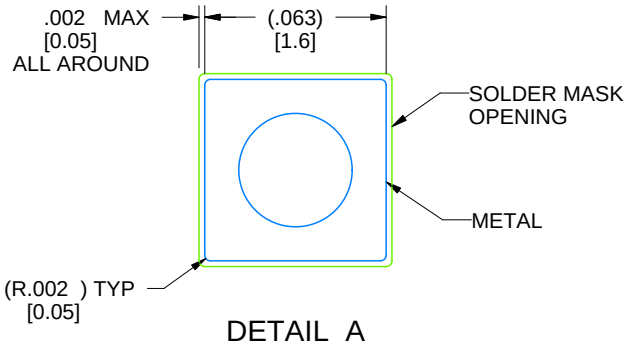



NOTES:

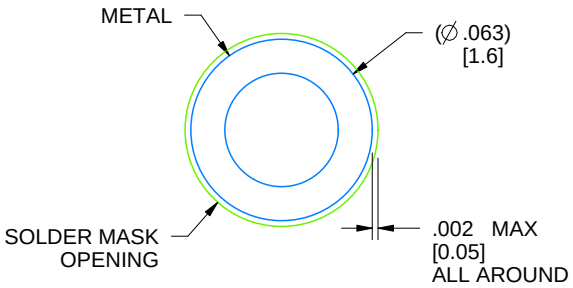
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

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