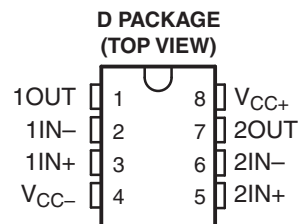


FEATURES

- Qualified for Automotive Applications
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Low Total Harmonic Distortion: 0.003% Typ
- High Input Impedance: JFET-Input Stage
- Latchup-Free Operation
- High Slew Rate: 13 V/ μ s Typ
- Common-Mode Input Voltage Range Includes V_{CC+}



DESCRIPTION/ORDERING INFORMATION

The TL082 JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The device features high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

The I-suffix device is characterized for operation from -40°C to 85°C . The Q-suffix device is characterized for operation from -40°C to 125°C .

ORDERING INFORMATION⁽¹⁾

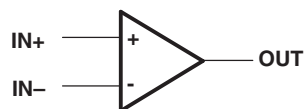
T_J	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Reel of 2500	TL082IDRQ1	TL082I
-40°C to 125°C	SOIC – D	Reel of 2500	TL082QDRQ1	TL082Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

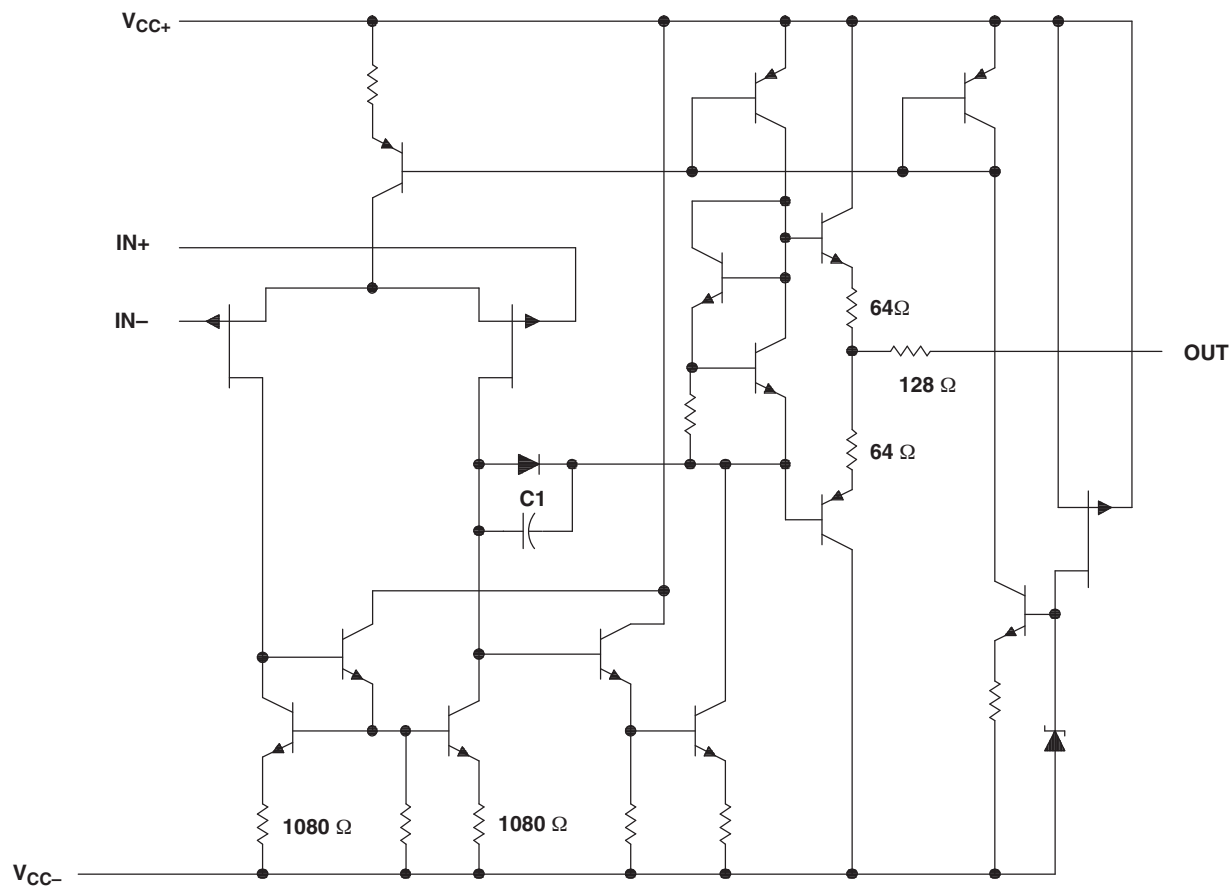


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SYMBOL (EACH AMPLIFIER)



SCHEMATIC (EACH AMPLIFIER)



A. Component values shown are nominal.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			VALUE
V _{CC+}	Supply voltage, positive ⁽²⁾		18 V
V _{CC–}	Supply voltage, negative ⁽²⁾		–18 V
V _{ID}	Differential input voltage ⁽³⁾		±30 V
V _I	Input voltage ⁽²⁾⁽⁴⁾		±15 V
Duration of output short circuit ⁽⁵⁾			Unlimited
Continuous total power dissipation			⁽⁶⁾
T _A	Operating free-air temperature range	TL082I	–40°C to 85°C
		TL082Q	–40°C to 125°C
θ _{JA}	Package thermal impedance, junction to free air ⁽⁷⁾		97°C/W
ESD rating ⁽⁸⁾	Human-Body Model		1.5 kV (H1C)
	Charged-Device Model		1.5 kV (C5)
	Machine Model		200 V (M3)
Operating virtual junction temperature			150°C
T _{stg}	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
- (6) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.
- (8) ESD protection level per JEDEC classifications JESD22-A114 (HBM), JESD22-A115 (MM), and JESD22-C101 (CDM).

ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A ⁽²⁾	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C		3	6	mV
			Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	Full range		18		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current ⁽³⁾	$V_O = 0$	25°C		5	100	pA
			Full range			20	nA
I_{IB}	Input bias current ⁽³⁾	$V_O = 0$	25°C		30	200	pA
			Full range			50	nA
V_{ICR}	Common-mode input voltage range		25°C	± 11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	± 12	± 13.5		V
		$R_L \geq 10\ \text{k}\Omega$	Full range	± 12			
		$R_L \geq 2\ \text{k}\Omega$		± 10	± 12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$, $R_L \geq 2\ \text{k}\Omega$	25°C		50	200	V/mV
			Full range		15		
B1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15\text{ V}$ to $\pm 9\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	80	86		dB
I_{CC}	Supply current (per amplifier)	$V_O = 0$, No load	25°C		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

(2) Full range for T_A is -40°C to 85°C for I-suffix devices and -40°C to 125°C for Q-suffix devices.

(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 14. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

OPERATING CHARACTERISTICS

$V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_I = 10\text{ V}$, $R_L = 2\ \text{k}\Omega$, $C_L = 100\ \text{pF}$, See Figure 1	8	13		V/ μs
t_r	Rise time	$V_I = 20\ \text{mV}$, $R_L = 2\ \text{k}\Omega$, $C_L = 100\ \text{pF}$, See Figure 1		0.05		μs
	Overshoot factor	$V_I = 20\ \text{mV}$, $R_L = 2\ \text{k}\Omega$, $C_L = 100\ \text{pF}$, See Figure 1		20		%
V_n	Equivalent input noise voltage	$R_S = 20\ \Omega$		18		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\ \text{Hz}$ to $10\ \text{kHz}$		4		μV
I_n	Equivalent input noise current	$R_S = 20\ \Omega$, $f = 1\ \text{kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{I\text{rms}} = 6\ \text{V}$, $f = 1\ \text{kHz}$, $AVD = 1$, $R_S \leq 1\ \text{k}\Omega$, $R_L \geq 2\ \text{k}\Omega$		0.003		%

PARAMETER MEASUREMENT INFORMATION

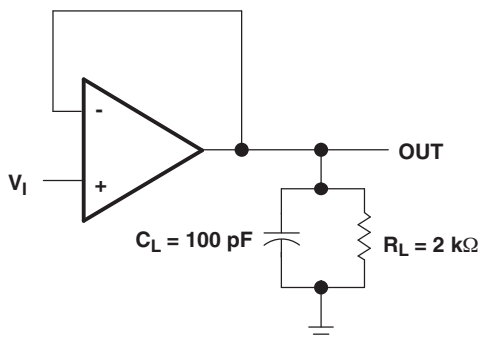


Figure 1.

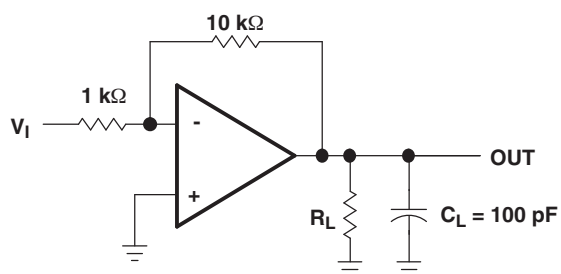


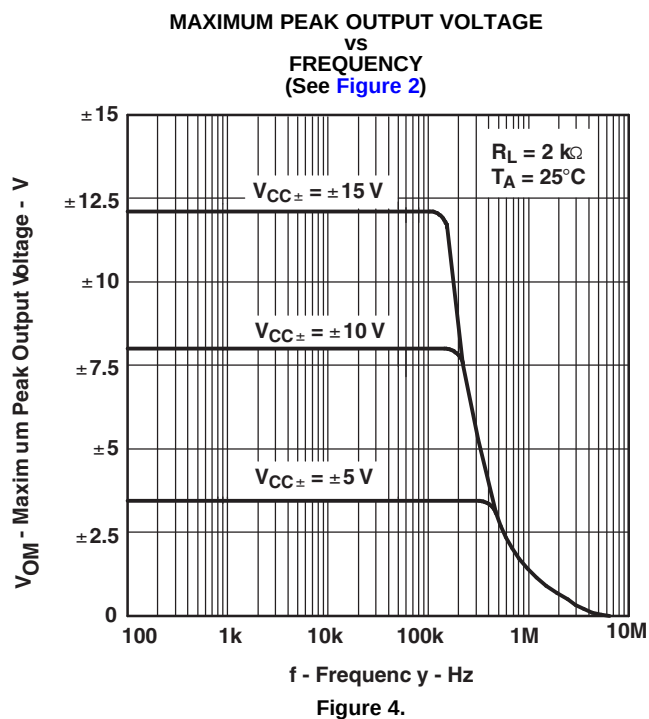
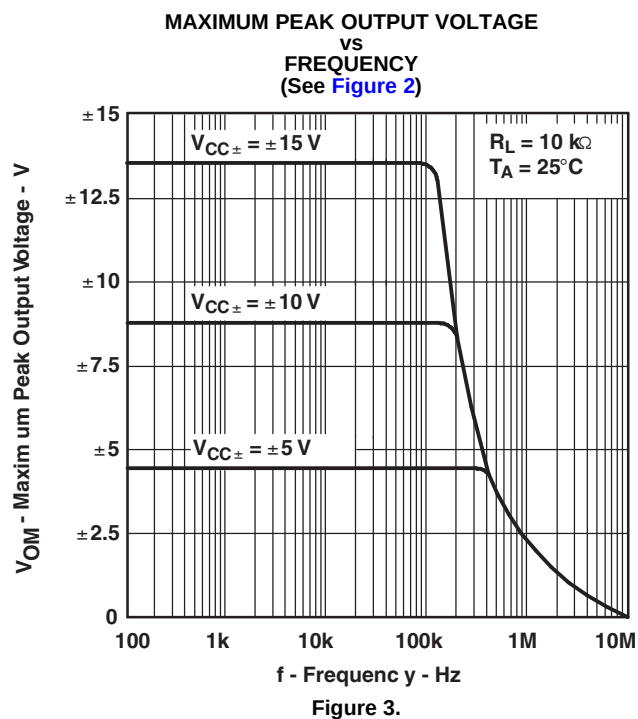
Figure 2.

TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Frequency	3, 4, 5
		vs Free-air temperature	6
		vs Load resistance	7
		vs Supply voltage	8
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature	9
		vs Frequency	10
P_D	Total power dissipation	vs Free-air temperature	11
I_{CC}	Supply current	vs Free-air temperature	12
		vs Supply voltage	13
I_{IB}	Input bias current	vs Free-air temperature	14
	Large-signal pulse response	vs Time	15
V_O	Output voltage	vs Elapsed time	16
CMRR	Common-mode rejection ratio	vs Free-air temperature	17
V_n	Equivalent input noise voltage	vs Frequency	18
THD	Total harmonic distortion	vs Frequency	19



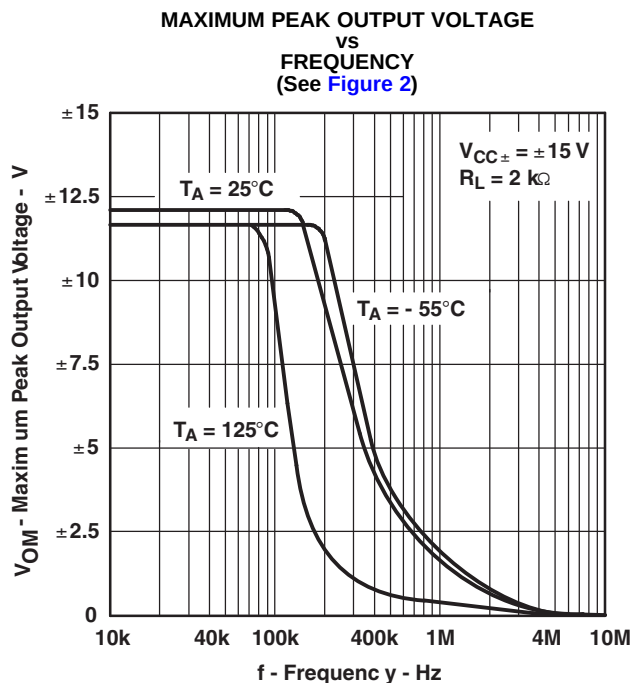


Figure 5.

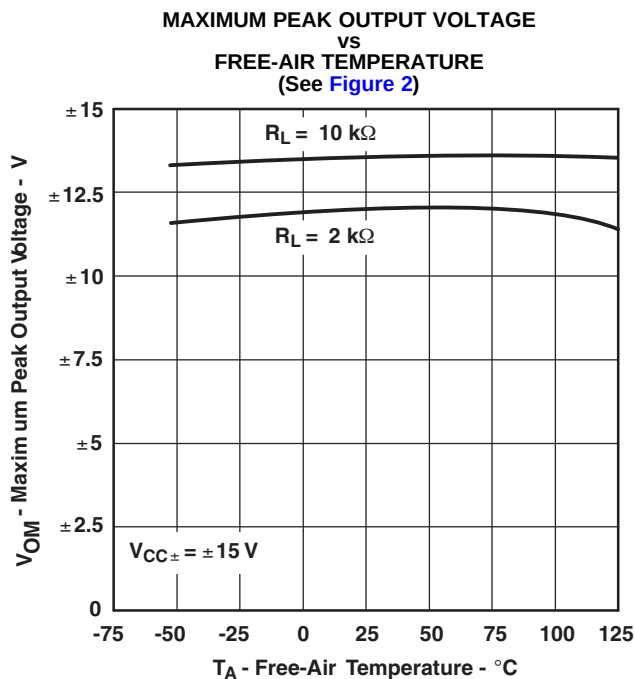


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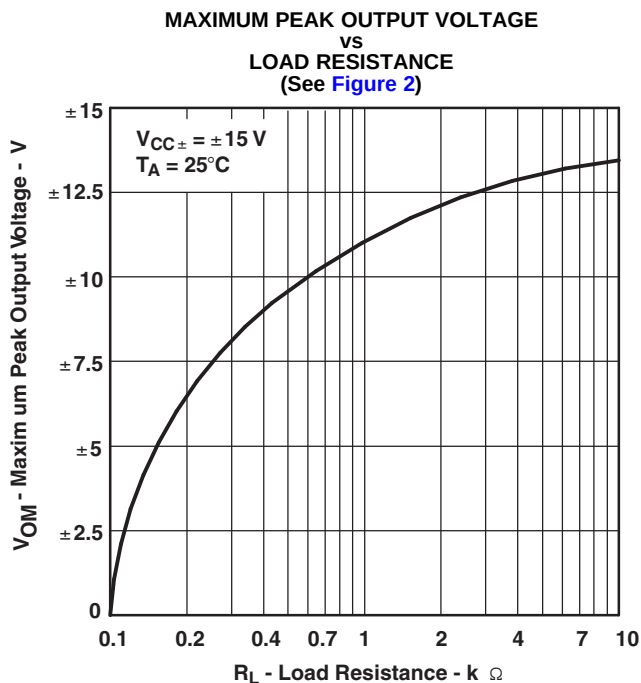


Figure 7.

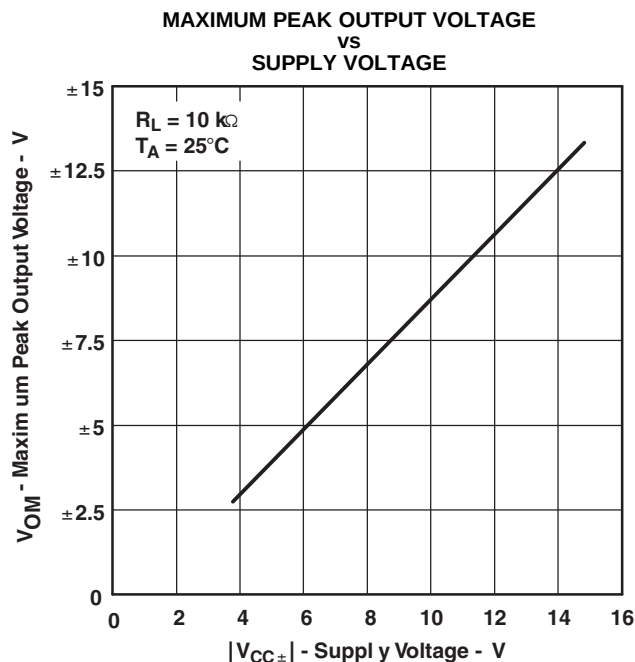


Figure 8.

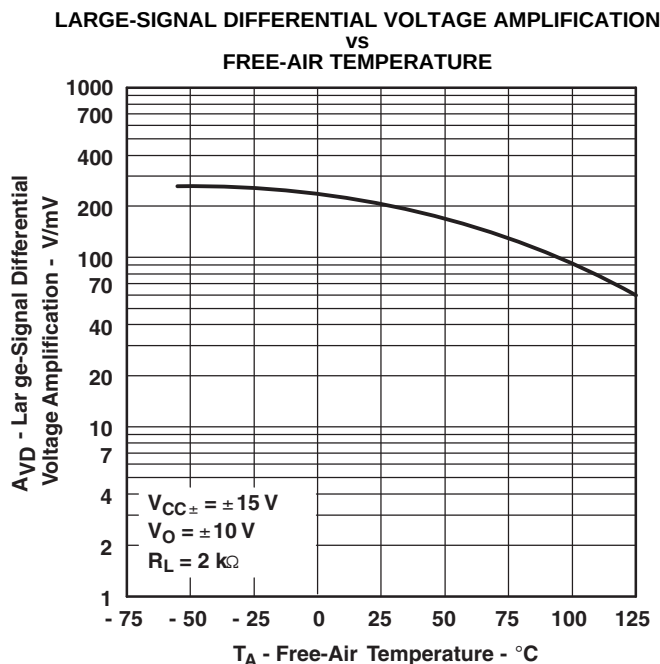


Figure 9.

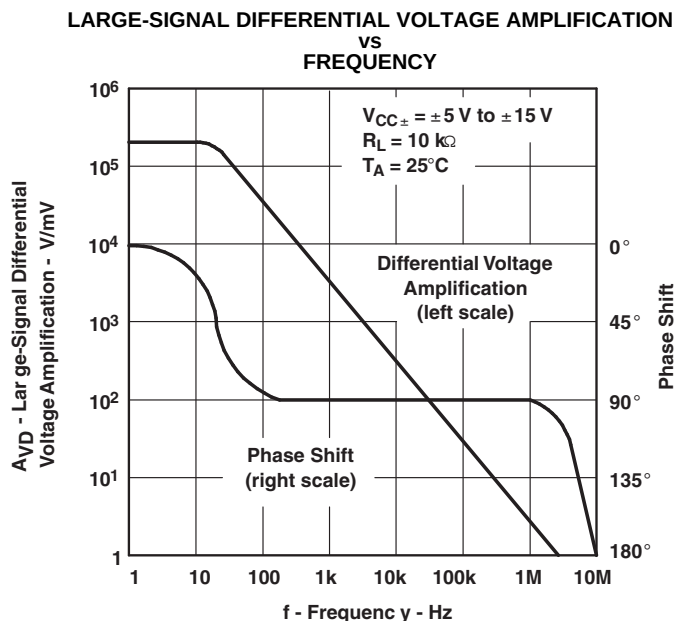


Figure 10.

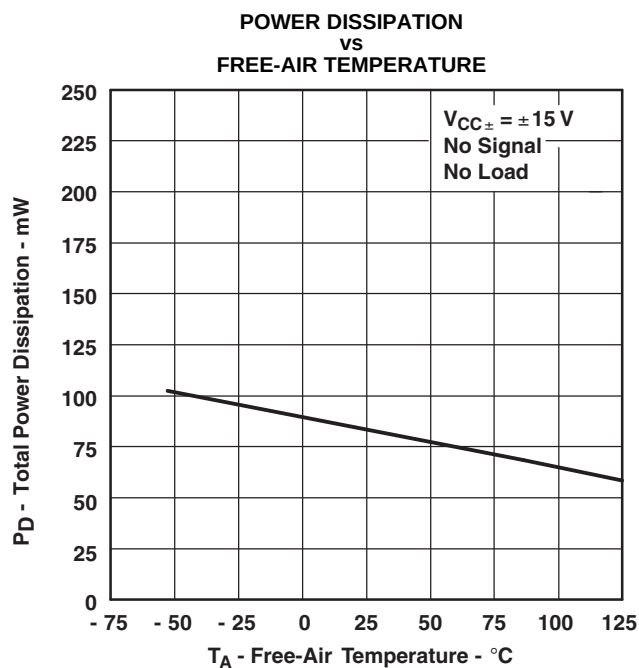


Figure 11.

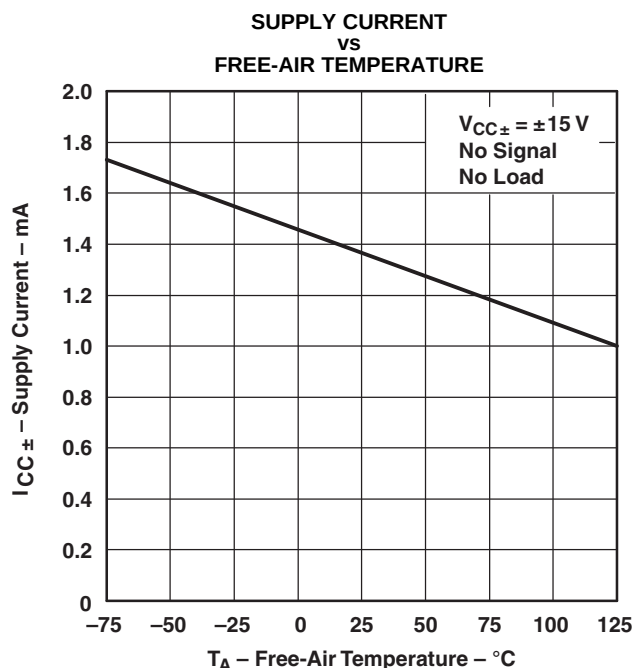


Figure 12.

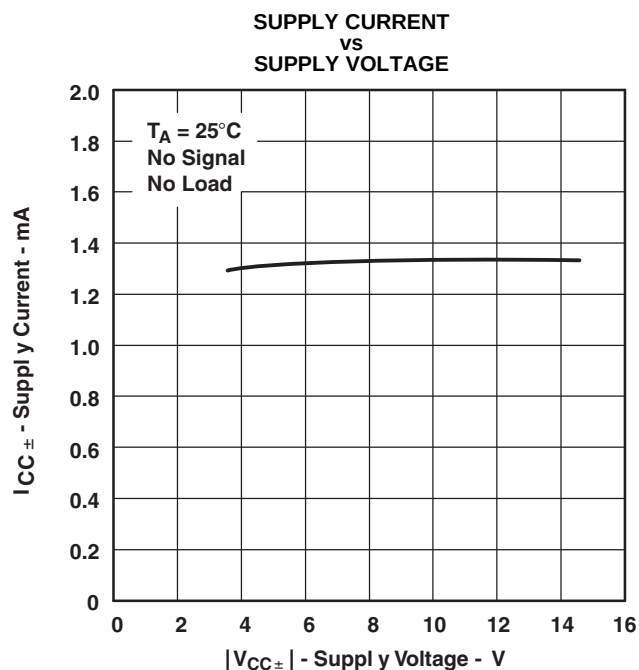


Figure 13.

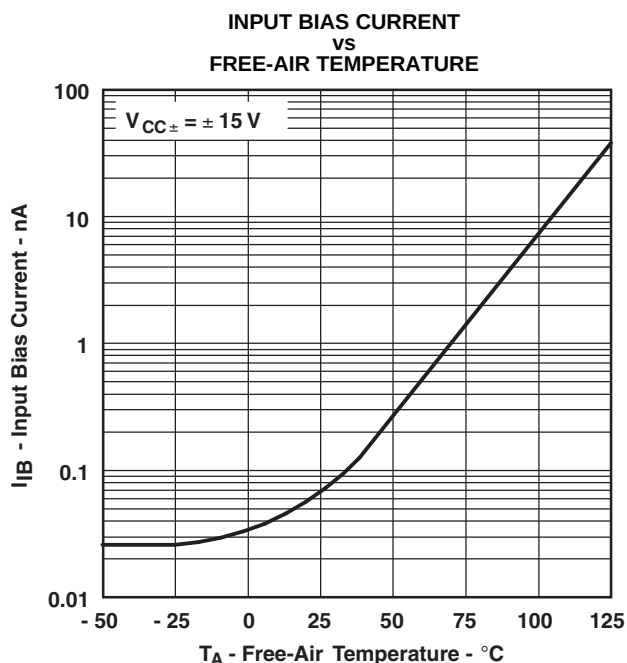


Figure 14.

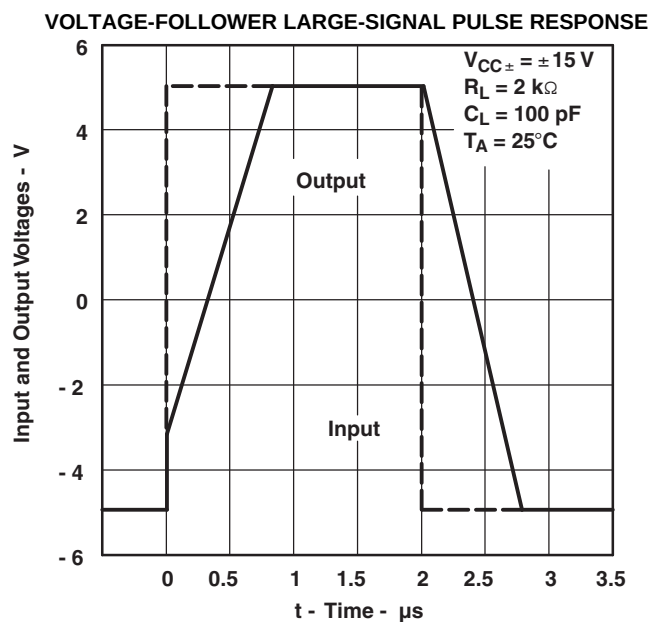


Figure 15.

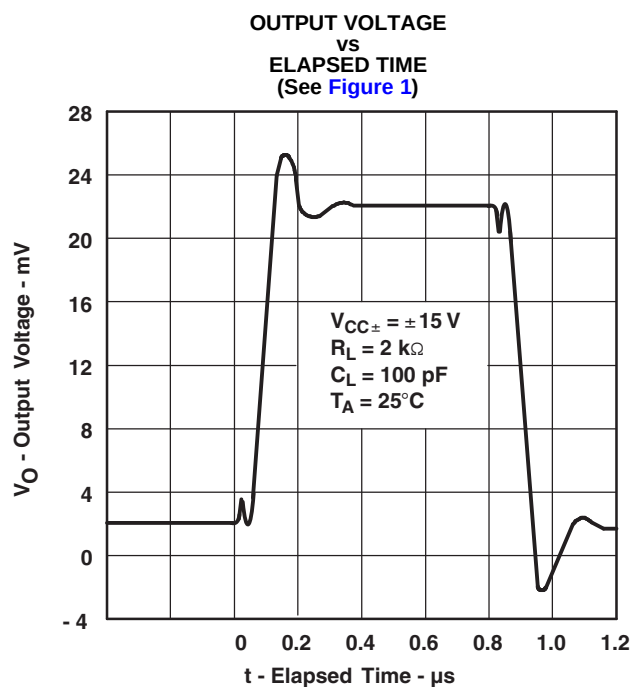


Figure 16.

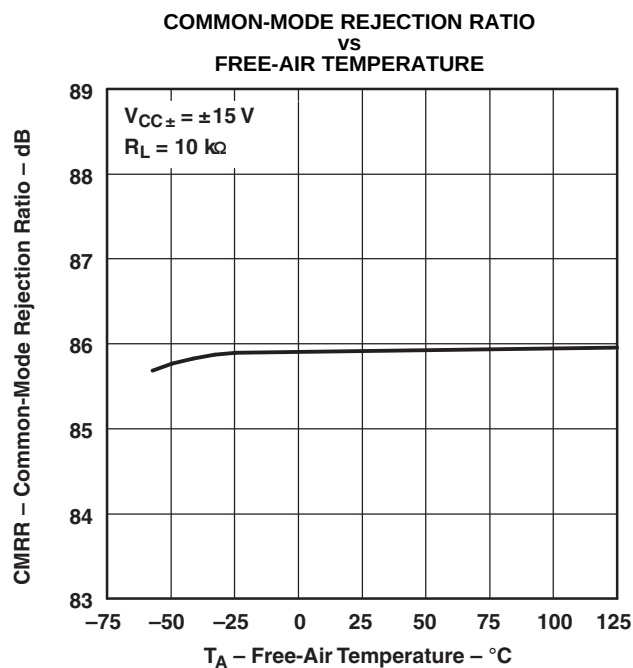


Figure 17.

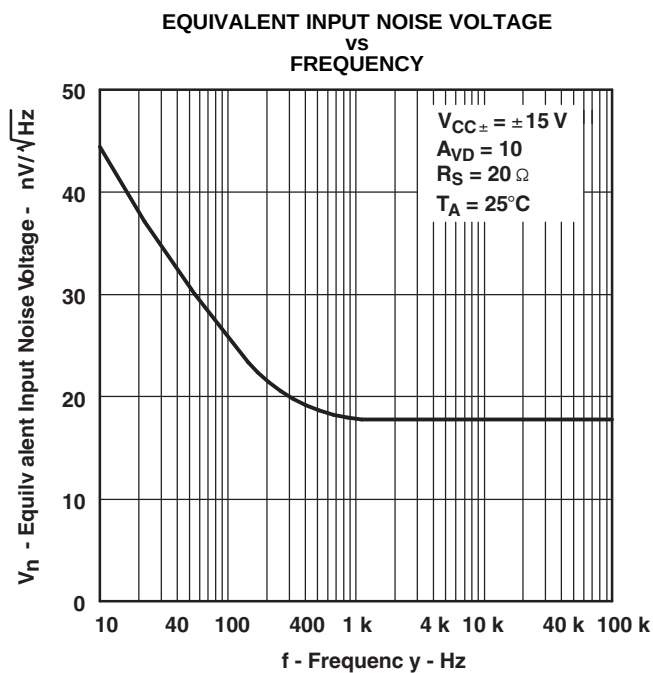


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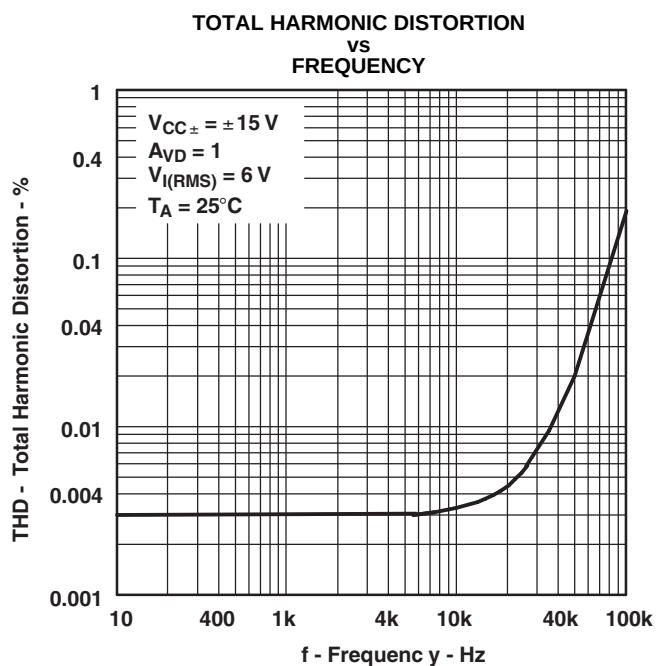


Figure 19.

APPLICATION INFORMATION

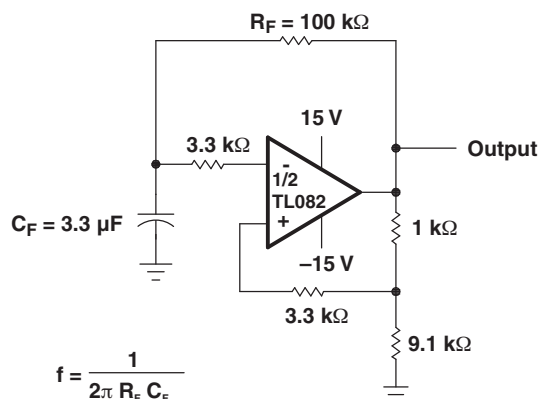


Figure 20.

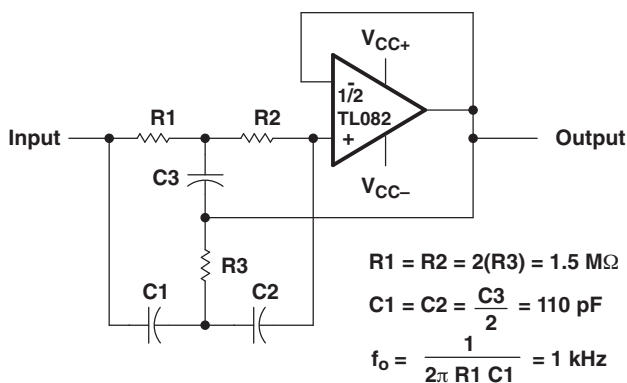


Figure 21.

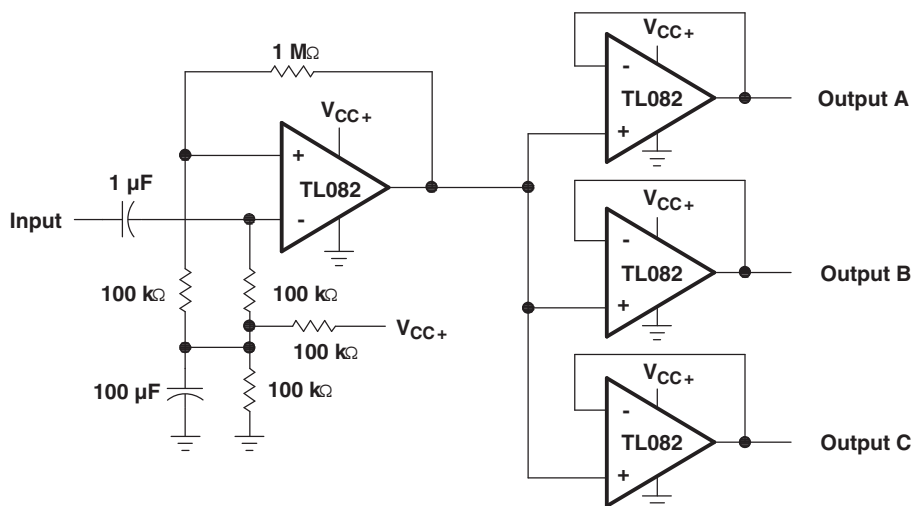
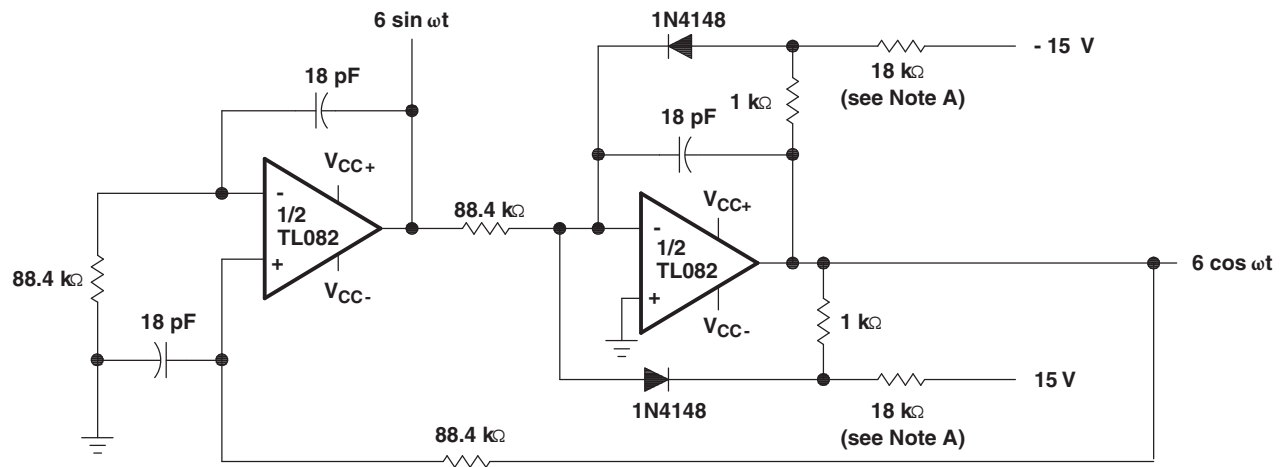


Figure 22. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

Figure 23. 100-kHz Quadrature Oscillator

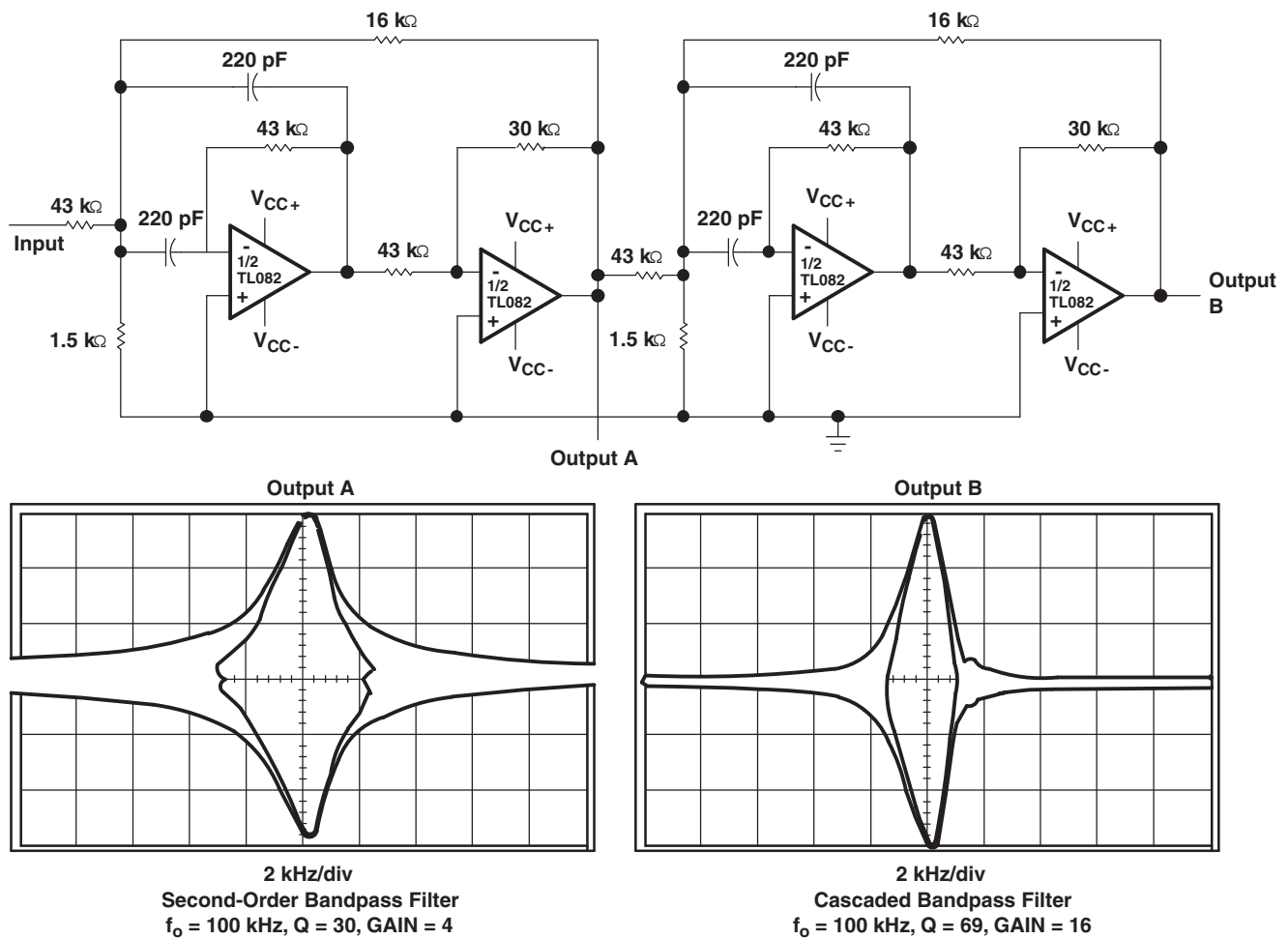


Figure 24. Positive-Feedback Bandpass Filter

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL082IDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082IDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082Q
TL082QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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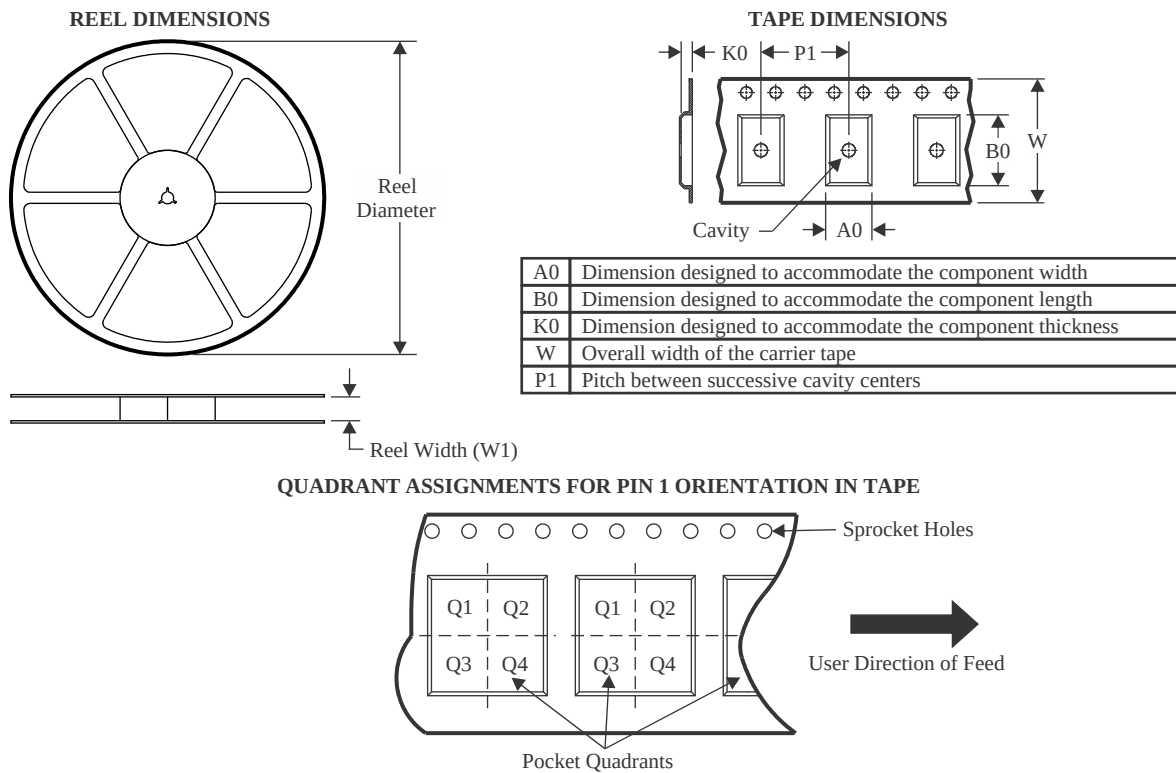
OTHER QUALIFIED VERSIONS OF TL082-Q1 :

- Catalog : [TL082](#)
- Military : [TL082M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

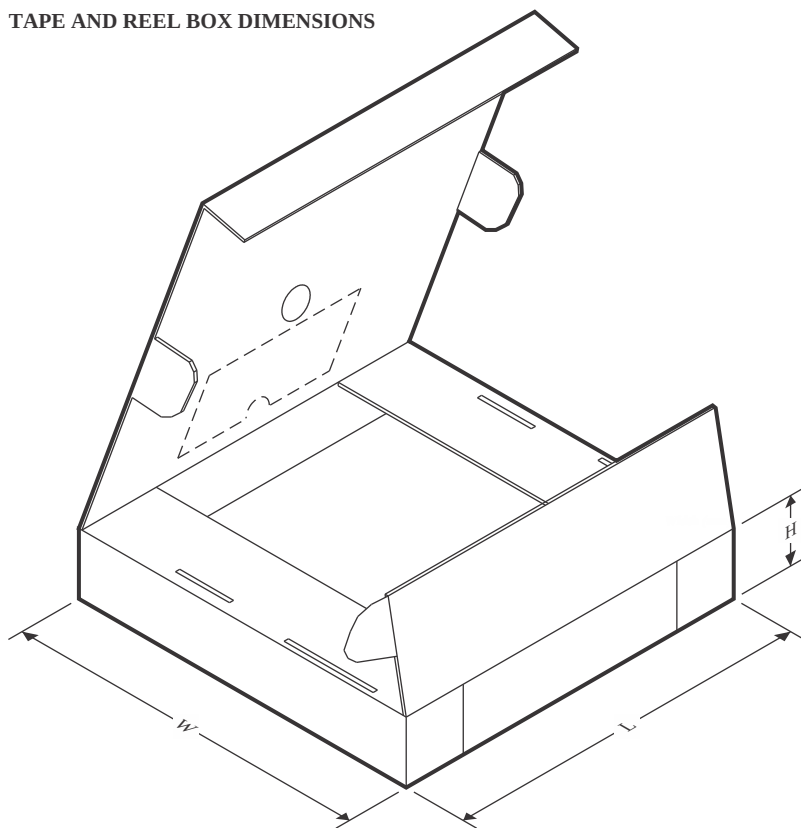
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082IDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082IDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TL082QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



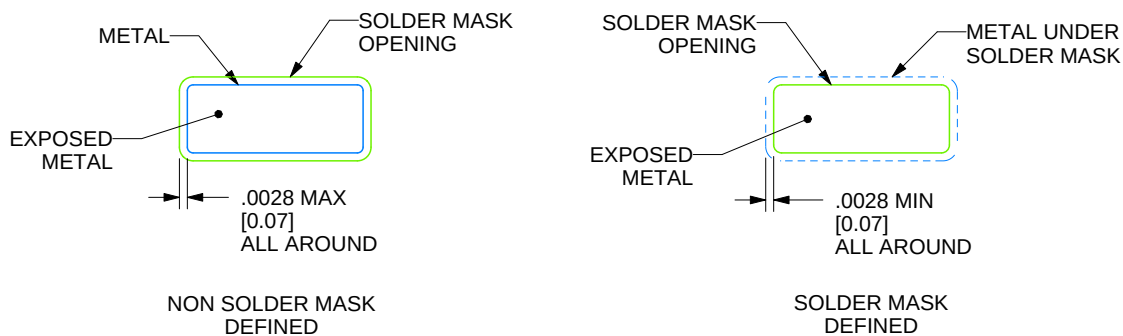
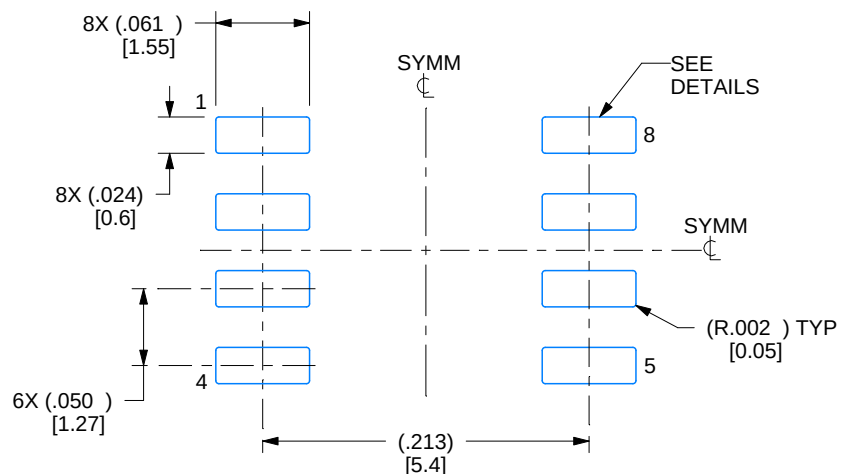
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

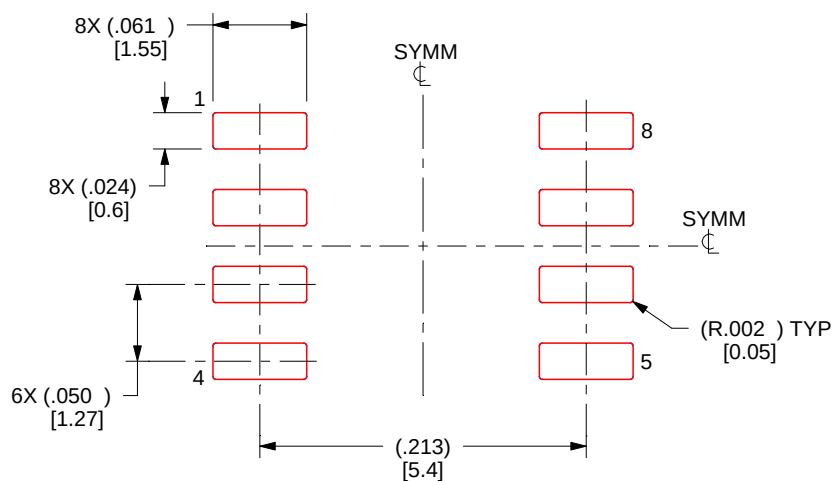
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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