UCC21222 4A, 6A, 3kVRMS Isolated Dual-Channel Gate Driver

1 Features

- Universal: dual low-side, dual high-side or halfbridge driver
- Junction temperature range –40 to +150°C
- Up to 4A peak source and 6A peak sink output
- Common-mode transient immunity (CMTI) greater than 125V/ns
- Up to 25V VDD output drive supply
  - 8V, VDD UVLO options
- Switching parameters:
  - 33ns typical propagation delay
  - 5ns maximum pulse-width distortion
  - 10µs maximum VDD power-up delay
- UVLO protection for all power supplies
- Fast disable for power sequencing
- Safety-related certifications (planned):
  - 4242V_{PK} isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 3000V_{RMS} isolation for 1 minute per UL 1577
  - CQC Certification per GB4943.1-2022

2 Applications

- On-board battery chargers
- High-voltage DC-DC converters
- Automotive HVAC, body electronics

3 Description

The UCC21222 is an isolated dual channel gate driver family with programmable dead time and wide temperature range. It is designed with 4A peak-source and 6A peak-sink current to drive power MOSFET, SiC, GaN, and IGBT transistors.

The UCC21222 can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. The input side is isolated from the two output drivers by a 3kV_{RMS} isolation barrier, with a minimum of 125V/ns common-mode transient immunity (CMTI).

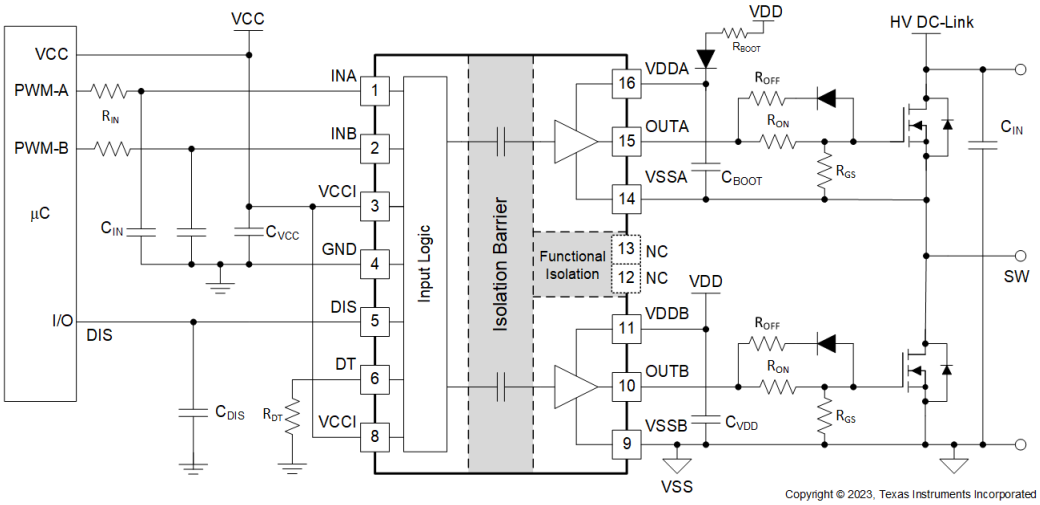
Protection features include: resistor programmable dead time, disable feature to shut down both outputs simultaneously, and integrated de-glitch filter that rejects input transients shorter than 5ns. All supplies have UVLO protection.

With all these advanced features, the UCC21222 device enables high efficiency, high power density, and robustness in a wide variety of power applications.

Device Information

PART NUMBER	PACKAGE(1)	REC. VDD SUPPLY MIN
UCC21222	D (SOIC 16)	9.2V

(1) For all available packages, see Section 13.



Typical Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

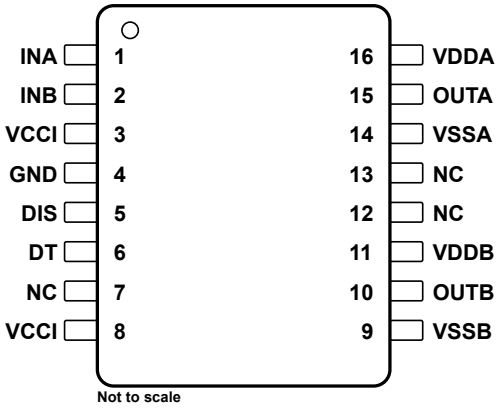

Figure 4-1. D Package 16-Pin SOIC Top View

Table 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
DIS	5	I	Disable both driver outputs if asserted high, enable both outputs if set low. It is recommended to tie this pin to ground if not used to achieve better noise immunity. This pin is internally pulled high if left floating. It is recommended to use an RC filter on DIS pin to filter high frequency noise when connecting to a microcontroller, with R = 0 Ω to 100 Ω and C = 100 pF to 1000 pF.
DT	6	I	DT pin configurations: • DT pin float or short to VCCI disables dead time interlock function (allows outputs to overlap) • Place 1.7-kΩ to 100-kΩ resistor (RDT) between DT and GND to set minimum dead time between driver outputs • Place 0-Ω to 150-Ω resistor, or short DT pin to GND to have two outputs interlocked • TI does not recommend bypassing this pin with a ceramic capacitor >1nF.
GND	4	G	Primary-side ground reference. All signals in the primary side are referenced to this ground.
INA	1	I	Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to use an RC filter on INA to filter high frequency noise, with R = 10 Ω to 100 Ω and C = 10 pF to 100 pF.
INB	2	I	Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to use an RC filter on INB to filter high frequency noise, with R = 10 Ω to 100 Ω and C = 10 pF to 100 pF.
NC	7	–	No Internal connection.
NC	12	–	No internal connection.
NC	13	–	No internal connection.
OUTA	15	O	Output of driver A. Connect to the gate of the A channel transistor through a gate resistor.
OUTB	10	O	Output of driver B. Connect to the gate of the B channel transsitor through a gate resistor.
VCCI	3	P	Primary-side supply voltage. Locally decouple to GND using a low ESR/ESL capacitor located as close to the device as possible.
VCCI	8	P	Primary-side supply voltage. This pin is internally shorted to pin 3.
VDDA	16	P	Secondary-side power for driver A. Locally decouple to VSSA using a low ESR/ESL capacitor located as close to the device as possible.
VDDB	11	P	Secondary-side power for driver B. Locally decouple to VSSB using low ESR/ESL capacitor located as close to the device as possible.
VSSA	14	G	Ground reference for secondary side A channel.
VSSB	9	G	Ground reference for secondary side B channel.

(1) P = Power, G = Ground, I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
VCCI to GND	Input bias supply voltage	–0.3	6	V
VDDA, VDDB to VSS	Output bias supply voltage	–0.3	30	V
OUTA to VSSA, OUTB to VSSB	Output signal DC voltage	–0.3	VDDA/B + 0.3	V
	Output signal transient voltage for 200-ns	–2	VDDA/B + 0.3	V
INA, INB, DT, DIS to GND	Input signal DC voltage	–0.3	VCCI + 0.3[2]	V
INA, INB to GND	Input signal transient voltage for 50-ns	–5	VCCI + 0.3[2]	V
Channel to channel isolation voltage	|VSSA-VSSB| in D package		1500	V
T_J	Junction temperature	–40	150	℃
T_{stg}	Storage temperature	–65	150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CCI}	Input bias pin supply voltage	3.0		5.5	V
VDDA, VDDB	UCC21222 0 - 8V UVLO Output bias supply voltage, VDDA-VSSA, VDDB-VDDB	9.2		25	V
T_J	Junction temperature	–40		150	℃

5.4 Thermal Information

THERMAL METRIC[1]		UCC21222 0 D 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
Ψ_{JT}	Junction-to-top(center) characterization parameter	28	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCCI = 5V, VDDA/VDDB = 20V, INA/B = 3.3V, 460kHz 50% duty cycle square wave, C_L=2.2nF, T_J=150°C, T_A=25°C			950	mW
P_{DI}	Maximum power dissipation by transmitter side				50	mW
P_{DA}, P_{DB}	Maximum power dissipation by each driver side				450	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
General				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	>4	mm
CPG	External Creepage[1]	Shortest terminal-to-terminal distance across the package surface	>4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1200	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 6-1	850	V_{RMS}
		DC voltage	1200	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	4242	V_{PK}
V_{IMP}	Maximum inpulse voltage	Tested in air, 1.2/50-µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[2]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	6500	V_{PK}
q_{pd}	Apparent charge[3]	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[4]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	~1.2	pF
R_{IO}	Insulation resistance, input to output[4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage for UCC2155x	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

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5.7 Safety Limiting Values

PARAMETER		TEST CONDITIONS	SIDE	MIN	TYP	MAX	UNIT
I_S	Safety output supply current	$R_{\theta\ JA}$ = 80.2°C/W, $V_{DDA/B}$ = 15 V, T_J = 150°C, T_A = 25°C	DRIVER A, DRIVER B			50	mA
		$R_{\theta\ JA}$ = 80.2°C/W, $V_{DDA/B}$ = 25 V, T_J = 150°C, T_A = 25°C				30	
P_S	Safety supply power	$R_{\theta\ JA}$ = 80.2°C/W, T_J = 150°C, T_A = 25°C	INPUT			50	mW
			DRIVER A			750	
			DRIVER B			750	
			TOTAL			1550	
T_S	Maximum safety temperature(1)					150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{qJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where VI is the maximum supply voltage.

5.8 Electrical Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitance from VCCI to GND, V_{VDDx} = 12V (for 5V and 8V UVLO), , 1-µF + 100-nF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin floating, EN = VCC or DIS = GND, T_J = –40°C to +150°C, C_L = 0 pF, unless otherwise noted [(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC}	VCC quiescent current	V_{INx} = 0 V, DIS = GND; VCC=3.3V		1.4	2	mA
		V_{INx} = 0 V, DIS = GND; VCC=5V		1.4	2	
		V_{INx} = VCC, DIS = GND; VCC=3.3V		4.2	4.8	
		V_{INx} = VCC, DIS = GND; VCC=5V		4.2	4.8	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, DIS = GND; VCC=3.3V		2.7	3.2	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, DIS = GND; VCC=5V		2.7	3.2	
I_{VDDx}	VDDx quiescent current	V_{INx} = 0 V, DIS = GND		1.2	2	mA
		V_{INx} = 0 V, DIS = GND; VDD=25V		1.4	2.3	
		V_{INx} = VCC, DIS = GND		1.4	2.2	
		V_{INx} = VCC, DIS = GND; VDD=25V		1.5	2.5	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, DIS = GND		2.7	4.4	
		V_{INx} PWM at 0V to VCC at f_{SW} = 500kHz, DIS = GND; VDD=25V		2.7	4.4	
VCC SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCC_ON}	VCC UVLO Rising Threshold		2.55	2.7	2.85	V
V_{VCC_OFF}	VCC UVLO Falling Threshold		2.35	2.5	2.65	
V_{VCC_HYS}	VCC UVLO Threshold Hysteresis			0.2		
$t_{VCC+ \text{ to } OUT}$	VCC UVLO ON Delay		18		80	µs
$t_{VCC- \text{ to } OUT}$	VCC UVLO OFF Delay		0.5	1.2	7	
t_{VCCFIL}	VCC UVLO Deglitch Filter		0.4	0.9	3.1	
VDD SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS AND DELAY						
V_{VDD_ON}	VDDx UVLO Rising Threshold	8-V UVLO Option	7.7	8.5	8.9	V
V_{VDD_OFF}	VDDx UVLO Falling Threshold		7.2	7.9	8.4	
V_{VDD_HYS}	VDDx UVLO Threshold Hysteresis			0.6		
$t_{VDD+ \text{ to } OUT}$	VDDx UVLO ON Delay				10	µs
$t_{VDD- \text{ to } OUT}$	VDDx UVLO OFF Delay		0.1	0.5	2	
t_{VDDFIL}	VDDx UVLO Deglitch Filter		0.1	0.17		
INA, INB, AND / DIS						
V_{INx_H}, V_{DIS_H} ,	Input High Threshold Voltage			2	2.3	V
V_{INx_L}, V_{DIS_L} ,	Input Low Threshold Voltage		0.8	1		
V_{INx_HYS}, V_{DIS_HYS} ,	Input Threshold Hysteresis			1		
R_{INxD}	INx Pin Pull Down Resistance	INx = 3.3V	50	90	185	kΩ
R_{DISD}	DIS Pin Pull Up Resistance	DIS= 3.3V	50	90	185	kΩ
OUTPUT DRIVER STAGE						
I_{O+}	Peak Output Source Current	C_{VDDx} = 10 µF, C_L = 0.22 µF, f = 1 kHz		–4		A
I_{O-}	Peak Output Sink Current	C_{VDDx} = 10 µF, C_L = 0.22 µF, f = 1 kHz		6		A
R_{OH}	Pull up resistance. R_{OH} does not represent drive pull-up performance. See Section 8.3.4 for details.	I_{OUTx} = –0.05A		5		Ω
R_{OL}	Pull down resistance	I_{OUTx} = 0.05A		0.55		
ACTIVE PULL-DOWN						
V_{OUTPD}	Output Active Pull Down on OUTx	I_{OUT} = 200mA, VDDx floating and unpowered.		1.6	2	V

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5.8 Electrical Characteristics (continued)

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitance from VCCI to GND, V_{VDDx} = 12V (for 5V and 8V UVLO), , 1-µF + 100-nF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin floating, EN = VCC or DIS = GND, T_J = –40°C to +150°C, C_L = 0 pF, unless otherwise noted (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUTPD}	Output Active Pull Down on OUTx	I_{OUT} = 200mA, C_{VDD}=100nF and unpowered.		1.6	2	V
DEADTIME AND OVERLAP PROGRAMMING						
DT_S	Disable DT Function	DT pin open or pull DT pin to VCC	Output overlapping determined by INA, INB			-
	Deadtime Programming for R_{DT}≤0.15kΩ	R_{DT}=0~0.15kΩ	-6	0.2	6	ns
	Deadtime Programming for 1.7kΩ≤R_{DT}≤100kΩ DT (ns) = 8.6×R_{DT}(kΩ) + 13	R_{DT} = 10 kΩ	86	99	112	ns
		R_{DT} = 20 kΩ	167	185	203	
		R_{DT} = 50 kΩ	399	443	487	

(1) Current direction in the testing conditions are defined to be positive into the pin and negative out of the specified terminal (unless otherwise noted)

5.9 Switching Characteristics

V_{VCCI} = 3.3 V or 5.0 V, 0.1-µF capacitance from VCCI to GND, V_{VDDx} = 12V (for 5V and 8V UVLO) , 1-µF+100-nF capacitance from VDDA and VDDB to VSSA and VSSB, DT pin floating, EN = VCC or DIS = GND, T_J = –40°C to +150°C, C_L = 0 pF, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}	Output Rise Time	C_L=1.8nF, VDDx=12V, 20% to 80%		8		ns
		C_L=1.8nF, VDDx=25V, 20% to 80%		8		
t_{FALL}	Output Fall Time	C_L=1.8nF, VDDx=12V, 10% to 90%		8		ns
		C_L=1.8nF, VDDx=25V, 10% to 90%		8		
t_{PDLH}	Propagation Delay – Low to High	Input Pulse Width = 100ns, 500kHz, measure with Input VIH to output 10%	26	33	45	ns
t_{PDHL}	Propagation Delay – High to Low	Input Pulse Width = 100ns, 500kHz, measure with Input VIL to output 90%	26	33	45	ns
$t_{PD_DIS_HL}$	DIS Response Delay – High to Low	t_{EN/DIS_FIL} = 20 ns (typ), VDD=VDD_ON+0.2V and above, Input Pulse Width = 100ns, 500kHz	27	48	80	ns
$t_{PD_DIS_LH}$	DIS Response Delay – Low to High		27	48	80	ns
t_{PWmin}	Minimum Input Pulse Width That Passes to Output	VDD=VDD_ON+0.2V and above	4	12	30	ns
t_{DM}	Propagation Delay Matching for Dual Channel Driver	Input Pulse Width = 100ns, 500kHz, T_J = –40°C to -10°C $\lvert t_{PDLHA} – t_{PDLHB}\rvert$, $\lvert t_{PDHLA} – t_{PDHLB}\rvert$	0		6.5	ns
		Input Pulse Width = 100ns, 500kHz, T_J = –10°C to +150°C $\lvert t_{PDLHA} – t_{PDLHB}\rvert$, $\lvert t_{PDHLA} – t_{PDHLB}\rvert$	0		5	ns
t_{PWD}	Pulse Width Distortion	Input Pulse Width = 100ns, 500kHz $\lvert t_{PDLHA} – t_{PDHLA}\rvert$, $\lvert t_{PDLHB}– t_{PDHLB}\rvert$	0		5	ns
$\lvert CM_H\rvert$	High-level Common Mode Transient Immunity	V_{CM} = 1500V	125			V/ns
$\lvert CM_L\rvert$	Low-level Common Mode Transient Immunity		125			V/ns

5.10 Insulation Characteristics Curves

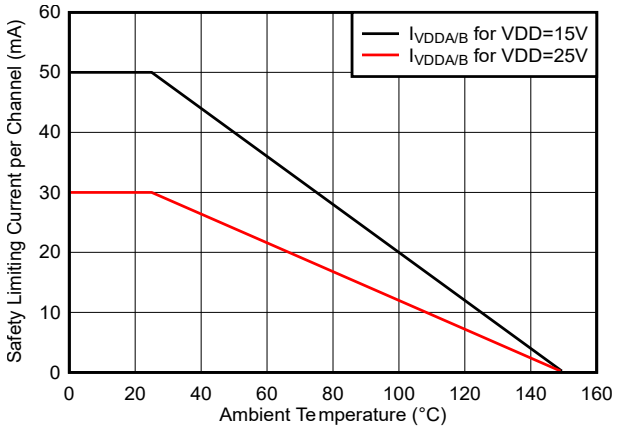

Figure 5-1. Thermal Derating Curve for Limiting Current per VDE (current in each channel with both channels running simultaneously)

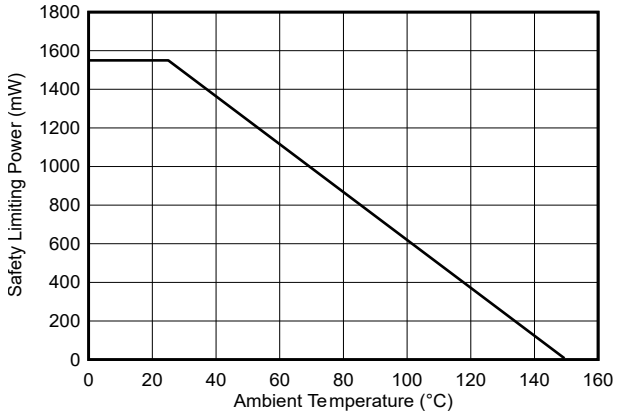

Figure 5-2. Thermal Derating Curve for Safety-Related Limiting Power per VDE

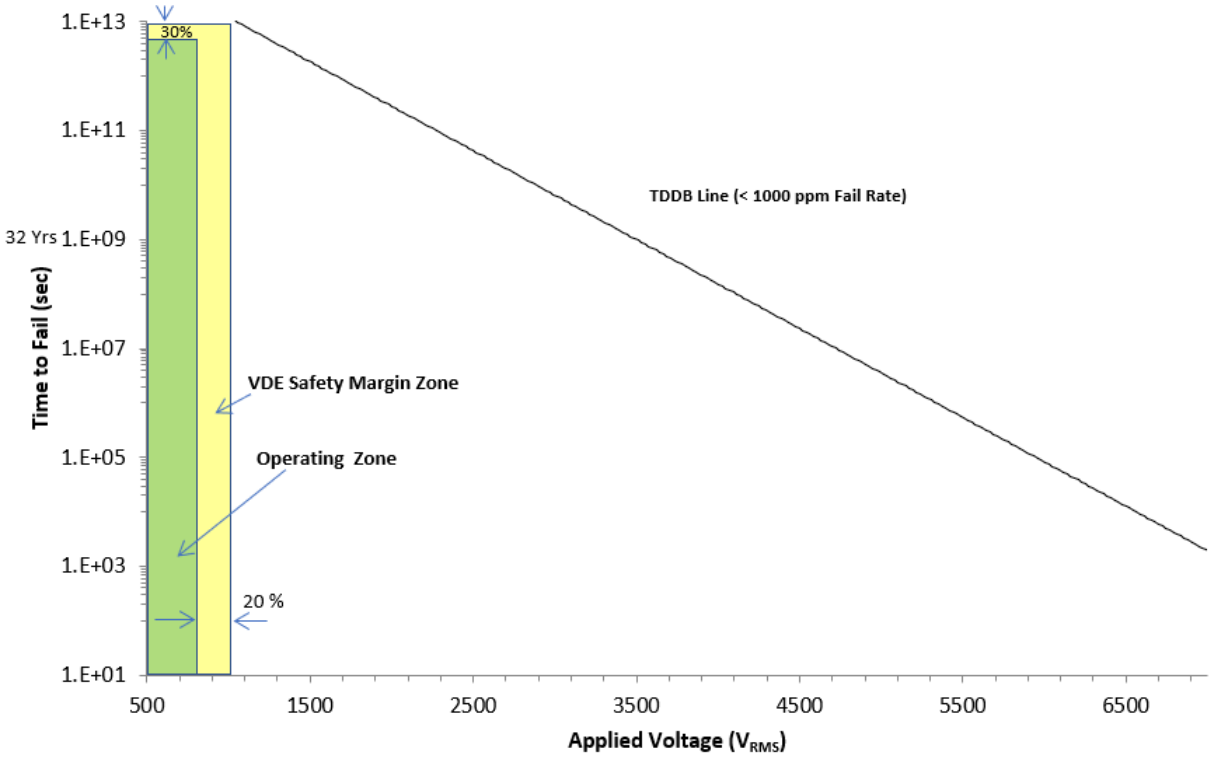

Figure 5-3. Basic Isolation Capacitor Life Time Projection

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5.11 Typical Characteristics

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

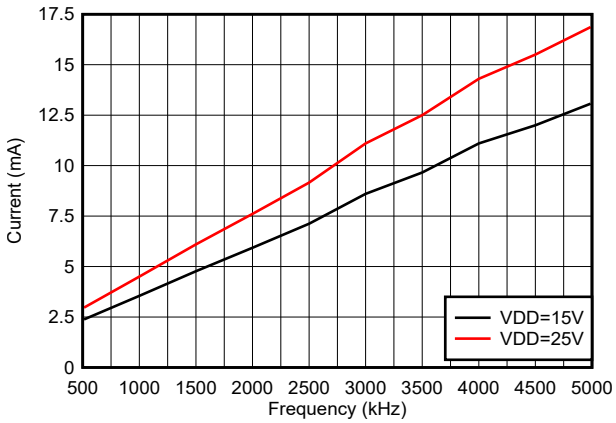

Figure 5-4. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (no load, VDD = 15V or 25V)

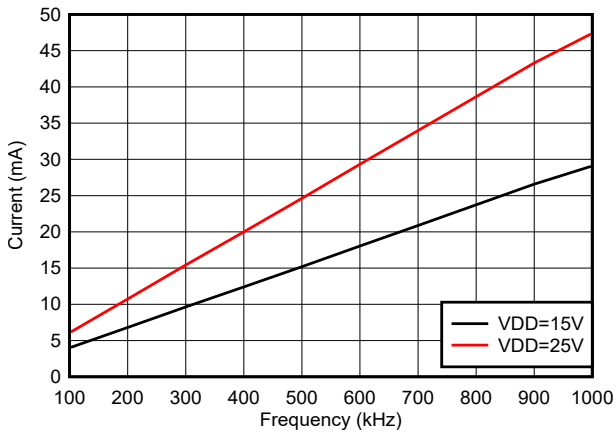

Figure 5-5. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (1-nF load, VDD = 15V or 25V)

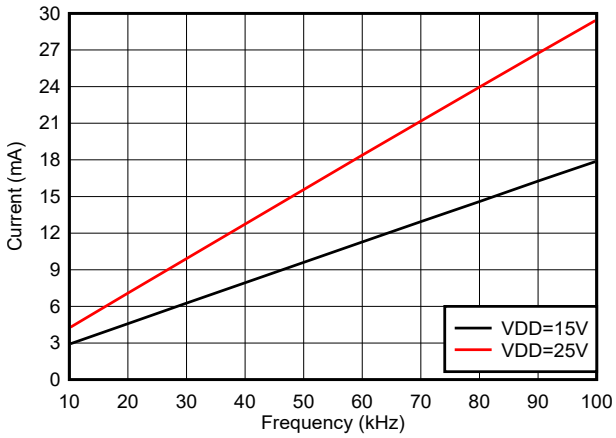

Figure 5-6. Per Channel Current Consumption ($I_{VDDA/B}$) vs Frequency (10-nF load, VDD = 15V or 25V)

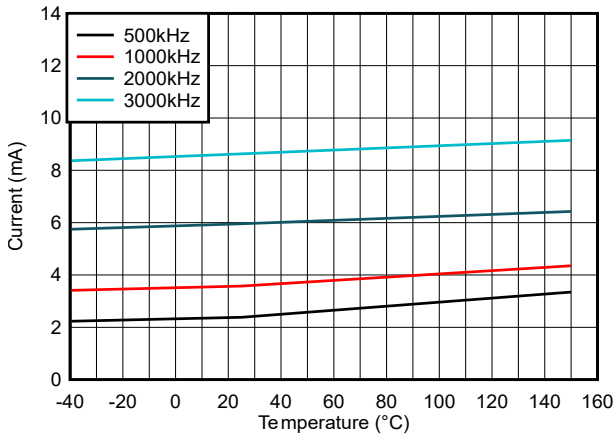

Figure 5-7. Per Channel ($I_{VDDA/B}$) Supply Current vs Temperature (no load, different switching frequencies)

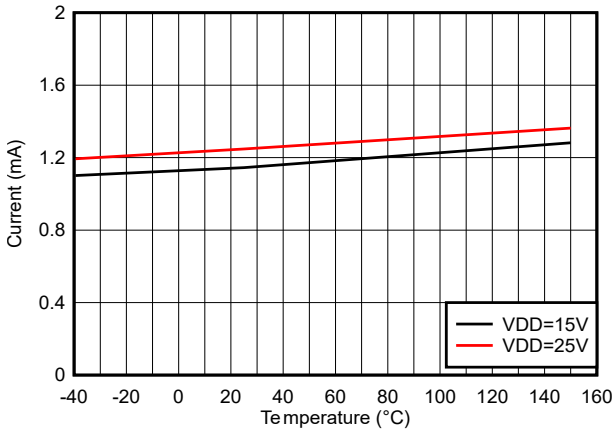

Figure 5-8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature (no load, input low, no switching)

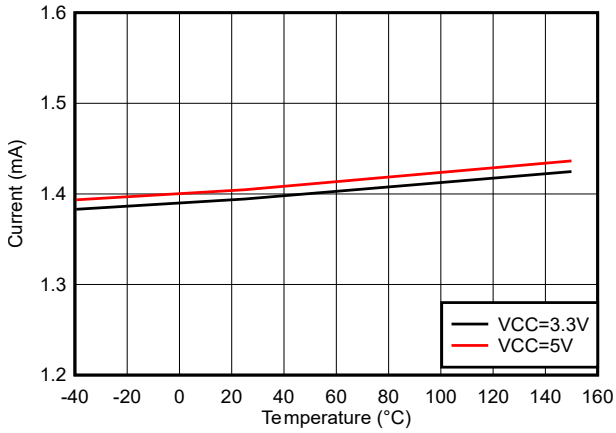

Figure 5-9. I_{VCCI} Quiescent Supply Current vs Temperature (no load, input low, no switching)

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5.11 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

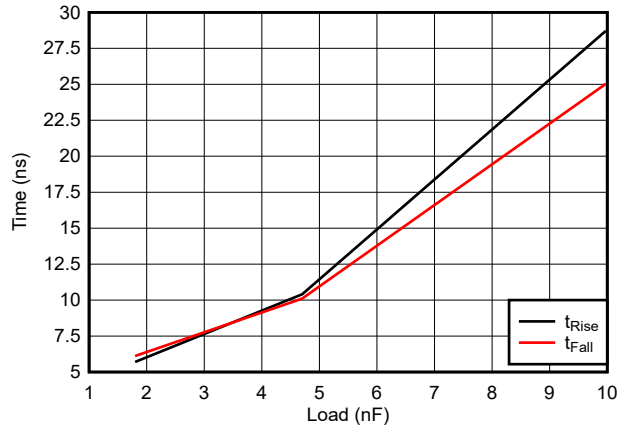

Figure 5-10. Rising and Falling Times vs Load (VDD = 15V)

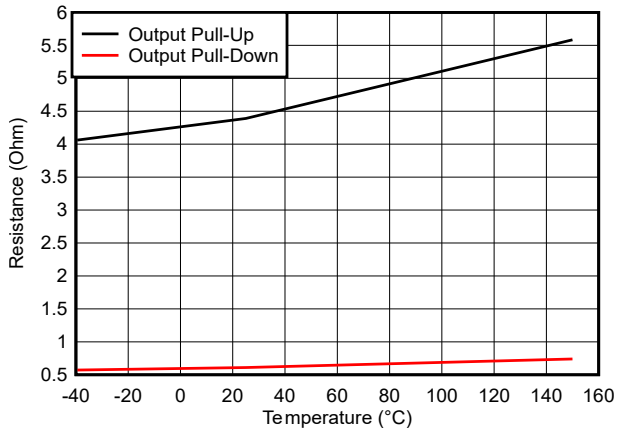

Figure 5-11. Output Resistance vs Temperature

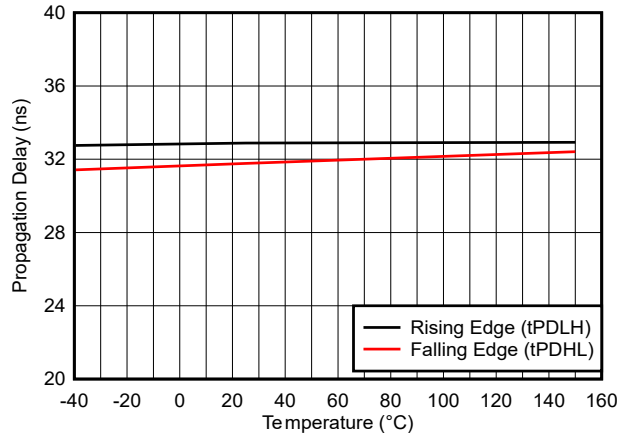

Figure 5-12. Propagation Delay vs Temperature

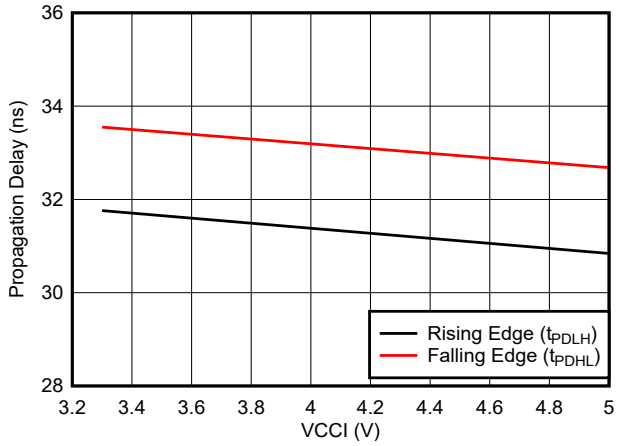

Figure 5-13. Propagation Delay vs VCCI

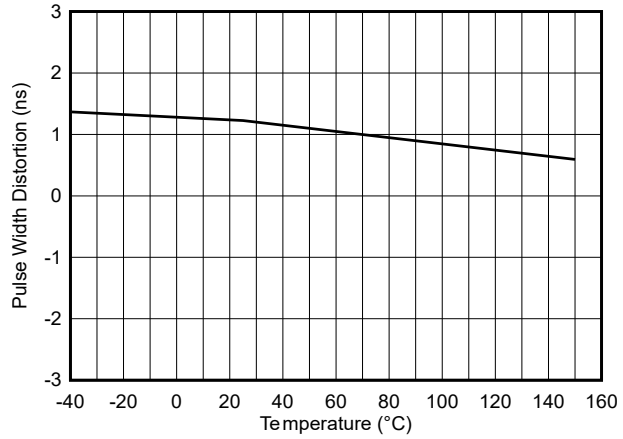

Figure 5-14. Pulse Width Distortion vs Temperature

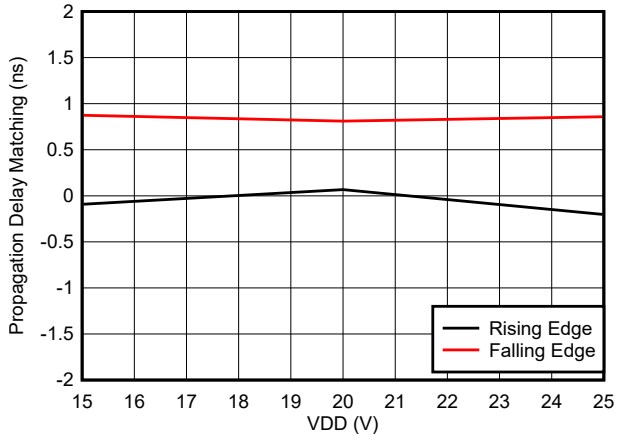

Figure 5-15. Propagation Delay Matching (t_{DM}) vs VDD

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5.11 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

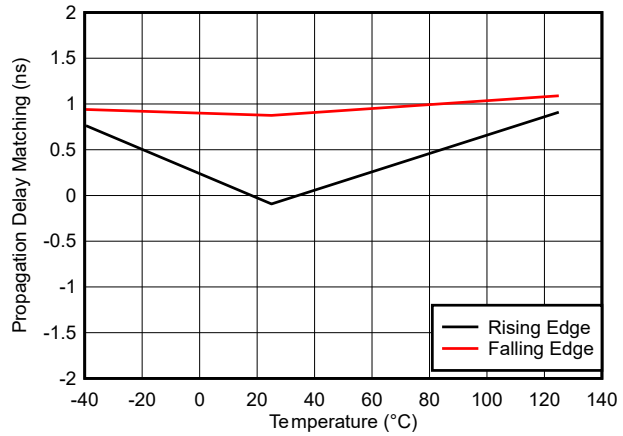

Figure 5-16. Propagation Delay Matching (t_{DM}) vs Temperature

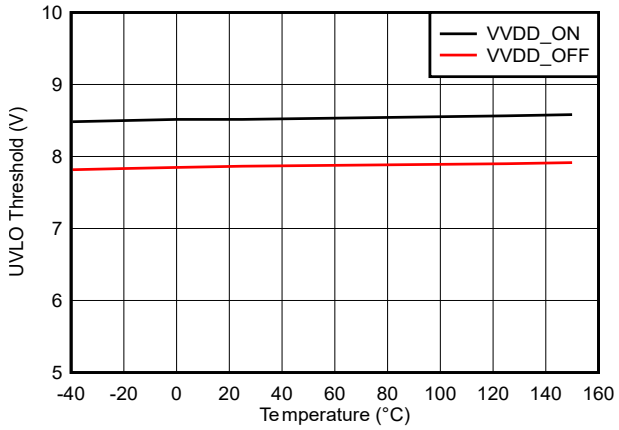

Figure 5-17. VDD 8-V UVLO Threshold vs Temperature

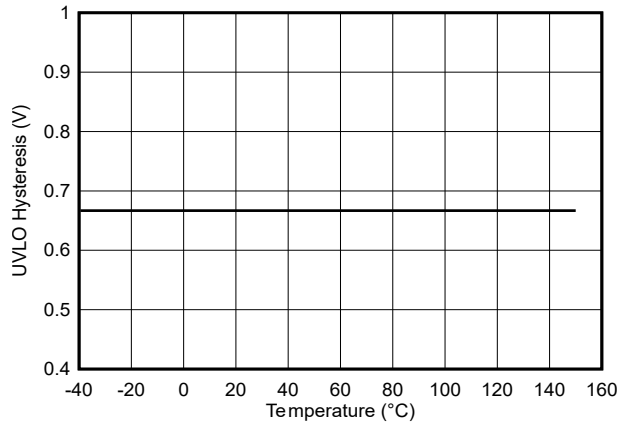

Figure 5-18. VDD 8-V UVLO Hysteresis vs Temperature

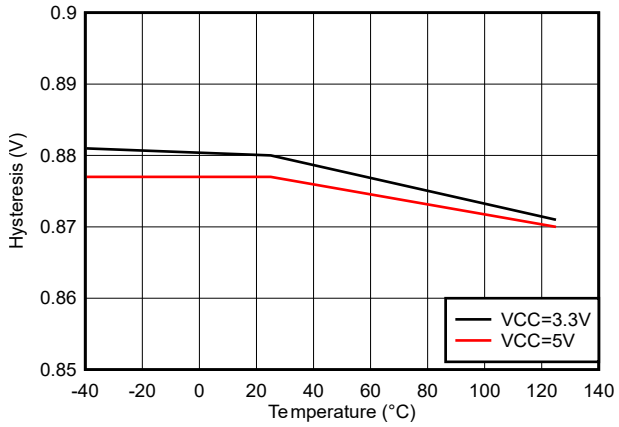

Figure 5-19. IN/DIS Hysteresis vs Temperature

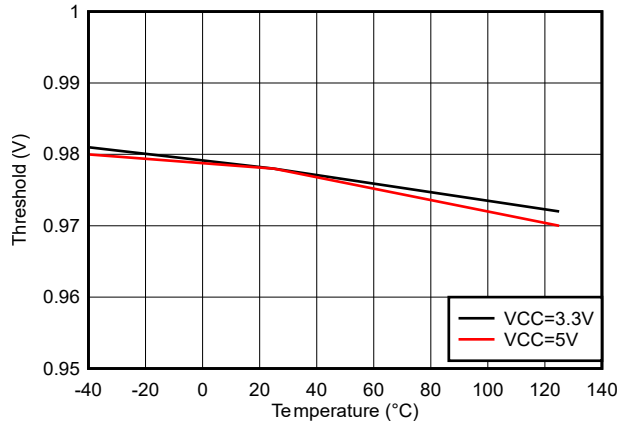

Figure 5-20. IN/DIS Low Threshold

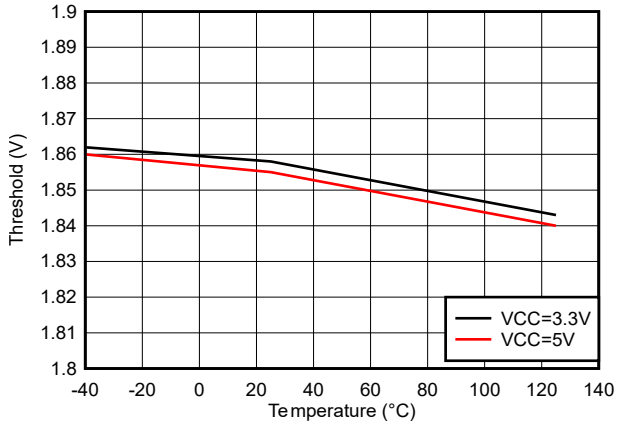

Figure 5-21. IN/DIS High Threshold

5.11 Typical Characteristics (continued)

VDDA = VDDB= 15 V, VCCI = 3.3 V, T_A = 25°C, No load unless otherwise noted.

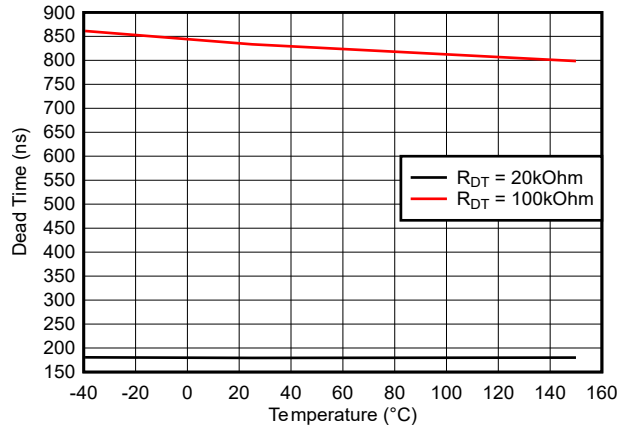

Figure 5-22. Dead Time vs Temperature (with R_{DT} = 20kΩ and 100kΩ)

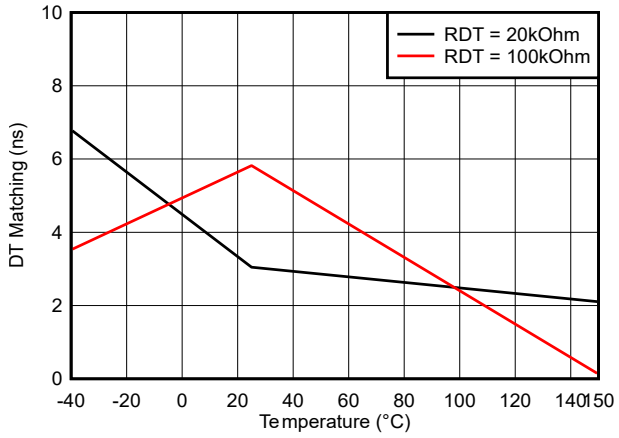

Figure 5-23. Dead Time Matching vs Temperature (with R_{DT} = 20kΩ and 100kΩ)

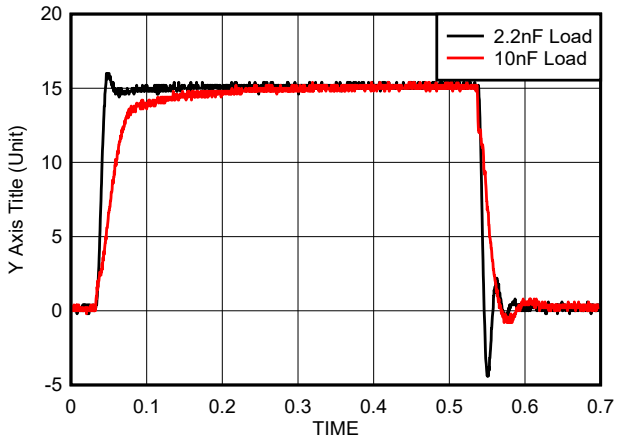

Figure 5-24. Typical Output Waveforms

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6 Parameter Measurement Information

6.1 Propagation Delay and Pulse Width Distortion

Figure 6-1 shows how one calculates pulse width distortion (t_{PWD}) and delay matching (t_{DM}) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase and disabling the dead time function by shorting the DT Pin to VCC.

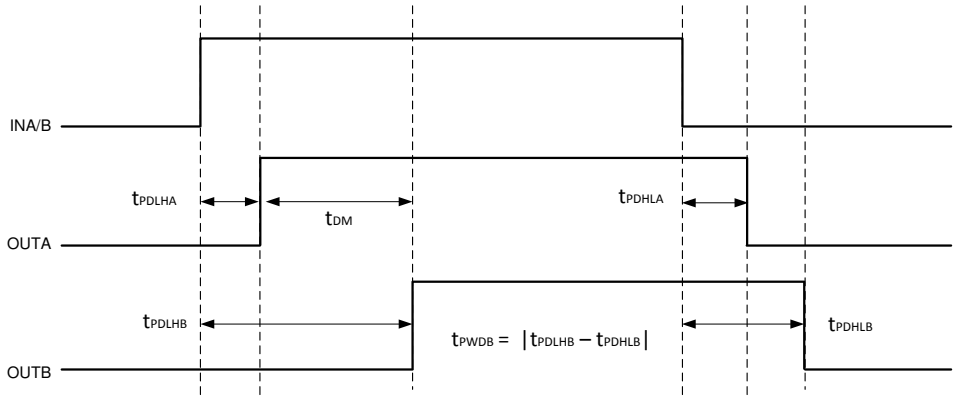

Figure 6-1. Overlapping Inputs, Dead Time Disabled

6.2 Rising and Falling Time

Figure 6-2 shows the criteria for measuring rising (t_{RISE}) and falling (t_{FALL}) times. For more information on how short rising and falling times are achieved see Section 7.3.4.

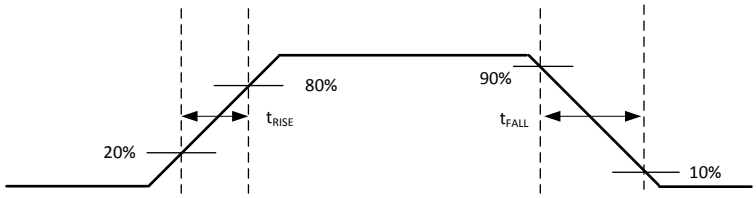

Figure 6-2. Rising and Falling Time Criteria

6.3 Input and Disable Response Time

Figure 6-3 shows the response time of the disable function. It is recommended to bypass using a ≈1nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance. For more information, see Section 7.4.1.

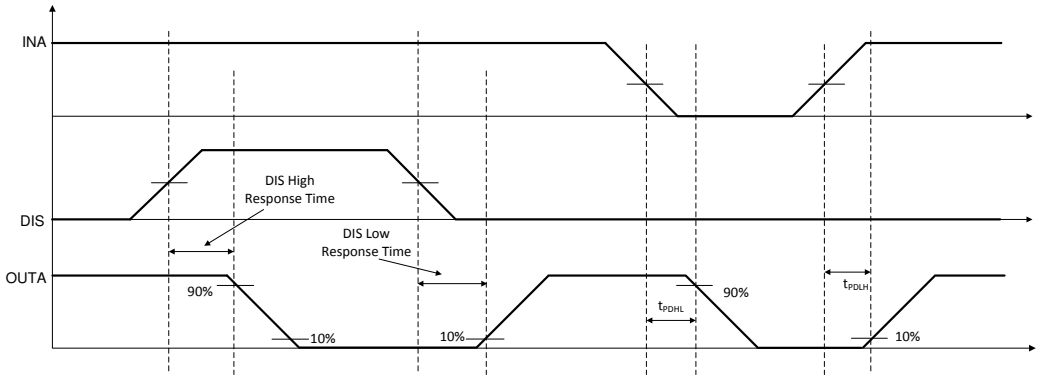

Figure 6-3. Disable Pin Timing

6.4 Programmable Dead Time

Connecting the DT pin to GND through an appropriate resistor (R_{DT}) sets a dead-time interval. For more details on dead time, refer to Section 7.4.2.

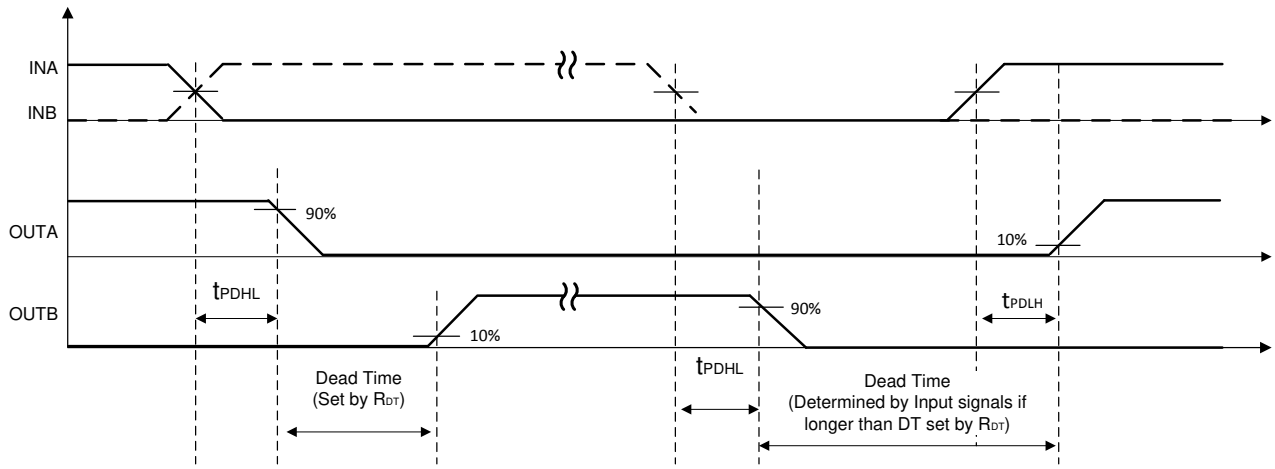

Figure 6-4. Dead-Time Switching Parameters

6.5 Power-up UVLO Delay to OUTPUT

Before the driver is ready to deliver a proper output state, there is a power-up delay from the UVLO rising edge to output and it is defined as $t_{VCCI+\ to\ OUT}$ for VCCI UVLO (typically 40us) and $t_{VDD+\ to\ OUT}$ for VDD UVLO (typically 5us). It is recommended to consider proper margin before launching PWM signal after the driver's VCCI and VDD bias supply is ready. Figure 6-5 and Figure 6-6 show the power-up UVLO delay timing diagram for VCCI and VDD.

If INA or INB are active before VCCI or VDD have crossed above their respective on thresholds, the output will not update until $t_{VCCI+\ to\ OUT}$ or $t_{VDDx+\ to\ OUT}$ after VCCI or VDD crossing its UVLO rising threshold. However, when either VCCI or VDD receive a voltage less than their respective off thresholds, there is <2µs delay, depending on the voltage slew rate on the supply pins, before the outputs are held low. This asymmetric delay is designed to ensure safe operation during VCCI or VDD brownouts.

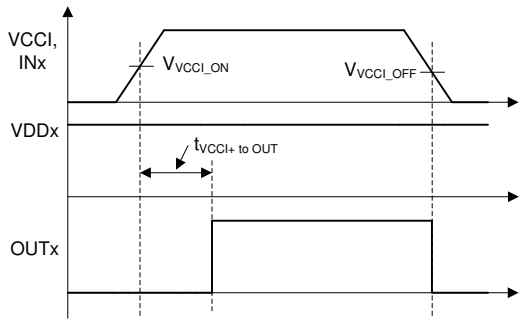

Figure 6-5. VCCI Power-up UVLO Delay

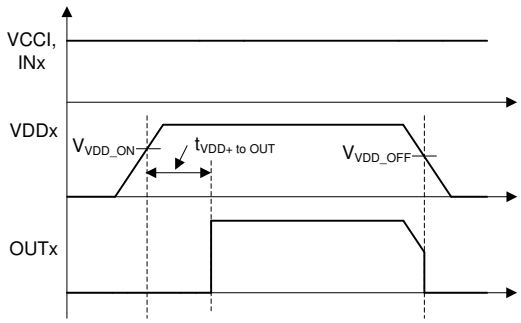

Figure 6-6. VDDA/B Power-up UVLO Delay

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6.6 CMTI Testing

Figure 6-7 is a simplified diagram of the CMTI testing configuration.

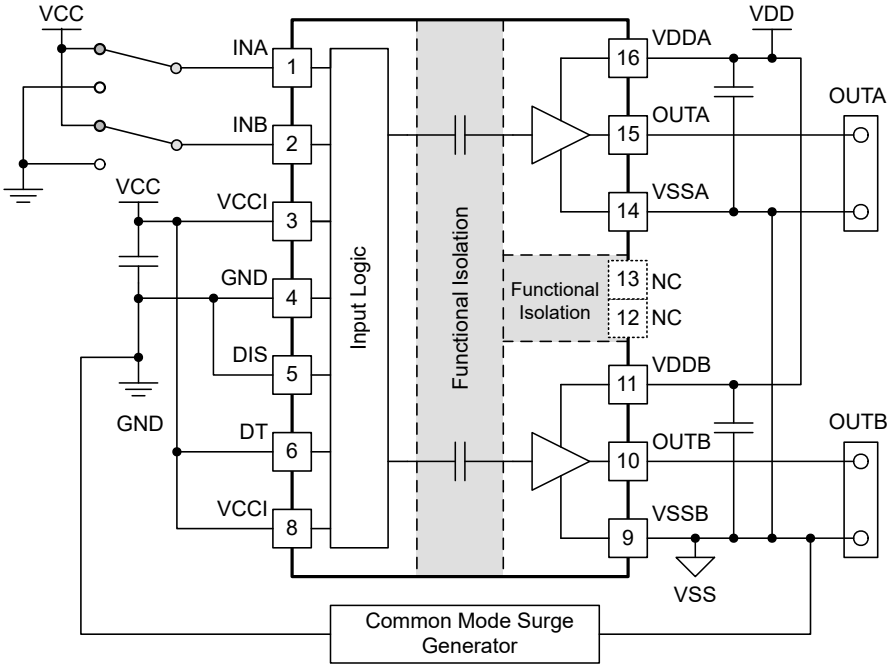


Figure 6-7. Simplified CMTI Testing Setup

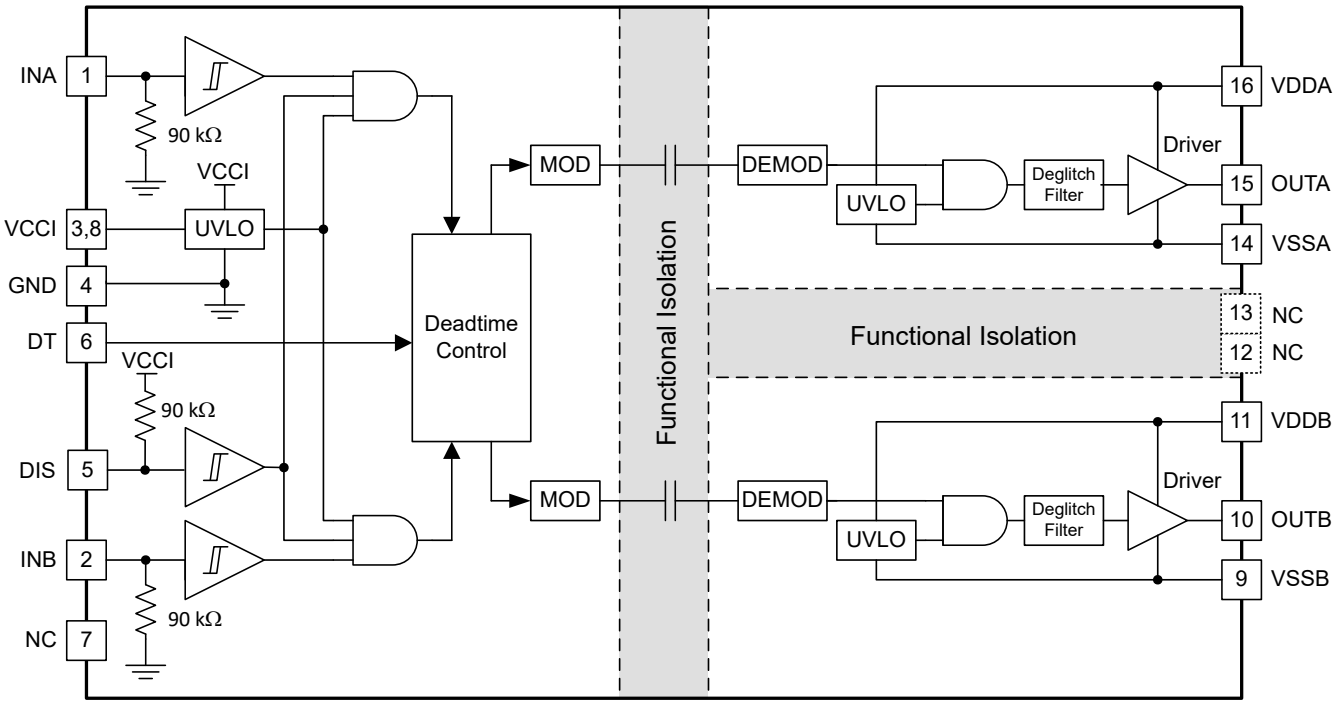
7 Detailed Description

7.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21222 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. The device has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor-programmable dead time (DT) control, a DIS pin that is internally pulled up, and under voltage lock out (UVLO) for both input and output voltages. The UCC21222 also hold its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 VDD, VCCI, and Undervoltage Lock Out (UVLO)

The UCC21222 has an internal undervoltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than V_{VDD_ON} at device start-up or lower than V_{VDD_OFF} after start-up, the VDD UVLO feature holds the affected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in Figure 7-1). In this condition, the upper PMOS is resistively held off by $R_{Hi\text{-}Z}$ while the lower NMOS gate is tied to the driver output through R_{CLAMP}. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically around 1.5 V, when no bias power is available.

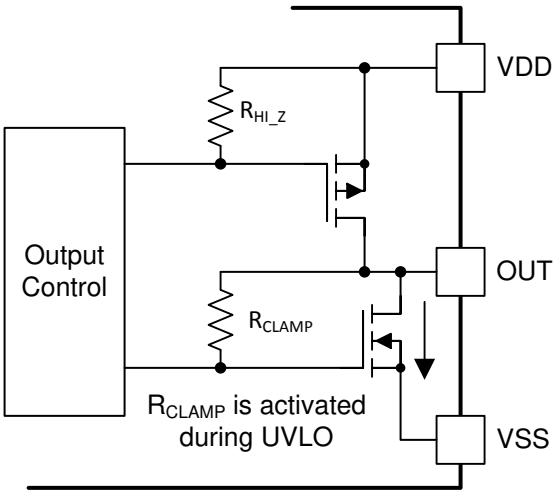

Figure 7-1. Simplified Representation of Active Pulldown Feature

The VDD UVLO protection has a hysteresis feature (V_{VDD_HYS}). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21222 also has an internal undervoltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed V_{VCCI_ON} on start up. And a signal will cease to be delivered when that pin receives a voltage less than V_{VCCI_OFF}. And, just like the UVLO for VDD, there is hysteresis (V_{VCCI_HYS}) to ensure stable operation.

All versions of the UCC21222 can withstand an absolute maximum of 30 V for VDD, and 5.5 V for VCCI.

Table 7-1. UCC21222 VCCI UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VCCI-GND < V_{VCCI_ON} during device start up	H	L	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	H	H	L	L
VCCI-GND < V_{VCCI_ON} during device start up	L	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	L	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	H	H	L	L
VCCI-GND < V_{VCCI_OFF} after device start up	L	L	L	L

Table 7-2. UCC21222 VDD UVLO Feature Logic

CONDITION	INPUTS		OUTPUTS	
	INA	INB	OUTA	OUTB
VDD-VSS < V_{VDD_ON} during device start up	H	L	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	H	H	L	L
VDD-VSS < V_{VDD_ON} during device start up	L	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	L	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	H	H	L	L
VDD-VSS < V_{VDD_OFF} after device start up	L	L	L	L

7.3.2 Input and Output Logic Table

Table 7-3. Input/Output Logic Table

Assume VCCI, VDDA, VDDB are powered up. See Section 7.3.1 for more information on UVLO operation modes.

INPUTS(1)		DIS	OUTPUTS		NOTE
INA	INB		OUTA	OUTB	
L	L	L	L	L	If Dead Time function is used, output transitions occur after the dead time expires. See Section 7.4.2
L	H	L	L	H	
H	L	L	H	L	
H	H	L	L	L	
H	H	L	H	H	DT pin left open or tied to VCCI
Left Open	Left Open	L	L	L	-
X	X	H or Left Open	L	L	-

(1) "X" means L, H or left open.

7.3.3 Input Stage

The input pins (INA, INB, and DIS) of the UCC21222 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V micro-controllers), since the UCC21222 has typical high threshold (V_{INAH}) of 2.0 V and a typical low threshold of 1 V. A wide hysterisis (V_{INA_HYS}) of 1 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 90 kΩ (see Section 7.2). However, it is still recommended to ground an input if it is not being used.

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Since the input side of the UCC21222 is isolated from the output drivers, this allows the user to choose the most efficient VDD for their chosen gate. The amplitude of any signal applied to INA or INB should *never* be at a voltage higher than VCCI.

7.3.4 Output Stage

The UCC21222 output stages feature a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high.

The R_{OH} parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. This N-channel device has an on-resistance of approximately 1.47 Ω. Therefore, the effective resistance of the UCC21222 pull-up stage during this brief turn-on phase is the parallel resistance between the pull-up NMOS and pull-up PMOS, which is 1.47Ω // 5Ω, much lower than what is represented by the R_{OH} parameter. The value of R_{OH} belies the fast nature of the UCC21222 turn-on time.

The pull-down structure in the UCC21222 is simply composed of an N-channel MOSFET. The R_{OL} parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21222 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

To ensure robust and reliable operation of gate drivers, pay special attention to the minimum pulse width. The minimum pulse width shown in the electrical characteristics table describes the minimum input pulse that would be passed to the output in an unloaded driver. This is dictated by the deglitch filter present in the driver IC. An input ON or OFF pulse width longer than the maximum specification is needed to guarantee an output state change and avoid potential shoot-through. With a loaded driver, extra precaution must be taken to ensure robust operation of the system. During gate switching, if the output state changes before the driver completes each transition, a non-zero current switching event occurs. Combined with layout parasitics, non-zero current switching can cause internal rail overshoot and EOS damage of the gate driver. Thus, a minimum output width is needed for reliable system operation. This minimum output pulse width is dependent on several factors: gate capacitance, VDD supply voltage, gate resistance, and PCB layout parasitics. The minimum pulse width for robust operation might be magnitudes larger than the minimum pulse width shown in the electrical characteristics table. System-level study should be carried out to determine the minimum output pulse width required for each system.

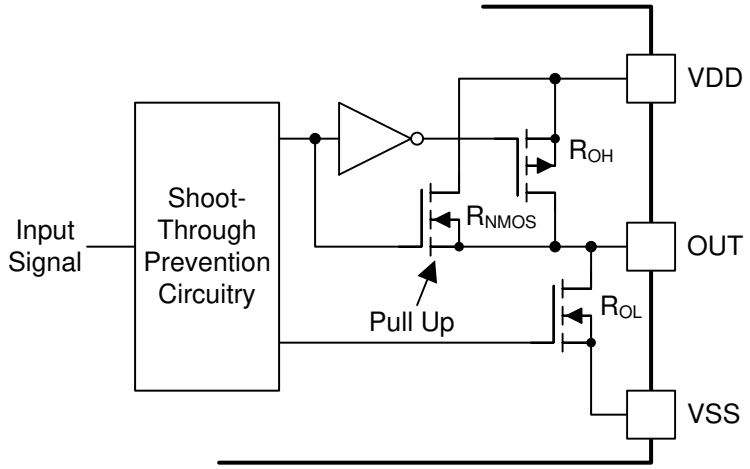

Figure 7-2. Output Stage

7.3.5 Diode Structure in the UCC21222

Figure 7-3 illustrates the multiple diodes involved in the ESD protection components of the UCC21222. This provides a pictorial representation of the absolute maximum rating for the device.

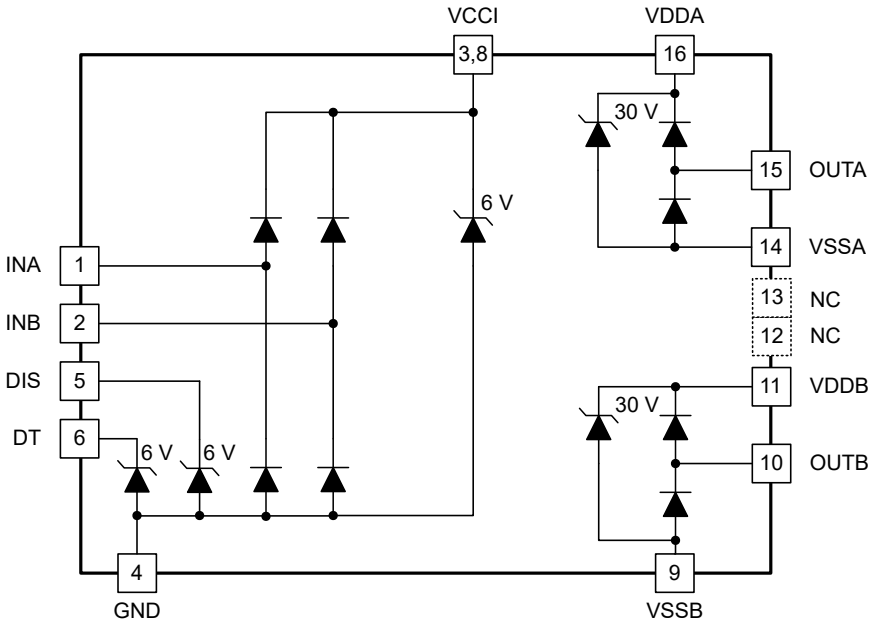

Figure 7-3. ESD Structure

7.4 Device Functional Modes

7.4.1 Disable Pin

Setting the DIS pin high (or left open) shuts down both outputs simultaneously. Grounding the DIS pin allows the UCC21222 to operate normally. The DIS response time is in the range of 48 ns and quite responsive, which is as fast as propagation delay. The DIS pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is recommended to tie this pin to ground if the DIS pin is not used to achieve better noise immunity, and it is recommended to bypass using a ≈1-nF low ESR/ESL capacitor close to DIS pin when connecting DIS pin to a micro controller with distance.

7.4.2 Programmable Dead-Time (DT) Pin

The UCC21222 allows the user to adjust dead time (DT) in the following ways:

7.4.2.1 Tying the DT Pin to VCC

Outputs completely match inputs, so no dead time is asserted. This allows outputs to overlap.

7.4.2.2 DT Pin Connected to a Programming Resistor Between DT and GND Pins

Program t_{DT} by placing a resistor, R_{DT}, between the DT pin and GND. The appropriate R_{DT} value can be determined, where R_{DT} is in kΩ and t_{DT} is in ns:

$$t_{DT} \approx 8.6 \times R_{DT} + 13 \quad (1)$$

The equation above is true when R_{DT} is in the range of 1.7 kΩ to 100 kΩ. It is not recommended to use a R_{DT} with value greater than 100 kΩ.

An input signal's falling edge activates the programmed dead time for the other signal. The output signals' dead time is always set to the longer of either the driver's programmed dead time or the input signal's own dead time. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent

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shoot-through, and it does not affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in Figure 7-4:

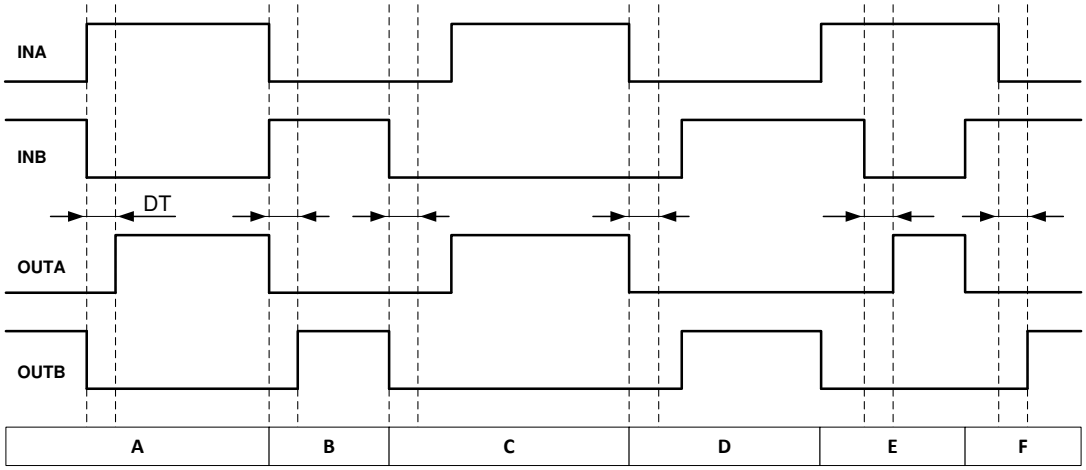

Figure 7-4. Input and Output Logic Relationship With Input Signals

Condition A: INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

Condition B: INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

Condition C: INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal's *own* dead time is longer than the programmed dead time. Thus, when INA goes high, it immediately sets OUTA high.

Condition D: INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. INB's *own* dead time is longer than the programmed dead time. Thus, when INB goes high, it immediately sets OUTB high.

Condition E: INA goes high, while INB and OUTB are still high. To avoid overshoot, INA immediately pulls OUTB low and keeps OUTA low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

Condition F: INB goes high, while INA and OUTA are still high. To avoid overshoot, INB immediately pulls OUTA low and keeps OUTB low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC21222 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21222 (with up to 5.5-V VCCI and 25-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and disable) and optimized switching performance; the UCC21222 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

8.2 Typical Application

The circuit in Figure 8-1 shows a reference design with the UCC21222 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications.

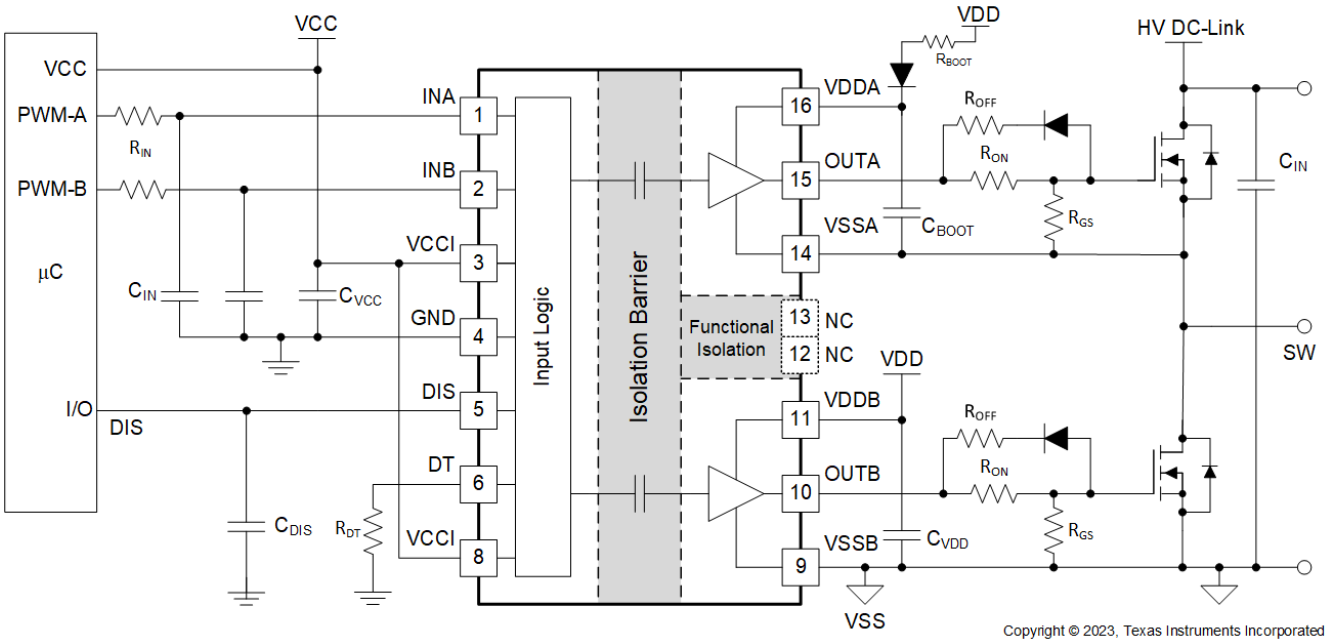

Figure 8-1. Typical Application Schematic

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8.2.1 Design Requirements

Table 8-1 lists reference design parameters for the example application: UCC21222 driving 1200-V SiC-MOSFETs in a high side-low side configuration.

Table 8-1. UCC21222 Design Requirements

PARAMETER	VALUE	UNITS
Power transistor	C2M0080120D	-
VCC	5.0	V
VDD	20	V
Input signal amplitude	3.3	V
Switching frequency (f_s)	100	kHz
DC link voltage	800	V

8.2.2 Detailed Design Procedure

8.2.2.1 Designing INA/INB Input Filter

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input R_{IN}-C_{IN} filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an R_{IN} in the range of 0 Ω to100 Ω and a C_{IN} between 10 pF and 100 pF. In the example, an R_{IN} = 51 Ω and a C_{IN} = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

8.2.2.2 Select External Bootstrap Diode and its Series Resistor

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode's forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

When selecting external bootstrap diodes, it is recommended that one chose high voltage, fast recovery diodes or SiC Schottky diodes with a low forward voltage drop and low junction capacitance in order to minimize the loss introduced by reverse recovery and related grounding noise bouncing. In the example, the DC-link voltage is 800 V_{DC}. The voltage rating of the bootstrap diode should be higher than the DC-link voltage with a good margin. Therefore, a 1200-V SiC diode, C4D02120E, is chosen in this example.

When designing a bootstrap supply, it is recommended to use a bootstrap resistor, R_{BOOT}. A bootstrap resistor, is also used to reduce the inrush current in D_{BOOT} and limit the ramp up slew rate of voltage of VDDA-VSSA during each switching cycle.

Failure to limit the voltage to VDDx-VSSx to less than the Absolute Maximum Ratings of the FET and UCC21222 may result in permanent damage to the device in certain cases.

The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used. In the example, a current limiting resistor of 2.2 Ω is selected to limit the inrush current of bootstrap diode. The estimated worst case peak current through D_{Boot} is,

$$I_{DBoot(pk)} = \frac{V_{DD} - V_{BDF}}{R_{Boot}} = \frac{20V - 2.5V}{2.2\Omega} \approx 8A \tag{2}$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop at 8 A.

8.2.2.3 Gate Driver Output Resistor

The external gate driver resistors, R_{ON}/R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, for example peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in Section 7.3.4, the UCC21222 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{OA+} = \min\left(4A, \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}}\right) \tag{3}$$

$$I_{OB+} = \min\left(4A, \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}}\right) \tag{4}$$

where

- V_{BDF} is the estimated bootstrap diode forward voltage drop at 8 A.
- R_{ON}: External turn-on resistance.
- R_{GFET_INT}: Power transistor internal gate resistance, found in the power transistor datasheet.
- I_{O+} = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{OA+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}} = \frac{20V - 0.8V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.4A \tag{5}$$

$$I_{OB+} = \frac{V_{DD}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET_Int}} = \frac{20V}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.6\Omega} \approx 2.5A \tag{6}$$

Therefore, the high-side and low-side peak source current is 2.4 A and 2.5 A respectively. Similarly, the peak sink current can be calculated with:

$$I_{OA-} = \min\left(6A, \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}}\right) \tag{7}$$

$$I_{OB-} = \min\left(6A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}}\right) \tag{8}$$

where

- R_{OFF}: External turn-off resistance;
- V_{GDF}: The anti-parallel diode forward voltage drop which is in series with R_{OFF}. The diode in this example is an MSS1P4.
- I_{O-}: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

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In this example,

$$I_{OA-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} = \frac{20V - 0.8V - 0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.6A \tag{9}$$

$$I_{OB-=} \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} = \frac{20V\text{-}0.75V}{0.55\Omega + 0\Omega + 4.6\Omega} \approx 3.7A \tag{10}$$

Therefore, the high-side and low-side peak sink current is 3.6 A and 3.7 A respectively.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

Failure to control OUTx voltage to less than the Absolute Maximum Ratings in the datasheet (including transients) may result in permanent damage to the device in certain cases. To reduce excessive gate ringing, it is recommended to use a ferrite bead near the gate of the FET. External clamping diodes can also be added in the case of extended overshoot/undershoot, in order to clamp the OUTx voltage to the VDDx and VSSx voltages.

8.2.2.4 Gate to Source Resistor Selection

A gate to source resistor, R_{GS}, is recommended to pull down the gate to the source voltage when the gate driver output is unpowered and in an indeterminate state. This resistor also helps to mitigate the risk of dv/dt induced turn-on due to Miller current before the gate driver is able to turn on and actively pull low. This resistor is typically sized between 5.1 kΩ and 20 kΩ, depending on the Vth and ratio of C_{GD} to C_{GS} of the power device.

8.2.2.5 Estimate Gate Driver Power Loss

The total loss, P_G, in the gate driver subsystem includes the power losses of the UCC21222 (P_{GD}) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in P_G and not discussed in this section.

P_{GD} is the key power loss which determines the thermal safety-related limits of the UCC21222, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. P_{GDQ} is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. In this example, V_{VCCI} = 5 V and V_{VDD} = 20 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be I_{VCCI} = 2.5 mA, and I_{VDDA} = I_{VDDB} = 2.5 mA. Therefore, the P_{GDQ} can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{VDDB} \times I_{DDB} = 112.5mW \tag{11}$$

The second component is switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, P_{GSW}, can be estimated with

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times f_{SW} \tag{12}$$

where

- Q_G is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 20V \times 60nC \times 100kHz = 240mW \tag{13}$$

Q_G represents the total gate charge of the power transistor switching 800 V at 20 A, and is subject to change with different testing conditions. The UCC21222 gate driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} will be equal to P_{GSW} if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21222. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \times \left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET_Int}} \right) \tag{14}$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21222 gate driver loss can be estimated with:

$$P_{GDO} = \frac{240mW}{2} \times \left(\frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 4.6\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 4.6\Omega)} \right) \approx 30mW \tag{15}$$

Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = 2 \times f_{SW} \times \left[4A \times \int_0^{T_{R_Sys}} \left(V_{DD} - V_{OUTA/B}(t) \right) dt + 6A \times \int_0^{T_{F_Sys}} V_{OUTA/B}(t) dt \right] \tag{16}$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the P_{GDO} will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21222, P_{GD}, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \tag{17}$$

which is equal to 142.5 mW in the design example.

8.2.2.6 Estimating Junction Temperature

The junction temperature (T_J) of the UCC21222 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD} \tag{18}$$

where

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- T_C is the UCC21222 case-top temperature measured with a thermocouple or some other instrument, and
- Ψ_{JT} is the Junction-to-top characterization parameter

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. Ψ_{JT} is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

8.2.2.7 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 V_{DC} is applied.

8.2.2.7.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

8.2.2.7.2 Selecting a VDDA (Bootstrap) Capacitor

A VDDA capacitor, also referred to as a *bootstrap capacitor* in bootstrap power supply configurations, allows for gate drive current transients up to 6 A, and needs to maintain a stable gate drive voltage for the power transistor.

The total charge needed per switching cycle can be estimated with

$$Q_{Total} = Q_G + \frac{I_{VDD}}{f_{sw}} = 60nC + \frac{2.5mA}{100kHz} = 85nC \tag{19}$$

where

- Q_{Total}: Total charge needed
- Q_G: Gate charge of the power transistor.
- I_{VDD}: The channel self-current consumption with no load at 100 kHz.
- f_{SW}: The switching frequency of the gate driver

Therefore, the absolute minimum C_{Boot} requirement is:

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{VDDA}} = \frac{85nC}{0.5V} = 170nF \tag{20}$$

where

- ΔV_{VDDA} is the voltage ripple at VDDA, which is 0.5 V in this example.

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V 1-µF capacitor is chosen in this example.

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$$C_{Boot} = 1\mu F \tag{21}$$

Care should be taken when selecting the bootstrap capacitor to ensure that the VDD to VSS voltage does not drop below the recommended minimum operating level listed in the Recommended Operating Conditions section. The value of the bootstrap capacitor should be sized such that it can supply the initial charge to switch the power device, and then continuously supply the gate driver quiescent current for the duration of the high-side on-time.

If the high-side supply voltage drops below the UVLO falling threshold, the high-side gate driver output will turn off and switch the power device off. Uncontrolled hard-switching of power devices can cause high di/dt and high dv/dt transients on the output of the driver and may result in permanent damage to the device.

To further lower the AC impedance for a wide frequency range, it is recommended to have bypass capacitor placed very close to VDDx - VSSx pins with a low ESL/ESR. In this example a 100-nF, X7R ceramic capacitor, is placed in parallel with C_{Boot} to optimize the transient performance.

Note

Too large C_{BOOT} is not always good. C_{BOOT} may not be charged within the first few cycles and V_{BOOT} could stay below UVLO. As a result, the high-side FET does not follow input signal command. Also during initial C_{BOOT} charging cycles, the bootstrap diode has highest reverse recovery current and losses.

8.2.2.7.3 Select a VDDB Capacitor

Chanel B has the same current requirements as Channel A, Therefore, a VDDB capacitor (shown as C_{VDD} in Figure 8-1) is needed. In this example with a bootstrap configuration, the VDDB capacitor will also supply current for VDDA through the bootstrap diode. A 50-V, 10-µF MLCC and a 50-V, 220-nF MLCC are chosen for C_{VDD}. If the bias power supply output is a relatively long distance from the VDDB pin, a tantalum or electrolytic capacitor, with a value over 10 µF, should be used in parallel with CVDD.

8.2.2.8 Dead Time Setting Guidelines

For power converter topologies utilizing half-bridges, the dead time setting between the top and bottom transistor is important for preventing shoot-through during dynamic switching.

The UCC21222 dead time specification in the electrical table is defined as the time interval from 90% of one channel's falling edge to 10% of the other channel's rising edge (see Figure 6-4). This definition ensures that the dead time setting is independent of the load condition, and ensures linearity through manufacture testing. However, this dead time setting may not reflect the dead time in the power converter system, since the dead time setting is dependent on the external gate drive turn-on/off resistor, DC-Link switching voltage/current, as well as the input capacitance of the load transistor.

Here is a suggestion on how to select an appropriate dead time:

$$DT_{Setting} = DT_{Req} + T_{F_Sys} + T_{R_Sys} - T_{D(on)} \tag{22}$$

where

- $DT_{setting}$: UCC21222 dead time setting in ns, $DT_{Setting}$ = 8.6 × RDT(in kΩ) + 13.
- DT_{Req}: System required dead time between the real V_{GS} signal of the top and bottom switch with enough margin, or ZVS requirement.
- T_{F_Sys}: In-system gate turn-off falling time at worst case of load, voltage/current conditions.
- T_{R_Sys}: In-system gate turn-on rising time at worst case of load, voltage/current conditions.
- $T_{D(on)}$: Turn-on delay time, from 10% of the transistor gate signal to power transistor gate threshold.

It should be noted that the UCC21222 dead time setting is decided by the DT pin configuration (see Section 7.4.2), and it cannot automatically fine-tune the dead time based on system conditions.

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8.2.2.9 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (for example, TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

Figure 8-2 shows the first example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, V_A, is equal to 25 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 25 V – 5.1 V ≈ 20 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs two power supplies for a half-bridge configuration, and there will be steady state power consumption from R_Z.

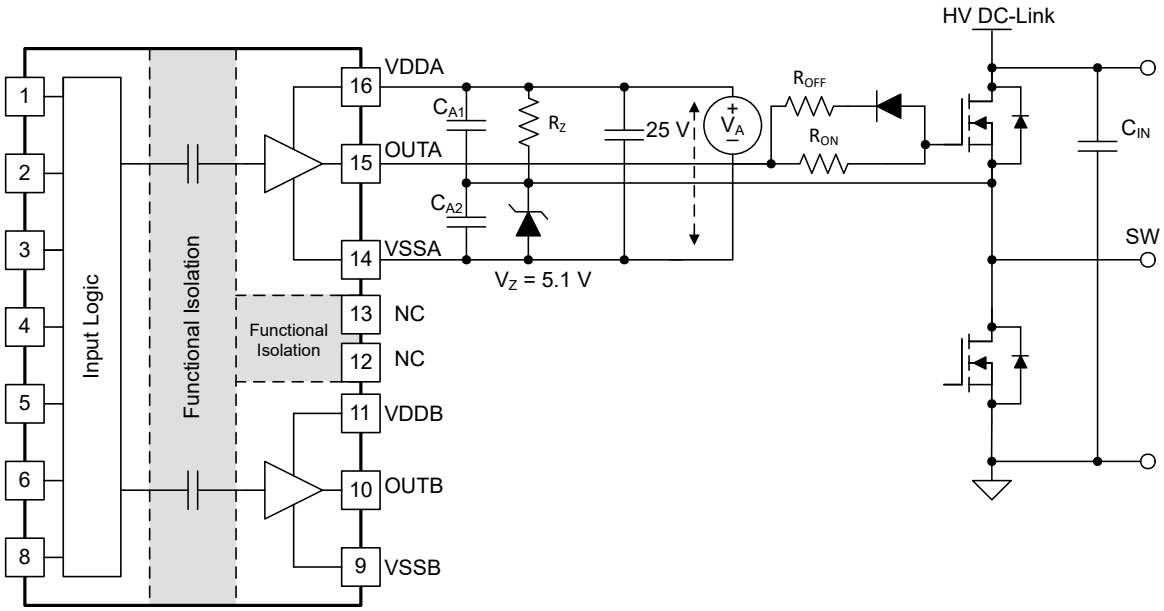

Figure 8-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output

Figure 8-3 shows another example which uses two supplies (or single-input-double-output power supply). Power supply V_{A+} determines the positive drive output voltage and V_{A-} determines the negative turn-off voltage. The configuration for channel B is the same as channel A. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

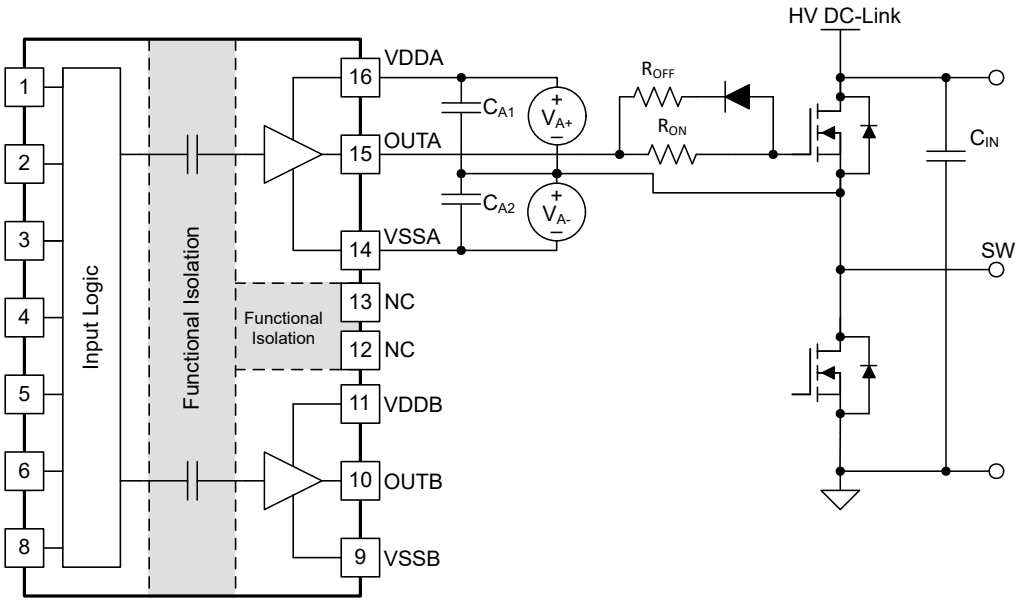

Figure 8-3. Negative Bias with Two Iso-Bias Power Supplies

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The last example, shown in Figure 8-4, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

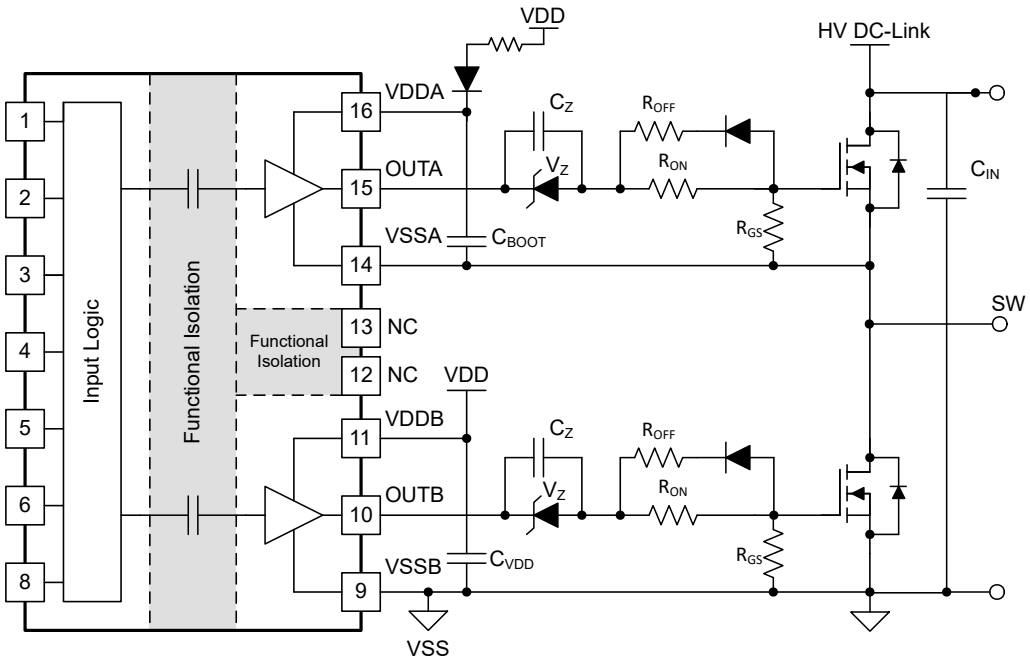

Figure 8-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

8.2.3 Application Curves

Figure 8-5 shows the bench test waveforms for the design example shown in Figure 8-1 under these conditions: VCC = 5 V, VDD = 20 V, f_{SW} = 100 kHz, $V_{DC\text{-}Link}$ = 0 V.

Channel 1 (Yellow): UCC21222 INA pin signal.

Channel 2 (Blue): UCC21222 INB pin signal.

Channel 3 (Pink): Gate-source signal on the high side power transistor.

Channel 4 (Green): Gate-source signal on the low side power transistor.

Figure 8-5. Bench Test Waveform for INA/B and OUTA/B

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9 Power Supply Recommendations

The recommended input supply voltage (VCCI) for the UCC21222 is between 2.7 V and 5.5 V. The output bias supply voltage (VDDA/VDDB) range depends on which version of the UCC21222 is being used. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. VDD or VCCI cannot fall below their respective UVLO thresholds (for more information on UVLO see Section 7.3.1). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by the UCC21222 with a recommended maximum VDDA/VDDB of 25 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested to place two such capacitors: one with a value of ≈10-µF for device biasing, and an additional ≤100-nF capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC21222, this bypass capacitor has a minimum recommended value of 100 nF.

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10 Layout

10.1 Layout Guidelines

The user must pay close attention to PCB layout in order to achieve optimum performance for the UCC21222. Below are some key points.

Component Placement:

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- It is recommended to place the dead-time setting resistor, R_{DT}, and its bypassing capacitor close to DT pin of the UCC21222.
- It is recommended to bypass using a ≈1-nF low ESR/ESL capacitor, C_{DIS}, close to DIS pin when connecting to a µC with distance.

Grounding Considerations:

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

High-Voltage Considerations:

- To ensure isolation performance between the primary and secondary side, one should avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the UCC21222's isolation performance.
- For half-bridge, or high-side/low-side configurations, where the channel A and channel B drivers could operate with a DC-link voltage up to 1500 V_{DC}, one should try to increase the creepage distance of the PCB layout between the high and low-side PCB traces.

Thermal Considerations:

- A large amount of power may be dissipated by the UCC21222 if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to Section 8.2.2.5 for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance (θ_{JB}).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see Figure 10-2 and Figure 10-3). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. However, keep in mind that there should not be any traces/coppers from different high voltage planes overlapping.

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10.2 Layout Example

Figure 10-1 shows a 2-layer PCB layout example with the signals and key components labeled.

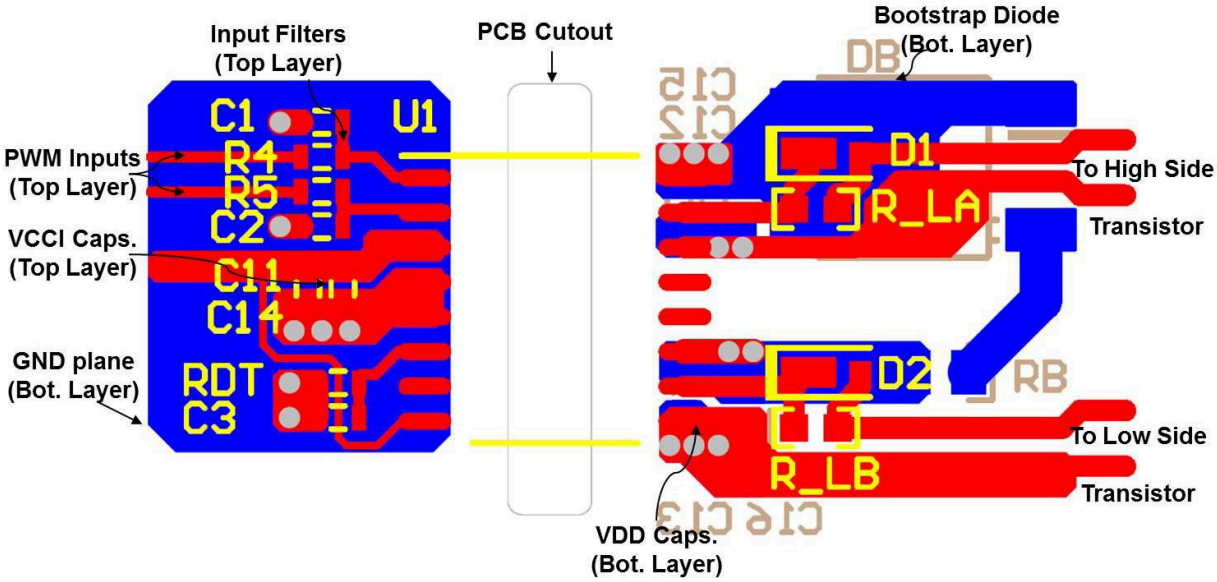

Figure 10-1. Layout Example

Figure 10-2 and Figure 10-3 shows top and bottom layer traces and copper.

Note

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

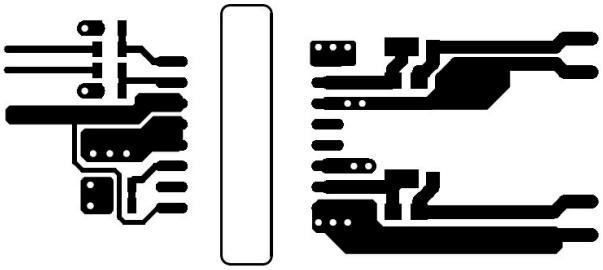

Figure 10-2. Top Layer Traces and Copper

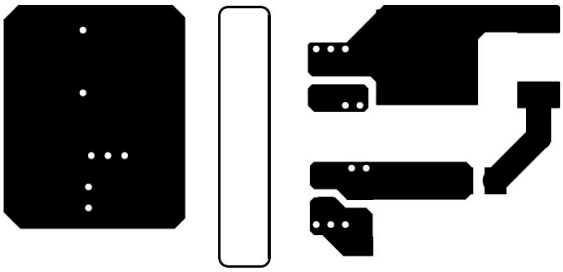

Figure 10-3. Bottom Layer Traces and Copper

Figure 10-4 and Figure 10-5 are 3D layout pictures with top view and bottom views.

Note

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

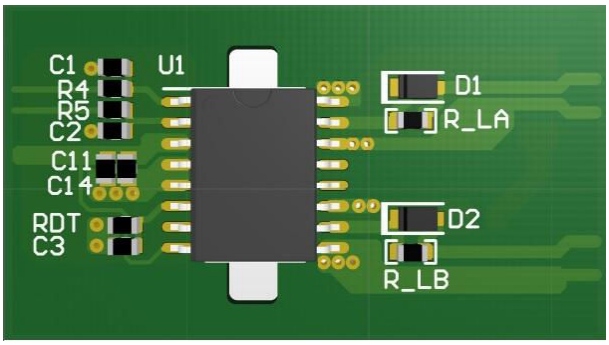

Figure 10-4. 3-D PCB Top View

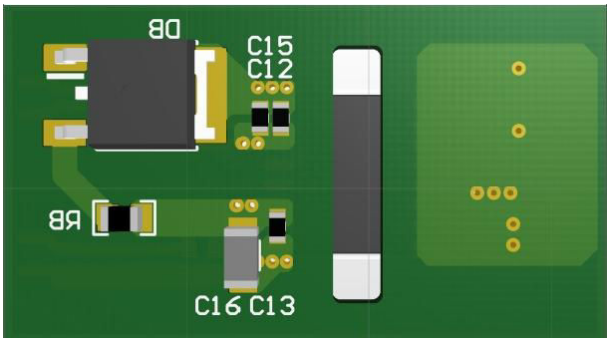

Figure 10-5. 3-D PCB Bottom View

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics Application Report*
- Isolation Glossary

11.3 Certifications

UL Online Certifications Directory, *"FPPT2.E181974 Nonoptical Isolating Devices - Component"* Certificate Number: 20160516-E181974,

VDE Pruf- und Zertifizierungsinstitut Certification, Certificate of Conformity with Factory Surveillance

CQC Online Certifications Directory, "GB4943.1-2011, Digital Isolator Certificate" Certificate Number:CQC16001155011

CSA Online Certifications Directory, "CSA Certificate of Compliance" Certificate Number:70097761, Master Contract Number:220991

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2024) to Revision C (November 2024) **Page**

- Updated Features section to reflect device characteristics.... 1
- Added junction temperature range.... 1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns.... 1
- Changed maximum VDD output drive supply from 18V to 25V.... 1
- Changed typical propagation delay from 28ns to 33ns.... 1
- Deleted bullet on maximum delay matching.... 1
- Changed maximum pulse-width distortion from 5.5ns to 5ns.... 1
- Deleted bullet on minimum pulse width.... 1
- Added maximum VDD power-up delay of 10us.... 1
- Deleted bullets on isolation barrier life and surge immunity.... 1
- Updated certification to the latest standards.... 1
- Updated applications section.... 1
- Updated description section to reflect device characteristics.... 1
- Changed CMTI from greater than 100V/ns to greater than 125V/ns.... 1
- Deleted sentence on negative voltage handling.... 1
- Changed Functional Block Diagram to Typical Application Schematic.... 1
- Changed DIS pin description; leaving DIS pin open would disable the device, and the pin is internally pulled high instead of low.... 3
- Deleted DT pin recommended capacitor size of 2.2nF or greater. Changed DT pin equation.... 3
- Added INA and INB RC filter recommendation.... 3
- Changed all -0.5V minimum to -0.3V to keep consistent with newly released datasheets.... 4
- Changed VDDA-VSSA and VDDB-VSSB absmax from 20V to 30V.... 4
- Changed all absolute maximum value from supply+0.5V to supply+0.3V to keep consistent with newly released datasheets.... 4
- Changed input signal trasient voltage from -2V to -5V and changed test condition from 200ns to 50ns.... 4
- Added D package channel to channel isolation voltage.... 4
- Updated ESD spec from HBM = ±4000 and CDM = ±1500 to HBM = ±2000 and CDM = ±1000 to match ESD industry standards.... 4
- Changed VDDA-VSSA and VDDB-VSSB recommended max from 18V to 25V.... 4
- Deleted ambient temperature spec.... 4
- Changed junction temperature max from 130°C to 150°C.... 4
- Updated thermal values from RθJA = 68.5°C/W, RθJC(top) = 30.5°C/W, RθJB = 22.8°C/W, ψJT = 17.1°C/W, ψJB = 22.5°C/W to RθJA = 80.2°C/W, RθJC(top) = 36.6°C/W, RθJB = 45°C/W, ψJT = 28°C/W, ψJB = 44.3°C/W.... 4
- Updated values from PD = 1825mW, PDI = 15mW, PDA/PDB = 905mW to PD = 950mW, PDI = 50mW, PDA/PDB = 450mW. Changed test conditions.... 5
- Updated DIN EN IEC to the latest standard, updated insulation voltage values.... 6
- Changed barrier capacitance from 0.5pF to ~1.2pF.... 6
- Deleted safety-related certifications section, certification ongoing.... 6
- Changed IS testing condition. Changed IS value from 75mA (with VDDA/B=12V) to 50mA (with VDDA/B=15V) and 30mA (with VDDA/B=25V).... 7
- Updated safety-limiting values from PS = 15mW/905mW/905mW/1825mW to PS = 50mW/750mW/750mW/1550mW.... 7
- Updated IVCCI quiescent current spec Typ value from 1.5mA to 1.4mA.... 8
- Added more test conditions for IVCC and IVDD.... 8
- Updated IVCCI operating current Typ value from 2.5mA to 2.7mA and added Max value 3.2mA.... 8
- Updated IVDDA/IVDDB quiescent current spec Typ from 1.0mA to 1.2mA and Max value from 1.8mA to 2.0mA.... 8
- Updated IVDDA/IVDDB operating current Typ value from 2.5mA to 2.7mA and added Max value 4.4mA. Deleted Cload from test condition.... 8
- Changed VCCI power-up delay from Typ = 40us to Min = 18us, Max = 80us.... 8
- Added VCC UVLO OFF delay and deglitch specs.... 8

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- Updated values from Rising threshold Min = 8V, Typ = 8.5V, Max = 9V to Min = 7.7V, Typ = 8.5V, Max = 8.9V.... 8
- Updated values from Falling threshold Min = 7.5V, Typ = 8V, Max = 8.5V to Min = 7.2V, Typ = 7.9V, Max = 8.4V.... 8
- Updated 8-V UVLO hysteresis typ = 0.5V to 0.6V.... 8
- Deleted VDD power up delay Typ 22us and added Max value of 10us.... 8
- Added VDD UVLO OFF delay and deglitch specs.... 8
- Updated Input high threshold Typ = 1.8V, Max = 2V to Typ = 2V, Max = 2.3V. Deleted Min spec.... 8
- Deleted Input low threshold voltage Max spec.... 8
- Updated Input threshold hysteresis Typ = 0.8V to Typ = 1V.... 8
- Added spec INx Pin Pull Down Resistance.... 8
- Updated peak current test condition to 0.22uF load capacitance. Changed peak output source current direction.... 8
- Updated output resistance test condition from ±10mA to ±0.05A.... 8
- Deleted output voltage at high/low state specs.... 8
- Updated active pull-down Typ = 1.75V, Max = 2.1V to Typ = 1.6V, Max = 2V.... 8
- Updated DT pin specs, deleted dead time matching.... 8
- Changed output rise time Typ from 5ns to 8ns. Deleted Max value.... 9
- Changed output fall time Typ from 6ns to 8ns. Deleted Max value.... 9
- Changed propagation delay TPDHL and TPDLH from Typ=28ns, Max = 40ns to Min = 26ns, Typ = 33ns, Max = 45ns.... 9
- Changed minimum pulse width from Typ = 10ns, Max = 20ns to Min = 4ns, Typ = 12ns, Max = 30ns.... 9
- Changed propagation delay matching from Max = 5ns to Max = 6.5ns from TJ = -40C to -10C and Max = 5ns from TJ = -10C to 150C.... 9
- Changed pulse width distortion max from 5.5ns to 5ns.... 9
- Updated CMTI from Min = 100V/ns to 125V/ns.... 9
- Updated thermal curves to match updated characteristics.... 10
- Updated typical char plots to show device characteristics.... 11
- Deleted mininum pulses in parameter measurement information.... 15
- Changed DT formula. Deleted recommended DT decoupling capacitor size of 2.2nF or greater.... 16
- Updated UVLO delay to match new specs.... 16
- Updated functional block diagram to reflect device characteristics.... 18
- Changed logic table; leaving DIS pin open disables the driver.... 20
- Updated input stage section to match new specs.... 20
- Added paragraph on minimum pulse width to Output Stage section.... 21
- Updated ESD structure diagram to reflect device characteristics.... 22
- Changed dead time equation, deleted recommendation on 2.2nF or greater DT capacitor.... 22
- Changed typical application schematic to remove DT capacitor.... 24
- Updated applications sections to match the latest specs.... 26
- Added Dead Time Setting Guidelines section.... 30
- Changed maximum VDDA/VDDB from 18V to 25V.... 35
- Deleted DT capacitor size recommendation of ≥ 2.2 nF.... 36
- Updated layout guidelines.... 36

Changes from Revision A (April 2018) to Revision B (February 2024) **Page**

- Changed CTI and Material Group values in insulation specifications and added table note.... 6

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC21222D	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 125	21222
UCC21222DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21222
UCC21222DR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21222
UCC21222DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	21222

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC21222 :

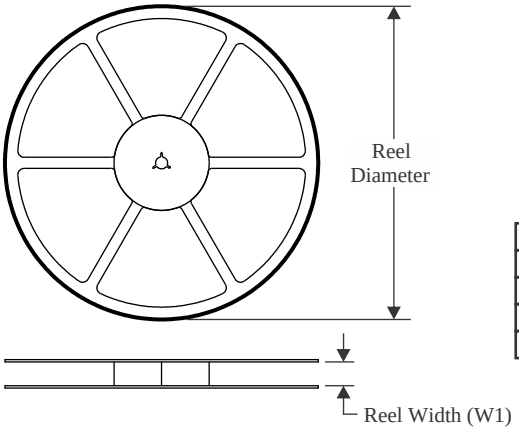
- Automotive : UCC21222-Q1

NOTE: Qualified Version Definitions:

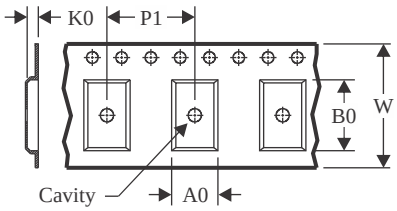
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

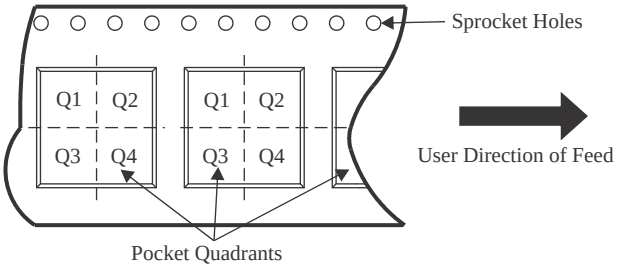


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

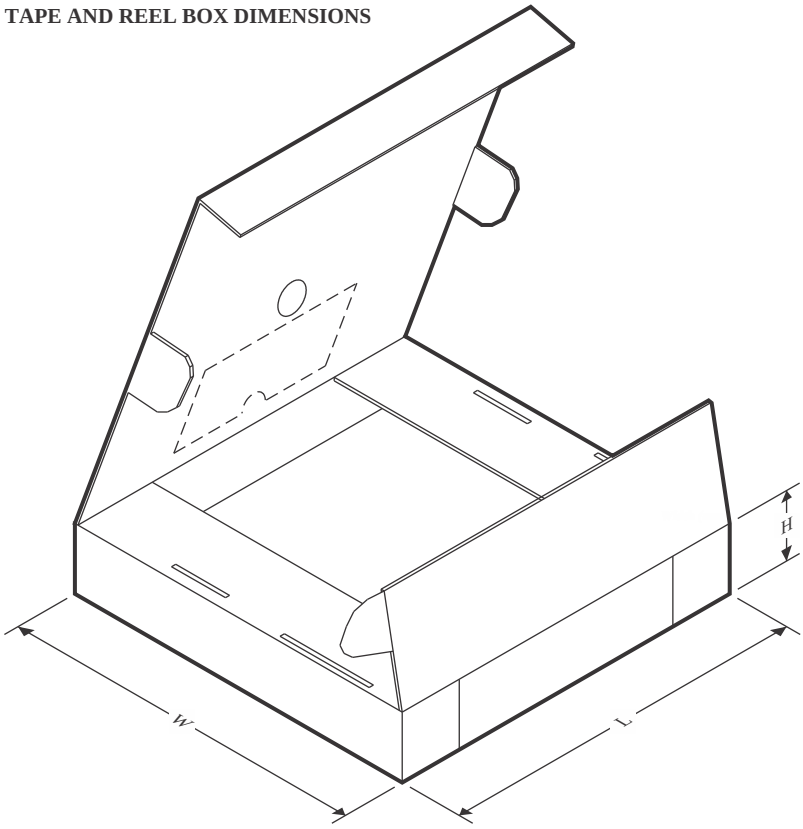
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC21222DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

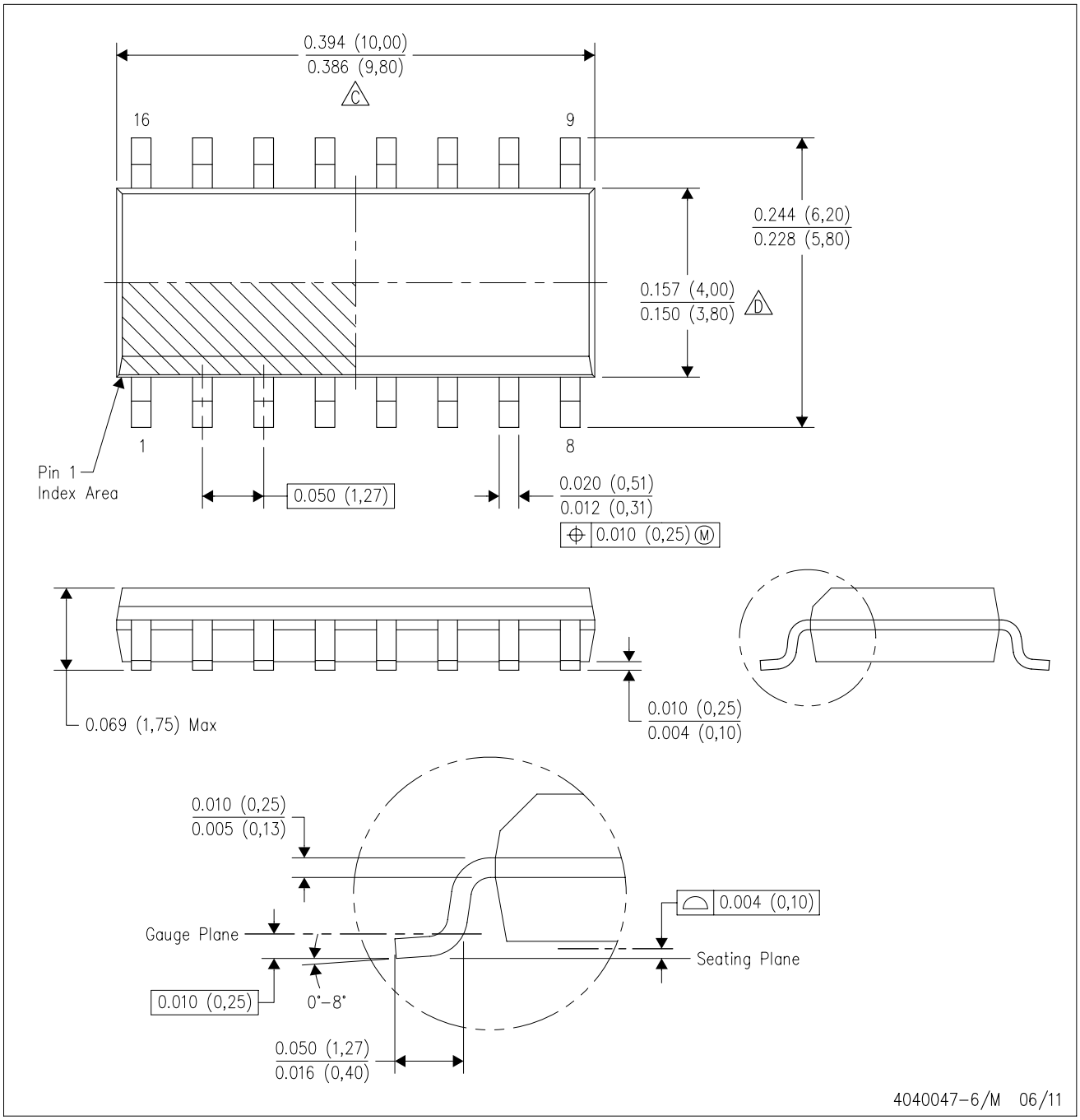
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC21222DR	SOIC	D	16	2500	356.0	356.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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