

HIGH-SPEED DIFFERENTIAL LINE TRANSCEIVERS

FEATURES

- **Sixteen Low-Voltage Differential Transceivers.**
Designed for Signaling Rates up to 200 Mbps per Receiver or 650 Mbps per Transmitter.
- **Simplex (Point-to-Point) or Half-Duplex (Multipoint) Interface**
- **Typical Differential Output Voltage of 340 mV Into a 50-Ω Load**
- **Integrated 110-Ω Line Termination on 'LVDM1677 Product**
- **Propagation Delay Time:**
 - Driver: 2.5 ns Typ
 - Receiver: 3 ns Typ
- **Driver is High Impedance When Disabled or With $V_{CC} < 1.5$ V for Power Up/Down**
Glitch-Free Performance and Hot-Plugging Events
- **Bus-Terminal ESD Protection Exceeds 12 kV**
- **Low-Voltage TTL (LVTTTL) Logic Input Levels Are 5-V Tolerant**
- **Packaged in Thin Shrink Small-Outline Package With 20 mil Terminal Pitch**

DESCRIPTION

The SN65LVDM1676 and SN65LVDM1677 (integrated termination) are sixteen differential line transmitters or receivers (transceivers) that use low-voltage differential signaling (LVDS) to achieve signaling rates up to 200 Mbps per transceiver configured as a receiver and up to 650 Mbps per transceiver configured as a transmitter. These products are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts except that the output current of the drivers are doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50-Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of 100 mV with up to 1 V of ground potential difference between a transmitter and receiver.

SN65LVDM1676DGG (Marked as LVDM1676)

SN65LVDM1677DGG (Marked as LVDM1677)

(TOP VIEW)

GND	1	64	A1Y
V _{CC}	2	63	A1Z
V _{CC}	3	62	A2Y
GND	4	61	A2Z
ATX/RX	5	60	A3Y
A1A	6	59	A3Z
A2A	7	58	A4Y
A3A	8	57	A4Z
A4A	9	56	B1Y
BTX/RX	10	55	B1Z
B1A	11	54	B2Y
B2A	12	53	B2Z
B3A	13	52	B3Y
B4A	14	51	B3Z
GND	15	50	B4Y
V _{CC}	16	49	B4Z
V _{CC}	17	48	C1Y
GND	18	47	C1Z
C1A	19	46	C2Y
C2A	20	45	C2Z
C3A	21	44	C3Y
C4A	22	43	C3Z
CTX/RX	23	42	C4Y
D1A	24	41	C4Z
D2A	25	40	D1Y
D3A	26	39	D1Z
D4A	27	38	D2Y
DTX/RX	28	37	D2Z
GND	29	36	D3Y
V _{CC}	30	35	D3Z
V _{CC}	31	34	D4Y
GND	32	33	D4Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of transceivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

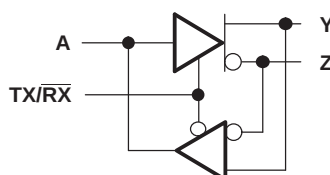
The SN65LVDM1676 and SN65LVDM1677 are characterized for operation from -40°C to 85°C .

FUNCTION TABLE⁽¹⁾

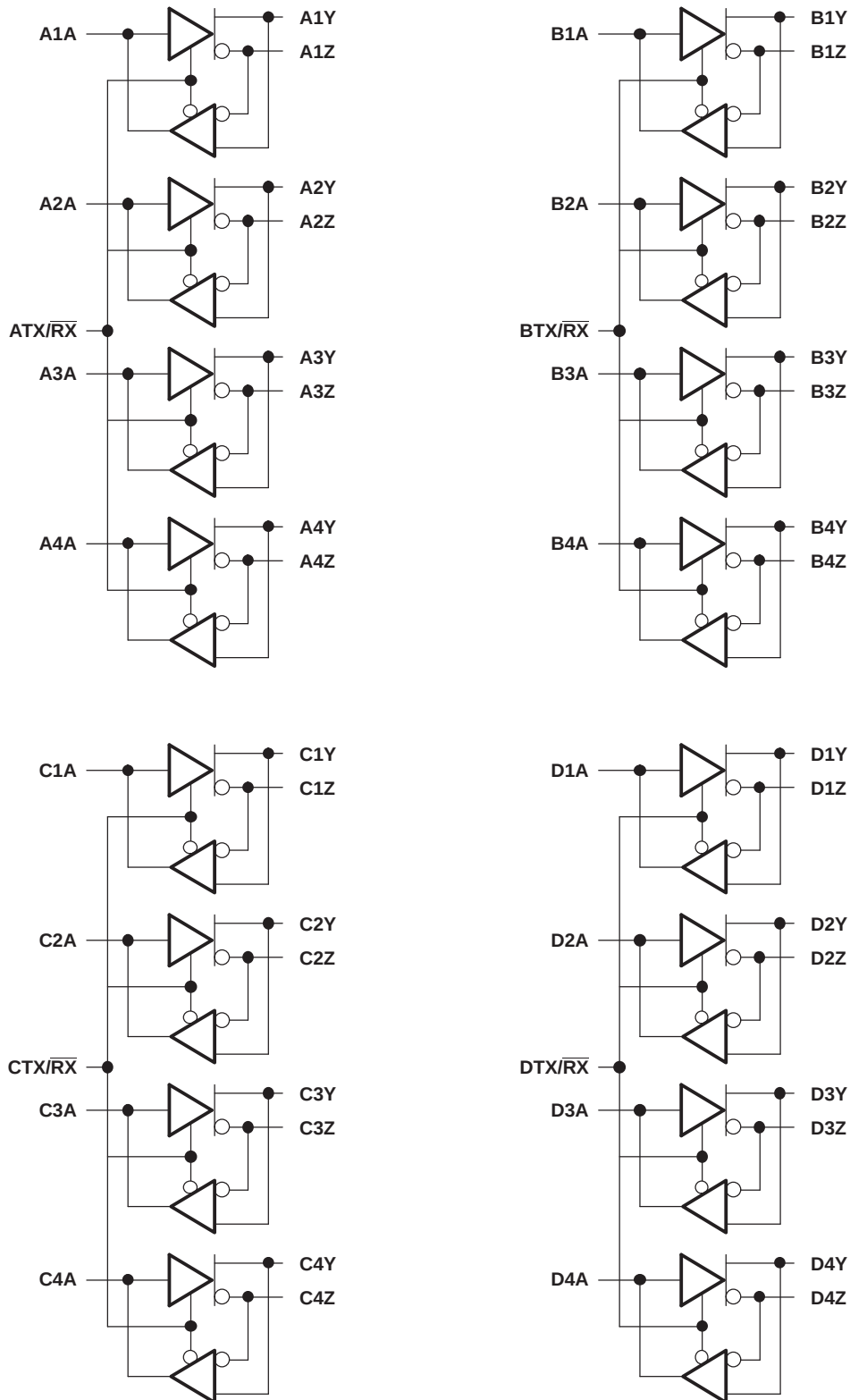
INPUTS			OUTPUTS		
(Y – Z)	TX/RX	A	Y	Z	A
$V_{ID} \geq 100 \text{ mV}$	L	NA	Z	Z	H
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$	L	NA	Z	Z	?
$V_{ID} \leq -100 \text{ mV}$	L	NA	Z	Z	L
Open circuit	L	NA	Z	Z	H
NA	H	L	L	H	Z
NA	H	H	H	L	Z

(1) H = high level, L = low level, Z = high impedance, ? = indeterminate

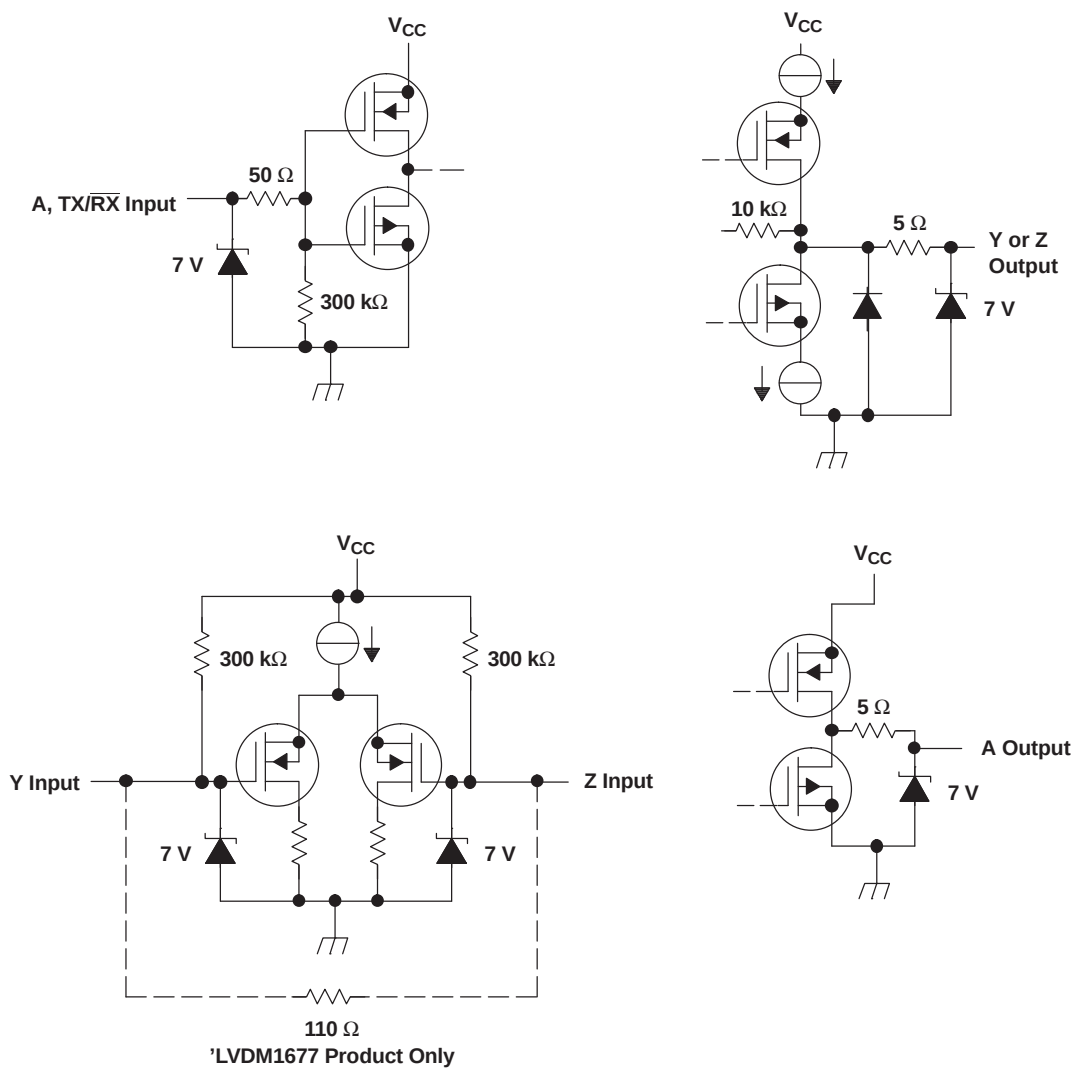
LVD Transceiver



LOGIC DIAGRAM (POSITIVE LOGIC)



EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

			RATING
V _{CC}	Supply voltage range		–0.5 V to 4 V
V _I	Input voltage range	A, TX/RX	–0.5 V to 6 V
		Y or Z	–0.5 V to 4 V
V _{ID}	Differential input voltage magnitude, (SN65LVDM1677 only)		1 V
I _O	Receiver output current		±20 mA
P _D	Continuous power dissipation		See the Dissipation Rating Table
ESD	Electrostatic discharge ⁽³⁾	Y, Z, and GND	Class 3, A: 8 kV, B: 600 V
		All Pins	Class 3, A: 7 kV, B: 500 V

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 85°C POWER RATING
DGG	2094 mW	16.7 mW/°C	1089 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	3	3.3	3.6	V
V _{IH}	High-level input voltage	2			
V _{IL}	Low-level input voltage			0.8	
V _{ID}	Magnitude of differential input voltage	0.1		0.6	
V _{IC}	Common-mode input voltage	$\frac{ V_{ID} }{2}$	$2.4 - \frac{ V_{ID} }{2}$		
			V _{CC} –0.8		V
I _{OL}	Receiver low-level output current			8	mA
I _{OH}	Receiver high-level output current	–8 ⁽¹⁾			
T _A	Operating free-air temperature	–40		85	°C

- (1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DRIVER						
I_{CC}	Supply current	Driver enabled, receiver disabled $R_L = 50\ \Omega$ ('LVDM1676) or $R_L = 100\ \Omega$ ('LVDM1677)	140	175		mA
		Driver disabled, receiver enabled, no load	45	60		
$ V_{OD} $	Differential output voltage magnitude	$R_L = 50\ \Omega$ ('LVDM1676) or $R_L = 100\ \Omega$ ('LVDM1677), See Figure 2 and Figure 1	247	340	454	mV
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	$R_L = 50\ \Omega$ ('LVDM1676) or $R_L = 100\ \Omega$ ('LVDM1677), See Figure 3	1.125	1.375		V
$\Delta V_{OC(S)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		50		150	mV
I_{IH}	High-level input current	$V_{IH} = 2\text{ V}$		3	20	μA
I_{IL}	Low-level input current	$V_{IL} = 0.8\text{ V}$		2	10	μA
I_{OS}	Short-circuit output current	V_{OY} or $V_{OZ} = 0\text{ V}$			10	mA
		$V_{OD} = 0\text{ V}$			10	
$I_{O(OFF)}$	Power-off output current	$V_{CC} = 1.5\text{ V}$, $V_O = 2.4\text{ V}$	–10		10	μA
C_{IN}	Input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{ V}$		5		pF
RECEIVER						
V_{IT+}	Positive-going differential input voltage threshold	See Figure 6 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		–100			
V_{OH}	High-level output voltage	$I_{OH} = -8\text{ mA}$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8\text{ mA}$			0.4	V
I_I	Input current (Y or Z inputs)	$V_{IY} = V_{IZ} = 0\text{ V}$	–40	–24		μA
		$V_{IY} = V_{IZ} = 2.4\text{ V}$		–8	–1.2	
I_{ID}	Differential input current $ I_{IY} - I_{IZ} $ (inputs)	'LVDM1676 $V_{IY} = 0\text{ V}$ and $V_{IZ} = 100\text{ mV}$, $V_{IY} = 2.4\text{ V}$ and $V_{IZ} = 2.3\text{ V}$		5	10	μA
		'LVDM1677 $V_{IY} = 0.2\text{ V}$ and $V_{IZ} = 0\text{ V}$, $V_{IY} = 2.4\text{ V}$ and $V_{IZ} = 2.2\text{ V}$	1.5		2.2	mA
$I_{I(OFF)}$	Power-off input current (Y or Z inputs)	$V_{CC} = 0\text{ V}$, $V_I = 2.4\text{ V}$	–25		25	μA

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DRIVER						
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 50 Ω ('LVDM1676) or R _L = 100 Ω ('LVDM1677), C _L = 10 pF, See Figure 4	1.3	2.5	3.6	ns
t _{PHL}	Propagation delay time, high-to-low-level output		1.3	2.5	3.6	
t _r	Differential output signal rise time			0.5	1.2	
t _f	Differential output signal fall time			0.5	1.2	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			0.1	0.6	
t _{sk(o)}	Channel-to-channel output skew ⁽²⁾			0.1	0.4	
t _{sk(pp)}	Part-to-part skew ⁽³⁾				1	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		11	20	
t _{PZL}	Propagation delay time, high-impedance-to-low-level output			10	20	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			3	10	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			3	10	
RECEIVER						
t _{PLH}	Propagation delay time, low-to-high-level output	C _L = 10 pF, See Figure 7	1.5	3	4.5	ns
t _{PHL}	Propagation delay time, high-to-low-level output		1.5	3	4.5	
t _r	Output signal rise time			0.6	1.6	
t _f	Output signal fall time			0.6	1.6	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			0.2	0.8	
t _{sk(o)}	Channel-to-channel output skew ⁽⁴⁾			0.7	1.2	
t _{sk(pp)}	Part-to-part skew ⁽⁵⁾				1	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 8		9	15	
t _{PZL}	Propagation delay time, high-impedance-to-low-level output			8	15	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			12	20	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			11	20	

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

(5) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

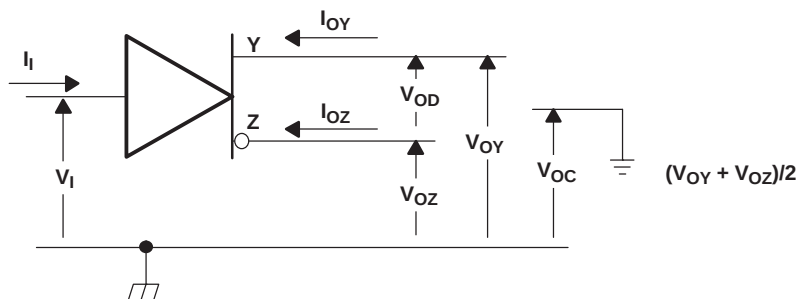


Figure 1. Driver Voltage and Current Definitions

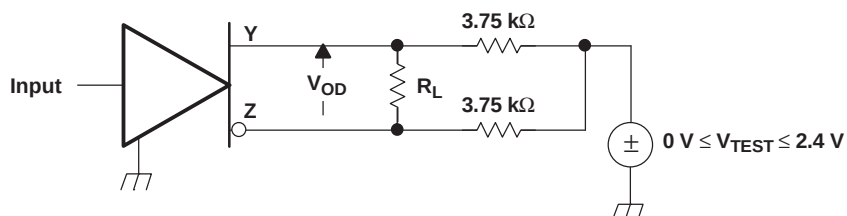
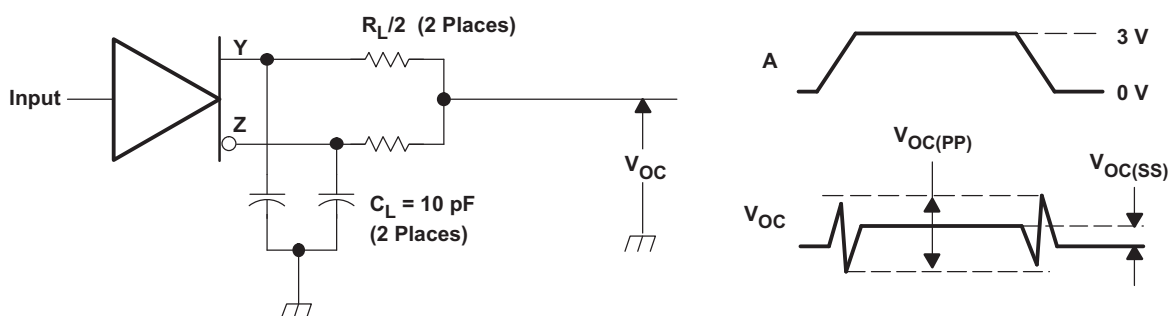


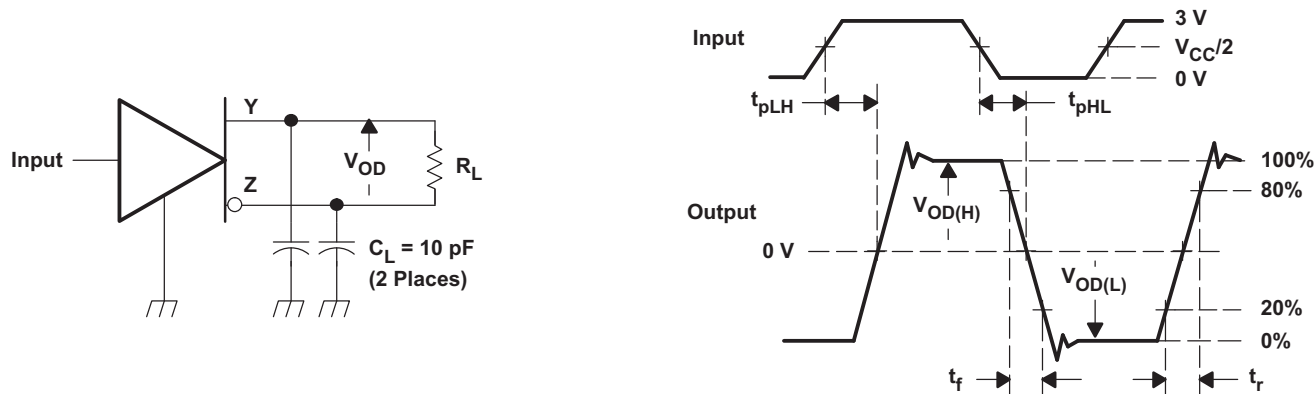
Figure 2. Driver V_{OD} Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

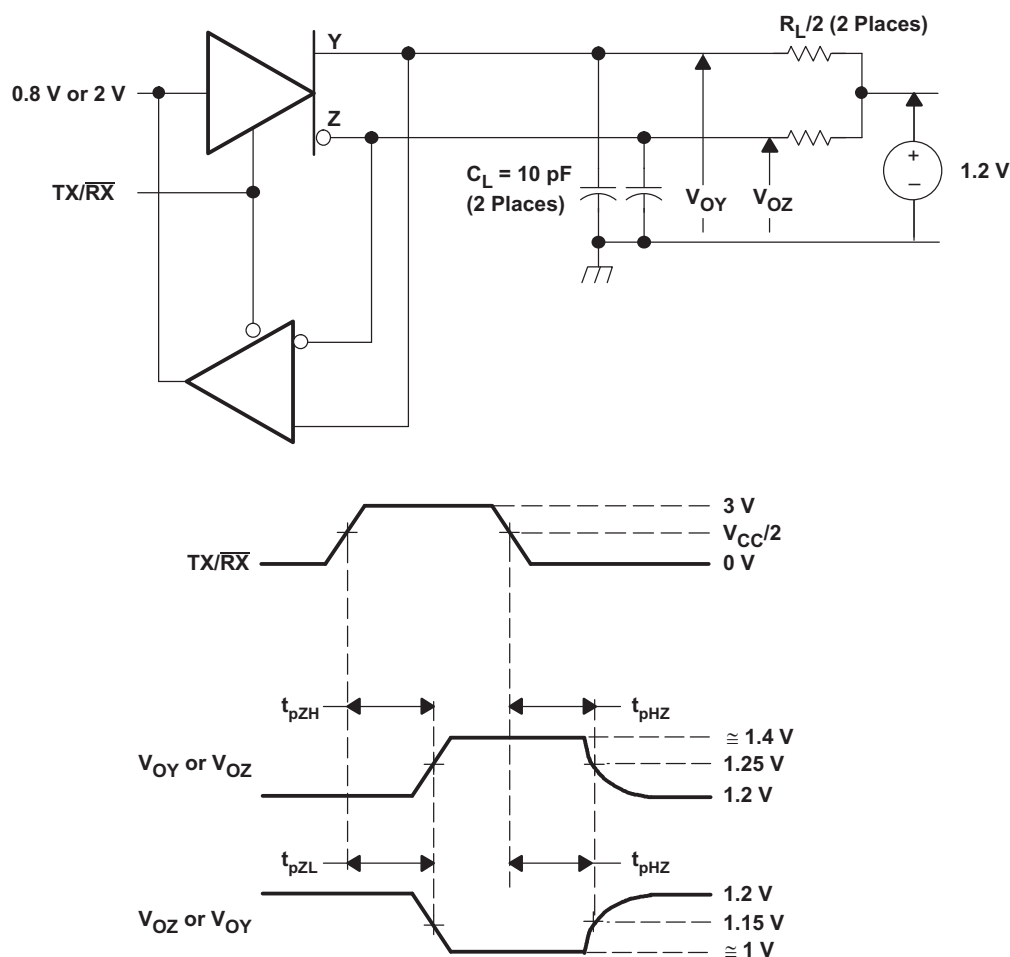
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = $10 \pm 0.2 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = $500 \pm 10 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

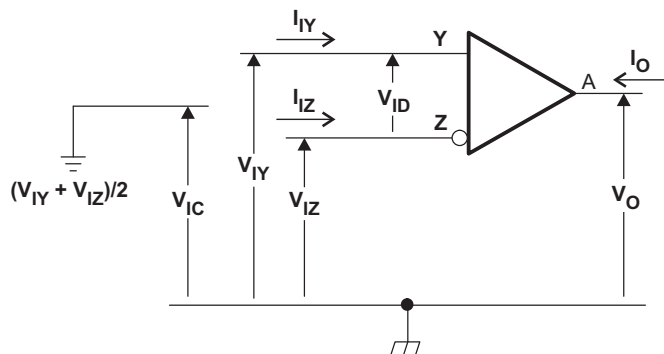
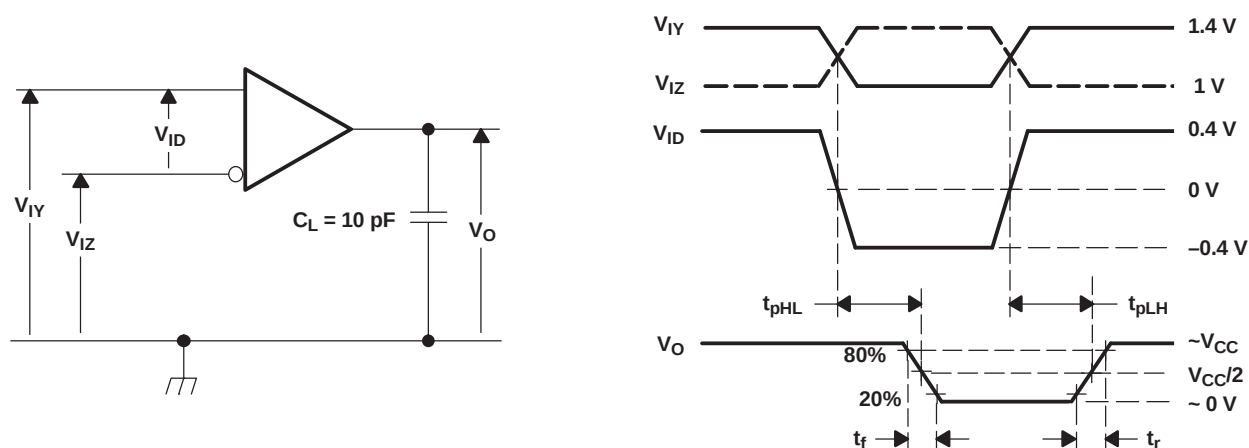


Figure 6. Voltage Definitions

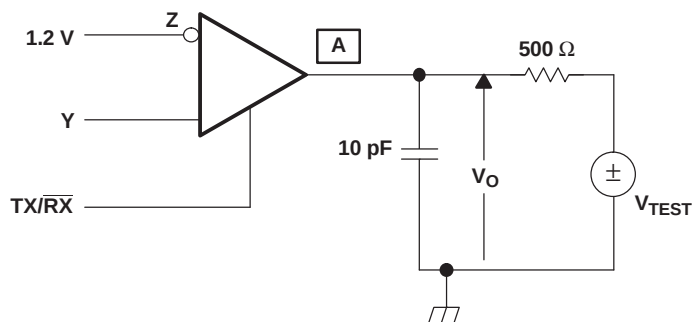
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE
V_{IY}	V_{IZ}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T.

Figure 7. Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

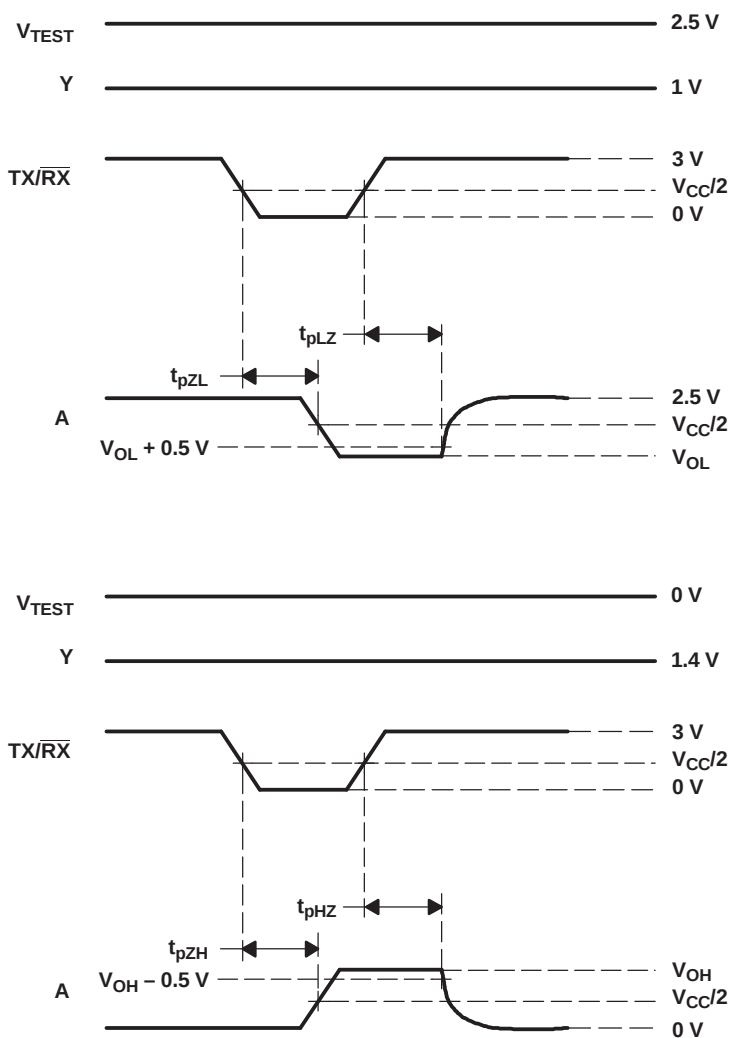


Figure 8. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

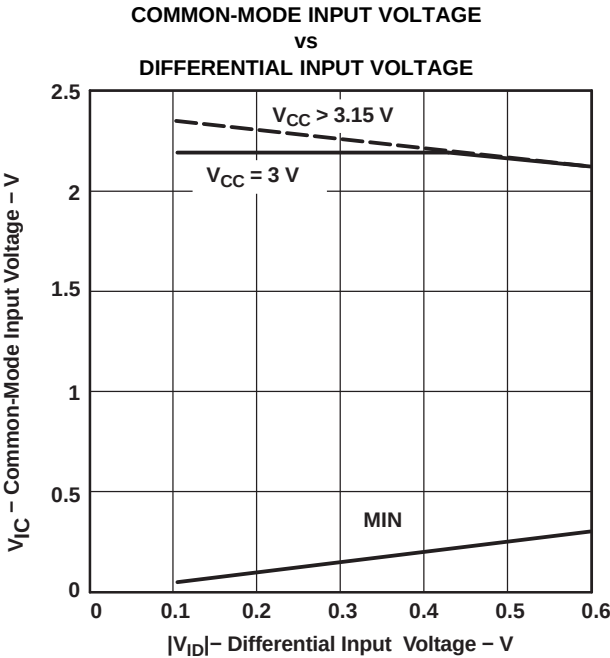


Figure 9.

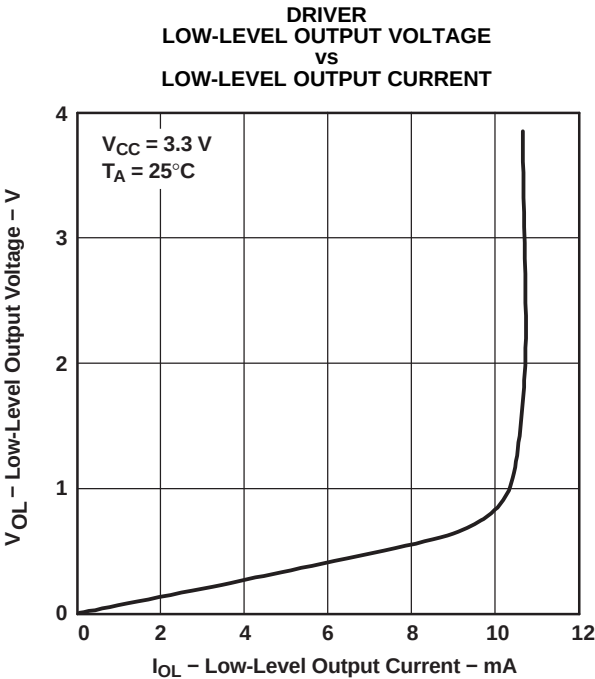


Figure 10.

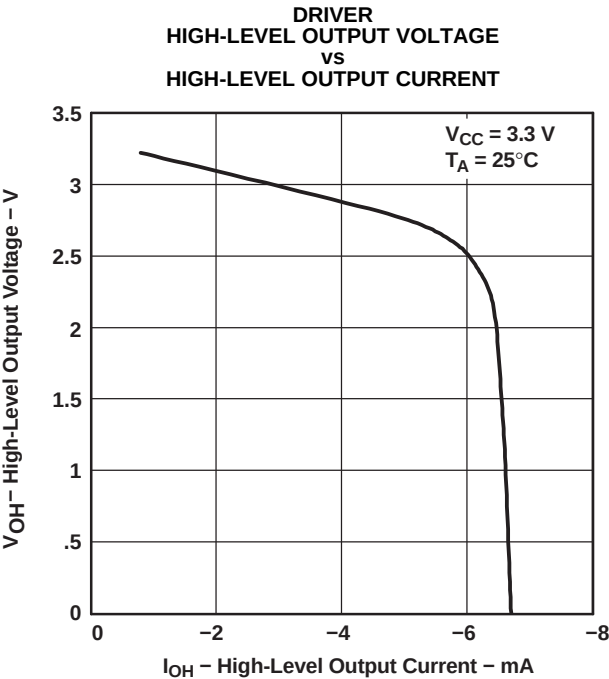


Figure 11.

TYPICAL CHARACTERISTICS (continued)

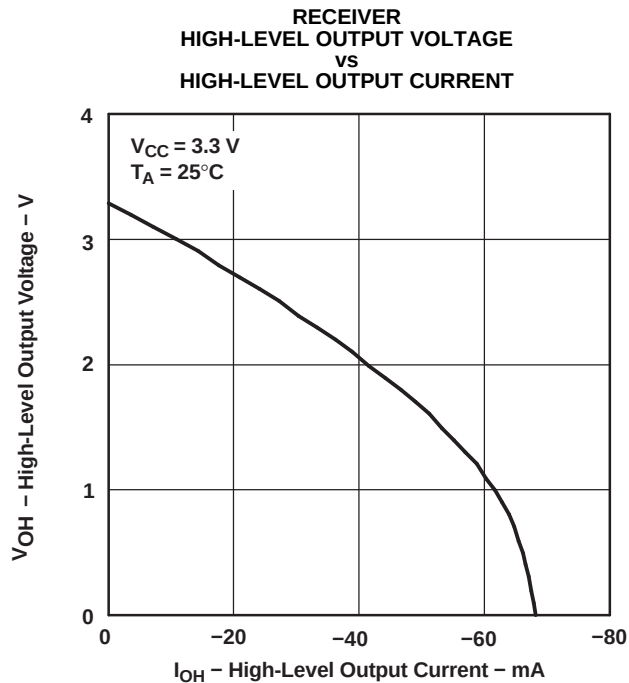


Figure 12.

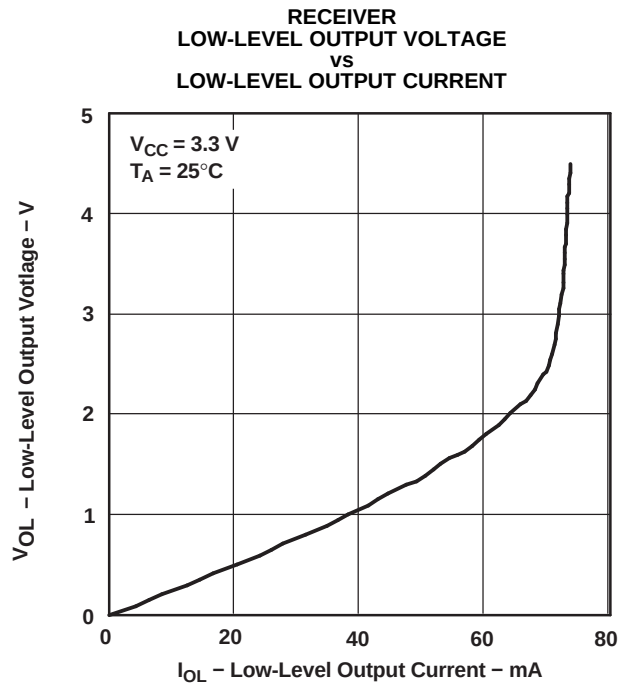


Figure 13.

TYPICAL CHARACTERISTICS (continued)

DRIVER EYE PATTERN

TEST CONDITIONS

- $V_{CC} = 3.6\text{ V}$
- $T_A = 25^\circ\text{C}$ (ambient temperature)
- All 16 channels switching simultaneously with NRZ data. Scope is triggered at the same frequency with pulse. Input signal level = 0 V to 3 V single ended.
- Resistive loading with no added capacitance

EQUIPMENT

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS6604 Digital Storage Scope
- Agilent ParBERT E4832A

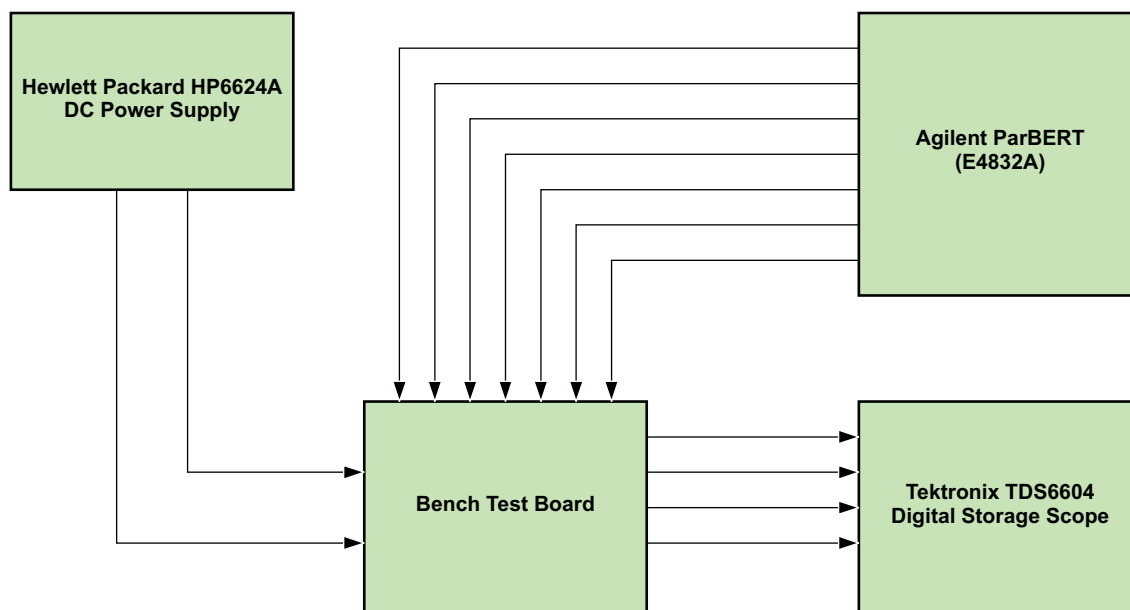
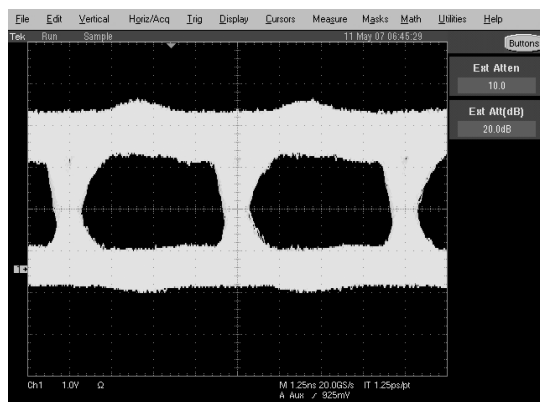
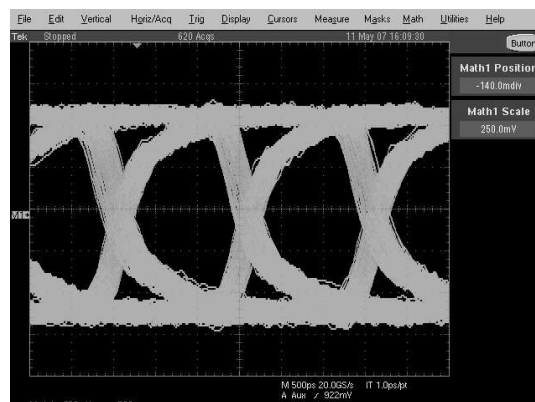


Figure 14. Equipment Setup

TYPICAL CHARACTERISTICS (continued)



(a) representative Transceiver configured as Rx @ 200 Mbps
(Ch1 = xyA)



(b) representative Transceiver configured as Tx @ 650 Mbps
(M1 = xyY-xyZ)

NOTE: x represents transceiver group A, B, C, or D, and y represents transceiver 1, 2, 3, or 4.

Figure 15. Typical Driver Eye Pattern for the SN65LVDM1676 With 12 Transceivers Configured as Rx and 4 Transceivers Configured as Tx all Switching Frequency Asynchronous Data
($T_A = 25^\circ\text{C}$; $V_{CC} = 3.6\text{ V}$; PRBS = $2^{23}-1$)

APPLICATION INFORMATION

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -50 mV and 50 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different, however, in how it handles the open-input circuit situation.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through $300\text{-k}\Omega$ resistors as shown in [Figure 16](#). The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

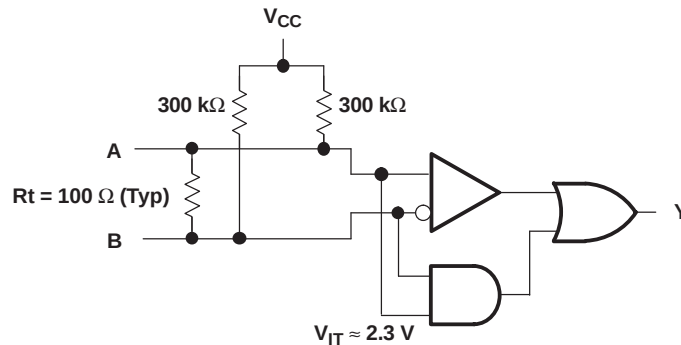


Figure 16. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 50-mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDM1676DGG	Active	Production	TSSOP (DGG) 64	25 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGG.B	Active	Production	TSSOP (DGG) 64	25 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGG4	Active	Production	TSSOP (DGG) 64	25 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGG4.B	Active	Production	TSSOP (DGG) 64	25 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGR	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1676DGGR.B	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1676
SN65LVDM1677DGG	Active	Production	TSSOP (DGG) 64	25 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGG.B	Active	Production	TSSOP (DGG) 64	25 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGR	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGR.B	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGRG4	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677
SN65LVDM1677DGGRG4.B	Active	Production	TSSOP (DGG) 64	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDM1677

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

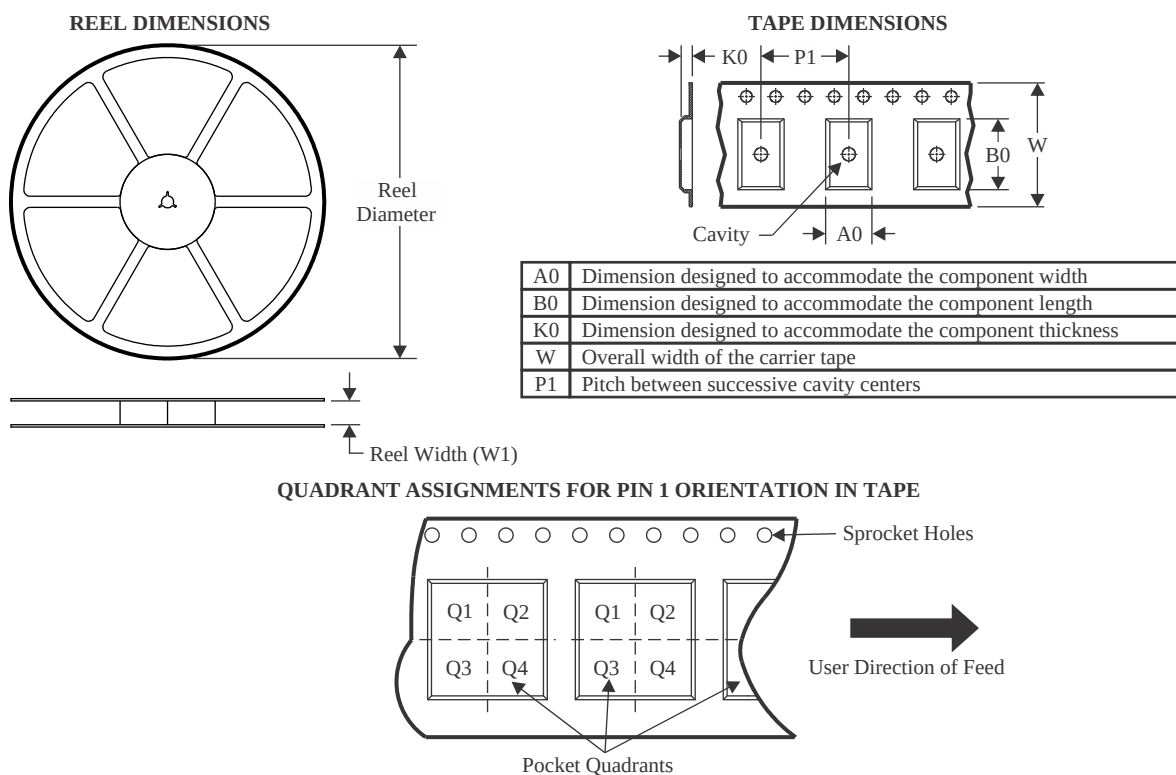
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

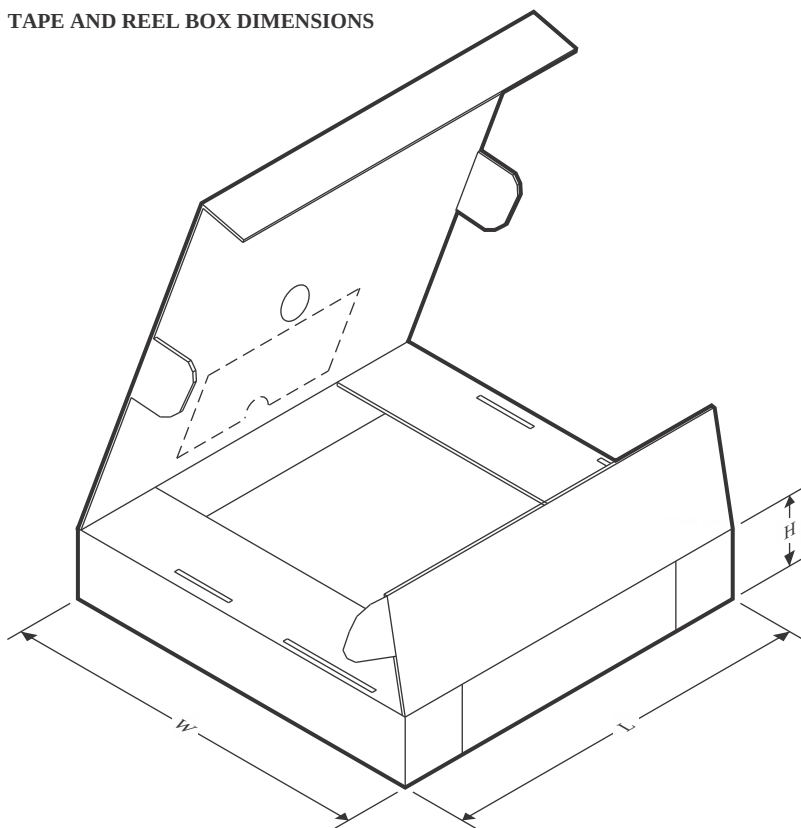
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDM1676DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDM1677DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDM1677DGGRG4	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

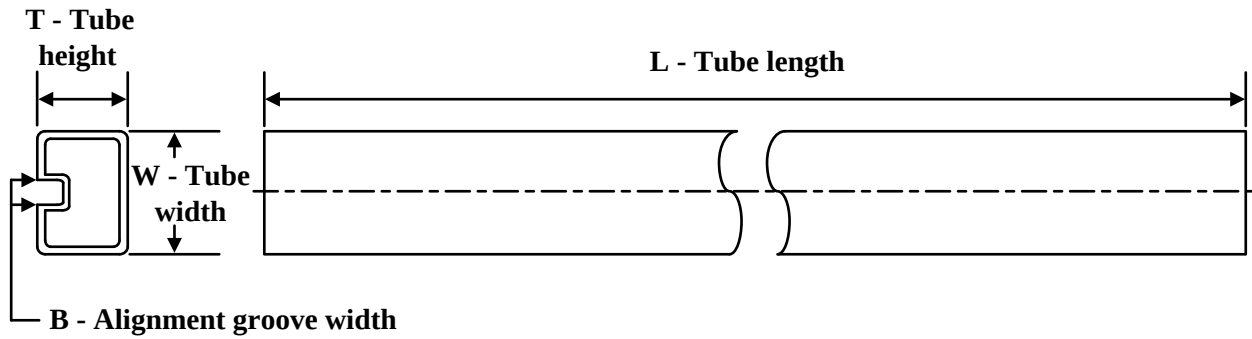
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDM1676DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN65LVDM1677DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN65LVDM1677DGGRG4	TSSOP	DGG	64	2000	367.0	367.0	45.0

TUBE



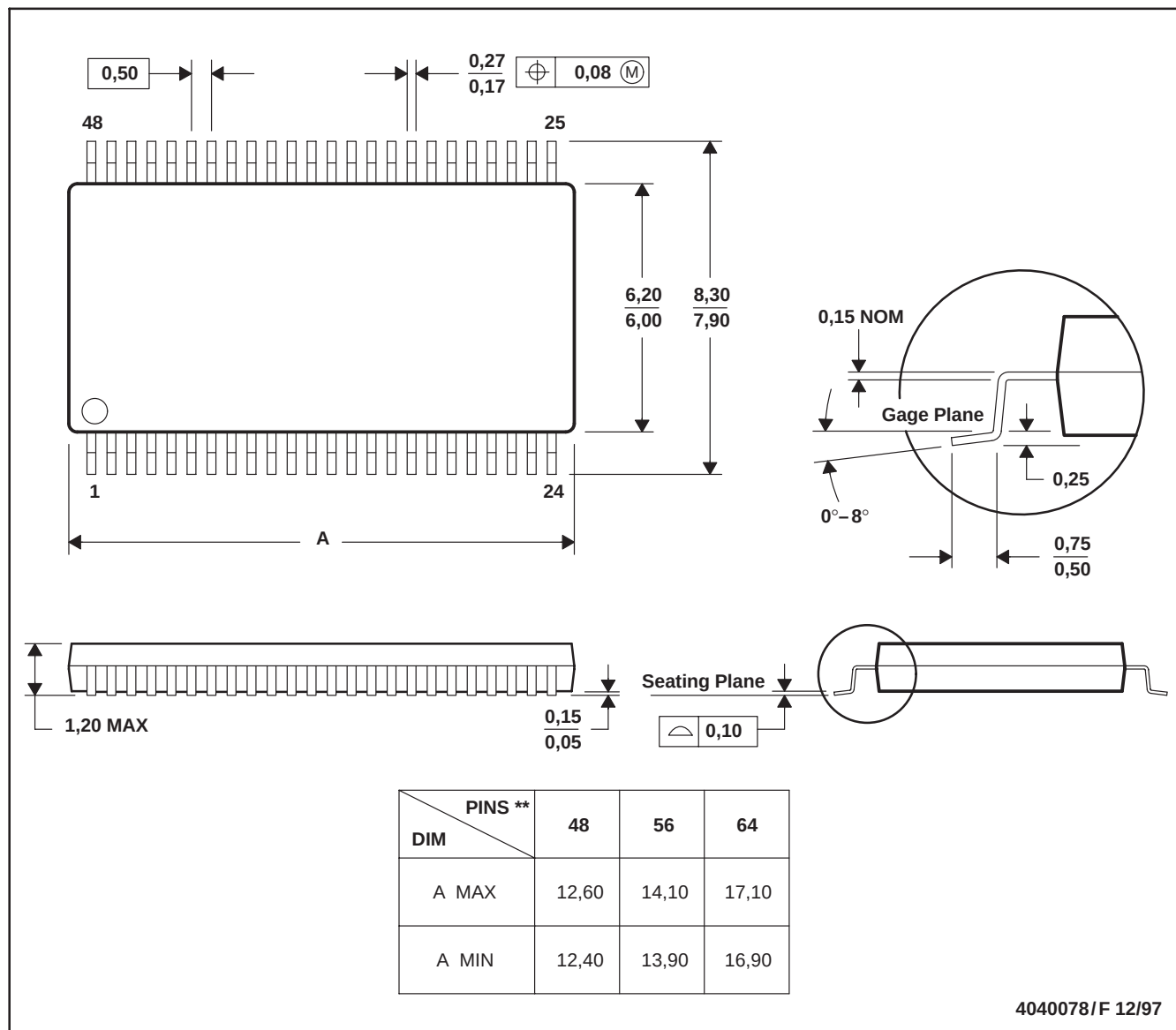
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVDM1676DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1676DGG.B	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1676DGGG4	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1676DGGG4.B	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1677DGG	DGG	TSSOP	64	25	530	11.89	3600	4.9
SN65LVDM1677DGG.B	DGG	TSSOP	64	25	530	11.89	3600	4.9

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated