

DS34LV87T Enhanced CMOS Quad Differential Line Driver

Check for Samples: [DS34LV87T](#)

FEATURES

- Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation
- Interoperable With Existing 5V RS-422 Networks
- Ensured V_{OD} of 2V Min Over Operating Conditions
- Balanced Output Crossover for Low EMI (Typical Within 40 mV of 50% Voltage Level)
- Low Power Design (330 μ W @ 3.3V Static)
- ESD ≥ 7 kV on Cable I/O Pins (HBM)
- Industrial Temperature Range
- Ensured AC Parameter:
 - Maximum Driver Skew: 2 ns
 - Maximum Transition Time: 10 ns
- Pin Compatible With DS26C31
- Available in SOIC Packaging

DESCRIPTION

The DS34LV87T is a high speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV87T features low static I_{CC} of 100 μ A max which makes it ideal for battery powered and power conscious applications. The TRI-STATE enable, EN, allows the device to be disabled when the device is not in use to minimize power. The dual enable scheme allows for flexibility in turning devices on or off.

Protection diodes protect all the driver inputs against electrostatic discharge. The driver and enable inputs (DI and EN) are compatible with LVTTTL and LVCMOS devices. Differential outputs have the same V_{OD} (≥ 2 V) ensure as the 5V version. The outputs have enhanced ESD Protection providing greater than 7 kV tolerance.

Connection Diagram

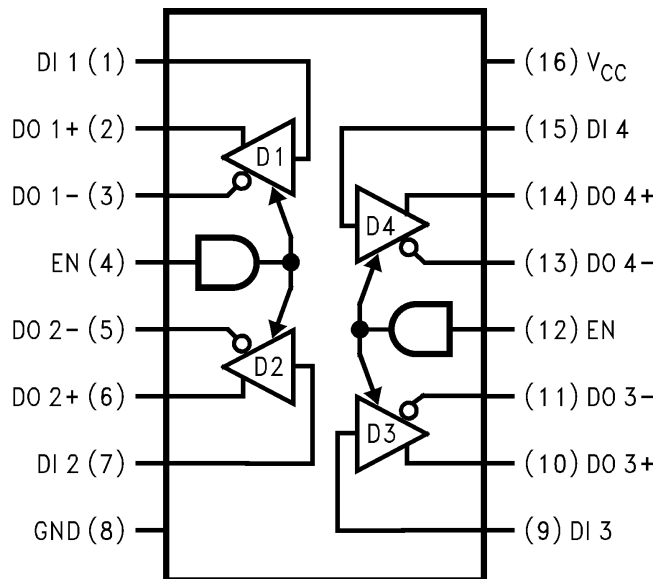


Figure 1. Dual-In-Line Package (Top View)
See Package Number D0016A

TRUTH TABLE⁽¹⁾

Enables	Input	Outputs	
EN	DI	DO+	DO-
L	X	Z	Z
H	H	H	L
H	L	L	H

- (1) L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		-0.5V to +7V
Enable Input Voltage (EN)		-0.5V to $V_{CC} + 0.5V$
Driver Input Voltage (D_I)		-0.5V to $V_{CC} + 0.5V$
Clamp Diode Current		± 20 mA
DC Output Current, per pin		± 150 mA
Driver Output Voltage	(Power Off: DO+, DO-)	-0.5V to +7V
Maximum Package Power Dissipation @+25°C	D Package	1226 mW
Derate D Package		9.8 mW/°C above +25°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature Range (Soldering, 4 sec.)		+260°C
ESD Ratings (HBM, 1.5k, 100 pF)	Driver Outputs	≥ 7 kV
	Other Pins	≥ 2.5 kV

- (1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (2) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The table of [Electrical Characteristics](#) specifies conditions of device operation.

RECOMMENDED OPERATING CONDITIONS

		Min	Typ	Max	Units
Supply Voltage (V_{CC})		3.0	3.3	3.6	V
Operating Free Air	Temperature Range (T_A) DS34LV87T	-40	25	+85	°C
Input Rise and Fall Time				500	ns

ELECTRICAL CHARACTERISTICS⁽¹⁾⁽²⁾

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V _{OD1}	Output Differential Voltage	R _L = ∞, (No Load)	DO+, DO–		3.3	4.0	V
V _{OD2}	Output Differential Voltage	R _L = 100Ω See Figure 2		2	2.6		V
ΔV _{OD2}	Change in Magnitude of Output Differential Voltage			–400	7	400	mV
V _{OD3}	Output Differential Voltage	R _L = 3900Ω (V.11), See Figure 2 ⁽³⁾			3.2	3.5	V
V _{OC}	Common Mode Voltage	R _L = 100Ω See Figure 2			1.5	2	V
ΔV _{OC}	Change in Magnitude of Common Mode Voltage			–400	6	400	mV
I _{OZ}	TRI-STATE Leakage Current	V _{OUT} = V _{CC} or GND Drivers Disabled			±0.5	±20	μA
I _{SC}	Output Short Circuit Current	V _{OUT} = 0V V _{IN} = V _{CC} or GND ⁽⁴⁾		–40	–70	–150	mA
I _{OFF}	Output Leakage Current	V _{CC} = 0V, V _{OUT} = 3V			0.03	100	μA
		V _{CC} = 0V, V _{OUT} = –0.25V			–0.08	–100	μA
V _{IH}	High Level Input Voltage		DI, EN	2.0		V _{CC}	V
V _{IL}	Low Level Input Voltage			GND		0.8	V
I _{IH}	High Level Input Current	V _{IN} = V _{CC}				10	μA
I _{IL}	Low Level Input Current	V _{IN} = GND		–10			μA
V _{CL}	Input Clamp Voltage	I _{IN} = –18 mA				–1.5	V
I _{CC}	Power Supply Current	No Load, V _{IN} (all) = V _{CC} or GND	V _{CC}			100	μA

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages V_{OD1}, V_{OD2}, V_{OD3}.
- (2) All typical values are given for V_{CC} = 3.3V and T_A = +25°C.
- (3) This specification limit is for compliance with TIA/EIA-422-B and ITU-T V.11.
- (4) Only one output shorted at a time. The output (true or complement) is configured High.

SWITCHING CHARACTERISTICS⁽¹⁾⁽²⁾

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 50\text{ pF}$ See Figure 3 and Figure 4	6	10.5	16	ns
t_{PLHD}	Differential Propagation Delay Low to High		6	11	16	ns
t_{SKD}	Differential Skew $ t_{PHLD} - t_{PLHD} $			0.5	2.0	ns
t_{SK1}	Skew, Pin to Pin (same device)			1.0	2.0	ns
t_{SK2}	Skew, Part to Part ⁽³⁾			3.0	5.0	ns
t_{TLH}	Differential Transition Time Low to High (20% to 80%)			4.2	10	ns
t_{THL}	Differential Transition Time High to Low (80% to 20%)			4.7	10	ns
t_{PHZ}	Disable Time High to Z	See Figure 5 and Figure 6		12	20	ns
t_{PLZ}	Disable Time Low to Z			9	20	ns
t_{PZH}	Enable Time Z to High			22	32	ns
t_{PZL}	Enable Time Z to Low			22	32	ns
f_{MAX}	Maximum Operating Frequency ⁽⁴⁾			32		MHz

(1) $f = 1\text{ MHz}$, t_r and $t_f \leq 6\text{ ns}$ (10% to 90%).

(2) See TIA/EIA-422-B specifications for exact test conditions.

(3) Devices are at the same V_{CC} and within 5°C within the operating temperature range.

(4) All channels switching, output duty cycle criteria is 40%/60% measured at 50%. This parameter is ensured by design and characterization.

PARAMETER MEASUREMENT INFORMATION

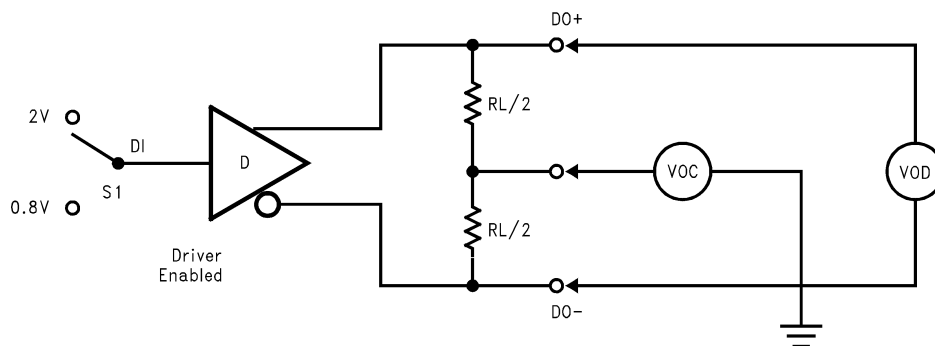


Figure 2. Differential Driver DC Test Circuit

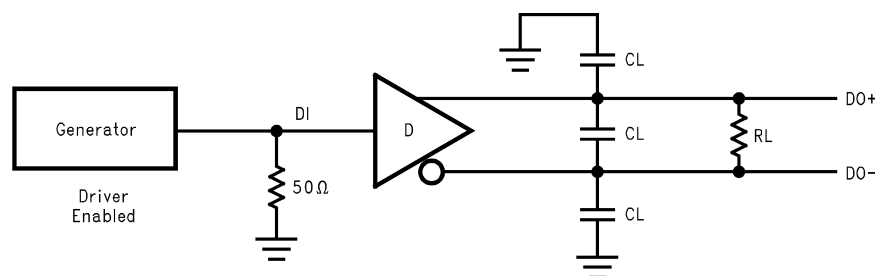
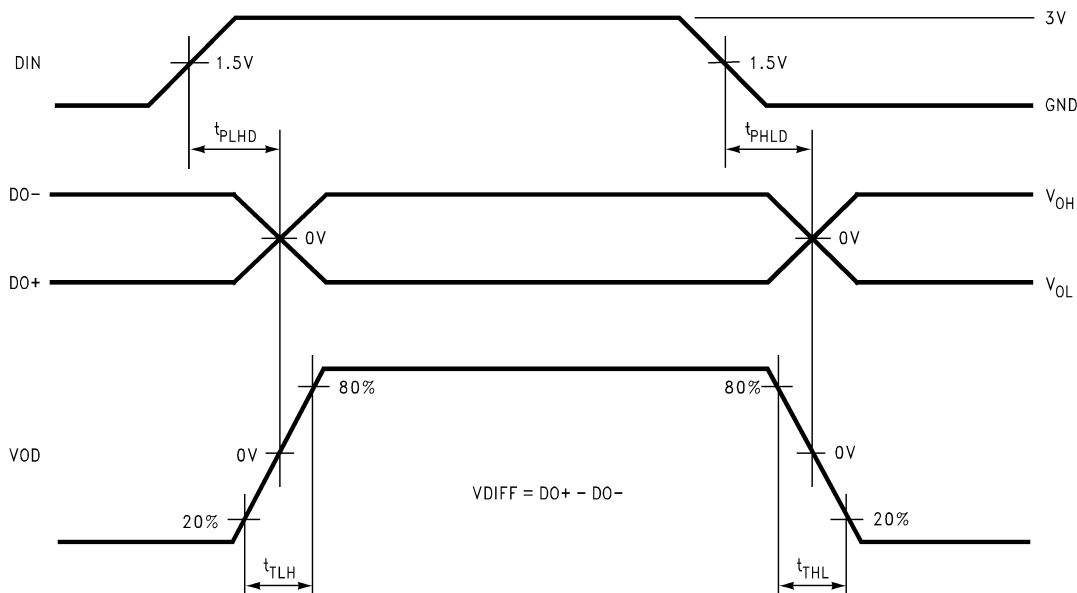


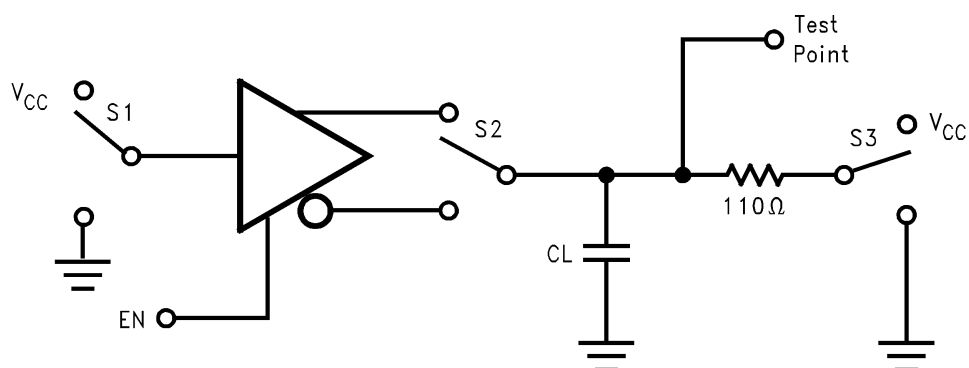
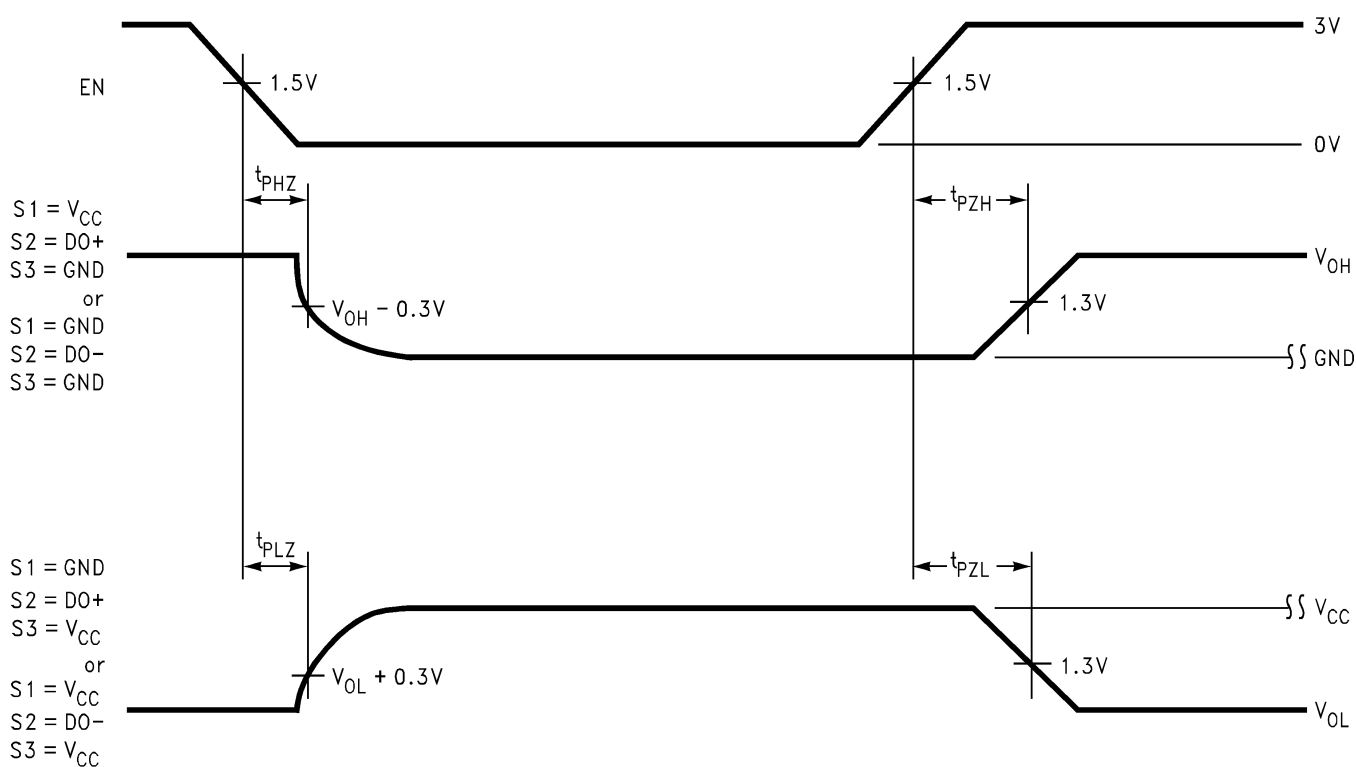
Figure 3. Differential Driver Propagation Delay and Transition Time Test Circuit



Generator waveform for all tests unless otherwise specified: $f = 1\text{ MHz}$, Duty Cycle = 50%, $Z_o = 50\Omega$, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

C_L includes probe and fixture capacitance.

Figure 4. Differential Driver Propagation Delay and Transition Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)**Figure 5. Driver Single-Ended Tri-state Test Circuit****Figure 6. Driver Single-Ended Tri-state Waveforms**

TYPICAL APPLICATION INFORMATION

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

- Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423([SNLA137](#))
- A Comparison of Differential Termination Techniques([SNLA304](#))

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 μF in parallel with 0.01 μF at the power supply pin. A 10 μF or greater tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

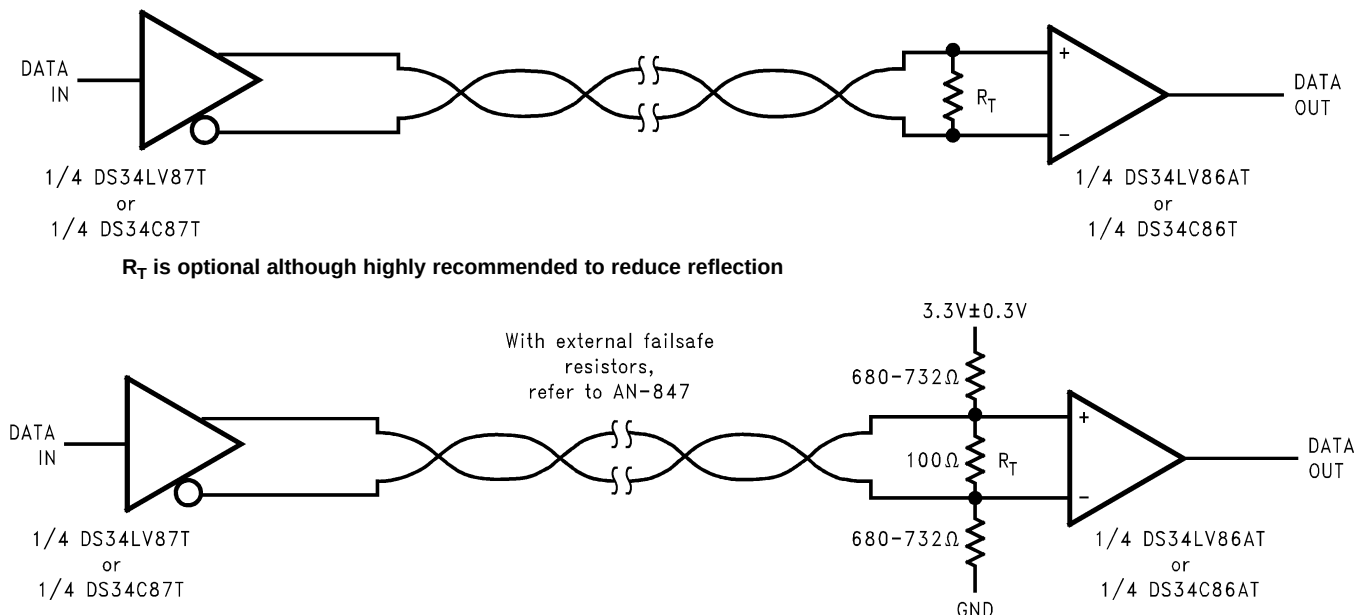


Figure 7. Typical Driver Connection

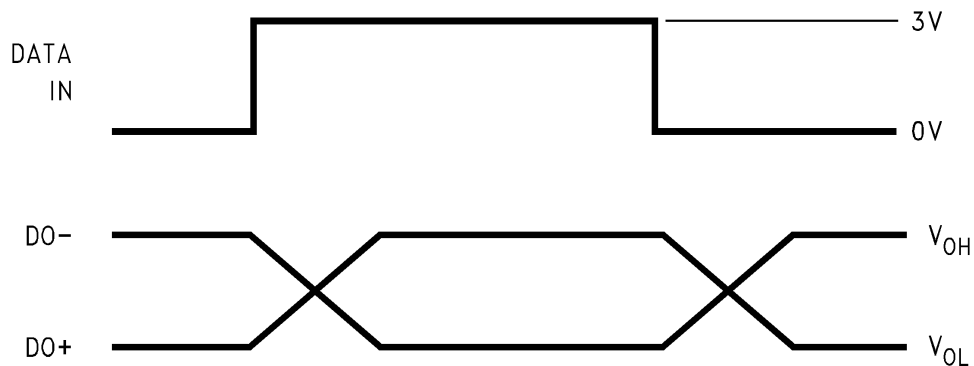


Figure 8. Typical Driver Output Waveforms

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS34LV87TM/NOPB	Active	Production	SOIC (D) 16	48 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS34LV87 TM
DS34LV87TM/NOPB.A	Active	Production	SOIC (D) 16	48 TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS34LV87 TM
DS34LV87TMX/NOPB	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS34LV87 TM
DS34LV87TMX/NOPB.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS34LV87 TM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

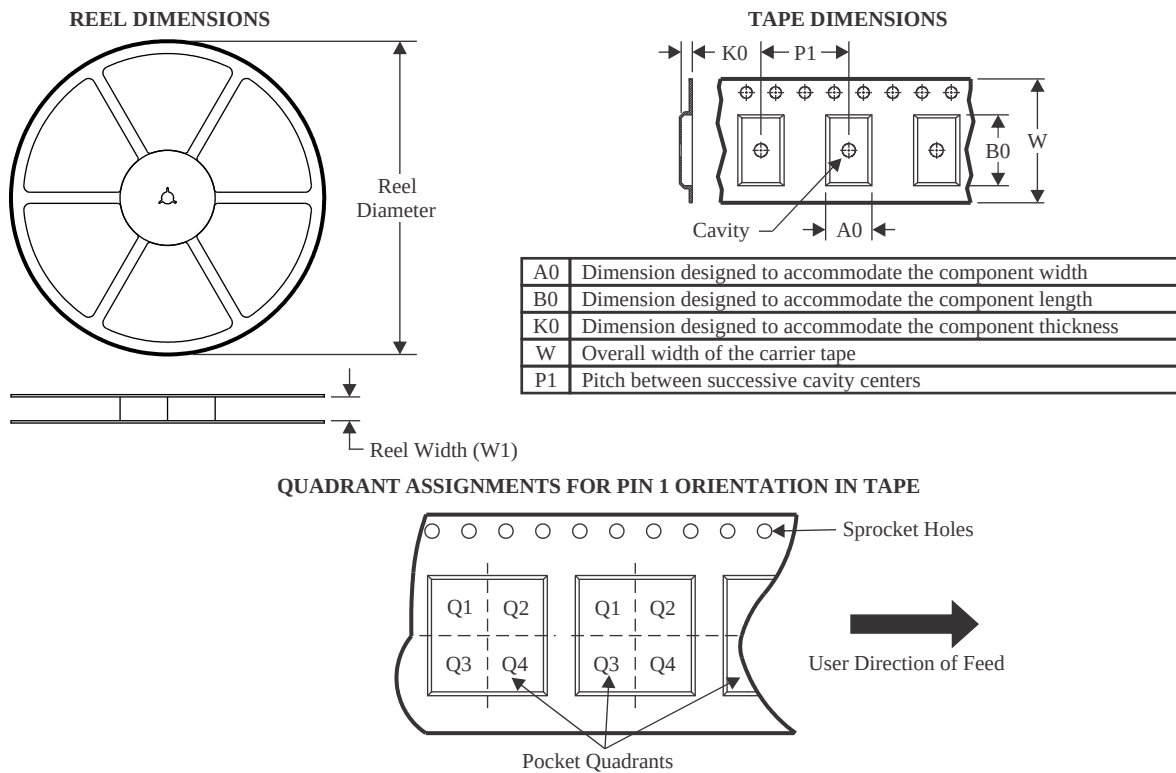
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

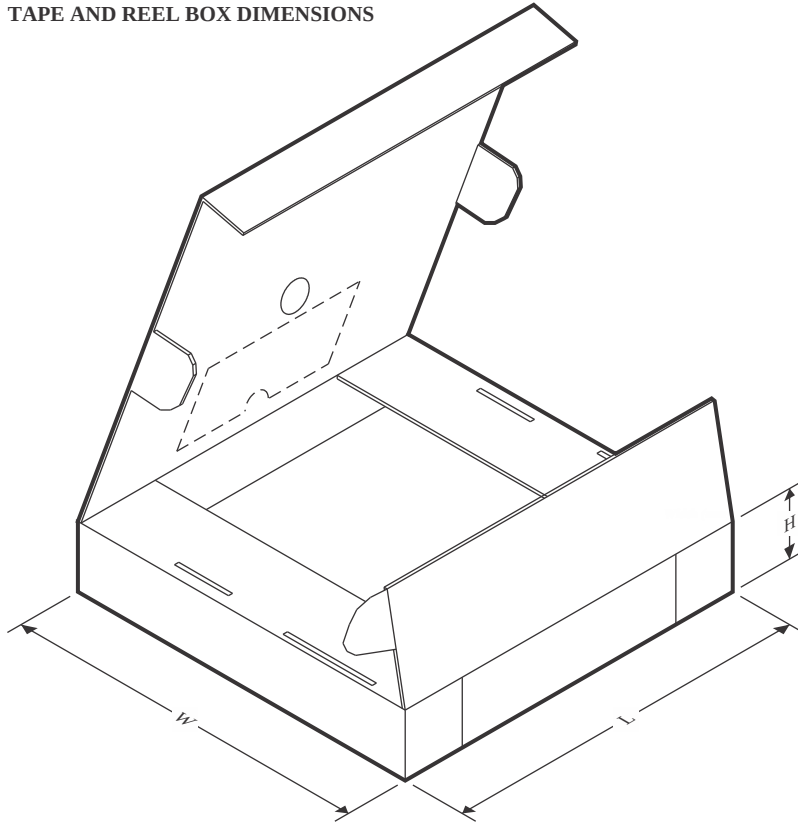
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34LV87TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

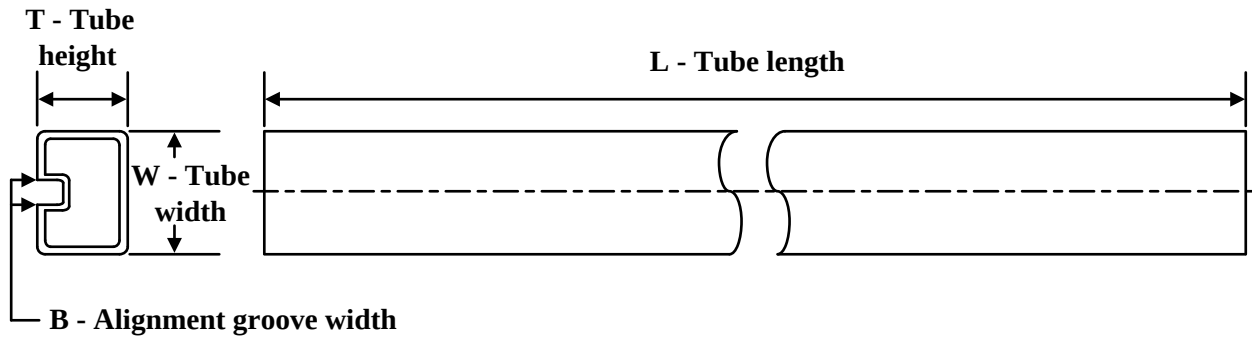
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34LV87TMX/NOPB	SOIC	D	16	2500	356.0	356.0	35.0

TUBE

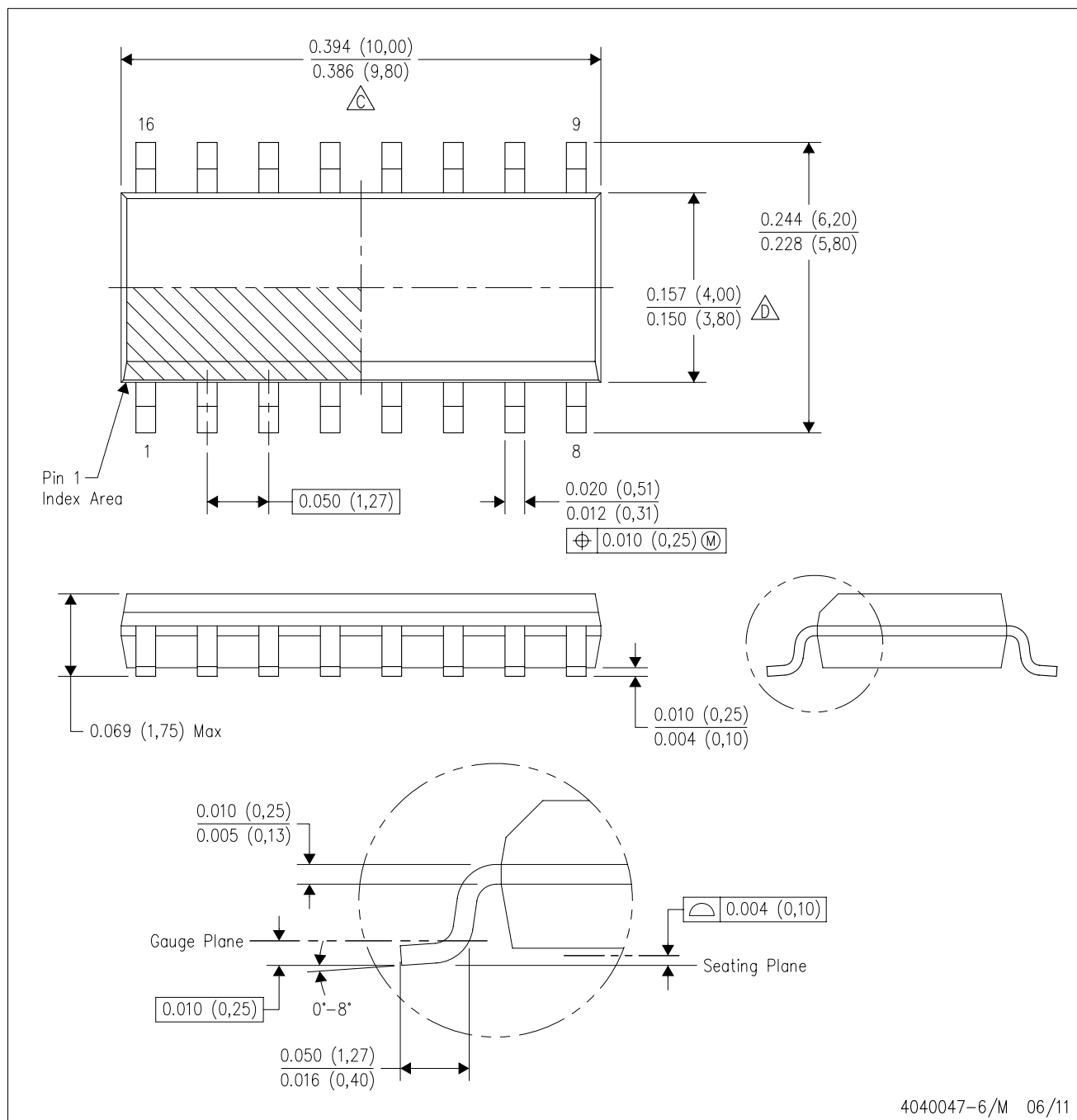


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DS34LV87TM/NOPB	D	SOIC	16	48	495	8	4064	3.05
DS34LV87TM/NOPB.A	D	SOIC	16	48	495	8	4064	3.05

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated