DRV8256E/P H-Bridge Motor Driver With Integrated Current Sense and Smart Tune Technology

1 Features

- N-channel H-bridge motor driver
  - Drives one bidirectional brushed-DC motor
  - Two unidirectional brushed DC motors
- Integrated current sensing and regulation
- 4.5 V to 48 V Operating supply voltage range
- Multiple control interface options
  - PHASE/ENABLE (PH/EN)
  - PWM (IN/IN)
- Smart tune, fast and mixed decay options
- Low $R_{DS(ON)}$: 165 mΩ HS + LS at 24 V, 25°C
- High Output Current Capability: 6.4-A peak
- Limits inrush current of brushed-DC motors
- Configurable Off-Time PWM Chopping
  - 7, 16, 24 or 32 µs
- Supports 1.8 V, 3.3 V, 5.0 V logic inputs
- Low-current sleep mode (2 µA)
- Spread spectrum clocking for low EMI
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Brushed DC Motors
- Printers and scanners
- ATMs and Textile Machines
- Major home appliances
- Vacuum, humanoid, and robotics
- Smart Meters

3 Description

The DRV8256E/P devices are single H-bridge motor drivers for a wide variety of industrial applications. The devices integrate an N-channel H-bridge, charge pump regulator, current sensing and regulation, and protection circuitry.

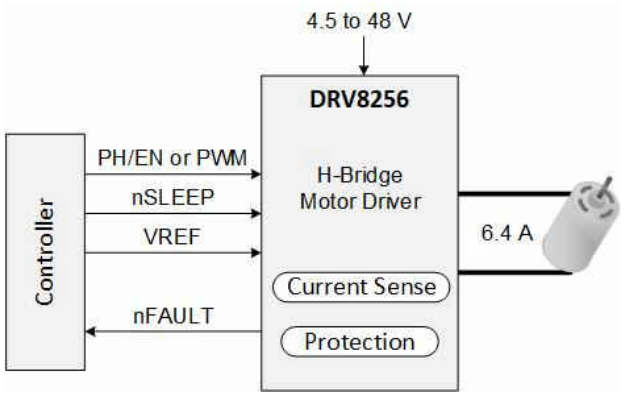
Integrated current sensing allows the driver to regulate the motor inrush current during start up and high load events. A current limit can be set with an adjustable external voltage reference. The integrated current sensing uses an internal current mirror architecture, removing the need for a large power shunt resistor, saving board area and reducing system cost. A low-power sleep mode is provided to achieve ultra-low quiescent current draw by shutting down most of the internal circuitry.

Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output overcurrent (OCP), and device overtemperature (TSD). Fault conditions are indicated on nFAULT.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
DRV8256EPWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8256ERGER	VQFN (24)	4.0mm x 4.0mm
DRV8256PPWPR	HTSSOP (28)	9.7mm x 4.4mm
DRV8256PRGER	VQFN (24)	4.0mm x 4.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DRV8256 Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (June 2021)	Page
• Updated peak current to 6 A	1
• Updated *Current Regulation* section	15
• Updated *Current Regulation* section	27
• Updated *Layout Guidlines* section	31
• Updated drawings in *Layout Example*	31
• Removed one set of QFN package drawings	34

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5 Pin Configuration and Functions

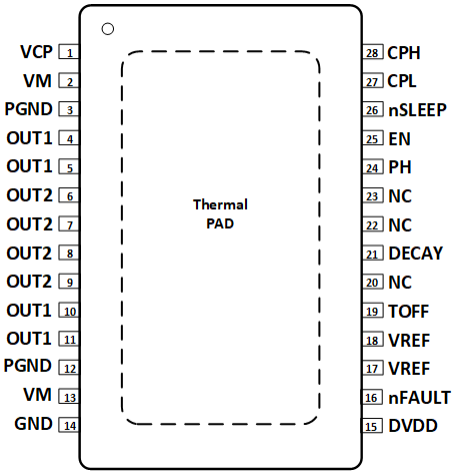

Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View DRV8256E

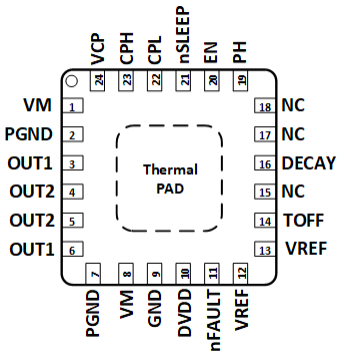

Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View DRV8256E

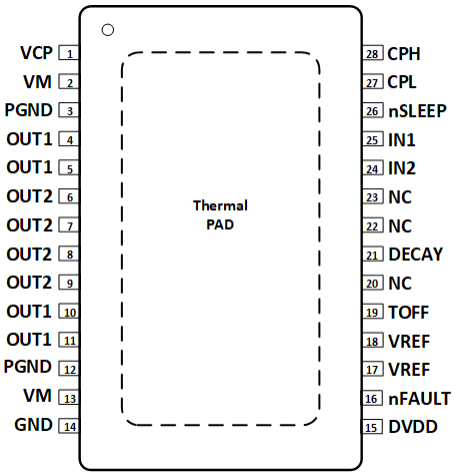

Figure 5-3. PWP PowerPAD™ Package 28-Pin HTSSOP Top View DRV8256P

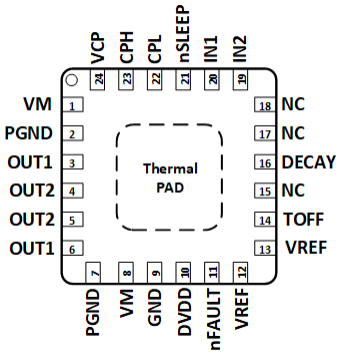

Figure 5-4. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View DRV8256P

Pin Functions

PIN					TYPE	DESCRIPTION
NAME	PWP		RGE			
	DRV8256E	DRV8256P	DRV8256E	DRV8256P		
DECAY	21	21	16	16	I	Decay mode setting pin. Quad-level pin.
EN	25	—	20	—	I	Enable input. Logic high enables bridge; logic low disables the bridge Hi-Z.
IN1	—	25	—	20	I	PWM input. Logic controls the state of H-bridge; internal pulldown.
IN2	—	24	—	19	I	PWM input. Logic controls the state of H-bridge; internal pulldown.
OUT1	4, 5, 10, 11	4, 5, 10, 11	3, 6	3, 6	O	Winding output. Connect to motor winding.
OUT2	6, 7, 8, 9	6, 7, 8, 9	4, 5	4, 5	O	Winding output. Connect to motor winding.
PH	24	—	19	—	I	Phase input. Logic high drives current from OUT1 to OUT2.
VREF	17, 18	17, 18	12, 13	12, 13	I	Reference voltage input pins. Voltage on these pins sets the full scale chopping current in H-bridge. The two pins must be tied together.
NC	20, 22, 23	20, 22, 23	15, 17, 18	15, 17, 18	I	No Connect.
CPH	28	28	23	23	PWR	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	27	22	22		
GND	14	14	9	9	PWR	Device ground. Connect to system ground.
TOFF	19	19	14	14	I	Sets the decay mode off-time during current chopping; quad-level pin. Also sets the ripple current in smart tune ripple control mode.
DVDD	15	15	10	10	PWR	Logic supply voltage. Connect a X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VCP	1	1	24	24	O	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	2, 13	2, 13	1, 8	1, 8	PWR	Power supply. Connect to motor supply voltage and bypass to PGND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
PGND	3, 12	3, 12	2, 7	2, 7	PWR	Power ground. Connect to system ground.
nFAULT	16	16	11	11	O	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.

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PIN					TYPE	DESCRIPTION
NAME	PWP		RGE			
	DRV8256E	DRV8256P	DRV8256E	DRV8256P		
nSLEEP	26	26	21	21	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
PAD	-	-	-	-	-	Thermal pad. Connect to system ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) [(1)]

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (PH, EN, IN1, IN2, nFAULT, DECAY, TOFF)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.75	V
Continuous phase node pin voltage (OUT1, OUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (OUT1, OUT2)	–3	V_{VM} + 3	V
Peak drive current (OUT1, OUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	48	V
V_I	Logic level input voltage	0	5.5	V
V_{REF}	Reference rms voltage range (VREF)	0.05	5	V
f_{PWM}	Applied PWM signal (PH, EN, IN1, IN2)	0	100	kHz
I_{FS}	Peak output current	0	6.4	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC		PWP (HTSSOP) 28 PINS	RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.7	39.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.0	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	16.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.2	15.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	3.4	°C/W

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6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No motor load		4	5.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	120			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to clear fault	20		40	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.8	1.2	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.8	1.2	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 48 V	4.75	5	5.25	V
		No external load, V_{VM} = 4.5V	4.2	4.35		V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	6 V < V_{VM} < 48 V		V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		360		kHz
LOGIC-LEVEL INPUTS (PH, EN, IN1, IN2, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			100	µA
t_{PD}	Propagation delay	PH, EN, INx input to current change		800		ns
QUAD-LEVEL INPUTS (DECAY, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z (>500kΩ to GND)	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage		–1		1	µA
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ONH)}$	High-side FET on resistance	T_J = 25 °C, I_O = -1 A		82	100	mΩ
		T_J = 125 °C, I_O = -1 A		125	150	mΩ
		T_J = 150 °C, I_O = -1 A		140	175	mΩ
$R_{DS(ONL)}$	Low-side FET on resistance	T_J = 25 °C, I_O = 1 A		82	100	mΩ
		T_J = 125 °C, I_O = 1 A		125	150	mΩ
		T_J = 150 °C, I_O = 1 A		140	175	mΩ
t_{SR}	Output slew rate	VM = 24V, I_O = 1 A, Between 10% and 90%		240		V/µs
CURRENT REGULATION (VREF)						
I_{VREF}	VREF Leakage Current	VREF = 3.3 V			8.25	µA

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Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		
ΔI_{TRIP}	I_{TRIP} Current Accuracy	0.5 A < I_{TRIP} < 1 A	-12		12	%
		1 A < I_{TRIP} < 2 A	-6		6	
		2 A < I_{TRIP} < 5 A	-4		4	
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.1	4.25	4.35	V
		VM rising, UVLO rising	4.2	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	8			A
t_{OCP}	Overcurrent deglitch time			2		µs
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.5.1 Typical Characteristics

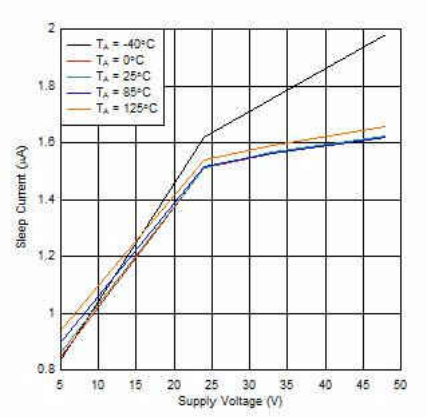

Figure 6-1. Sleep Current over Supply Voltage

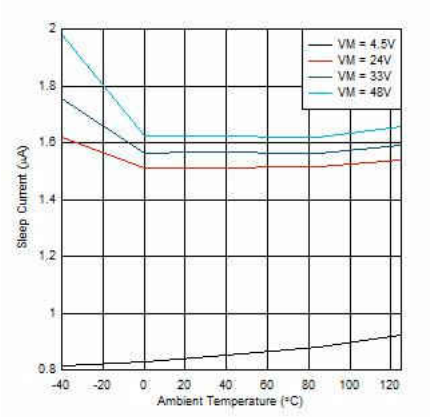

Figure 6-2. Sleep Current over Temperature

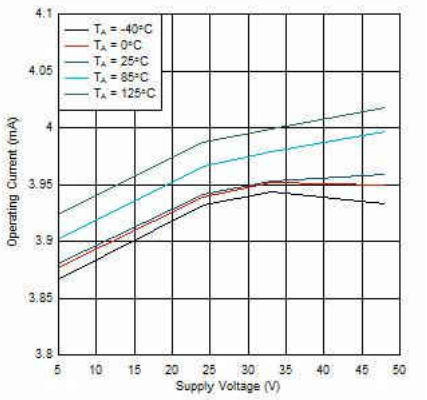

Figure 6-3. Operating Current over Supply Voltage

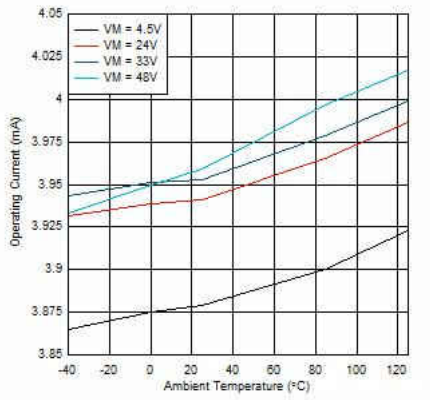

Figure 6-4. Operating Current over Temperature

6.5.1 Typical Characteristics (continued)

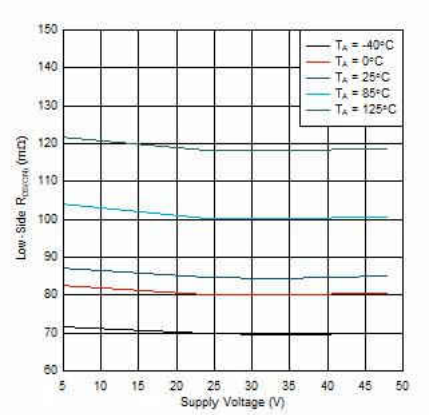

Figure 6-5. Low-Side $R_{DS(ON)}$ over Supply Voltage

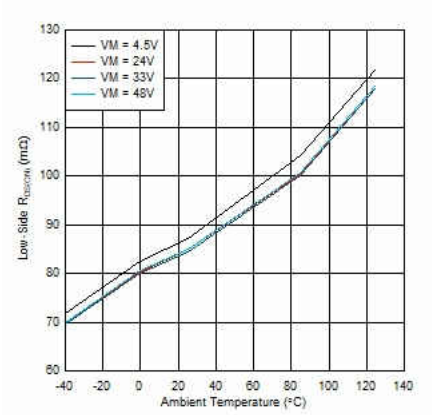

Figure 6-6. Low-Side $R_{DS(ON)}$ over Temperature

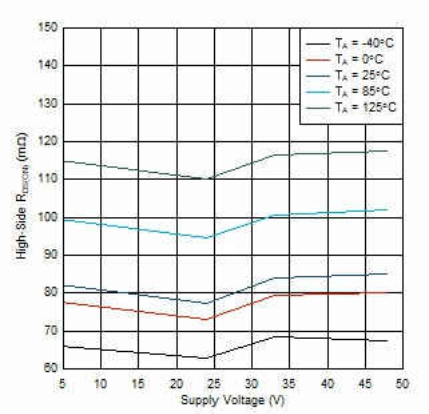

Figure 6-7. High-Side $R_{DS(ON)}$ over Supply Voltage

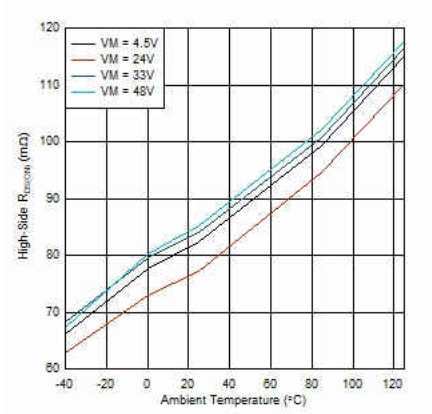

Figure 6-8. High-Side $R_{DS(ON)}$ over Temperature

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7 Detailed Description

7.1 Overview

The DRV8256E/P devices are brushed DC motor drivers that operate from 4.5 V to 48 V supporting a wide range of output load currents for various types of motors and loads. The devices integrate an H-bridge output power stage and a charge pump regulator to support more efficient high-side N-channel MOSFETs. The devices operate off a single power supply input (VM) which can be directly connected to a battery or DC voltage supply. The nSLEEP pin provides an ultra low power mode to minimize current draw during system inactivity.

The devices also integrate current sensing using current mirrors on the low-side power MOSFETs. The integrated current sensing allows the devices to limit the output current with a fixed off-time PWM chopping scheme. The integrated current sensing out performs traditional external shunt resistor sensing by removing the need for an external power shunt resistor. The off-time PWM current regulation level can be configured during motor operation through the VREF pin to limit the load current accordingly to the system demands. The current regulation is highly configurable, with several decay modes of operation. The PWM off-time, t_{OFF}, can be adjusted to 7, 16, 24, or 32 µs.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), charge pump undervoltage (CPUV), overcurrent protection (OCP), and overtemperature shutdown (TSD). Fault conditions are indicated on the nFAULT pin.

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7.2 Functional Block Diagrams

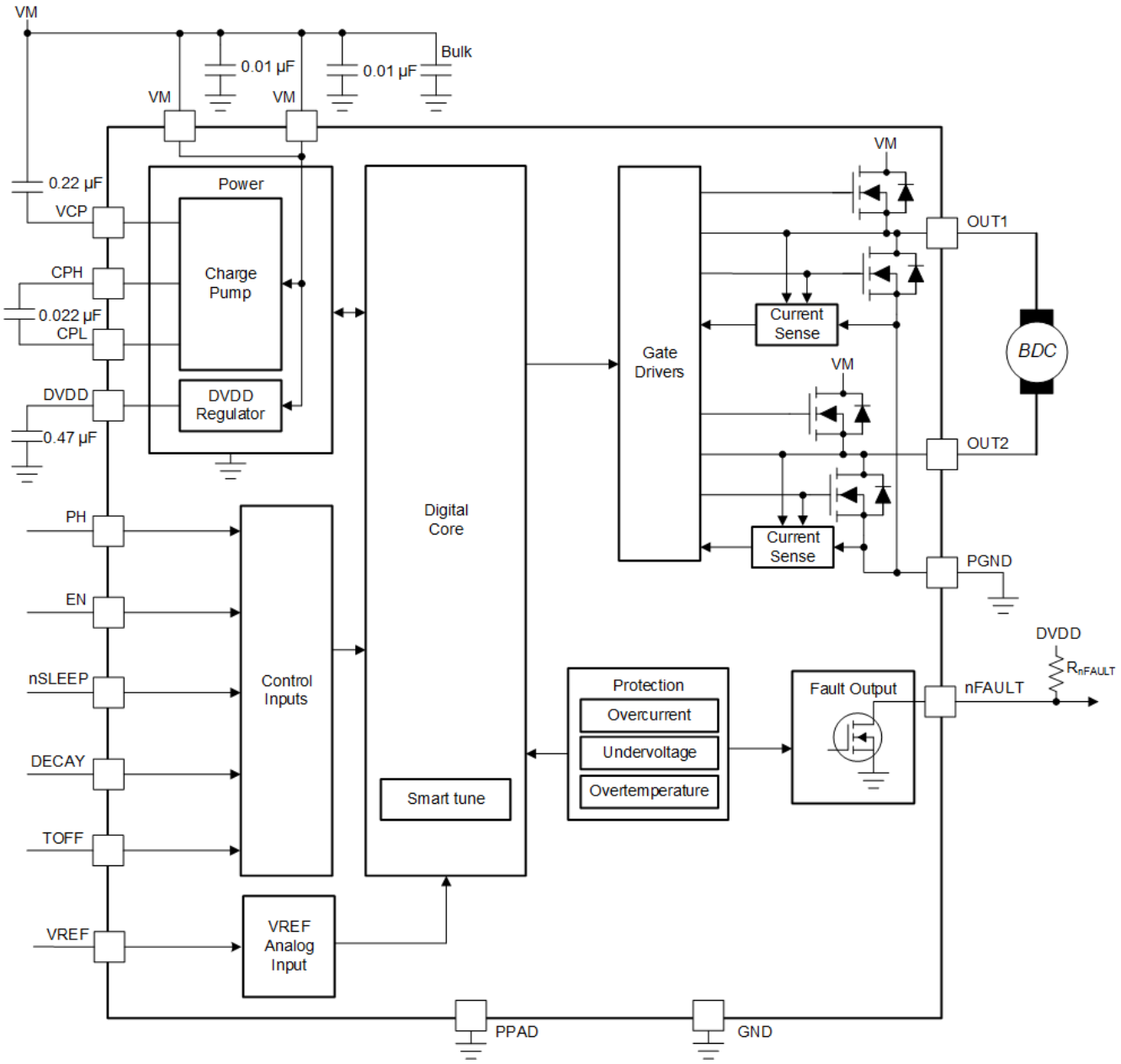

Figure 7-1. DRV8256E Block Diagram

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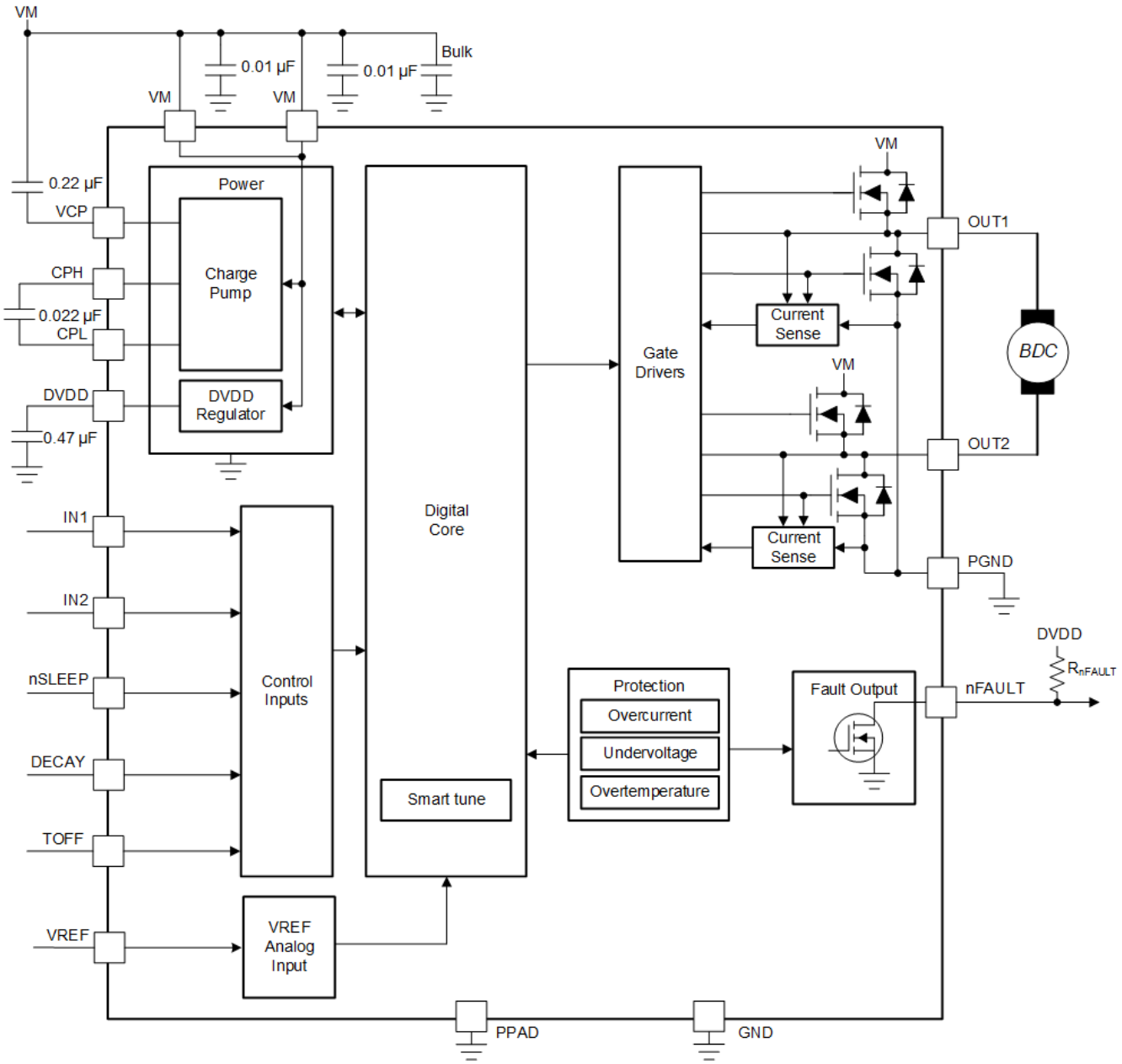

Figure 7-2. DRV8256P Block Diagram

7.3 Feature Description

The following table shows the recommended values of the external components for the driver.

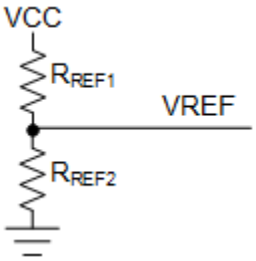

Figure 7-3. Resistor divider connected to the VREF pins

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	PGND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{nFAULT}	VCC	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREF	GND	

VCC is not a pin on the device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD.

7.3.1 Bridge Control

The DRV8256E is controlled using a PH/EN interface. Table 7-2 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8256E. Positive current is defined in the direction of OUT1 to OUT2.

Table 7-2. DRV8256E (PH/EN) Control Interface

nSLEEP	EN	PH	OUT1	OUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	X	Hi-Z	Hi-Z	H-bridge disabled Hi-Z
1	1	0	L	H	Reverse (current OUT2 to OUT1)
1	1	1	H	L	Forward (current OUT1 to OUT2)

The DRV8256P is controlled using a PWM interface. Table 7-3 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8256P. Positive current is defined in the direction of OUT1 to OUT2.

Table 7-3. DRV8256P (PWM) Control Interface

nSLEEP	IN1	IN2	OUT1	OUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	0	L	L	Brake; low-side slow decay
1	0	1	L	H	Reverse (current OUT2 to OUT1)
1	1	0	H	L	Forward (current OUT1 to OUT2)
1	1	1	H	H	Brake; high-side slow decay

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7.3.2 Current Regulation

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle. The current is measured by an internal current mirror architecture that removes the needs for an external power sense resistor.

When the voltage on the VREF pin does not exceed 3.3 V, the ITRIP current (I_{TRIP}) can be calculated as I_{TRIP} (A) = V_{REFx} (V) / 0.66 (V/A).

When the VREF voltage exceeds 3.3V, the ITRIP current does not have a linear relation with the VREF voltage. When VREF is tied to DVDD or an external 5 V, the device can deliver maximum 6.4 A peak current. However, the thermal performance of the device must be carefully considered - heat sinks might be required to drive more than 5 A peak current.

Table 7-4. Off-Time Settings

TOFF	OFF-TIME t_{OFF}
0	7 µs
1	16 µs
Hi-Z	24 µs
330kΩ to GND	32 µs

7.3.3 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-4, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 7-4, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7-4, Item 3.

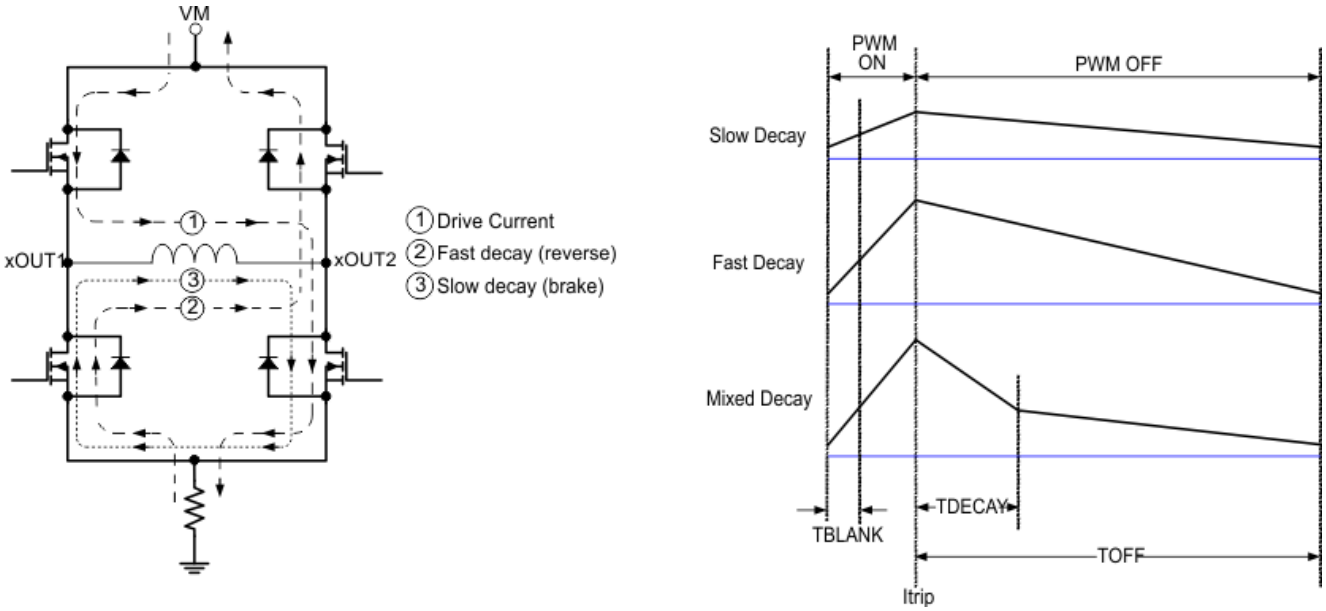

Figure 7-4. Decay Modes

The decay mode is selected by setting the quad-level DECAY pin as shown in Table 7-5.

Table 7-5. Decay Mode Settings

DECAY	DECAY MODE
0	Smart tune Dynamic Decay
1	Smart tune Ripple Control
Hi-Z	Mixed decay: 30% fast
330k to GND	Fast decay

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7.3.3.1 Mixed Decay

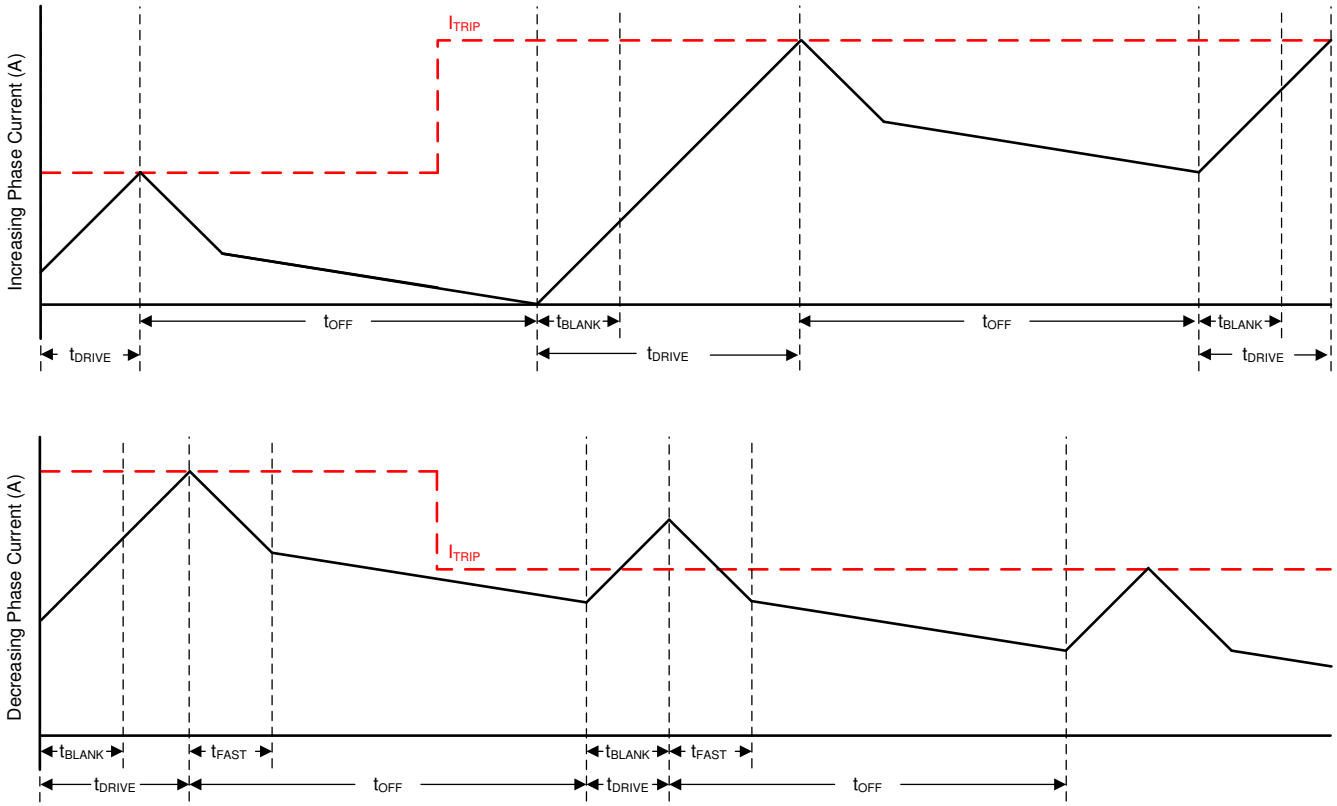

Figure 7-5. Mixed Decay Mode

Mixed decay begins as fast decay for 30% of t_{OFF}, followed by slow decay for the remainder of t_{OFF}.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.3.2 Fast Decay

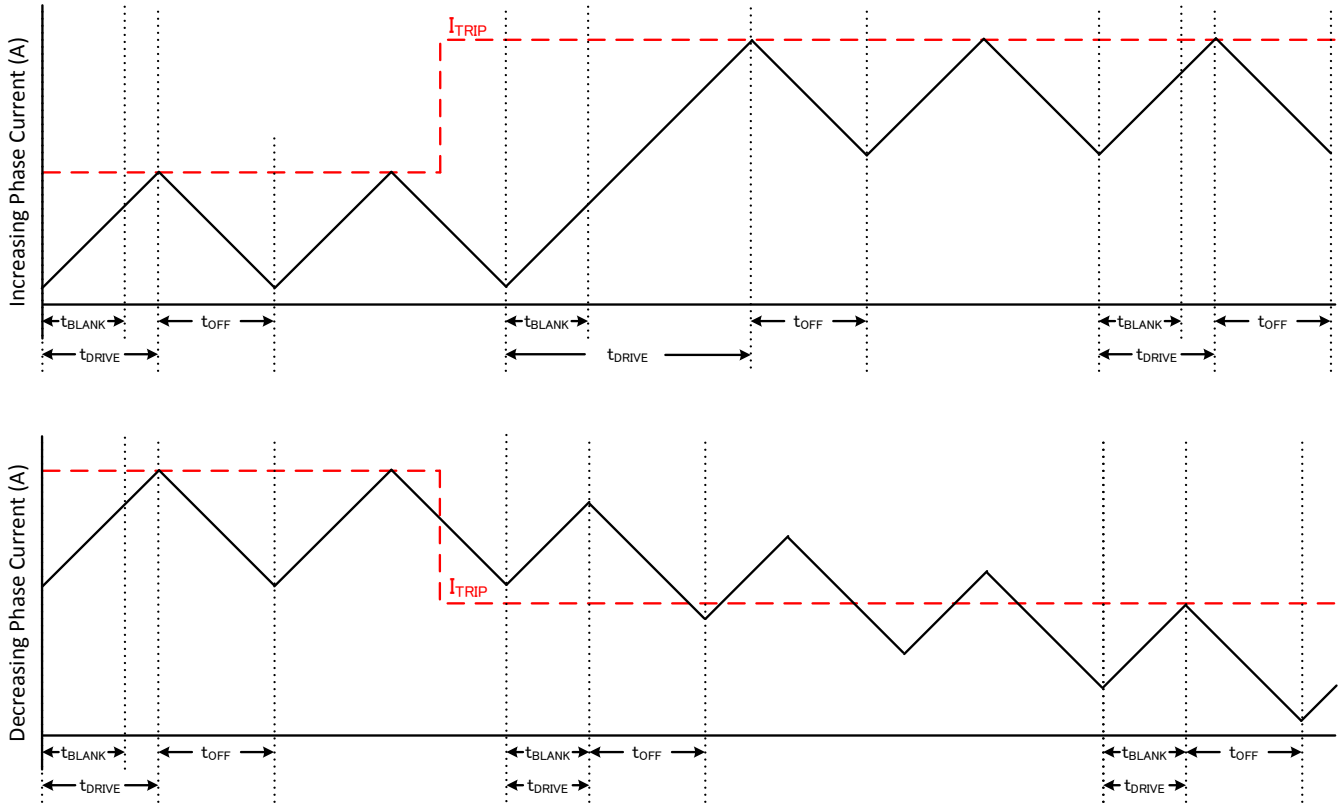

Figure 7-6. Fast/Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

7.3.3.3 Smart tune Dynamic Decay

The smart tune current regulation scheme is an advanced current-regulation control method compared to traditional fixed off-time current regulation schemes. Smart tune current regulation scheme helps the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Low-current versus high-current dI/dt

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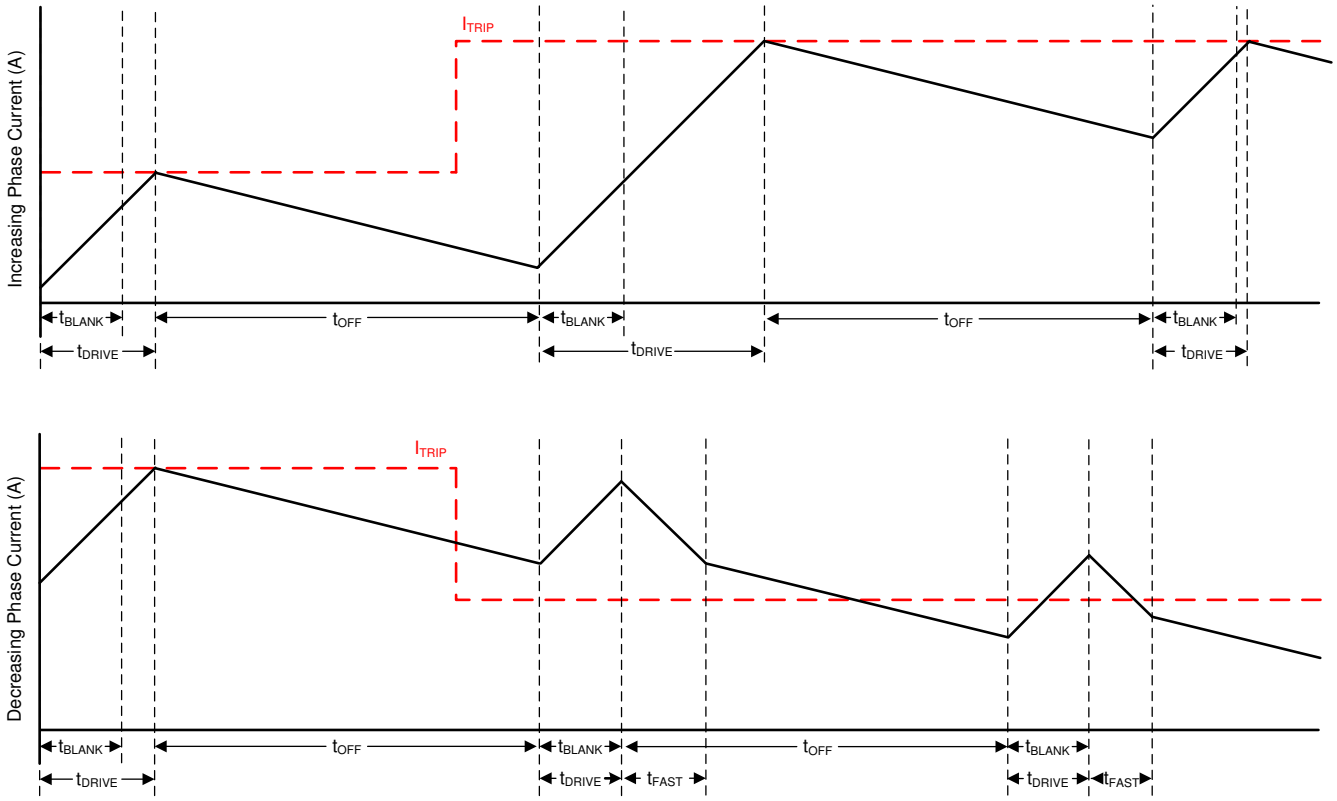

Figure 7-7. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

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7.3.3.4 Smart tune Ripple Control

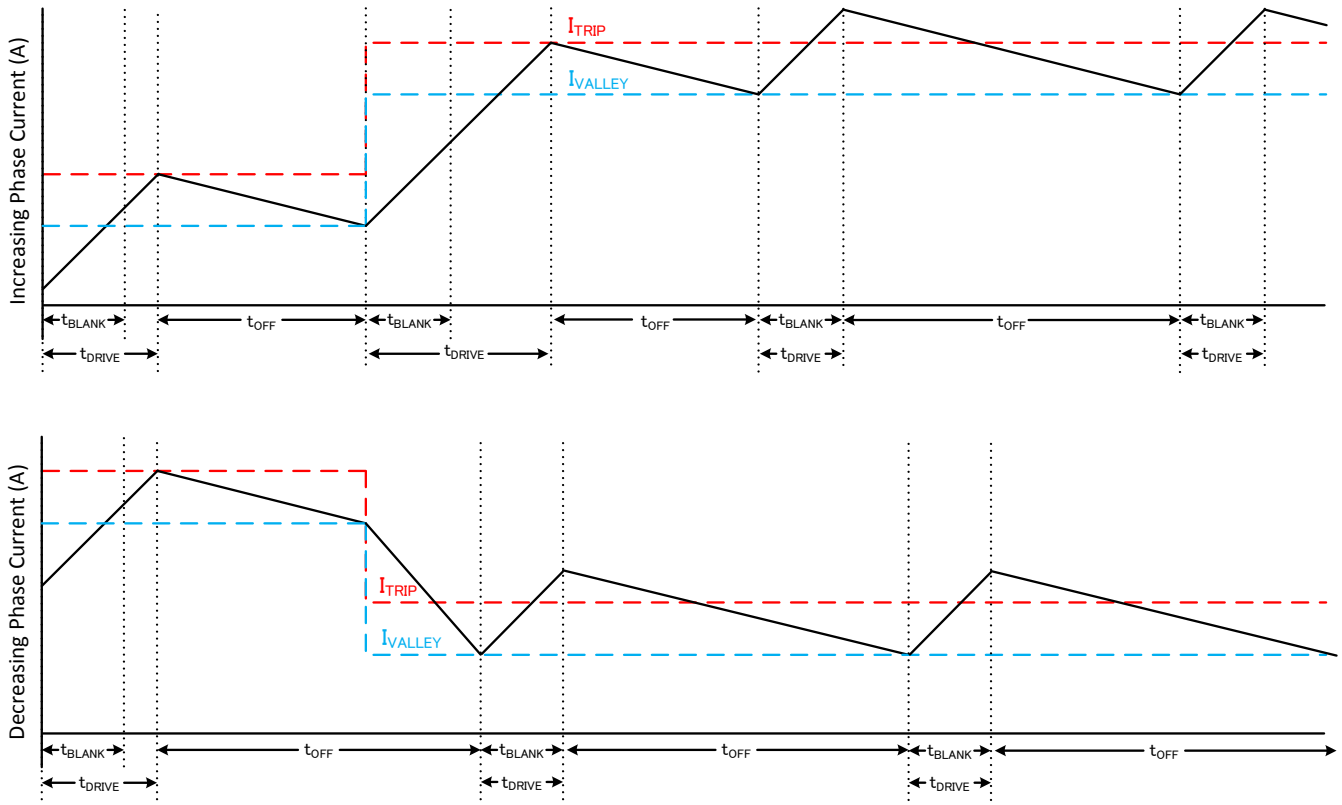

Figure 7-8. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

7.3.3.5 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 1 µs.

7.3.4 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

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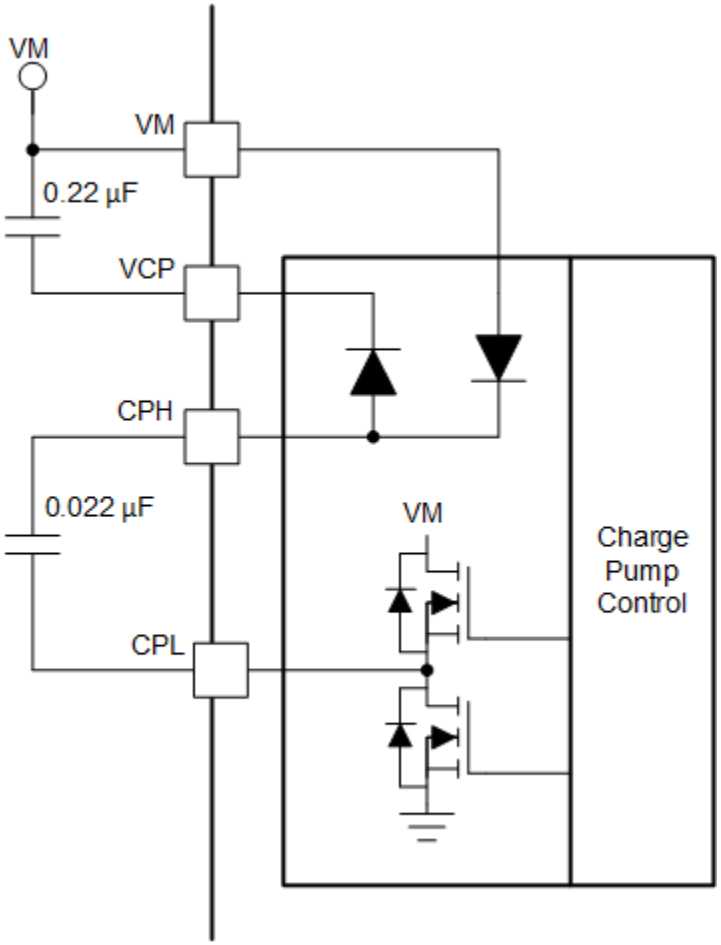

Figure 7-9. Charge Pump Block Diagram

7.3.5 Linear Voltage Regulators

A linear voltage regulator is integrated in the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

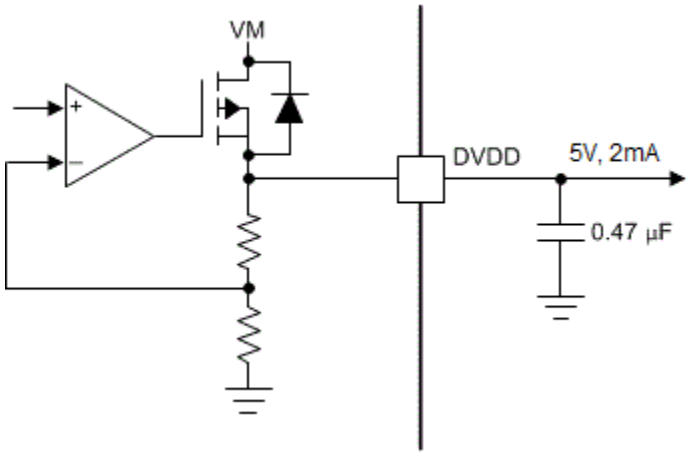

Figure 7-10. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, DECAY or TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

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7.3.6 Logic and Quad-Level Pin Diagrams

Figure 7-11 gives the input structure for logic-level pins PH, EN, IN1, IN2 and nSLEEP:

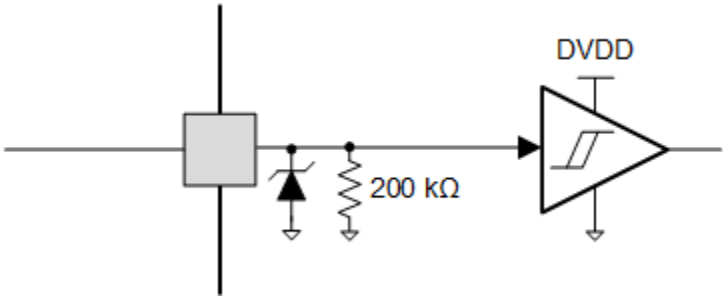

Figure 7-11. Logic-level Input Pin Diagram

Quad-level logic pins TOFF and DECAY have the following structure as shown in Figure 7-12.

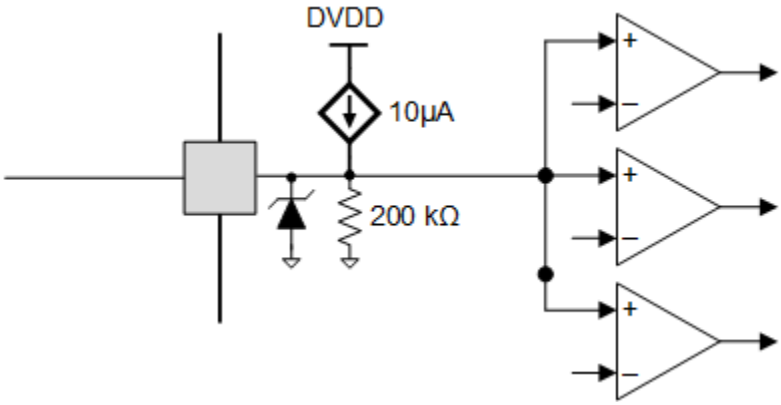

Figure 7-12. Quad-Level Input Pin Diagram

7.3.6.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V, 3.3-V or 1.8-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V or 1.8-V pullup, an external supply must be used.

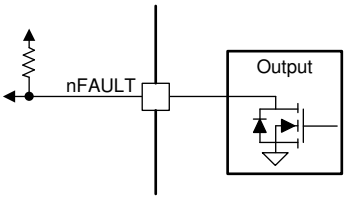

Figure 7-13. nFAULT Pin

7.3.7 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.7.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition.

Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

7.3.7.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.3.7.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the H-bridge is disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. Once the OCP condition is removed, normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

7.3.7.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. After the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS_OTSD}$), normal operation resumes after applying an nSLEEP reset pulse or a power cycling.

Fault Condition Summary

Table 7-6. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	nFAULT	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
CP undervoltage (CPUV)	VCP < V_{CPUV}	nFAULT	Disabled	Operating	Operating	VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	nFAULT	Disabled	Operating	Operating	Latched
Thermal Shutdown (OTSD)	T_J > T_{TSD}	nFAULT	Disabled	Disabled	Operating	Latched

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The state of the device is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.3 nSLEEP Reset Pulse

A latched fault can be cleared through a quick nSLEEP pulse. This pulse width must be greater than 20 µs and shorter than 40 µs. If nSLEEP is low for longer than 40 µs, but less than 120 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see Figure 7-14). This reset pulse does not affect the status of the charge pump or other functional blocks.

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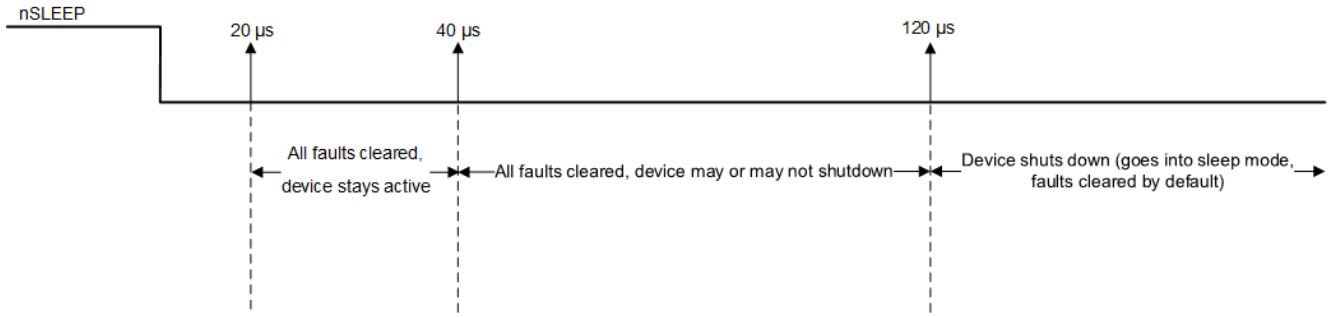

Figure 7-14. nSLEEP Reset Pulse

Functional Modes Summary

Table 7-7 lists a summary of the functional modes.

Table 7-7. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 48 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled
Operating	4.5 V < VM < 48 V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8256E/P devices can be used in a variety of applications that require a H-bridge power stage configuration. Common application examples include brushed DC motors. The application examples below will highlight how to use the device in bidirectional current control applications requiring an H-bridge driver.

8.2 Typical Application

In this application example, the device is configured to drive a bidirectional current through a brushed DC motor using an H-bridge configuration. The H-bridge polarity and duty cycle are controlled with a PWM and IO resource from the external controller to the IN1 and IN2 pins. The current limit threshold (I_{TRIP}) is generated with a resistor divider from the VREF pin. The device is configured for the smart tune ripple control decay by tying the DECAY pin to DVDD.

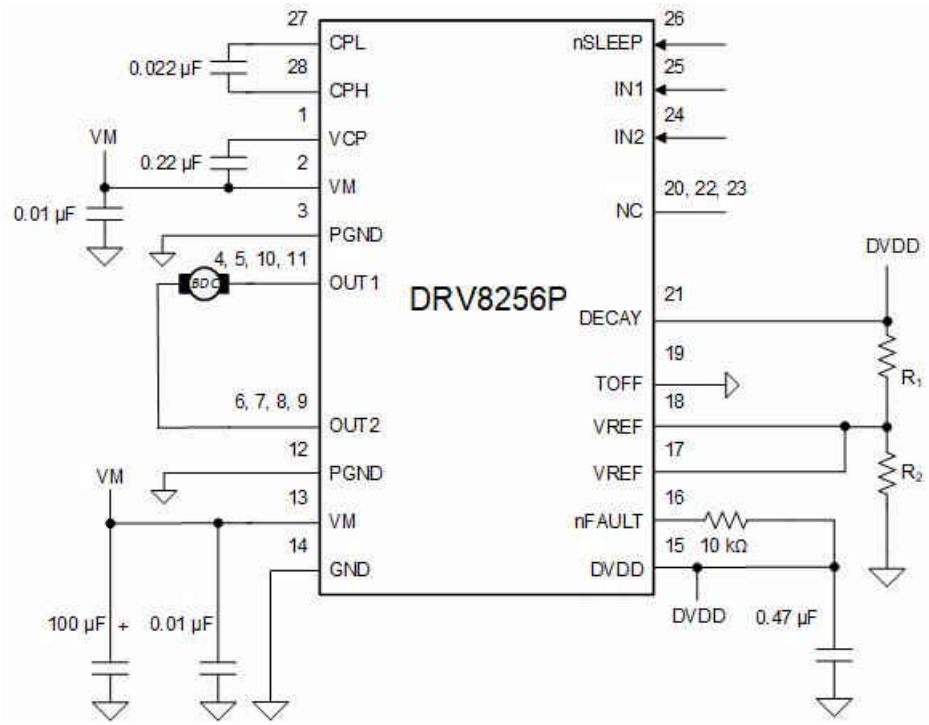

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1 lists the design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply Voltage	VM	24 V
Output RMS Current	I_{RMS}	3.5 A
Current Regulation Trip Point	I_{TRIP}	4 A

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Table 8-1. Design Parameters (continued)

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Switching Frequency	f_{PWM}	35 kHz
Ambient Temperature	T_A	25 °C

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

The output current regulation trip point (I_{TRIP}) is configured with the voltage on VREF pin. If VREF does not exceed 3.3 V, VREF = I_{TRIP} x 0.66 V/A. If I_{TRIP} is 4 A, then VREF should be set to 2.64 V. When VREF exceeds 3.3 V, the device can deliver even higher peak current - up to 6.4 A when VREF is at 5 V. VREF can be generated with a simple resistor divider from the DVDD.

8.2.2.1.1 Power Dissipation and Thermal Calculation

The output current and power dissipation capabilities of the device are heavily dependent on the PCB design and external system conditions. This section provides some guidelines for calculating these values.

Total power dissipation (P_{TOT}) for the device is composed of three main components. These are the power MOSFET $R_{DS(ON)}$ (conduction) losses, the power MOSFET switching losses and the quiescent supply current dissipation. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

$P_{TOT} = P_{COND} + P_{SW} + P_Q$

P_{COND} can be calculated from the device $R_{DS(ON)}$ and average output current (I_{RMS}).

$P_{COND} = (I_{RMS})^2 \times (R_{DS(ONH)} + R_{DS(ONL)})$

It should be noted that $R_{DS(ON)}$ has a strong correlation with the device temperature. A curve showing the normalized $R_{DS(ON)}$ with temperature can be found in the Typical Characteristics curves.

$P_{COND} = (3.5\text{-A})^2 \times (0.082\text{-}\Omega + 0.082\text{-}\Omega) = 2.009\text{-W}$

P_{SW} can be calculated from the nominal supply voltage (VM), average output current (I_{RMS}), switching frequency (f_{PWM}) and the device output rise (t_{RISE}) and fall (t_{FALL}) time specifications.

$P_{SW} = P_{SW_RISE} + P_{SW_FALL}$

$P_{SW_RISE} = 0.5 \times VM \times I_{RMS} \times t_{RISE} \times f_{PWM}$

$P_{SW_FALL} = 0.5 \times VM \times I_{RMS} \times t_{FALL} \times f_{PWM}$

$P_{SW_RISE} = 0.5 \times 24\text{ V} \times 3.5\text{ A} \times 100\text{ ns} \times 35\text{ kHz} = 0.147\text{ W}$

$P_{SW_FALL} = 0.5 \times 24\text{ V} \times 3.5\text{ A} \times 100\text{ ns} \times 35\text{ kHz} = 0.147\text{ W}$

$P_{SW} = 0.147\text{ W} + 0.147\text{ W} = 0.294\text{ W}$

P_Q can be calculated from the nominal supply voltage (VM) and the I_{VM} current specification.

$P_Q = VM \times I_{VM} = 24\text{ V} \times 4\text{ mA} = 0.096\text{ W}$

The total power dissipation (P_{TOT}) is calculated as the sum of conduction loss, switching loss and the quiescent power loss.

$P_{TOT} = P_{COND} + P_{SW} + P_Q = 2.009\text{-W} + 0.294\text{-W} + 0.096\text{-W} = 2.399\text{-W}$

For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as

$T_J = T_A + (P_{TOT} \times R_{\theta JA})$

Considering a JEDEC standard 4-layer PCB, the junction-to-ambient thermal resistance ($R_{\theta JA}$) is 29.7 °C/W for the HTSSOP package and 39 °C/W for the VQFN package.

Assuming 25°C ambient temperature, the junction temperature for the HTSSOP package is calculated as -

T_J = 25°C + (2.399-W x 29.7 °C/W) = 96.25 °C

The junction temperature for the VQFN package is calculated as -

TJ = 25°C + (2.399-W x 39 °C/W) = 118.56 °C

It should be ensured that the device junction temperature is within the specified operating region.

8.2.2.1.2 Application Curves

CH3 = VM (10V/div), CH1 = nFAULT (3V/div), CH5 = nSLEEP (3V/div), CH7 = I_{OUT} (4 A/div)

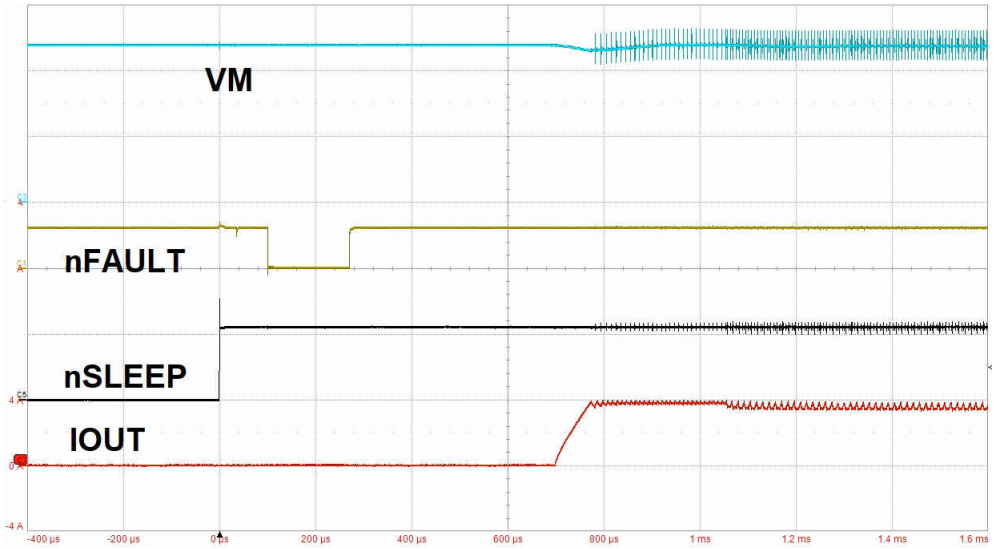

Figure 8-2. Device Power-up with nSLEEP

CH3 = VM (10V/div), CH1 = nFAULT (3V/div), CH5 = nSLEEP (3V/div), CH7 = I_{OUT} (4 A/div)

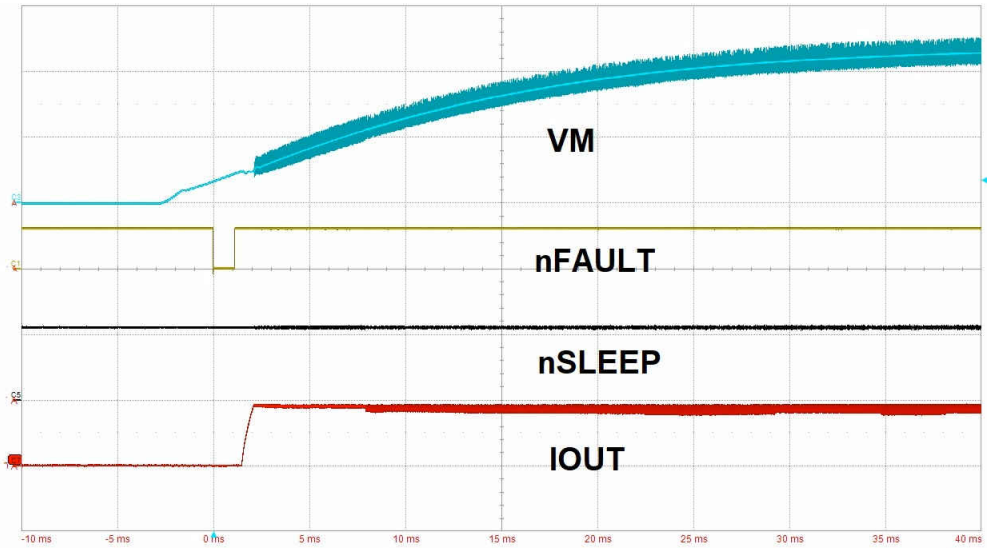

Figure 8-3. Device Power-up with Supply Voltage (VM) Ramp

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CH1 = IN1 (3V/div), CH7 = I_{RMS} (2 A/div), CH3 = OUT1 (24V/div), CH2 = OUT2 (24V/div)

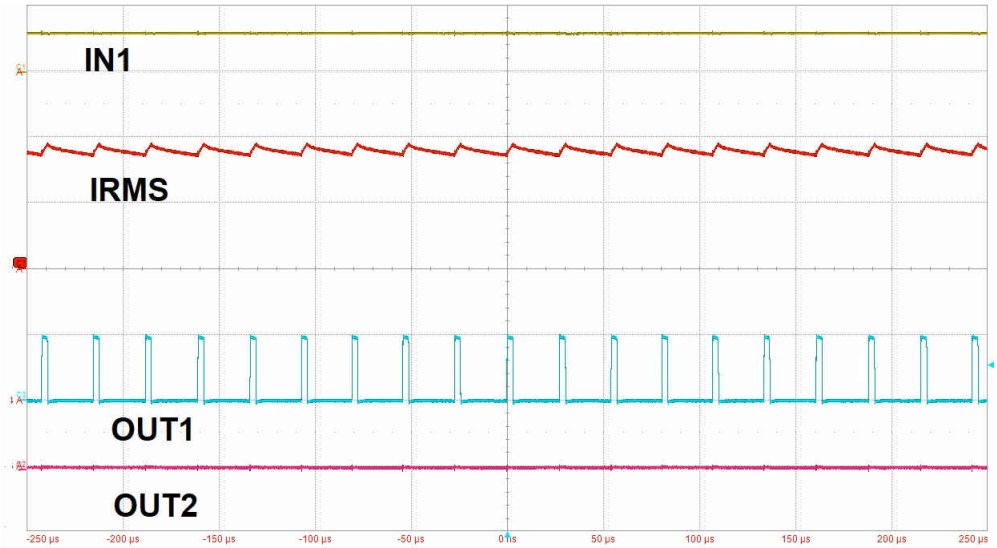

Figure 8-4. Driver Full On Operation with Current Regulation

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 48 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

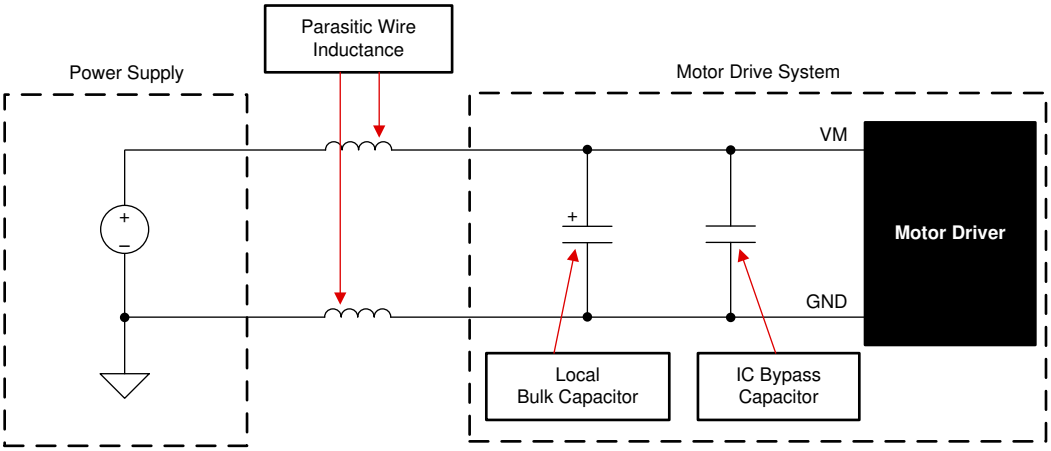

Figure 9-1. Setup of Motor Drive System With External Power Supply

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10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to PGND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device PGND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

The OUT1 pins (pins 4, 5, 10, 11 for HTSSOP package; pins 3, 6 for QFN package) must be connected together using a thick PCB trace. Similarly, the OUT2 pins (pins 6, 7, 8, 9 for HTSSOP package; pins 4, 5 for QFN package) must be connected together using a thick PCB trace.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground. To drive more than 5A peak current, a heat sink might be required to be placed near the device.

10.2 Layout Example

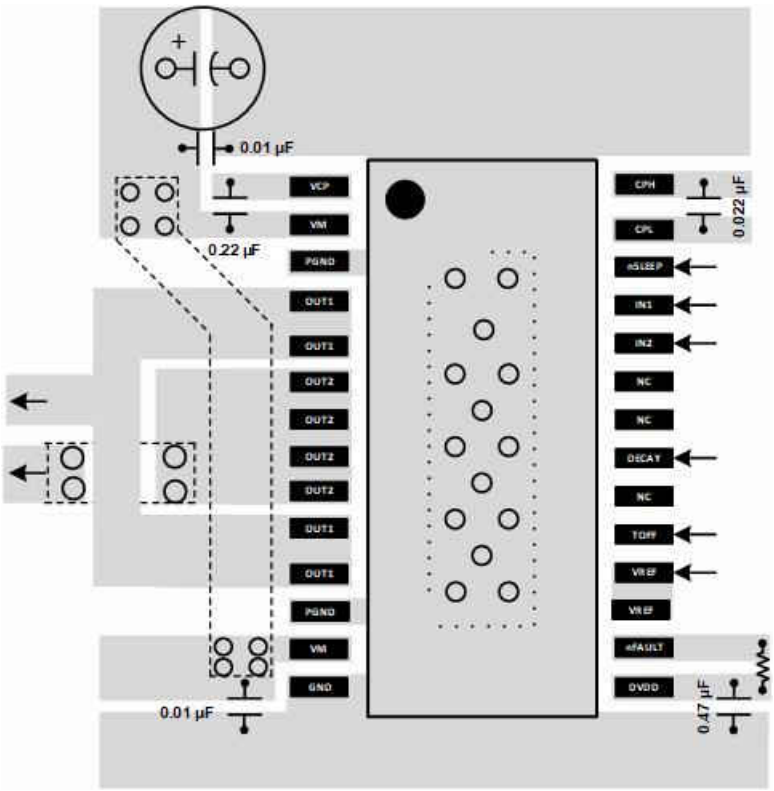

Figure 10-1. HTSSOP Layout Example

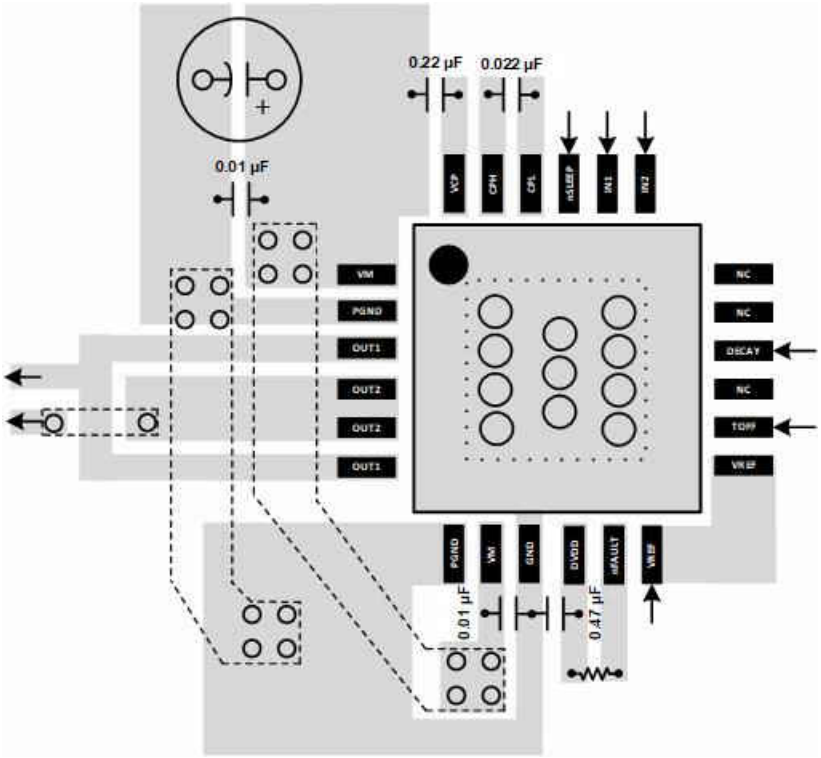

Figure 10-2. QFN Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *High Resolution Microstepping Driver With the DRV88xx Series* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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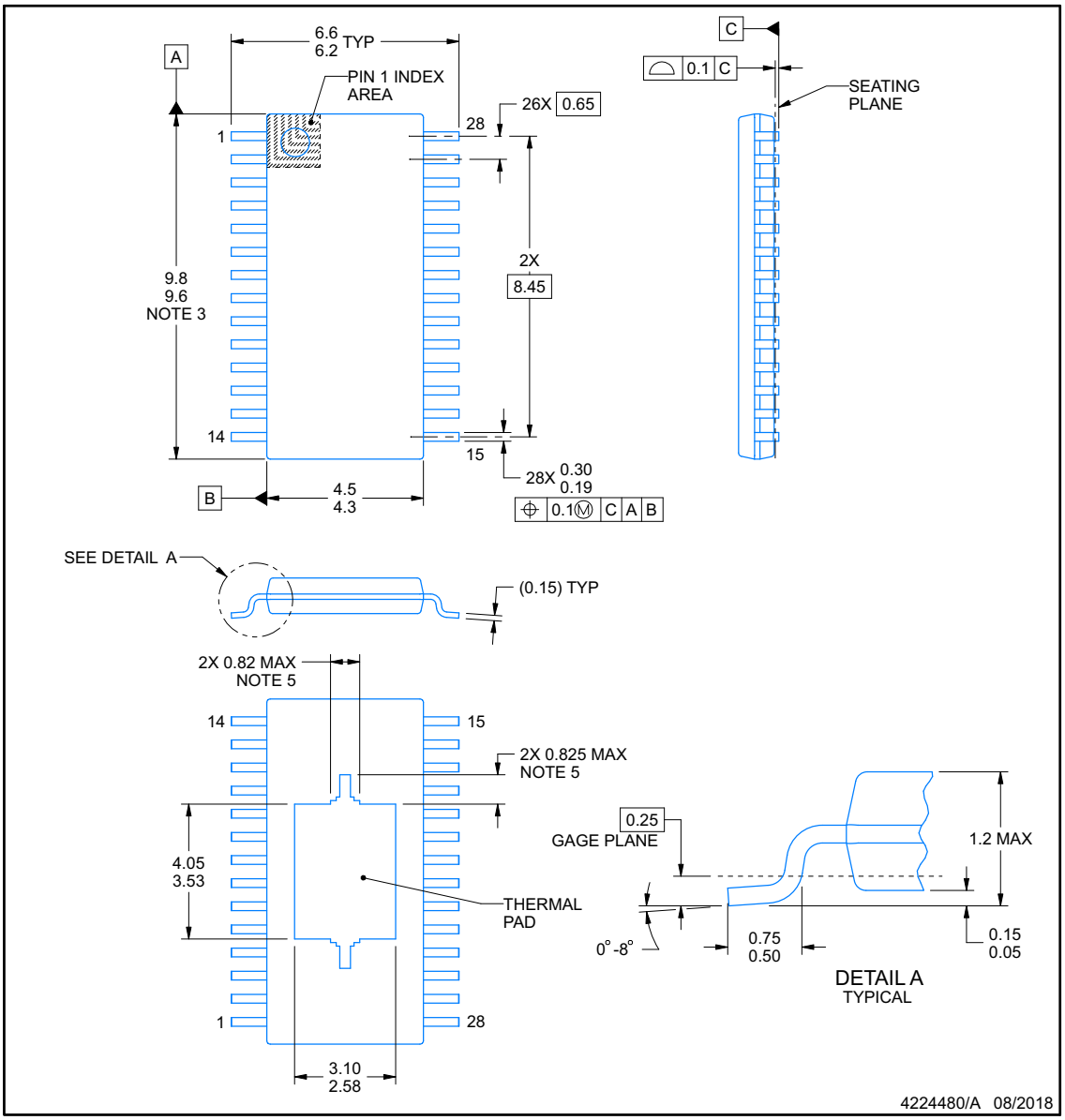
PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

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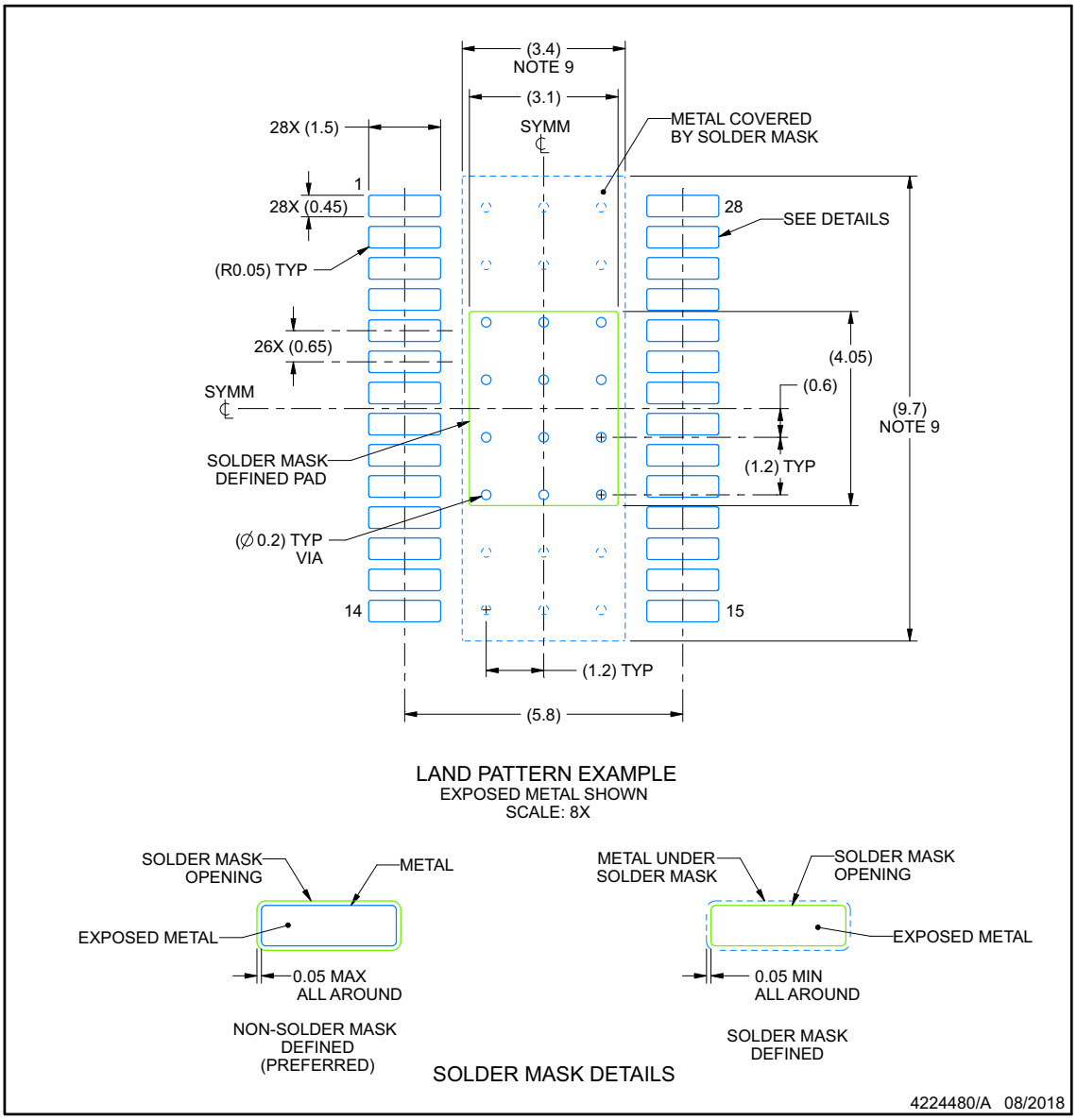
EXAMPLE BOARD LAYOUT

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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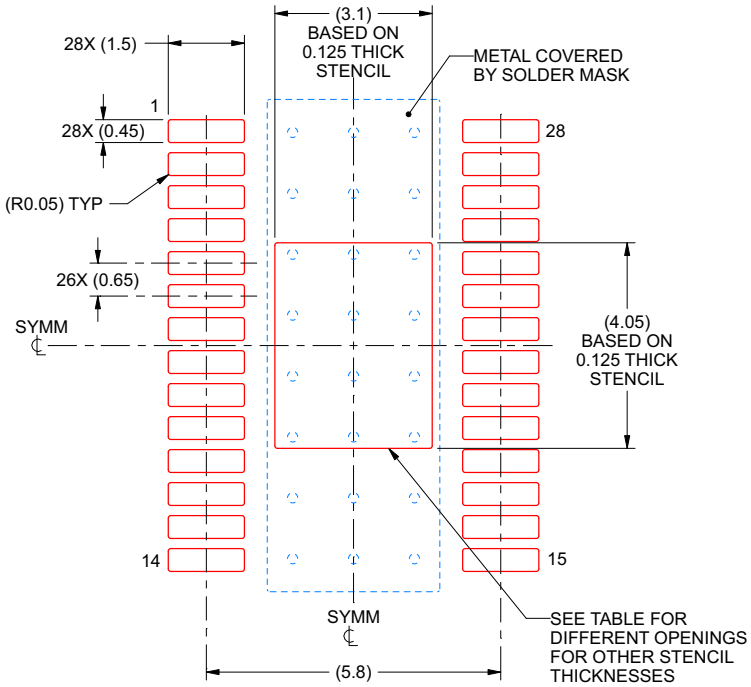
EXAMPLE STENCIL DESIGN

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8256EPWPR	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8256E
DRV8256EPWPR.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8256E
DRV8256ERGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8256E
DRV8256ERGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8256E
DRV8256PPWPR	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8256P
DRV8256PPWPR.A	Active	Production	HTSSOP (PWP) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8256P
DRV8256PRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8256P
DRV8256PRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8256P
DRV8256PRGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8256P
DRV8256PRGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8256P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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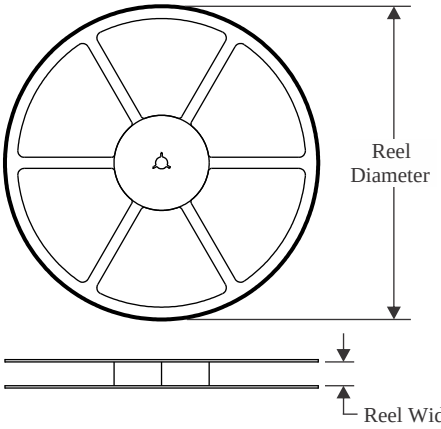
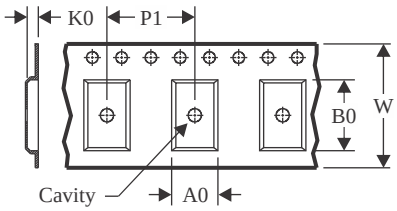
TAPE AND REEL INFORMATION

REEL DIMENSIONS

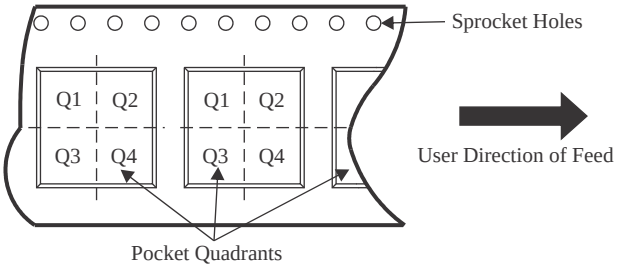


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

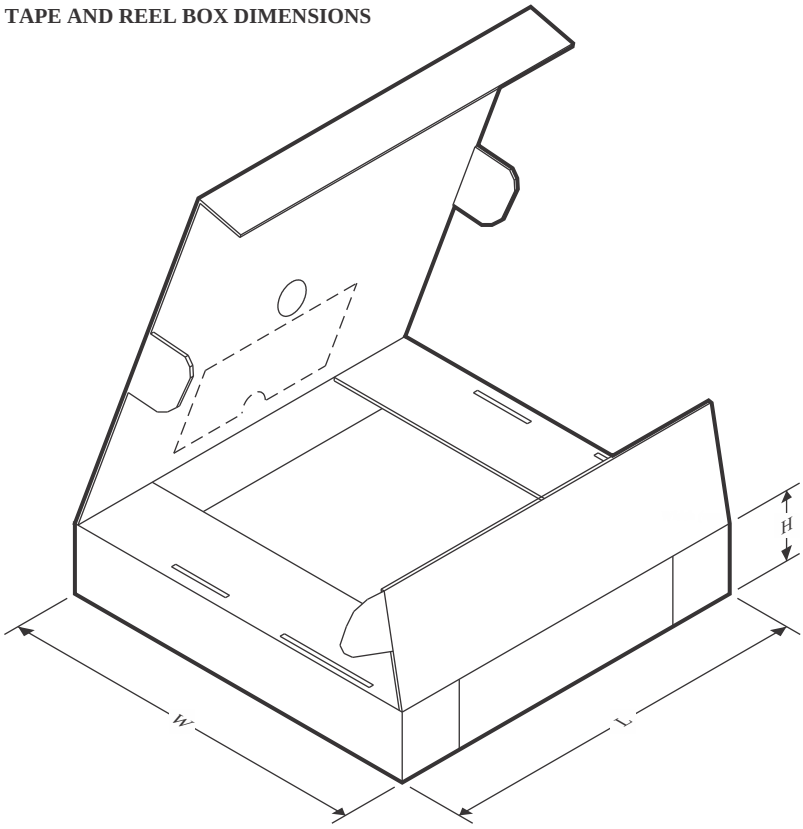
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8256EPWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
DRV8256ERGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8256PPWPR	HTSSOP	PWP	28	2500	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
DRV8256PRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
DRV8256PRGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

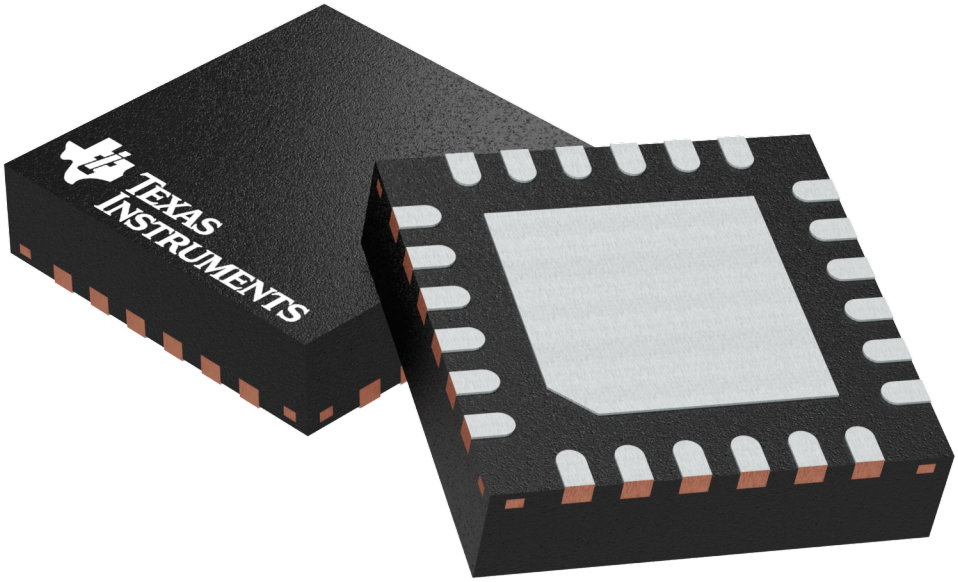


*All dimensions are nominal

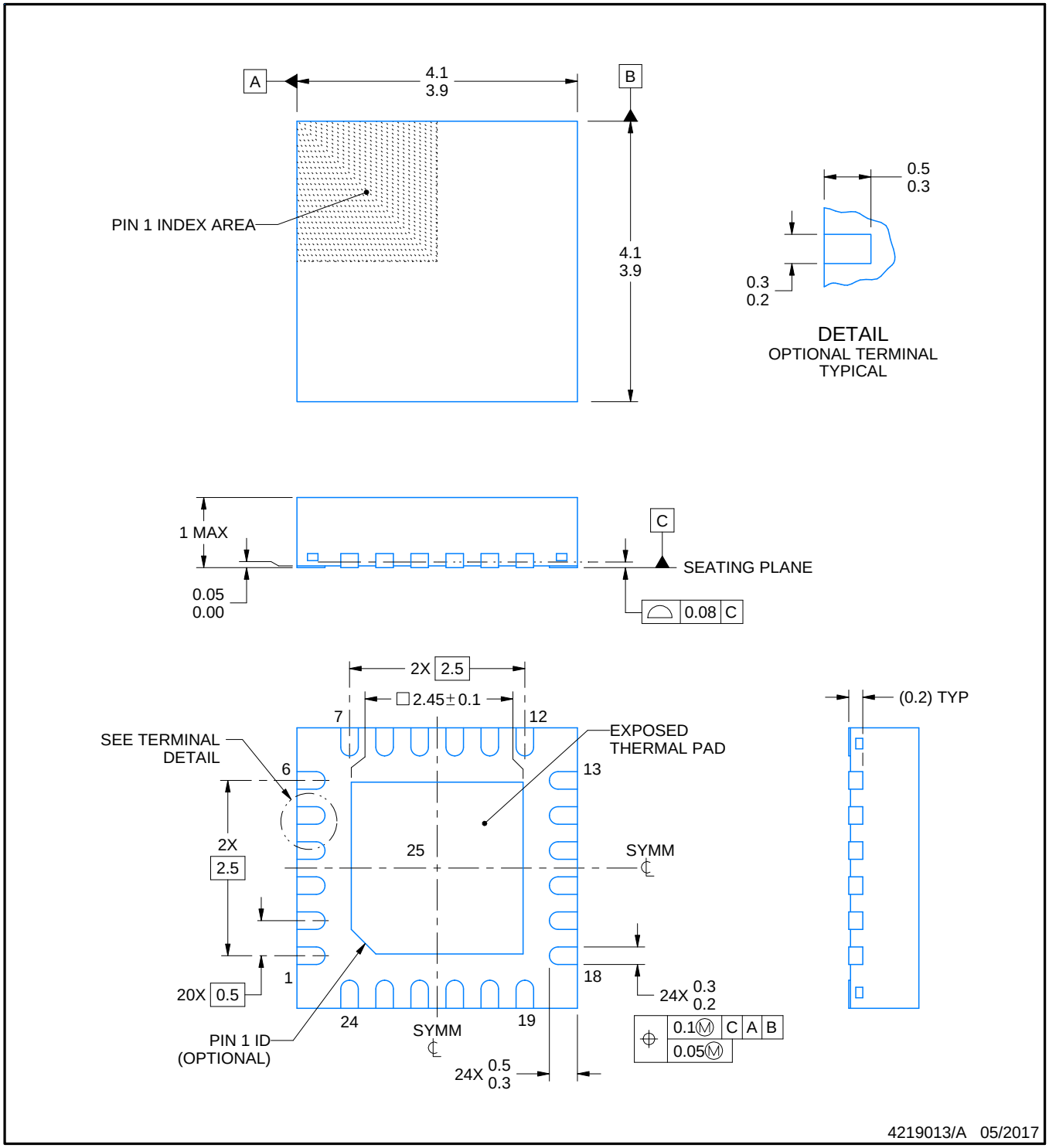
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8256EPWPR	HTSSOP	PWP	28	2500	356.0	356.0	35.0
DRV8256ERGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DRV8256PPWPR	HTSSOP	PWP	28	2500	356.0	356.0	35.0
DRV8256PRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
DRV8256PRGERG4	VQFN	RGE	24	3000	367.0	367.0	35.0

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

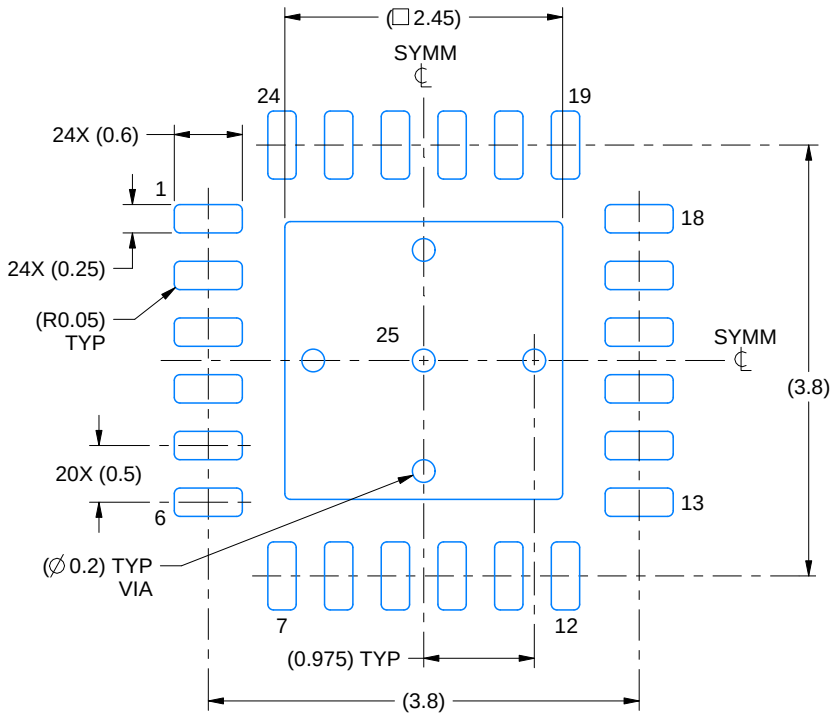


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

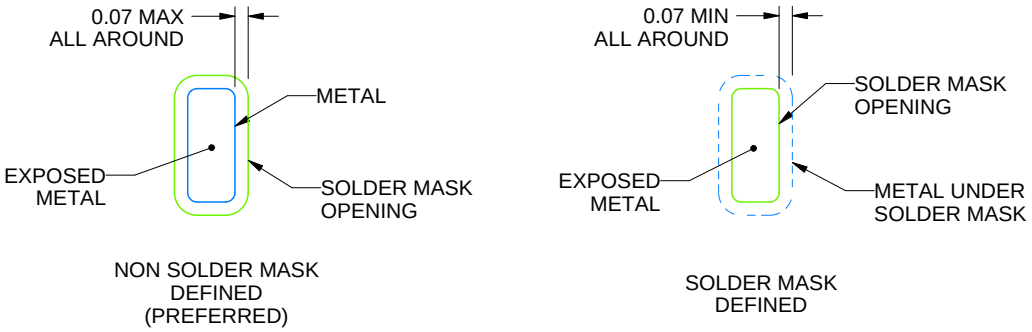


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

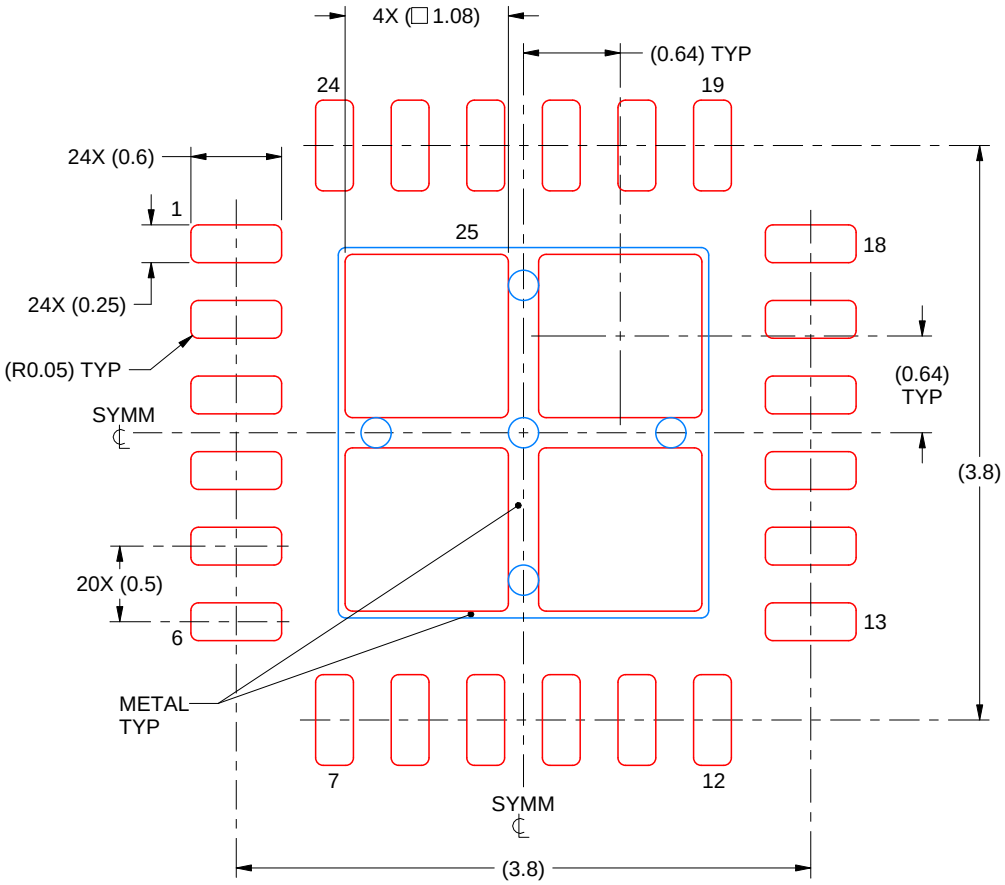


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

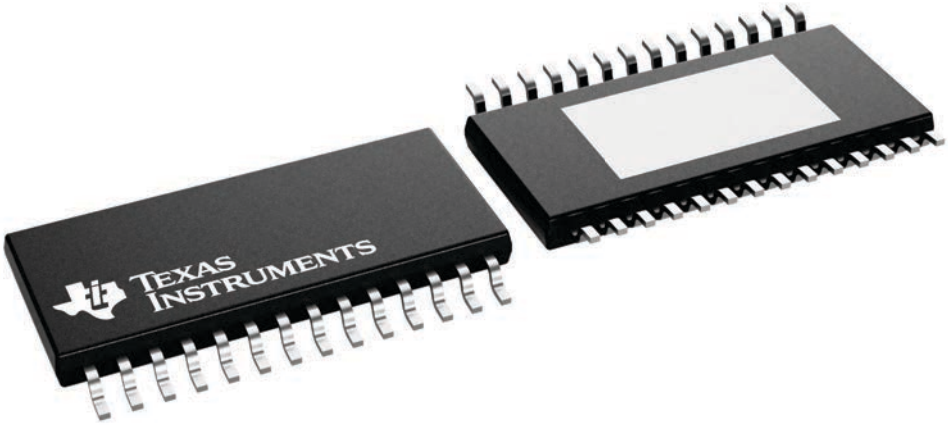
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

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