

## 1:3 LVPECL CLOCK BUFFER WITH PROGRAMMABLE DIVIDER

Check for Samples: [CDCP1803](#)

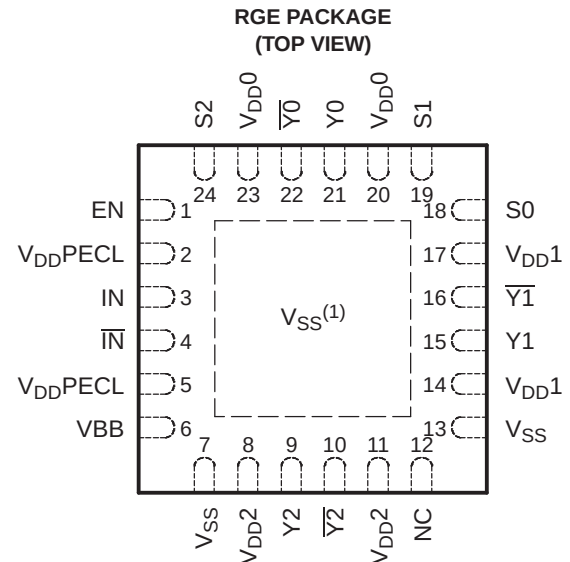
### FEATURES

- Distributes One Differential Clock Input to Three LVPECL Differential Clock Outputs
- Programmable Output Divider for Two LVPECL Outputs
- Low-Output Skew 15 ps (Typical)
- $V_{CC}$  Range 3 V–3.6 V
- Signaling Rate Up to 800-MHz LVPECL
- Differential Input Stage for Wide Common-Mode Range
- Provides VBB Bias Voltage Output for Single-Ended Input Signals
- Receiver Input Threshold  $\pm 75$  mV
- 24-Terminal QFN Package (4 mm  $\times$  4 mm)
- Accepts Any Differential Signaling: LVDS, HSTL, CML, VML, SSTL-2, and Single-Ended: LVTTTL/LVCMOS

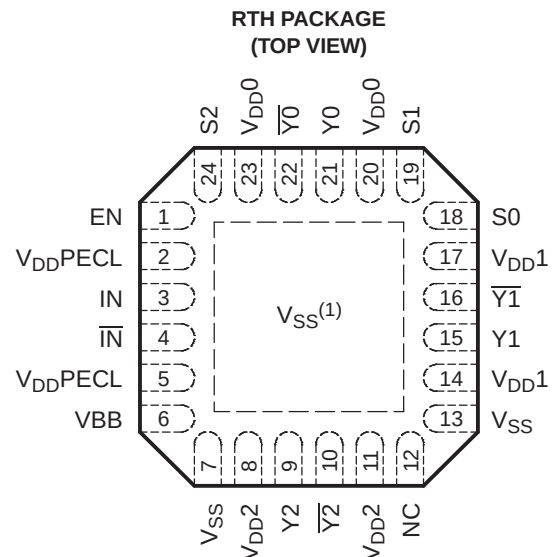
### DESCRIPTION

The CDCP1803 clock driver distributes one pair of differential clock inputs to three pairs of LVPECL differential clock outputs  $Y[2:0]$  and  $\overline{Y}[2:0]$  with minimum skew for clock distribution. The CDCP1803 is specifically designed for driving 50- $\Omega$  transmission lines.

The CDCP1803 has three control terminals, S0, S1, and S2, to select different output mode settings; see [Table 1](#) for details. The CDCP1803 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . For use in single-ended driver applications, the CDCP1803 also provides a VBB output terminal that can be directly connected to the unused input as a common-mode voltage reference.


(1) Thermal pad must be connected to  $V_{SS}$ .

P0024-02


(1) Thermal pad must be connected to  $V_{SS}$ .

P0025-02

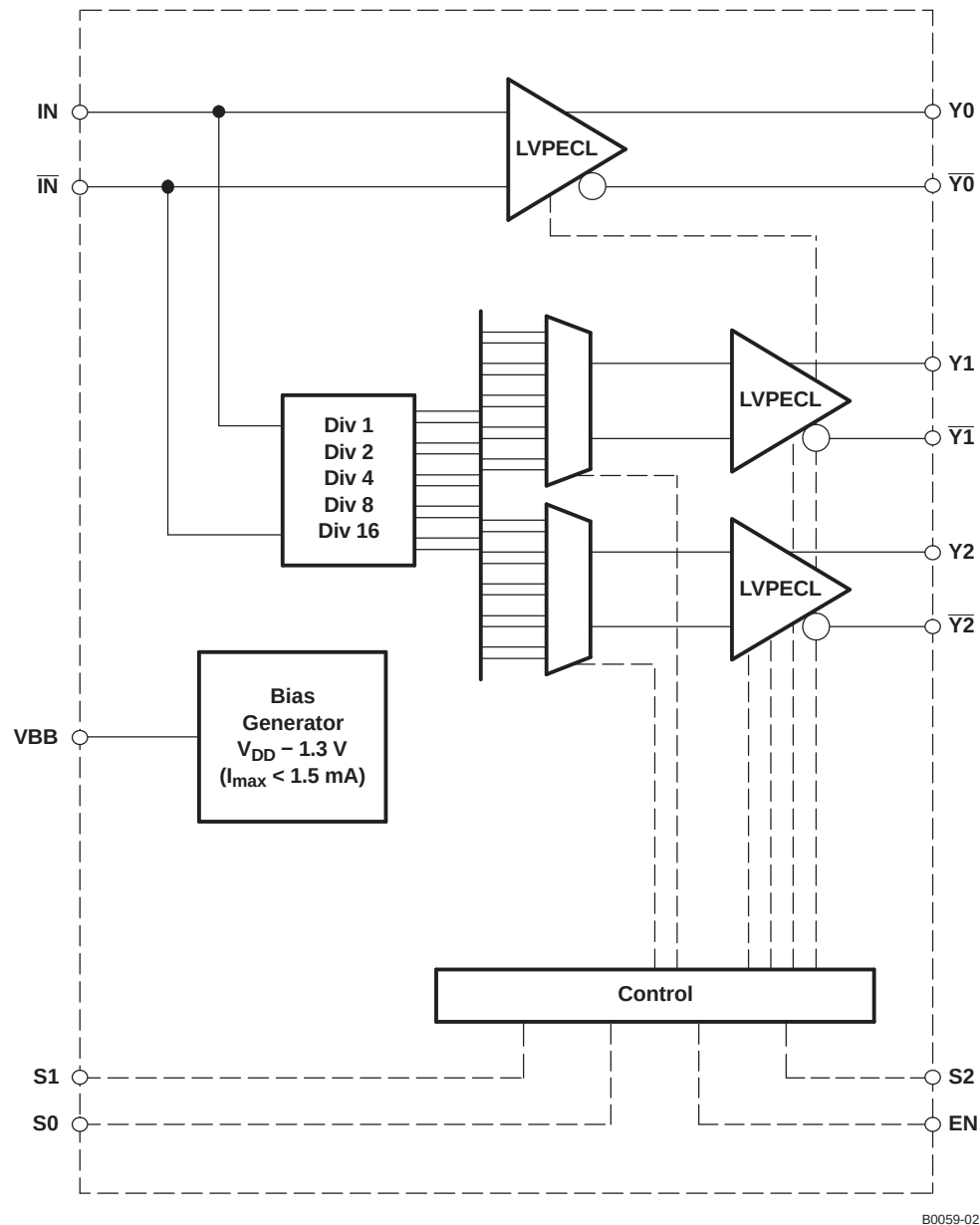


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## FUNCTIONAL BLOCK DIAGRAM



**TERMINAL FUNCTIONS**

| TERMINAL                             |                          | I/O                              | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|--------------------------------------|--------------------------|----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                                 | NO.                      |                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| EN                                   | 1                        | I<br>(with 60-k $\Omega$ pullup) | <p>ENABLE: Enables or disables all outputs simultaneously.</p> <p>EN = 1: outputs on according to S[2:0] settings</p> <p>EN = 0: outputs Y[2:0] off (high impedance)</p> <p>See <a href="#">Table 1</a> for details.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| IN, $\overline{\text{IN}}$           | 3, 4                     | I (differential)                 | <p>Differential input clock. Input stage is sensitive and has a wide common-mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Because the input is high-impedance, it is recommended to terminate the PCB transmission line before the input (e.g., with 100 <math>\Omega</math> across input). Input can also be driven by a single-ended signal if the complementary input is tied to VBB. A more-advanced scheme for single-ended signals is given in the <i>Application Information</i> section near the end of this document.</p> <p>The inputs employ an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than <math>\sim 0.7</math> V. Reverse biasing of the IC through these inputs is possible and must be prevented by limiting the input voltage <math>&lt; V_{DD}</math>.</p> |
| NC                                   | 12                       |                                  | No connect. Leave this terminal open or tie to ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| S[2:0]                               | 24, 19, 18               | I<br>(with 60-k $\Omega$ pullup) | Select mode of operation. Defines the output configuration of Y[2:0], see <a href="#">Table 1</a> for configuration.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| VBB                                  | 6                        | O                                | <p>Bias voltage output can be used to bias unused complementary input <math>\overline{\text{IN}}</math> for single-ended input signals.</p> <p>The output voltage of VBB is <math>V_{DD} - 1.3</math> V. When driving a load, the output current drive is limited to about 1.5 mA.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| $V_{DD\text{PECL}}$                  | 2, 5                     | Supply                           | Supply voltage PECL input + internal logic                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| $V_{DD[2:0]}$                        | 8, 11, 14,<br>17, 20, 23 | Supply                           | <p>PECL output supply voltage for output Y[2:0]. Each output can be disabled by pulling the corresponding <math>V_{DDX}</math> to GND.</p> <p><b>CAUTION:</b> In this mode, no voltage from outside may be forced, because internal diodes could be forced in forward direction. Thus, it is recommended to disconnect the output if it is not being used.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| $V_{SS}$                             | 7, 13                    | Supply                           | Device ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| $\overline{\text{Y}}[2:0]$<br>Y[2:0] | 9, 15, 21<br>10, 16, 22  | O (LVPECL)                       | LVPECL clock outputs. These outputs provide low-skew copies of IN or down-divided copies of clock IN based on selected mode of operation S[2:0]. If an output is unused, the output can simply be left open to save power and minimize noise impact to the remaining outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

# CDCP1803

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## CONTROL TERMINAL SETTINGS

The CDCP1803 has three control terminals (S0, S1, and S2) and an enable terminal (EN) to select different output mode settings.

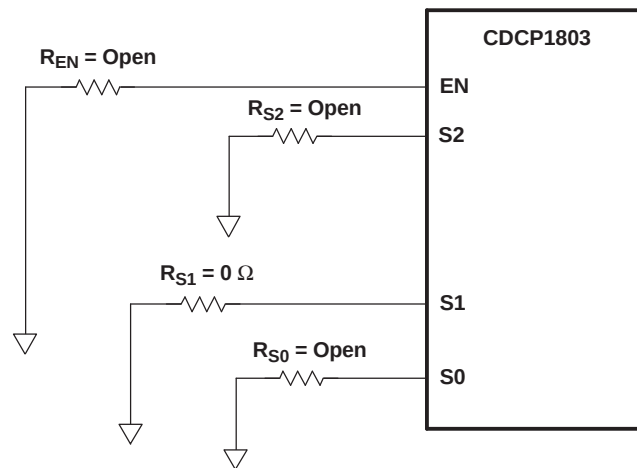
Setting for Mode 20:

EN = 1

S2 = 1

S1 = 0

S0 = 1



S0084-02

**Figure 1. Control Terminal Setting for Example**

**Table 1. Selection Mode Table**

| MODE | EN                 | S2                 | S1                 | S0                 | LVPECL <sup>(1)</sup> |              |              |
|------|--------------------|--------------------|--------------------|--------------------|-----------------------|--------------|--------------|
|      |                    |                    |                    |                    | Y0                    | Y1           | Y2           |
| 0    | 0                  | x                  | x                  | x                  | Off (high-z)          |              |              |
| 1    | 1                  | 0                  | 0                  | 0                  | ÷ 1                   | ÷ 1          | ÷ 1          |
| 2    | 1                  | 0                  | 0                  | V <sub>DD</sub> /2 | ÷ 1                   | Off (high-z) | Off (high-z) |
| 3    | 1                  | 0                  | 0                  | 1                  | ÷ 1                   | ÷ 1          | Off (high-z) |
| 4    | 1                  | 0                  | V <sub>DD</sub> /2 | 0                  | ÷ 1                   | ÷ 2          | Off (high-z) |
| 5    | 1                  | 0                  | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 | ÷ 1                   | ÷ 4          | Off (high-z) |
| 6    | 1                  | 0                  | V <sub>DD</sub> /2 | 1                  | ÷ 1                   | ÷ 8          | Off (high-z) |
| 7    | 1                  | 0                  | 1                  | 0                  | ÷ 1                   | Off (high-z) | ÷ 1          |
| 8    | 1                  | 0                  | 1                  | 1                  | ÷ 1                   | ÷ 2          | ÷ 1          |
| 9    | 1                  | V <sub>DD</sub> /2 | 0                  | 0                  | ÷ 1                   | ÷ 4          | ÷ 1          |
| 10   | 1                  | V <sub>DD</sub> /2 | 0                  | V <sub>DD</sub> /2 | ÷ 1                   | ÷ 8          | ÷ 1          |
| 11   | 1                  | V <sub>DD</sub> /2 | 0                  | 1                  | ÷ 1                   | Off (high-z) | ÷ 2          |
| 12   | 1                  | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 | 0                  | ÷ 1                   | ÷ 1          | ÷ 2          |
| 13   | 1                  | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 | ÷ 1                   | ÷ 2          | ÷ 2          |
| 14   | 1                  | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 | 1                  | ÷ 1                   | ÷ 4          | ÷ 2          |
| 15   | 1                  | V <sub>DD</sub> /2 | 1                  | 0                  | ÷ 1                   | ÷ 8          | ÷ 2          |
| 16   | 1                  | V <sub>DD</sub> /2 | 1                  | V <sub>DD</sub> /2 | ÷ 1                   | Off (high-z) | ÷ 4          |
| 17   | 1                  | V <sub>DD</sub> /2 | 1                  | 1                  | ÷ 1                   | ÷ 1          | ÷ 4          |
| 18   | 1                  | 1                  | 0                  | 0                  | ÷ 1                   | ÷ 2          | ÷ 4          |
| 19   | 1                  | 1                  | 0                  | V <sub>DD</sub> /2 | ÷ 1                   | ÷ 4          | ÷ 4          |
| 20   | 1                  | 1                  | 0                  | 1                  | ÷ 1                   | ÷ 8          | ÷ 4          |
| 21   | 1                  | 1                  | V <sub>DD</sub> /2 | 0                  | ÷ 1                   | Off (high-z) | ÷ 8          |
| 22   | 1                  | 1                  | V <sub>DD</sub> /2 | V <sub>DD</sub> /2 | ÷ 1                   | ÷ 1          | ÷ 8          |
| 23   | 1                  | 1                  | V <sub>DD</sub> /2 | 1                  | ÷ 1                   | ÷ 2          | ÷ 8          |
| 24   | 1                  | 1                  | 1                  | 0                  | ÷ 1                   | ÷ 4          | ÷ 8          |
| 25   | 1                  | 1                  | 1                  | V <sub>DD</sub> /2 | ÷ 1                   | ÷ 8          | ÷ 8          |
| 26   | 1                  | 1                  | 1                  | 1                  | ÷ 1                   | Off (high-z) | ÷ 16         |
| 27   | V <sub>DD</sub> /2 | 0                  | 0                  | 0                  | ÷ 1                   | ÷ 1          | ÷ 16         |
| 28   | V <sub>DD</sub> /2 | 0                  | 0                  | V <sub>DD</sub> /2 | ÷ 1                   | ÷ 2          | ÷ 16         |
| 29   | V <sub>DD</sub> /2 | 0                  | 0                  | 1                  | ÷ 1                   | ÷ 4          | ÷ 16         |
| 30   | V <sub>DD</sub> /2 | 0                  | V <sub>DD</sub> /2 | 0                  | ÷ 1                   | ÷ 8          | ÷ 16         |
| Rsv  | V <sub>DD</sub> /2 | 1                  | V <sub>DD</sub> /2 | 1                  | Reserved              | Reserved     | Reserved     |
| Rsv  | V <sub>DD</sub> /2 | 1                  | 1                  | 0                  | N/A                   | Low          | Low          |

- (1) The LVPECL outputs are open-emitter stages. Thus, if the unused LVPECL outputs Y0, Y1, or Y2 are left unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding V<sub>DD</sub> input to GND.

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### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

|           |                                                                                 |                               |
|-----------|---------------------------------------------------------------------------------|-------------------------------|
| $V_{DD}$  | Supply voltage                                                                  | –0.3 V to 3.8 V               |
| $V_I$     | Input voltage                                                                   | –0.2 V to ( $V_{DD} + 0.2$ V) |
| $V_O$     | Output voltage                                                                  | –0.2 V to ( $V_{DD} + 0.2$ V) |
|           | Differential short-circuit current, $Y_n$ , $\overline{Y_n}$ , $I_{OSD}$        | Continuous                    |
|           | Electrostatic discharge (HBM 1.5 k $\Omega$ , 100 pF), ESD                      | >2000 V                       |
|           | Moisture level 24-terminal QFN package (solder reflow temperature of 235°C) MSL | 2                             |
| $T_{stg}$ | Storage temperature                                                             | –65°C to 150°C                |
| $T_J$     | Maximum junction temperature                                                    | 125°C                         |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

|          |                                | MIN | TYP | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| $V_{DD}$ | Supply voltage                 | 3   | 3.3 | 3.6 | V    |
| $T_A$    | Operating free-air temperature | –40 |     | 85  | °C   |

### ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

#### LVPECL INPUT $IN$ , $\overline{IN}$

| PARAMETER | TEST CONDITIONS                                                     | MIN                   | TYP            | MAX      | UNIT       |
|-----------|---------------------------------------------------------------------|-----------------------|----------------|----------|------------|
| $f_{clk}$ | Input frequency                                                     | 0                     |                | 800      | MHz        |
| $V_{CM}$  | High-level input common mode                                        | 1                     | $V_{DD} - 0.3$ |          | V          |
| $V_{IN}$  | Input voltage swing between $IN$ and $\overline{IN}$ <sup>(1)</sup> | 500                   |                | 1300     | mV         |
|           | Input voltage swing between $IN$ and $\overline{IN}$ <sup>(2)</sup> | 125                   |                | 1300     |            |
| $I_{IN}$  | Input current                                                       | $V_I = V_{DD}$ or 0 V |                | $\pm 10$ | $\mu A$    |
| $R_{IN}$  | Input impedance                                                     | 300                   |                |          | k $\Omega$ |
| $C_I$     | Input capacitance at $IN$ , $\overline{IN}$                         |                       | 1              |          | pF         |

- (1) Is required to maintain ac specifications  
(2) Is required to maintain device functionality

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

### LVPECL OUTPUT DRIVER Y[2:0], $\overline{Y[2:0]}$

| PARAMETER       |                                                                                    | TEST CONDITIONS                                            | MIN             | TYP | MAX             | UNIT     |
|-----------------|------------------------------------------------------------------------------------|------------------------------------------------------------|-----------------|-----|-----------------|----------|
| $f_{clk}$       | Output frequency, see <a href="#">Figure 3</a> .                                   |                                                            | 0               |     | 800             | MHz      |
| $V_{OH}$        | High-level output voltage                                                          | Termination with 50 $\Omega$ to $V_{DD} - 2$ V             | $V_{DD} - 1.18$ |     | $V_{DD} - 0.81$ | V        |
| $V_{OL}$        | Low-level output voltage                                                           | Termination with 50 $\Omega$ to $V_{DD} - 2$ V             | $V_{DD} - 1.98$ |     | $V_{DD} - 1.55$ | V        |
| $V_O$           | Output voltage swing between Y and $\overline{Y}$ , see <a href="#">Figure 3</a> . | Termination with 50 $\Omega$ to $V_{DD} - 2$ V             | 500             |     |                 | mV       |
| $I_{OZL}$       | Output 3-state current                                                             | $V_{DD} = 3.6$ V, $V_O = 0$ V                              |                 |     | 5               | $\mu$ A  |
| $I_{OZH}$       |                                                                                    | $V_{DD} = 3.6$ V, $V_O = V_{DD} - 0.8$ V                   |                 |     | 10              |          |
| $t_r/t_f$       | Rise and fall times                                                                | 20% to 80% of $V_{OUTPP}$ , see <a href="#">Figure 7</a> . | 200             |     | 350             | ps       |
| $t_{skpecl(o)}$ | Output skew between any LVPECL output Y[2:0] and $\overline{Y[2:0]}$               | See Note A in <a href="#">Figure 6</a> .                   |                 | 15  | 30              | ps       |
| $t_{Duty}$      | Output duty-cycle distortion <sup>(1)</sup>                                        | Crossing point-to-crossing point distortion                | -50             |     | 50              | ps       |
| $t_{sk(pp)}$    | Part-to-part skew                                                                  | Any Y, see Note B in <a href="#">Figure 6</a> .            |                 | 50  | 300             | ps       |
| $C_O$           | Output capacitance                                                                 | $V_O = V_{DD}$ or GND                                      |                 | 1   |                 | pF       |
| LOAD            | Expected output load                                                               |                                                            |                 | 50  |                 | $\Omega$ |

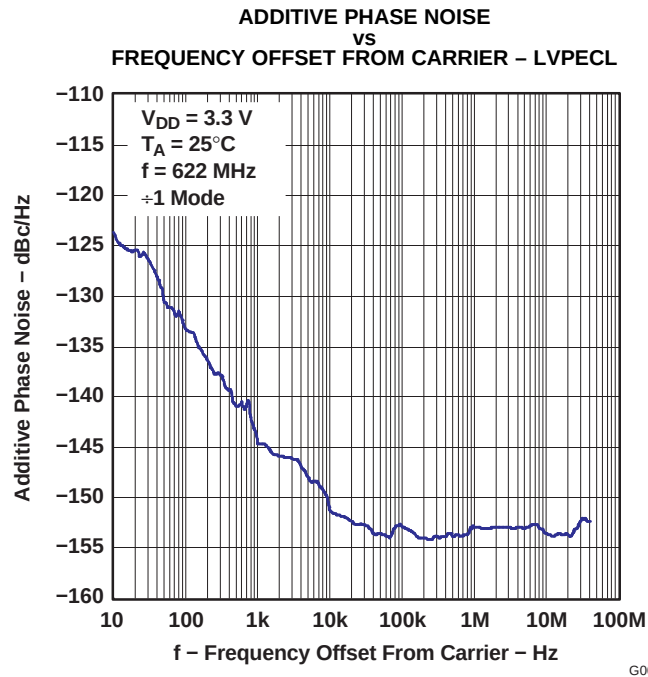
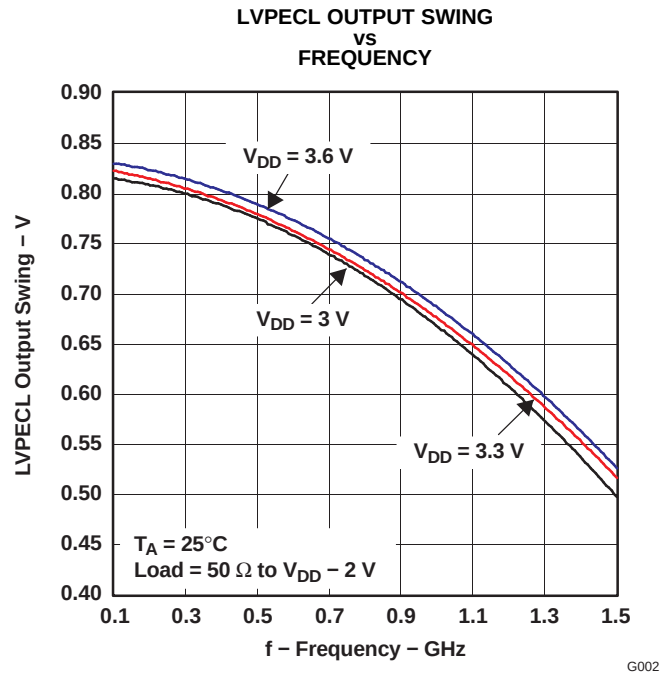
(1) For an 800-MHz signal, the 50-ps error would result in a duty cycle distortion of  $\pm 4\%$  when driven by an ideal clock input signal.

### LVPECL INPUT-TO-LVPECL OUTPUT PARAMETERS

| PARAMETER    |                                 | TEST CONDITIONS                                      | MIN | TYP | MAX | UNIT |
|--------------|---------------------------------|------------------------------------------------------|-----|-----|-----|------|
| $t_{pd(lh)}$ | Propagation delay, rising edge  | VOX to VOX                                           | 320 |     | 600 | ps   |
| $t_{pd(hl)}$ | Propagation delay, falling edge | VOX to VOX                                           | 320 |     | 600 | ps   |
| $t_{sk(p)}$  | LVPECL pulse skew               | VOX to VOX, see Note C in <a href="#">Figure 6</a> . |     |     | 100 | ps   |

### JITTER CHARACTERISTICS

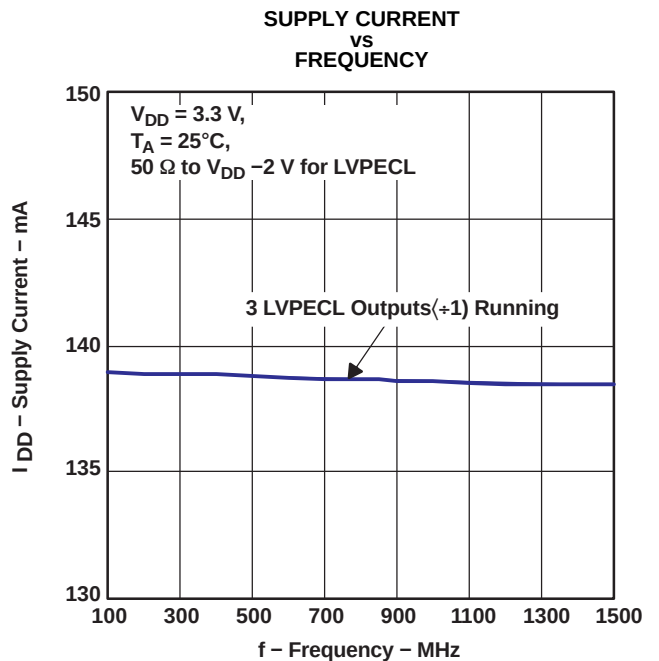
| PARAMETER                     |                                                                                          | TEST CONDITIONS                                                          | MIN | TYP | MAX  | UNIT   |
|-------------------------------|------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-----|-----|------|--------|
| <b>JITTER CHARACTERISTICS</b> |                                                                                          |                                                                          |     |     |      |        |
| $t_{jitterLVPECL}$            | Additive phase jitter from input to LVPECL output Y[2:0], see <a href="#">Figure 2</a> . | 12 kHz to 20 MHz,<br>$f_{out} = 250$ MHz to 800 MHz,<br>divide-by-1 mode |     |     | 0.15 | ps rms |
|                               |                                                                                          | 50 kHz to 40 MHz,<br>$f_{out} = 250$ MHz to 800 MHz,<br>divide-by-1 mode |     |     | 0.25 |        |


**Figure 2.**

**Figure 3.**

## SUPPLY CURRENT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |                                                                 |           | TEST CONDITIONS                                                                                                                             | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------------------------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $I_{DD}$  | Supply current                                                  | Full load | All outputs enabled and terminated with 50 $\Omega$ to $V_{DD} - 2$ V on LVPECL outputs, $f = 800$ MHz for LVPECL outputs, $V_{DD} = 3.3$ V |     | 140 |     | mA   |
|           |                                                                 | No load   | Outputs enabled, no output load, $f = 800$ MHz for LVPECL outputs, $V_{DD} = 3.6$ V                                                         |     | 90  |     |      |
|           | Supply current saving per LVPECL output stage disabled, no load |           | $f = 800$ MHz for LVPECL output, $V_{DD} = 3.3$ V                                                                                           |     | 10  |     |      |
| $I_{DDZ}$ | Supply current, 3-state                                         |           | All outputs in high-impedance state by control logic, $f = 0$ Hz, $V_{DD} = 3.6$ V                                                          |     | 0.5 |     | mA   |



**Figure 4.**

## PACKAGE THERMAL RESISTANCE

| PARAMETER                                                                                      | TEST CONDITIONS                                                                                              | MIN | TYP   | MAX | UNIT |
|------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|-----|-------|-----|------|
| $R_{\theta JA-1}$ QFN-24 package thermal resistance <sup>(1)</sup>                             | 4-layer JEDEC test board (JESD51-7),<br>airflow = 0 ft/min                                                   |     | 106.6 |     | °C/W |
| $R_{\theta JA-2}$ QFN-24 package thermal resistance<br>with thermal vias in PCB <sup>(1)</sup> | 4-layer JEDEC test board (JESD51-7) with four<br>thermal vias of 22-mil diameter each,<br>airflow = 0 ft/min |     | 55.4  |     | °C/W |

- (1) It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

### Example:

**Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:**

$T_{\text{Chassis}} = 85^{\circ}\text{C}$  (temperature of the chassis)

$P_{\text{effective}} = I_{\text{max}} \times V_{\text{max}} = 90 \text{ mA} \times 3.6 \text{ V} = 324 \text{ mW}$  (max power consumption inside the package)

$\theta T_{\text{Junction}} = \theta_{JA-2} \times P_{\text{effective}} = 55.45^{\circ}\text{C/W} \times 324 \text{ mW} = 17.97^{\circ}\text{C}$

$T_{\text{Junction}} = \theta T_{\text{Junction}} + T_{\text{Chassis}} = 17.97^{\circ}\text{C} + 85^{\circ}\text{C} = 103^{\circ}\text{C}$  (the maximum junction temperature of

$T_{\text{die-max}} = 125^{\circ}\text{C}$  is not violated)

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## CONTROL INPUT CHARACTERISTICS

over recommended operating free-air temperature range

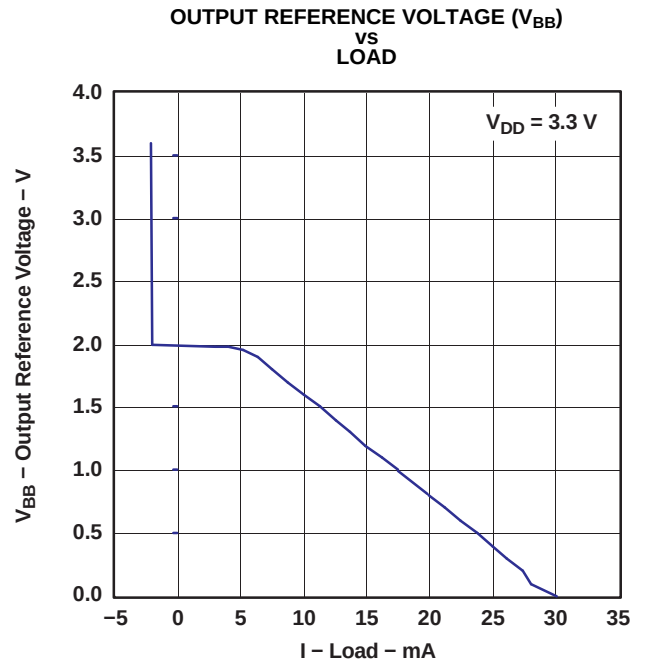
| PARAMETER       |                                                                                                                                                                          | TEST CONDITIONS | MIN          | TYP | MAX          | UNIT       |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------|-----|--------------|------------|
| $t_{su}$        | Setup time, S0, S1, S2, and EN terminals before clock IN                                                                                                                 |                 | 25           |     |              | ns         |
| $t_h$           | Hold time, S0, S1, S2, and EN terminals after clock IN                                                                                                                   |                 | 0            |     |              | ns         |
| $t_{(disable)}$ | Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)                                     |                 |              | 10  |              | ns         |
| $t_{(enable)}$  | Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals) |                 |              | 1   |              | $\mu s$    |
| Rpullup         | Internal pullup resistor on S[2:0] and EN input                                                                                                                          |                 | 42           | 60  | 78           | k $\Omega$ |
| $V_{IH(H)}$     | Three-level input high, S0, S1, S2, and EN terminals <sup>(1)</sup>                                                                                                      |                 | 0.9 $V_{DD}$ |     |              | V          |
| $V_{IL(L)}$     | Three-level low, S0, S1, S2, and EN terminals                                                                                                                            |                 |              |     | 0.1 $V_{DD}$ | V          |
| $I_{IH}$        | Input current, S0, S1, S2, and EN terminals                                                                                                                              | $V_I = V_{DD}$  |              |     | -5           | $\mu A$    |
| $I_{IL}$        |                                                                                                                                                                          | $V_I = GND$     | 38           |     | 85           | $\mu A$    |

(1) Leaving this terminal floating automatically pulls the logic level high to  $V_{DD}$  through an internal pullup resistor of 60 k $\Omega$ .

## BIAS VOLTAGE VBB

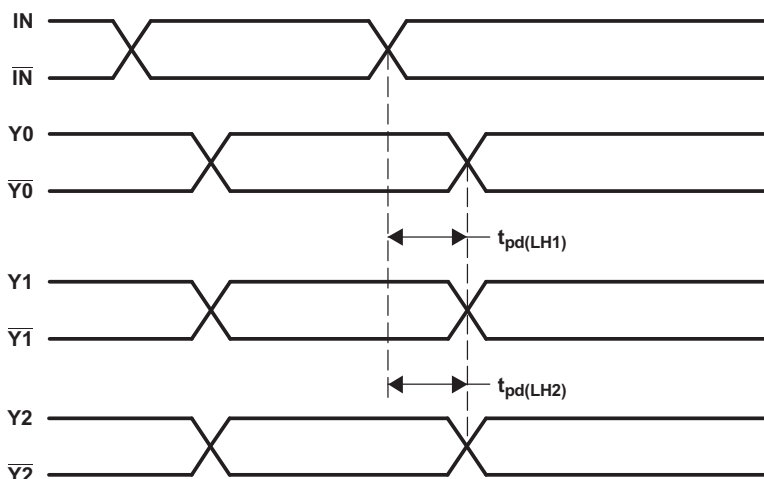
over operating free-air temperature range

| PARAMETER                    | TEST CONDITIONS                                                    | MIN            | TYP | MAX            | UNIT |
|------------------------------|--------------------------------------------------------------------|----------------|-----|----------------|------|
| VBB Output reference voltage | $V_{DD} = 3\text{ V}$ – $3.6\text{ V}$ , $I_{BB} = -0.2\text{ mA}$ | $V_{DD} - 1.4$ |     | $V_{DD} - 1.2$ | V    |



**Figure 5.**

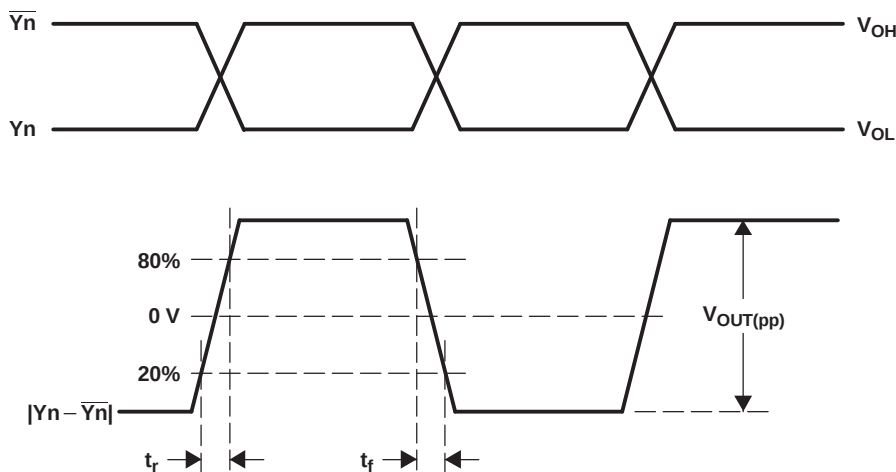
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew,  $t_{sk(o)}$ , is calculated as the greater of:
- The difference between the fastest and the slowest  $t_{pd(LH)n}$  ( $n = 0 \dots 2$ )
  - The difference between the fastest and the slowest  $t_{pd(HL)n}$  ( $n = 0 \dots 2$ )
- B. Part-to-part skew,  $t_{sk(pp)}$ , is calculated as the greater of:
- The difference between the fastest and the slowest  $t_{pd(LH)n}$  ( $n = 0 \dots 2$  for LVPECL across multiple devices)
  - The difference between the fastest and the slowest  $t_{pd(HL)n}$  ( $n = 0 \dots 2$  for LVPECL across multiple devices)
- C. Pulsaskew,  $t_{sk(p)}$ , is calculated as the magnitude of the absolute time difference between the high-to-low ( $t_{pd(HL)}$ ) and the low-to-high ( $t_{pd(LH)}$ ) propagation delays when a single switching input causes one or more outputs to switch,  $t_{sk(p)} = |t_{pd(HL)} - t_{pd(LH)}|$ . Pulse skew is sometimes referred to as pulse width distortion or duty cycle skew.

T0067-02

**Figure 6. Waveforms for Calculation of  $t_{sk(o)}$  and  $t_{sk(pp)}$**



T0058-02

**Figure 7. LVPECL Differential Output Voltage and Rise/Fall Time**

## PCB DESIGN FOR THERMAL FUNCTIONALITY

It is recommended to take special care of the PCB design for good thermal flow from the QFN 24-terminal package to the PCB.

Due to the three LVPECL outputs, the current consumption of the CDCP1803 is fixed.

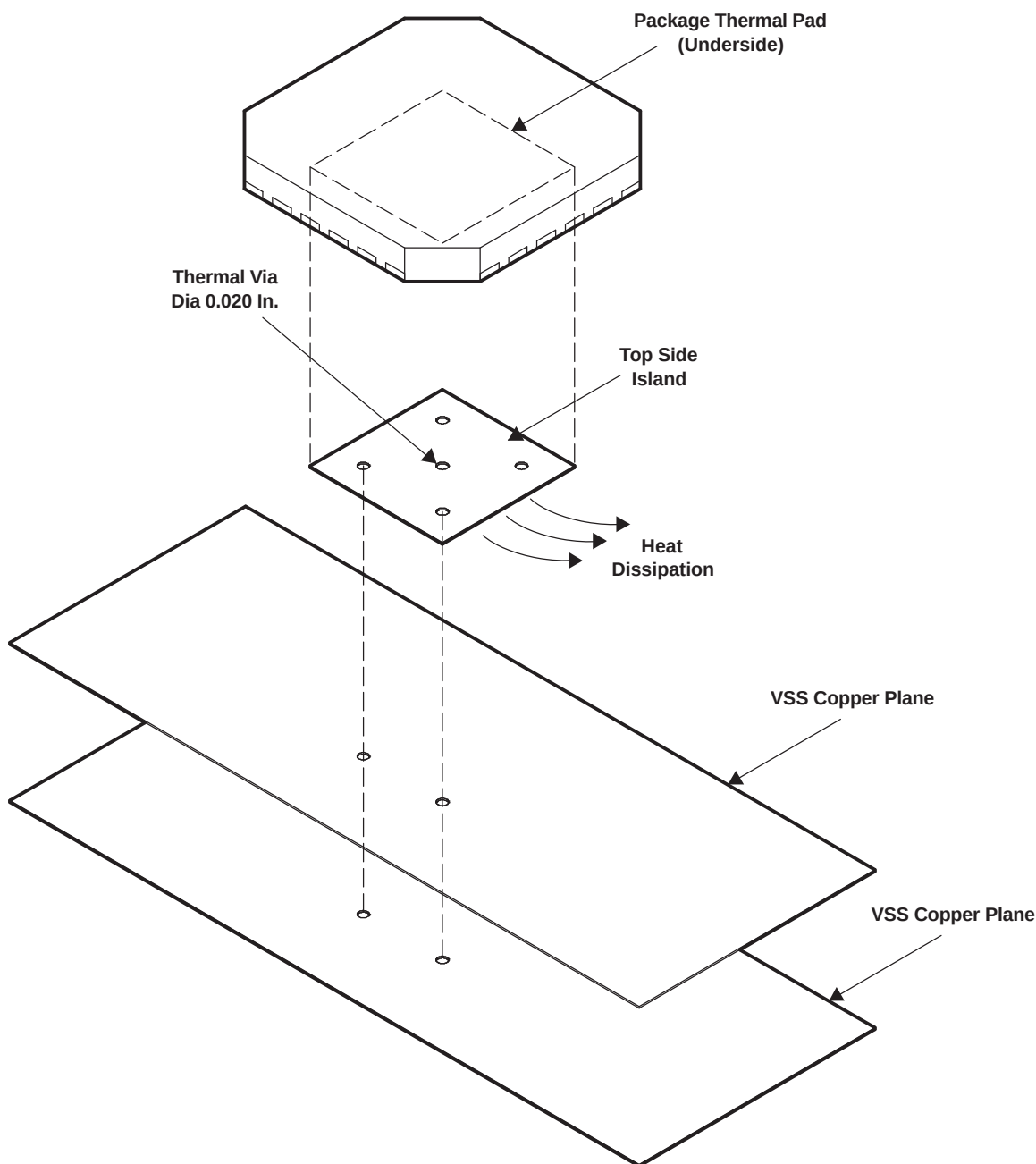
JEDEC JESD51-7 specifies thermal conductivity for standard PCB boards.

## PARAMETER MEASUREMENT INFORMATION (continued)

Modeling the CDCP1803 with a standard 4-layer JEDEC board results in a 59.5°C maximum temperature with  $R_{\theta JA}$  of 106.62°C/W for 25°C ambient temperature.

When deploying four thermal vias (one per quadrant), the thermal flow improves significantly, yielding 42.9°C maximum temperature with  $R_{\theta JA}$  of 55.4°C/W for 25°C ambient temperature.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications enabling all four outputs at once.



M0029-01

**Figure 8. Recommended Thermal Via Placement**

See the *Quad Flatpack No-Lead Logic Packages* ([SCBA017](#)) and *QFN/SON PCB Attachment* ([SLUA271](#)) application reports for further package-related information.

## APPLICATION INFORMATION

### LVPECL RECEIVER INPUT TERMINATION

The input of the CDCP1803 has a high impedance and comes with a large common-mode voltage range.

For optimized noise performance, it is recommended to properly terminate the PCB trace (transmission line). If a differential signal drives the CDCP1803, then a 100- $\Omega$  termination resistor is recommended to be placed as close as possible across the input terminals. An even better approach is to install  $2 \times 50\text{-}\Omega$  resistors, with the center tap connected to a capacitor (C) to terminate odd-mode noise and make up for transmission line mismatches. The VBB output can also be connected to the center tap to bias the input signal to ( $V_{DD} - 1.3\text{ V}$ ) (see Figure 9).

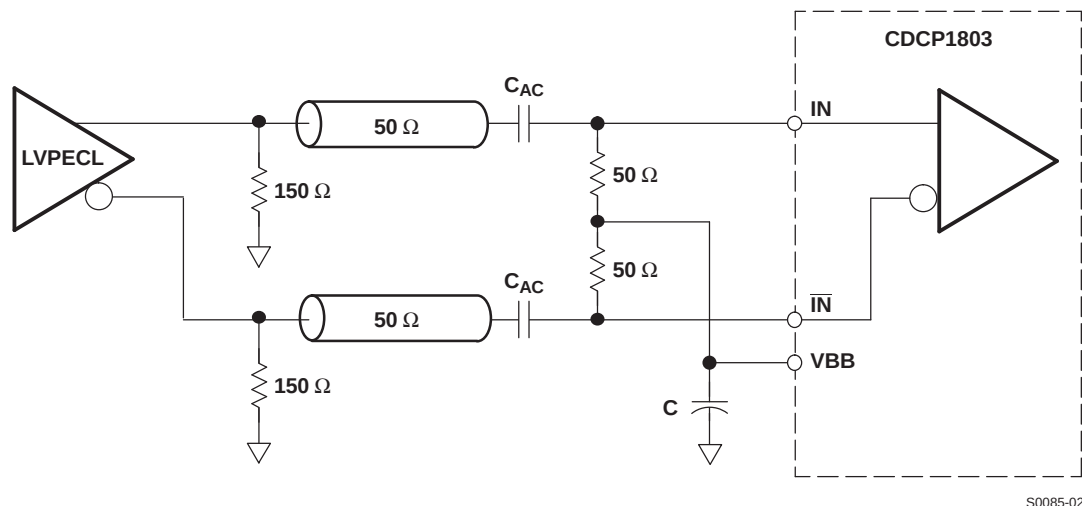


Figure 9. Recommended AC-Coupling LVPECL Receiver Input Termination

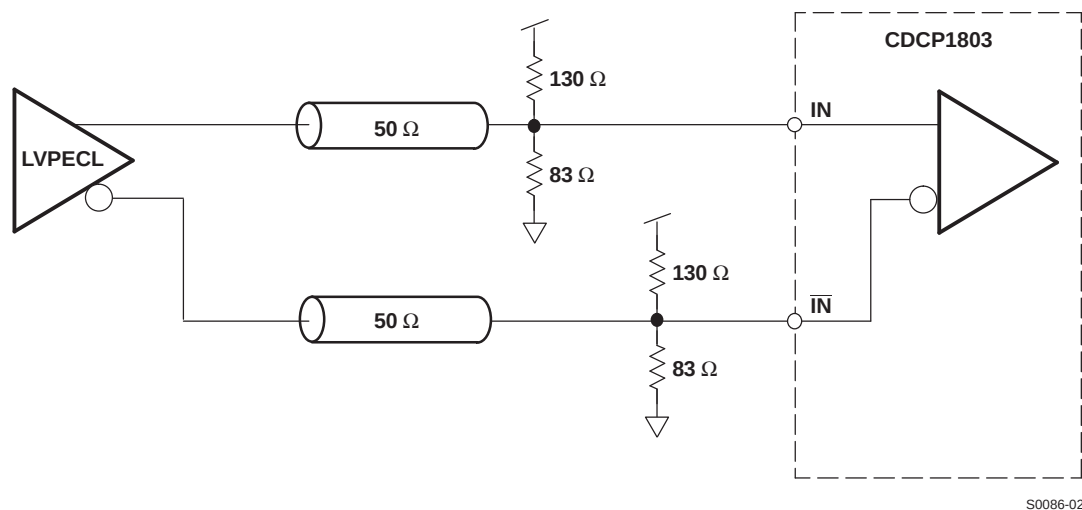
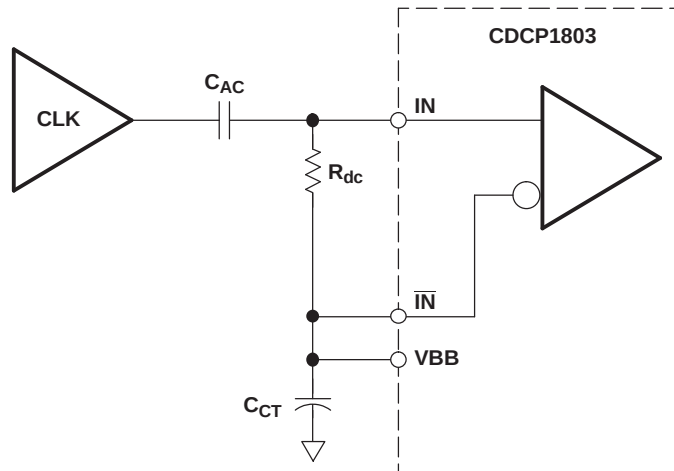


Figure 10. Recommended DC-Coupling LVPECL Receiver Input Termination

The CDCP1803 can also be driven by single-ended signals. Typically, the input signal becomes connected to one input, while the complementary input must be properly biased to the center voltage of the incoming input signal. For LVCMOS signals, this would be  $V_{CC}/2$ , realized by a simple voltage divider (e.g., two 10-k $\Omega$  resistors). The best option (especially if the dc offset of the input signal might vary) is to ac-couple the input signal and then rebias the signal using the VBB reference output. See Figure 11.



NOTE:  $C_{AC}$  – AC-coupling capacitor (e.g., 10 nF)  
 $C_{CT}$  – Capacitor keeps voltage at  $\overline{IN}$  constant (e.g., 10 nF)  
 $R_{dc}$  – Load and correct duty cycle (e.g., 50  $\Omega$ )  
VBB – Bias voltage output

S0087-02

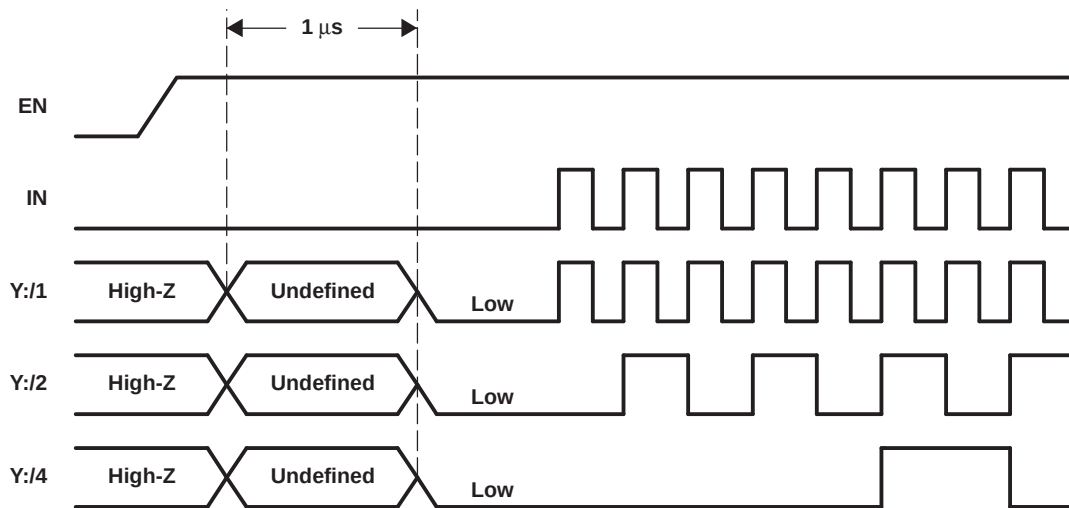
**Figure 11. Typical Application Setting for Single-Ended Input Signals Driving the CDCP1803**

## DEVICE BEHAVIOR DURING RESET AND CONTROL-TERMINAL SWITCHING

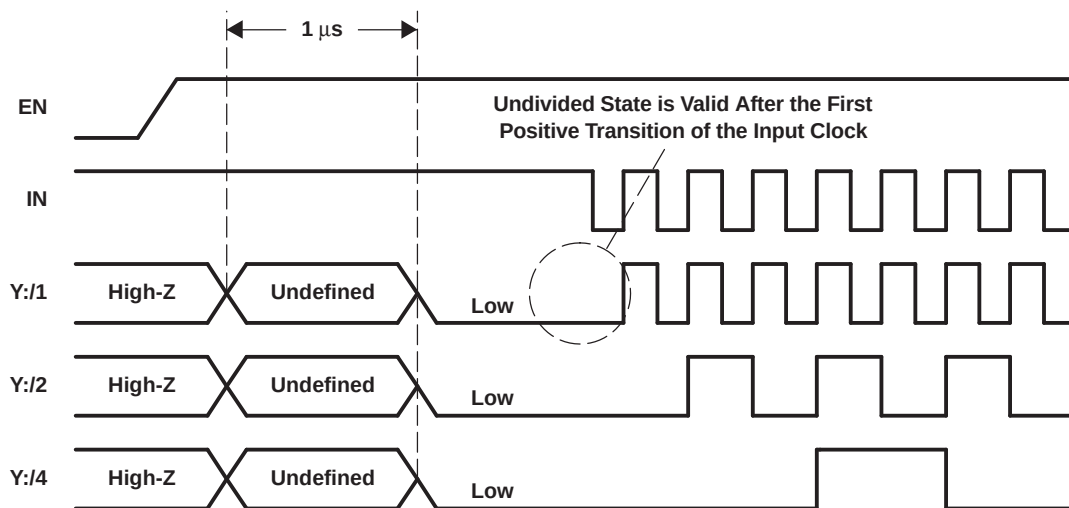
### Output Behavior From Enabling the Device ( $EN = 0 \rightarrow 1$ )

In disable mode ( $EN = 0$ ), all output drivers are switched in high-Z mode. The  $S[2:0]$  control inputs are also switched off. In the same mode, all flip-flops are reset. The typical current consumption is below 500  $\mu A$ .

When the device is enabled again, it takes typically 1  $\mu s$  for the settling of the reference voltage and currents. During this time, the outputs  $Y[2:0]$  and  $\overline{Y}[2:0]$  drive a high signal. After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device is as shown in [Figure 12](#). The inverting input and output signal is not included. The  $Y:/1$  waveform is the undivided output driver state.



Signal State After the Device is Enabled (IN = Low)



Signal State After the Device is Enabled (IN = High)

T0068-01

**Figure 12. Waveforms**

# CDCP1803

SCAS727F – NOVEMBER 2003 – REVISED DECEMBER 2013

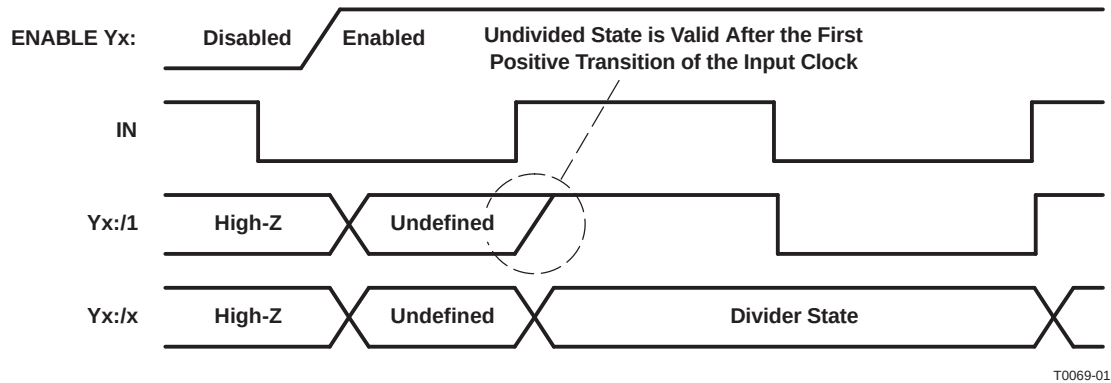
www.ti.com

## Enabling a Single Output Stage

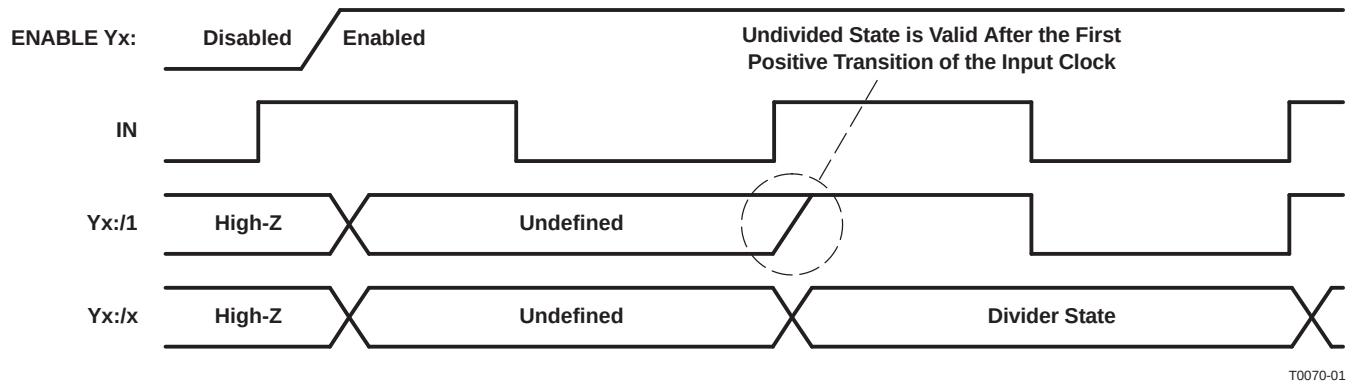
If a single output stage becomes enabled:

- $Y[2:0]$  is either low or high (undefined).
- $\overline{Y[2:0]}$  is the inverted signal of  $Y[2:0]$ .

With the first positive clock transition, the undivided output becomes the input clock state. The divided output states are equal to the actual internal divider. The internal divider is not reset while enabling single output drivers.



**Figure 13. Signal State After an Output Driver Becomes Enabled While  $IN = 0$**



**Figure 14. Signal State After an Output Driver Becomes Enabled While  $IN = 1$**

## REVISION HISTORY

| Changes from Revision E (January 2007) to Revision F                                                                                 | Page |
|--------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed $t_{sk(pp)}$ Part-to-part skew - included a MAX value of 300 ps .....                                                      | 7    |
| • Changed Note B in <a href="#">Figure 6</a> From: (n = 0...2 for LVPECL, n = 3 for LVCMOS) To: (n = 0...2 for LVPECLS) across ..... | 11   |

## PACKAGING INFORMATION

| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CDCP1803RGER</a> | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CDCP<br>1803        |
| CDCP1803RGER.B               | Active        | Production           | VQFN (RGE)   24 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CDCP<br>1803        |
| <a href="#">CDCP1803RGET</a> | Active        | Production           | VQFN (RGE)   24 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CDCP<br>1803        |
| CDCP1803RGET.B               | Active        | Production           | VQFN (RGE)   24 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CDCP<br>1803        |
| CDCP1803RGETG4               | Active        | Production           | VQFN (RGE)   24 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CDCP<br>1803        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

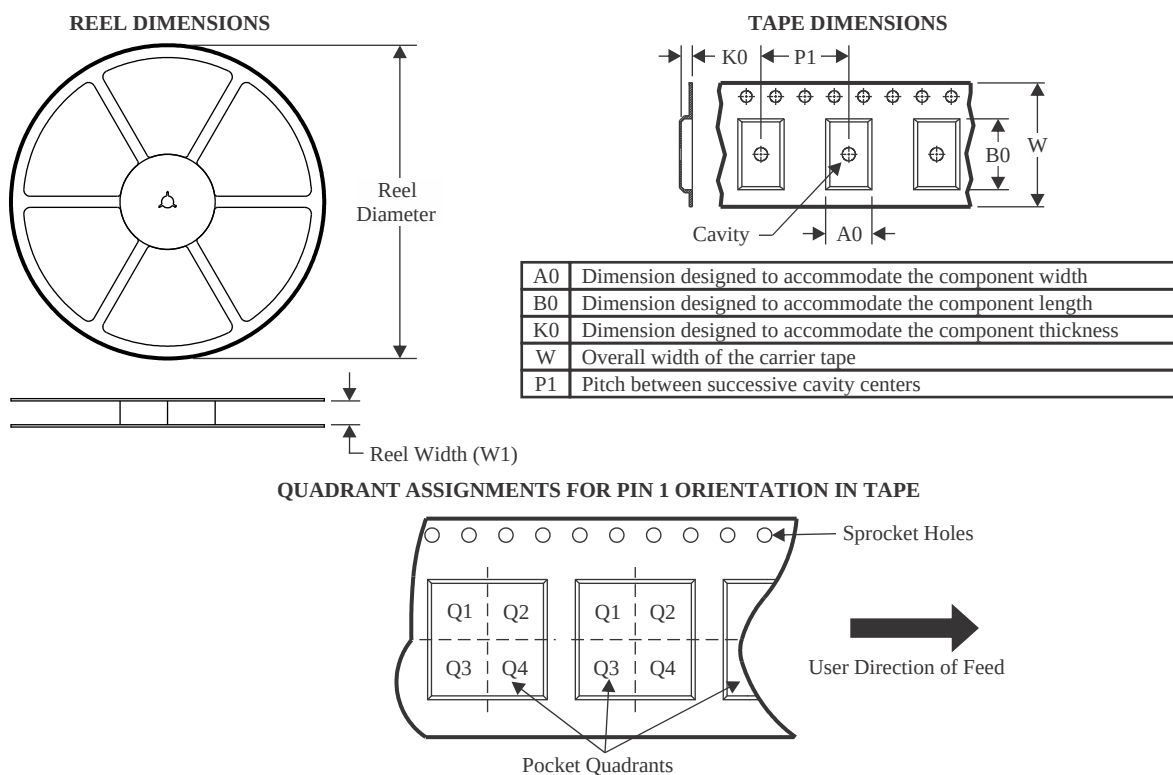
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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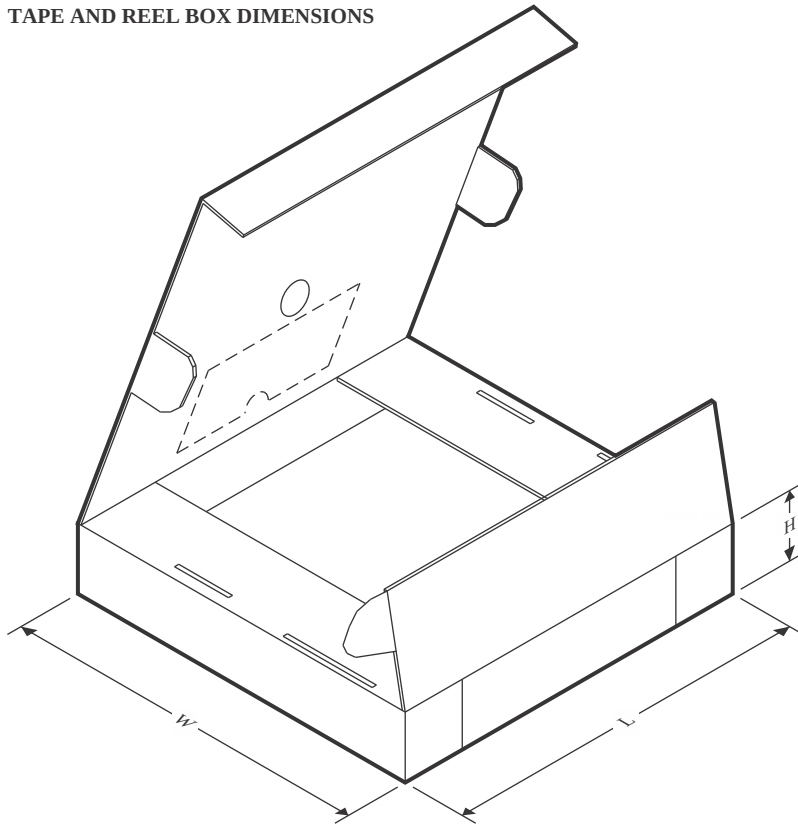
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCP1803RGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.3     | 4.3     | 1.5     | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

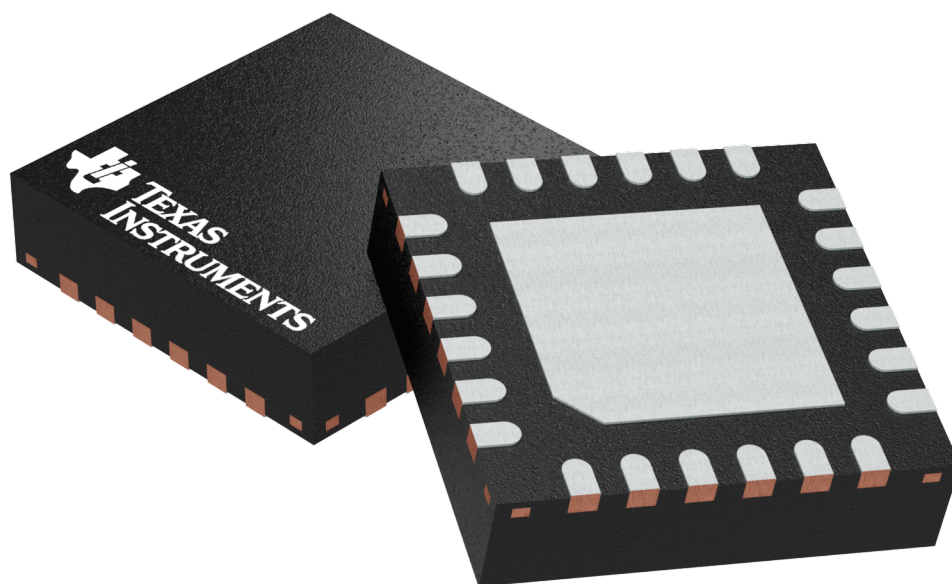
| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCP1803RGER | VQFN         | RGE             | 24   | 3000 | 350.0       | 350.0      | 43.0        |

**RGE 24**

**GENERIC PACKAGE VIEW**

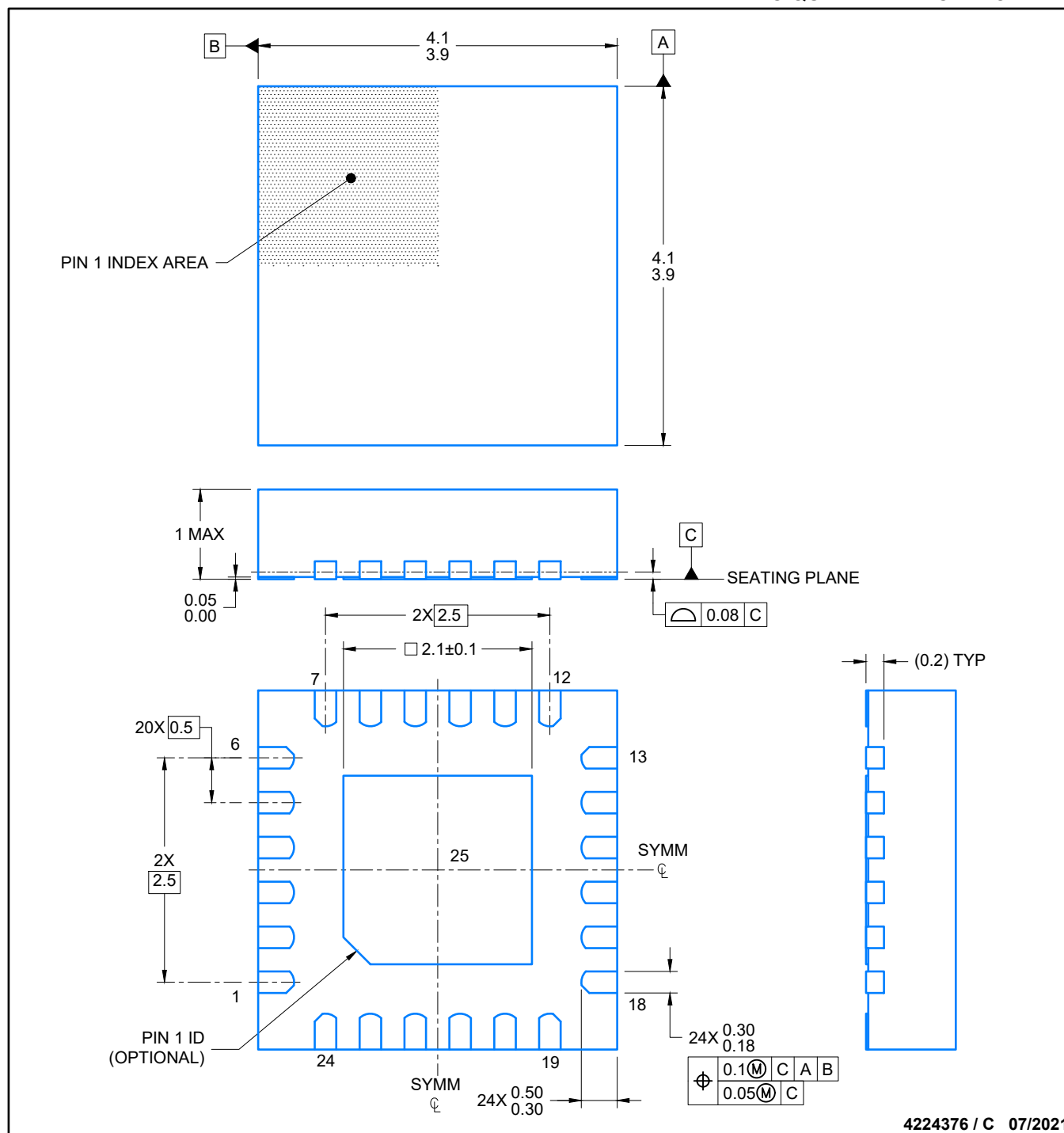
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



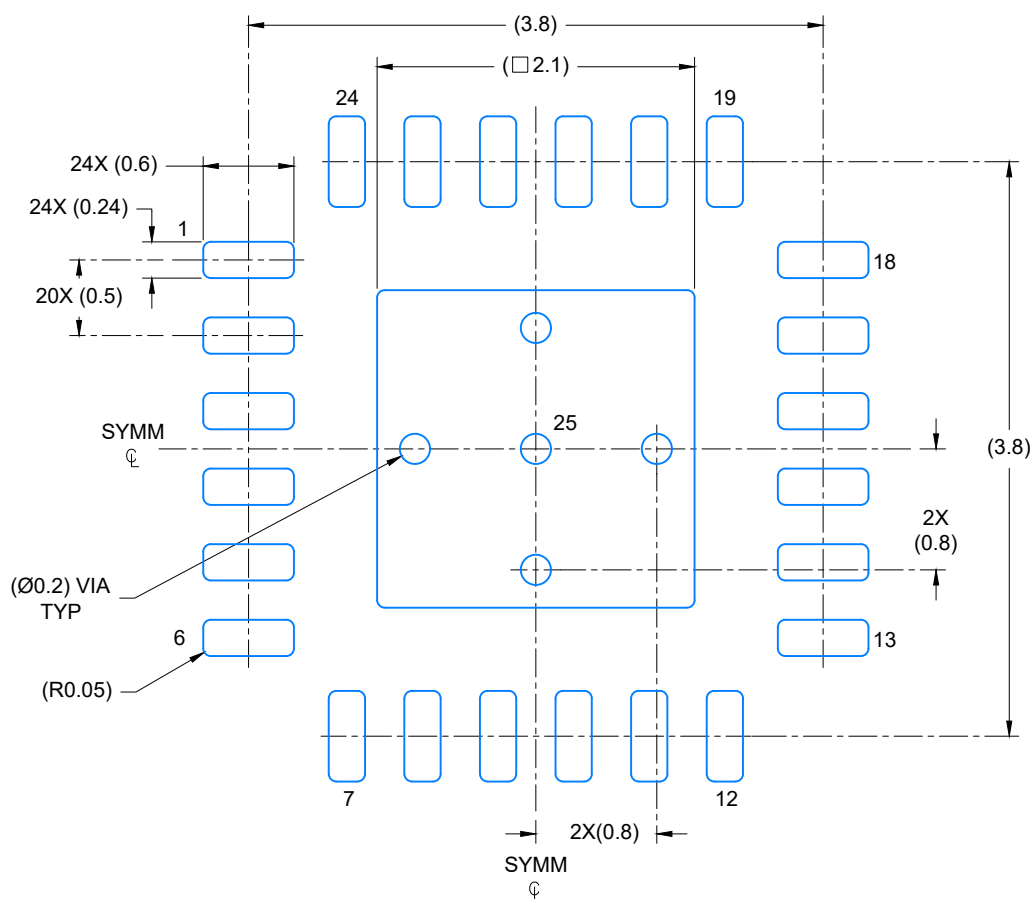
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H

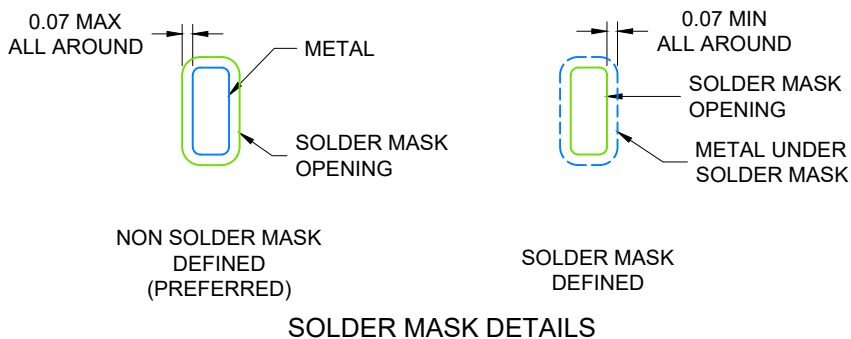


## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



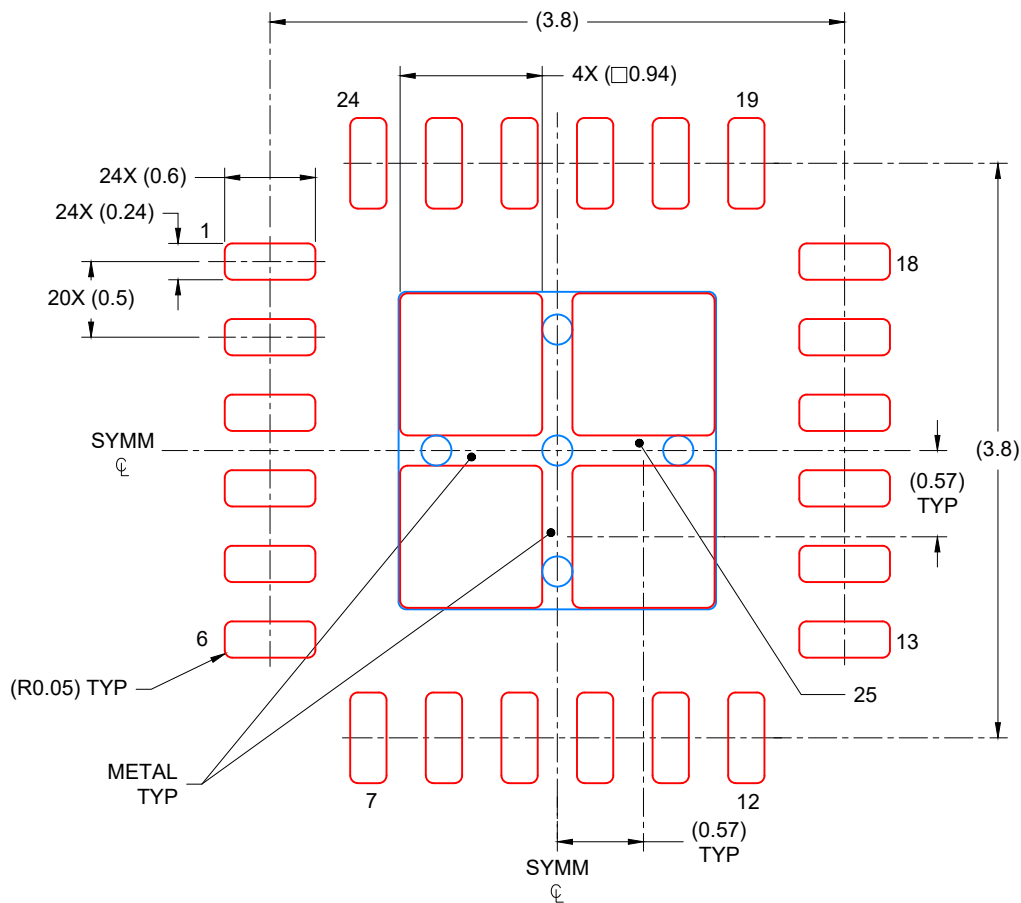
LAND PATTERN EXAMPLE  
SCALE: 20X



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## NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 80% PRINTED COVERAGE BY AREA  
 SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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