CDCM9102 Low-Noise Two-Channel 100-MHz Clock Generator

1 Features

- Integrated Low-Noise Clock Generator Including PLL, VCO, and Loop Filter
- Two Low-Noise 100-MHz Clocks (LVPECL, LVDS, or pair of LVCMOS)
  - Support for HCSL Signaling Levels (AC-Coupled)
  - Typical Period Jitter: 21 ps pk-pk
  - Typical Random Jitter: 510 fs RMS
  - Output Type Set by Pins
- Bonus Single-Ended 25-MHz Output
- Integrated Crystal Oscillator Input Accepts 25-MHz Crystal
- Output Enable Pin Shuts Off Device and Outputs
- 5-mm × 5-mm 32-Pin VQFN Package
- ESD Protection Exceeds 2000 V HBM, 500 V CDM
- Industrial Temperature Range (–40°C to 85°C)
- 3.3-V Power Supply

2 Applications

- Reference Clock Generation for PCI Express Gen 1, Gen 2, and Gen 3
- General-Purpose Clocking

3 Description

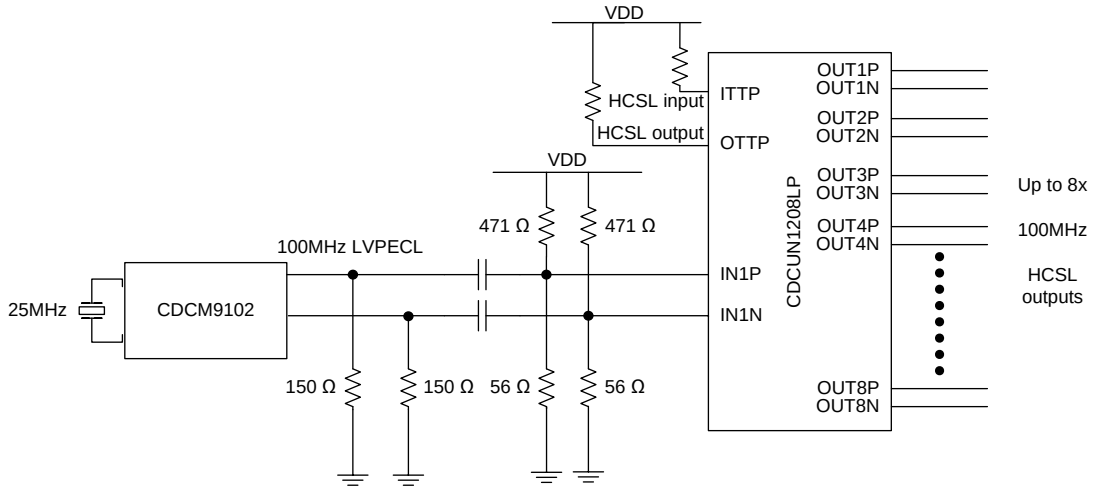
The CDCM9102 is a low-jitter clock generator designed to provide reference clocks for communications standards such as PCI Express™. The device supports up to PCIE gen3 and is easy to configure and use. The CDCM9102 provides two 100-MHz differential clock ports. The output types supported for these ports include LVPECL, LVDS, or a pair of LVCMOS buffers. HCSL signaling is supported using an AC-coupled network. The user configures the output buffer type desired by strapping device pins. Additionally, a single-ended 25-MHz clock output port is provided. Uses for this port include general-purpose clocking, clocking Ethernet PHYs, or providing a reference clock for additional clock generators. All clocks generated are derived from a single external 25-MHz crystal.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCM9102	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2012) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added text to *Description*: The device supports up to PCIE gen3 and is	1
• Changed part number to 1134 25M0000000	11
• Changed part number to FP2500002	11
• Added text and Figure 16 to *PCI Express Applications*	15

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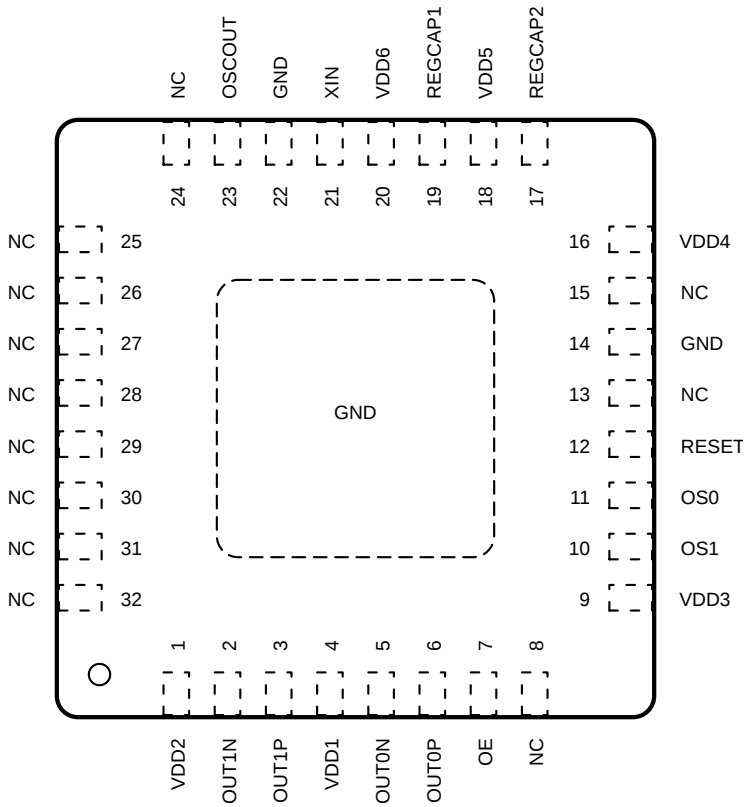
5 Device Comparison Table

PACKAGED DEVICES	FEATURES	T_A
CDCM9102RHBT	32-pin VQFN (RHB) package, small tape and reel	–40°C to 85°C
CDCM9102RHBR	32-pin VQFN (RHB) package, tape and reel	

6 Pin Configuration and Functions

RHB Package
32-Pin VQFN
(Top View)



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
POWER SUPPLIES			
GND	Thermal pad, 14, 22	G	Power supply ground and thermal relief
REGCAP1	19	P	Capacitor for internal regulator, connect 10-µF Y5V capacitor to GND
REGCAP2	17	P	Capacitor for internal regulator, connect 10-µF Y5V capacitor to GND
VDD1	4	P	Power Supply, OUT0 clock port
VDD2	1	P	Power Supply, OUT1 clock port
VDD3	9	P	Power supply, low-noise clock generator
VDD4	16	P	Power supply, low-noise clock generator
VDD5	18	P	Power supply, low-noise clock generator
VDD6	20	P	Power supply, crystal oscillator input

(1) G = Ground, I = Input, O = Output, P = Power

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Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DEVICE CONFIGURATION AND CONTROL			
NC	8, 13, 15, 24–32	—	No connection permitted
OE	7	O	Output enable/shutdown control input (see Table 2)
OS1	10	O	Output format select control inputs (see Table 3)
OS0	11	O	Output format select control inputs (see Table 3)
RESET	12	I	Device reset input (active-low) (see Table 4)[2]
CRYSTAL OSCILLATOR			
XIN	21	I	Parallel resonant crystal input (25 MHz)
DEVICE OUTPUTS			
OSCOUT	23	O	Oscillator output port (25 MHz)
OUT0N	5	O	Output 0 – negative terminal (100 MHz)
OUT0P	6	O	Output 0 – positive terminal (100 MHz)
OUT1N	2	O	Output 1 – negative terminal (100 MHz)
OUT1P	3	O	Output 1 – positive terminal (100 MHz)

(2) For proper device startup, it is recommended that a capacitor be installed from pin 12 to GND. See *Start-Up Time Estimation* for more details.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
I_{IN}	Input current		20	mA
I_{OUT}	Output current		50	mA
V_{DDx}	Supply voltage[2]	–0.5	4.6	V
V_{IN}	Input voltage[3]	–0.5	V_{DDx} + 0.5	V
V_{OUT}	Output voltage[3]	–0.5	V_{DDx} + 0.5	V
T_A	Operating temperature		85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Supply voltages must be applied simultaneously.
(3) The input and output negative voltage ratings may be exceeded if the input and output clamp–current ratings are observed

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DDX}	DC power-supply voltage	3	3.3	3.6	V
T_A	Ambient temperature	–40		85	°C

7.4 Thermal Information

THERMAL METRIC[1][2]		CDCM9102 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	0.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.12	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) 4 × 4 Vias on Pad.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS INPUTS (1)						
V_{IH}	Input high voltage		0.6 × V_{DD}			V
V_{IL}	Input low voltage				0.4 × V_{DD}	V
I_{IH}	Input high current	V_{DD} = 3.6 V, V_{IL} = 0 V			200	µA
I_{IL}	Input low current	V_{DD} = 3 V, V_{IH} = 3.6 V			–200	µA
C_{IN}	Input capacitance			8	10	pF
R_{PU}	Input pullup resistor			150		kΩ
CRYSTAL CHARACTERISTICS (XIN) (2)						
f_{XTAL}	Crystal input frequency	Fundamental mode		25		MHz
ESR	Effective series resistance of crystal				50	Ω
C_{IN}	On-chip load capacitance			8	10	pF
$XTAL_{DL}$	Maximum drive level - XTAL		0.1		1	mW
C_{SHUNT}	Maximum shunt capacitance				7	pF
CLOCK OUTPUT BUFFER (OUTPUT MODE = LVPECL) (3)						
V_{OH}	Output high voltage		V_{DD} – 1.18		V_{DD} – 0.73	V
V_{OL}	Output low voltage		V_{DD} – 2		V_{DD} – 1.55	V
$\|V_{OD}\|$	Differential output voltage		0.6		1.23	V
t_R and t_F	Output rise and fall time	20% to 80%			175	ps
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				20	ps
CLOCK OUTPUT BUFFER (OUTPUT MODE = LVDS) (4)						
$\|V_{OD}\|$	Differential output voltage		0.247		0.454	V
ΔV_{OD}	V_{OD} magnitude change				50	mV
V_{OS}	Common-mode voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} magnitude change				50	mV
t_R and t_F	Output rise and fall time	20% to 80%			255	ps
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				30	ps
CLOCK OUTPUT BUFFER (OUTPUT MODE = LVCMOS) (5)						
V_{OH}	Output high voltage	V_{CC} = 3 V to 3.6 V, I_{OH} = –100 µA	V_{DD} – 0.5			V
V_{OL}	Output low voltage	V_{CC} = 3 V to 3.6 V, I_{OH} = 100 µA			0.3	V
t_{SLEW}	Output rise/fall slew rate	20% to 80%	2.4			V/ns
ODC	Output duty cycle		45%		55%	
t_{SKEW}	Skew between outputs				50	ps

(1) LVCMOS inputs at T_A = –40°C to 85°C
(2) Crystal characteristics for external 25 MHz crystal with V_{DD} = 3.3 V, T_A = –40°C to 85°C
(3) Clock output buffer with output mode = LVPECL at VDD1, VDD2 = 3.3 V; T_A = –40°C to 85°C
(4) Clock output buffer with output mode = LVDS at VDD1, VDD2 = 3.3 V; T_A = –40°C to 85°C
(5) Clock output buffer with output mode = LVCMOS at VDD1, VDD2 = 3.3 V; T_A = –40°C to 85°C

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7.6 Timing Requirements

f_{OUT} = 100 MHz, V_{DD} = 3.3 V, T_A = 25°C, and jitter integration bandwidth between 10 kHz and 20 MHz (unless otherwise noted)

	MIN	TYP	MAX	UNIT
LVCMOS OUTPUT MODE				
Random jitter			507	fs RMS
Period jitter			24.5	ps pk-pk
LVPECL OUTPUT MODE				
Random jitter			510	fs RMS
Period jitter			20.7	ps pk-pk
LVDS OUTPUT MODE				
Random jitter			533	fs RMS
Period jitter			26.5	ps pk-pk

7.7 Typical Characteristics

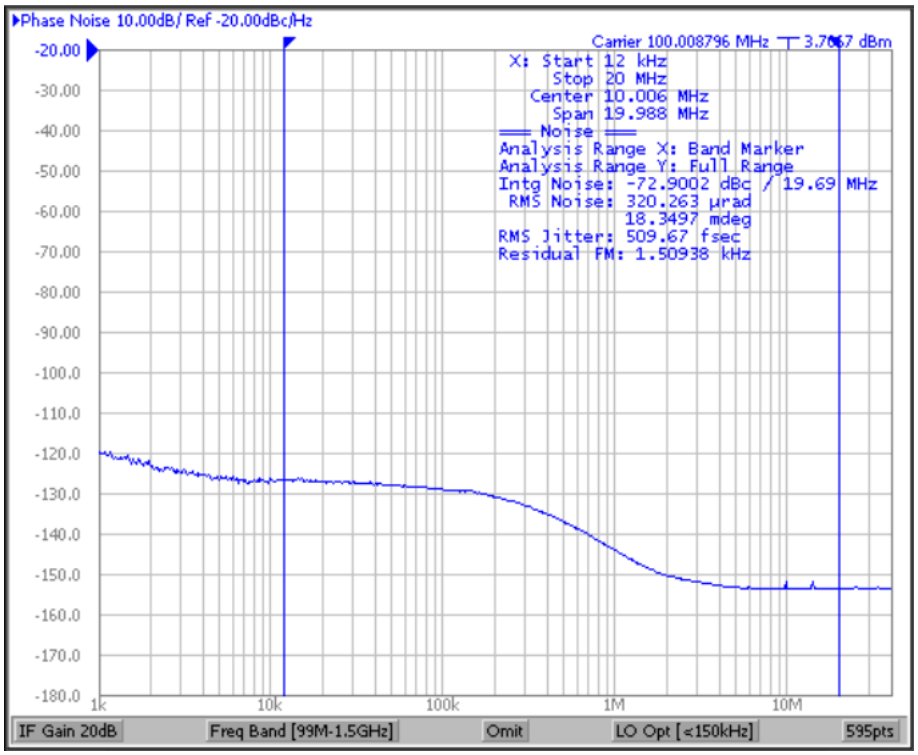

Figure 1. CDCM9102 Typical Phase Noise Performance (LVPECL Mode)

8 Parameter Measurement Information

8.1 Test Configurations

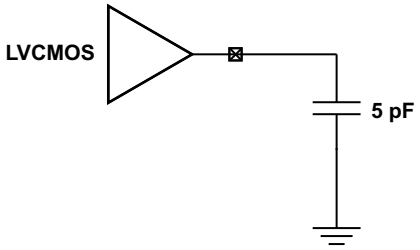

Figure 2. LVCMOS Output Test Load

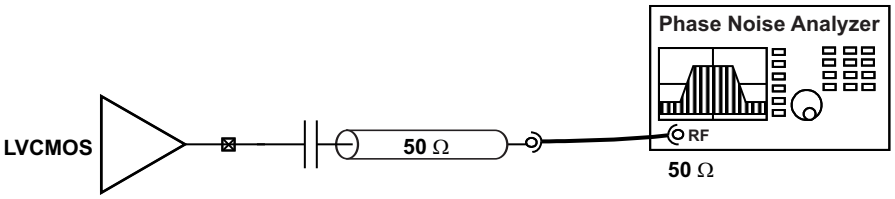

Figure 3. LVCMOS AC Configuration for Device Test

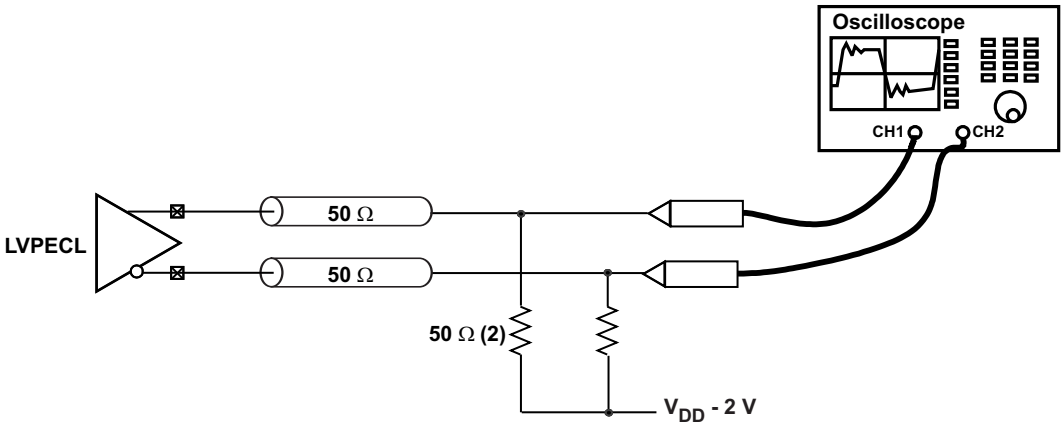

Figure 4. LVPECL DC Configuration for Device Test

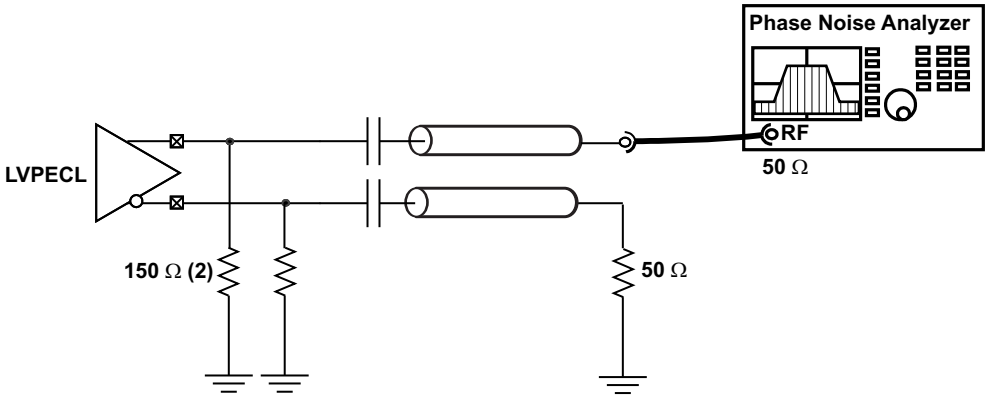

Figure 5. LVPECL AC Configuration for Device Test

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Test Configurations (continued)

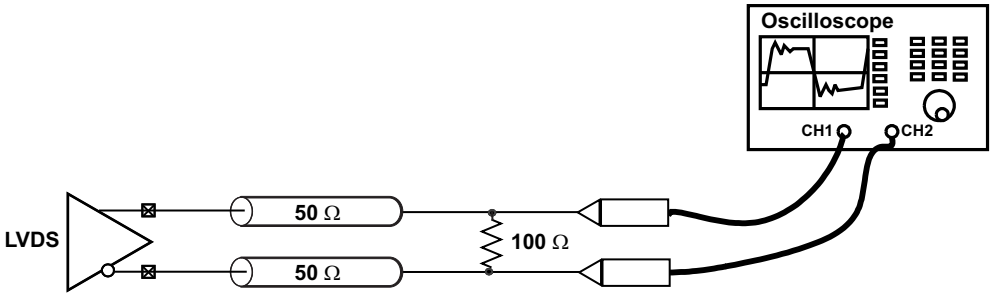


Figure 6. LVDS DC Configuration for Device Test

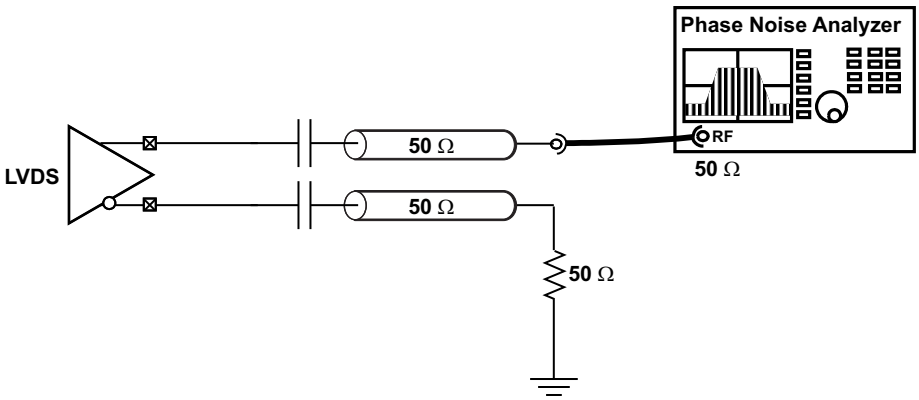


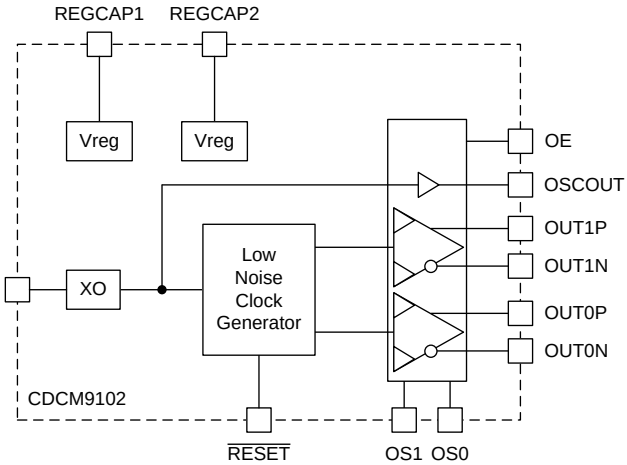
Figure 7. LVDS AC Configuration for Device Test

9 Detailed Description

9.1 Overview

The CDCM9102 is a high-performance PLL that generates 2 copies of commonly-used reference clocks with less than 1-ps RMS jitter from a low-cost crystal.

9.2 Functional Block Diagrams



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9.3 Feature Description

The CDCM9102 includes an on-chip PLL with an on-chip VCO. The PLL blocks consist of a crystal input interface, a phase frequency detector (PFD), a charge pump, an on-chip loop filter, and prescaler and feedback dividers. Completing the CDCM9102 device are the output divider and universal output buffer. The PLL and output divider are pre-programmed to generate 2 copies of 100 MHz in LVCMOS, LVPECL or LVDS format.

The PLL is powered by on-chip, low-dropout (LDO) linear voltage regulators. The regulated supply network is partitioned such that the sensitive analog supplies are powered from separate LDOs rather than the digital supplies which use a separate LDO regulator. These LDOs provide isolation for the PLL from any noise in the external power-supply rail. The REG_CAP1 and REG_CAP2 pins should each be connected to ground by 10-µF capacitors to ensure stability.

9.4 Device Functional Modes

9.4.1 Crystal Input (XIN) Interface

The CDCM9102 implements a *Colpitts oscillator*; therefore, one side of the crystal connects to the XIN pin and the other crystal terminal connects to ground. The device requires the use of a fundamental-mode crystal, and the oscillator operates in parallel resonance mode. The correct load capacitance is necessary to ensure that the circuit oscillates properly. The load capacitance comprises all capacitances in the oscillator feedback loop (the capacitances seen between the terminals of the crystal in the circuit). It is important to account for all sources of capacitance when calculating the correct value for the external discrete load capacitance shown in Figure 8.

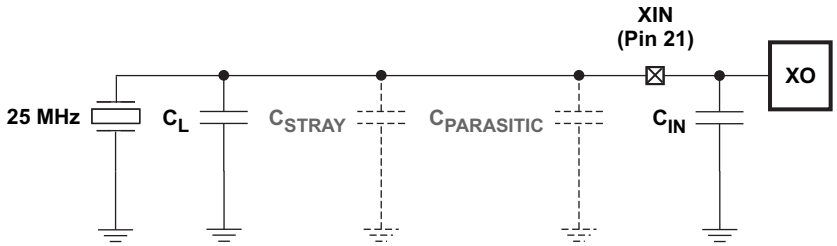

Figure 8. Configuration of Circuit for CDCM9102 XIN Oscillator

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Device Functional Modes (continued)

The CDCM9102 has been characterized with 10-pF parallel-resonant crystals. The input stage of the crystal oscillator in the CDCM9102 is designed to oscillate at the correct frequency for all parallel-resonant crystals with low-pull capability and rated with a load capacitance that is equal to the sum of the on-chip load capacitance at the XIN pin (C_{IN} = 10 pF maximum), crystal stray capacitance, and board parasitic capacitance between the crystal and XIN pin. To minimize stray and parasitic capacitances, minimize the trace distance routed from the crystal to the XIN pin and avoid other active traces and active circuitry in the area of the crystal oscillator circuit. Table 1 lists crystal types that have been evaluated with the CDCM9102.

Table 1. CDCM9102 Crystal Recommendations

MANUFACTURER	PART NUMBER
Vectron	VXC1-1134 25M0000000
Fox	218-3
Saronix	FP2500002

A mismatch of the load capacitance results in a frequency error according to Equation 1.

$$\frac{\Delta f}{f} = \frac{C_S}{2\left(C_{Lr} + C_O\right)} - \frac{C_S}{2\left(C_{La} + C_O\right)}$$

where

- Δf is the frequency error required by the application.
- f is the fundamental frequency of the crystal.
- C_S is the motional capacitance of the crystal. This is a parameter in the data sheet of the crystal.
- C_0 is the shunt capacitance of the crystal. This is a parameter in the data sheet of the crystal.
- C_{Lr} is the rated load capacitance of the crystal. This is a parameter in the data sheet of the crystal.
- C_{La} is the actual load capacitance implemented on the PCB (C_{IN} + stray capacitance + parasitic capacitance + C_L). (1)

The difference between the rated load capacitance (from the crystal datasheet) and the actual load capacitance ($C_{La} = C_{IN} + C_L + C_{STRAY} + C_{PARASITIC}$) should be minimized. A crystal with a low pullability rating (low C_S) is ideal.

Design Example:

Desired frequency tolerance Δf ≤ ±80 ppm

Crystal Vendor Parameters:

Intrinsic Frequency Tolerance = ±30 ppm

C_0 = 7 pF (shunt capacitance)

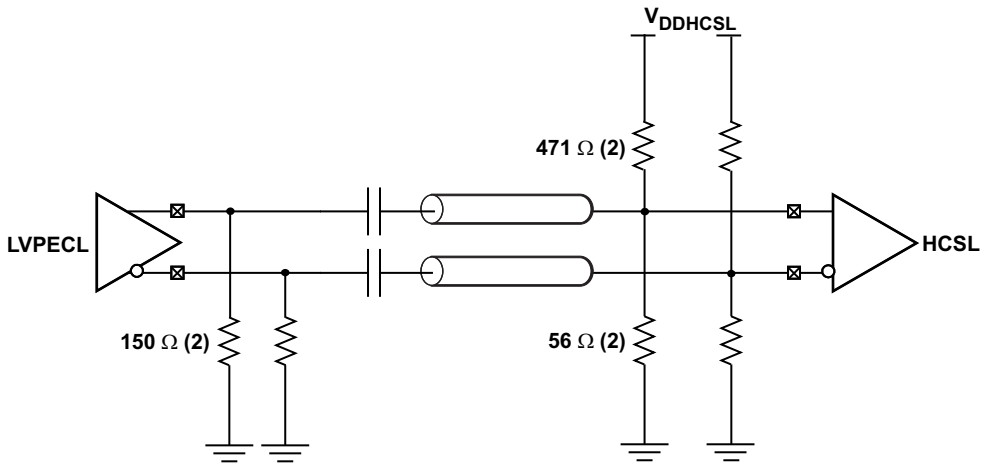
C_S = 10 fF (motional capacitance)

C_{Lr} = 12 pF (load capacitance)

Substituting these parameters into Equation 1 yields a maximum value of C_{La} = 17 pF to achieve the desired Δf (±50 ppm). Recall that $C_{La} = C_{IN} + C_L + C_{STRAY} + C_{PARASITIC}$ = 8 pF + ($C_L + C_{STRAY} + C_{PARASITIC}$). Ideally, the load presented to this crystal should be 12 pF; therefore, the sum of ($C_L + C_{STRAY} + C_{PARASITIC}$) must be less than 9 pF. Stray and parasitic capacitance must be controlled. This is because the Colpitts oscillator is particularly sensitive to capacitance in parallel with the crystal; therefore, good layout practice is essential. TI recommends that the designer extract the stray and parasitic capacitance from the printed-circuit board design tool and adjust C_L accordingly to achieve $C_{Lr} = C_{La}$. In common scenarios, the external load capacitor is often unnecessary; however, TI recommends that pads be implemented to accommodate an external load capacitor so that the ppm error can be minimized.

9.4.2 Interfacing between LVPECL and HCSL (PCI Express)

Certain PCI Express applications require HCSL signaling. Because the common-mode voltage for LVPECL and HCSL are different, applications requiring HCSL signaling must use AC-coupling as shown in Figure 9. The 150-Ω resistors ensure proper biasing of the CDCM9102 LVPECL output stage. The 471-Ω and 56-Ω resistor network biases the HCSL receiver input stage.



C_{IN} = 8 pF (typical), 10 pF (maximum); see *Electrical Characteristics.*

Figure 9. Interfacing Between LVPECL and HCSL

9.5 Programming

Table 2 and Table 3 list the pin controls and pin configurations of the CDCM9102 output. Table 4 lists the device reset.

9.5.1 Device Configuration

Table 2. CDCM9102 Pin Control of Output Enable

OE (Pin 7)	MODE	DEVICE CORE	OUTPUT
0	Power down	Power down	Hi-Z
1	Normal	Active	Active

Table 3. CDCM9102 Pin Configuration of Output Type

CONTROL PINS		OUTPUT MODE
OS1 (Pin 10)	OS0 (Pin 11)	
0	0	LVCMOS, OSCOUT = OFF
0	1	LVDS, OSCOUT = OFF
1	0	LVPECL, OSCOUT = OFF
1	1	LVPECL, OSCOUT = ON

Table 4. CDCM9102 Device Reset

RESET (Pin 12)	OPERATING MODE	DEVICE OUTPUTS
0	Device reset	Hi-Z
0 → 1	Clock generator calibration	Hi-Z
1	Normal	Active

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Start-Up Time Estimation

The CDCM9102 contains a low-noise clock generator that calibrates to an optimal operating point at device power up. To ensure proper device operation, the oscillator must be stable before the low-noise clock generator calibration procedure. Quartz-based oscillators can take up to 2 ms to stabilize; therefore, TI recommends that the application ensure that the RESET pin is de-asserted at least 5 ms after the power supply has finished ramping. This can be accomplished by controlling the RESET pin directly, or by applying a 47-nF capacitor to ground on the RESET pin (this provides a delay because the RESET pin includes a 150-kΩ pullup resistor.

The CDCM9102 start-up time can be estimated based on parameters defined in Table 5 and graphically shown in Figure 10.

Table 5. CDCM9102 Start-Up Time Dependencies

PARAMETER	DEFINITION	DESCRIPTION	FORMULA OR METHOD OF DETERMINATION
t_{REF}	Reference clock period	The reciprocal of the applied reference frequency in seconds	$t_{REF} = \frac{1}{f_{REF}} = 0.04\ \mu s$
t_{pul}	Power-up time (low limit)	Power-supply rise time to low limit of power-on-reset trip point	Time required for power supply to ramp to 2.27 V
t_{puh}	Power-up time (high limit)	Power supply rise time to high limit of power-on-reset trip point	Time required for power supply to ramp to 2.64 V
t_{rsu}	Reference start-up time	After POR releases, the Colpitts oscillator is enabled. This start-up time is required for the oscillator to generate the requisite signal levels for the delay block to be clocked by the reference input.	500 µs best case and 800 µs worst case (for a crystal input)
t_{delay}	Delay time	Internal delay time generated from the reference clock. This delay provides time for the reference oscillator to stabilize.	$t_{delay} = 16{,}384 \times t_{REF} = 655\ \mu s$
t_{VCO_CAL}	VCO calibration time	VCO calibration time generated from the reference clock. This process selects the operating point for the VCO based on the PLL settings.	$t_{VCO_CAL} = 550 \times t_{REF} = 22\ \mu s$
t_{PLL_LOCK}	PLL lock time	Time requried for PLL to lock within ±10 ppm of f_{REF}	The PLL settles in 12.5 µs

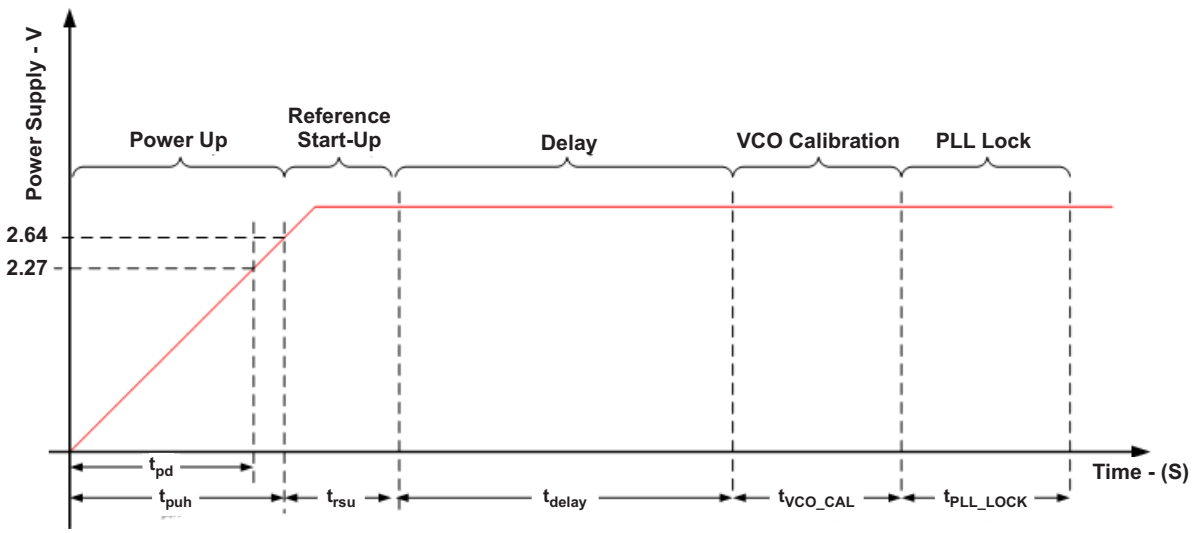

Figure 10. CDCM9102 Start-Up Time Dependencies

The CDCM9102 start-up time limits, t_{MAX} and t_{MIN}, can now be calculated with Equation 2 and Equation 3.

$$t_{MAX} = t_{puh} + t_{rsu} + t_{delay} + t_{VCO_CAL} + t_{PLL_LOCK} \quad (2)$$

$$t_{MIN} = t_{pul} + t_{rsu} + t_{delay} + t_{VCO_CAL} + t_{PLL_LOCK} \quad (3)$$

10.1.2 Output Termination

The CDCM9102 is a 3.3-V clock driver which has the following options for the output type: LVPECL, LVDS, and LVCMOS.

10.1.3 LVPECL Termination

The CDCM9102 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination is required to ensure correct operation of the device and to optimize signal integrity. The proper termination for LVPECL is 50 Ω to (Vcc-2) V but this DC voltage is not readily available on a board. Thus a Thevenin's equivalent circuit is worked out for the LVPECL termination in both direct-coupled (DC) and AC-coupled cases, as shown in Figure 11 and Figure 12. TI recommends placing all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, AC coupling is required.

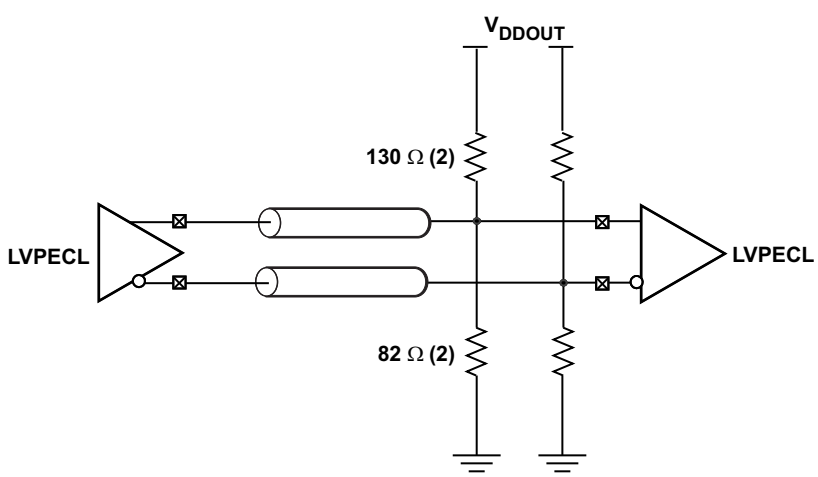

Figure 11. LVPECL Output Termination (DC-Coupled)

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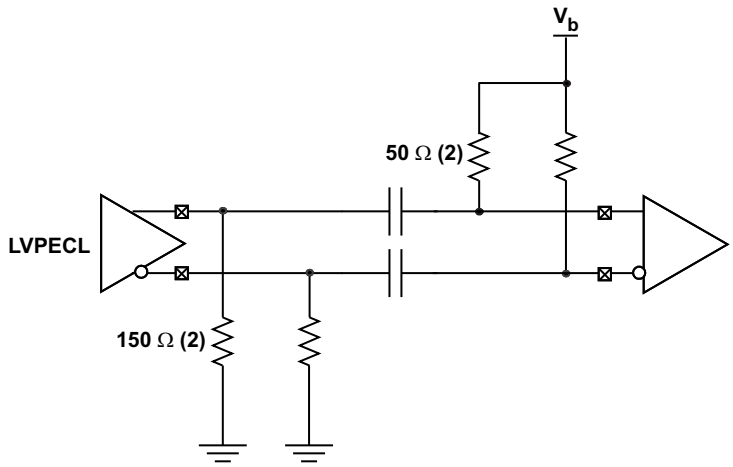

Figure 12. LVPECL Output Termination (AC-Coupled)

10.1.4 LVDS Termination

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either a direct-coupled (dc) termination or ac-coupled termination can be used for LVDS outputs, as shown in Figure 13 and Figure 14. TI recommends placing all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, AC coupling is required.

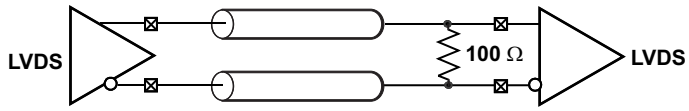

Figure 13. LVDS Output Termination (DC Coupled)

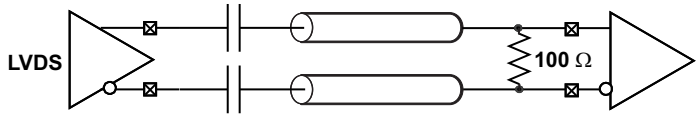

Figure 14. LVDS Output Termination (AC Coupling)

10.1.5 LVCMOS Termination

Series termination is a common method to maintain the signal integrity for LVCMOS drivers, if connected to a receiver with a high-impedance input. For series termination, a series resistor, Rs, is placed close to the driver, as shown in Figure 15. The sum of the driver impedance and Rs should be close to the transmission-line impedance, which is usually 50 Ω. Because the LVCMOS driver in the CDCM9102 has an impedance of 30 Ω, TI recommends Rs be 22 Ω to maintain proper signal integrity.

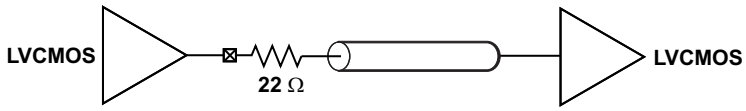

Figure 15. LVCMOS Output Termination

10.1.6 PCI Express Applications

Texas Instruments offers a complete clock solution for PCI Express applications. The CDCUN1208LP can be used to fan out reference clock generated by the CDCM9102 as shown in Figure 16.

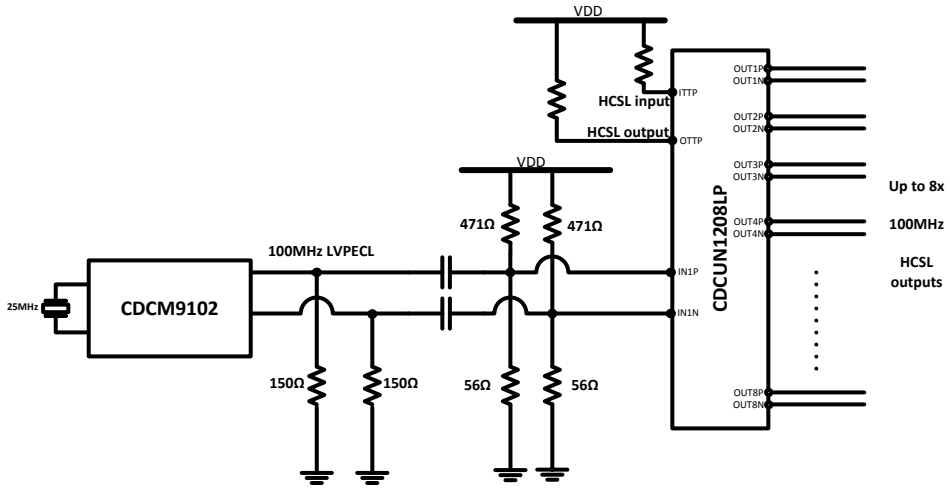

Figure 16. Clock Solution for PCIE Express Applications

10.2 Typical Application

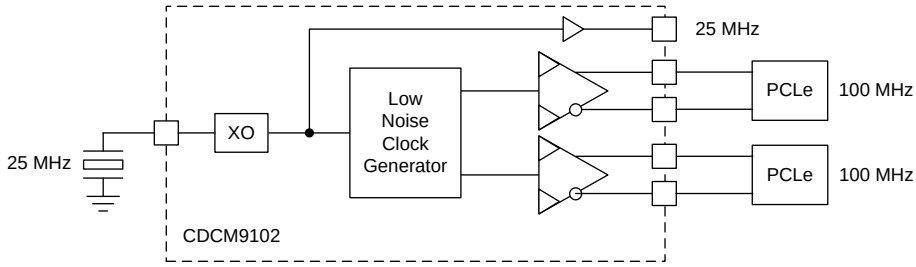

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Figure 17. CDCM9102 Typical Application Example

10.2.1 Design Requirements

Consider a typical wired communications application, like a top-of-rack switch, which needs to clock PCI Express Gen 2 or 3 PHYs. For such asynchronous systems, the reference input can be a crystal. In such systems, the clocks are expected to be available upon power up without the need for any device-level programming. An example of clock input and output requirements is shown below:

- Clock Input:
  - 25-MHz crystal
- Clock Outputs:
  - 2× 100 MHz clock for PCI Express Gen 3 (8 GT/s), LVPECL

See *Detailed Design Procedure* for how to generate the required output frequencies for this application using the CDCM9102.

Typical Application (continued)

10.2.2 Detailed Design Procedure

Design of all aspects of the CDCM61004 is quite involved and software support is available to assist in part selection and phase noise simulation. This design procedure will give a quick outline of the process.

1. Device Selection
   - The first step is to calculate the VCO frequency given the required output frequency. The device must be able to produce the VCO frequency that can be divided down to the required output frequency.
   - The WEBENCH Clock Architect Tool from TI will aid in the selection of the right device that meets the customer's output frequencies and format requirements.
2. Device Configuration
   - The WEBENCH Clock Architect Tool attempts to maximize the phase detector frequency, use smallest dividers, and maximizes PLL bandwidth.

10.2.2.1 Device Selection

Use the WEBENCH Clock Architect Tool. Enter the required frequencies and formats into the tool. To use this device, find a solution using the CDCM9102.

10.2.2.1.1 Calculation Using LCM

In this example, the valid VCO frequency for CDCM9102 is 1.8 GHz.

10.2.2.2 Device Configuration

For this example, when using the WEBENCH Clock Architect Tool, the reference would have been manually entered as 25 MHz according to input frequency requirements. Enter the desired output frequencies and click on Generate Solutions. Select CDCM9102 from the solution list.

From the simulation page of the WEBENCH Clock Architect Tool, it can be seen that to maximize phase detector frequencies, the N divider is set to 24 and prescaler divider is set to 3. This results in a VCO frequency of 1.8 GHz. The output divider is set to 6. At this point the design meets all input and output frequency requirements and simulate performance on the clock outputs. Figure 18 shows the typical phase noise plot of the 100 MHz LVPECL output.

Typical Application (continued)

10.2.3 Application Curve

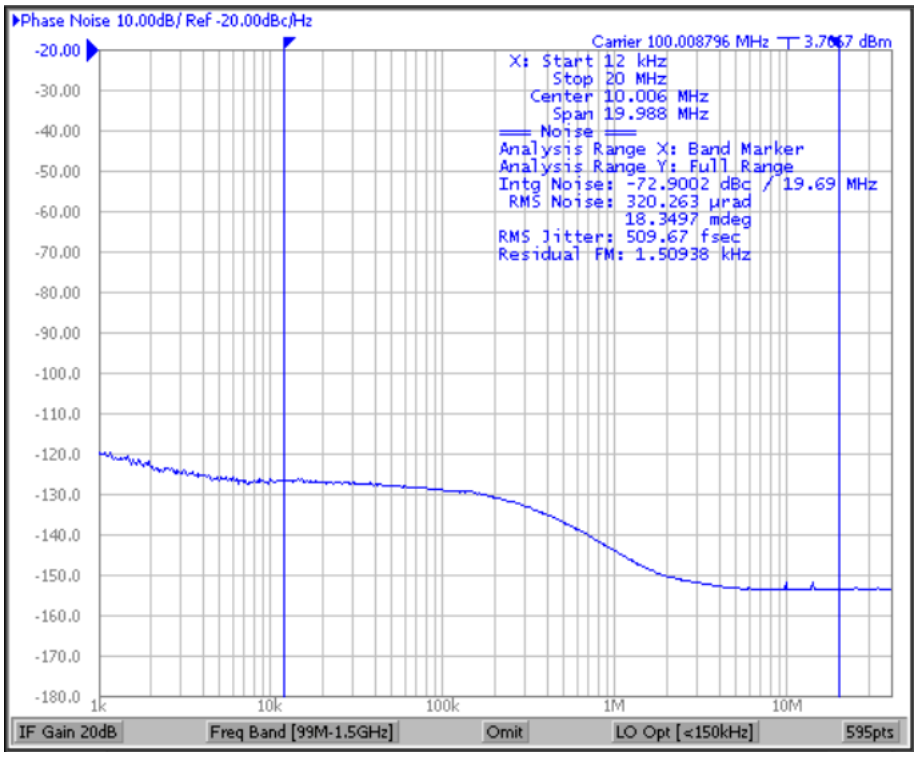

Figure 18. Typical Phase Noise Plot of 100 MHz LVPECL Output

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11 Power Supply Recommendations

T_A = –40°C to 85°C, VDDx = 3.3 V, OE = 1, values represent cumulative current/power on all VDDx pins.

Table 6. Device Current Consumption

BLOCK	CONDITION	CURRENT (mA)	DEVICE POWER (mW)	EXTERNAL RESISTOR POWER (mW)
Entire device, core current		85	280	
Output Buffers	LVPECL	28	42.4	50
	LVDS	20	66	
	LVCMOS	$V \times f_{out} \times (C_L + 20 \times 10^{-12}) \times 10^3$	$V^2 \times f_{out} \times (C_L + 20 \times 10^{-12}) \times 10^3$	

11.1 Thermal Management

To ensure optimal performance and reliability, good thermal design practices are important when using the CDCM9102. Die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times $R_{\theta JA}$ should not exceed 125°C.

The device package has an exposed pad that provides the primary heat removal path as well as an electrical grounding to the printed circuit board (PCB). To maximize the removal of heat from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. A recommended land and via pattern is shown in Figure 19.

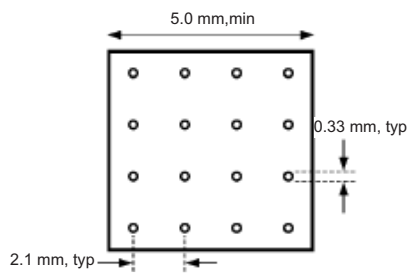

Figure 19. Recommended PCB Layout for CDCM9102

11.2 Power Supply Filtering

PLL-based frequency synthesizers are very sensitive to noise on the power supply, which can dramatically increase the jitter of the PLL. This is especially true for analog-based PLLs. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL has attenuated jitter due to power supply noise at frequencies beyond the PLL bandwidth due to attenuation by the loop response.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low-impedance path for high-frequency noise and guard the power supply system against induced fluctuations. The bypass capacitors also provide a source of instantaneous current as required by the device output stages. Therefore, bypass capacitors must have low ESR. To properly use the bypass capacitors, they must be placed very close to the power supply pins and must be laid out with short loops to minimize inductance.

Figure 20 shows a general recommendation for decoupling the power supply. The CDCXM9102 power supplies fall into one of two categories: analog supplies (VDD3, VDD4, and VDD5), and input/output supplies (VDD1, VDD2, and VDD6). Short the analog supplies together to form the analog supply node; likewise, short the input/output supplies together to form the I/O supply node. Isolate the analog node from the PCB power supply and I/O node by inserting a ferrite bead. This helps isolate the high-frequency switching noises generated by the clock drivers and I/O from the sensitive analog supply node. Choosing an appropriate ferrite bead with low dc resistance is important, as it is imperative to maintain a voltage at the power-supply pin of the CDCM9102 that is over the minimum voltage needed for its proper operation.

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Power Supply Filtering (continued)

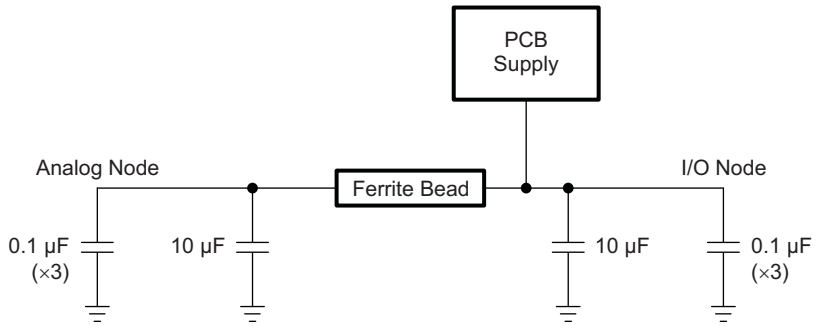

Figure 20. CDCM9102 Power Supply Decoupling – Power Pin Bypass Concept

12 Layout

12.1 Layout Guidelines

The CDCM9102 is a high-performance device; therefore, pay careful attention to device configuration and printed-circuit board layout with respect to power consumption. Observing good thermal layout practices enables the thermal pad on the backside of the 32-pin VQFN package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

12.2 Layout Example

Figure 21 shows a general recommendation of PCB layout with the CDCM9102 that ensures good system-level thermal reliability.

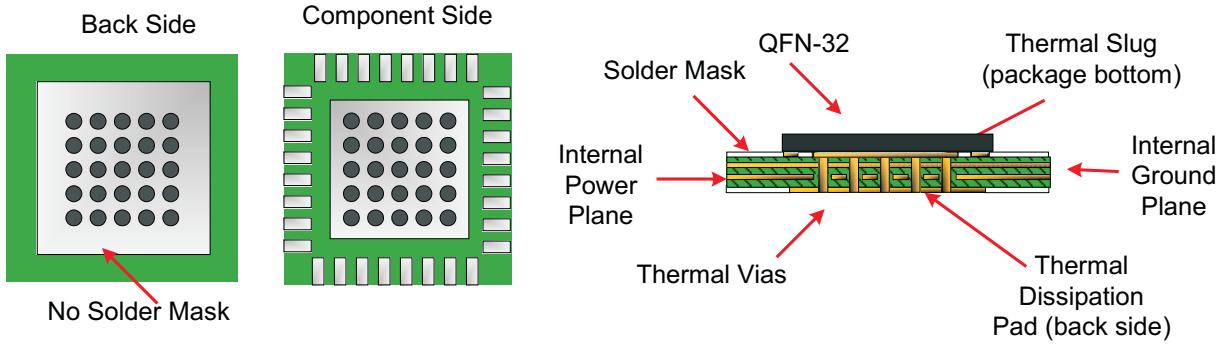

Figure 21. Recommended PCB Layout

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13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.
PCI Express is a trademark of PCI-SIG.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCM9102RHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 9102
CDCM9102RHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 9102
CDCM9102RHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 9102
CDCM9102RHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	CDCM 9102

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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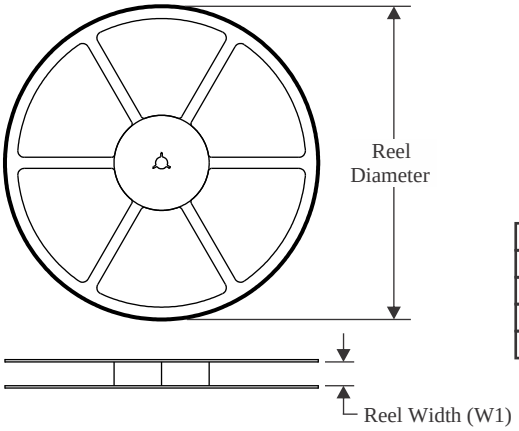
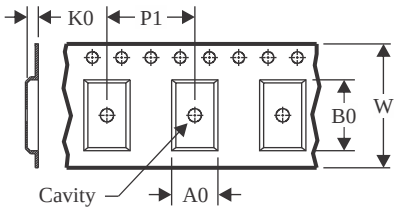
TAPE AND REEL INFORMATION

REEL DIMENSIONS

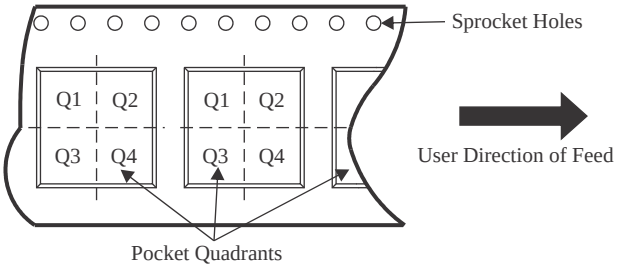


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

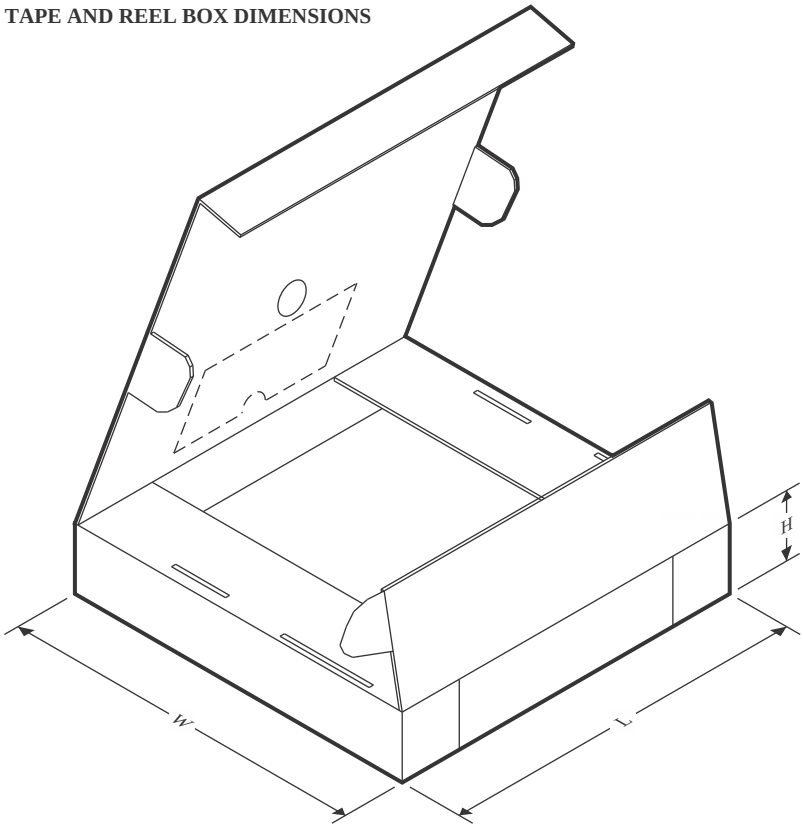
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM9102RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
CDCM9102RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM9102RHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
CDCM9102RHBT	VQFN	RHB	32	250	213.0	191.0	35.0

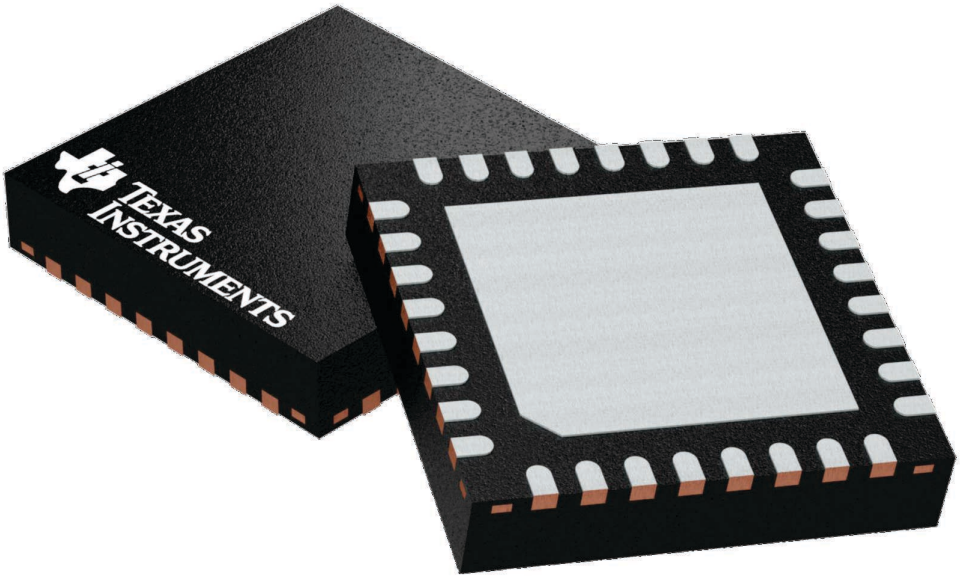
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

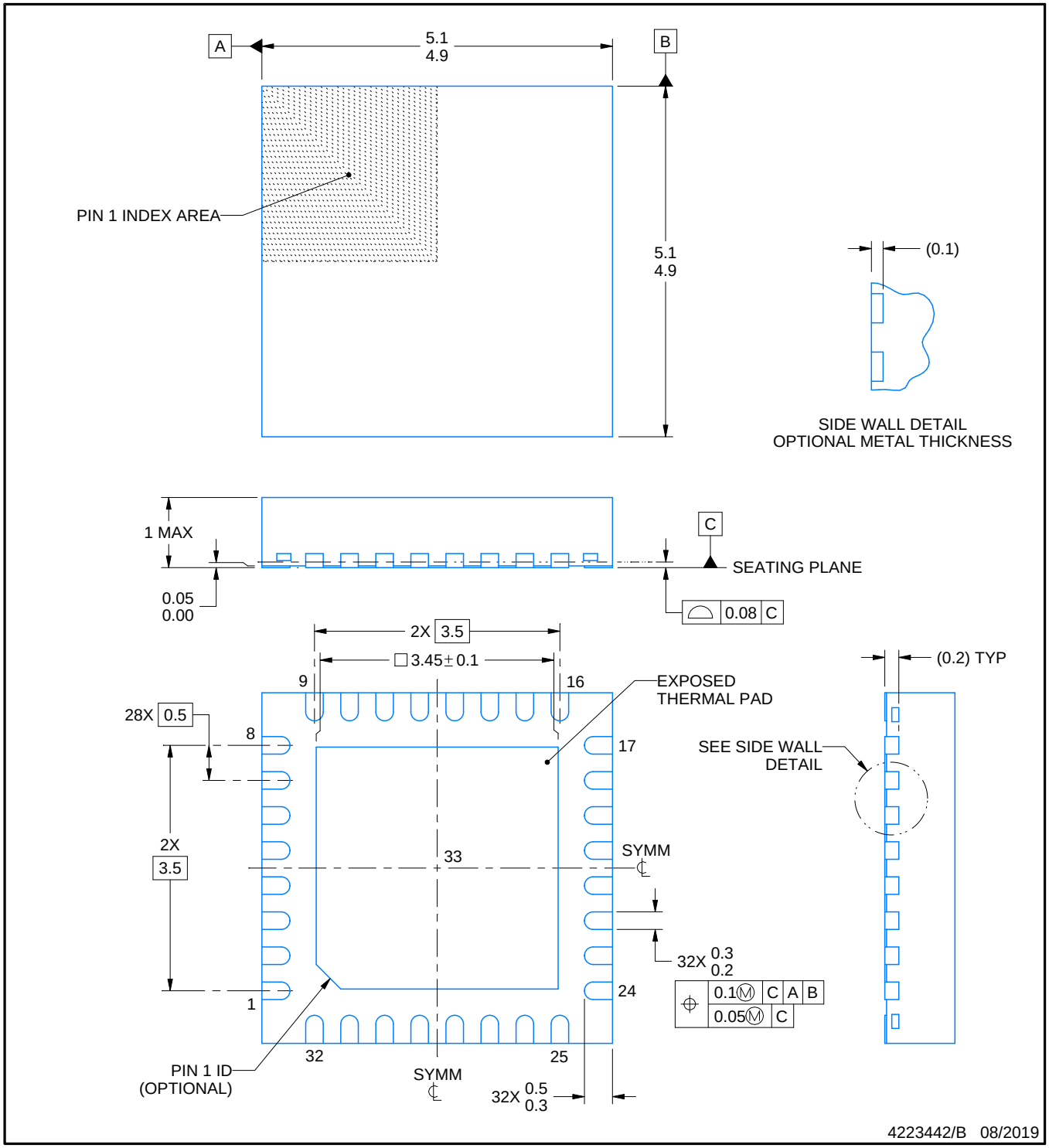
4224745/A

RHB0032E

PACKAGE OUTLINE

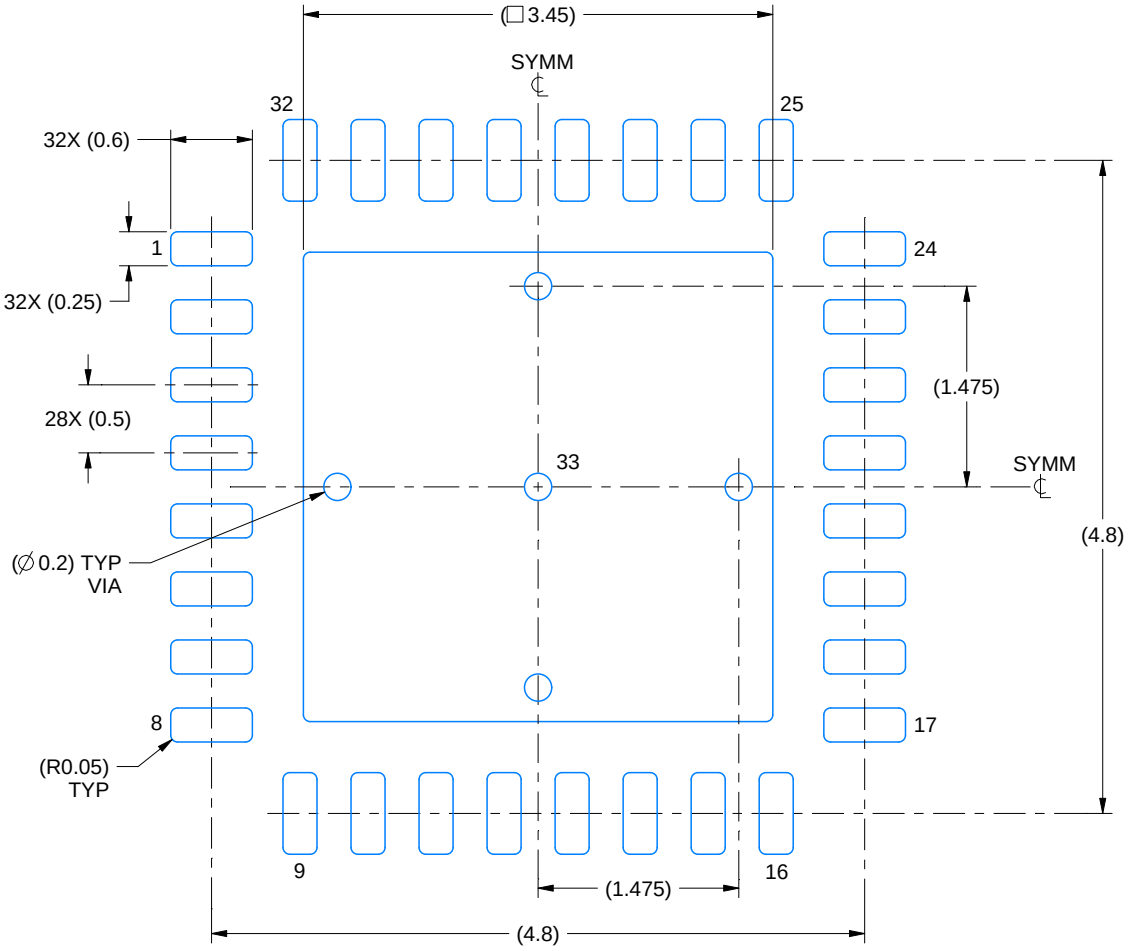
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

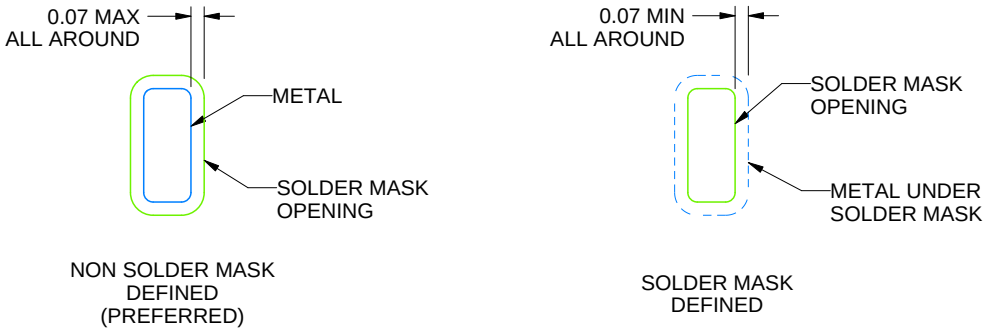


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

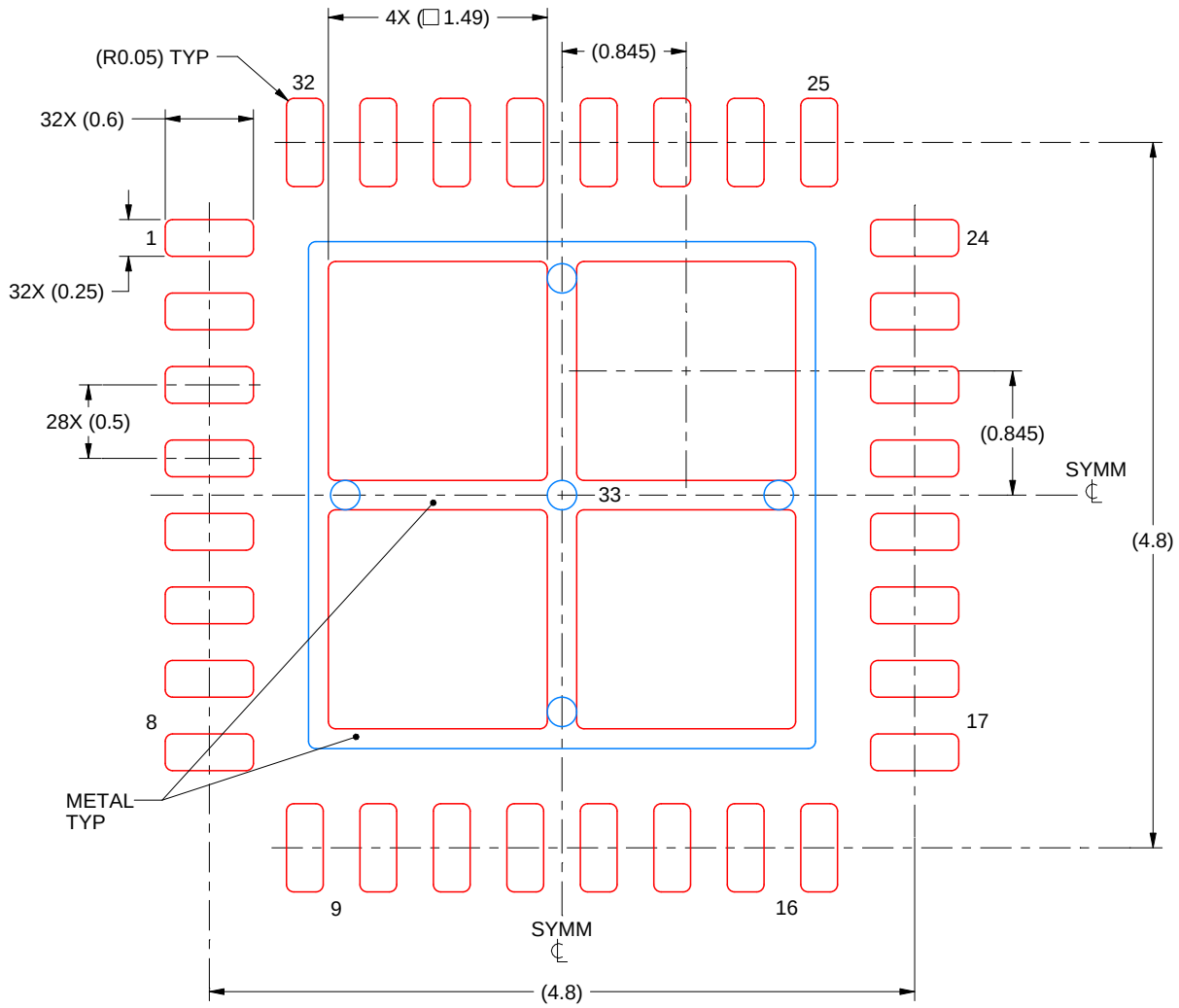


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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