LP38856 3-A Fast-Response High-Accuracy LDO Linear Regulator With Enable

1 Features

- Input Voltage: 1.1 V to 5.5 V
- Wide V_{BIAS} Supply Operating Range: 3 V to 5.5 V
- Standard V_{OUT}: 0.8 V and 1.2 V
- Stable with 10-µF Ceramic Capacitors
- Dropout Voltage of 240 mV (Typical) at 3-A Load Current
- Precision Output Voltage Across All Line and Load Conditions:
  - ±1% for T_J = 25°C
  - ±2% for 0°C ≤ T_J ≤ +125°C
  - ±3% for –40°C ≤ T_J ≤ +125°C
- Overtemperature and Overcurrent Protection
- –40°C to +125°C Operating Temperature Range

2 Applications

- ASIC Power Supplies In:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulator

3 Description

The LP38856 is a high-current, fast-response regulator which can maintain output voltage regulation with an extremely low input-to-output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: V_{BIAS} provides power for the internal bias and control circuits, as well as drive for the gate of the N-MOS power transistor, while V_{IN} supplies power to the load. The use of an external bias rail allows the part to operate from ultra-low V_{IN} voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of this device makes it suitable for use in powering DSP, microcontroller core voltages, and switch mode power supply post regulators. The LP38856 is available in 5-pin TO-220 and DDPAK/TO-263 packages.

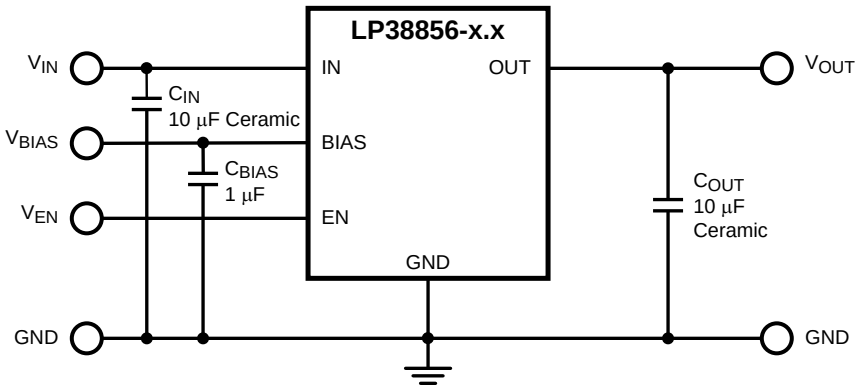
- Dropout Voltage: 240 mV (typical) at 3-A load current.
- Low Ground Pin Current: 10 mA (typical) at 3-A load current.
- Shutdown Current: 1 µA (typical) $I_{IN(GND)}$ when EN pin is low.
- Precision Output Voltage: ±1% for T_J = 25°C and ±2% for 0°C ≤ T_J ≤ +125°C, across all line and load conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP38856	DDPAK/TO-263 (5)	10.16 mm × 8.42 mm
	TO-220 (5)	14.986 mm × 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 3
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 4
6.6 Typical Characteristics ... 6
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 11
8 Application and Implementation ... 12
8.1 Application Information ... 12
8.2 Typical Application ... 12
9 Power Supply Recommendations ... 14
10 Layout ... 15
10.1 Layout Guidelines ... 15
10.2 Layout Example ... 15
11 Device and Documentation Support ... 16
11.1 Community Resources ... 16
11.2 Trademarks ... 16
11.3 Electrostatic Discharge Caution ... 16
11.4 Glossary ... 16
12 Mechanical, Packaging, and Orderable Information ... 17

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F	Page
• Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; remove lead temp from Abs Max (in POA), remove obsolete heatsinking content	1

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National data sheet to TI format	14

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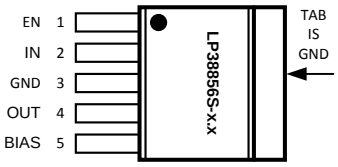
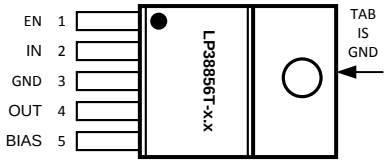
5 Pin Configuration and Functions

KTT Package
5-Pin DDPAK/TO-263
Top View



NDH Package
5-Pin TO-220
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	EN	I	The device enable pin.
2	IN	I	The unregulated input voltage pin
3	GND	—	Ground
4	OUT	O	The regulated output voltage pin
5	BIAS	I	The supply for the internal control and reference circuitry
TAB	TAB	—	The TAB is a thermal connection that is physically attached to the backside of the die, and is used as a thermal heat-sink connection. See the *Application and Implementation* section for details

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	Power dissipation(3)	Internally limited		
V_{IN}	Supply voltage (survival)	–0.3	6	V
V_{BIAS}	Supply voltage (survival)	–0.3	6	V
V_{EN}	Voltage (survival)	–0.3	6	V
V_{OUT}	Voltage (survival)	–0.3	6	V
I_{OUT}	Current (survival)	Internally Limited		
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.
(3) Device power dissipation must be de-rated based on device power dissipation (T_D), ambient temperature (T_A), and package junction to ambient thermal resistance ($R_{\theta JA}$). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See *Application and Implementation* for details.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	(V_{OUT} + V_{DO})		V_{BIAS}	
V_{BIAS}	Supply voltage	3		5.5	V
V_{EN}	Enable input voltage	0.0		V_{BIAS}	
I_{OUT}	Output current	0		3	mA/A
	Junction temperature range[2]	–40		125	°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits (see *Electrical Characteristics*). Specifications do not apply when operating the device outside of its rated operating conditions.
(2) Device power dissipation must be de-rated based on device power dissipation (T_D), ambient temperature (T_A), and package junction to ambient thermal resistance ($R_{\theta JA}$). Additional heat-sinking may be required to ensure that the device junction temperature (T_J) does not exceed the maximum operating rating. See *Application and Implementation* for details.

6.4 Thermal Information

THERMAL METRIC[1]		LP38856		UNIT
		KTT (DDPAK/TO-263)	NDH (TO-220)	
		5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	32.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.0	43.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.8	18.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.1	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.8	18.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise specified: V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10 µF, C_{BIAS} = 1 µF, V_{EN} = V_{BIAS}. Limits apply for T_J = 25°C only unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output Voltage Tolerance	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ V_{BIAS} 3 V ≤ V_{BIAS} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 3 A	–1%	0%	+1%	
		$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ V_{BIAS} 3 V ≤ V_{BIAS} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 3 A T_J = –40°C to 125°C	–3%		3%	
		$V_{OUT(NOM)}$ + 1V ≤ V_{IN} ≤ V_{BIAS} 3 V ≤ V_{BIAS} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 3.0A 0°C ≤ T_J ≤ 125°C	–2%	0%	2%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation, V_{IN}[1]	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ V_{BIAS}		0.04		%/V
$\Delta V_{OUT}/\Delta V_{BIAS}$	Line regulation, V_{BIAS}[1]	3 V ≤ V_{BIAS} ≤ 5.5 V		0.10		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output voltage load regulation[2]	10 mA ≤ I_{OUT} ≤ 3 A		0.2		%/A
V_{DO}	Dropout voltage, V_{IN} – V_{OUT}[3]	I_{OUT} = 3 A		240	300	mV
		I_{OUT} = 3 A, T_J = –40°C to 125°C			450	

(1) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(2) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.
(3) Dropout voltage is defined the as input to output voltage differential (V_{IN} - V_{OUT}) where the input voltage is low enough to cause the output voltage to drop no more than 2% from the nominal value

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Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1$ V, $V_{BIAS} = 3$ V, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT} = 10$ µF, $C_{BIAS} = 1$ µF, $V_{EN} = V_{BIAS}$. Limits apply for $T_J = 25°C$ only unless otherwise specified. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{GND(IN)}$	Ground pin current drawn from V_{IN} supply	LP38856-0.8: 10 mA ≤ I_{OUT} ≤ 3 A		7	8.5	mA
		LP38856-0.8: 10 mA ≤ I_{OUT} ≤ 3 A T_J = –40°C to 125°C			9	
		LP38856-1.2: 10 mA ≤ I_{OUT} ≤ 3 A		11	12	
		LP38856-1.2: 10 mA ≤ I_{OUT} ≤ 3 A T_J = –40°C to 125°C			15	
		V_{EN} ≤ 0.5 V		1	10	µA
		V_{EN} ≤ 0.5 V, T_J = –40°C to 125°C			300	
$I_{GND(BIAS)}$	Ground pin current drawn from V_{BIAS} supply	10 mA ≤ I_{OUT} ≤ 3 A		3	3.8	mA
		10 mA ≤ I_{OUT} ≤ 3 A T_J = –40°C to 125°C			4.5	
		V_{EN} ≤ 0.5 V		100	170	µA
		V_{EN} ≤ 0.5 V, T_J = –40°C to 125°C			200	
UVLO	Undervoltage lock-out threshold	V_{BIAS} rising until device is functional	2.20	2.45	2.70	V
		V_{BIAS} rising until device is functional T_J = –40°C to 125°C	2		2.9	
$UVLO_{(HYS)}$	Undervoltage lock-out hysteresis	V_{BIAS} falling from UVLO threshold until device is non-functional	60	150	300	mV
			50		350	
I_{SC}	Output short-circuit current	$V_{IN} = V_{OUT(NOM)} + 1$ V, V_{BIAS} = 3 V V_{OUT} = 0 V		6.2		A
ENABLE PIN						
I_{EN}	ENABLE pin current	$V_{EN} = V_{BIAS}$		0.01		µA
		V_{EN} = 0 V, V_{BIAS} = 5.5 V	–19	–30	–40	
		V_{EN} = 0 V, V_{BIAS} = 5.5 V T_J = –40°C to 125°C	–13		–51	
$V_{EN(ON)}$	Enable voltage threshold	V_{EN} rising until Output = ON	1	1.25	1.50	V
		V_{EN} rising until Output = ON T_J = –40°C to 125°C	0.9		1.55	
$V_{EN(HYS)}$	Enable voltage hysteresis	V_{EN} falling from $V_{EN(ON)}$ until Output = OFF	50	100	150	mV
		V_{EN} falling from $V_{EN(ON)}$ until Output = OFF T_J = –40°C to 125°C	30		200	
t_{OFF}	Turn-OFF delay time	$R_{LOAD} \times C_{OUT} << t_{OFF}$		20		µs
t_{ON}	Turn-ON delay time	$R_{LOAD} \times C_{OUT} << t_{ON}$		15		
AC PARAMETERS						
PSRR (V_{IN})	Ripple rejection for V_{IN} input voltage	$V_{IN} = V_{OUT}$ +1 V, f = 120 Hz		80		dB
		$V_{IN} = V_{OUT}$ + 1V, f = 1 kHz		65		
PSRR (V_{BIAS})	Ripple rejection for V_{BIAS} voltage	$V_{BIAS} = V_{OUT}$ + 3 V, f = 120 Hz		58		dB
		$V_{BIAS} = V_{OUT}$ + 3 V, f = 1 kHz		58		
e_n	Output noise density	f = 120 Hz		1		µV/√Hz
	Output noise voltage	BW = 10 Hz − 100 kHz		150		$µV_{(RMS)}$
		BW = 300 Hz − 300 kHz		90		
THERMAL PARAMETERS						
T_{SD}	Thermal shutdown junction temperature			160		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			10		

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6.6 Typical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF ceramic, V_{EN} = V_{BIAS}.

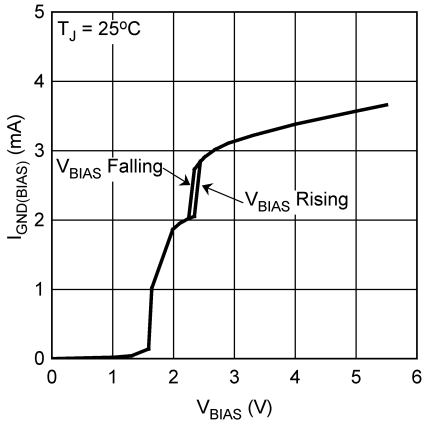

Figure 1. V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs V_{BIAS}

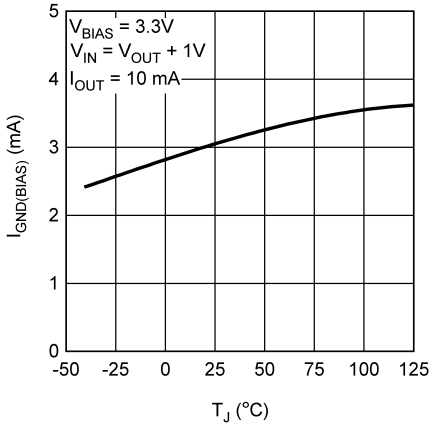

Figure 2. V_{BIAS} Ground Pin Current ($I_{GND(BIAS)}$) vs Temperature

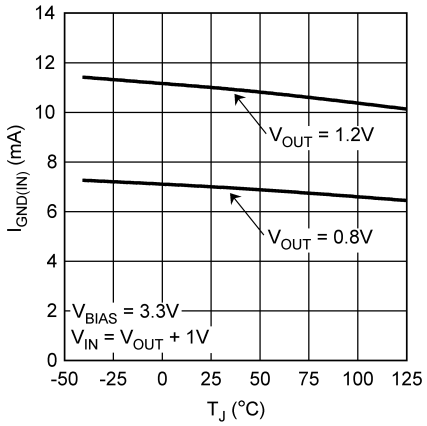

Figure 3. V_{IN} Ground Pin Current ($I_{GND(IN)}$) vs Temperature

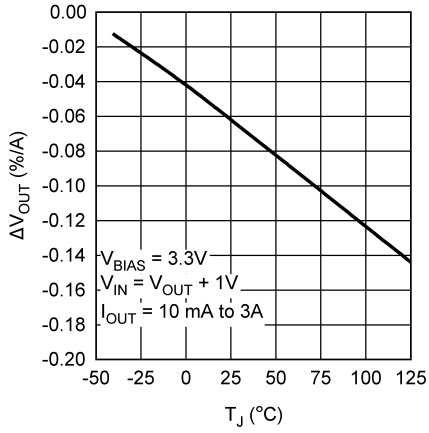

Figure 4. Load Regulation vs Temperature

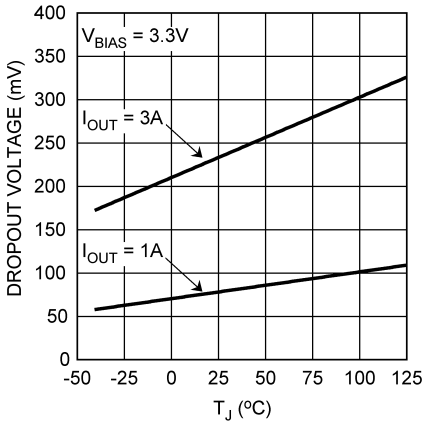

Figure 5. Dropout Voltage (V_{DO}) vs Temperature

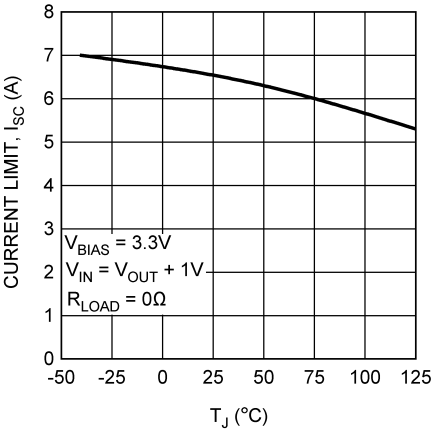

Figure 6. Output Current Limit (I_{SC}) vs Temperature

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Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF ceramic, V_{EN} = V_{BIAS}.

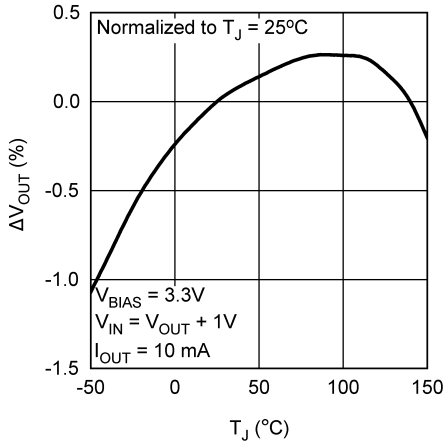


Figure 7. V_{OUT} vs Temperature

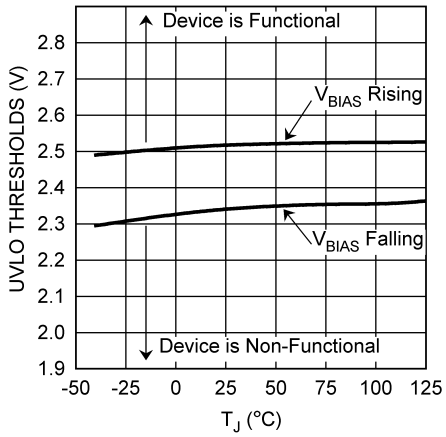


Figure 8. UVLO Thresholds vs Temperature

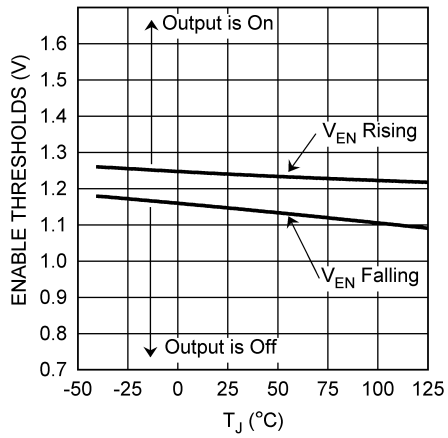


Figure 9. Enable Thresholds (V_{EN}) vs Temperature

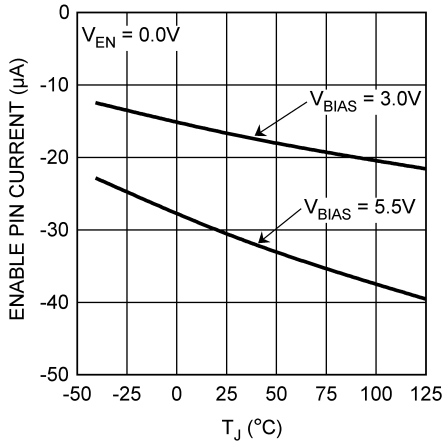


Figure 10. Enable Pull-Down Current (I_{EN}) vs Temperature

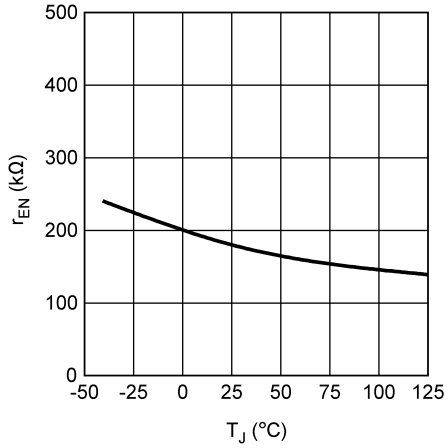


Figure 11. Enable Pull-Up Resistor (R_{EN}) vs Temperature

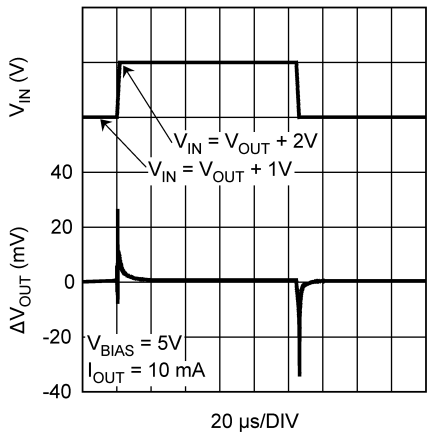


Figure 12. V_{IN} Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF ceramic, V_{EN} = V_{BIAS}.

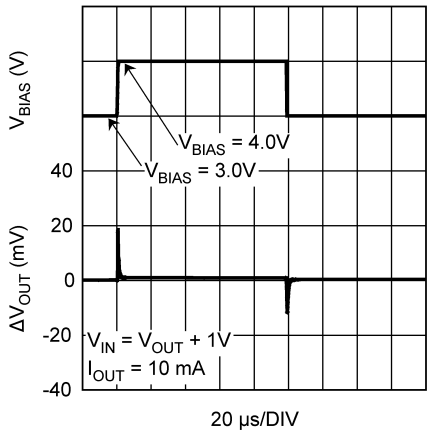


Figure 13. V_{BIAS} Line Transient Response

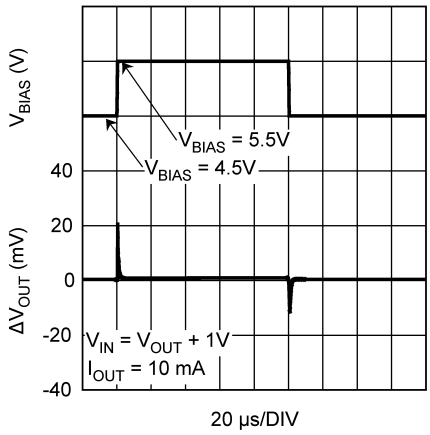


Figure 14. V_{BIAS} Line Transient Response

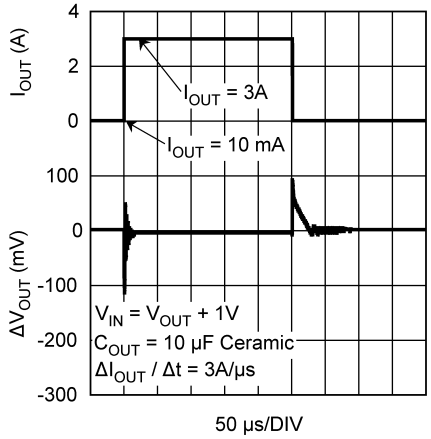
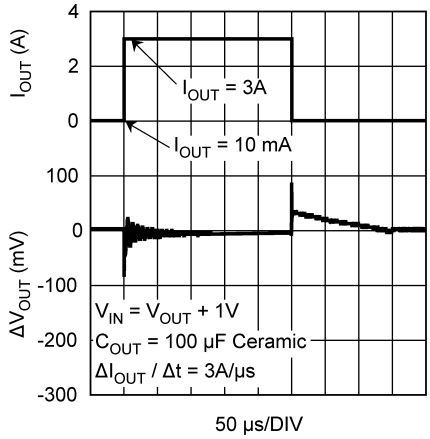
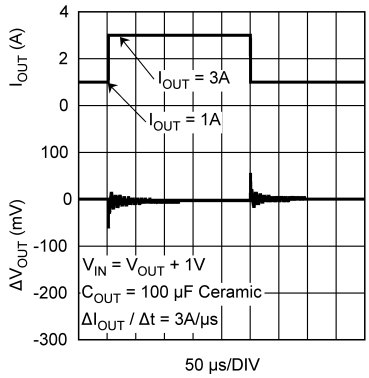


Figure 15. Load Transient Response, C_{OUT} = 10-µF Ceramic



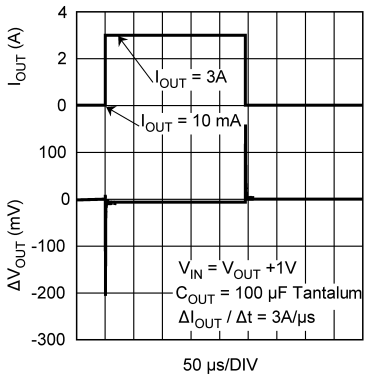
C_{OUT} = 100-µF Ceramic

Figure 16. Load Transient Response



C_{OUT} = 100-µF Ceramic

Figure 17. Load Transient Response



C_{OUT} = 100-µF Tantalum

Figure 18. Load Transient Response

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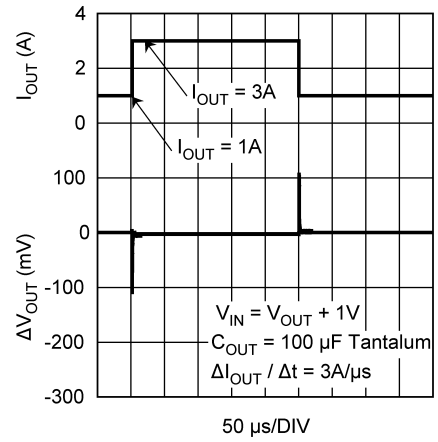
Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1 V, V_{BIAS} = 3 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 10-µF ceramic, C_{BIAS} = 1-µF ceramic, V_{EN} = V_{BIAS}.



C_{OUT} = 100-µF Tantalum

Figure 19. Load Transient Response

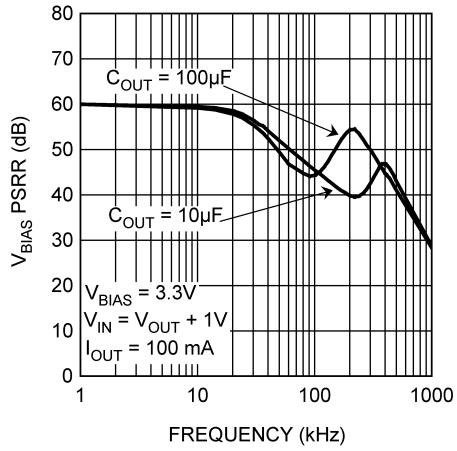


Figure 20. V_{BIAS} PSRR

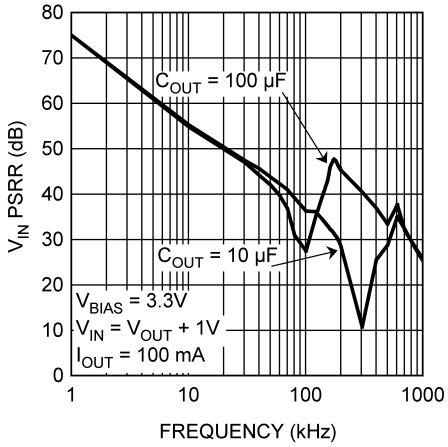


Figure 21. V_{IN} PSRR

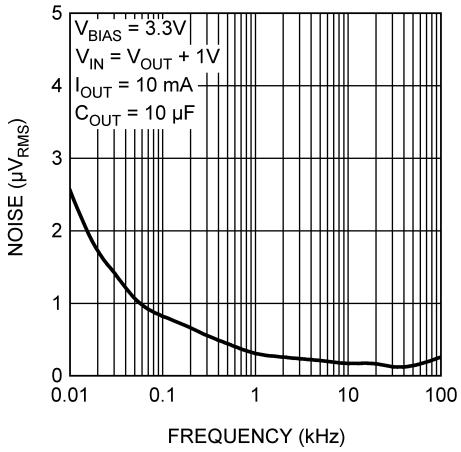


Figure 22. Output Noise

7 Detailed Description

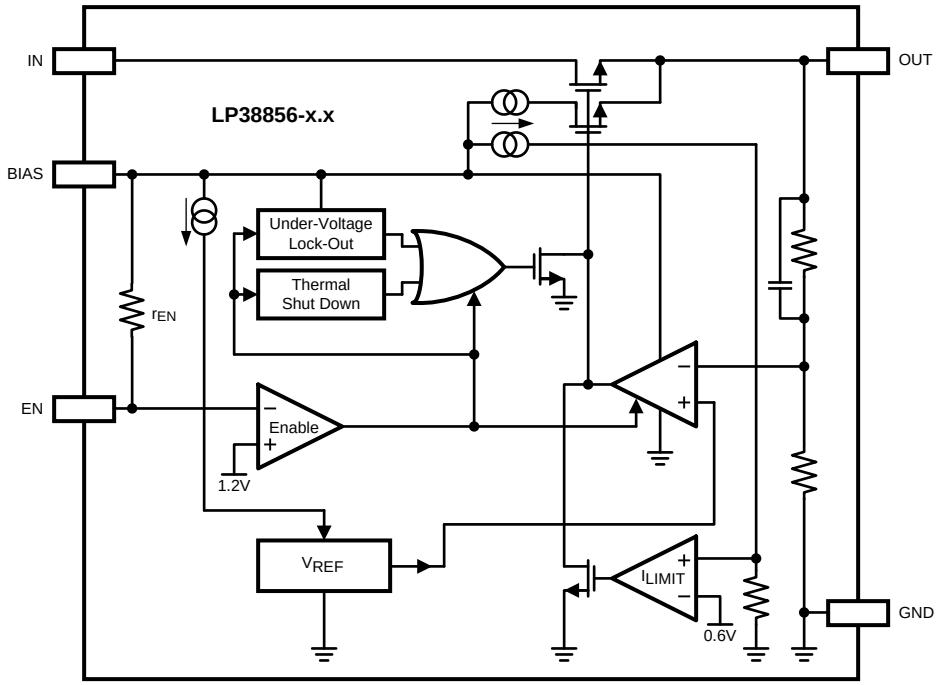
7.1 Overview

The LP38556 is a fast-response, high-current, low-dropout regulator, available in output voltages 0.8 V and 1.2 V. This device is capable of delivering 3-A continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are also included.

The LP38556 contains several features:

- Low dropout voltage, typical 240 mV at 3-A load.
- Low GND pin current, typical 10 mA at 3-A load.
- A shutdown feature is available, allowing the regulator to consume only 1 µA when EN pin is low.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable Operation

The enable pin (EN) provides a mechanism to enable, or disable, the regulator output stage. The EN pin has an internal pullup, through a typical 180-kΩ resistor, to V_{BIAS}.

If the EN pin is actively driven, pulling the EN pin above the V_{EN} threshold of 1.25 V (typical) will turn the regulator output on, while pulling the EN pin below the V_{EN} threshold will turn the regulator output off. There is approximately 100 mV of hysteresis built into the enable threshold provide noise immunity.

If the enable function is not needed, the EN pin must be left open, or connected directly to V_{BIAS}. If the EN pin is left open, stray capacitance on this pin must be minimized, otherwise the output turnon will be delayed while the stray capacitance is charged through the internal resistance (r_{EN}).

7.3.2 Input Voltage

The input voltage (V_{IN}) is the high current external voltage rail that will be regulated down to a lower voltage, which is applied to the load. The input voltage must be at least V_{OUT} + V_{DO}, and no higher than whatever value is used for V_{BIAS}.

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Feature Description (continued)

7.3.3 Bias Voltage

The bias voltage (V_{BIAS}) is a low current external voltage rail required to bias the control circuitry and provide gate drive for the N-FET pass transistor. The bias voltage must be in the range of 3 V to 5.5 V to ensure proper operation of the device.

7.3.4 Undervoltage Lockout

The bias voltage is monitored by a circuit which prevents the device from functioning when the bias voltage is below the undervoltage lock-out (UVLO) threshold of approximately 2.45 V.

As the bias voltage rises above the UVLO threshold the device control circuitry become active. There is approximately 150 mV of hysteresis built into the UVLO threshold to provide noise immunity.

When the bias voltage is between the UVLO threshold and the minimum operating rating value of 3 V the device will be functional, but the operating parameters will not be within the specified limits.

7.3.5 Supply Sequencing

There is no requirement for the order that V_{IN} or V_{BIAS} are applied or removed. However, the output voltage cannot be specified until both V_{IN} and V_{BIAS} are within the range of specified operating values.

If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommend for this diode clamp.

7.3.6 Reverse Voltage

A reverse voltage condition will exist when the voltage at the OUT pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed.

The NMOS pass element, by design, contains no body diode. This means that, as long as the gate of the pass element is not driven, there will not be any reverse current flow through the pass element during a reverse voltage event. The gate of the pass element is not driven when V_{BIAS} is below the UVLO threshold.

When V_{BIAS} is above the UVLO threshold the control circuitry is active and will attempt to regulate the output voltage. Because the input voltage is less than the output voltage, the control circuit will drive the gate of the pass element to the full V_{BIAS} potential when the output voltage begins to fall. In this condition, reverse current will flow from the OUT pin to the IN pin, limited only by the $R_{DS(ON)}$ of the pass element and the output-to-input voltage differential. This condition is outside the specified operating range and must be avoided.

7.4 Device Functional Modes

7.4.1 Operation with 3 V ≤ V_{BIAS} ≤ 5.5 V , $V_{OUT(TARGET)}$ + 0.3 V ≤ V_{IN} ≤ V_{BIAS}

The device operates if the bias voltage is equal to, or exceeds, 3 V; input voltage is equal to, or exceeds, $V_{OUT(TARGET)}$ + 0.3 V. At bias voltages below the minimum V_{BIAS} requirement, the device does not operate correctly, and output voltage may not reach target value.

7.4.2 Operation with V_{EN} Control

If the voltage on the EN pin is less than 1 V, the device is disabled. Raising V_{EN} above 1.5 V initiates the start-up sequence of the device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP38856 can provide 3-A output current with 240-mV dropout voltage (typical). The bias voltage must be in the range of 3 V to 5.5 V to ensure proper operation of the device. The input voltage must be at least V_{OUT} + V_{DO}, and no higher than whatever value is used for V_{BIAS}. Minimal input and output capacitor are 10 µF. The capacitor on the bias pin must be at least 1 µF.

8.2 Typical Application

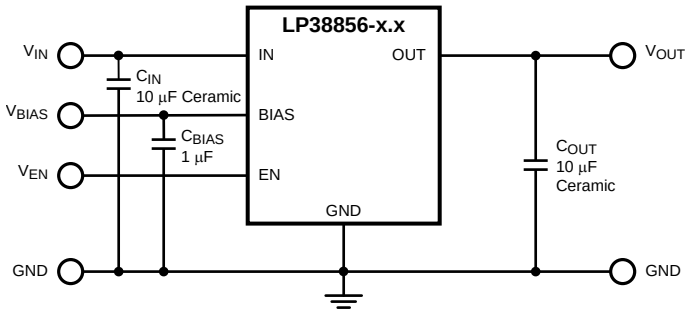

Figure 23. LP38856 Typical Application

8.2.1 Design Requirements

For LP38856 typical applications, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETERS	VALUE
Bias voltage	3 V to 5.5 V
Input voltage	V_{OUT}+0.3 V to V_{BIAS}
Output voltage	0.8 V or 1.2 V
Output current	3 A (maximum)
Bias capacitor	1 µF (minimum)
Input capacitor	10 µF (minimum)
Output capacitor	10 uF (minimum)

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

To assure regulator stability, capacitors are required on the IN, OUT, and BIAS pins as shown in Figure 23.

8.2.2.1.1 Output Capacitor

A minimum output capacitance of 10 µF, ceramic, is required for stability. The amount of output capacitance can be increased without limit. The output capacitor must be located less than 1 cm from the output pin of the device and returned to the device ground pin with a clean analog ground.

Only high quality ceramic types such as X5R or X7R should be used, as the Z5U and Y5F types do not provide sufficient capacitance over temperature.

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Tantalum capacitors will also provide stable operation across the entire operating temperature range. However, the effects of ESR may provide variations in the output voltage during fast load transients. Using the minimum recommended 10 µF ceramic capacitor at the output will allow unlimited capacitance, tantalum and/or aluminum, to be added in parallel.

8.2.2.1.2 Input Capacitor

The input capacitor must be at least 10 µF, but can be increased without limit. Its purpose is to provide a low source impedance for the regulator input. A ceramic capacitor, X5R or X7R, is recommended.

Tantalum capacitors may also be used at the input pin. There is no specific ESR limitation on the input capacitor (the lower, the better).

Aluminum electrolytic capacitors can be used, but are not recommended as their ESR increases very quickly at cold temperatures. They are not recommended for any application where the ambient temperature falls below 0°C.

8.2.2.1.3 Bias Capacitor

The capacitor on the bias pin must be at least 1 µF. It can be any good quality capacitor (ceramic is recommended).

8.2.2.2 Power Dissipation and Heatsinking

A heat-sink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

The total power dissipation of the device is the sum of three different points of dissipation in the device.

The first part is the power that is dissipated in the NMOS pass element, and can be determined with the formula:

$$P_{D(PASS)} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

The second part is the power that is dissipated in the bias and control circuitry, and can be determined with the formula:

$$P_{D(BIAS)} = V_{BIAS} \times I_{GND(BIAS)}$$

where

- $I_{GND(BIAS)}$ is the portion of the operating ground current of the device that is related to V_{BIAS}. (2)

The third part is the power that is dissipated in portions of the output stage circuitry, and can be determined with the formula:

$$P_{D(IN)} = V_{IN} \times I_{GND(IN)}$$

where

- $I_{GND(IN)}$ is the portion of the operating ground current of the device that is related to V_{IN}. (3)

The total power dissipation is then:

$$P_D = P_{D(PASS)} + P_{D(BIAS)} + P_{D(IN)} \quad (4)$$

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum anticipated ambient temperature ($T_{A(MAX)}$) for the application, and the maximum allowable operating junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (5)$$

The maximum allowable value for junction to ambient thermal resistance, $R_{\theta JA}$, can be calculated using the formula:

$$R_{\theta JA} \leq \Delta T_J / P_D \quad (6)$$

The LP38856 is available in TO-220 and DDPAK/TO-263 packages. The thermal resistance in the application depends on amount of copper area or heat-sink, and on air flow. If the maximum allowable value of $R_{\theta JA}$ calculated above is ≥ 32°C/W for TO-220 package and ≥ 41°C/W for DDPAK/TO-263 package no heat-sink is needed because the package alone can dissipate enough heat to satisfy these requirements. If the value needed for allowable $R_{\theta JA}$ falls below these limits, a heat-sink is required.

8.2.3 Application Curves

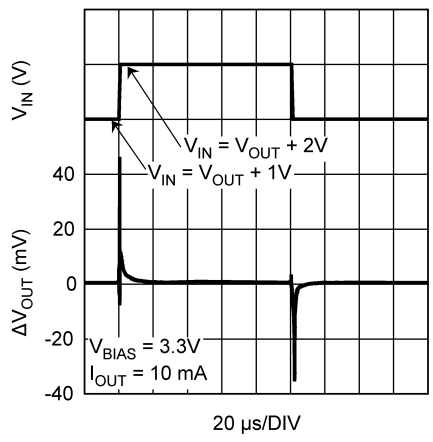

Figure 24. V_{IN} Line Transient Response

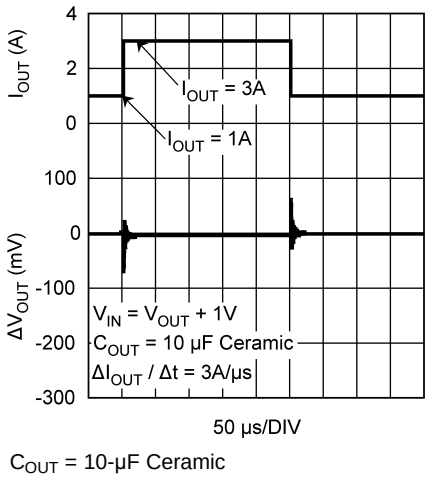

Figure 25. Load Transient Response

9 Power Supply Recommendations

The LP38856 device is designed to operate from an bias voltage supply range between 3 V and 5.5 V, and the input voltage in the range between V_{OUT} + 0.3 V and V_{BIAS}. Input supply must be well regulated. An input capacitor of at least 10 µF is required.

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10 Layout

10.1 Layout Guidelines

Good layout practices will minimize voltage error and prevent instability which can result from ground loops. The input and output capacitors must be directly connected to the device pins with short traces that have no other current flowing in them (Kelvin connect).

The best way to do this is to place the capacitors very near the device and make connections directly to the device pins via short traces on the top layer of the PCB. The regulator's ground pin must be connected through vias to the internal or backside ground plane so that the regulator has a single point ground.

The external resistors which set the output voltage must also be located very near the device with all connections directly tied via short traces to the pins of the device (Kelvin connect). Do not connect the resistive divider to the load point or DC error will be induced.

10.2 Layout Example

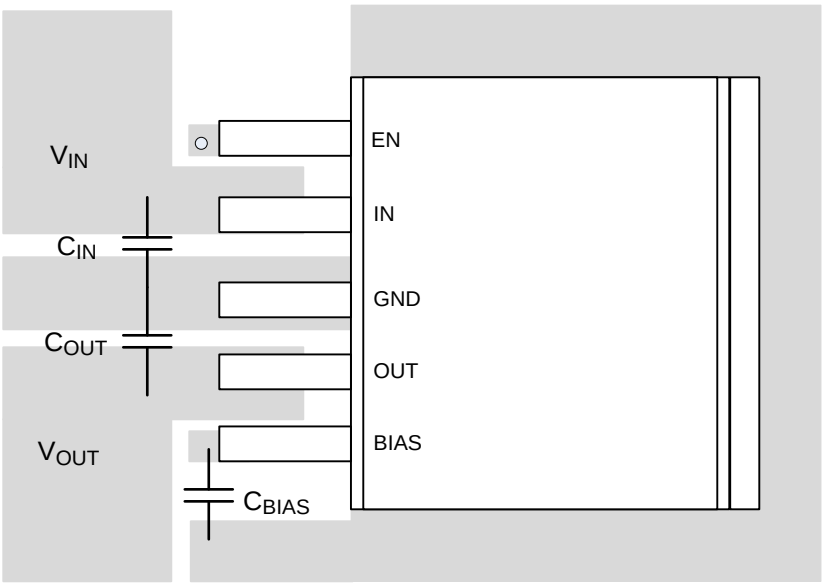

Figure 26. LP38856 Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP38856S-1.2/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38856S 1.2
LP38856S-1.2/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	45 | TUBE	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38856S 1.2
LP38856SX-1.2/NOPB	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38856S 1.2
LP38856SX-1.2/NOPB.A	Active	Production	DDPAK/ TO-263 (KTT) | 5	500 | LARGE T&R	ROHS Exempt	SN	Level-3-245C-168 HR	-40 to 125	LP38856S 1.2
LP38856T-1.2/NOPB	Active	Production	TO-220 (NDH) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38856T 1.2
LP38856T-1.2/NOPB.A	Active	Production	TO-220 (NDH) | 5	45 | TUBE	Yes	SN	Level-1-NA-UNLIM	-40 to 125	LP38856T 1.2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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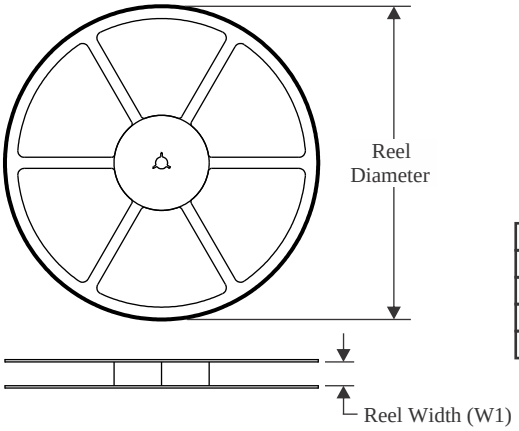
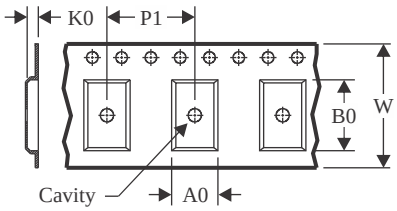
TAPE AND REEL INFORMATION

REEL DIMENSIONS

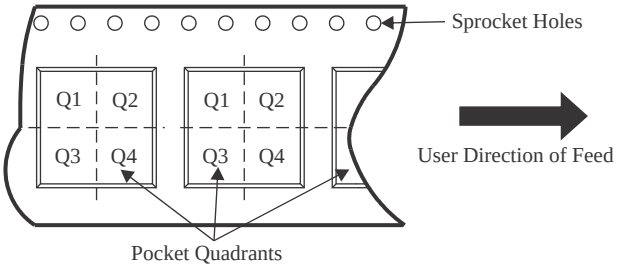


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

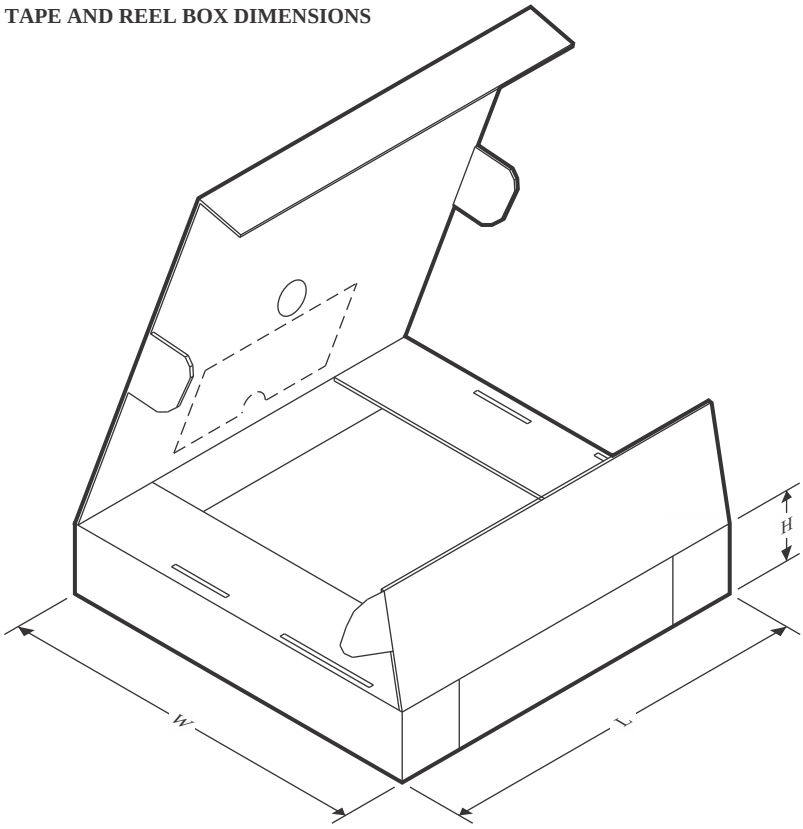
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38856SX-1.2/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

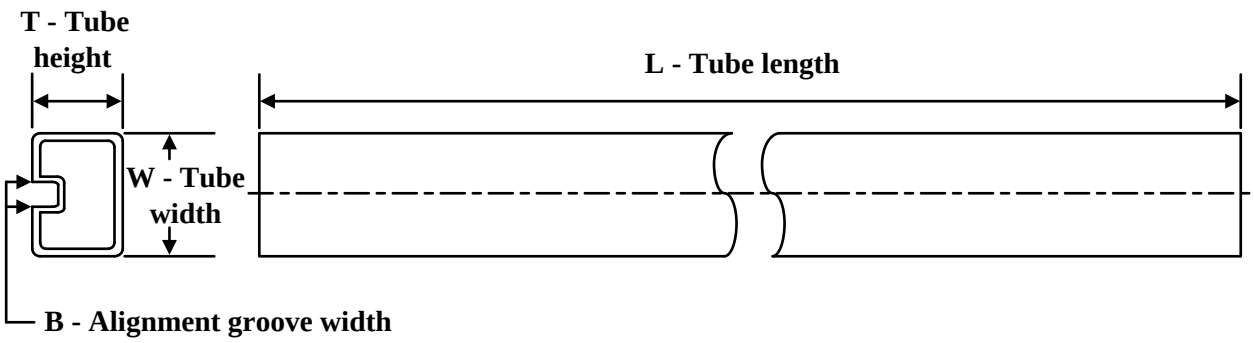
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38856SX-1.2/NOPB	DDPAK/TO-263	KTT	5	500	356.0	356.0	45.0

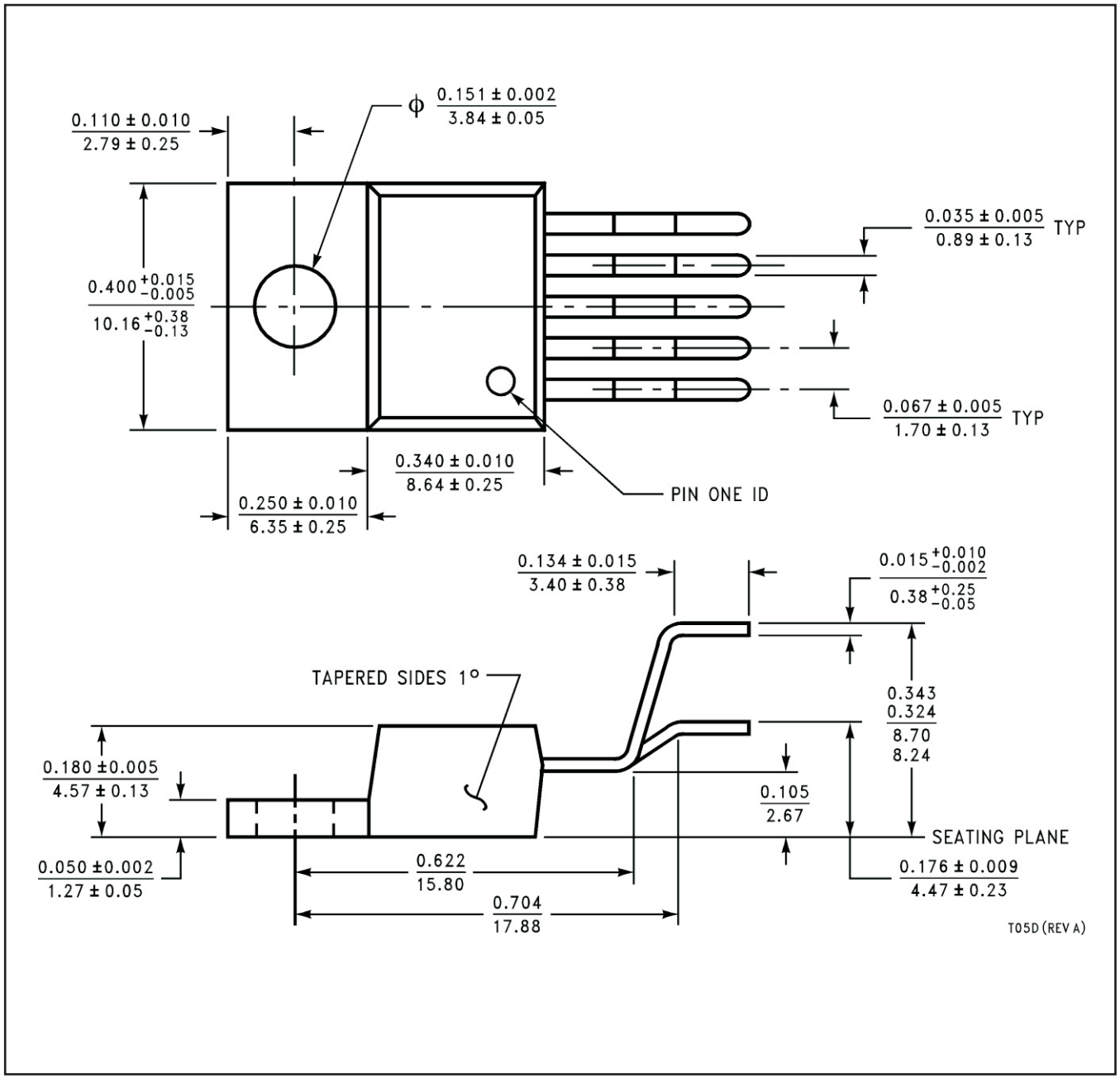
TUBE



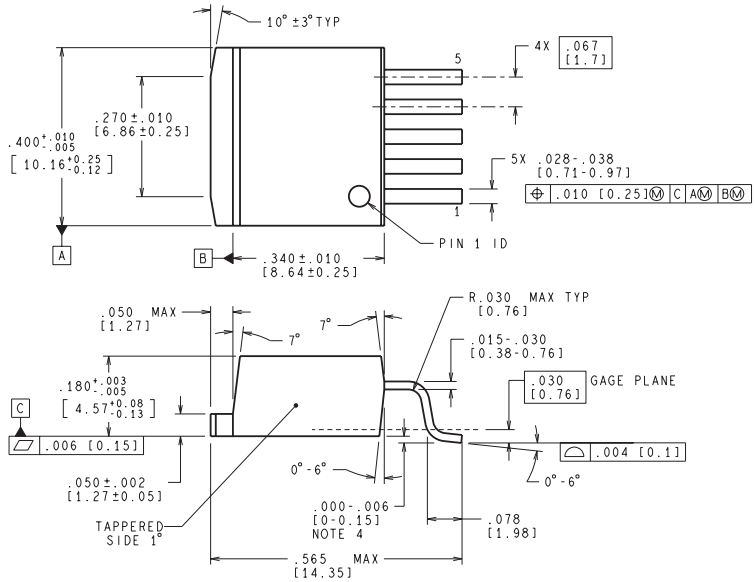
*All dimensions are nominal

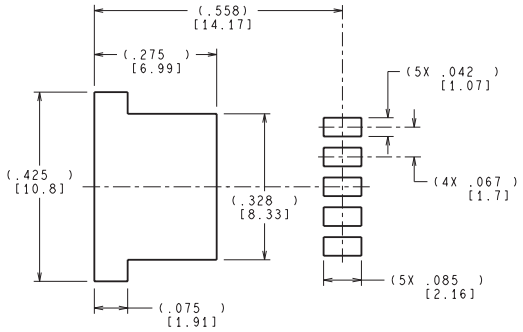
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38856S-1.2/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38856S-1.2/NOPB.A	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38856T-1.2/NOPB	NDH	TO-220	5	45	502	30	30048.2	10.74
LP38856T-1.2/NOPB.A	NDH	TO-220	5	45	502	30	30048.2	10.74

NDH0005D

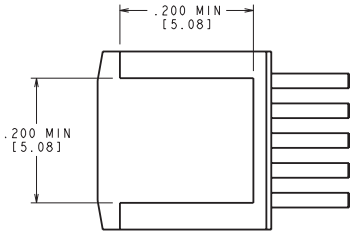

0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13
TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
0.622
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

KTT0005B





LAND PATTERN RECOMMENDATION



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