INA333 Micro-Power (50µA), Zerø-Drift, Rail-to-Rail Out Instrumentation Amplifier

1 Features

- Low Offset Voltage: 25 µV (Maximum), G ≥ 100
- Low Drift: 0.1 µV/°C, G ≥ 100
- Low Noise: 50 nV/√Hz, G ≥ 100
- High CMRR: 100 dB (Minimum), G ≥ 10
- Low Input Bias Current: 200 pA (Maximum)
- Supply Range: 1.8 V to 5.5 V
- Input Voltage: (V–) +0.1 V to (V+) –0.1 V
- Output Range: (V–) +0.05 V to (V+) –0.05 V
- Low Quiescent Current: 50 µA
- Operating Temperature: –40°C to +125°C
- RFI Filtered Inputs
- 8-Pin VSSOP and 8-Pin WSON Packages

2 Applications

- Bridge Amplifiers
- ECG Amplifiers
- Pressure Sensors
- Medical Instrumentation
- Portable Instrumentation
- Weigh Scales
- Thermocouple Amplifiers
- RTD Sensor Amplifiers
- Data Acquisition

3 Description

The INA333 device is a low-power, precision instrumentation amplifier offering excellent accuracy. The versatile 3-operational amplifier design, small size, and low power make it ideal for a wide range of portable applications.

A single external resistor sets any gain from 1 to 1000. The INA333 is designed to use an industry-standard gain equation: $G = 1 + (100\ k\Omega / R_G)$.

The INA333 device provides very low offset voltage (25 µV, G ≥ 100), excellent offset voltage drift (0.1 µV/°C, G ≥ 100), and high common-mode rejection (100 dB at G ≥ 10). It operates with power supplies as low as 1.8 V (±0.9 V) and quiescent current is only 50 µA, making it ideal for battery-operated systems. Using autocalibration techniques to ensure excellent precision over the extended industrial temperature range, the INA333 device also offers exceptionally low noise density (50 nV/√Hz) that extends down to DC.

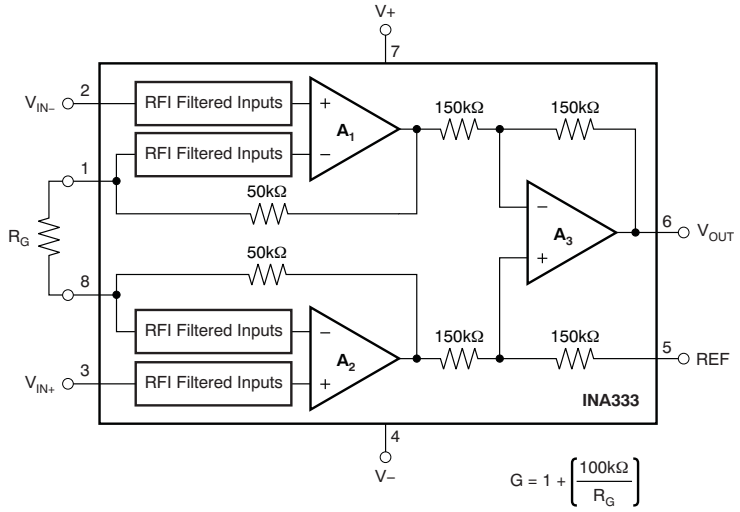
The INA333 device is available in both 8-pin VSSOP and WSON surface-mount packages and is specified over the T_A = –40°C to +125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA333	VSSOP (8)	3.00 mm × 3.00 mm
	WSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 7
7 Detailed Description ... 13
7.1 Overview ... 13
7.2 Functional Block Diagram ... 13
7.3 Feature Description ... 13
7.4 Device Functional Modes ... 13
8 Application and Implementation ... 14
8.1 Application Information ... 14
8.2 Typical Application ... 14
9 Power Supply Recommendations ... 19
10 Layout ... 20
10.1 Layout Guidelines ... 20
10.2 Layout Example ... 20
11 Device and Documentation Support ... 21
11.1 Device Support ... 21
11.2 Documentation Support ... 22
11.3 Trademarks ... 22
11.4 Electrostatic Discharge Caution ... 22
11.5 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

4 Revision History

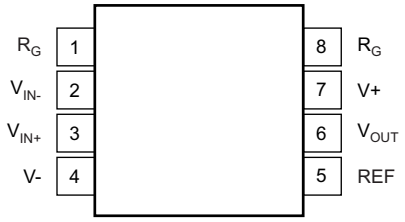
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2008) to Revision C	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

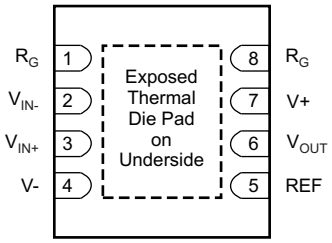
Copyright © 2008–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



DRG Package
8-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
RG	1, 8	—	Gain setting pins. For gains greater than 1, place a gain resistor between pins 1 and 8.
V^+	7	—	Positive supply
$V^–$	4	—	Negative supply
VIN+	3	I	Positive input
VIN–	2	I	Negative input
VOUT	6	O	Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage	7		V
Analog input voltage (2)	(V–) – 0.3	(V+) + 0.3	V
Output short-circuit (3)	Continuous		
Operating temperature, T_A	–40	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
	Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VS	Supply voltage	1.8	5.5	V
	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		INA333		UNIT
		DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.5	60	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	60	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.3	50	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.7	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2008–2015, Texas Instruments Incorporated

6.5 Electrical Characteristics

for V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT(1)						
V_{OSI}	Offset voltage, RTI(2)			±10 ±25/G	±25 ±75/G	µV
PSR	vs temperature	T_A = –40°C to +125°C			±0.1 ±0.5 / G	µV/°C
	vs power supply	1.8 V ≤ V_S ≤ 5.5 V		±1 ±5/G	±5 ±15/G	µV/V
	Long-term stability			See (3)		
	Turnon time to specified V_{OSI}	T_A = –40°C to +125°C		See *Typical Characteristics*		
	Impedance					
Z_{IN}	Differential			100 || 3		GΩ || pF
Z_{IN}	Common-mode			100 || 3		GΩ || pF
V_{CM}	Common-mode voltage range	V_O = 0 V	(V–) + 0.1		(V+) – 0.1	V
CMR	Common-mode rejection	DC to 60 Hz				
	G = 1	V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	80	90		dB
	G = 10	V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	100	110		dB
	G = 100	V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	100	115		dB
	G = 1000	V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	100	115		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±70	±200	pA
	vs temperature	T_A = –40°C to +125°C		See Figure 26		pA/°C
I_{OS}	Input offset current			±50	±200	pA
	vs temperature	T_A = –40°C to +125°C		See Figure 28		pA/°C
INPUT VOLTAGE NOISE						
e_{NI}	Input voltage noise	G = 100, R_S = 0 Ω, f = 10 Hz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 100 Hz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 1 kHz		50		nV/√Hz
		G = 100, R_S = 0 Ω, f = 0.1 Hz to 10 Hz		1		$µV_{PP}$
i_N	Input current noise	f = 10 Hz		100		fA/√Hz
		f = 0.1 Hz to 10 Hz		2		pA_{PP}
GAIN						
G	Gain equation			1 + (100 kΩ/R_G)		V/V
	Range of gain		1		1000	V/V
	Gain error	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV				
		G = 1		±0.01%	±0.1%	
		G = 10		±0.05%	±0.25%	
		G = 100		±0.07%	±0.25%	
		G = 1000		±0.25%	±0.5%	
	Gain vs temperature, G = 1	T_A = –40°C to +125°C		±1	±5	ppm/°C
	Gain vs temperature, G > 1(4)	T_A = –40°C to +125°C		±15	±50	ppm/°C
	Gain nonlinearity	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV				
	Gain nonlinearity, G = 1 to 1000	R_L = 10 kΩ		10		ppm
OUTPUT						
	Output voltage swing from rail	V_S = 5.5 V, R_L = 10 kΩ		See Figure 29	50	mV
	Capacitive load drive			500		pF
I_{SC}	Short-circuit current	Continuous to common		–40, +5		mA

(1) Total V_{OS}, referred-to-input = (V_{OSI}) + (V_{OSO} / G)
(2) RTI = Referred-to-input
(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV
(4) Does not include effects of external resistor R_G

Copyright © 2008–2015, Texas Instruments Incorporated

Electrical Characteristics (continued)

for V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
Bandwidth, –3dB		G = 1		150		kHz
		G = 10		35		kHz
		G = 100		3.5		kHz
		G = 1000		350		Hz
SR	Slew rate	V_S = 5 V, V_O = 4-V step, G = 1		0.16		V/µs
		V_S = 5 V, V_O = 4-V step, G = 100		0.05		V/µs
t_S	Settling time to 0.01%	V_{STEP} = 4 V, G = 1		50		µs
		V_{STEP} = 4 V, G = 100		400		µs
t_S	Settling time to 0.001%	V_{STEP} = 4 V, G = 1		60		µs
		V_{STEP} = 4 V, G = 100		500		µs
	Overload recovery	50% overdrive		75		µs
REFERENCE INPUT						
	R_{IN}			300		kΩ
	Voltage range		V–		V+	V
POWER SUPPLY						
Voltage range		Single voltage range	+1.8		+5.5	V
		Dual voltage range	±0.9		±2.75	V
I_Q	Quiescent current	V_{IN} = V_S / 2		50	75	µA
	vs temperature	T_A = –40°C to +125°C			80	µA
TEMPERATURE RANGE						
	Specified temperature range		–40		125	°C
	Operating temperature range		–40		150	°C

Copyright © 2008–2015, Texas Instruments Incorporated

6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

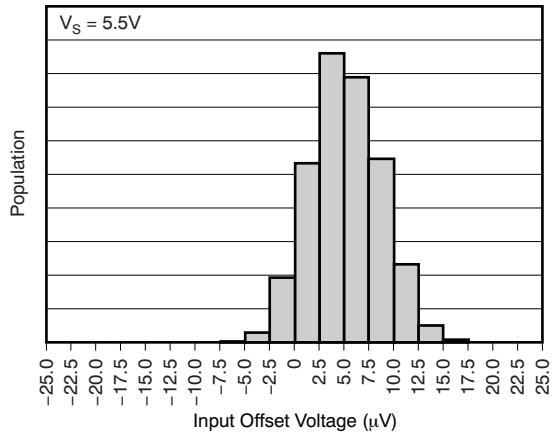


Figure 1. Input Offset Voltage

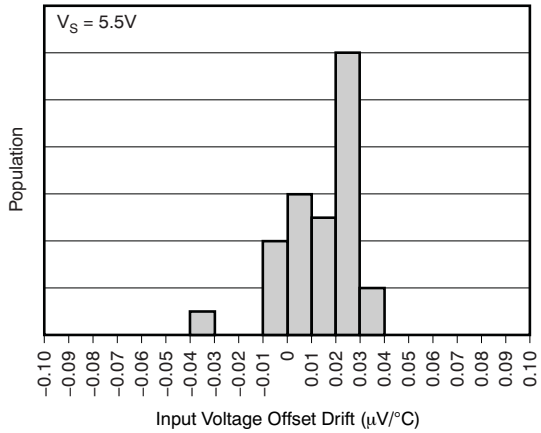


Figure 2. Input Voltage Offset Drift (–40°C to 125°C)

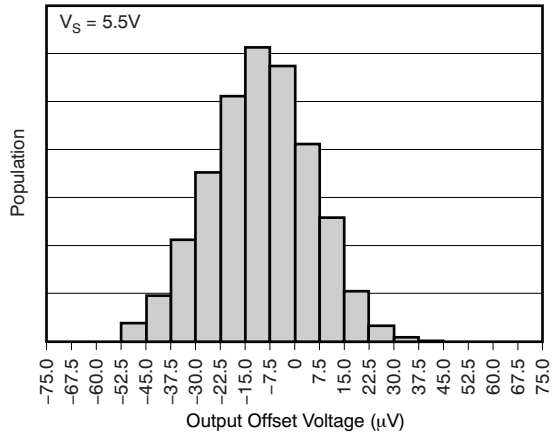


Figure 3. Output Offset Voltage

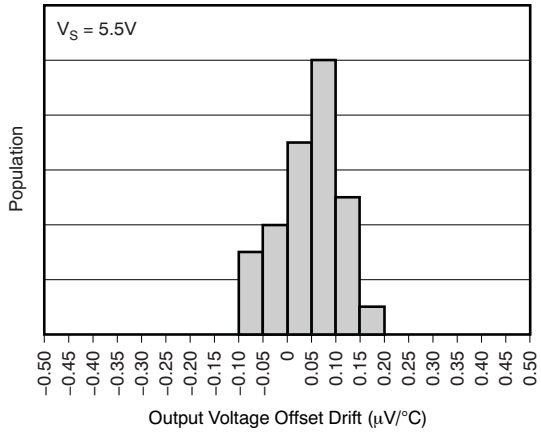


Figure 4. Output Voltage Offset Drift (–40°C to 125°C)

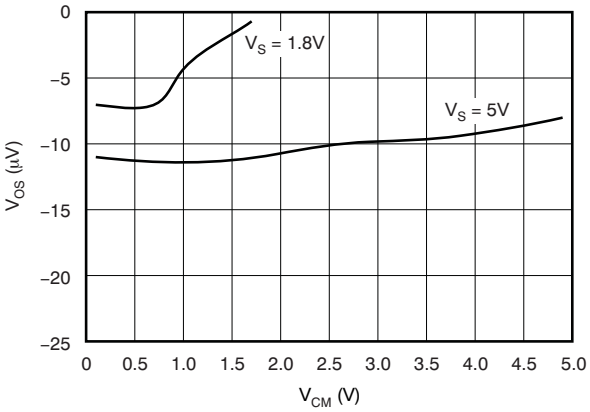


Figure 5. Offset Voltage vs Common-Mode Voltage

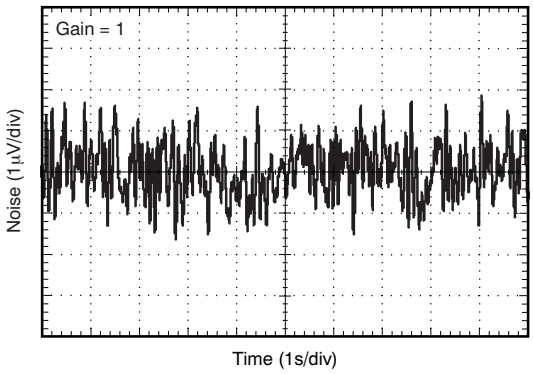


Figure 6. 0.1-Hz to 10-Hz Noise

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

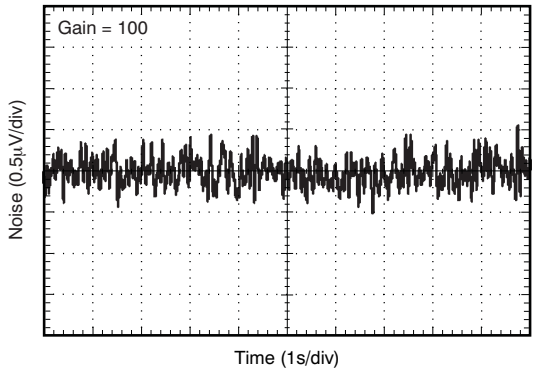


Figure 7. 0.1-Hz to 10-Hz Noise

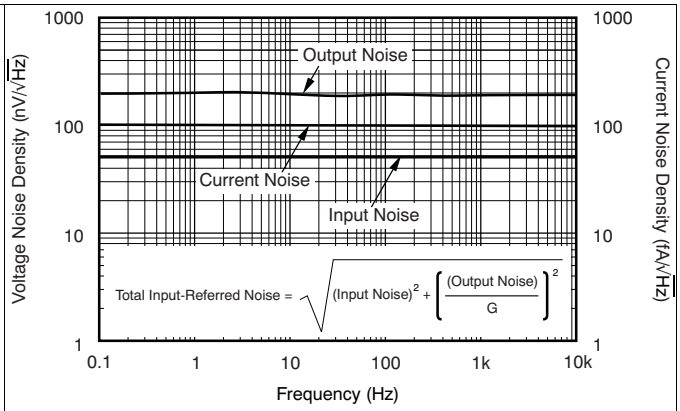


Figure 8. Spectral Noise Density

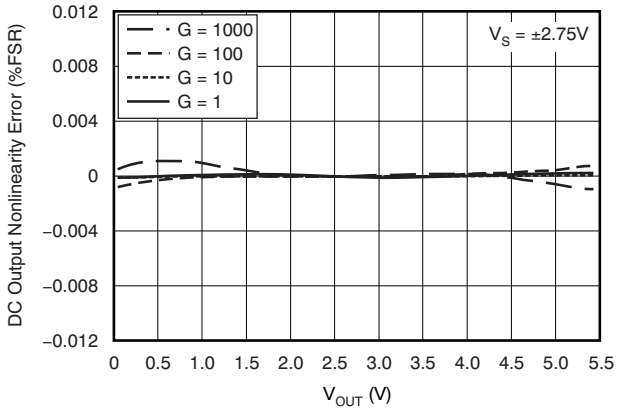


Figure 9. Nonlinearity Error

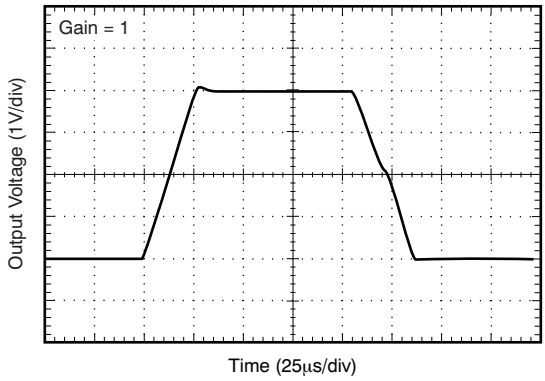


Figure 10. Large Signal Response

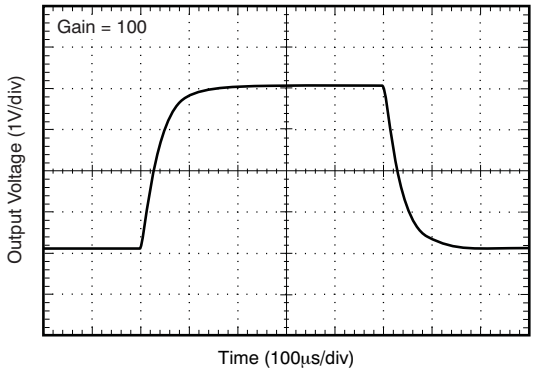


Figure 11. Large-Signal Step Response

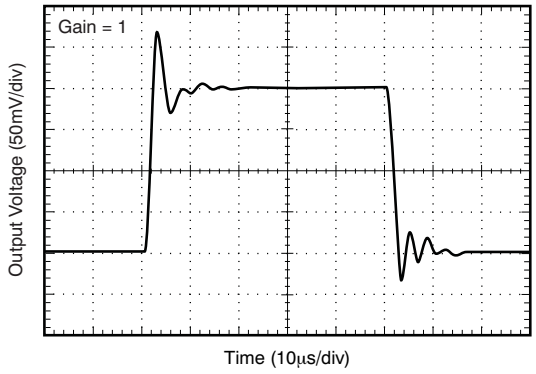


Figure 12. Small-Signal Step Response

Copyright © 2008–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

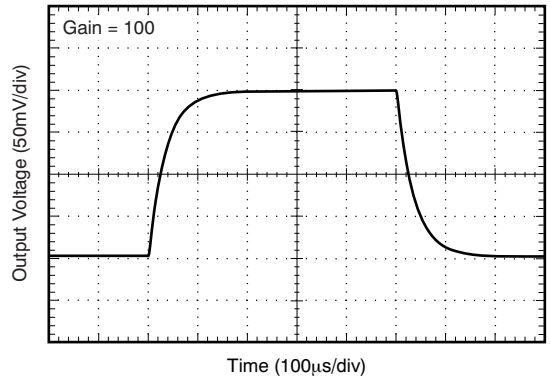


Figure 13. Small-Signal Step Response

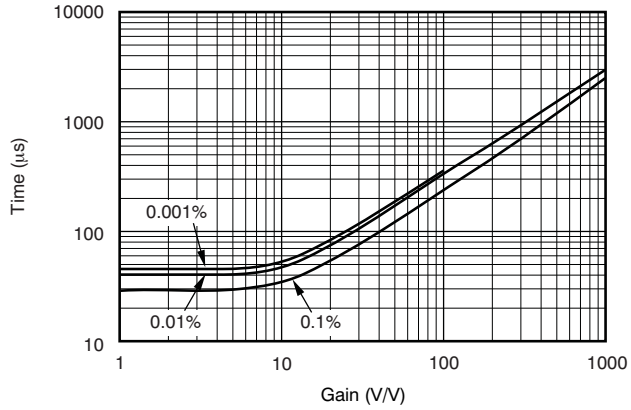


Figure 14. Settling Time vs Gain

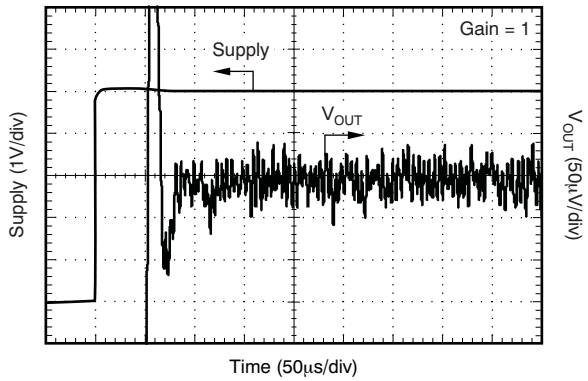


Figure 15. Start-Up Settling Time

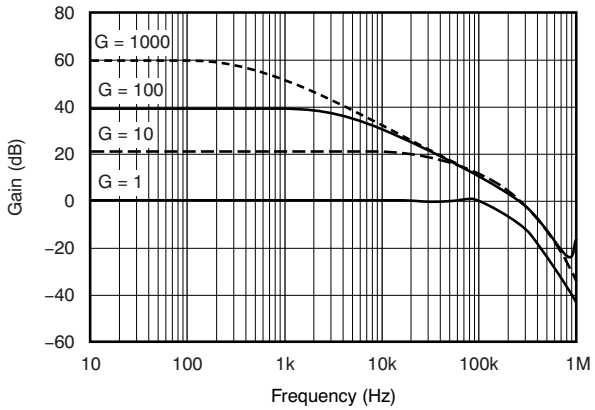


Figure 16. Gain vs Frequency

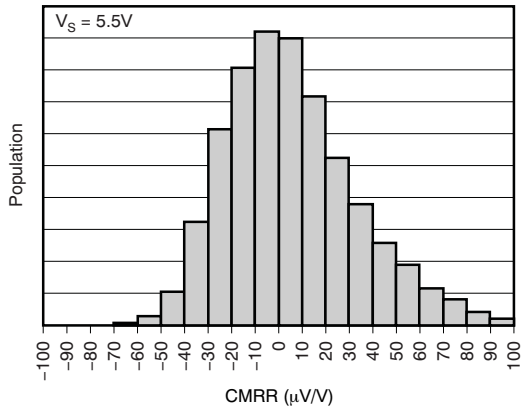


Figure 17. Common-Mode Rejection Ratio

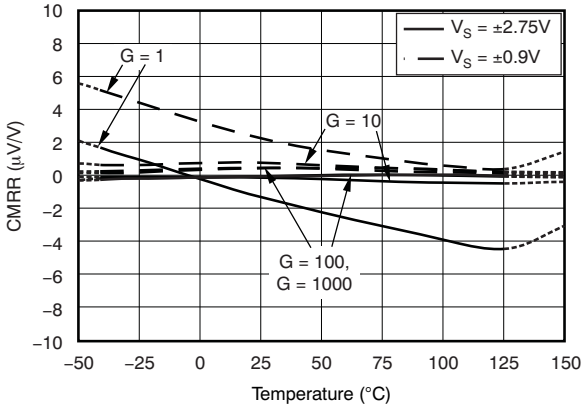


Figure 18. Common-Mode Rejection Ratio vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

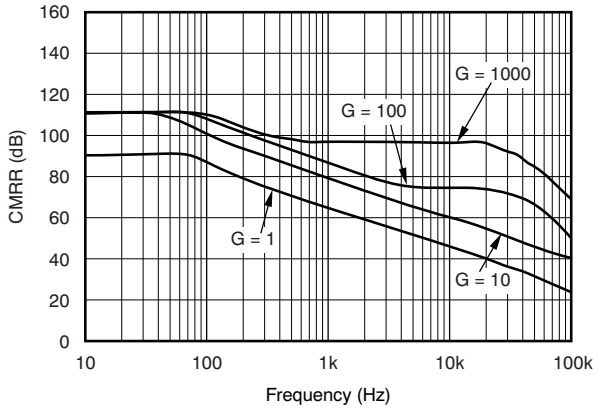


Figure 19. Common-Mode Rejection Ratio vs Frequency

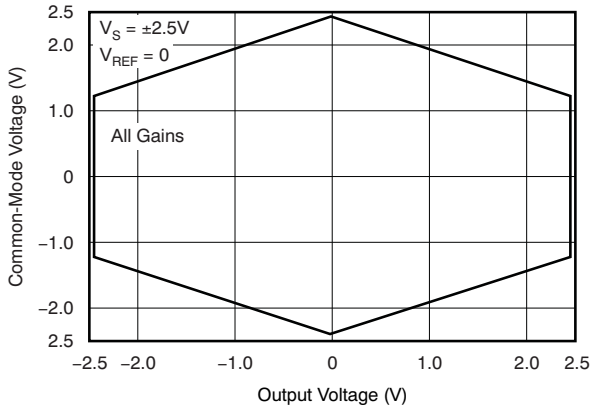


Figure 20. Typical Common-Mode Range vs Output Voltage

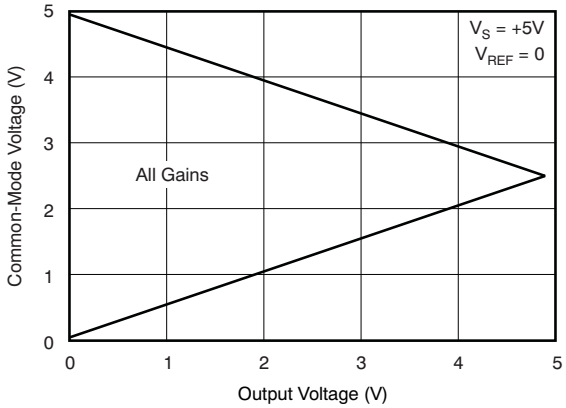


Figure 21. Typical Common-Mode Range vs Output Voltage

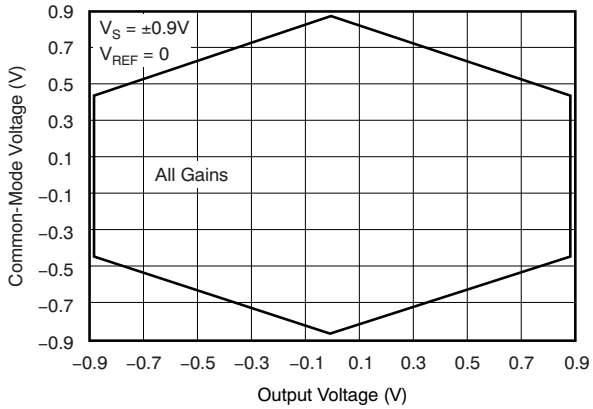


Figure 22. Typical Common-Mode Range vs Output Voltage

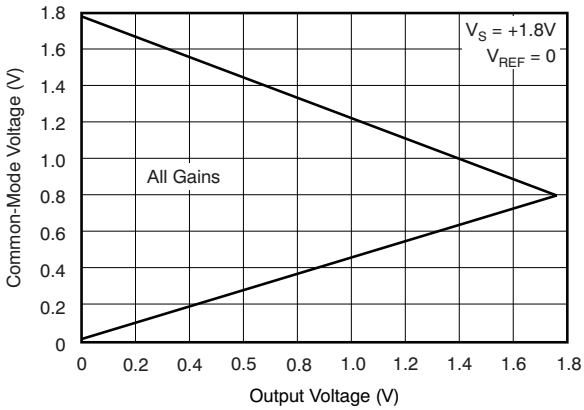


Figure 23. Typical Common-Mode Range vs Output Voltage

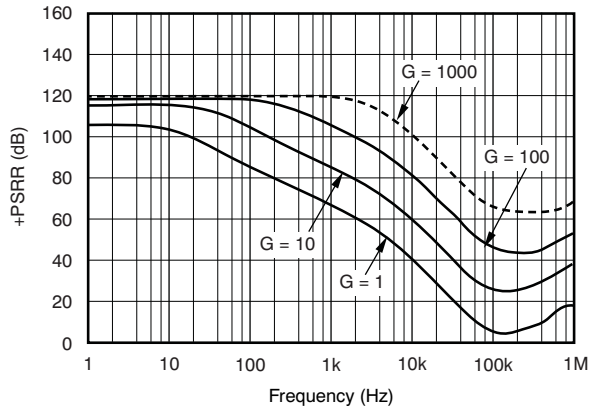


Figure 24. Positive Power-Supply Rejection Ratio

Copyright © 2008–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

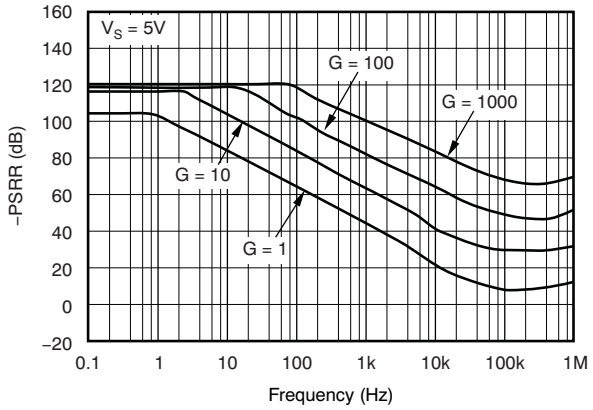


Figure 25. Negative Power-Supply Rejection Ratio

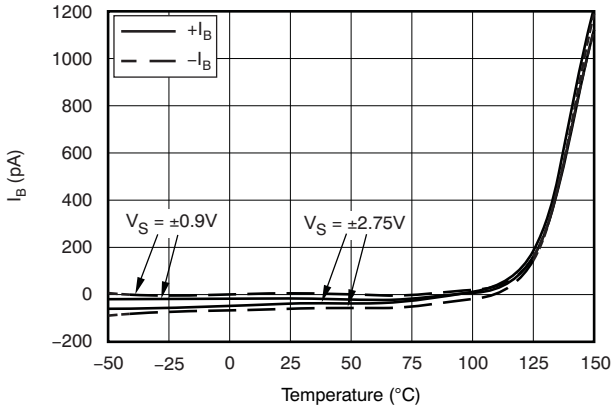


Figure 26. Input Bias Current vs Temperature

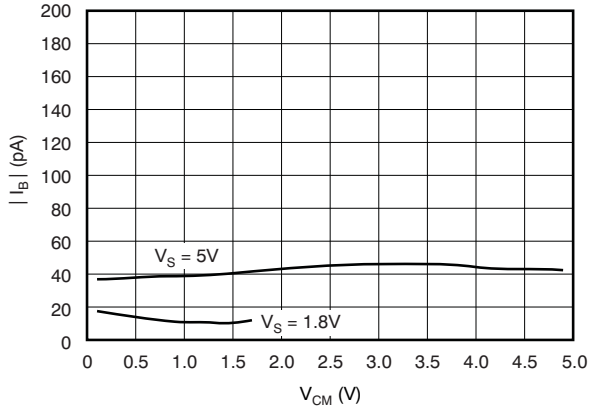


Figure 27. Input Bias Current vs Common-Mode Voltage

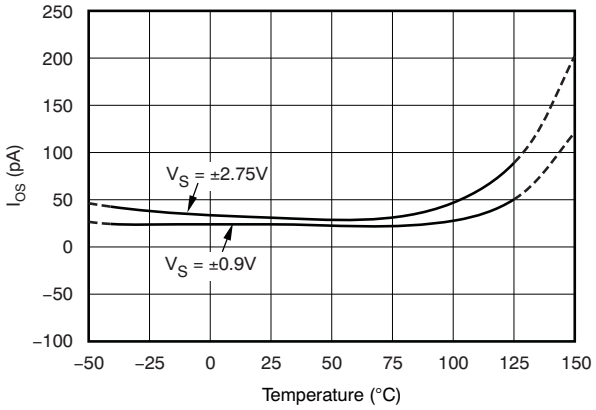


Figure 28. Input Offset Current vs Temperature

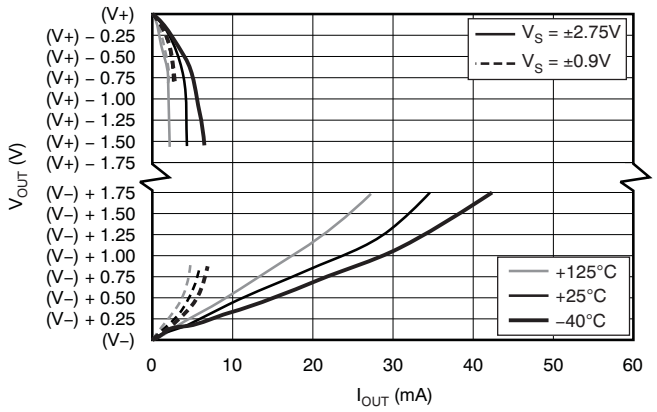


Figure 29. Output Voltage Swing vs Output Current

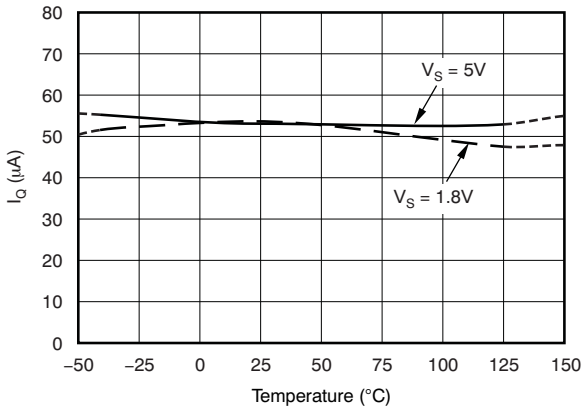


Figure 30. Quiescent Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

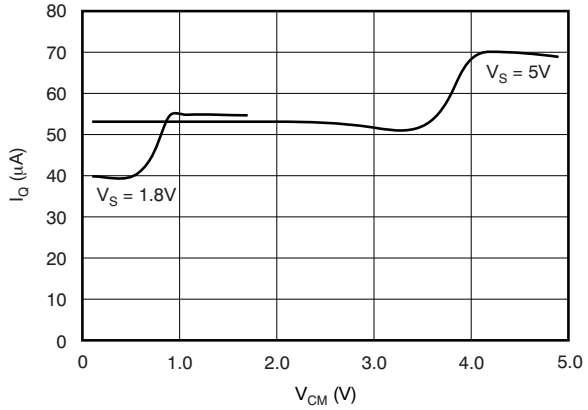


Figure 31. Quiescent Current vs Common-Mode Voltage

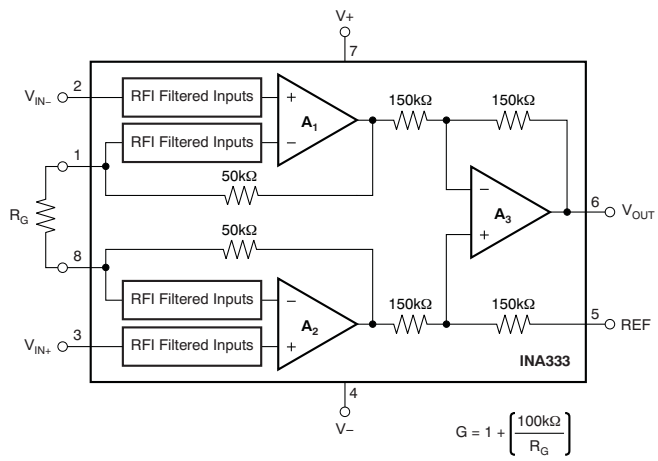
Copyright © 2008–2015, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The INA333 is a monolithic instrumentation amplifier (INA) based on the precision zero-drift OPA333 (operational amplifier) core. The INA333 also integrates laser-trimmed resistors to ensure excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding DC precision and makes the INA333 ideal for many 3.3-V and 5-V industrial applications.

7.2 Functional Block Diagram



7.3 Feature Description

The INA333 is a low-power, zero-drift instrumentation amplifier offering excellent accuracy. The versatile three-operational-amplifier design and small size make the amplifiers ideal for a wide range of applications. Zero-drift chopper circuitry provides excellent DC specifications. A single external resistor sets any gain from 1 to 10,000. The INA333 is laser trimmed for very high common-mode rejection (100 dB at G ≥ 100). This devices operate with power supplies as low as 1.8 V, and quiescent current of 50 µA, typically.

7.4 Device Functional Modes

7.4.1 Internal Offset Correction

INA333 internal operational amplifiers use an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power up, the amplifier requires approximately 100 µs to achieve specified VOS accuracy. This design has no aliasing or flicker noise.

7.4.2 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA333 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A1 and A2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see Figure 20.

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333 is near 0 V even though both inputs are overloaded.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA333 measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high input impedance makes the INA333 suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

8.2 Typical Application

Figure 32 shows the basic connections required for operation of the INA333 device. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333 device is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 15 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of Ωs in series with the REF pin can cause noticeable degradation in CMRR.

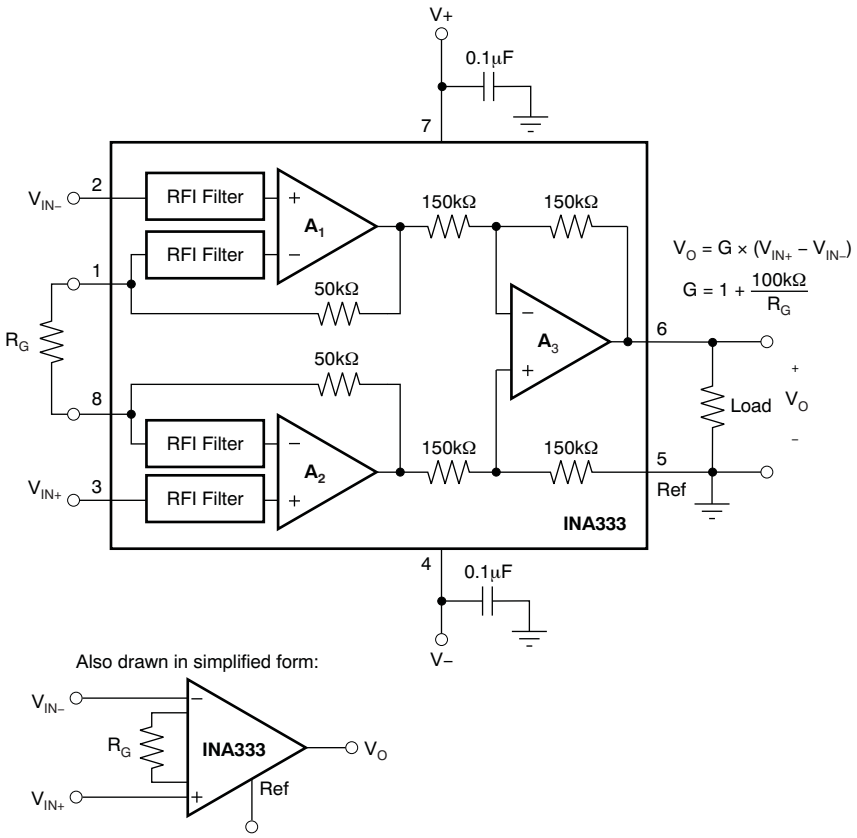


Figure 32. Basic Connections

Copyright © 2008–2015, Texas Instruments Incorporated

Typical Application (continued)

8.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor RG. The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground. When the input signal increases, the output voltage at the OUT pin increases, too.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

Gain of the INA333 device is set by a single external resistor, R_G, connected between pins 1 and 8. The value of R_G is selected according to Equation 1:

$$G = 1 + (100\ k\Omega / R_G) \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 100 kΩ in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333 device.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation will not converge unless a resistor is connected to the R_G pins; use a very large resistor value.

8.2.2.2 Internal Offset Correction

The INA333 device internal operational amplifiers use an auto-calibration technique with a time-continuous 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8.2.2.3 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF pin. Figure 33 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF pin is summed at the output. The operational amplifier buffer provides low impedance at the REF pin to preserve good common-mode rejection.

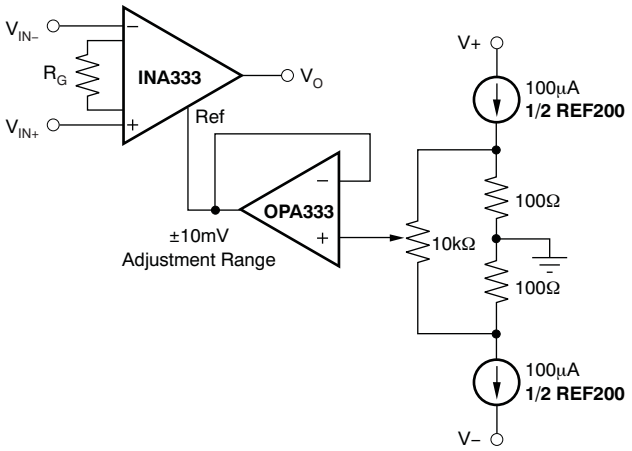


Figure 33. Optional Trimming of Output Offset Voltage

8.2.2.4 Noise Performance

The auto-calibration technique used by the INA333 device results in reduced low frequency noise, typically only 50 nV/$\sqrt{Hz}$, (G = 100). The spectral noise density can be seen in detail in Figure 8. Low frequency noise of the INA333 device is approximately 1 μV_{PP} measured from 0.1 Hz to 10 Hz, (G = 100).

8.2.2.5 Input Bias Current Return Path

The input impedance of the INA333 device is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically ±70 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 34 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA333 device, and the input amplifiers will saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 34). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

Copyright © 2008–2015, Texas Instruments Incorporated

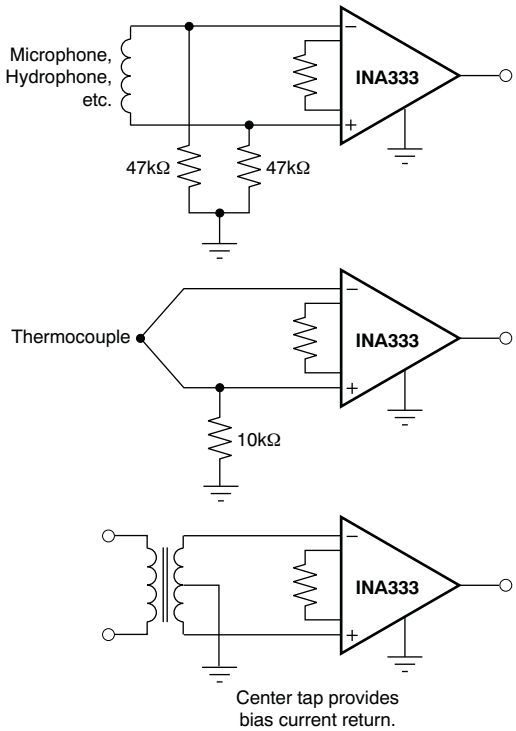


Figure 34. Providing an Input Common-Mode Current Path

8.2.2.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA333 device is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see Figure 20 to Figure 23 in the *Typical Characteristics* section.

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333 is near 0 V even though both inputs are overloaded.

8.2.2.7 Operating Voltage

The INA333 operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.2.2.8 Low Voltage Operation

The INA333 device can be operated on power supplies as low as ±0.9 V. Most parameters vary only slightly throughout this supply voltage range—see the *Typical Characteristics* section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. Figure 20 to Figure 23 show the range of linear operation for various supply voltages and gains.

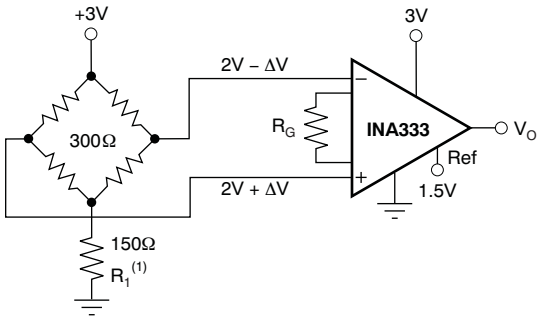
8.2.2.9 Single-Supply Operation

The INA333 device can be used on single power supplies of 1.8 V to 5.5 V. Figure 35 shows a basic single-supply circuit. The output REF pin is connected to mid-supply. Zero differential input voltage demands an output voltage of mid-supply. Actual output voltage swing is limited to approximately 50 mV more than ground, when the load is referred to ground as shown. Figure 29 shows how the output voltage swing varies with output current.

Copyright © 2008–2015, Texas Instruments Incorporated

With single-supply operation, V_{IN+} and V_{IN-} must both be 0.1 V more than ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

To show the issues affecting low voltage operation, consider the circuit in Figure 35. It shows the INA333 device operating from a single 3-V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier inputs.



(1) R_1 creates proper common-mode voltage, only for low-voltage operation—see *Single-Supply Operation*.

Figure 35. Single-Supply Bridge Amplifier

8.2.2.10 Input Protection

The input pins of the INA333 device are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3 V, the input signal current should be limited to less than 10 mA to protect the internal clamp diodes. This current limiting can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

Copyright © 2008–2015, Texas Instruments Incorporated

8.2.3 Application Curves

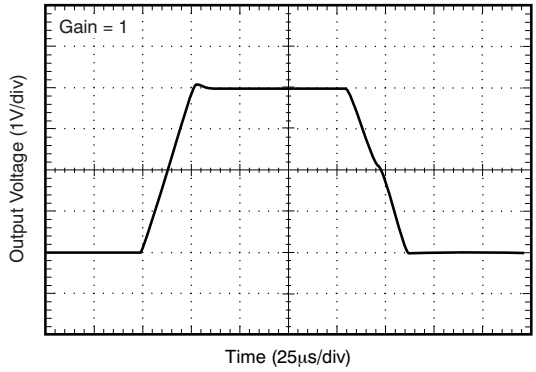


Figure 36. Large Signal Response

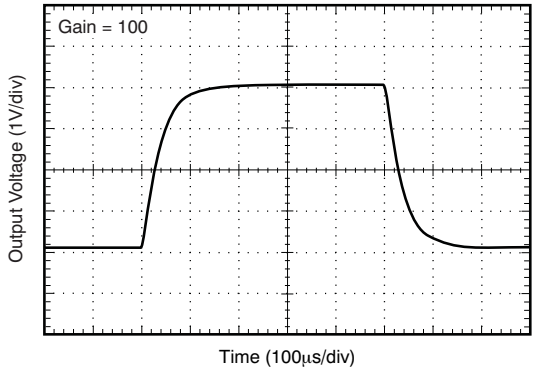


Figure 37. Large-Signal Step Response

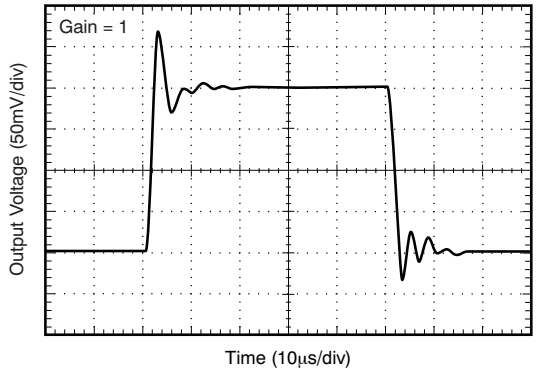


Figure 38. Small-Signal Step Response

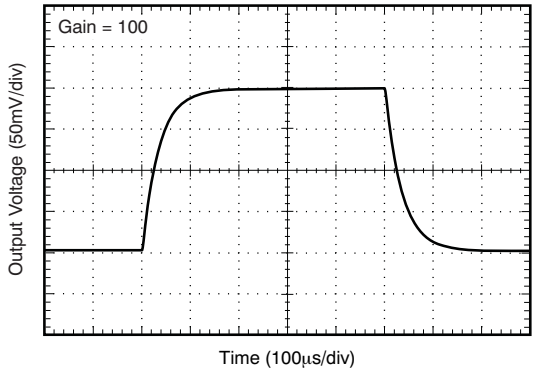


Figure 39. Small-Signal Step Response

9 Power Supply Recommendations

The minimum power supply voltage for INA333 is 1.8 V and the maximum power supply voltage is 5.5 V. For optimum performance, 3.3 V to 5 V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF bypass capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in the susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The INA333 device has been specifically designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the V_{IN+} and V_{IN-} inputs. As a result, the INA333 device demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may continue to cause varying offset levels, however, and may require additional shielding.

10.2 Layout Example

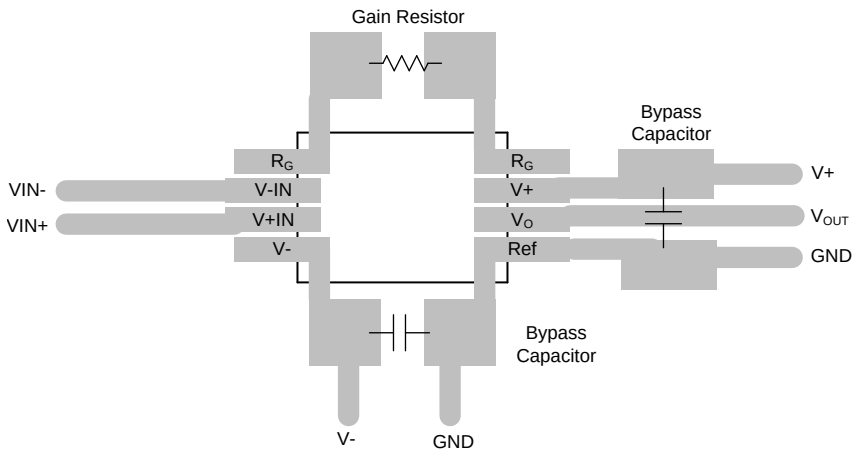


Figure 40. INA333 Layout

Copyright © 2008–2015, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI (Free Download Software)

Using TINA-TI SPICE-Based Analog Simulation Program with the INA333

TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional DC, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

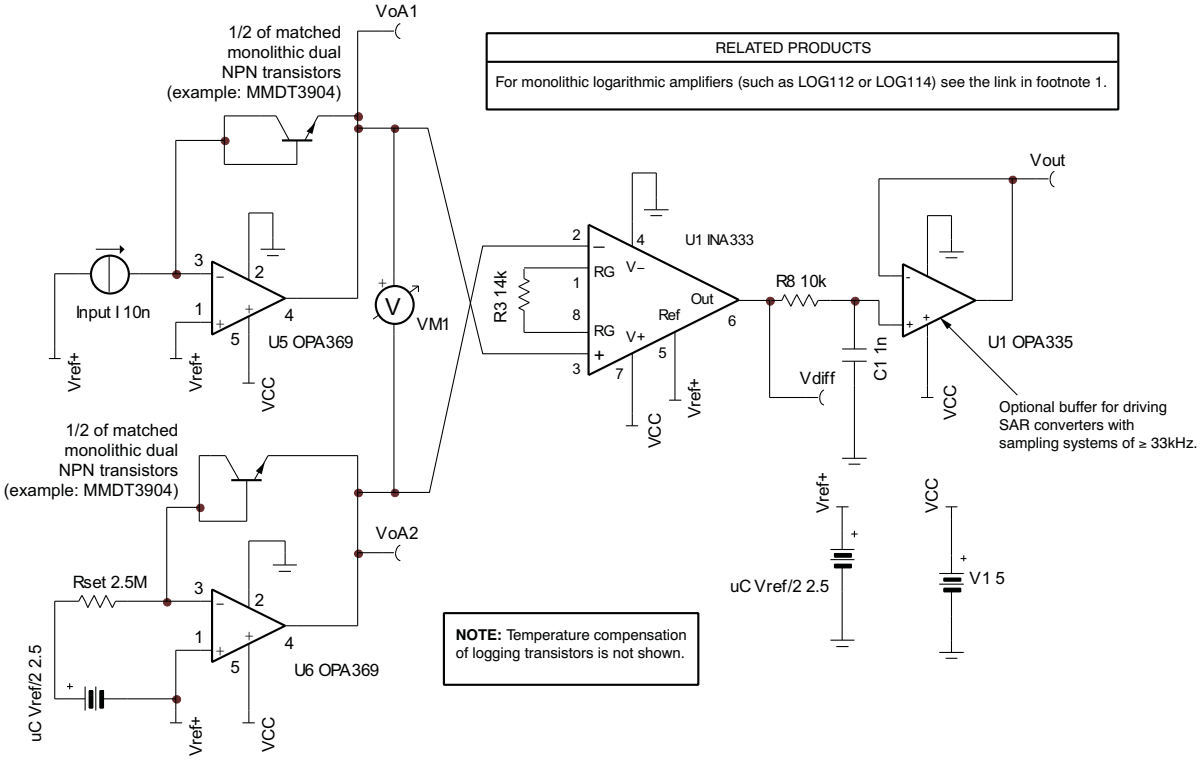
Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 41 and Figure 42 show example TINA-TI circuits for the INA333 device that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

NOTE

These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

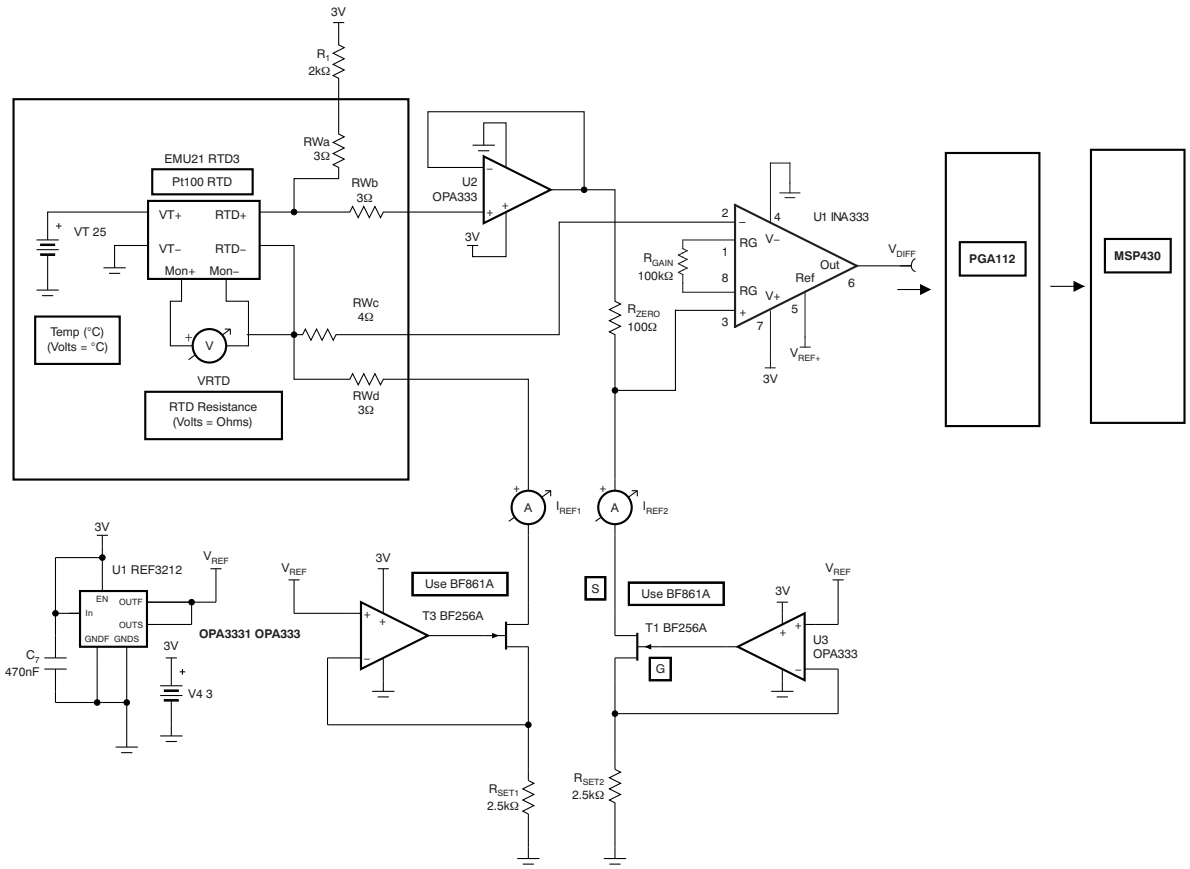


(1) The following link launches the TI logarithmic amplifiers web page: Logarithmic Amplifier Products Home Page

Figure 41. Low-Power Log Function Circuit for Portable Battery-Powered Systems (Example Glucose Meter)

Device Support (continued)

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: Log Circuit.



RWa, RWb, RWc, and RWd simulate wire resistance. These resistors are included to show the four-wire sense technique immunity to line mismatches. This method assumes the use of a four-wire RTD.

Figure 42. Four-Wire, 3-V Conditioner for a PT100 RTD With Programmable Gain Acquisition System

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: PT100 RTD.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Precision, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifiers*, SBOS642
- *50µV VOS, 0.25µV/°C, 35µA CMOS OPERATIONAL AMPLIFIERS Zerø-Drift Series*, SBOS432
- *4ppm/°C, 100µA, SOT23-6 SERIES VOLTAGE REFERENCE*, SBVS058
- *Circuit Board Layout Techniques*, SLOA089

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2008–2015, Texas Instruments Incorporated

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA333AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDGKTG4	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333
INA333AIDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGR.A	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGRG4	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGRG4.A	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A
INA333AIDRGT.A	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	I333A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA333 :

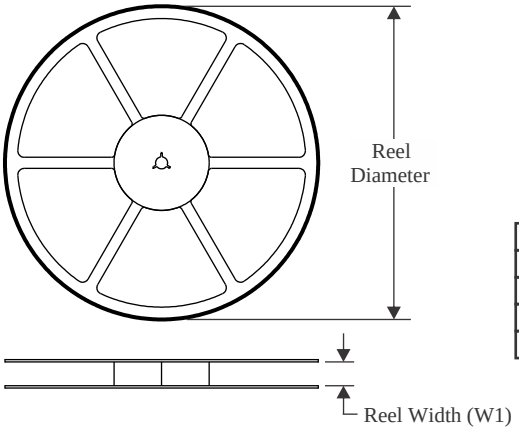
- Automotive : INA333-Q1

NOTE: Qualified Version Definitions:

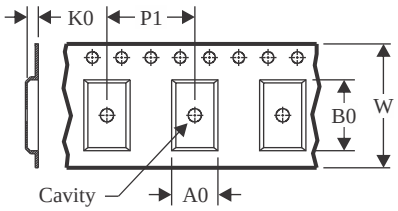
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

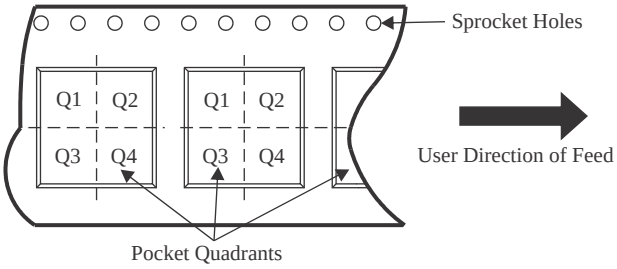


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

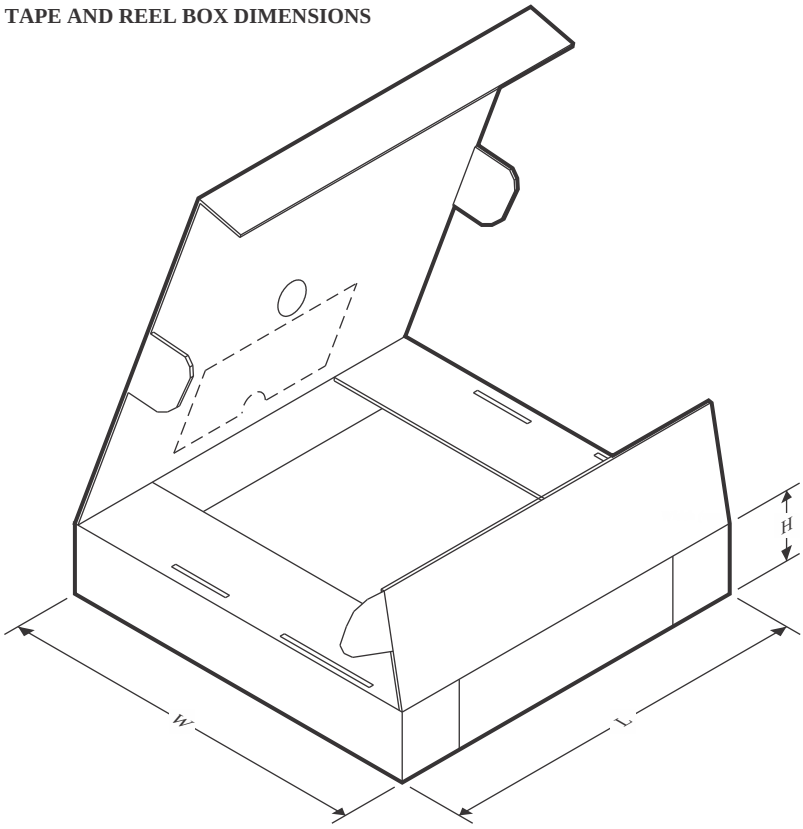
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA333AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA333AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA333AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA333AIDRGRG4	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA333AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

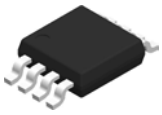


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA333AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA333AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA333AIDRGR	SON	DRG	8	3000	356.0	356.0	35.0
INA333AIDRGRG4	SON	DRG	8	3000	356.0	356.0	35.0
INA333AIDRGT	SON	DRG	8	250	213.0	191.0	35.0

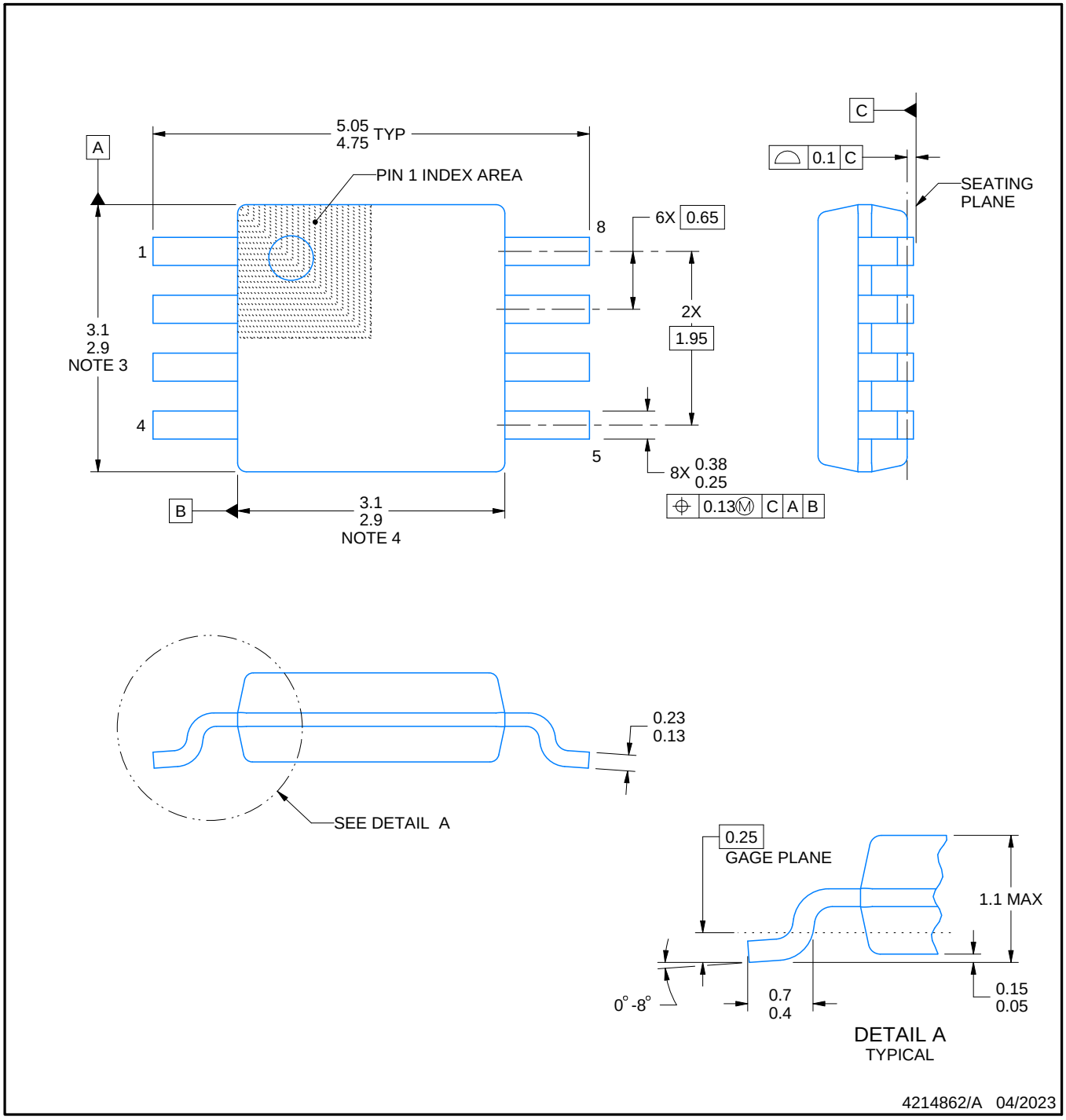
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

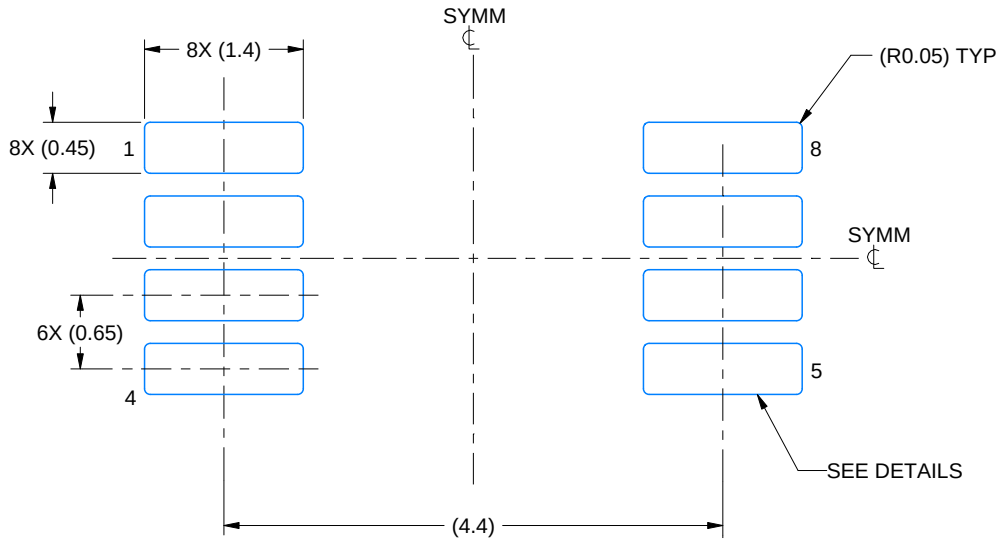
SMALL OUTLINE PACKAGE



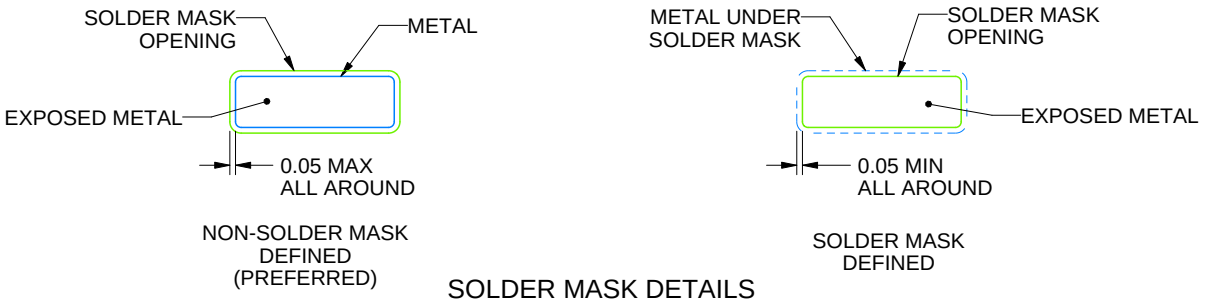
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

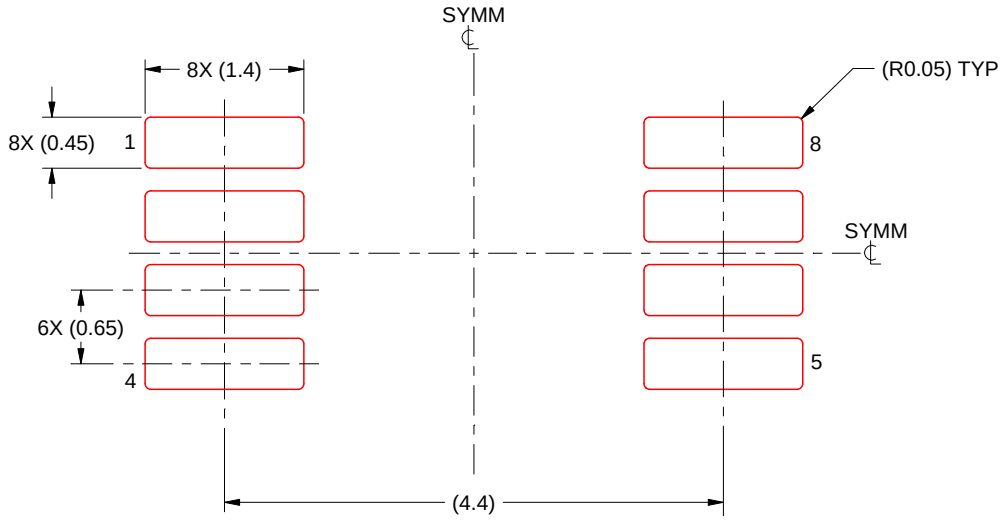


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

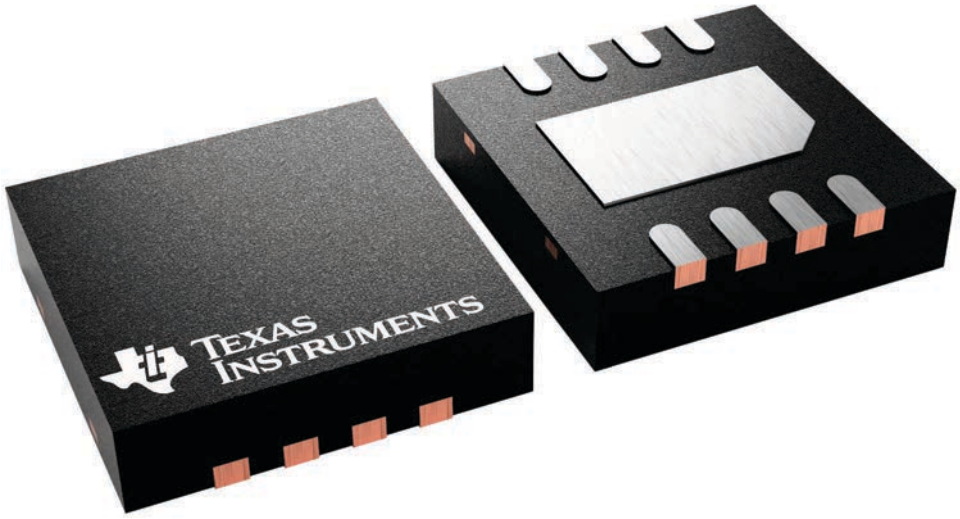
DRG 8

WSON - 0.8 mm max height

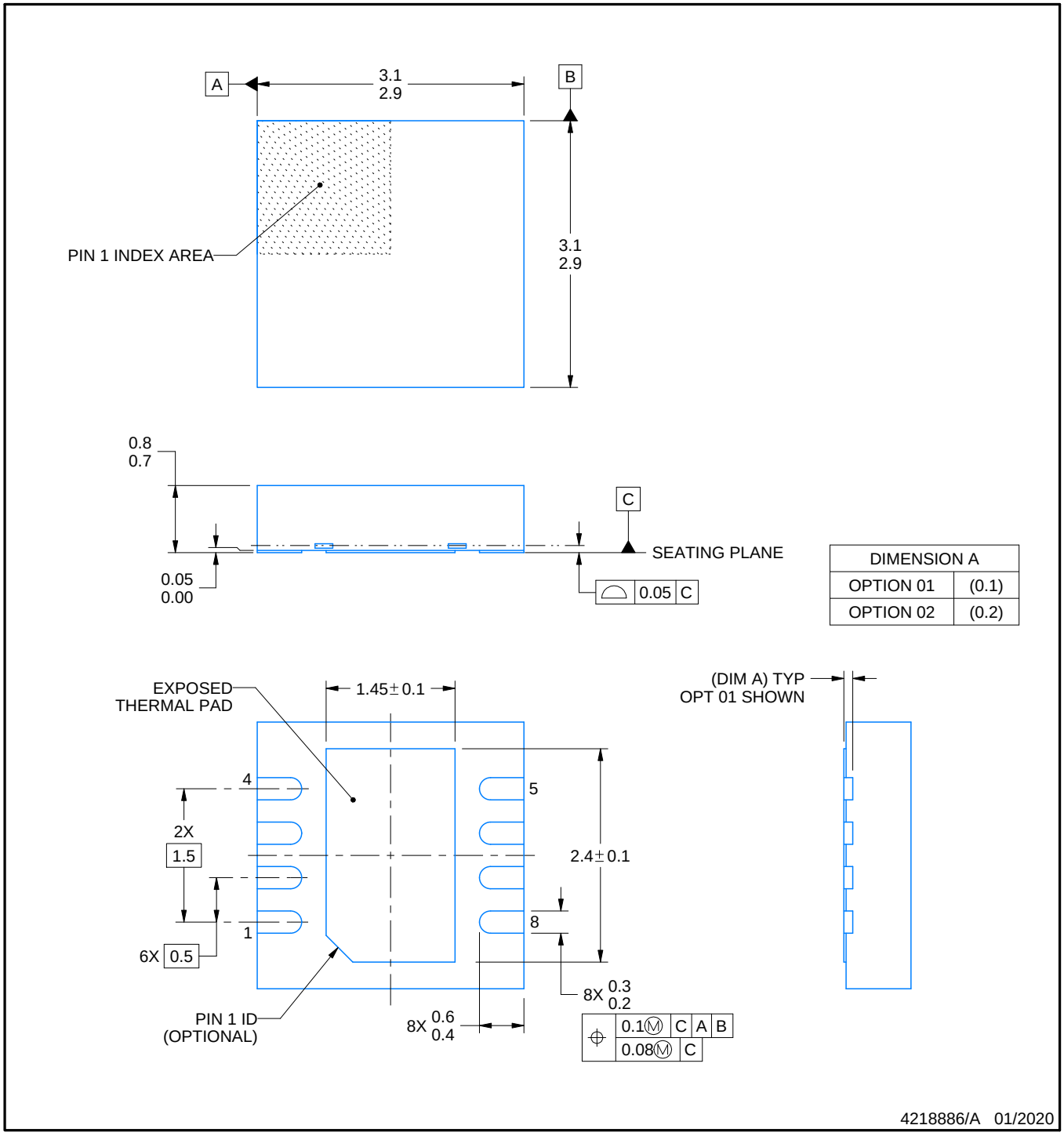
3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



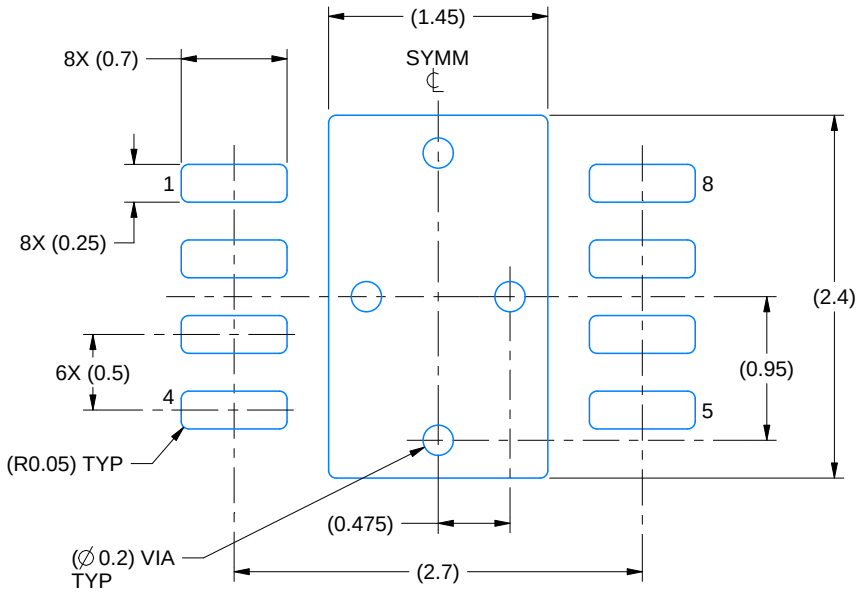
4225794/A



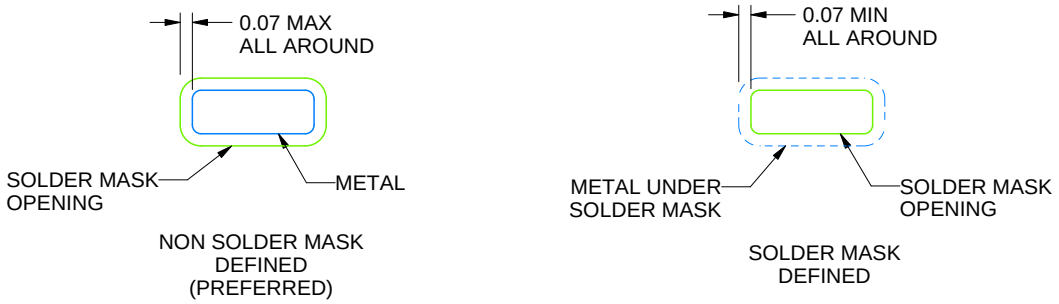
DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

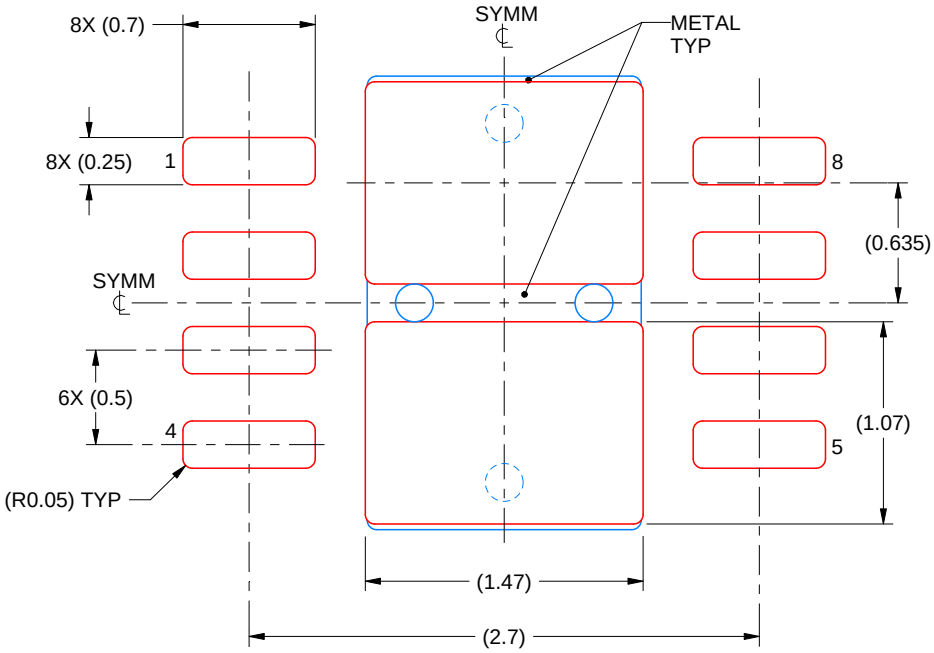


SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated