# UCC2752x Dual 5A High-Speed, Low-Side Gate Drivers

## 1 Features

- Industry-standard pinout
- Two independent gate-drive channels
- 5A peak source and sink-drive current
- Independent-enable function for each output
- TTL and CMOS compatible logic threshold independent of supply voltage
- Hysteretic-logic thresholds for high noise immunity
- Inputs and enable pin-voltage levels not restricted by VDD pin bias supply voltage
- 4.5V to 18V single-supply range
- Outputs held low during VDD-UVLO, (ensures glitch-free operation at power up and power down)
- Fast propagation delays (13ns typical)
- Fast rise and fall times (7ns and 6ns typical)
- 1ns typical delay matching between two channels
- Two outputs are in parallel for higher drive current
- Outputs held low when inputs floating
- PDIP (8), SOIC (8), MSOP (8) PowerPAD™ and 3mm × 3mm WSON-8 package options
- Operating temperature range of –40°C to 140°C

## 2 Applications

- Switched-mode power supplies
- DC-DC converters
- Motor control, solar power
- Gate drive for emerging wide band-gap power devices such as GaN

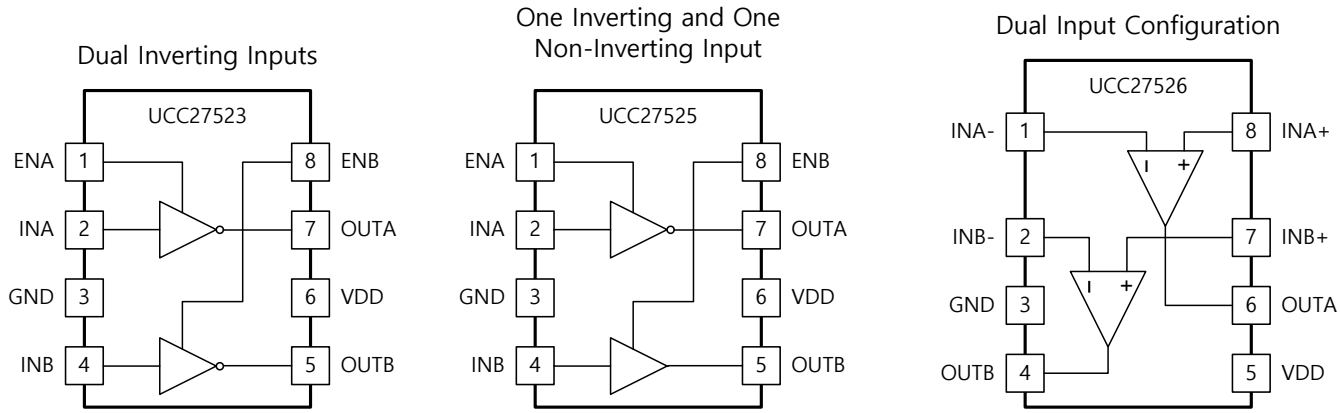
## 3 Description

The UCC2752x family of devices are dual-channel, high-speed, low-side gate-driver devices capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC2752x can deliver high-peak current pulses of up to 5A source and 5A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay (typically 13ns). In addition, the drivers feature matched internal propagation delays between the two channels. These delays are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with one input signal. The input pin thresholds are based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of the VDD supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| UCC27523 | D (SOIC 8) | 4.90mm × 3.91mm |
| | DGN (HVSSOP 8) | 3.00mm × 3.00mm |
| | DSD (WSON 8) | |
| UCC27525 | D (SOIC 8) | 4.90mm × 3.91mm |
| | DGN (HVSSOP 8) | 3.00mm × 3.00mm |
| | DSD (WSON 8) | |
| UCC27526 | DSD (WSON 8) | 3.00mm × 3.00mm |

(1) For all available packages, see Section 13.




**Pin Configurations**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Description (continued)**....3
**5 Pin Configuration and Functions**....4
**6 Specifications**....6
6.1 Absolute Maximum Ratings....6
6.2 ESD Ratings....6
6.3 Recommended Operating Conditions....6
6.4 Thermal Information....7
6.5 Electrical Characteristics....7
6.6 Switching Characteristics....8
6.7 Typical Characteristics....9
**7 Detailed Description**....12
7.1 Overview....12
7.2 Functional Block Diagrams....12
7.3 Feature Description....13
7.4 Device Functional Modes....20
**8 Application and Implementation**....21
8.1 Application Information....21
8.2 Typical Application....21
**9 Power Supply Recommendations**....26
**10 Layout**....27
10.1 Layout Guidelines....27
10.2 Layout Example....28
10.3 Thermal Considerations....28
**11 Device and Documentation Support**....30
11.1 Device Support....30
11.2 Receiving Notification of Documentation Updates....30
11.3 Support Resources....30
11.4 Trademarks....30
11.5 Electrostatic Discharge Caution....30
11.6 Glossary....30
**12 Revision History**....31
**13 Mechanical, Packaging, and Orderable Information**....32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## 4 Description (continued)

The UCC2752x family provides the combination of three standard logic options — dual inverting, dual noninverting, one inverting and one noninverting driver. The UCC27526 features a dual input design which offers flexibility of both inverting (IN– pin) and non-inverting (IN+ pin) configuration for each channel. Either IN+ or IN– pin controls the state of the driver output. The unused input pin is used for enable and disable functions. For safety purpose, internal pullup and pulldown resistors on the input pins of all the devices in UCC2752x family ensure that outputs are held LOW when input pins are in floating condition. The UCC27523 and UCC27525 devices feature Enable pins (ENA and ENB) to have better control of the operation of the driver applications. The pins are internally pulled up to VDD for active-high logic and are left open for standard operation.

The UCC2752x family of devices are available in SOIC-8 (D), MSOP-8 with exposed pad (DGN) and 3mm × 3mm WSON-8 with exposed pad (DSD) packages. The UCC27526 is only offered in a 3mm × 3mm WSON (DSD) package.

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## 5 Pin Configuration and Functions

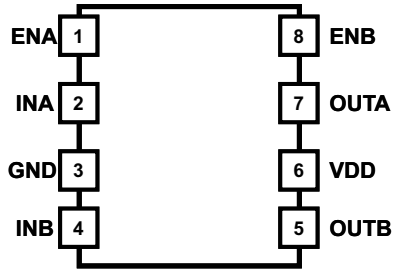


**Figure 5-1. D, DGN, Package UCC2752(3,5) 8-Pin SOIC-8, HVSSOP Top View**

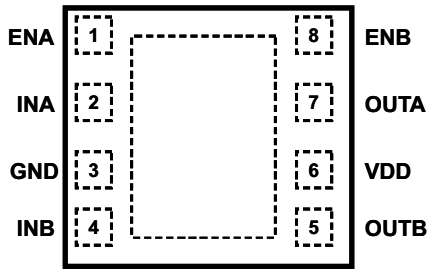


**Figure 5-2. DSD Package UCC2752(3,5) 8-Pin WSON Top View**

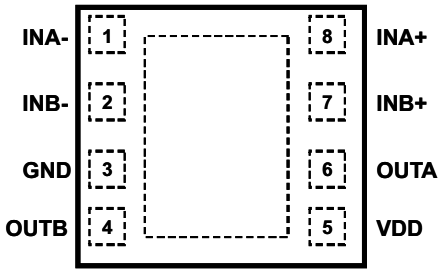


**Figure 5-3. DSD Package UCC27526 8-Pin WSON Top View**

**Table 5-1. Pin Functions (UCC27523 / UCC27525)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | ENA | I | **Enable input for Channel A:** ENA biased LOW Disables Channel A output regardless of INA state, ENA biased HIGH or floating Enables Channel A output, ENA allowed to float hence the pin-to-pin compatibility with UCC2732X N/C pin. |
| 2 | INA | I | **Input to Channel A:** Inverting Input in UCC27523, Non-Inverting Input in UCC27524, Inverting Input in UCC27525, OUTA held LOW if INA is unbiased or floating. |
| 3 | GND | - | **Ground:** All signals referenced to this pin. |
| 4 | INB | I | **Input to Channel B:** Inverting Input in UCC27523, Non-Inverting Input in UCC27524, Non-Inverting Input in UCC27525, OUTB held LOW if INB is unbiased or floating. |
| 5 | OUTB | O | **Output of Channel B** |
| 6 | VDD | I | **Bias supply input** |
| 7 | OUTA | O | **Output of Channel A** |
| 8 | ENB | I | **Enable input for Channel B:** ENB biased LOW Disables Channel B output regardless of INB state, ENB biased HIGH or floating Enables Channel B output, ENB allowed to float hence the pin-to-pin compatibility with UCC2732X N/C pin. |


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**Table 5-2. Pin Functions (UCC27526)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | INA– | I | **Inverting Input to Channel A:** When Channel A is used in Non-Inverting configuration, connect INA– to GND in order to Enable Channel A output, OUTA held LOW if INA– is unbiased or floating. |
| 2 | INB– | I | **Inverting Input to Channel B:** When Channel B is used in Non-Inverting configuration, connect INB– to GND in order to Enable Channel B output, OUTB held LOW if INB– is unbiased or floating. |
| 3 | GND | - | **Ground:** All signals referenced to this pin. |
| 4 | OUTB | I | **Output of Channel B** |
| 5 | VDD | O | **Bias Supply Input** |
| 6 | OUTA | I | **Output of Channel A** |
| 7 | INB+ | O | **Non-Inverting Input to Channel B:** When Channel B is used in Inverting configuration, connect INB+ to VDD in order to Enable Channel B output, OUTB held LOW if INB+ is unbiased or floating. |
| 8 | INA+ | I | **Non-Inverting Input to Channel A:** When Channel A is used in Inverting configuration, connect INA+ to VDD in order to Enable Channel A output, OUTA held LOW if INA+ is unbiased or floating. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1] [2]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | VDD | –0.3 | 20 | V |
| OUTA, OUTB voltage | DC | –0.3 | VDD + 0.3 | V |
| | Repetitive pulse < 200 ns[4] | –2 | VDD + 0.3 | V |
| Output continuous source/sink current | $I_{OUT_DC}$ | | 0.3 | A |
| Output pulsed source/sink current (0.5 µs) | $I_{OUT_pulsed}$ | | 5 | A |
| INA, INB, INA+, INA–, INB+, INB–, ENA, ENB voltage[3] | | –0.3 | 20 | V |
| Operating virtual junction temperature, $T_J$ | | –40 | 150 | °C |
| Lead temperature | Soldering, 10 s | | 300 | °C |
| | Reflow | | 260 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Section 13 for thermal limitations and considerations of packages.
(3) The maximum voltage on the Input and Enable pins is not restricted by the voltage on the $V_{DD}$ pin.
(4) Values are verified by characterization on bench.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±4000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, VDD | 4.5 | 12 | 18 | V |
| Operating junction temperature | –40 | | 140 | °C |
| Input voltage, INA, INB, INA+, INA–, INB+, INB– | 0 | | 18 | V |
| Enable voltage, ENA and ENB | 0 | | 18 | |


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | UCC27523/5 | | UCC27523/5/6 | UNIT |
|---|---|---|---|---|---|
| | | SOIC (D) | MSOP (DGN) | WSON (DSD) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 130.9 | 71.8 | 46.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 80 | 65.6 | 46.7 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 71.4 | 7.4 | 22.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.9 | 7.4 | 0.7 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 70.9 | 31.5 | 22.6 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | 19.6 | 9.5 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

$V_{DD}$ = 12 V, $T_A$ = $T_J$ = –40°C to 140°C, 1-µF capacitor from $V_{DD}$ to GND. Currents are positive into, negative out of the specified terminal (unless otherwise noted,)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BIAS CURRENTS** | | | | | | |
| $I_{DD(off)}$ | Start-up current, | $V_{DD}$ = 3.4 V, INA = $V_{DD}$, INB = $V_{DD}$ | 55 | 110 | 175 | µA |
| | | $V_{DD}$ = 3.4 V, INA = GND, INB = GND | 25 | 75 | 145 | |
| **UNDERVOLTAGE LOCKOUT (UVLO)** | | | | | | |
| $V_{ON}$ | Supply start threshold | $T_J$ = 25°C | 3.91 | 4.2 | 4.5 | V |
| | | $T_J$ = –40°C to 140°C | 3.7 | 4.2 | 4.65 | |
| $V_{OFF}$ | Minimum operating voltage after supply start | | 3.4 | 3.9 | 4.4 | |
| VDD_H | Supply voltage hysteresis | | 0.2 | 0.3 | 0.5 | |
| **INPUTS (INA, INB, INA+, INA–, INB+, INB–)** | | | | | | |
| $V_{IN_H}$ | Input signal high threshold | Output high for non-inverting input pins<br>Output low for inverting input pins | 1.9 | 2.1 | 2.3 | V |
| $V_{IN_L}$ | Input signal low threshold | Output low for non-inverting input pins<br>Output high for inverting input pins | 1 | 1.2 | 1.4 | |
| $V_{IN_HYS}$ | Input hysteresis | | 0.7 | 0.9 | 1.1 | |
| **ENABLE (ENA, ENB)** | | | | | | |
| $V_{EN_H}$ | Enable signal high threshold | Output enabled | 1.9 | 2.1 | 2.3 | V |
| $V_{EN_L}$ | Enable signal low threshold | Output disabled | 0.95 | 1.15 | 1.35 | |
| $V_{EN_HYS}$ | Enable hysteresis | | 0.7 | 0.95 | 1.1 | |
| **OUTPUTS (OUTA, OUTB)** | | | | | | |
| $I_{SNK/SRC}$ | Sink/source peak current[1] | $C_{LOAD}$ = 0.22 µF, $F_{SW}$ = 1 kHz | | ±5 | | A |
| $V_{DD}$-$V_{OH}$ | High output voltage | $I_{OUT}$ = –10 mA | | | 0.075 | V |
| $V_{OL}$ | Low output voltage | $I_{OUT}$ = 10 mA | | | 0.01 | |
| $R_{OH}$ | Output pullup resistance[2] | $I_{OUT}$ = –10 mA | 2.5 | 5 | 7.5 | Ω |
| $R_{OL}$ | Output pulldown resistance | $I_{OUT}$ = 10 mA | 0.15 | 0.5 | 1 | Ω |

(1) Ensured by design.
(2) $R_{OH}$ represents on-resistance of only the P-Channel MOSFET device in pullup structure of UCC2752X output stage.

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## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_R$ | Rise time (1) | $C_{LOAD}$ = 1.8 nF | | 7 | 18 | ns |
| $t_F$ | Fall time(1) | $C_{LOAD}$ = 1.8 nF | | 6 | 10 | |
| $t_M$ | Delay matching between 2 channels | INA = INB, OUTA and OUTB at 50% transition point | | 1 | 4 | |
| $t_{PW}$ | Minimum input pulse width that changes the output state | | | 15 | 25 | |
| $t_{D1}$, $t_{D2}$ | Input to output propagation delay (1) | $C_{LOAD}$ = 1.8 nF, 5-V input pulse | 6 | 13 | 23 | |
| $t_{D3}$, $t_{D4}$ | EN to output propagation delay (1) | $C_{LOAD}$ = 1.8 nF, 5-V enable pulse | 6 | 13 | 23 | |

(1) See timing diagrams in Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4

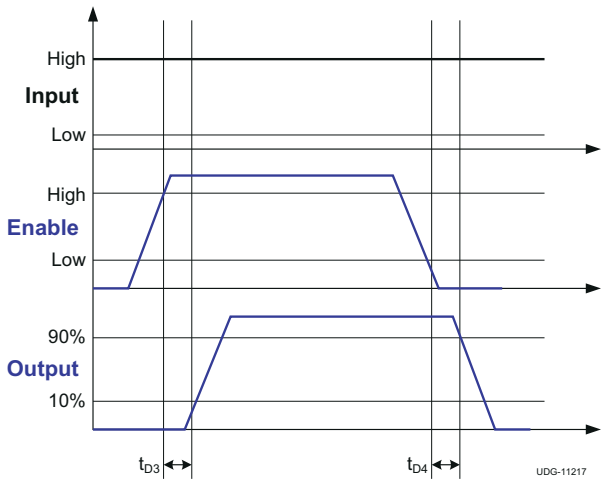


**Figure 6-1. Enable Function (For Non-Inverting Input Driver Operation)**

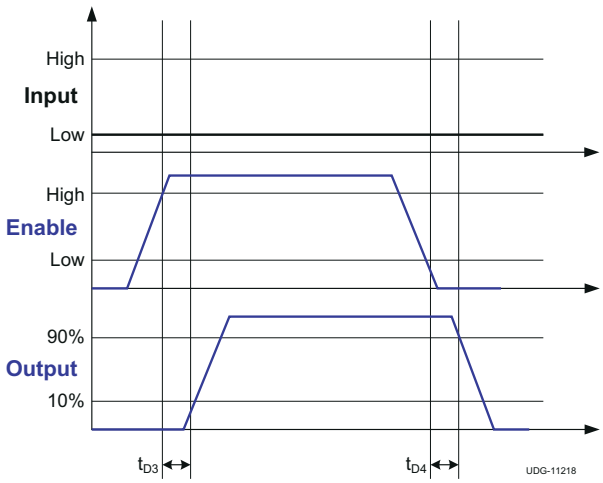


**Figure 6-2. Enable Function (For Inverting Input Driver Operation)**

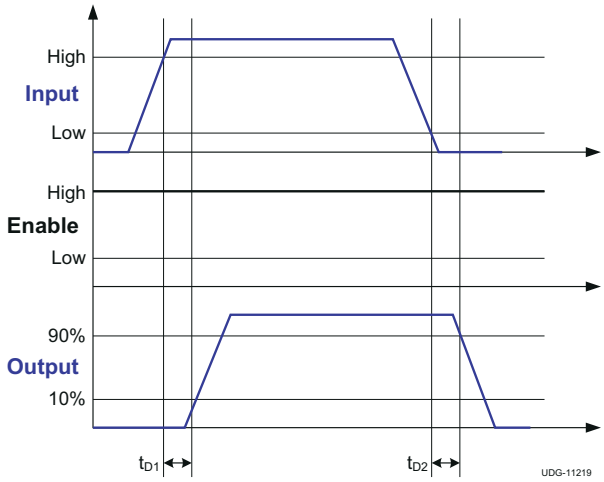


**Figure 6-3. Non-Inverting Input Driver Operation**

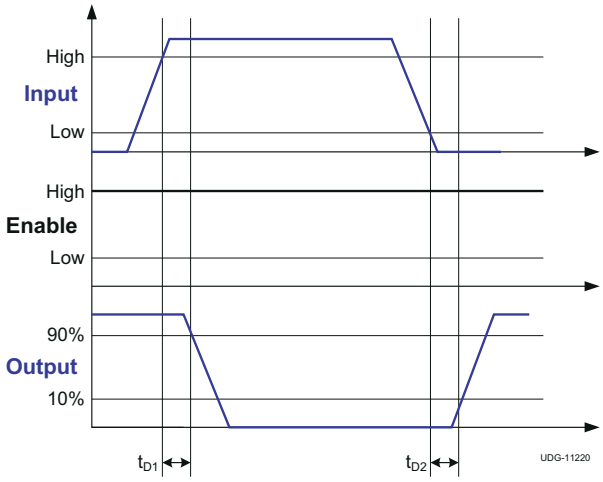


**Figure 6-4. Inverting Input Driver Operation**


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## 6.7 Typical Characteristics

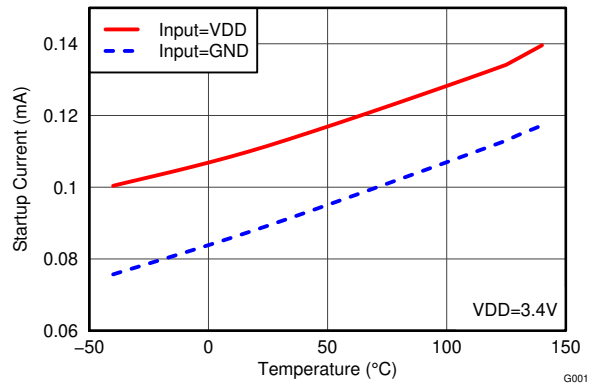


**Figure 6-5. Start-Up Current vs Temperature**

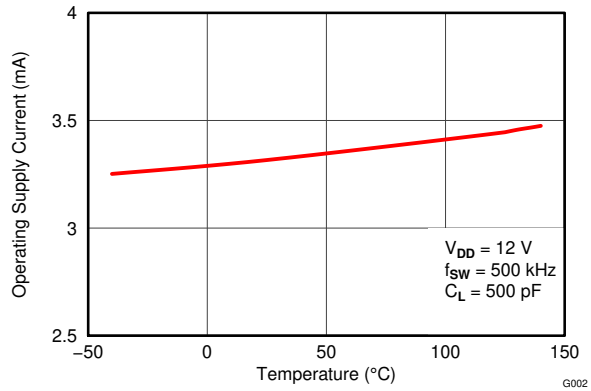


**Figure 6-6. Operating Supply Current vs Temperature (Outputs Switching)**

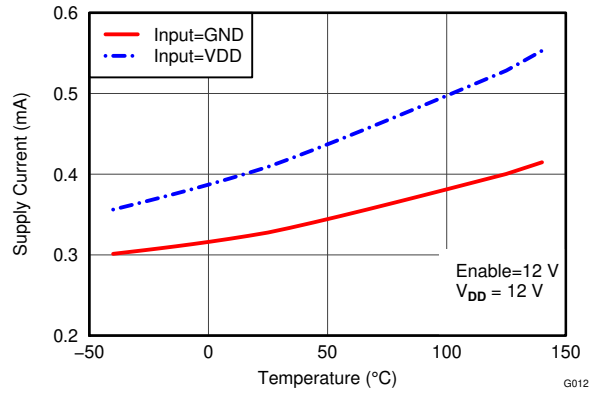


**Figure 6-7. Supply Current vs Temperature (Outputs in DC ON/OFF Condition)**

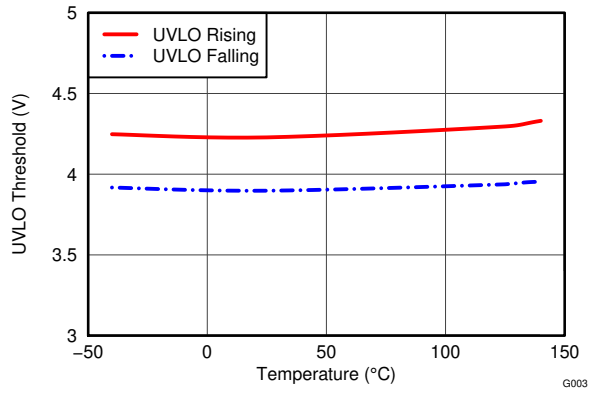


**Figure 6-8. UVLO Threshold vs Temperature**

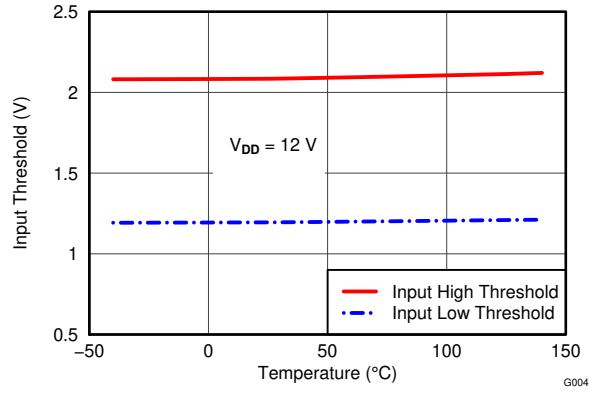


**Figure 6-9. Input Threshold vs Temperature**

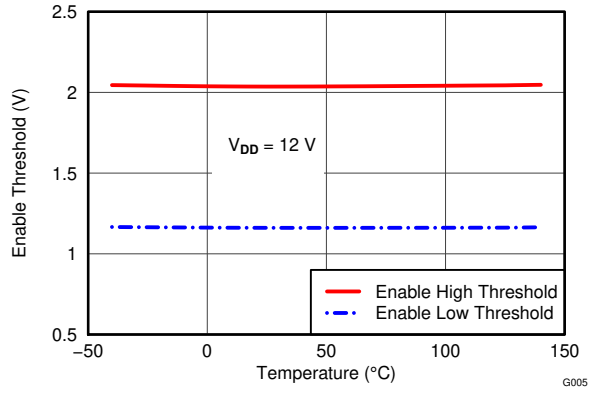


**Figure 6-10. Enable Threshold vs Temperature**

## 6.7 Typical Characteristics (continued)

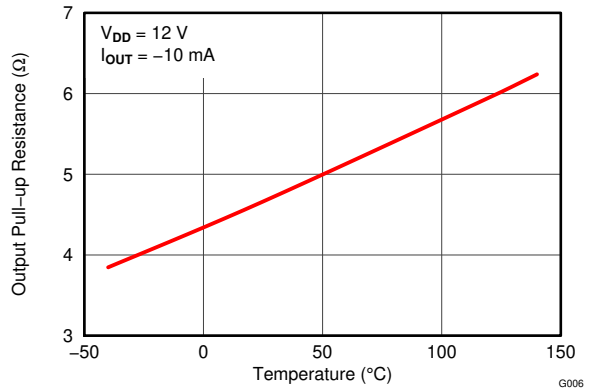


**Figure 6-11. Output Pullup Resistance vs Temperature**

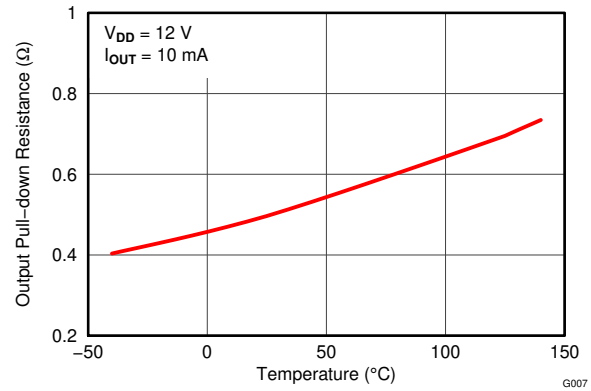


**Figure 6-12. Output Pulldown Resistance vs Temperature**

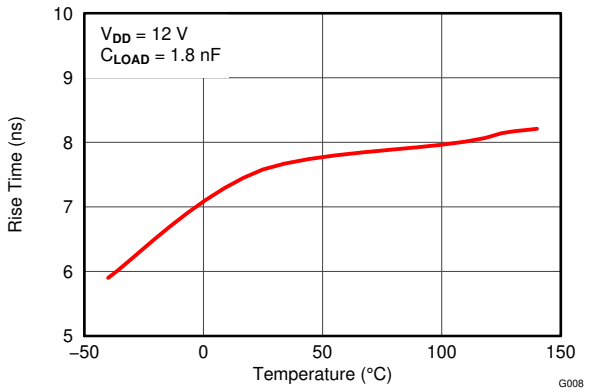


**Figure 6-13. Rise Time vs Temperature**

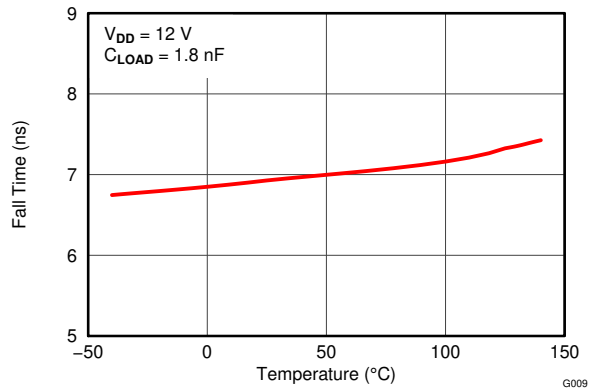


**Figure 6-14. Fall Time vs Temperature**

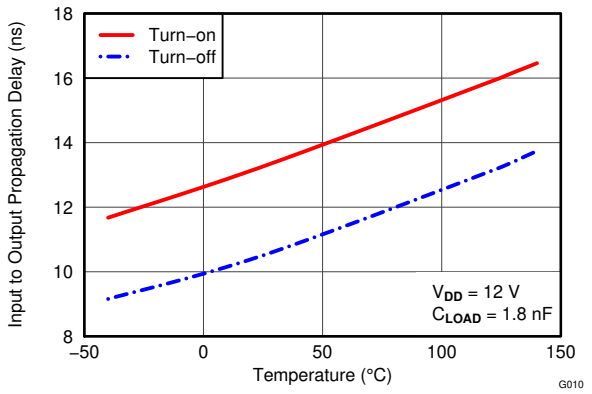


**Figure 6-15. Input to Output Propagation Delay vs Temperature**

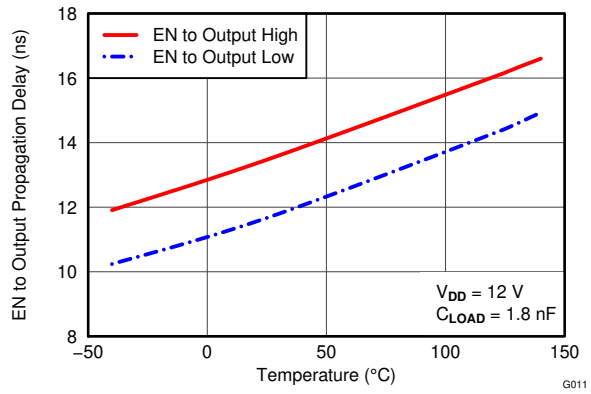


**Figure 6-16. EN to Output Propagation Delay vs Temperature**


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## 6.7 Typical Characteristics (continued)

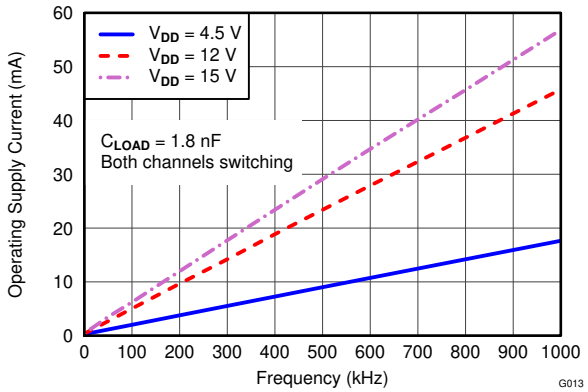


**Figure 6-17. Operating Supply Current vs Frequency**

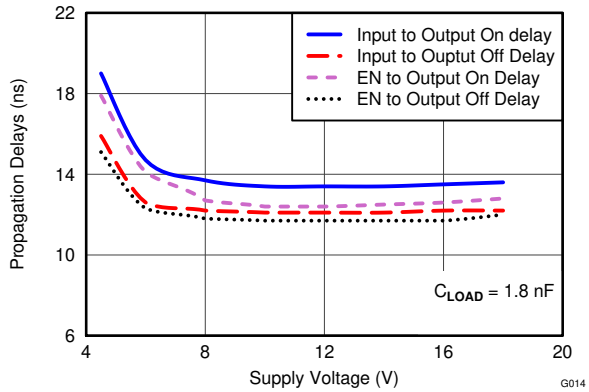


**Figure 6-18. Propagation Delays vs Supply Voltage**

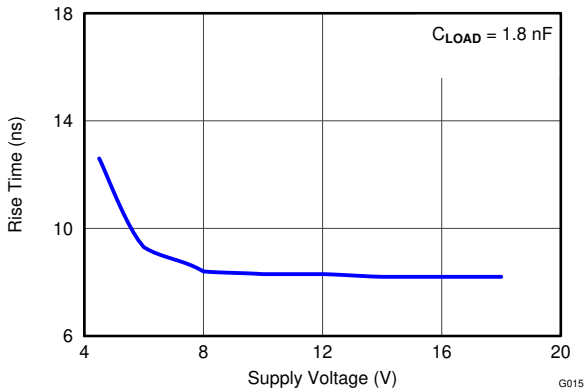


**Figure 6-19. Rise Time vs Supply Voltage**

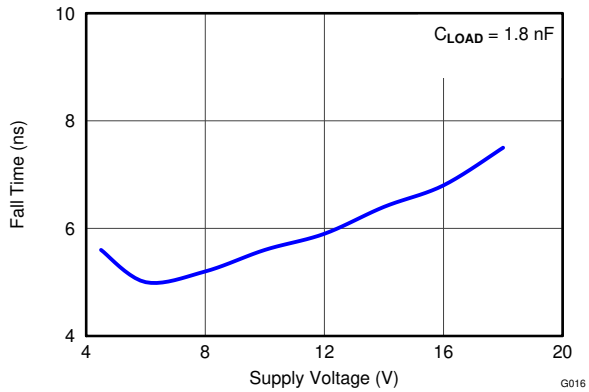


**Figure 6-20. Fall Time vs Supply Voltage**

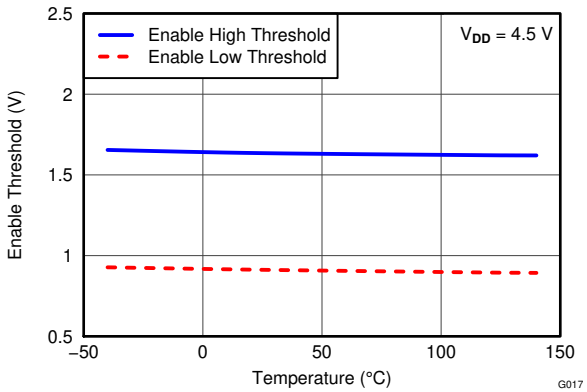


**Figure 6-21. Enable Threshold vs Temperature**

# 7 Detailed Description

## 7.1 Overview

The UCC2752x family of products represent TI's latest generation of dual-channel, low-side, high-speed gate-driver devices featuring 5-A source and sink current capability, industry best-in-class switching characteristics and a host of other features listed in Table 7-1 all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

**Table 7-1. UCC2752x Family of Features and Benefits**

| FEATURE | BENEFIT |
|---|---|
| Best-in-class 13-ns (typ) propagation delay | Extremely low-pulse transmission distortion |
| 1-ns (typ) delay matching between channels | Ease of paralleling outputs for higher (2 times) current capability, ease of driving parallel-power switches |
| Expanded VDD Operating range of 4.5 to 18 V | Flexibility in system design |
| Expanded operating temperature range of –40°C to 140°C (See Section 6.5) | |
| VDD UVLO Protection | Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down |
| Outputs held Low when input pins (INx) in floating condition | Safety feature, especially useful in passing abnormal condition tests during safety certification |
| Outputs enable when enable pins (ENx) in floating condition | Pin-to-pin compatibility with UCC2732X family of products from TI, in designs where pin 1 and 8 are in floating condition |
| CMOS/TTL compatible input and enable threshold with wide hysteresis | Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power |
| Ability of input and enable pins to handle voltage levels not restricted by $V_{DD}$ pin bias voltage | System simplification, especially related to auxiliary bias supply architecture |

## 7.2 Functional Block Diagrams

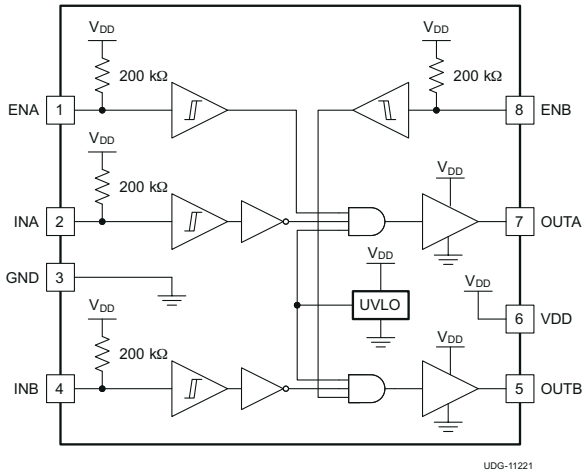


**Figure 7-1. UCC27523 Block Diagram**

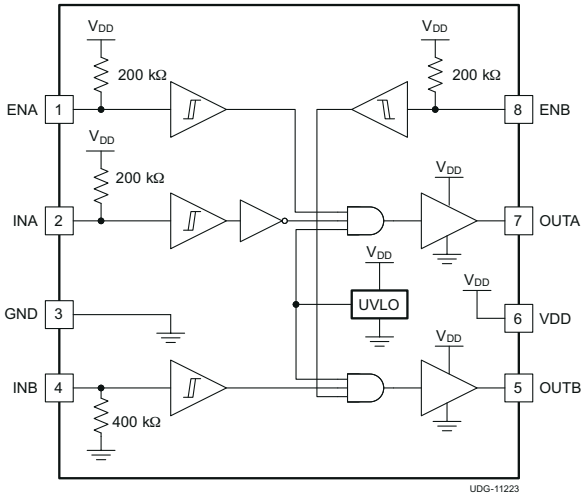


**Figure 7-2. UCC27525 Block Diagram**


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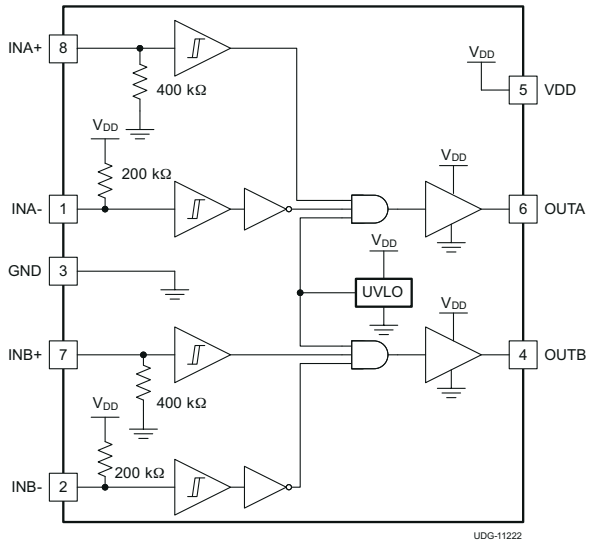


**Figure 7-3. UCC27526 Block Diagram**

## 7.3 Feature Description

### *7.3.1 $V_{DD}$ and Undervoltage Lockout*

The UCC2752x devices have internal undervoltage-lockout (UVLO) protection feature on the $V_{DD}$ pin supply circuit blocks. When $V_{DD}$ is rising and the level is still below UVLO threshold, this circuit holds the output LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis prevents chatter when low $V_{DD}$ supply voltages have noise from the power supply and also when there are droops in the $V_{DD}$ bias voltage when the system commences switching and there is a sudden increase in $I_{DD}$. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

For example, at power up, the UCC2752x driver-device output remains LOW until the $V_{DD}$ voltage reaches the UVLO threshold if Enable pin is active or floating. The magnitude of the OUT signal rises with $V_{DD}$ until steady-state $V_{DD}$ is reached. The non-inverting operation in Figure 7-4 shows that the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. The inverting operation in Figure 7-5 shows that the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. With UCC27526 the output turns to high-state only if INX+ is high and INX– is low after the UVLO threshold is reached.

Because the device draws current from the $V_{DD}$ pin to bias all internal circuits, for the best high-speed circuit performance, TI recommends two $V_{DD}$ bypass capacitors to prevent noise problems. TI highly recommends using surface-mount components. A 0.1-µF ceramic capacitor must be located as close as possible to the $V_{DD}$ to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-µF) with relatively low ESR must be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

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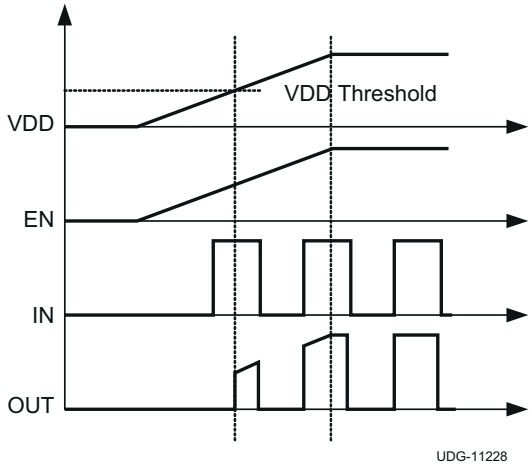


**Figure 7-4. Power up Non-Inverting Driver**

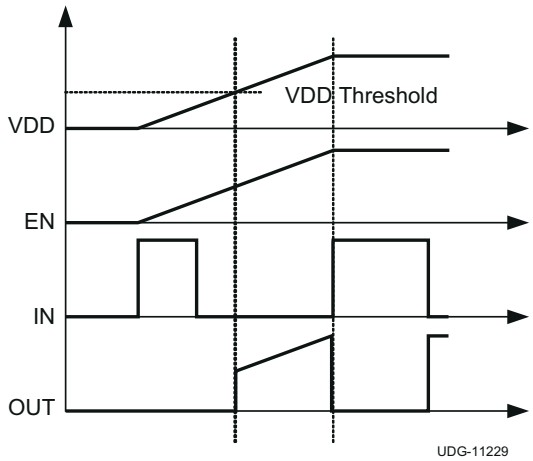


**Figure 7-5. Power up Inverting Driver**

### *7.3.2 Operating Supply Current*

The UCC2752x products feature very low quiescent $I_{DD}$ currents. The typical operating-supply current in UVLO state and fully on state (under static and switching conditions) are summarized in Figure 6-5, Figure 6-6 and Figure 6-7. The $I_{DD}$ current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 6-6) represents lowest quiescent $I_{DD}$ current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent $I_{DD}$ current, the average $I_{OUT}$ current due to switching and finally any current related to pullup resistors on the enable pins and inverting input pins. For example when the inverting Input pins are pulled low additional current is drawn from $V_{DD}$ supply through the pullup resistors (refer to Figure 7-1 though Figure 7-3). Knowing the operating frequency ($f_{SW}$) and the MOSFET gate ($Q_G$) charge at the drive voltage being used, the average $I_{OUT}$ current can be calculated as product of $Q_G$ and $f_{SW}$.

A complete characterization of the $I_{DD}$ current as a function of switching frequency at different $V_{DD}$ bias voltages under 1.8-nF switching load in both channels is provided in Figure 6-17. The strikingly linear variation and close correlation with theoretical value of average $I_{OUT}$ indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.


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### 7.3.3 Input Stage

The input pins of UCC2752x gate-driver devices are based on a TTL and CMOS compatible input-threshold logic that is independent of the $V_{DD}$ supply voltage. With typically high threshold = 2.1 V and typically low threshold = 1.2 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. Wider hysteresis (typ 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. UCC2752x devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 6-9). The very low input capacitance on these pins reduces loading and increases switching speed.

The UCC2752x devices feature an important safety feature wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using $V_{DD}$ pullup resistors on all the Inverting inputs (INA, INB in UCC27523, INA in UCC27525 and INA–, INB– in UCC27526) or GND pulldown resistors on all the non-inverting input pins (INB in UCC27525 and INA+, INB+ in UCC27526), as shown in the device block diagrams.

While UCC27523/5 devices feature one input pin per channel, the UCC27526 features a dual input configuration with two input pins available to control the output state of each channel. With the UCC27526 device the user has the flexibility to drive each channel using either a non-inverting input pin (INx+) or an inverting input pin (INx–). The state of the output pin is dependent on the bias on both the INx+ and INx– pins (where x = A, B). Once an Input pin is chosen to drive a channel, the other input pin of that channel (the unused input pin) must be properly biased in order to enable the output of the channel. The unused input pin cannot remain in a floating condition because, as mentioned earlier, whenever any input pin is left in a floating condition, the output of that channel is disabled using the internal pullup or pulldown resistors for safety purposes. Alternatively, the unused input pin is used effectively to implement an enable/disable function, as explained below.

- In order to drive the channel x (x = A or B) in a non-inverting configuration, apply the PWM control input signal to INx+ pin. In this case, the unused input pin, INx-, must be biased low (for example, tied to GND) in order to enable the output of this channel.
  - Alternately, the INx– pin can be used to implement the enable/disable function using an external logic signal. OUTx is disabled when INx- is biased High and OUTx is enabled when INX– is biased low.
- In order to drive the channel x (x = A or B) in an Inverting configuration, apply the PWM control input signal to INX– pin. In this case, the unused input pin, INX+, must be biased high (for example, tied to VDD) in order to enable the output of the channel.
  - Alternately, the INX+ pin can be used to implement the enable/disable function using an external logic signal. OUTX is disabled when INX+ is biased low and OUTX is enabled when INX+ is biased high.
- Finally, it is worth noting that the UCC27526 output pin can be driven into high state only when INx+ pin is biased high and INx- input is biased low.

Refer to the input/output logic truth table and typical application diagrams, (Figure 8-1, Figure 8-2, and Figure 8-2), for additional clarification.

The input stage of each driver is driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (< 200 ns) with a slow changing input voltage, the output of the driver may switch repeatedly at a high frequency. While the wide hysteresis offered in UCC2752x definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then TI highly recommends an external resistance between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate-driver device package and transferring it into the external resistor itself.

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### 7.3.4 Enable Function

The enable function is an extremely beneficial feature in gate-driver devices especially for certain applications such as synchronous rectification where the driver outputs disable in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

UCC27523/5 devices are provided with independent enable pins ENx for exclusive control of each driver-channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus when ENx pins are driven high the drivers are enabled and when ENx pins are driven low the drivers are disabled. Like the input pins, the enable pins are also based on a TTL and CMOS compatible input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The UCC2752X devices also feature tight control of the Enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 6-10). The ENx pins are internally pulled up to $V_{DD}$ using pullup resistors as a result of which the outputs of the device are enabled in the default state. Hence the ENx pins are left floating or Not Connected (N/C) for standard operation, where the enable feature is not needed. Essentially, this floating allows the UCC27523/5 devices to be pin-to-pin compatible with TI's previous generation drivers UCC27323/5 respectively, where pins 1, 8 are N/C pins. If the Channel A and Channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB are connected and driven together.

The UCC27526 device does not feature dedicated enable pins. However, as mentioned earlier, an enable/disable function is easily implemented in UCC27526 using the unused input pin. When INx+ is pulled down to GND or INx– is pulled down to VDD, the output is disabled. Thus INx+ pin is used like an enable pin that is based on active high logic, while INx– is used like an enable pin that is based on active low logic. Note that while the ENA, ENB pins in UCC27523/5 are allowed to be in floating condition during standard operation and the outputs will be enabled, the INx+, INx– pins in UCC27526 are not allowed to be floating because this will disable the outputs.


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### 7.3.5 Output Stage

The UCC2752x device output stage features a unique architecture on the pullup structure which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turnon transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P-channel MOSFET and an additional N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turnon. This is accomplished by briefly turning-on the N-channel MOSFET during a narrow instant when the output is changing state from Low to High.

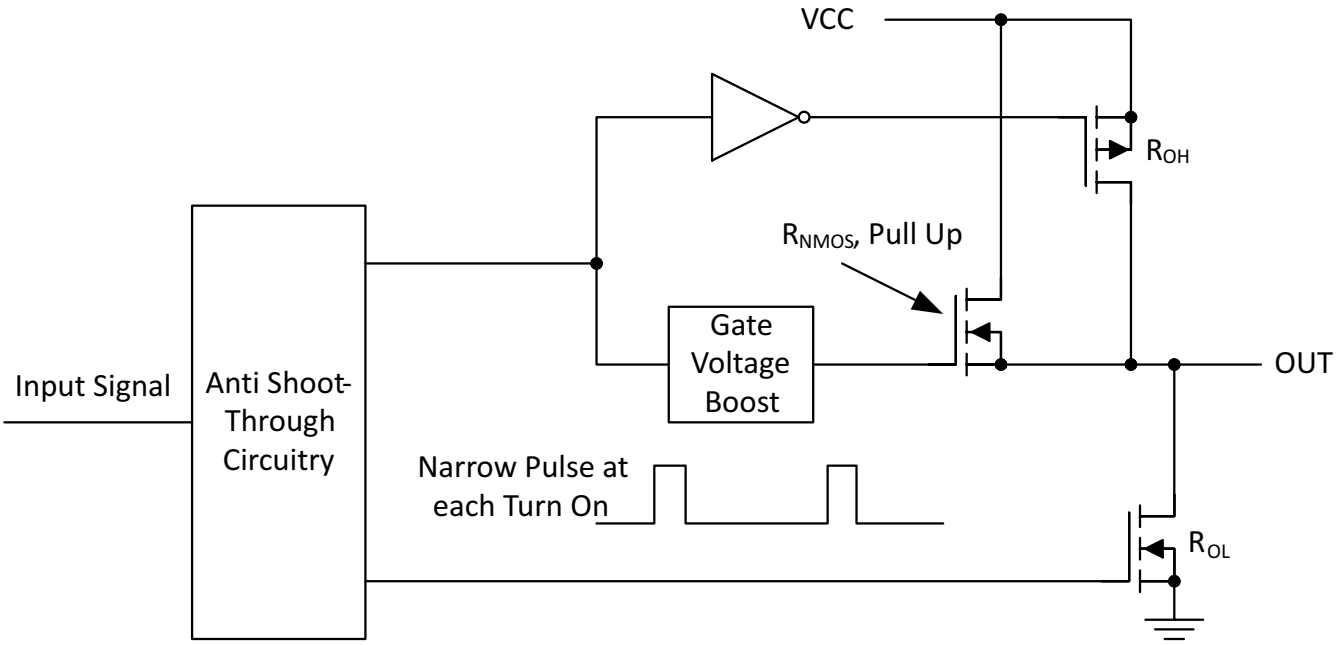


**Figure 7-6. UCC2752x Gate Driver Output Structure**

The $R_{OH}$ parameter (see Section 6.5) is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of UCC2752x pullup stage during the turnon instant is much lower than what is represented by $R_{OH}$ parameter.

The pulldown structure in UCC2752x is simply composed of a N-Channel MOSFET. The $R_{OL}$ parameter (see Section 6.5), which is also a DC measurement, is representative of the impedance of the pulldown stage in the device. In UCC2752x, the effective resistance of the hybrid pullup structure during turnon is estimated to be approximately 1.5 × $R_{OL}$, estimated based on design considerations.

Each output stage in UCC2752x can supply 5-A peak source and 5-A peak sink current pulses. The output voltage swings between $V_{DD}$ and GND providing rail-to-rail operation, thanks to the MOS-output stage which delivers very low drop-out. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky-diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

The UCC2752x devices are particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This situation is due to the extremely low drop-out offered by the MOS output stage of these devices, both during high ($V_{OH}$) and low ($V_{OL}$) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

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For applications that have zero voltage switching during power MOSFET turnon or turnoff interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

### *7.3.6 Low Propagation Delays and Tightly Matched Outputs*

The UCC2752x driver devices feature a best in class, 13-ns (typical) propagation delay between input and output which goes to offer the lowest level of pulse-transmission distortion available in the industry for high frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when one driver device is used to drive both the SR MOSFETs. Further, the driver devices also feature an extremely accurate, 1-ns (typ) matched internal-propagation delays between the two channels which is beneficial for applications requiring dual gate drives with critical timing. For example in a PFC application, a pair of paralleled MOSFETs may be driven independently using each output channel, which the inputs of both channels are driven by a common control signal from the PFC controller device. In this case the 1ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion with the minimum of turnon delay difference. Yet another benefit of the tight matching between the two channels is that the two channels are connected together to effectively increase current drive capability, for example A and B channels may be combined into one driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together. Then, one signal controls the paralleled combination.

Caution must be exercised when directly connecting OUTA and OUTB pins together because there is the possibility that any delay between the two channels during turnon or turnoff may result in shoot-through current conduction as shown in Figure 7-7. While the two channels are inherently very well matched (4-ns Max propagation delay), note that there may be differences in the input threshold voltage level between the two channels which causes the delay between the two outputs especially when slow dV/dt input signals are employed. TI recommends the following guidelines whenever the two driver channels are paralleled using direct connections between OUTA and OUTB along with INA and INB:

- Use very fast dV/dt input signals (20 V/µs or greater) on INA and INB pins to minimize impact of differences in input thresholds causing delays between the channels.
- INA and INB connections must be made as close to the device pins as possible.

Wherever possible, a safe practice would be to add an option in the design to have gate resistors in series with OUTA and OUTB. This allows the option to use 0-Ω resistors for paralleling outputs directly or to add appropriate series resistances to limit shoot-through current, should it become necessary.

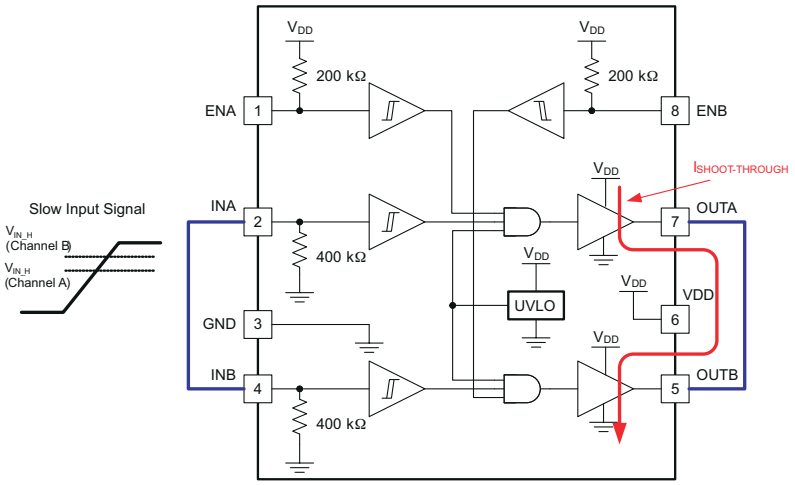


**Figure 7-7. Slow Input Signal May Cause Shoot-Through Between Channels During Paralleling (Recommended dV/dT is 20 V/Ms or Higher)**


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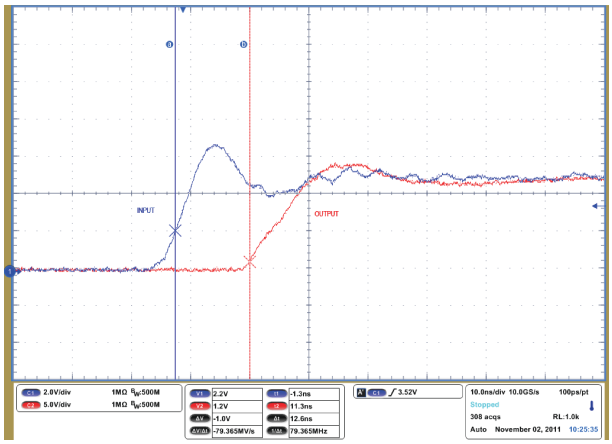


**Figure 7-8. Turnon Propagation Delay ($C_L$ = 1.8 nF, $V_{DD}$ = 12 V)**

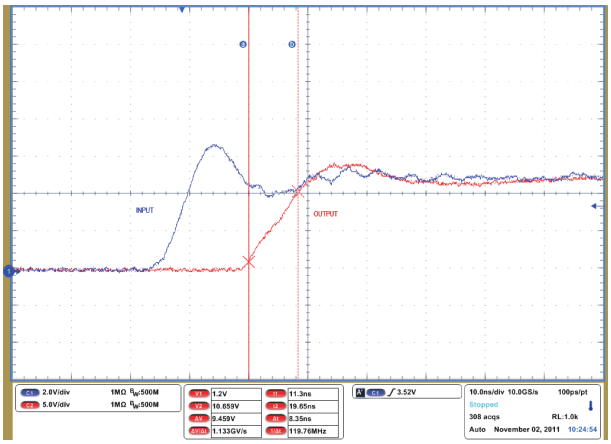


**Figure 7-9. Turnon Rise Time ($C_L$ = 1.8 nF, $V_{DD}$ = 12 V)**

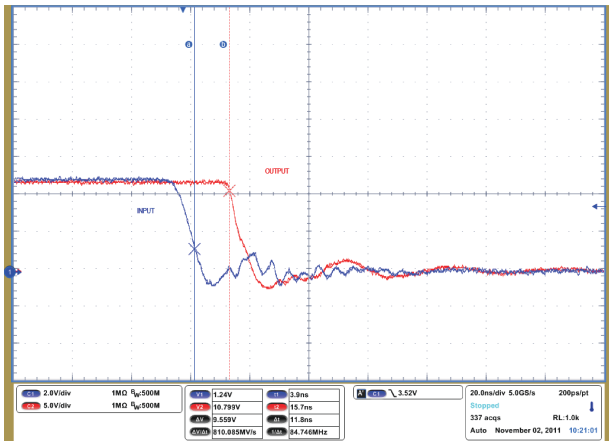


**Figure 7-10. Turnoff Propagation Delay ($C_L$ = 1.8 nF, $V_{DD}$ = 12 V)**

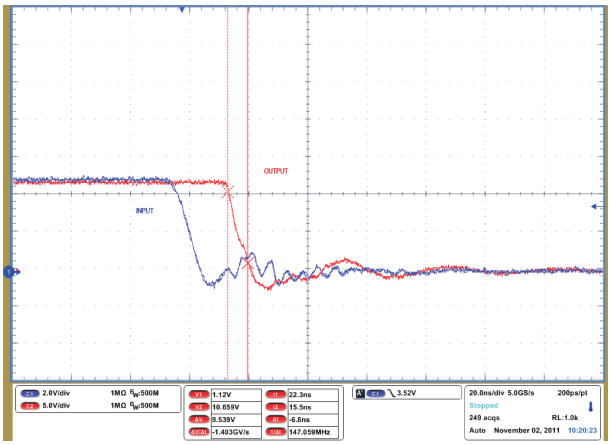


**Figure 7-11. Turnoff Fall Time ($C_L$ = 1.8 nF, $V_{DD}$ = 12 V)**

## 7.4 Device Functional Modes

**Table 7-2. Device Logic Table (UCC27523/5)**

| UCC27523/5 | | | | UCC27523 | | UCC27525 | |
|---|---|---|---|---|---|---|---|
| ENA | ENB | INA | INB | OUTA | OUTB | OUTA | OUTB |
| H | H | L | L | H | H | H | L |
| H | H | L | H | H | L | H | H |
| H | H | H | L | L | H | L | L |
| H | H | H | H | L | L | L | H |
| L | L | Any | Any | L | L | L | L |
| Any | Any | x(1) | x(1) | L | L | L | L |
| x(1) | x(1) | L | L | H | H | H | L |
| x(1) | x(1) | L | H | H | L | H | H |
| x(1) | x(1) | H | L | L | H | L | L |
| x(1) | x(1) | H | H | L | L | L | H |

(1) Floating condition.

**Table 7-3. Device Logic Table (UCC27526)**

| INx+ (x = A or B) | INx- (x = A or B) | OUTx (x = A or B) |
|---|---|---|
| L | L | L |
| L | H | L |
| H | L | H |
| H | H | L |
| x(1) | Any | L |
| Any | x(1) | L |

(1) x = Floating condition.


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching-power losses, a powerful gate-driver device employs between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate-driver devices are indispensable when having the PWM controller device directly drive the gates of the switching devices is sometimes not feasible. With advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter-follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller.

Finally, emerging wide band-gap power-device technologies such as GaN based switches, which can support very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include operation at low $V_{DD}$ voltages (5 V or lower), low propagation delays, tight delay matching and availability in compact, low-inductance packages with good thermal capability.

In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low-cost, component-count, board-space reduction, and simplified system design.

## 8.2 Typical Application

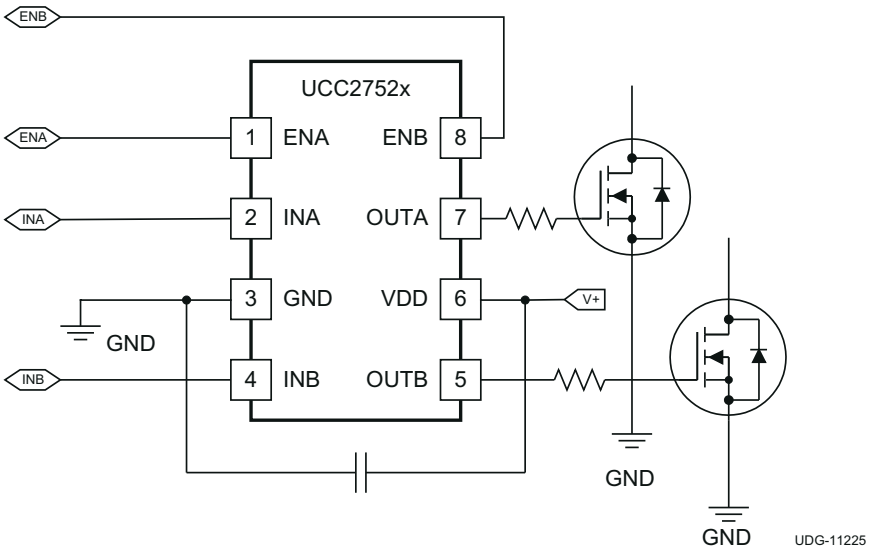


**Figure 8-1. UCC2752x Typical Application Diagram (x = 3, or 5)**

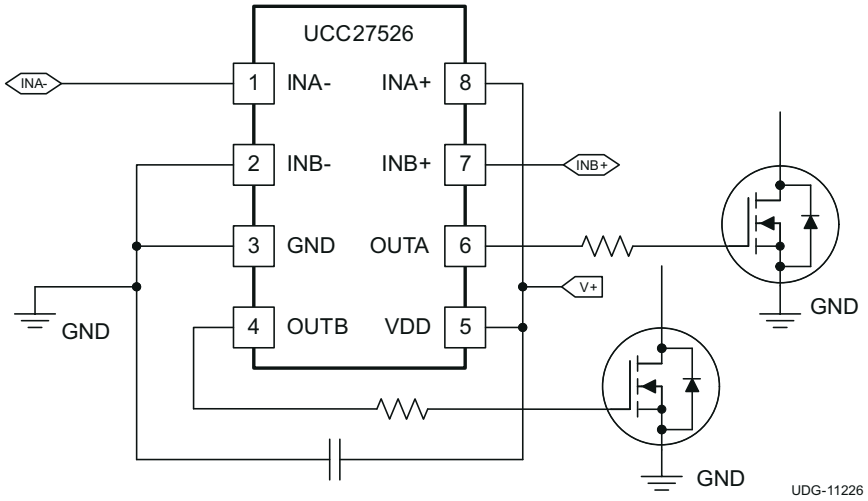


**Figure 8-2. UCC27526 Channel A in Inverting and Channel B in Non-Inverting Configuration (Enable Function Not Used)**

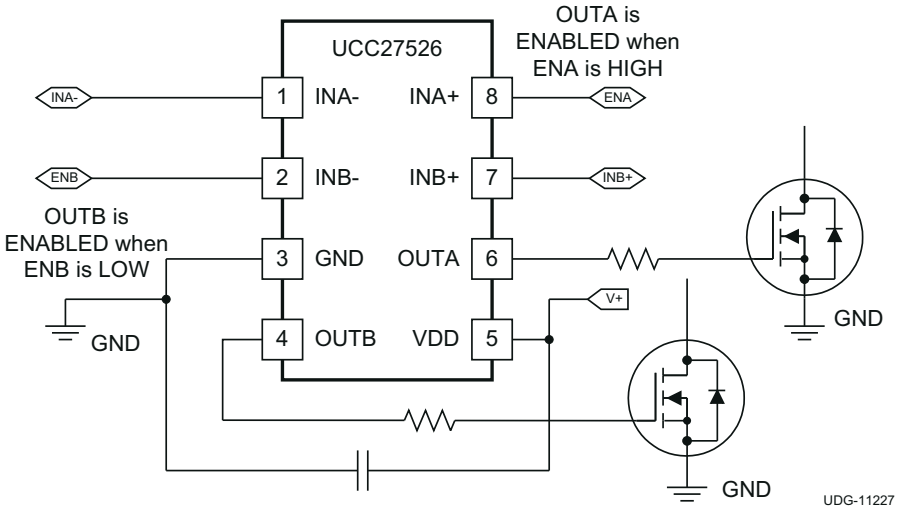


**Figure 8-3. UCC27526 Channel A in Inverting and Channel B in Non-Inverting Configuration (Enable Function Implemented)**

### *8.2.1 Design Requirements*

When selecting the proper gate-driver device for an end application, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are input-to-output logic, VDD, UVLO, Drive current and power dissipation.

### *8.2.2 Detailed Design Procedure*

#### 8.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. The UCC27523 device can provide dual inverting input to output with enable control. The UCC27525 device can provide one inverting and one non-inverting input to output control. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the non-inverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. UCC27526 has dual configuration channel. Each Channel of UCC27526 device can be configured in either an inverting or non-inverting input-to-output configuration using the INx– or INx+ pins respectively like in Figure 8-2 and Figure 8-3. To configure the channel for use in inverting mode, tie the INx+ pin to VDD and apply the input


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signal to the INx– pin. For the non-inverting configuration, tie the INx– pin to GND and apply the input signal to the INx+ pin.

#### 8.2.2.2 Enable and Disable Function

Certain applications demand independent control of the output state of the driver. The UCC27523/5 device offers two independent enable pins ENx for exclusive control of each driver channels as listed in Table 7-2.

The UCC27526 device does not feature dedicated enable pins. However, as mentioned earlier, an enable/disable function can be easily implemented in UCC27526 using the unused input pin. When INx+ is pulled-down to GND or INx– is pulled-down to VDD, the output is disabled as listed in Table 7-3. Thus INx+ pin can be used like an enable pin that is based on active high logic, while INx– can be used like an enable pin that is based on active low logic. It is important to note that while the ENA, ENB pins in the UCC27523/5 are allowed to be in floating condition during standard operation and the outputs will be enabled, the INx+, INx– pins in UCC27526 are not allowed to be floating because this will disable the outputs.

#### 8.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the Section 6.3. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC2752x device can be used to drive a variety of power switches, such as Si MOSFETs (for example, VGS = 4.5 V, 10 V, 12 V), IGBTs (VGE = 15 V, 18 V).

#### 8.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2752x device features fast 13-ns (typical) propagation delays which ensures very little pulse distortion and allows operation at very high-frequencies. See Section 6.6 for the propagation and switching characteristics of the UCC2752x device.

#### 8.2.2.5 Drive Current and Power Dissipation

The UCC27523/5/6 family of drivers are capable of delivering 5-A of current to a MOSFET gate for a period of several-hundred nanoseconds at $V_{DD}$ = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating frequency of the power device. The power dissipated in the gate-driver device package depends on the following factors:

- Gate charge required of the power MOSFET (usually a function of the drive voltage $V_{GS}$, which is very close to input bias supply voltage $V_{DD}$ due to low $V_{OH}$ drop-out)
- Switching frequency
- Use of external gate resistors

Because UCC2752x features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 1.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{1}$$

where

- $C_{LOAD}$ is load capacitor
- $V_{DD}$ is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 2.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{2}$$

where

- $f_{SW}$ is the switching frequency

With $V_{DD}$ = 12 V, $C_{LOAD}$ = 10 nF and $f_{SW}$ = 300 kHz the power loss is calculated as (see Equation 3):

$$P_G = 10\,nF \times 12\,V^2 \times 300\,kHz = 0.432\,W \tag{3}$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge $Q_g$, the power that must be dissipated when charging a capacitor is determined which by using the equivalence $Q_g = C_{LOAD}V_{DD}$ to provide Equation 4 for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

Assuming that UCC2752x is driving power MOSFET with 60 nC of gate charge ($Q_g$ = 60 nC at $V_{DD}$ = 12 V) on each output, the gate charge related power loss is calculated as (see Equation 5):

$$P_G = 2\,x\,60\,nC \times 12\,V \times 300\,kHz = 0.432\,W \tag{5}$$

This power PG is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows (see Equation 6):

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left( \frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \tag{6}$$

where

- $R_{OFF} = R_{OL}$
- $R_{ON}$ (effective resistance of pullup structure) = 1.5 x $R_{OL}$


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In addition to the above gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in Figure 6-6, the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation is calculated easily with Equation 7.

$$P_Q = I_{DD} V_{DD} \tag{7}$$

Assuming , $I_{DD}$ = 6 mA, the power loss is:

$$P_Q = 0.6\ \text{mA} \times 12\ \text{V} = 7.2\ \text{mW} \tag{8}$$

Clearly, this power loss is insignificant compared to gate charge related power dissipation calculated earlier.

With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432\ \text{W}}{12\ \text{V}} = 0.036\ \text{A} \tag{9}$$

### *8.2.3 Application Curves*

Figure 8-4 and Figure 8-5 show the typical switching characteristics of the non-inverting input driver operation for UCC27523/5/6 device. $C_L$ = 1.8 nF, $V_{DD}$ = 12 V.

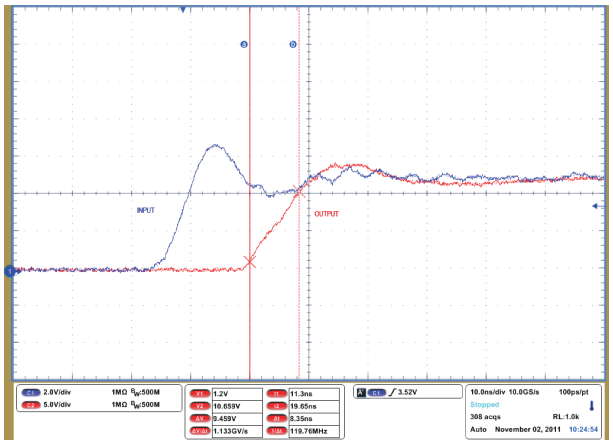


**Figure 8-4. Typical Turnon Waveform**

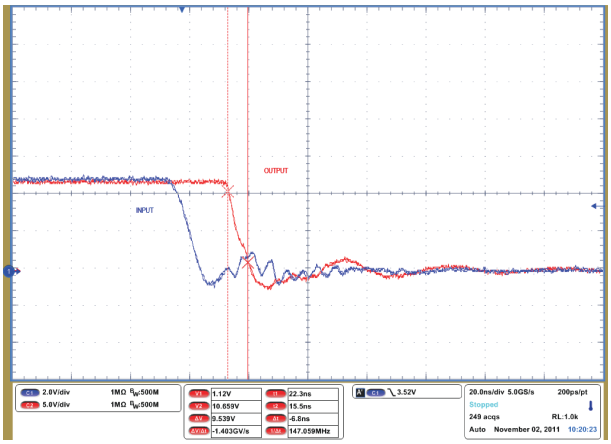


**Figure 8-5. Typical Turnoff Waveform**

## 9 Power Supply Recommendations

The bias supply voltage range for which the UCC2752X device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the VON supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the VDD pin bias voltage has exceeded the threshold voltage, device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification VDD_H. Therefore, ensuring that, while operating at or near the 4.2-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VOFF threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the VDD pin voltage has exceeded above the VON threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. It is important to recognize that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same VDD pin. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus ensuring that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends having two capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.


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# 10 Layout

## 10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27523/5/6 family of gate drivers incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate voltage transitions very quickly. At higher $V_{DD}$ voltages, the peak current capability is even higher (5-A peak current is at $V_{DD}$ = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. TI strongly recommends the following circuit layout guidelines when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the Output pins and the Gate of the power device.
- Locate the $V_{DD}$ bypass capacitors between $V_{DD}$ and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from $V_{DD}$ during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current loop paths (driver device, power MOSFET and $V_{DD}$ bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at 2 instances during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- In noisy environments, tying inputs of an unused channel of UCC27526 to $V_{DD}$ (in case of INx+) or GND (in case of INX–) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.
- Exercise caution when replacing the UCC2732x/UCC2742x devices with the UCC2752x:
  - UCC2752x is a much stronger gate driver (5-A peak current versus 4-A peak current).
  - UCC2752x is a much faster gate driver (13-ns/13-ns rise/fall propagation delay versus 25-ns/35-ns rise/fall propagation delay).

## 10.2 Layout Example

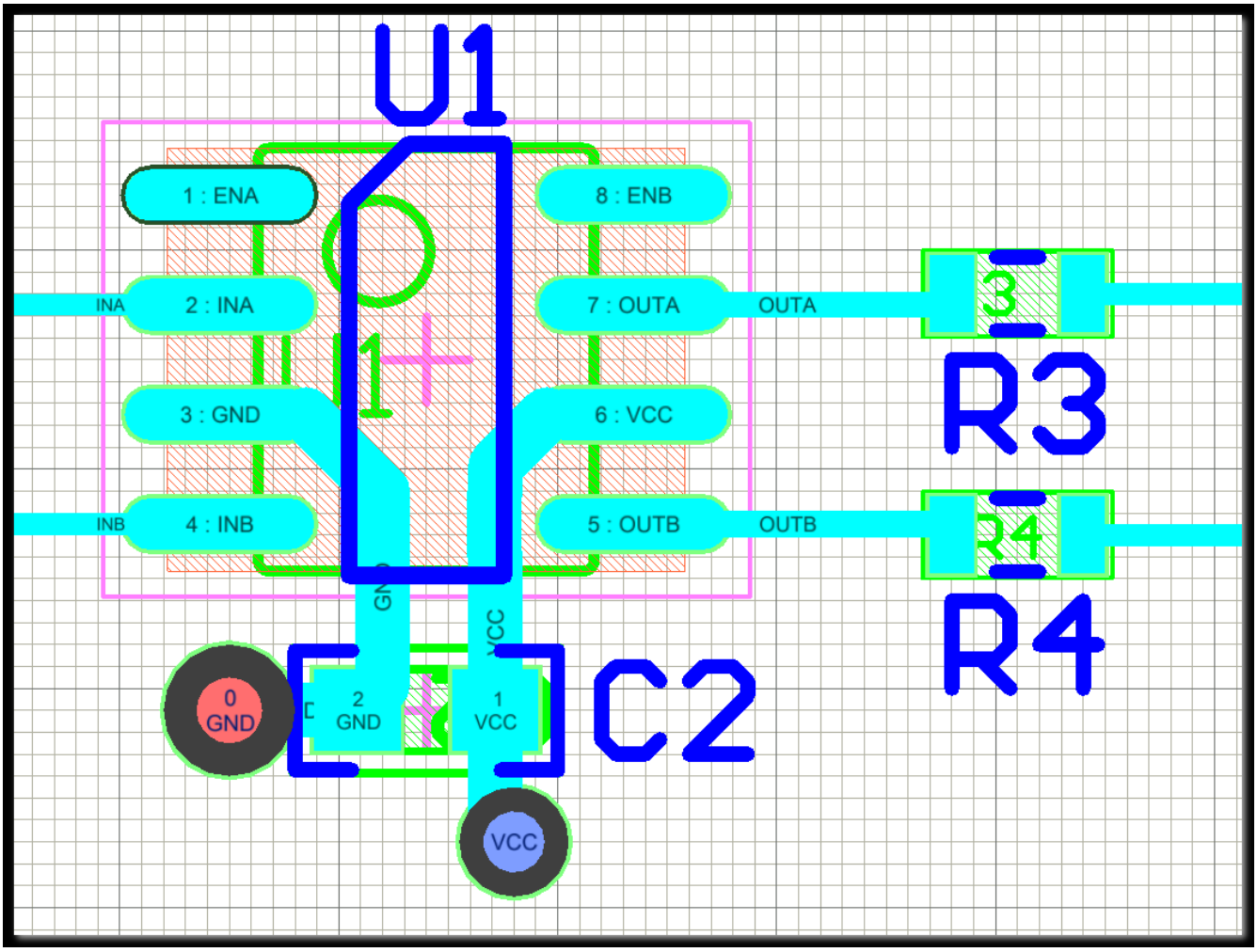


**Figure 10-1. Layout Example for UCC27523/5 (D, DGN)**

## 10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate-driver device to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC27523/5/6 family of drivers is available in four different packages to cover a range of application requirements. The thermal metrics for each of these packages are summarized in Section 6.4. For detailed information regarding the thermal information table, refer to Application Note from Texas Instruments entitled, *IC Package Thermal Metrics* (SPRA953).

Among the different package options available in the UCC2752x family, of particular mention are the DSD and DGN packages when it comes to power dissipation capability. The MSOP PowerPAD-8 (DGN) package and 3-mm × 3-mm WSON (DSD) package offer a means of removing the heat from the semiconductor junction through the bottom of the package. Both these packages offer an exposed thermal pad at the base of the package. This pad is soldered to the copper on the printed-circuit-board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over that available in the D packages. The printed-circuit-board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the MSOP-8 (PowerPAD) and WSON-8 packages are not directly connected to any leads of the package, however, it is electrically and thermally


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connected to the substrate of the device which is the ground of the device. TI recommends to externally connect the exposed pads to GND in PCB layout for better EMI immunity.

# 11 Device and Documentation Support

## 11.1 Device Support

### *11.1.1 Third-Party Products Disclaimer*

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## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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TI E2E™ is a trademark of Texas Instruments.
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## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |


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## 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision G (April 2015) to Revision H (June 2024)** **Page**

- Deleted the UCC27524 throughout the data sheet, changed the package in the device information table from SOT-23 to SOIC. 1
- Changed package from SOT-23 to SOIC-8. 4

**Changes from Revision F (May, 2013) to Revision G (April, 2015)** **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed UCC2752X Gate Driver Output Structure image. 17

**Changes from Revision E (June 2012) to Revision F (May 2013)** **Page**

- Added 0.5 to $P_{SW}$ equation in *Drive Current and Power Dissipation* section. 23

**Changes from Revision D (April 2012) to Revision E (June 2012)** **Page**

- Added OUTA, OUTB voltage field and values. 6
- Changed table note from "Values are verified by characterization and are not production tested." to "Values are verified by characterization on bench.". 6
- Added note, "Values are verified by characterization and are not production tested.". 6
- Changed Switching Time $t_{PW}$ values from 10 ns and 25 ns to 15 ns and 25 ns ns. 7
- Changed Functional Block Diagrams images. 12
- Changed Slow Input Signal Figure 33. 18

**Changes from Revision C (March 2012) to Revision D (April 2012)** **Page**

- Changed Inputs (INA, INB, INA+, INA–, INB+, INB-) section to include UCC2752X (D, DGN, DSD) information. 7
- Added Inputs (INA, INB, INA+, INA-, INB+, INB-) UCC27524P ONLY section. 7
- Changed Enable (ENA, ENB) section to include UCC2752X (D, DGN, DSD) information. 7
- Added ENABLE (ENA, ENB) UCC27524P ONLY section. 7

**Changes from Revision B ( December 2011) to Revision C ( March 2012)** **Page**

- Added $R_{OH}$ note in the Outputs (OUTA, OUTB) section. 7
- Added an updated Output Stage section. 17
- Added UCC2752X Gate Driver Output Structure image. 17
- Added an updated Low Propagation Delays and Tightly Matched Outputs section. 18
- Added Slow Input Signal Combined with Differences in Input Threshold Voltage image. 18
- Added updated Drive Current and Power Dissipation section. 23
- Added a PSW... equation. 23

| Changes from Revision A (November 2011) to Revision B (December 2011) | Page |
|---|---|
| • Changed Supply start threshold row to include two temperature ranges | 7 |
| • Changed Minimum operating voltage after supply start min and max values from 3.6 V to 4.2 V to 3.40 V and 4.40 V | 7 |
| • Changed Supply voltage hysteresis typ value from 0.35 to 0.30 | 7 |
| • Changed UCC27526 Block Diagram drawing | 12 |
| • Changed UCC27526 Channel A in Inverting and Channel B in Non-Inverting Configuration drawing | 21 |

| Changes from Revision * (November 2011) to Revision A (November 2011) | Page |
|---|---|
| • Changed data sheet status to Production Data | 1 |

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCC27523D | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523D.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523D.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DGN | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DGN.A | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DGN.B | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DGNR | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DGNR.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DGNR.B | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DRG4 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DRG4.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DRG4.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27523 |
| UCC27523DSDR | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDR.A | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDR.B | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDT | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDT.A | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDT.B | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDTG4 | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDTG4.A | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27523DSDTG4.B | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27523 |
| UCC27525D | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525D.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525D.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DG4 | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DG4.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCC27525DG4.B | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DGN | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DGN.A | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DGN.B | Active | Production | HVSSOP (DGN) \| 8 | 80 \| TUBE | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DGNR | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DGNR.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DGNR.B | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DR.B | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 140 | 27525 |
| UCC27525DSDR | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDR.A | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDR.B | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDRG4 | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDRG4.A | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDRG4.B | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDT | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDT.A | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27525DSDT.B | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | 27525 |
| UCC27526DSDR | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | SCB |
| UCC27526DSDR.A | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | SCB |
| UCC27526DSDR.B | Active | Production | SON (DSD) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | SCB |
| UCC27526DSDT | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | SCB |
| UCC27526DSDT.A | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | SCB |
| UCC27526DSDT.B | Active | Production | SON (DSD) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 140 | SCB |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

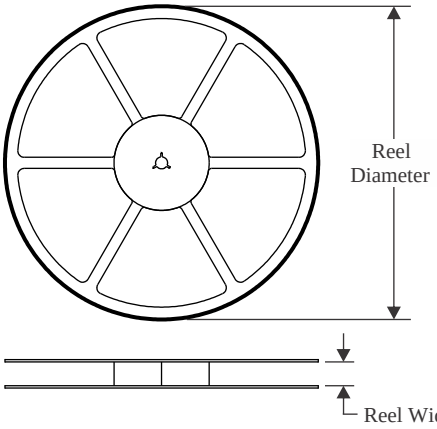
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

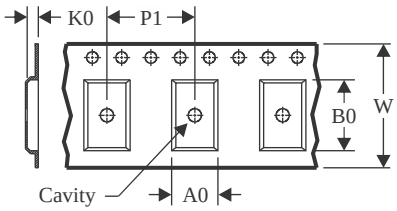
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

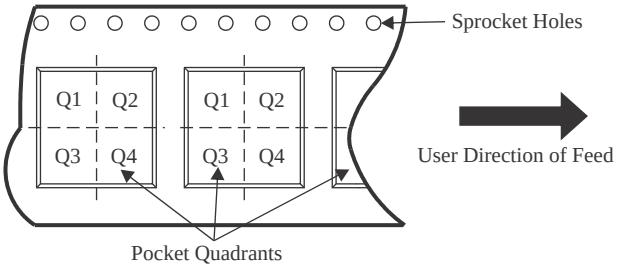



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

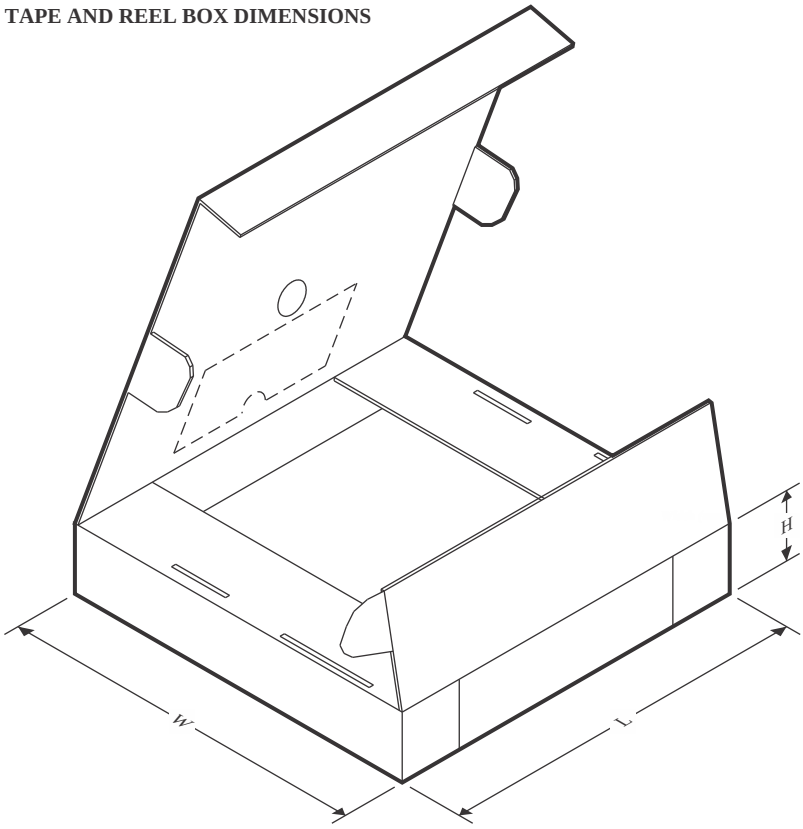



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC27523DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| UCC27523DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UCC27523DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UCC27523DSDR | SON | DSD | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27523DSDR | SON | DSD | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27523DSDT | SON | DSD | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27523DSDT | SON | DSD | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27523DSDTG4 | SON | DSD | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27523DSDTG4 | SON | DSD | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27525DGNR | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| UCC27525DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| UCC27525DSDR | SON | DSD | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27525DSDRG4 | SON | DSD | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27525DSDT | SON | DSD | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27526DSDR | SON | DSD | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27526DSDR | SON | DSD | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC27526DSDT | SON | DSD | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCC27526DSDT | SON | DSD | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

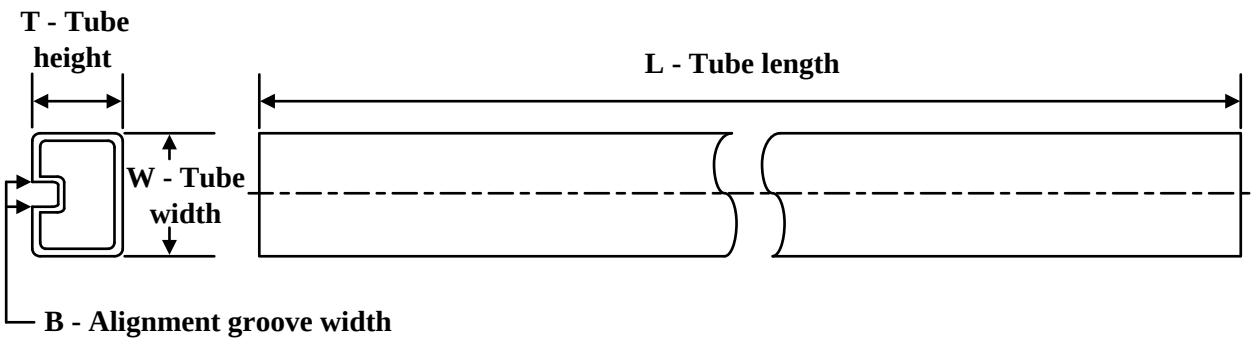
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC27523DGNR | HVSSOP | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| UCC27523DR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| UCC27523DRG4 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| UCC27523DSDR | SON | DSD | 8 | 3000 | 346.0 | 346.0 | 33.0 |
| UCC27523DSDR | SON | DSD | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| UCC27523DSDT | SON | DSD | 8 | 250 | 210.0 | 185.0 | 35.0 |
| UCC27523DSDT | SON | DSD | 8 | 250 | 210.0 | 185.0 | 35.0 |
| UCC27523DSDTG4 | SON | DSD | 8 | 250 | 210.0 | 185.0 | 35.0 |
| UCC27523DSDTG4 | SON | DSD | 8 | 250 | 210.0 | 185.0 | 35.0 |
| UCC27525DGNR | HVSSOP | DGN | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| UCC27525DR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |
| UCC27525DSDR | SON | DSD | 8 | 3000 | 346.0 | 346.0 | 33.0 |
| UCC27525DSDRG4 | SON | DSD | 8 | 3000 | 346.0 | 346.0 | 33.0 |
| UCC27525DSDT | SON | DSD | 8 | 250 | 210.0 | 185.0 | 35.0 |
| UCC27526DSDR | SON | DSD | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| UCC27526DSDR | SON | DSD | 8 | 3000 | 346.0 | 346.0 | 33.0 |
| UCC27526DSDT | SON | DSD | 8 | 250 | 210.0 | 185.0 | 35.0 |
| UCC27526DSDT | SON | DSD | 8 | 250 | 210.0 | 185.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| UCC27523D | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27523D.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27523D.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27523DGN | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| UCC27523DGN.A | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| UCC27523DGN.B | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| UCC27525D | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27525D.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27525D.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27525DG4 | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27525DG4.A | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27525DG4.B | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |
| UCC27525DGN | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| UCC27525DGN.A | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |
| UCC27525DGN.B | DGN | HVSSOP | 8 | 80 | 330 | 6.55 | 500 | 2.88 |

# GENERIC PACKAGE VIEW

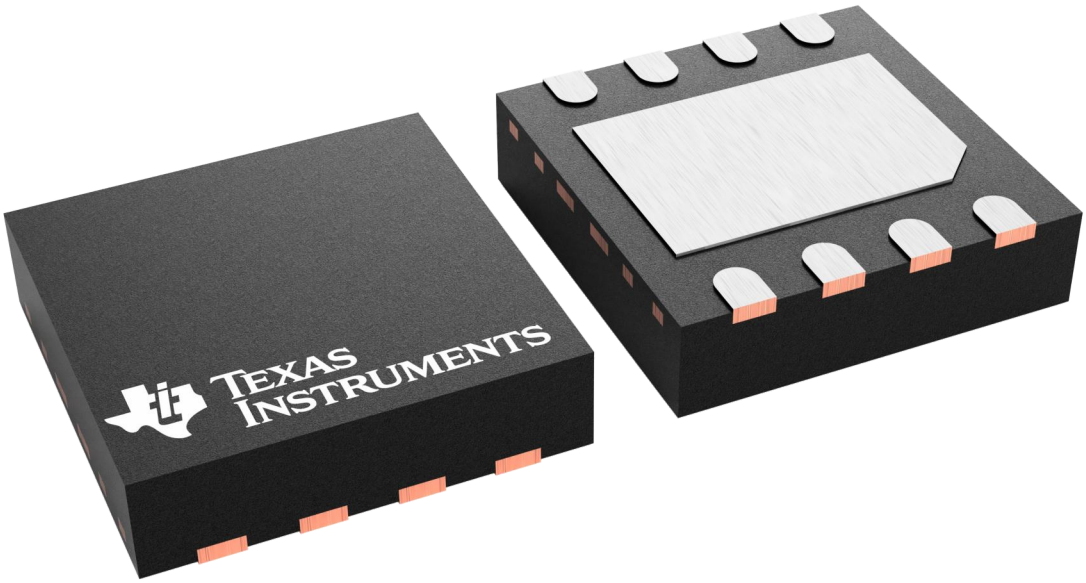
## DSD 8

## WSON - 0.8 mm max height

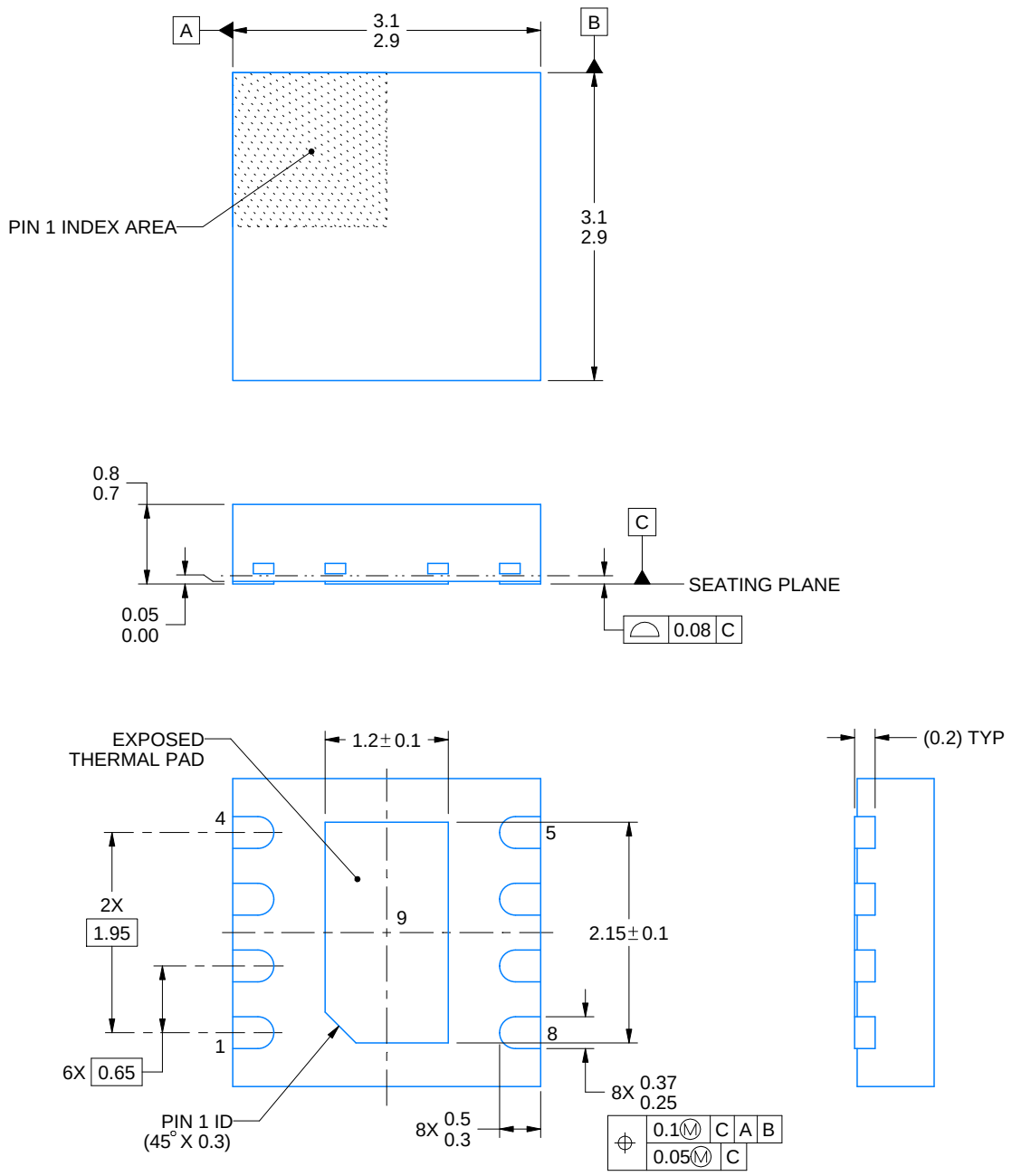
**3 X 3, 0.8 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



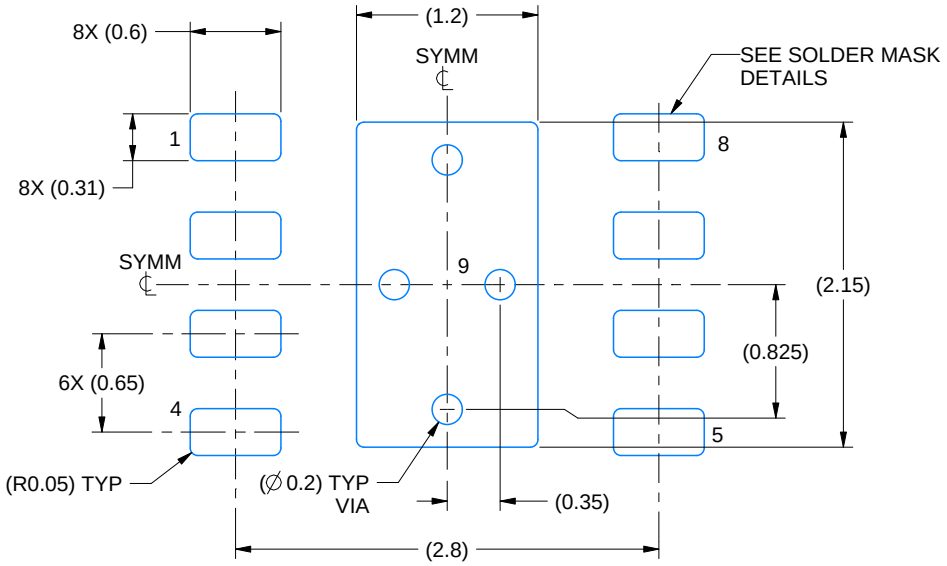

4227007/A



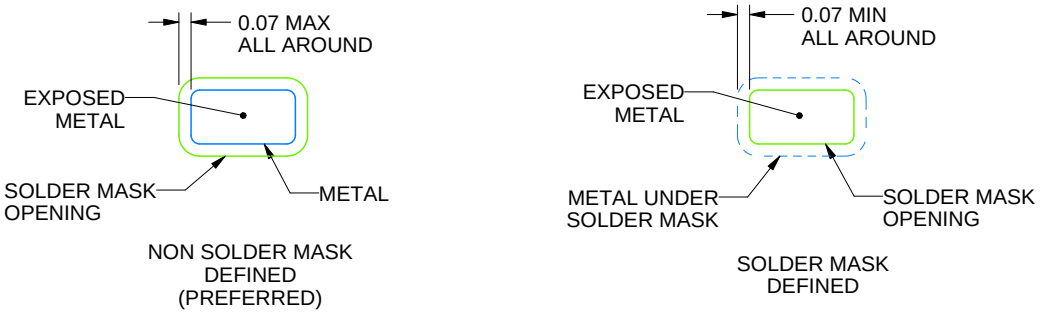

4218899/A 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

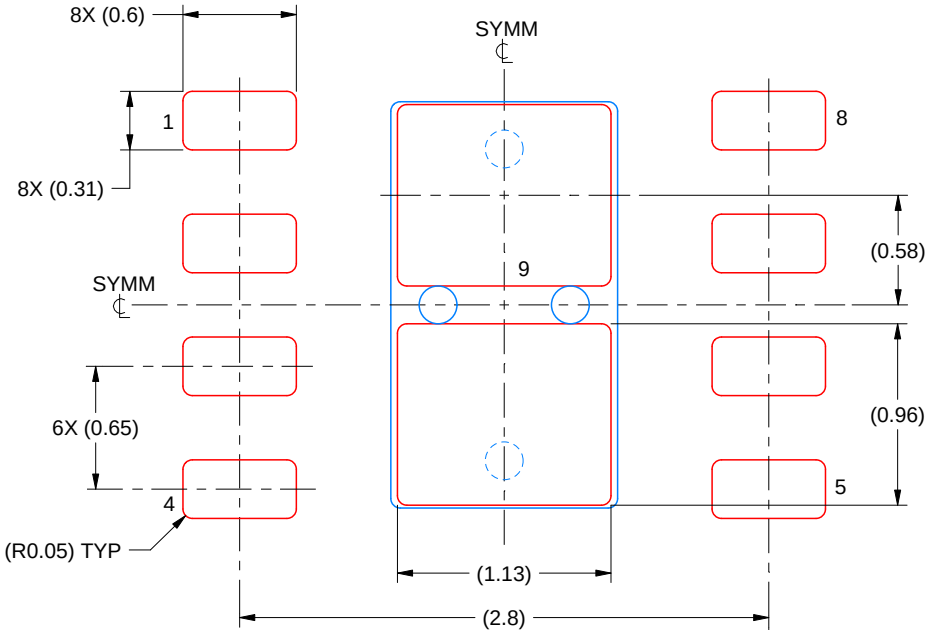



SOLDER MASK DETAILS

4218899/A 09/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218899/A 09/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# GENERIC PACKAGE VIEW

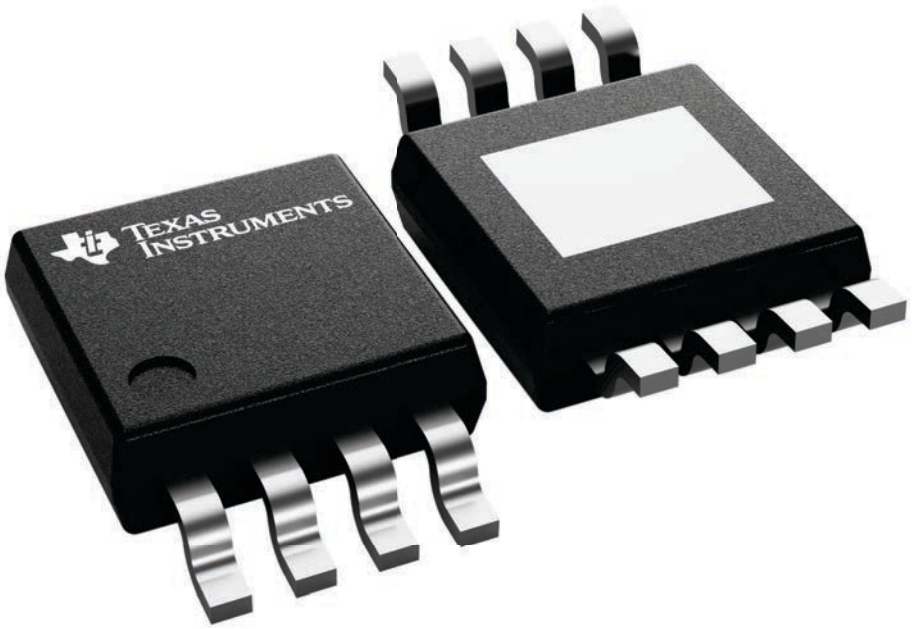
## DGN 8

## PowerPAD™ HVSSOP - 1.1 mm max height

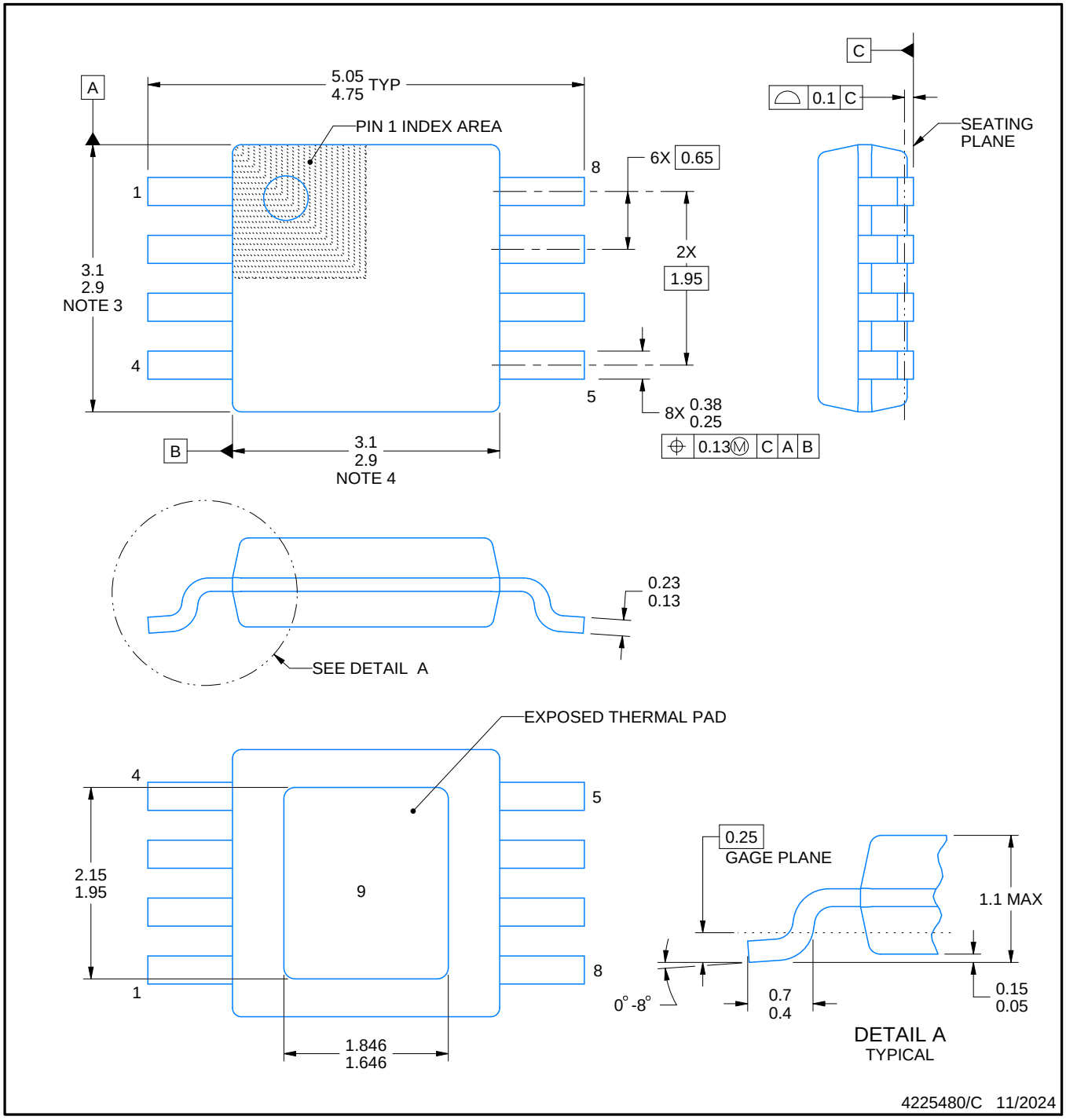
**3 x 3, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



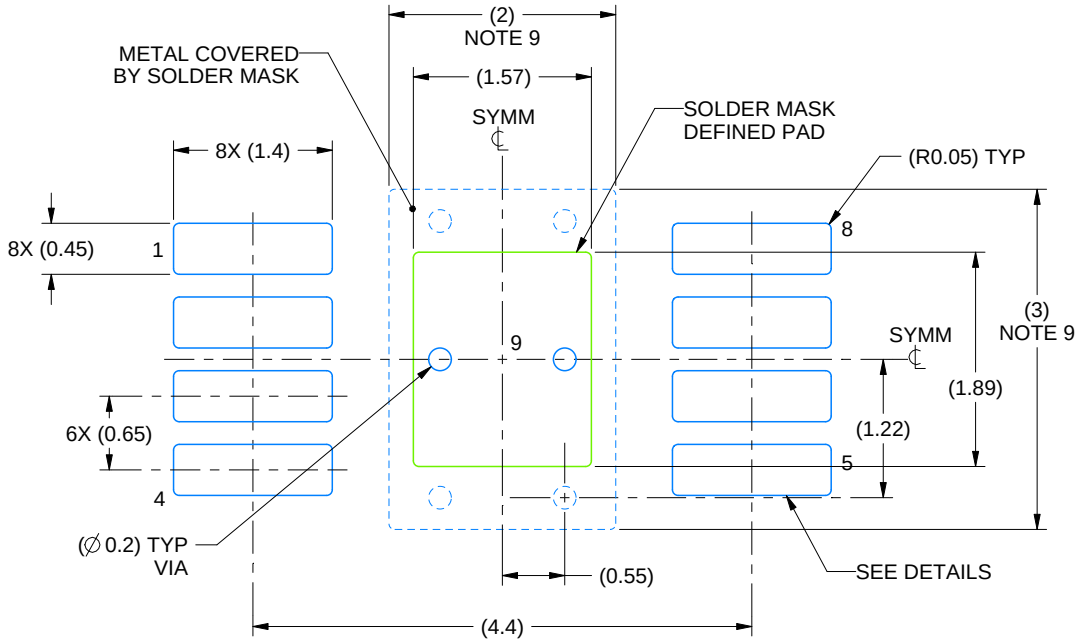

4225482/B



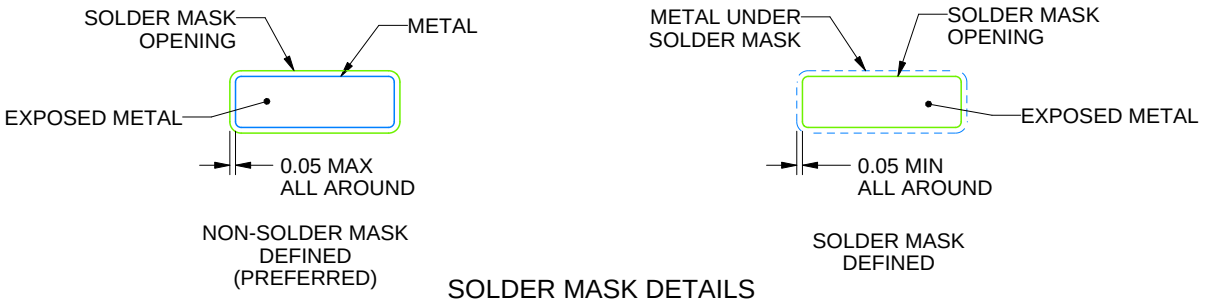

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

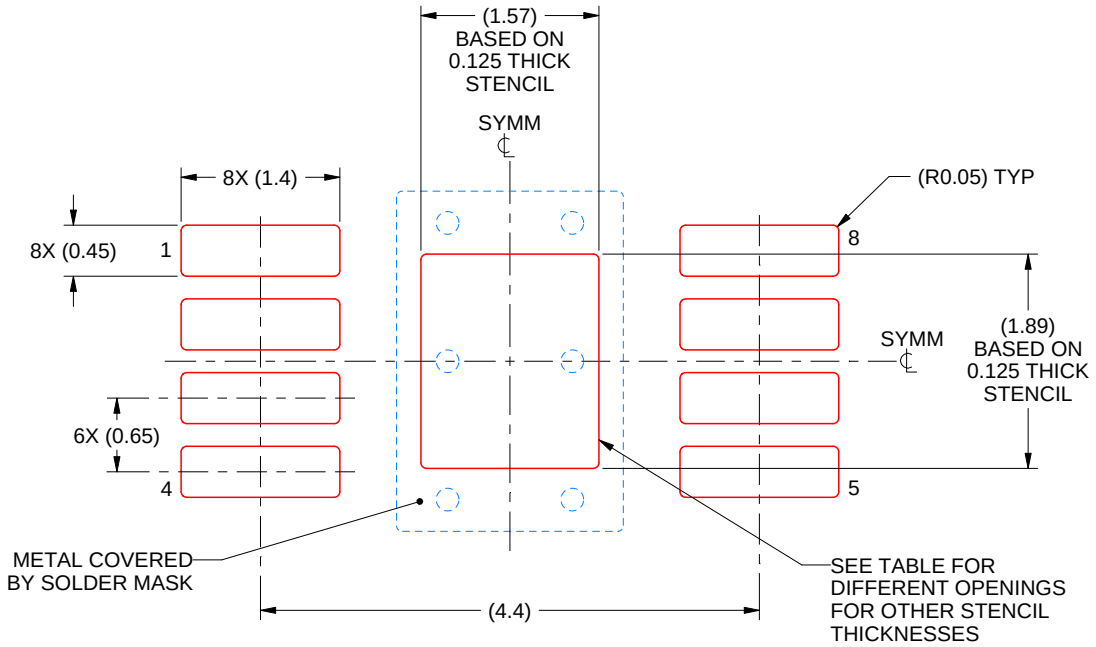



SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



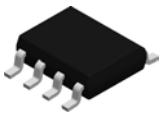

SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.76 X 2.11 |
| 0.125 | 1.57 X 1.89 (SHOWN) |
| 0.15 | 1.43 X 1.73 |
| 0.175 | 1.33 X 1.60 |

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

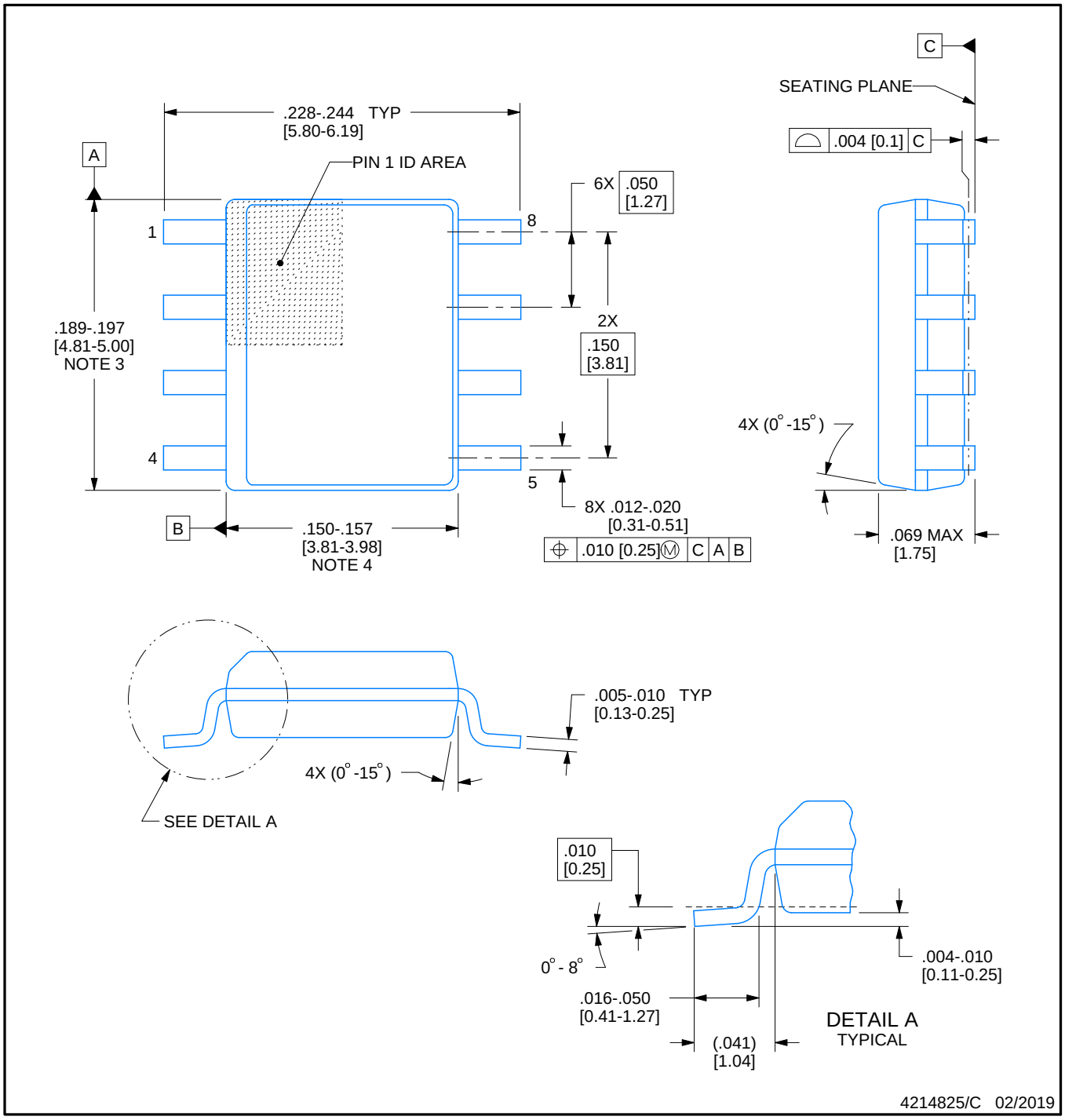


# PACKAGE OUTLINE

## D0008A

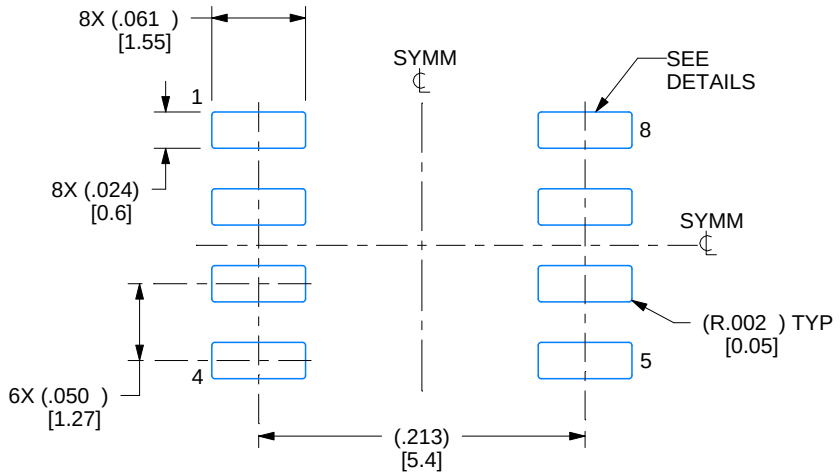
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

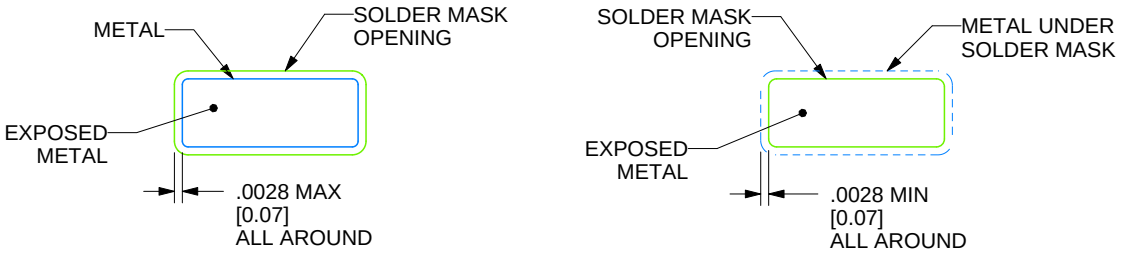



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

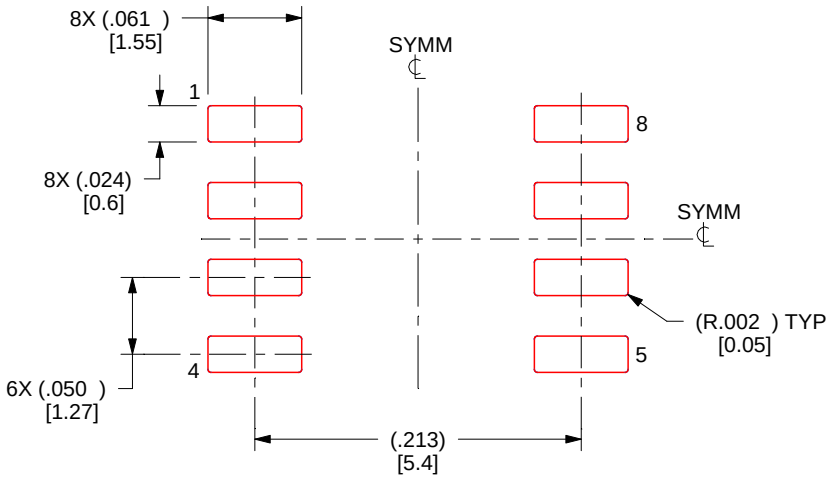



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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